SuperBigBite DAQ update

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Jefferson Lab

SBS DOE Review – November 2015

Outline

- SBS requirements
  - *Data Event Flow*
- Fastbus Readout
  - *Event Switching*
- FADC HCAL readout
- GEM readout
- Timeline
- Manpower

G_E^p DAQ requirements

- Focal Plane Polarimeter
  - Front tracker
  - Back tracker GEM 128 K channels
  - 288 channels HCAL on FADC (10 samples)
- Electron detector
  - 1800 channels ECAL
  - CDet 2152 Channels (TDC)

G_E^p event size (after deconvolution)

Detector	Channels	Single rate Hz	Occupancy 75 ns in %	Channels firing	Event size (bytes)	Data rate 5 KHz MB/s
Front tracker	41,000	3.3e9	18.1	7430	136,000	90
Back tracker	112,640	3.36e9	22.4	12600	230,000	150
HCal	288	_	100	288	7,200	36
ECAL	1800 + 225	_	100	2025	8,100	45
CDET	2152	_	10	216	864	4.3
Total						325.3 MB/s

Includes geometrical matching

HCAL and ECAL occupancies need to be evaluated : using 100 % for now

G_E^n, G_M^n DAQ requirements

- Bigbite
  - GEM 128 K channels
  - Shower 189 blocks (ADC)
  - Preshower 54 blocks (ADC)
  - Scintillator 180 bars 360 PMTs (ADC/TDC)
  - Cerenkov 550 PMTs (TDC)

- Neutron detector
  - 288 channels HCAL (FADC + high res TDC)
  - CDet 2152 Channels (TDC)

G_E^n, G_M^n event size (after deconvolution)

Arm	Detector	Channels	Single rate Hz	Occupancy 75 ns in %	Channels firing	Event size (bytes)	Data rate 5 KHz MB/s
BigBite	GEM	112,640	2.6e9	8.7	5248	62,976	300
	Lead glass	243	_	100	243	1003	5
	Scintillators	360	_	100	360	1485	7.4
	Cerenkov	550	_	100	550	2269	11.34
Neutron	HCal	288	_	100	288	7,200	36
	HCAL time	288	_	100	288	1170	5.85
	CDET	2152	_	10	216	864	4.3

Total at 5 KHz 370 MB/s Max

Fastbus update

- Use new CODA 3.0 TI and TS
  - More flexibility in programming
  - Event blocking
  - Absolute timestamp for synchronization check
  - Trigger partitioning capability only use a subset of modules
- Asked for modified firmware to DAQ group in May 2015 (William Gu and Bryan Moffit)
- Firmware being developed and tested

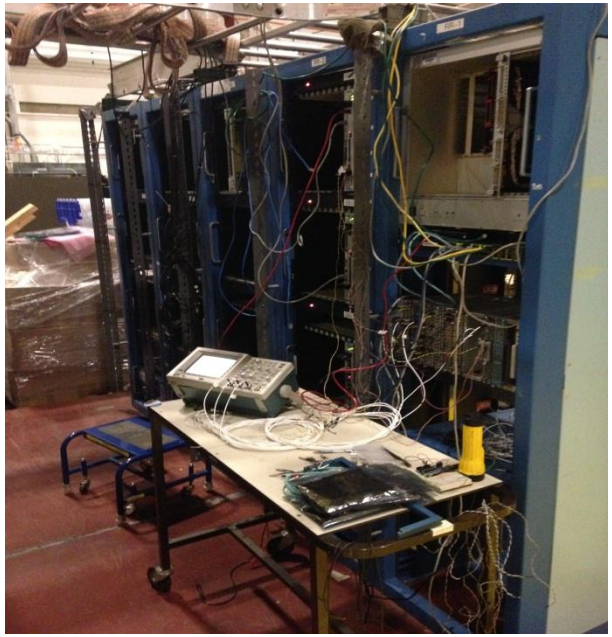
Fastbus update

- Have sufficient TDCs, ADCs, crates, SFI, aux. cards

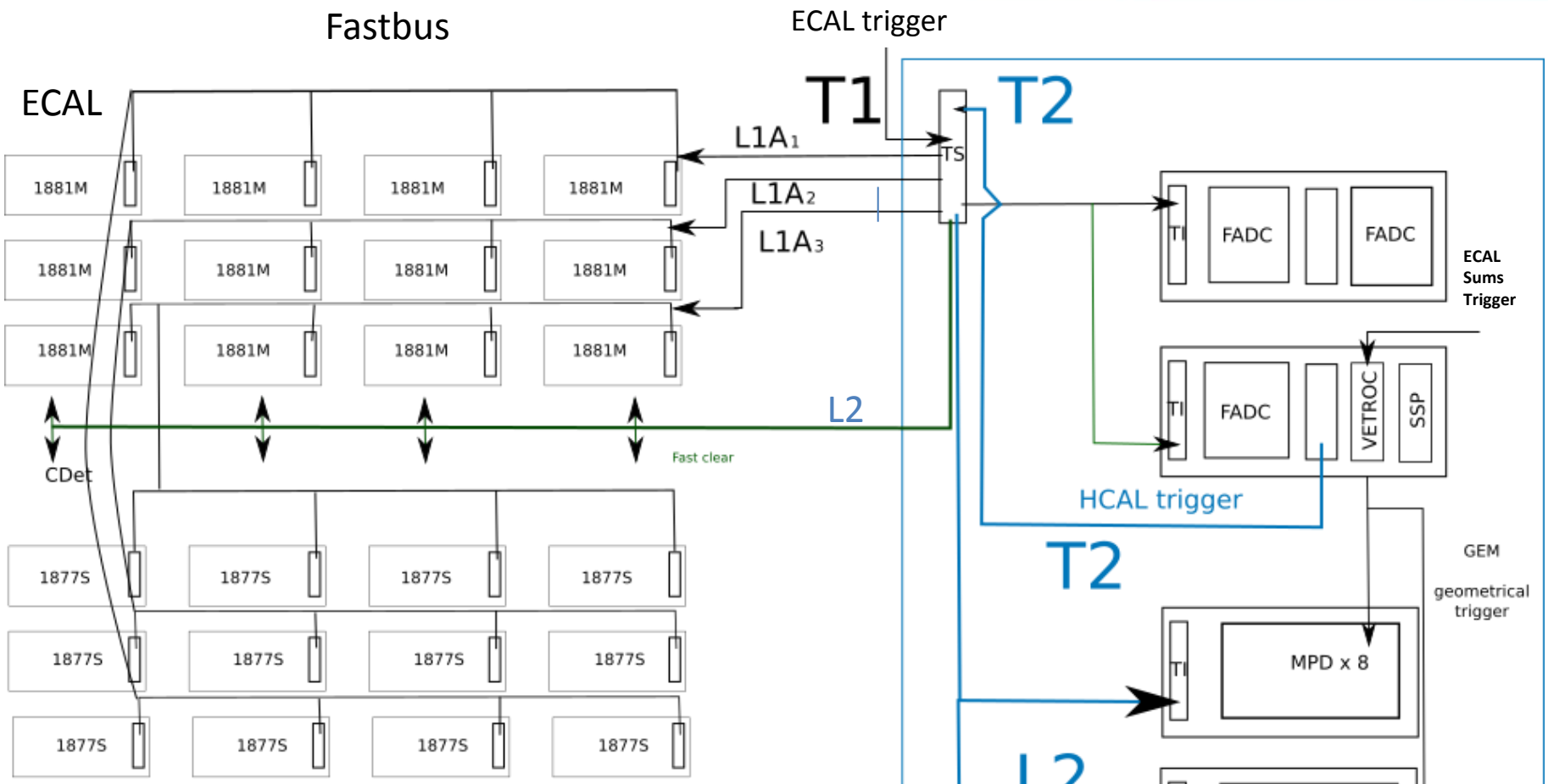
TDCs	ADCs	crates	SFI	aux. cards
have 236 need 124	have 113 need 94	have 30 need 21	have 21 need 21	have 15 (20 being made) need 30

- Making FB faster
  - sparsification – works
  - event blocking – works
  - event switching – being tested
  - merging with pipelining VME – to be tried

- Three large Fastbus systems assembled in the test lab.



G_E^p DAQ Configuration / both arms

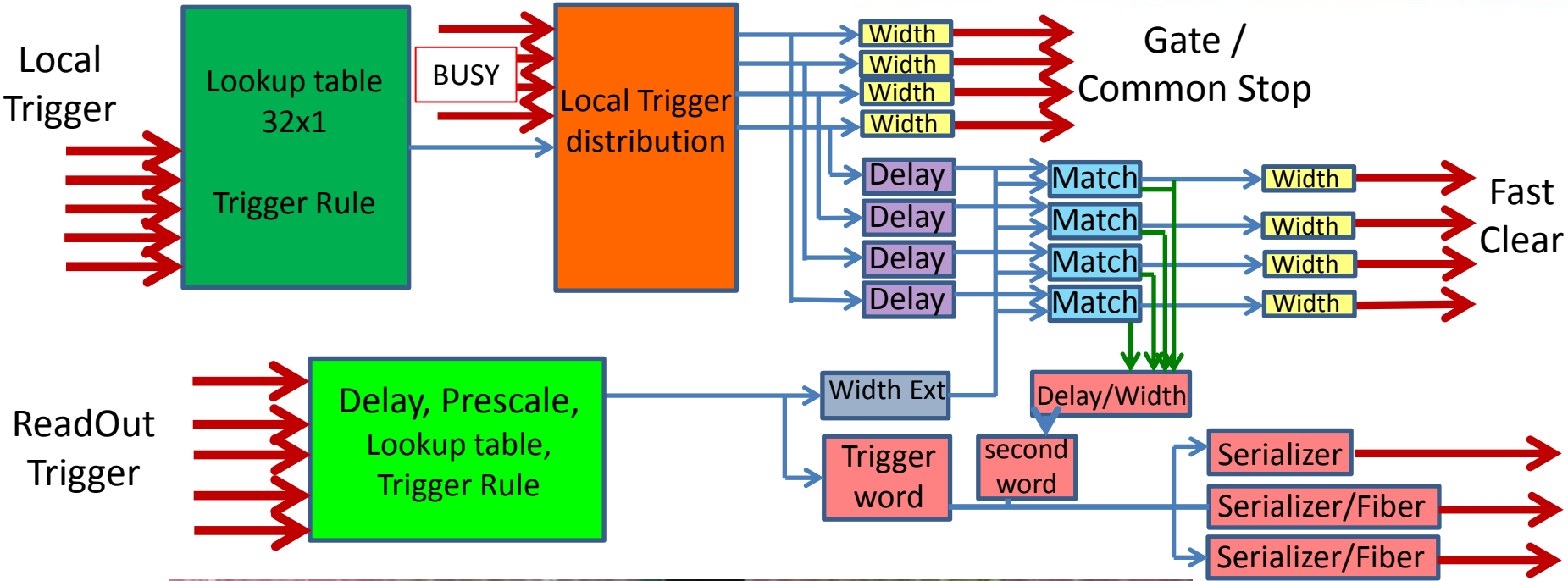


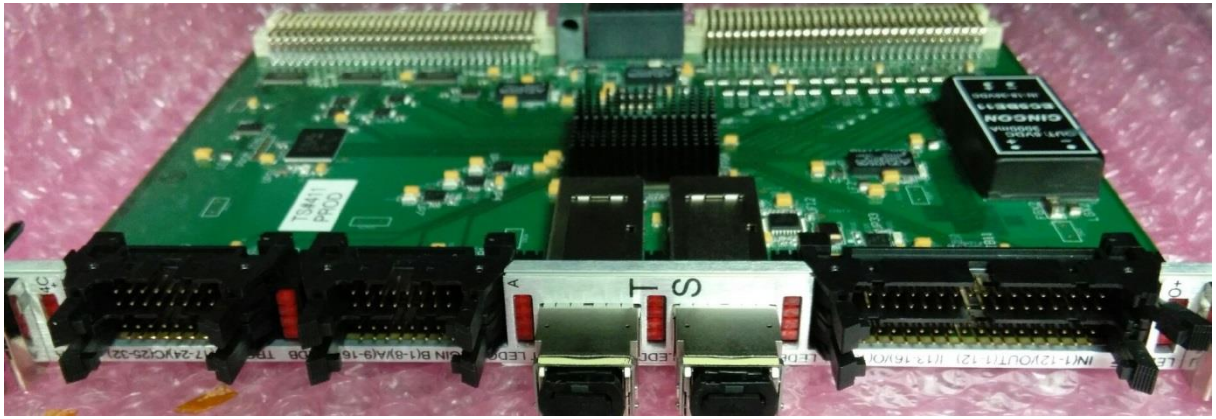
T2 distributed to Hadron and Electron Arms

If no L2A, Fast Clear to Fastbus

TI provides timestamp for every event

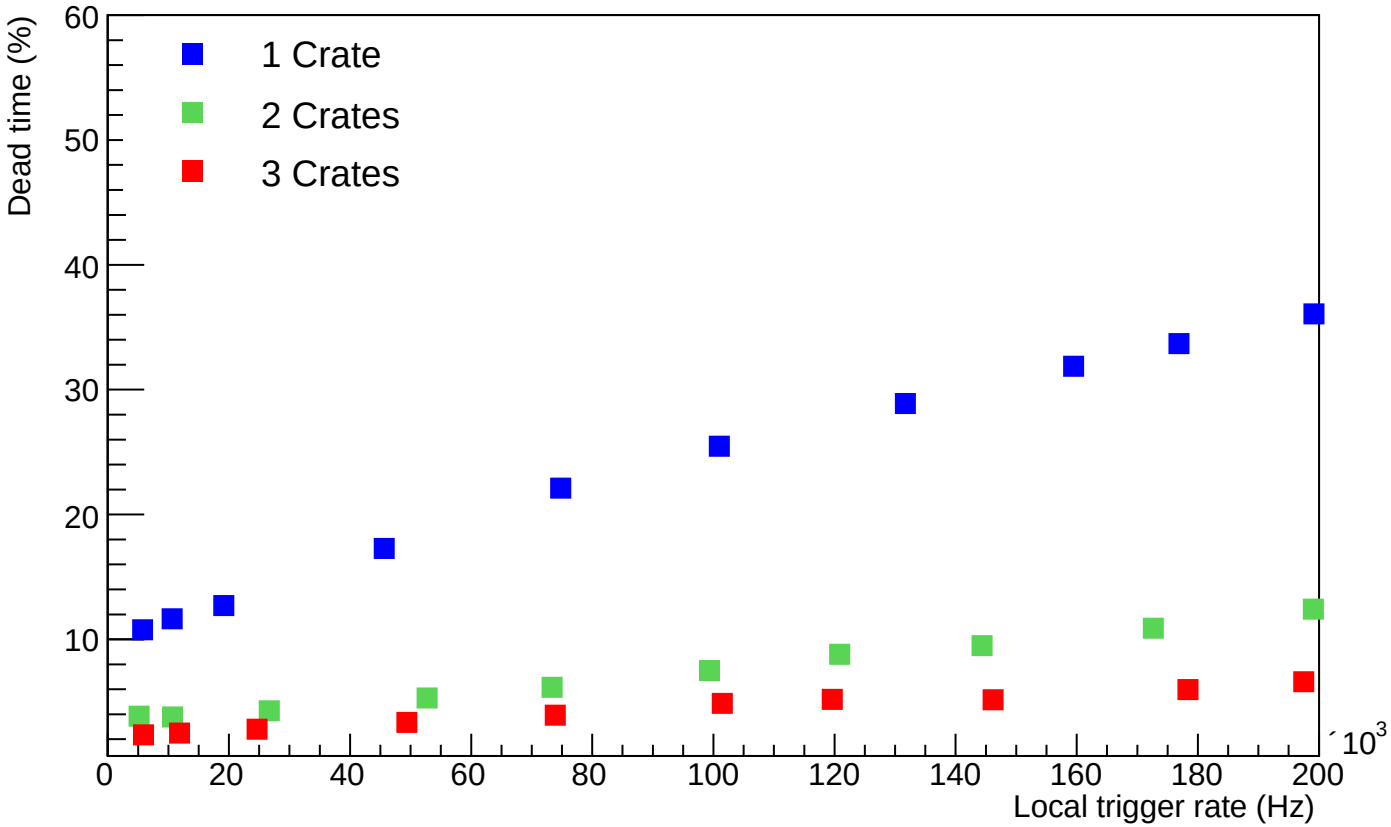
HallA SBS Trigger block diagram





Single Crate vs. Trigger Switching

Readout trigger rate ~ 5 kHz
Buffer Level = 4
8ADC - (reading pedestals on 6 channels in each ADC)

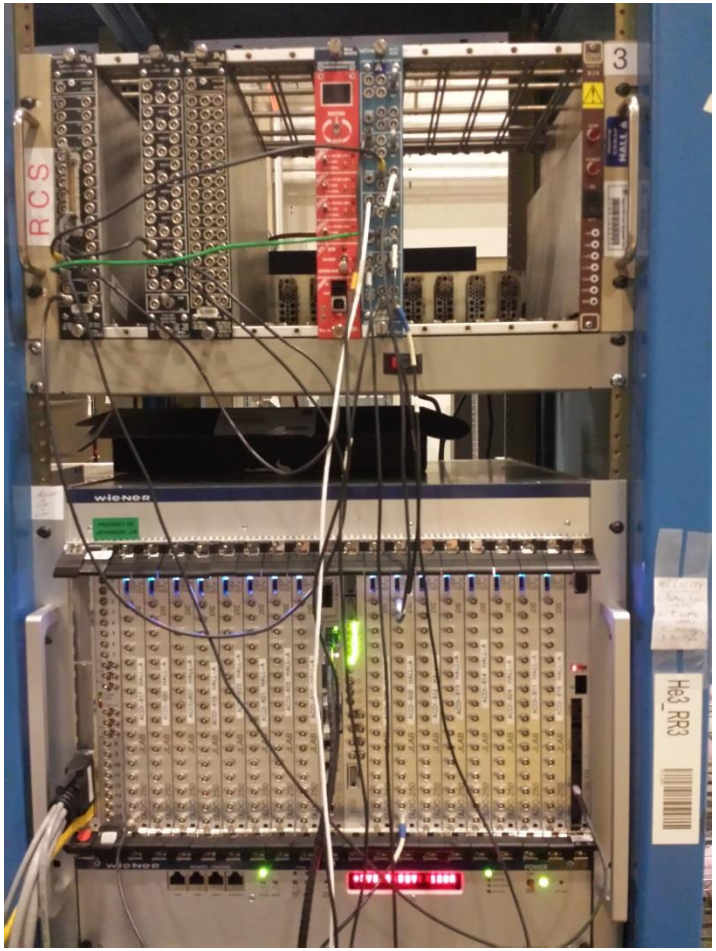


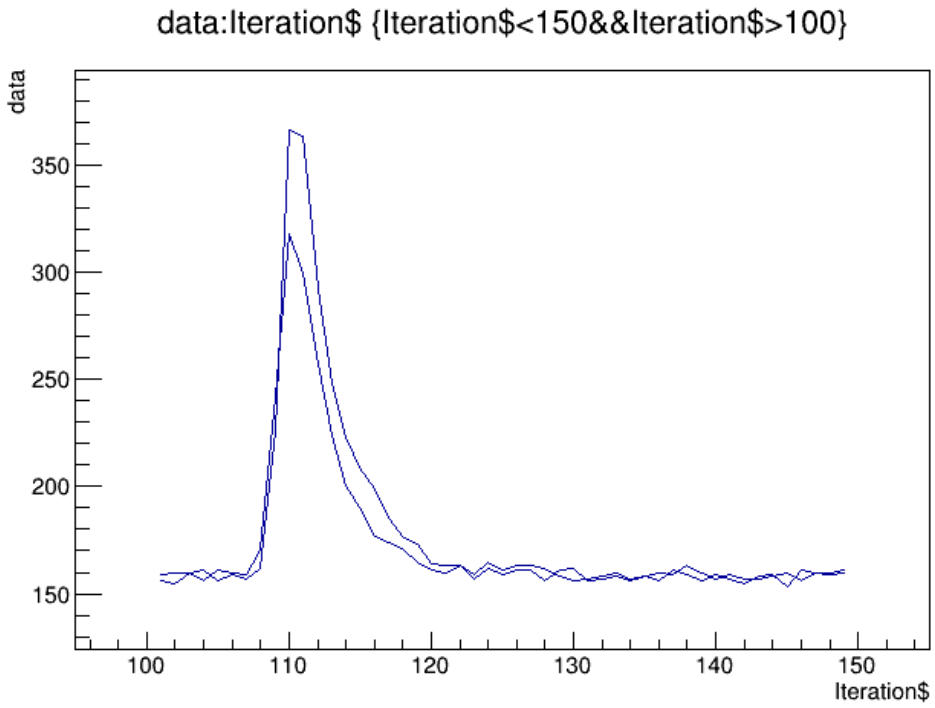
HCAL

- All FADC 16 delivered
- 2 VXS crates delivered
- 2 Intel Concurrent CPU delivered

- Readout tested
- Development of trigger using HPS firmware and Global Trigger Processor (GTP)
- New VTP ordered

HCAL FADC electronics

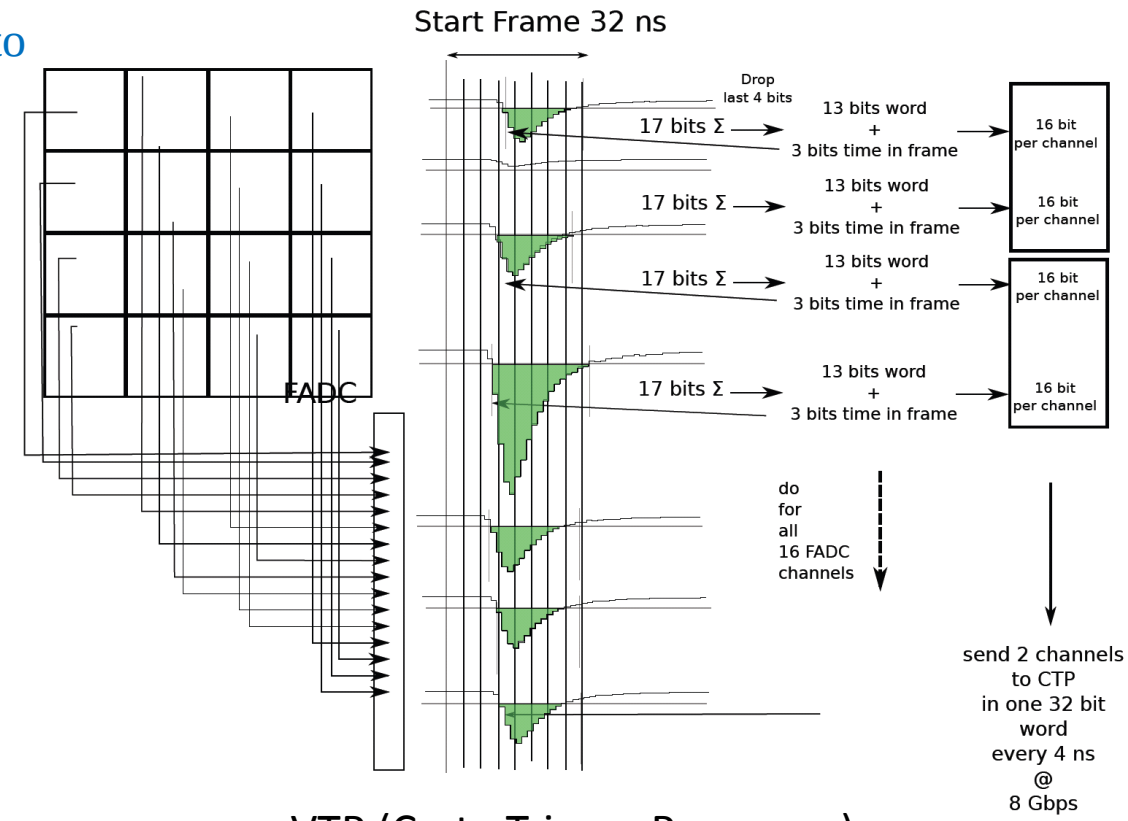




- Cosmics from calorimeter block
- Will test later with HCAL module

Hadron Arm - HCAL DAQ: proton trigger

HCal Signals to FADC inputs



- 2 VME switched Serial (VXS) Crates
- JLAB FADC250, a 16-channel 12-bit FADC sampling at 250 MHz
  - 16 FADC in VXS Crate 1
  - 2 FADC in VXS Crate 2
  - If signal pass threshold
    - Integrates signal and subtracts pedestal
    - Sends time frame info

- VTP (Crate Trigger Processor)
  - Located in VXS crates
  - Collects integrated signal and timing from FADC channels
  - Sends data to the second VTP for clustering

HCAL trigger development

- HPS firmware installed on FADC and GTP
- FADC readout tested with cosmics
- Testing triggering capability

- Need
  - implement decoder for analysis
  - Test using 2 crates and new VTP

GEM MPD readout

- INFN MPD used for several years using custom C++ package
- Package ported to intel CPU
- New C library written for easy integration into CODA

(Bryan Moffit, Evaristo Cisbani, Danning Di)

- CODA configuration running
- Debugging module initialization

GEM optical link readout

- Aurora protocol based
  - Implemented by Paolo Musico. To be tested.
- 2 Gbit optical link to SubSystem Processor (SSP) module
  - 250 MB/s per link
- Readout up to 32 MPD in parallel
  - 8 GB/s bandwidth compared to ~100 MB/s using VME
- SSP library
  - Readout routines – Completed.
  - MPD configuration routines – In progress
- Link from MPD to SSP module
  - Implemented by Ben Raydo. Works.

Timeline

4th quarter 2015	1st quarter 2016	2st quarter 2016	Future

• Finish MPD CODA readout – debug
• Finish Fastbus Readout – debug
• Small scale setup
  • 200 KHz L1
  • 5 kHz coinc
  • Fastbus, MPD, and HCAL FADC
• Cdet Fastbus
• Analysis software : check synchronization
• Test MPD optical readout (SSP)
• HCAL trigger ordered
	• Implement new HCAL Trigger module
	• HCAL cosmics
	• GEM cosmics with MPD
	• Test GEM readout with optical link in high background at UVA
	• Develop GEM analysis software
		• GEM installed on BigBite for tritium experiment
		• ECal cosmics
		• DVCS experiment
		  Parasitic test: Fastbus and FADC setup
			• Tritium experiment
			  Parasitic test: Fastbus and FADC setup

Manpower

- Fastbus
  - JLAB : Dasuni Adikaram, Mark Jones, Robert Michaels, Bryan Moffit, William Gu
- MPD
  - INFN : Evaristo Cisbani, Paolo Musico
  - UVA : Danning Di, Kondo Gnanvo, Nilanga Liyanage
  - JLAB : Ben Raydo, Bryan Moffit
  - Stony Brook : Seamus Riordan
- HCAL
  - JLAB : Alexandre Camsonne, Ben Raydo, Bryan Moffit

Conclusion

- Fastbus event switching works well
  - Preliminary results show acceptable dead time in experiment conditions
  - Need to develop software and check synchronization
- HCAL:
  - FADC ready
  - trigger implemented and being tested
- MPD:
  - CODA readout implemented
  - Debugging of the software driver
  - Optical readout in progress
- Small scale test setup in a few weeks

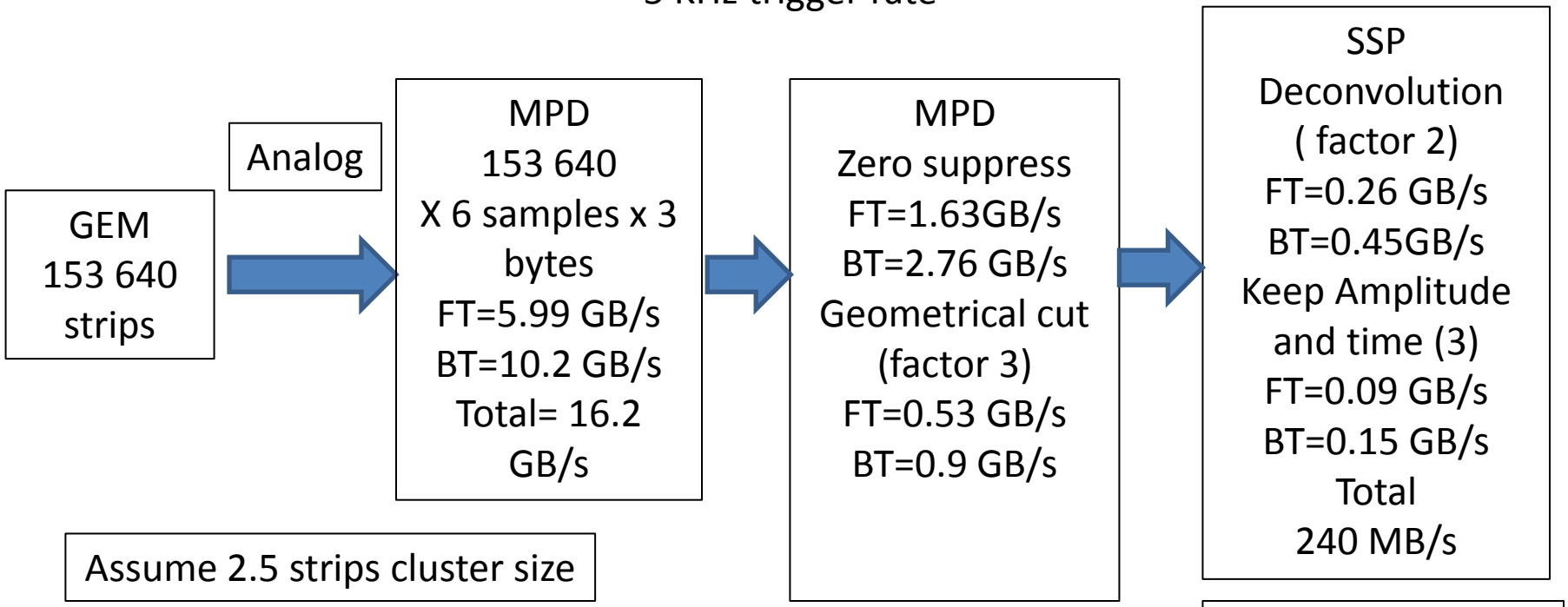
Backup Slides

$G_{E_p}5$

- Focal Plane Polarimeter
  - Front tracker
  - Back tracker GEM 128 K channels
  - 288 channels HCAL on FADC (10 samples)
- Electron detector
  - 1800 channels ECAL
  - CDet 2152 Channels (TDC)

GEM data flow GEp

5 KHz trigger rate



Assume 2.5 strips cluster size

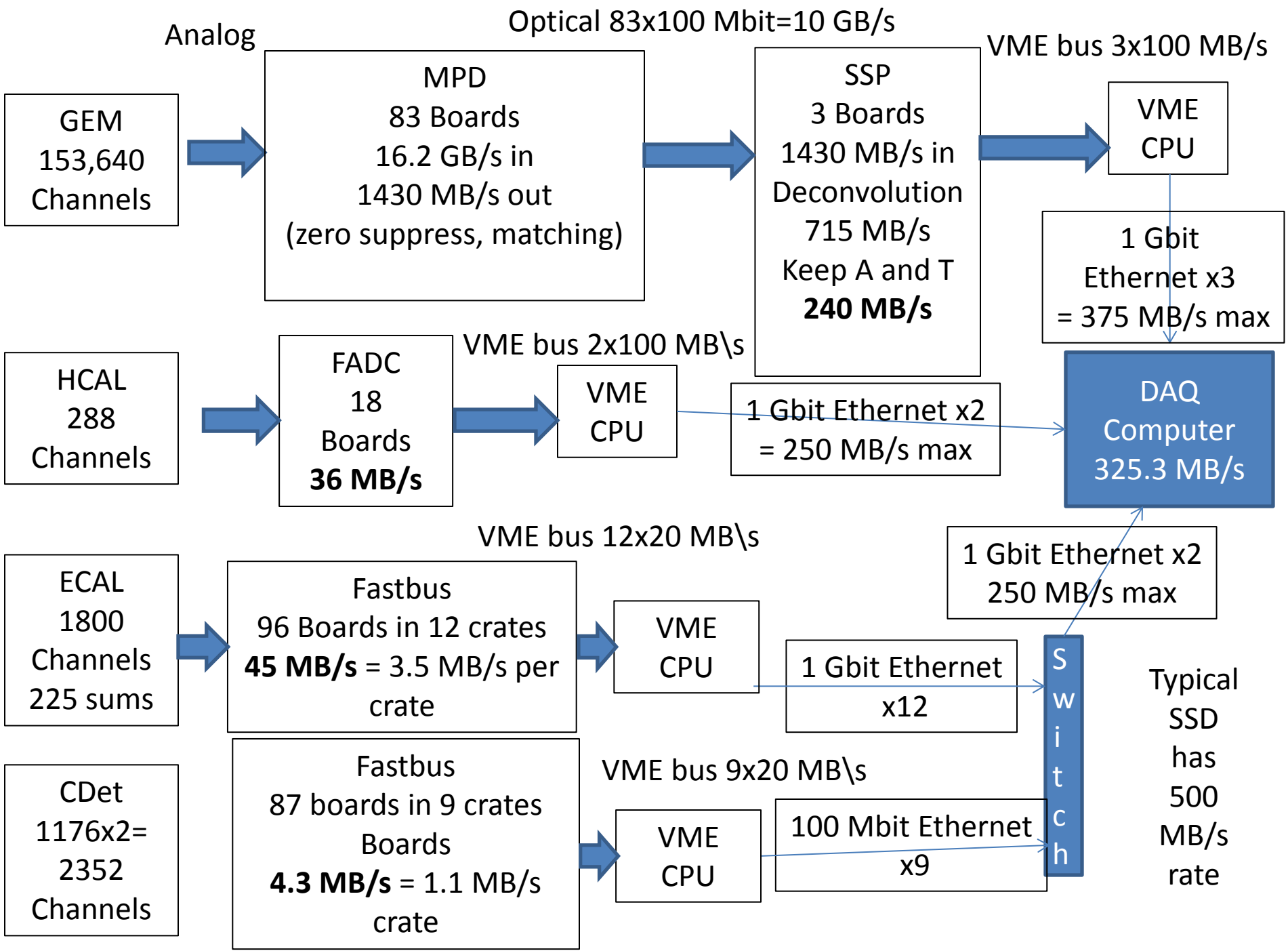
Time window	6x25 ns	3x25 ns
Occupancy forward tracker in %	36.2	18.1
Occupancy back tracker In %	22.4	11.2

Need to test clustering and correlations betweens planes for further reduction

GEp5 event size (after deconvolution and geomtrical matching)

Detector	Channels	Single rate Hz	Occupancy 75 ns in %	Channels firing	Event size (bytes)	Data rate 5 KHz MB/s
Front tracker	41,000	3.3e9	18.1	7430	136,000	90
Back tracker	128,000	3.36e9	22.4	12600	230,000	150
HCal	288	_	100	288	7,200	36
ECAL	1800 + 225	_	100	2025	8,100	45
CDET	2152	_	10	216	864	4.3
Total						325.3 MB/s

HCAL and ECAL occupancies need to be evaluated : using 100 % for now


Analog
Optical 83x100 Mbit=10 GB/s
VME bus 3x100 MB/s
GEM
153,640
Channels
MPD
83 Boards
16.2 GB/s in
1430 MB/s out
(zero suppress, matching)
SSP
3 Boards
1430 MB/s in
Deconvolution
715 MB/s
Keep A and T
240 MB/s
VME
CPU
1 Gbit
Ethernet x3
= 375 MB/s max
HCAL
288
Channels
FADC
18
Boards
36 MB/s
VME bus 2x100 MB\s
VME
CPU
1 Gbit Ethernet x2
= 250 MB/s max
DAQ
Computer
325.3 MB/s
VME bus 12x20 MB\s
1 Gbit Ethernet x2
250 MB/s max
ECAL
1800
Channels
225 sums
Fastbus
96 Boards in 12 crates
45 MB/s = 3.5 MB/s per
crate
VME
CPU
1 Gbit Ethernet
x12
Switch
Typical
SSD
has
500
MB/s
rate
CDet
1176x2=
2352
Channels
Fastbus
87 boards in 9 crates
Boards
4.3 MB/s = 1.1 MB/s
crate
VME bus 9x20 MB\s
VME
CPU
100 Mbit Ethernet
x9

G_{E_n} and G_{M_n}

- Bigbite
  - GEM 128 K channels
  - Shower 189 blocks (ADC)
  - Preshower 54 blocks (ADC)
  - Scintillator 180 bars 360 PMTs (ADC/TDC)
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- Neutron detector
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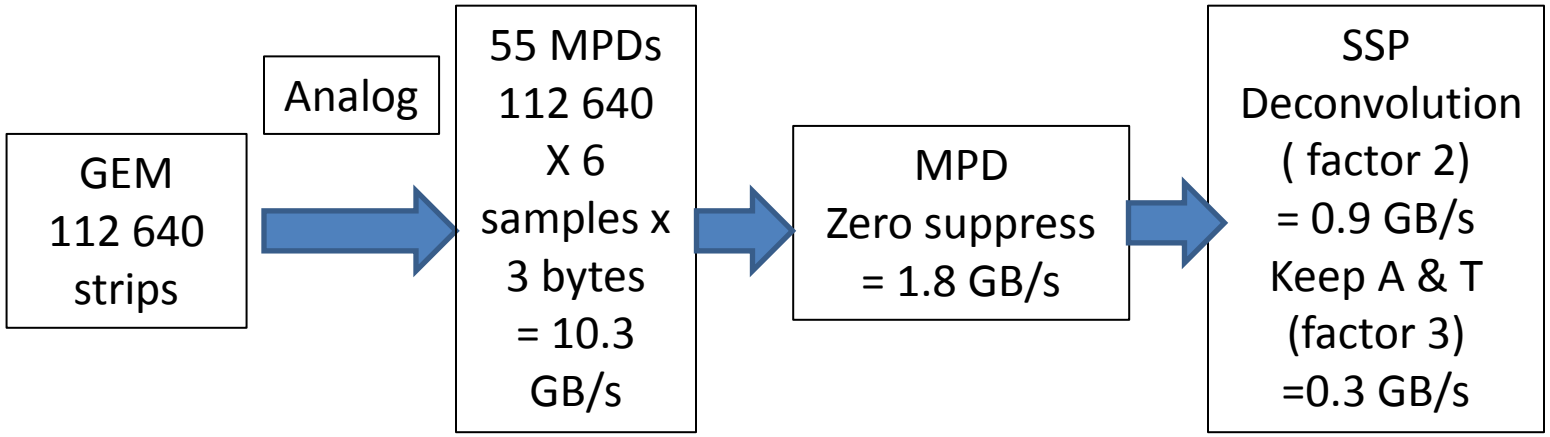
Gen trigger rates (95 % QE peak)

Q^2	Rate [kHz]
1.5	3
4	0.4
7	0.09
10	0.06

GEM data flow GEp

5 KHz trigger rate



Time window	6x25 ns	3x25 ns
Occupancy back tracker In %	17.4	8.7

Assume each MPD word packed on 24 bits = 3 bytes

Gen and GMn event size

Arm	Detector	Channels	Single rate Hz	Occupancy 150 ns in %	Channels firing	Event size (bytes)	Data rate 5 KHz MB/s
BigBite	GEM	112,640	2.6e9	17.4	19680	359,775	1798
	Lead glass	243	_	100	243	1003	5
	Scintillators	360	_	100	360	1485	7.4
	Cerenkov	550	_	100	550	2269	11.34
Neutron	HCal	288	_	100	288	7,200	36
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Gen and GMn event size deconvoluted

Arm	Detector	Channels	Single rate Hz	Occupancy 100 ns in %	Channels firing	Event size (bytes)	Data rate 5 KHz MB/s
BigBite	GEM	112,640	2.6e9	8.7	5248	62,976	300
	Lead glass	243	_	100	243	1003	5
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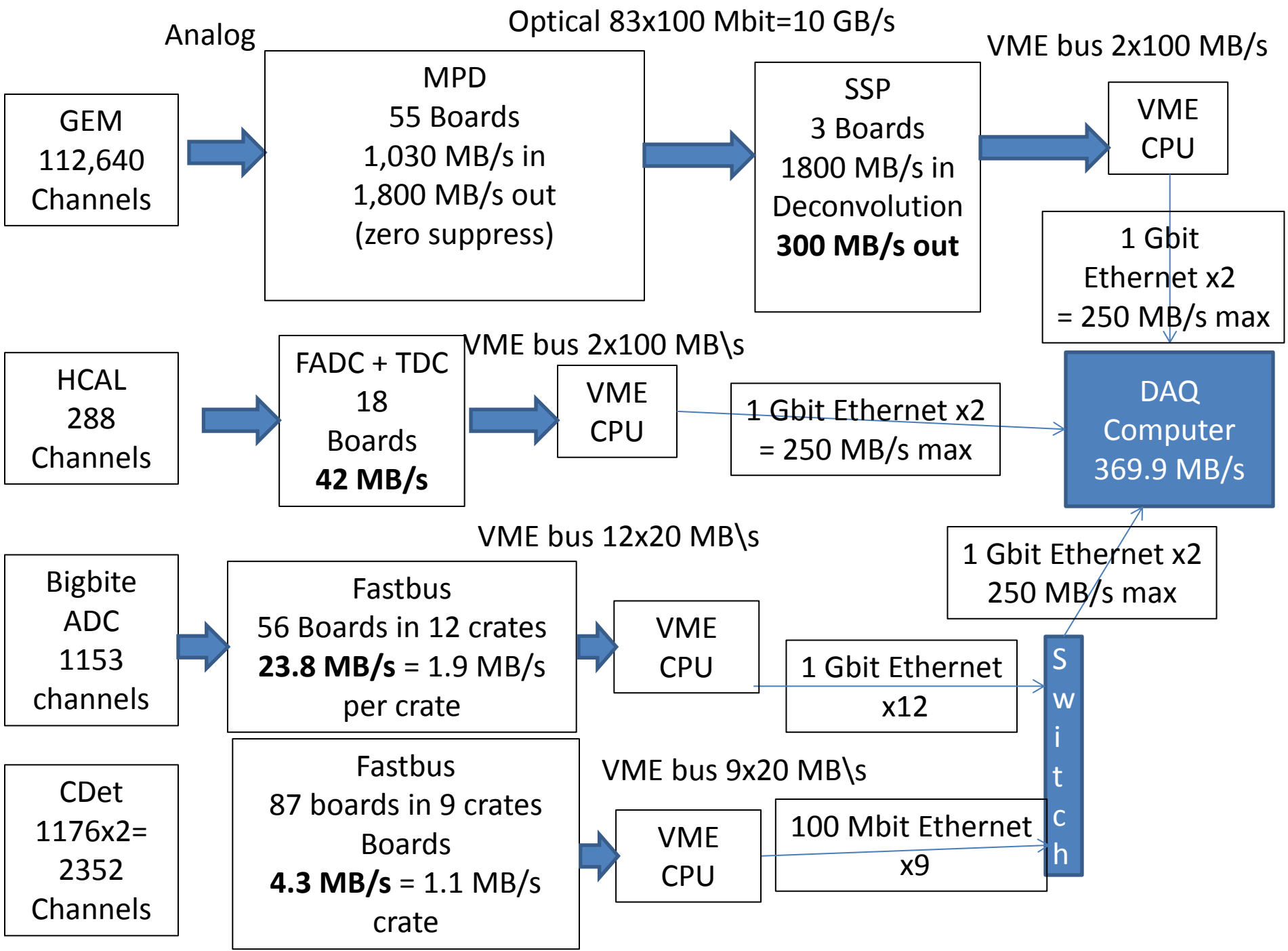
Total at 5 KHz 369.89 MB/s Max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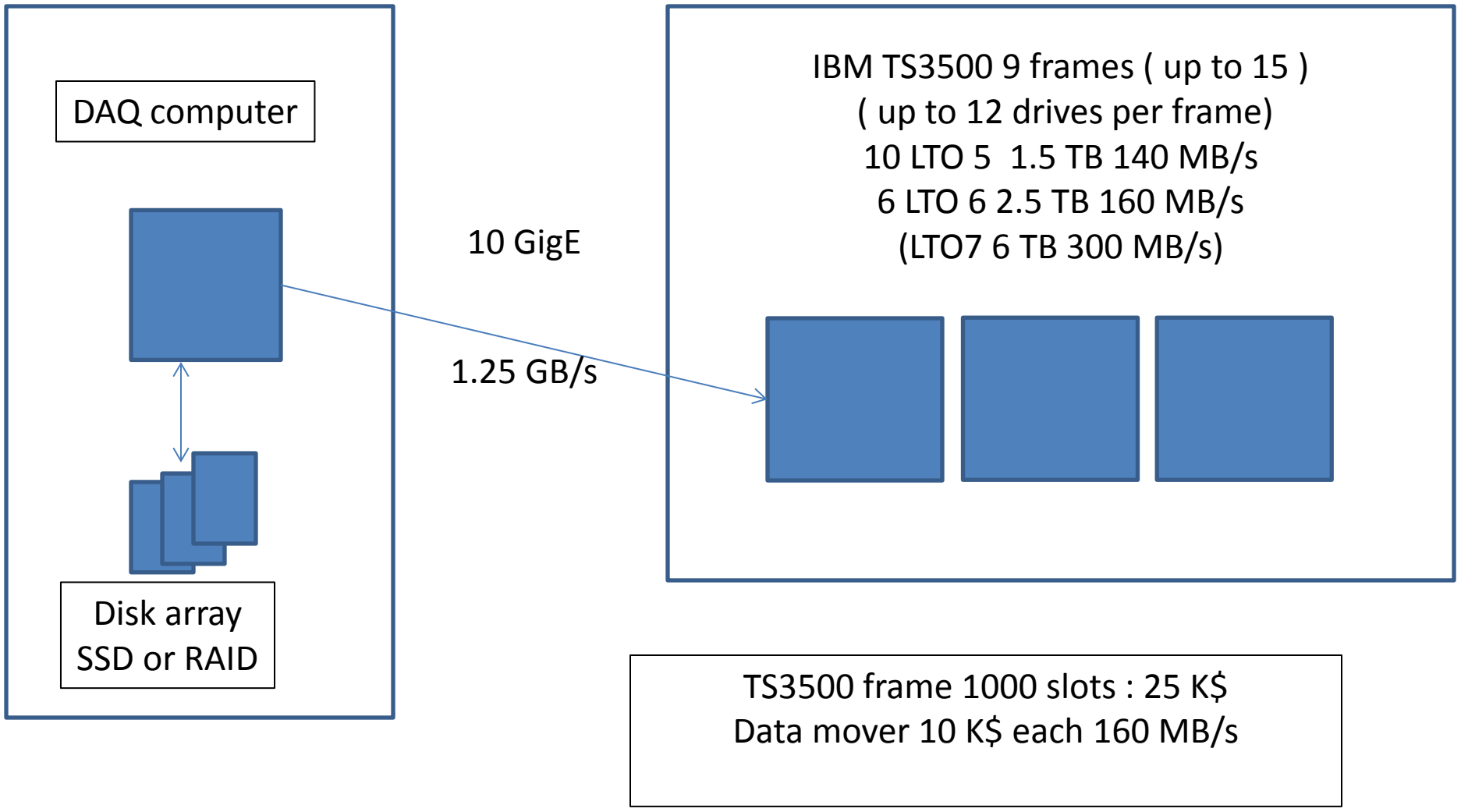
Channels
MPD
55 Boards
1,030 MB/s in
1,800 MB/s out
(zero suppress)
SSP
3 Boards
1800 MB/s in
Deconvolution
300 MB/s out
VME
CPU
1 Gbit
Ethernet x2
= 250 MB/s max
HCAL
288
Channels
FADC + TDC
18
Boards
42 MB/s
VME bus 2x100 MB\s
VME
CPU
1 Gbit Ethernet x2
= 250 MB/s max
DAQ
Computer
369.9 MB/s
VME bus 12x20 MB\s
1 Gbit Ethernet x2
250 MB/s max
Bigbite
ADC
1153
channels
Fastbus
56 Boards in 12 crates
23.8 MB/s = 1.9 MB/s
per crate
VME
CPU
1 Gbit Ethernet
x12
Switch
CDet
1176x2=
2352
Channels
Fastbus
87 boards in 9 crates
Boards
4.3 MB/s = 1.1 MB/s
crate
VME bus 9x20 MB\s
VME
CPU
100 Mbit Ethernet
x9

SILO



TS3500 frame 1000 slots : 25 K$
Data mover 10 K$ each 160 MB/s

Tape cost 250 MB/s

		Days	Data rate	Seconds	Total data TB	Double	DLO5 in $	DLO6 in $	Tape DLO6
E12-12-09-019	GMN	25	250	2160000	540	1080	54000	32400	216
E12-09-016	GEN	50	250	4320000	1080	2160	108000	64800	432
E12-07-109	GEP/GMP	45	250	3888000	972	1944	97200	58320	388.8
E12-09-018	SIDIS	64	250	5529600	1382.4	2764.8	138240	82944	552.96
	Total	184		15897600	3974.4	7948.8	397440	**238464**	1589.76
Actual days	Actual years		Time in s			Per year	394200	236520	
368	1.01	184	15897600						

1 600 LTO6 tapes for 240 K$, if go to 500 MB/s 480 K$
2 frames with 8 data movers 130 K$

Conclusion

- Estimated rate for max 5 KHz (expect to run at 2 to 3 KHz)
- 325.3 MB/s for GEp5
- 370 MB/s for GEn (no geometrical correlation)
- Will work on clustering and plane coincidence in SSP, reduction factor to be determined using simulation
- Need implement hardware and test