



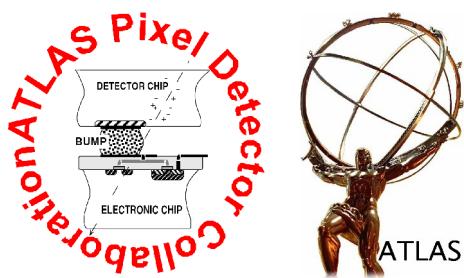
Commissioning Perspectives for the ATLAS Pixel Detector

Dissertation
zur Erlangung des akademischen Grades
eines Doktors der Naturwissenschaften
des Fachbereichs Physik
der Universität Dortmund

vorgelegt von
DIPL.-PHYS. DANIEL ADAM DOBOS



Lehrstuhl für Experimentelle Physik IV
Fachbereich Physik
Universität Dortmund



Dortmund, 1. September 2007

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Abstract:

The ATLAS Pixel Detector, the innermost sub-detector of the ATLAS experiment at the Large Hadron Collider, CERN, is an 80 million channel silicon pixel tracking detector designed for high-precision charged particle tracking and secondary vertex reconstruction. It was installed in the ATLAS experiment and commissioning for the first proton-proton collision data taking in 2008 has begun. Due to the complex layout and limited accessibility, quality assurance measurements were continuously performed during production and assembly to ensure that no problematic components are integrated. The assembly of the detector at CERN and related quality assurance measurement results, including comparison to previous production measurements, will be presented. In order to verify that the integrated detector, its data acquisition readout chain, the ancillary services and cooling system as well as the detector control and data acquisition software perform together as expected approximately 8% of the detector system was progressively assembled as close to the final layout as possible. The so-called System Test laboratory setup was operated for several months under experiment-like environment conditions. The interplay between different detector components was studied with a focus on the performance and tunability of the optical data transmission system. Operation and optical tuning procedures were developed and qualified for the upcoming commissioning. The front-end electronics preamplifier threshold tuning and noise performance were studied and noise occupancy of the detector with low sensor bias voltages was investigated. Data taking with cosmic muons was performed to test the data acquisition and trigger system as well as the offline reconstruction and analysis software. The data quality was verified with an extended version of the pixel online monitoring package which was implemented for the ATLAS Combined Testbeam. The detector raw data of the Combined Testbeam and of the System Test cosmic run was converted for offline data analysis with the Pixel bytestream converter which was continuously extended and adapted according to the offline analysis software needs.

Commissioning Perspectives for the ATLAS Pixel Detector

A Scientific Madman Threatens the World

stripped-down and dramatically improved edition of the classical
almost-twentysix-volume "Chronicles of The Atlas Club –
Encyclopedia Of Sense–Transparent Three (And One Order Of
Magnitude More Or Less) Letter Acronyms [EOSTT(AOOOMMOL)LA]"

by Jack Dapid

edited, shorted, commented and unchanged by Daniel Dobos

Prologue

While other kids in our transatlantic neighborhood had been playing with their particle slingshots and top marbles in the late thirties of the last century, I was confined by my 'Scientia Curiositatis Syndrome' to my home and my books. So neither sunlight nor social contacts disturbed my early growth and only Jack Dapid, the author, publisher and only other proven customer of my favorite book "Chronicles of The Atlas Club", formed my clean untouched mind to its brilliance today. Therefore and due to a temporary leak of fantasy during the last three years I decided to just condense my favorite book to a carryable amount instead of writing my own one. Nevertheless I hope you enjoy this exciting document with a glass of red wine sitting by the fireplace and if you think to accuse somebody of copyright infringement or insufficient burning time I kindly refer you to the original author Jack Dapid.

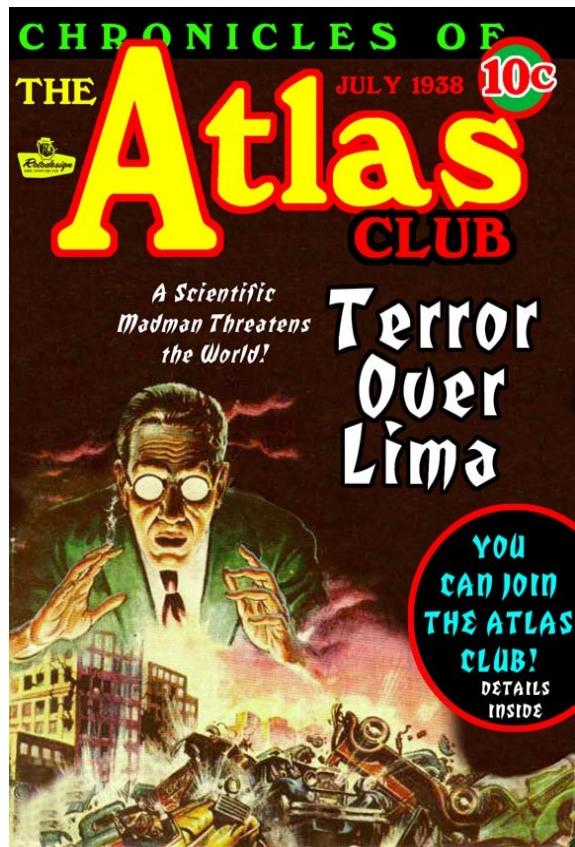
Even though Jack's book is an encyclopedia it tells a story. Anyhow all paragraphs contain an unexplained three-to-four letter abbreviation in pseudo-alphabetical order. He tells the story of the placid, likeable (aside from his hobby of planning to blow mankind out of existence) and charming wannabe titan Attila Lasko. After carrying the firmament for some time [HES00], [HOM00] & [DOB04] and a deep thought (till 1842 AD – the year a bottle apple juice has fallen on my grandfathers head and he invented liquid gravity – but this is another story) Attila decides that supporting the canopy is by far not the most interesting task and is even more boring than playing croquet. Jack moves his central character to Pregnin, central France (in France even 'Guyane française' is 'somehow' central) and describes in the next 36 (thirtysix!) chapters (847 pages) in detail how Attila searches for a farm (243 p.), curses seven real-estate agents (417 p.), swears to never buy a farm through a real-estate agent (25 p.), and finally describes the fabulous new farm ($\frac{1}{2}$ page) he bought from this beautiful French real-estate agent (here the first time I slightly shortened Jack's pleading to "Attila bought a farm in France." in the first and to "Later ..." in the second iteration). Fortunately Jack never mentioned this farm again in his book even though I'm sad that I have to deny you the three sentences about this 23-year-old French real-estate agent in her blue dress. Not even Willy Shakespeare managed to describe a woman like this.

So my story directly continues with Attila's dream in his new farm about 21 point-like fundamental pies (he named them pieticles). All these pies have different colors, flavour, smell and calorie content. Even though he gives a rough overview of his system of tasty pieticles (his so-called 'Standard Model of Tasty Pieticles [SMTP – I guess you always asked yourself for what this one stands for]') and the poorly understood hierarchy of calorie content you will miss pictures in his records (I guess mainly to save you from hunger).

However things starts to go wrong when Attila gets an idea (during falling down the stairway and hitting his head against his own self-confidence) about a new fundamental pie, the HIGGS (Holy Imaginary Gorgeous Grail Search) which should be responsible for the calorie content of all other pieticles or at least for crop circles. He describes the huge (mainly to impress the blue dressed real-estate agent) machine he is going to build for his quest. He calls it ATLAS (Any Three Letter Acronym ruleS).

Later (without buying any farms) he awakes with heavy headaches in a strange world in front of a huge sign with the inscription: 'SPYLESS TIME TEXT; CAN REVENGE'. His flair immediately tells him this has to be an anagram. So he thinks: "This has to be an anagram!" but the best he comes up with is 'TEMPEST STYLE SIX' for the first line. He explores his new environment and sees curious white or blue creatures with just as strange voluminous blue or white feet. They are lurching around in a huge white, window-annihilating room (a space ship? an over dimensioned shoe box? probably a mixture of the two). Some of the creatures badger robots that are lying pretty depressed around with different kind of semi-extraterrestrial tools. It takes Attila quite a while (and about 12 coffees) to understand that he is in a hospital for frustrated robots. He watches for a while how the blue/white doctor creatures try to get the robots to react, but nothing happens. Always ready to help with his infamous smartness Attila shouts: "The reason for their melancholy is obvious: They all look like overweight toilet paper rolls." Everybody in the robo-ward turns around and glares at him. Immediately feeling queasy Attila adds sheepishly: "Or maybe we need a new database?" The looks relax and the doctors continue their robot invocations. Only one of them still looks at Attila and asks in a weird and causal-less language "ROLSCTDAQTRTRODDCSPIXELBOCDDCROB?" Attila answers with "QWERTYUIOP", the only sentence he remembers from his C++ language course, which means something like "I have no ***** idea!" The doctor shrugs Attila off and wants to turn around, but suddenly, not believing his eyes, he sees the smallest of the robots starts to ...

But why am I telling you the entire story? Read it yourself and maybe – maybe I rejoin you in the Epilogue. And if not please read the 26 volume original (especially if you want to know more about French real-estate agents) before you ask for your money back.



original book cover from 1938

*»Ich werde versuchen mich gegen alles zu wappnen, bis auf den Erfolg.
Erstens ist das nicht nötig, und zweitens wäre es aussichtslos.«*

Martin Walser

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Chapter 1

Introduction

Physicists aim to describe nature with general laws, explain its behavior with models and quantify fundamental relations between measurable values. Particle physics investigates the fundamental structure and constituents of matter and the forces between them. This quest includes the discovery and characterization of elementary particles, the question of the origin of mass and the deeper reason behind the structure and relations between these particles. The Standard Model of particle physics is a theory which answers some of these questions and summarizes today's image of the fundamental composition of the universe. It describes the properties of the fundamental particles and their elementary interactions. These twelve particles are grouped into two different kinds of matter and their interaction is described by four general forces. Ordinary observable matter consists of only three of these particles, but two heavier copies exist of each. The investigation of the Standard Model also includes the effort of unification of the known general forces to a single primal one.

Over the last 30 years the Standard Model has been verified with incredible precision and has successfully predicted the existence of new particles. It is one of the most extensively tested scientific theories and can explain and predict most of the particle and interaction properties with unexpected accuracy. Nevertheless an obvious deficiency of the Standard Model is the lack of an explanation for the origin of mass as particles are described to be massless. An extension to the standard model that could explain the origin of mass has been proposed by Peter Higgs. In this theory, particles acquire their mass by coupling to a scalar field as a consequence of a spontaneous symmetry breaking. It is associated with the prediction of the existence of a new massive particle, the Higgs boson, and its discovery has become the 'holy grail' of particle physics over the past few decades.

Collisions of high energy particle beams produce enormous energy densities. This allows searches for new particles like the Higgs boson, the investigation of the properties of our universe split seconds after the Big Bang and the search for further general symmetries and laws of nature. Particle accelerators, like the LHC¹ at CERN², accelerate particles with electromagnetic fields and collide the high energy particles.

1 Large Hadron Collider » <http://www.cern.ch/lhc>

2 Conseil Européen pour la Recherche Nucléaire – since the laboratory has reoriented its research more to particle physics, only 'CERN' is the common name » <http://www.cern.ch>

This results in energy densities close to the Big Bang generating a multiplicity of known and most probably some unknown high energy particles. Most of these particles are very short-lived. Therefore conclusions on properties of these particles and their interactions are possible by measuring the impact parameters of all generated particles and a reconstruction of the collision.

The detection of the generated particles and the measurement of their impact parameters is done with detector systems, like the ATLAS³ detector. These are arranged around the collision point of the accelerated particles. A tracking system measures the tracks of generated particles in a magnetic field and the energy deposition of these particles is measured in a calorimeter system. This allows to identify, calculate the mass, momentum and energy of involved particles. It allows as well to conclude by which interactions and from which short-living particles they have been generated. A trigger system is used to filter rare interesting events out of the background of well known ones.

At the LHC interaction point of ATLAS about 10^9 proton-proton interactions per second are expected. This means close to 1600 tracks of charged particles 40 million times a second. This poses enormous challenges on the detectors. Detectors close to the interaction point need to have a high granularity in order to distinguish individual tracks and, due to the high particle rate, they have to withstand high radiation doses. Therefore silicon detectors are used in the ATLAS experiment for tracking and secondary vertex determination. The ATLAS Pixel Detector is the innermost tracking detector with a minimal distance of ~ 5 cm to the interaction point. It is an 80 million channel silicon tracking detector and provides per track three high precision space points without ambiguities. The Pixel Detector consists of 1744 hybrid modules which are a flip-chip assembly of a silicon sensor with 46 thousand $50 \times 400 \mu\text{m}$ pixels and 16 front-end amplifier and digitization chips. Modules are located in three cylindrical layers and three disks in each forward region forming an 1.4 m long and 0.5 m in diameter detector centered on the interaction point. Due to its complex layout and the difficult accessibility in the ATLAS experiment continuous quality assurance measurements during the production of the detector components and the assembly were necessary. The Pixel Detector final assembly was performed at CERN and it was integrated into the ATLAS experiment in summer 2007. Commissioning for the first LHC proton-proton collision data taking in summer 2008 has begun.

In the scope of this work quality assurance measurements for the assembly of the Pixel barrel at CERN were developed, performed and analyzed. In order to verify the performance and interplay of the integrated detector and the ancillary services a fraction of $\sim 8\%$ of the detector system was assembled as close to the final layout as possible and operated in a System Test laboratory setup. Since the performance of the complete detector system is studied in the System Test, a detailed description of the Pixel Detector including the silicon sensor and attached front-end electronics, mechanical structure, the optical data transmission system, the readout and control system, power supply system, interlock matrix and detector control software is given. The System Test layout including the cooling and cosmic muon scintillator trigger system is described and differences to the final experiment layout are highlighted. Results of the System Test operation are analyzed with a focus on the tuning of the optical data transmission system, the detector front-end electronics tuning and noise

³ A Toroidal LHC ApparatuS » <http://www.atlas.ch>

occupancy at low sensor bias voltage. Problems identified in the System Test and the consequential adaptations of quality assurance measurements and detector components are discussed. Developed operation and optical tuning procedures are presented. In order to test the data acquisition and trigger system as well as the data acquisition, offline reconstruction and analysis software chain a cosmic muon data taking was performed with the System Test setup and the scintillator trigger system. The cosmic muon data quality was verified with an extended version of the Pixel online monitoring package, which was implemented in the scope of this work for the ATLAS Combined Testbeam data taking. Raw data taken during the Combined Testbeam and the System Test cosmic run was converted for offline reconstruction and analysis by the Pixel bytestream converter, which was continuously extended and adapted according to the offline analysis software needs.

In chapter 1 an overview of the basic principles of high energy collider physics, the Standard Model of particle physics and its fundamental forces as well as the basic motivation of ATLAS, namely the search of the Higgs boson, is presented. The basic physical effects which allow to use semiconductors for particle detection, the functionality and different concepts of segmented semiconductor detectors as well as their radiation damage in the experiment are discussed in chapter 2. Chapter 3 gives an introduction to the LHC accelerator, the different ATLAS subsystems, their aims and performance, in order to understand the global concept of the experiment and the task of the ATLAS Pixel Detector in the experiment. The Pixel Detector with its mechanical structure, silicon detector modules, front-end electronics, data acquisition readout chain and ancillary services is detailed in chapter 4. The integration of the Pixel Detector at CERN with the attendant production quality assurance measurements and tests are discussed and analyzed in chapter 5. Results of the measurements and the performance of the Pixel barrel are presented and the assembly of the Pixel Detector as well as the integration into the experiment are described. Layout and results of the Pixel System Test with particular focus on the tuning of the optical data transmission, developed operation and optical tuning procedures as well as the detector tuning performance are worked out and analyzed in chapter 6. A measurement method for the detector integrated irradiation dose using the sensor depletion voltage determined from noise occupancy versus sensor bias voltage scans is studied. The raw data output format of the Pixel Detector and implementations of the online data quality monitoring and the offline analysis raw data converter, which have been used in the ATLAS Combined Testbeam and the Pixel System Test cosmic data taking are described in chapter 7. In chapter 8 conclusions regarding the presented results are drawn and an outlook to the upcoming Pixel Detector commissioning and operation is given.

1.1 High Energy Collider Physics in a Nutshell

The discovery of a new particle and the measurement of its properties is 'in principle' a quite easy task. Producing this particle requires a very high energy density, close to the energy density split-seconds after the big-bang. This is because the new particle is expected to be heavy and therefore its mass creation requires an enormous amount of energy ($E=mc^2$). (Un)fortunately lighter particles have been already discovered by other physicists. The desired energy density can be reached by letting high energy (accelerated) particles collide.

To accelerate the particles one uses the fact that a charged particle is accelerated in an electric field, e.g like a tree trunk in a river. One can reach a more efficient acceleration by letting the electric field move with the particle. The particle rides on an electromagnetic wave like a surfer on a water wave. Nevertheless the necessary high energy requires very long (several tens of kilometers) straight accelerators. Another possibility is to let the particles pass multiple times through the same acceleration device in a ring accelerator. Ring accelerators have the drawback that a magnetic field is necessary to bend the charged particles to their orbit and the particles lose energy during their bending. Since the bending strength of magnets is limited and the energy loss is decreasing with decreasing bending, one has to use ring accelerator with several kilometers of radius. The basic acceleration and bending techniques are used in every TV tube.

The bending energy loss appears as radioactive radiation, which is one of the reasons to build ring accelerators underground. On a designated point in the ring one can let collide two particles, accelerated in opposite direction. Even though enough energy is provided for the generation of a new particle, it is expected to be produced very rarely. (Un)fortunately often generated particles have been discovered by others. Therefore one increases the number of colliding particles by letting many packages with lots of particles each collide and by focusing this packages on the collision point. The next problem is that the new particle is expected to live very short and decays into other particles after traveling split-millimeters with the speed of light. There is no technology available that would allow the identification or measurement of this new particle directly in this short distance. Therefore one tries to identify and measure all (known) particles that the new particle is decaying into. The identity and properties of the new particle can be reconstructed by calculation from the measured identities and properties of the decay product particles. Important properties of the decay particles are their charge, momentum, energy and mass. A detector system is arranged around the collision point to measure these properties.

In the innermost part of the detector one measures tracks of particles leaving the collision point. This is realized by as low as possible mass detectors, since high amount of material on the track of the particles would change their direction and make them lose energy. Different detector technologies with continuously measurement of particle tracks or only some few position measurements, when particles penetrate a detector layer, can be used. They all have the common purpose of precisely measuring the particles track without changing the particle track or energy. The track

measurement is done in a magnetic field. Therefore charged particles are bent and their charge and momentum are measured from the bending strength of their tracks.

To measure the energy of particles very heavy detectors are located around the innermost detector part. It is the goal to stop the particles and let them deposit their entire energy by interaction with the detector material, like a bullet in a gelatin block. Since the particles have high energies, high density absorber materials like lead or iron are used to allow reasonable detector sizes. These materials does not allow to measure how much energy has been deposited in them, therefore layers of sensitive detector material are integrated in the detectors. The sensitive layers produce light or electrical signals which allow to measure the amount of deposited energy. The usage of only sensitive layers would result in too big detectors. Different detector techniques with different absorber and sensitive materials are used, since they can be especially sensitive to different particles. Depending on the particle type, mass and energy the energy deposition position and shape is different. Hence the different sensitivity of detectors and the different energy deposition characteristics of particles allow to identify different particles.

Some particles are very weakly interacting with matter and can escape the energy detectors without depositing their main energy. For examples muons would require several hundreds meters of high density absorber material to measure their energy. This is not practicable and they have been already identified by the fact that they can leave the energy detectors. Therefore one concentrates on measuring their momentum in a magnetic field with special detectors. Basically this is the same technique as in the innermost detectors, only that the detectors, their dimensions and the strength of the magnetic field is optimized for muon detection. Other particles, the neutrinos, interact with matter even more weakly. They would require several lightyears of absorbing matter to be detected. But if one assumes that the energy of all other particles has been measured, an asymmetry in the energy sum can be identified as an neutrino carrying away the missing energy.

As already mentioned, new particles are produced very rarely. It is not possible to record data of all collisions and anyhow in most of the collisions all produced particles, their properties and interaction are well understood. Therefore the decision which collision data is kept, is made due to patterns of present particles, their direction and their amount of energy. For example many particles leaving the collision point in transversal direction indicate that the colliding particles hit head-on-head and thus the entire collision energy was available for the creation of the new particle.

For selected collisions one computes the collision process, the involved particles and their properties from the decay particles. The precision of the decay particle property measurements is not high enough to claim the discovery of the new particle from a single reconstructed particle with the expected properties of a single collision. Therefore possible collisions and the detector measurement are simulated (with expected new particle interactions) for the case the expected new particles exists and for the case it does not exist. The measured data are compared to these simulations. Anyhow one has to understand the measurement of the detector as well as the simulated collisions, their simulated measurement and the simulated selection very well to be sure the observed signal is caused by a new particle. Some of the reasons why this 'in principle' easy task of finding new particles requires a lot of knowledge, technology, time, financial and manpower effort are presented in this work.

1.2 The Particle Physics Standard Model

In the Standard Model (SM) of particle physics matter is composed of few elementary, point-like and structureless particles called fermions. They have spin $\frac{1}{2}$ and can be arranged in three generations with a striking mass hierarchy. Each generation consists of two quarks, carrying charges $\frac{2}{3}$, $-\frac{1}{3}$ as well as flavour quantum numbers, and two leptons with charges -1, 0 and lepton quantum numbers. Within one generation the masses increase from the uncharged leptons (the neutrinos) to the positively charged quarks. All stable matter in our universe consists of particles from the first generation. Elementary particles of the second and third generation are produced in high energy processes. Apart from the neutrinos they are short-lived and quickly decay via intermediate steps into stable particles of the first generation.

The structure and the enormous mass range of the SM is shown in Figure 1-1. The particles are represented by animals so that the animal masses scale with the particle masses. An antiparticle with same mass and opposite charge is associated to each fermion. The reason for the structure of generations, their enormous mass range and their hierarchy are basic open questions of particle physics.

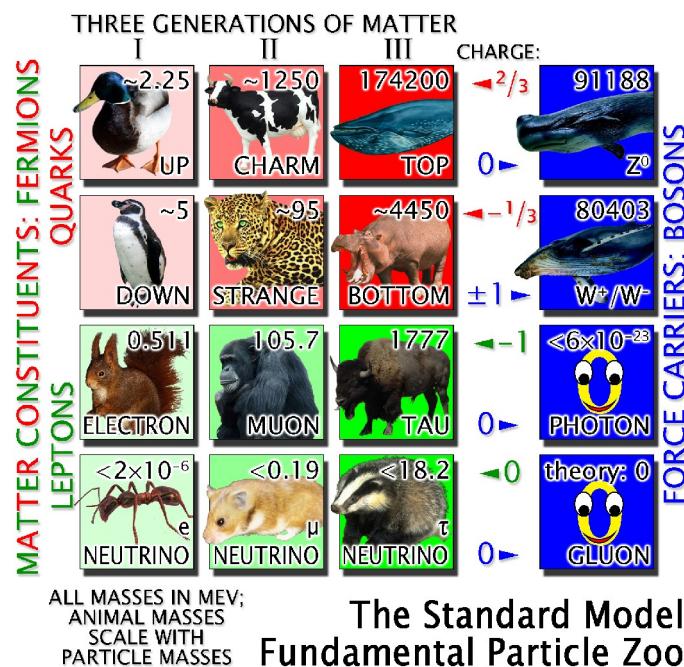


Figure 1-1 The Standard Model fundamental particle zoo

Forces between fermions are described by quantized fields with spin-1 boson field quanta, which mediate the forces through exchange between the interacting fermions. The electromagnetic force causes for example the emission of light from excited atoms. Its field quantum is the massless photon, which couples to all charged particles. The weak force interacts via the massive W^+ , W^- and Z^0 bosons between all fermions. It is, for example, the cause of nuclear beta decay. The strong force is mediated by eight

massless gluons between quarks and is responsible for binding nuclei. The gravitational force is described by the theory of general relativity and is not included in the Standard Model. It is responsible for the cohesion of orbs and their superior structures and acts on all particles with mass or energy. The postulated gravity exchange boson, the graviton, has not yet been observed. Since gravity is very weak in scales of particles and can be neglected in most cases, it is not further considered here. The four fundamental forces and their effect to the SM particles are illustrated in Figure 1-2.

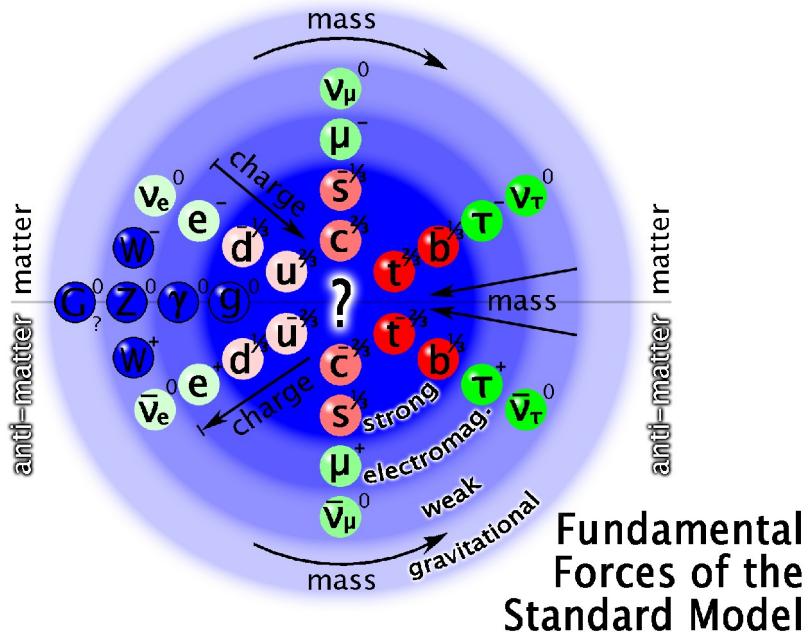


Figure 1-2 The Standard Model and the fundamental forces

The electric and magnetic force has been combined into a single electromagnetic theory by J.C. Maxwell in the 19th century [MAX73]. One of the achievements of the Standard Model is the unification of the electromagnetic and weak force to the electroweak force (see section 1.3). Physicists hope that this success can be repeated by a unification of the electroweak and the strong force in the so-called Grand Unified Theory (GUT). The combination of gravity with the GUT would be the next step of unification of the fundamental forces. This Theory Of Everything (TOE) would fulfill the desire of many physicists that all fundamental forces can be combined to a single primal one.

The number of generations can be measured with the peak cross section of the Z resonance. The peak cross section to a detectable final state f

$$\sigma_f^{peak} = \frac{12\pi}{M_Z^2} \frac{\Gamma_{ee}\Gamma_f}{\Gamma_z^2} \quad [1.1]$$

is sensitive to the number of light neutrino species, because

$$\Gamma_Z = \Gamma_{Z \rightarrow ee} + \Gamma_{Z \rightarrow \mu\mu} + \Gamma_{Z \rightarrow \tau\tau} + \Gamma_{Z \rightarrow qq} + N_\nu \Gamma_{Z \rightarrow \nu\nu} \quad [1.2]$$

Therefore the number of light neutrino species is given by:

$$N_\nu = \frac{(\Gamma_{Z \rightarrow \text{invisible}} / \Gamma_{Z \rightarrow \ell\ell})}{(\Gamma_{Z \rightarrow \nu\nu} / \Gamma_{Z \rightarrow \ell\ell})_{SM}} . \quad [1.3]$$

The numerator is the ratio of the Z decay width into invisible particles and the leptonic decay width. The denominator is the Standard Model value for the ratio of the partial widths to neutrinos and charged leptons. The result is $N_\nu = 2.9841 \pm 0.0083$ [LEP02], confirming three generations (with light neutrinos).

1.3 Unified Electroweak Force

Fermions are described in quantum field theories by spinor fields Ψ . They are functions of the four dimensional continuous Minkowski space-time coordinate x_μ . Since the weak interaction only couples to left-handed particles, they are described by left-handed fields Ψ_L . Right-handed particles are described by right-handed fields Ψ_R :

$$\Psi_L = \frac{1}{2}(1 - \gamma_5)\Psi , \quad \Psi_R = \frac{1}{2}(1 + \gamma_5)\Psi . \quad [1.4]$$

The electroweak interaction acts on weak-isospin left-handed doublets and right-handed singlets:

$$\begin{array}{ccc} \begin{pmatrix} u \\ d \end{pmatrix}_L \begin{pmatrix} c \\ s \end{pmatrix}_L \begin{pmatrix} t \\ b \end{pmatrix}_L & \begin{pmatrix} \nu_e \\ e \end{pmatrix}_L \begin{pmatrix} \nu_\mu \\ \mu \end{pmatrix}_L \begin{pmatrix} \nu_\tau \\ \tau \end{pmatrix}_L & I_3 = \begin{pmatrix} -\frac{1}{2} \\ +\frac{1}{2} \end{pmatrix} \\ \begin{matrix} u_R & c_R & t_R \\ d_R & s_R & b_R \end{matrix} & \begin{matrix} (\nu_{e,R} & \nu_{\mu,R} & \nu_{\tau,R})^* \\ e_R & \mu_R & \tau_R \end{matrix} & \begin{matrix} I_3 = 0 \\ I_3 = 0 \end{matrix} \\ * = \text{exist if } m_\nu \neq 0 & & \end{array} . \quad [1.5]$$

The weak-isospin I_3 is one of the three $SU(2)_L$ symmetry transformation generators, which form the weak-isospin operator $\mathbf{I} = (I_1, I_2, I_3)^t$. The generators can be written in matrix representation with the Pauli matrices σ_i as: $I_i = \frac{1}{2}\sigma_i$. Since the generators I_i do not commute: $[I_i, I_j] = i\epsilon_{ijk}I_k$ the gauge group is non-Abelian. The weak hypercharge Y is the generator of the $U(1)_Y$ symmetry group. It is connected with the weak-isospin and the electromagnetic charge Q by: $Q = I_3 + Y/2$. The dynamics of electromagnetic and weak forces can be determined by requiring the invariance of the free particle Lagrangian density:

$$\mathcal{L}_{\text{free}} = i\bar{\Psi}\gamma^\mu\partial_\mu\Psi \quad [1.6]$$

under the combined local phase (gauge) transformations of $SU(2)_L \times U(1)_Y$:

$$\Psi_L \rightarrow e^{ig_2\alpha(x)\mathbf{I} + ig_1\beta(x)Y}\Psi_L \quad \text{and} \quad \Psi_R \rightarrow e^{ig_1\beta(x)Y}\Psi_R \quad [1.7]$$

with an arbitrary three-component vector parameter $\alpha(x)$ and a one-dimensional function $\beta(x)$. To fulfill this demand the free Lagrangian has to be expanded by four spin 1 (vector) fields. The singlet field B_μ represents the $U(1)_Y$ transformation whereas the isos triplet field W_μ represents the $SU(2)_L$ transformation. Implementation of the fields is done by replacing the derivative in [1.6] by the covariant derivative:

$$D_\mu = \partial_\mu + i g_2 \mathbf{W}_\mu \cdot \mathbf{I} + i g_1 \frac{1}{2} B_\mu Y \quad [1.8]$$

and adding the kinetic energy term of the gauge fields:

$$E_{kin} = -\frac{1}{4} \mathbf{W}_{\mu\nu} \cdot \mathbf{W}^{\mu\nu} - \frac{1}{4} B_{\mu\nu} \cdot B^{\mu\nu} \quad [1.9]$$

with the field tensors:

$$\mathbf{W}_{\mu\nu} = \partial_\mu \mathbf{W}_\nu - \partial_\nu \mathbf{W}_\mu - g_2 \cdot \mathbf{W}_\mu \times \mathbf{W}_\nu \quad \text{and} \quad B_{\mu\nu} = \partial_\mu B_\nu - \partial_\nu B_\mu . \quad [1.10]$$

In the GSW⁴ [GLA61],[SAL68],[WEI67] Model the electromagnetic and weak interaction are described by one framework with quantized spin 1 fields and the gauge bosons as quanta of these fields. For Example a lepton-neutrino pair is described in this unified electroweak theory by:

$$\mathcal{L}_{GSW} = i \overline{\begin{pmatrix} \nu_e \\ e \end{pmatrix}}_L \gamma^\mu D_{\mu,L} \begin{pmatrix} \nu_e \\ e \end{pmatrix}_L + i \overline{\ell}_R \gamma^\mu \left[\partial_\mu - g_1 Y_R \frac{1}{2} B_\mu \right] \ell_R + E_{kin} . \quad [1.11]$$

1.4 Colored Strong Force

QCD⁵ is a quantum field theory based on the non-Abelian gauge color-field transformation group $SU(3)_c$. It attributes one of the three (color) charges: “red”, “green” and “blue” to each quark and one of their three anti-color charges to their anti-quarks. The number of colors can be experimentally approved by measuring the R-ratio:

$$R = \frac{\sigma(e^+ e^- \rightarrow q \bar{q})}{\sigma(e^+ e^- \rightarrow \mu^+ \mu^-)} = N_c \sum_q \left(\frac{Q_q}{e} \right)^2 \quad \text{with} \quad N_c = 3 . \quad [1.12]$$

This additional $SU(3)$ gauge degree of freedom (color charge) is necessary since otherwise particles like Δ^{++} , which consist of three quarks of the same type with parallel spin, would violate the Pauli principle. Through the different color of the quarks the total wave function becomes asymmetric, as required by the Pauli principle for fermions.

The strong force binds quarks together to form bounded-states called hadrons. All hadrons are color-singlets or “white”. Therefore quarks can only exist as free particles up to a hadronisation scale of ~ 1 fm. Mesons are built of a quark and an antiquark, whereas baryons consist of three quarks or three antiquarks. The exchange particles of the QCD are eight massless gauge bosons: the gluons. They are a consequence of invoking local gauge invariance of the Lagrangian. In contrast to weak interactions the gauge symmetry of $SU(3)_c$ is exact. The color charges can be interchanged without changing the physics, thus three quarks only differing in color have the same mass. The quantum chromodynamics is described by the gauge invariant Lagrangian:

⁴ Glashow, Weinberg, Salam

⁵ Quantum ChromoDynamics

$$\mathcal{L}_{QCD} = \bar{q} (i \gamma^\mu \partial_\mu - m) q - g_s (\bar{q} \gamma^\mu T_a q) G_\mu^a - \frac{1}{4} G_{\mu\nu}^a G_a^{\mu\nu} \quad [1.13]$$

with the strong coupling constant g_s , the quark field q , the eight gluon gauge fields G_μ^a and the eight generators of the $SU(3)_c$ group T_a . The gluons couple to the colors and each of them carries a color and an anti-color. Therefore they can interact with themselves. Three and four gluon vertices are allowed. This self-coupling is responsible for an anti-screening effect. Therefore the strength of the strong force decreases towards small distances and quarks are asymptotically free at short distances. On the other hand the strength of the strong force increases with increasing distance. This is the confinement of quarks in color neutral hadrons. As the distance between a quark-antiquark pair increases beyond the hadronisation scale, enough energy exists in the strong force field to produce a new quark-antiquark pair. This is called hadronisation.

1.5 Acquiring Mass by the Higgs Field

Fermions and bosons in SM concepts with Lagrangians like \mathcal{L}_{free} and \mathcal{L}_{GSW} are massless and obvious mass-terms are not gauge invariant. The minimal gauge invariant choice of mass generation is the addition of four scalar fields in terms of an isospin doublet $\Phi = (\phi^+, \phi^0)^t$ with complex fields resulting in a Lagrangian [WAG05]:

$$\mathcal{L}_{Higgs} = \mathcal{L}_{GSW} + |D_\mu \Phi|^2 - V(\Phi^\dagger \Phi) \quad [1.14]$$

with a scalar Higgs potential:

$$V(\Phi^\dagger \Phi) = \mu^2 \Phi^\dagger \Phi + \lambda (\Phi^\dagger \Phi)^2 . \quad [1.15]$$

A solution can be expanded with perturbation theory starting from the ground state of the system. This so-called vacuum expectation value of the Higgs potential:

$$|\Phi_{vacuum}| = \sqrt{-\frac{1}{2} \frac{\mu^2}{\lambda}} \quad [1.16]$$

can be different from zero by choosing appropriate parameters μ and λ . The scalar Higgs fields in Φ can be redefined such that new fields do have a zero vacuum expectation value. The symmetry of the Lagrangian is broken, due to the insertion of the new parametrization of the scalar fields into the Lagrangian. The Lagrangian is not an even function of the Higgs fields and the ground states do not share the symmetry of the Lagrangian anymore. Due to this spontaneous symmetry breaking mechanism one of the new Higgs fields (H^0) has acquired mass, whereas the other three fields remain massless [HIG64],[HIG66]. The electroweak gauge bosons acquire mass by using the spontaneous symmetry breaking mechanism on the Lagrangian \mathcal{L}_{Higgs} and requiring its local gauge invariance. However, the gauge bosons are not the included fields W_μ and B_μ , but instead a mixture:

$$W_\mu^\pm = \frac{(W_\mu^1 \mp i W_\mu^2)}{\sqrt{2}} \quad [1.17]$$

for the W^\pm bosons, the photon field A_μ and the Z^0 field Z_μ :

$$\begin{pmatrix} A_\mu \\ Z_\mu \end{pmatrix} = \begin{pmatrix} \cos\theta_W & \sin\theta_W \\ -\sin\theta_W & \cos\theta_W \end{pmatrix} \begin{pmatrix} B_\mu \\ W_\mu^3 \end{pmatrix} . \quad [1.18]$$

The Weinberg mixing angle is determined by the coupling constants g_1 and g_2 :

$$\frac{g_1}{g_2} = \tan\theta_W \quad [1.19]$$

and defines on his part the Z^0 to W^\pm mass ratio:

$$\frac{m_W}{m_Z} = \cos\theta_W \quad [1.20]$$

The leptons acquire their mass by the same spontaneous symmetry breaking if Yukawa interaction terms are added to the Lagrangian for the lepton and Higgs fields:

$$\mathcal{L}_{Yukawa}^\ell = -G_\ell \left[\bar{\ell}_R \left(\Phi^\dagger \begin{pmatrix} \nu_\ell \\ \ell \end{pmatrix}_L \right) + \left(\overline{(\nu_\ell, \ell)}_L^\dagger \Phi \right) \ell_R \right] . \quad [1.21]$$

The coupling constant G_ℓ describes the coupling of the lepton and its neutrino to the Higgs field, with the neutrinos assumed to be massless.

Quark mass is acquired by adding Yukawa interactions to the Lagrangian as well. In this case both weak-isospin doublet members need to receive mass. This is possible by constructing an additional conjugate Higgs multiplet $\Phi_C = i\tau_2 \Phi^* = (\phi^{0*}, -\phi^-)^t$. The Lagrangian Yukawa interaction terms for the quarks are:

$$\mathcal{L}_{Yukawa}^q = \sum_{i=1}^3 \sum_{j=1}^3 \tilde{G}_{ij} \overline{u_{iR}} \tilde{\Phi}^\dagger \begin{pmatrix} u_j \\ d_j \end{pmatrix}_L + G_{ij} \overline{d_{iR}} \Phi^\dagger \begin{pmatrix} u_j \\ d_j \end{pmatrix}_L + \text{h.c.} \quad [1.22]$$

The u_i are the weak eigenstates of the up-type quarks and the d_j the weak eigenstates of the down-type quarks. Through spontaneous symmetry breaking the Yukawa terms produce mass terms, which are given by:

$$\overline{(u_1, u_2, u_3)_R} M^u (u_1, u_2, u_3)_L^t \quad \text{and} \quad \overline{(d_1, d_2, d_3)_R} M^d (d_1, d_2, d_3)_L^t \quad [1.23]$$

with:

$$M_{ij}^u = |\Phi_{vac}| \cdot \tilde{G}_{ij} \quad \text{and} \quad M_{ij}^d = |\Phi_{vac}| \cdot G_{ij} \quad [1.24]$$

Thus, couplings between different generation quarks are allowed. The mass matrices can be diagonalized by unitary transformations. This changes the basis from weak eigenstates to mass eigenstates (identical to the flavour eigenstates). Transitions between mass eigenstates of different generations (generation mixing) is allowed through charged-current interactions, this means a exchange of a W^\pm . By setting weak and mass eigenstates of up-type quarks equal, it is possible to describe the mixing by mixing of the down-type quarks only:

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix}_L = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix}_L . \quad [1.25]$$

The weak force eigenstates d' , s' and b' and the strong force eigenstates d , s and b are coupled through the Cabibbo-Kobayashi-Maskawa (CKM) matrix [CAB63][KOB73]. The CKM matrix describes the transition probability from a quark q to a quark q' with the transition proportional to $|V_{qq'}|^2$.

The quantum of the Higgs field H^0 is the neutral scalar Higgs boson H^0 . It is the only Standard Model particle not yet observed. The experimental observation of the H^0 boson would be fundamental for a better understanding of the mechanism of electro-weak symmetry-breaking. The production rates and decay modes of the Higgs boson depend on its mass and are predicted by the theory. But the Higgs mass M_H is a free parameter of the theory. A lower limit of $114.4 \text{ GeV}/c^2$ at 95% CL is provided by LEP-2 direct measurements [LEP03]. A theoretical upper limit of about 1 TeV can be derived from unitarity arguments, for example [LEE77]. The upper limit from electroweak precision fits is 144 GeV (single-sided 95% CL derived from $\Delta\chi^2 = 2.7$) and increases to 182 GeV if the LEP-2 direct search limit is included [LEP07]:

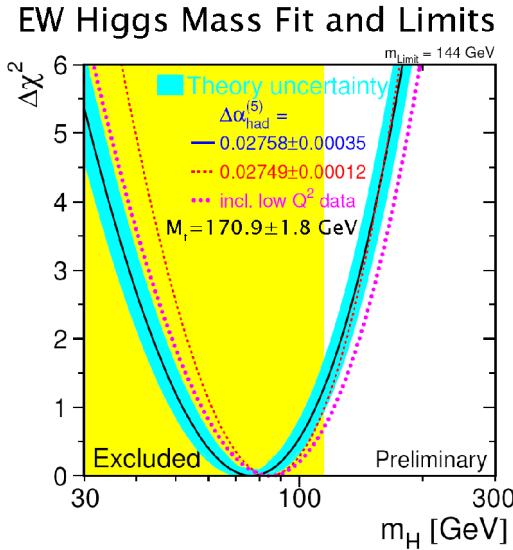


Figure 1-3 $\Delta\chi^2$ curve derived from high- Q^2 precision electroweak measurements, performed at LEP and by SLD, CDF, and D0, as a function of the Higgs-boson mass [LEP07]

Four different possible SM Higgs production channels at LHC are illustrated in Figure 1-4. Their cross-sections and overall events for an integrated luminosity of 100 fb^{-1} for Higgs masses between 90 and 1000 GeV are shown in Figure 1-4 as well. The SM Higgs is searched in different decay channels. Their choice depends on the expected signal rates and signal-to-background ratios [GIA00],[ATL99b]:

$$\bullet \quad M_H < 2 M_Z: \begin{cases} t\bar{t}H \rightarrow \ell b\bar{b} + X \\ H \rightarrow \gamma\gamma \\ H \rightarrow ZZ^* \rightarrow 4\ell \\ H \rightarrow WW^{(*)} \rightarrow \ell\nu\ell\nu \end{cases} \quad \text{direct \& associated } WH, ZH \& t\bar{t}H \quad [1.26]$$

$$\bullet \quad M_H > 2 M_Z: \begin{cases} H \rightarrow ZZ \rightarrow 4\ell \\ \left\{ \begin{array}{l} H \rightarrow ZZ \rightarrow \ell\ell\nu\nu \\ H \rightarrow ZZ \rightarrow \ell\ell jj \\ H \rightarrow WW \rightarrow \ell\nu jj \end{array} \right\} \end{cases} \quad \begin{array}{l} \text{'gold-plated'} \\ M_H > 300 \text{ GeV forward jet tag} \end{array} \quad [1.27]$$

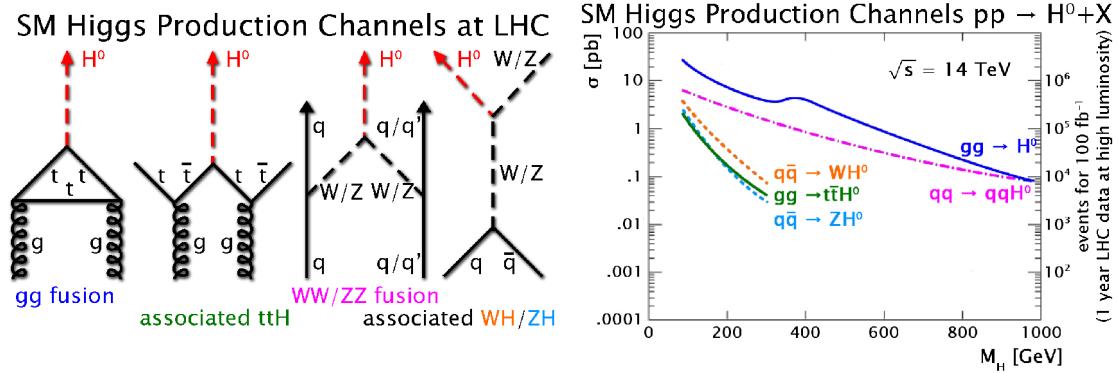


Figure 1-4 Standard Model Higgs boson production channels, their cross-sections and events for 100 fb⁻¹ for one year LHC operation at high luminosity [SPI98],[GIA00]

The expected H → γγ signal for an integrated luminosity of 100 fb⁻¹ and an assumed Higgs mass M_H = 120 GeV on top of the irreducible γγ background is shown in Figure 1-5. In supersymmetric theories the Higgs sector is extended to contain at least two doublets of scalar fields. In the minimal extension, the MSSM⁶ model [NIL84], five physical Higgs particles exist: the two CP-even Higgs bosons H and h, the CP-odd Higgs boson A, and the two charged Higgs bosons H[±]. The structure of the Higgs sector at tree-level is determined by two parameters. Typically these are chosen to be M_A and tan(β), the ratio between the vacuum expectation values of the two Higgs doublets. In Figure 1-6 the expected M_{μμ} distributions of the reducible background (shaded histogram), of the overall background (dashed curve) and of the sum of H/A → μμ signal and background (solid histogram) are shown for an integrated luminosity of 30 fb⁻¹ and tan(β) = 30.

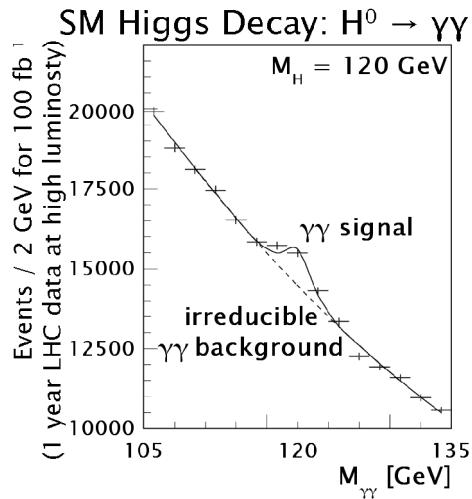


Figure 1-5 Expected M_{γγ} distribution for H → γγ decay [ATL99b]

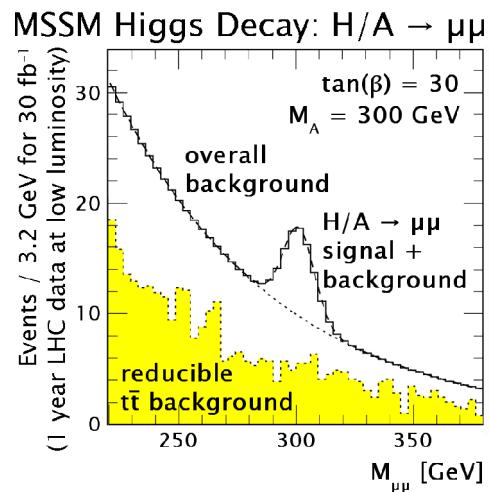


Figure 1-6 Expected M_{μμ} distribution for H/A → μμ decay [ATL99b]

Chapter 2

Basic Principles of Semiconductor Detectors

If an ionizing particle penetrates a semiconductor detector it ionizes the semiconductor atoms and produces pairs of movable electrons and holes along its track. The number of electron-hole pairs is proportional to the energy loss. An externally applied electric field separates the charge carriers before they recombine and pulls them to the surface of the detector. The collected charge on the surface electrodes produce a current pulse, whose integral is a measure for the deposited energy by the incident particle. The electrode pulses can be detected using charge sensitive amplifying electronics.

Intrinsic semiconductor materials like silicon have properties that make them particularly suitable for the detection of ionizing radiation and photons [LUT99]:

- small band gap \Rightarrow required average energy to create an electron-hole pair (see section 2.3) is low (an order of magnitude smaller than the ionization energy of gases) \Rightarrow large number of charge carriers per unit energy loss of ionizing particles \Rightarrow high intrinsic energy resolution
- high density (2.33 g/cm^3) \Rightarrow large energy loss per traversed material length (3.8 MeV/cm for MIPs⁷) of ionizing particles \Rightarrow thin detectors possible \Rightarrow low interaction length detectors possible
- small range of δ -electrons \Rightarrow low shift of the primary ionization center of gravity from the track \Rightarrow high spatial resolution (few μm) possible
- high mobility of electrons ($\mu_n = 1450 \text{ cm}^2/\text{Vs}$) and holes ($\mu_p = 450 \text{ cm}^2/\text{Vs}$) \Rightarrow rapid charge collection ($\sim 10 \text{ ns}$) \Rightarrow high rate compatibility
- possibility of creating fixed space charges by doping \Rightarrow possibility of modifying detector properties by changing the doping structure (no analogy in gas detectors)
- feasibility of building integrated circuit electronics from silicon \Rightarrow integration of amplifier and readout electronics in the detector is practical

Due to their unmatched energy and spatial resolution and their excellent response time semiconductor detectors are popular in many high-energy physics applications. The usage of semiconductor microtechnology for common consumer electronics chips allow reliable large-scale production of detectors at acceptable cost.

7 Minimum Ionizing Particles (see section 2.2)

2.1 Energy Loss of Photons in Matter

The interaction between photons, the quantum of the electromagnetic radiation, and matter mainly occurs by three different effects [LEO94]:

- The photoelectric effect is a interaction in which the entire energy of an incident photon is transferred to a bound electron. A nucleus is required to absorb the recoil momentum, since a free electron cannot absorb a photon while conserving both energy and momentum of the system. If the absorbed energy is bigger than the binding energy of the electron in the system (e.g. an atom) the electron can escape. The resulting energy of the free electron is the binding energy of the electron subtracted from the energy of the photon:

$$E_e = \hbar\omega - E_{binding} \quad [2.1]$$

The energy of this electron is distributed by impacts with other bound electrons until the complete energy of the gamma ray is absorbed by the material.

- Compton / Thomson / Rayleigh scattering is the interaction of a photon with a free electron / a free electron in the classical limit / a free atom as a whole. Even if the electron is bound it can be treated as approximatively free if the photon energy is high with respect to the binding energy. The energy of the photon after this elastic Compton scattering is:

$$\hbar\omega' = \frac{\hbar\omega}{1 + \gamma(1 - \cos\theta)} \quad \& \quad \gamma = \frac{\hbar\omega}{m_e c^2}; \quad \begin{aligned} \hbar\omega &: \text{initial energy} \\ m_e &: \text{electron mass} \\ c &: \text{speed of light} \end{aligned} \quad [2.2]$$

where θ is the change of the photon angle. The cross section is described by the Klein-Nishina formula (e.g. [LEO94]-2.107). Thomson and Rayleigh scattering are characterized by a change of momentum only. The energy of the photon is unchanged and the atom is neither excited nor ionized.

- Pair production describes the conversion of a photon into an electron-positron pair. Since at least the energy for the mass of the new generated pair is required the pair production has a photon energy threshold of 1.022 MeV (e^-e^+ pair rest mass). A third body, usually a nucleus, is necessary in order to conserve momentum. Pair production cross section is described by the Bethe-Heitler formula [BEH34].

The total or sum absorption coefficient for all three processes is:

$$\mu = \mu_{photo} + \mu_{Comp} + \mu_{pair} \quad \& \quad \mu = \frac{\sigma N_a \rho}{A}; \quad \begin{aligned} \sigma &: \text{cross section} \\ N_a &: \text{Avogadro's Number} \\ \rho &: \text{density of material} \\ A &: \text{molecular weight} \end{aligned} \quad [2.3]$$

The dominant process depends on the photon energy and on the nucleus charge Z of the absorber material as shown in Figure 2-1. For silicon ($Z=14$) the dominant effect for photon energies under 50 keV is the photoelectric effect, whereas over 10 MeV the pair production is the dominant effect. In between 50 keV and 10 MeV the Compton

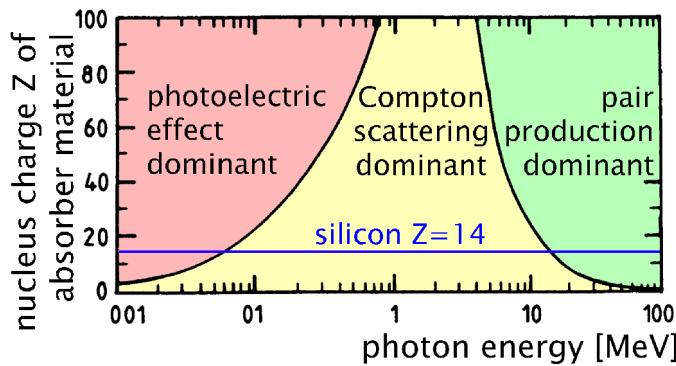


Figure 2-1 Dominant photon-matter interaction depending on the photon energy and on the nucleus charge Z of the absorber material [GRU96]

effect is dominant. Interacting photons are either absorbed or deflected by a big angle from their incident direction. Therefore the intensity of a γ -ray decreases like:

$$I = I_0 e^{-\mu x} ; \quad I_0 : \text{initial intensity} \\ x : \text{absorber thickness} \quad [2.4]$$

Compared with cross sections for inelastic scattering of charged particles the photon cross sections are much lower. Thus the detection probability is much lower as well. For example the absorption coefficient for 59.5 keV γ s from a ^{241}Am source is $0.3 \text{ cm}^2 \text{ g}^{-1}$. Thus the detection probability in a 300 μm silicon detector is only 2% [OVE98]. On the assumption that the electron does not leave the detector γ -sources are suitable for calibration purpose, because the entire photon energy can be detected in the sensor.

2.2 Energy Loss of Charged Particles in Matter

Charged particles traversing matter lose energy and are deflected from their incident direction. These effects are the result of many different processes:

- inelastic scattering from atomic electrons
- elastic impacts with nuclei
- emission of Čerenkov radiation
- nuclear reactions
- bremsstrahlung

Electrons and positrons lose the main part of their energy by bremsstrahlung (energy loss $\propto 1/m^2$) because of their low mass. At higher energies (heavy particles) the inelastic collision is almost solely responsible. The energy loss per length of a particle by inelastic, elastic and Čerenkov processes is described by the Bethe-Bloch formula. It can be improved by density effect and shell corrections (e.g. [LEO94]-2.27). The energy dependence of dE/dx is shown in Figure 2-2. The Bethe-Bloch formula is plotted for several particles as a function of their kinetic energy. In Figure 2-3 the dE/dx energy dependence for silicon is shown. At non-relativistic energies the dE/dx

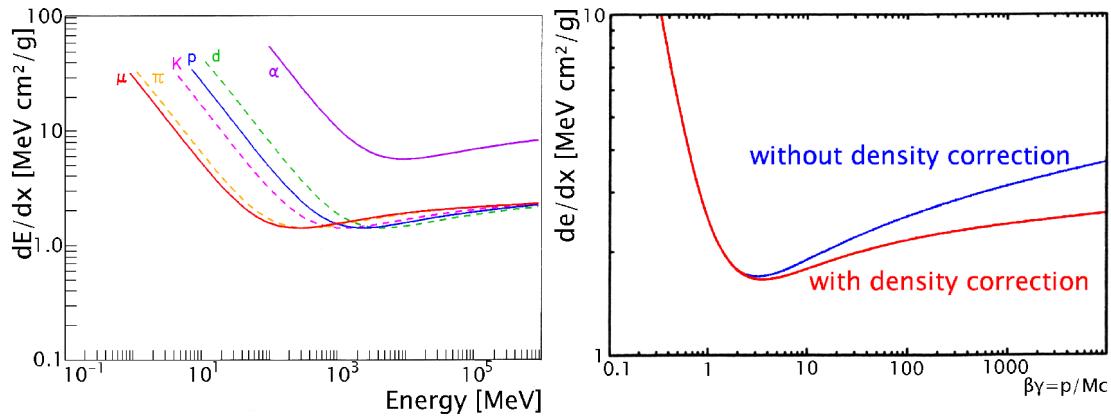


Figure 2-2 Schematic dE/dx as function of kinetic energy for different particles [LEO94]

Figure 2-3 dE/dx for silicon as function of kinetic energy for heavy charged particles [KEI01]

function is dominated by an overall $1/\beta^2$ factor and therefore decreases with increasing velocity. Depending on the nucleus charge number Z a minimum is reached at a velocity of about $0.96 c$. Particles with the corresponding energy are called MIPs. Above this point the $1/\beta^2$ term becomes almost constant and the dE/dx increases again due to its logarithmic dependence. This is called relativistic rise.

In thick absorbers (with a multiplicity of interactions) the energy loss can be described as a Gaussian distribution. The Gaussian curve is centered at the mean and most probable value, which are equal. These can be calculated with the Bethe-Bloch formula. In thin absorbers there is a lower probability for large energy transfers to atomic electrons. These electrons are called δ -electrons and can additionally ionize other atoms. The resulting asymmetry can be described by a Landau distribution. The energy loss of a MIP in a $250 \mu\text{m}$ thick silicon sensor is shown in Figure 2-4. Its mean energy loss is higher than the most probable energy loss. This results in a mean amount of 27,000 created electron-hole pairs for a MIP in this detector whereas the most probable amount is 19,400 electron-hole pairs.

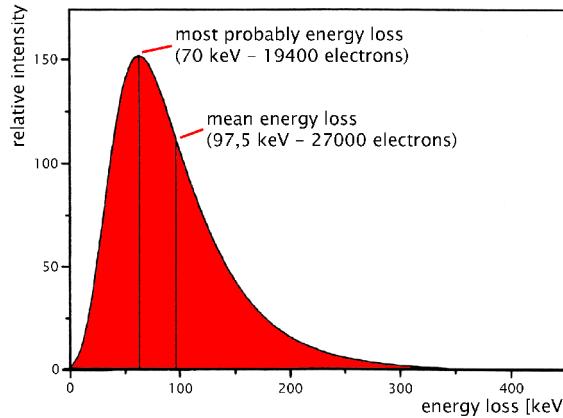


Figure 2-4 Mean and most probably energy loss of a MIP in a $250 \mu\text{m}$ thick silicon sensor [KOH02]

2.3 Electron-hole Pair Production Energy

Energy deposited in the semiconductor sensor material excites electrons from the semiconductor conduction band to the valence band. Electron-hole pairs are created and lattice vibrations are excited. This excitation leads to a higher creation energy for electron-hole pairs compared with the band gap energy of the semiconductor (1.12 eV for silicon at 300°K). A mean electron-hole pair production energy of 3.63 eV has been measured for silicon [ABS80]. A linear fit of production energy measurements for different semiconductor results into:

$$\varepsilon = 1.91 \cdot E_g + 1.55 \text{ eV} ; \begin{array}{l} \varepsilon : \text{mean pair production energy} \\ E_g : \text{band gap energy} \end{array} \quad [2.5]$$

With this equation the electron-hole pair production energy for silicon can be calculated to a value of 3.69 eV.

2.4 Functionality of Semiconductor Detectors

Electrons and holes created by a charged particle or photon in the semiconductor would recombine after a short time. This would lead to a loss of all information about the traversing particle. Therefore an external voltage is applied to the semiconductor to separate the charge carriers. The charge carriers with opposite charge polarities are drifting in the electric field to the opposite sides of the semiconductor crystal. On either one or both sides of the semiconductor crystal electrodes are located, which are connected to amplifier and readout electronics.

A general problem of particle detection with intrinsic semiconductors is the high noise provoked by the existence of electron-hole pairs in the sensor material. These are neither created by a charged particle nor a photon, but by thermal excitation. This electron-hole pairs also recombine and an equilibrium concentration is established under stable environmental conditions. The concentration of these thermal charge carrier pairs in an intrinsic semiconductor can be calculated by Fermi-Dirac statistics (e.g. [LEO94] formula 10.1):

$$n_i = \sqrt{N_C N_V} \exp\left(\frac{-E_g}{2kT}\right) ; \begin{array}{l} N_C : \# \text{ of states in the conduction band} \\ N_V : \# \text{ of states in the valence band} \\ k : \text{Boltzmann constant} \\ T : \text{temperature} \end{array} \quad [2.6]$$

Typical concentration values for silicon at room temperature are in the region of $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$. Due to the non-negligible amount of charge carrier pairs in the intrinsic semiconductor its finite resistivity (230 kΩcm for silicon) leads to an intrinsic current flow if a voltage is applied to the semiconductor crystal. The drift velocity of electrons and holes through a semiconductor under the influence of an externally applied electrical field can be written as:

$$v_n = \mu_n E_{ext} \quad \& \quad v_p = \mu_p E_{ext} ; \quad E_{ext} : \text{magnitude of external electric field} \quad [2.7]$$

Typical mobilities in silicon at room temperature are about $1450 \text{ cm}^2/\text{Vs}$ for electrons and $450 \text{ cm}^2/\text{Vs}$ for holes. Since electrons and holes are discrete charge carriers the intrinsic current shows shot noise, proportional to the intrinsic current strength. Depending on the resistivity of the semiconductor material the amplitude of this intrinsic noise can be the same order of magnitude as a signal generated by a penetrating charged particle or photon. Therefore this semiconductor is not suitable for particle detection.

It is possible to increase the signal-to-background ratio by using a junction made of p- and n-doped semiconductors. The equilibrium of holes and electron numbers in an intrinsic semiconductor can be changed by small amounts of impurity atoms. Compared to the bulk material, typically impurity (doping) atoms with one more (p-doped) or less (n-doped) valence electron in their outer atomic shell are used. For silicon this means either pentavalent donor atoms or trivalent acceptor atoms. The doping atoms are integrated in the crystal lattice and replace bulk material atoms. The crystal lattice structures of n-type and p-type doped silicon are schematically shown in Figure 2-5 a). The creation of a filled discrete donor energy level close to the conduction band ($\sim 0.05 \text{ eV}$ for silicon) and an empty discrete acceptor energy level close to the valence band are shown in Figure 2-5 b). The donor level is filled due to thermal excitation. Free movable electrons in the conduction band of the n-doped and free movable holes in the valence band of the p-doped semiconductor are the result.

The formation of a pn junction is illustrated in Figure 2-5 c). It creates a depletion zone at the interface between both different doped materials. The band structures of the semiconductors are deformed until both Fermi levels E_F have reached the same energy. The different concentrations of holes and electrons in both materials lead to an initial diffusion of electrons towards the p-side and a diffusion of holes towards the n-region. These holes capture electrons on the n-side whereas the diffusing electrons fill holes in the p-region. As a consequence of this initial diffusion the recombination causes a charge build-up on both sides of the junction. The p-side becomes negative and the n-region positive. An electric field gradient across the junction is set up, which halts the diffusion process. The charge density and electrical field profile are schematically illustrated in Figure 2-5 e). A potential difference across the junction is known as the contact potential V_C . Its value is $\sim 0.7 \text{ V}$ for silicon. The region of immobile space charge is called depletion zone. It is particularly attractive for radiation detection, since any electron or hole created in this region will be swept out by the electric field and can be detected by electronics connected with electrodes on both sides of the junction.

The goal is to enlarge the depletion zone and thus the sensitive volume for radiation detection. This can be reached by applying reversed-bias voltage to the semiconductor as visible in Figure 2-5 d). The width of both depletion layers can be calculated with:

$$x_n = \sqrt{\frac{2 \epsilon (V_C + V_{bias})}{e N_D \left(1 + \frac{N_D}{N_A}\right)}} \quad \& \quad x_p = \sqrt{\frac{2 \epsilon (V_C + V_{bias})}{e N_A \left(1 + \frac{N_A}{N_D}\right)}} ; \quad \begin{aligned} \epsilon &: \text{dielectric const.} \\ e &: e^- \text{ charge} \\ N_D &: \text{donor conc.} \\ N_A &: \text{acceptor conc.} \end{aligned} \quad [2.8]$$

The combined depletion zone grows with applied bias voltage. High bias voltages

Doped Semiconductors and the np Junction

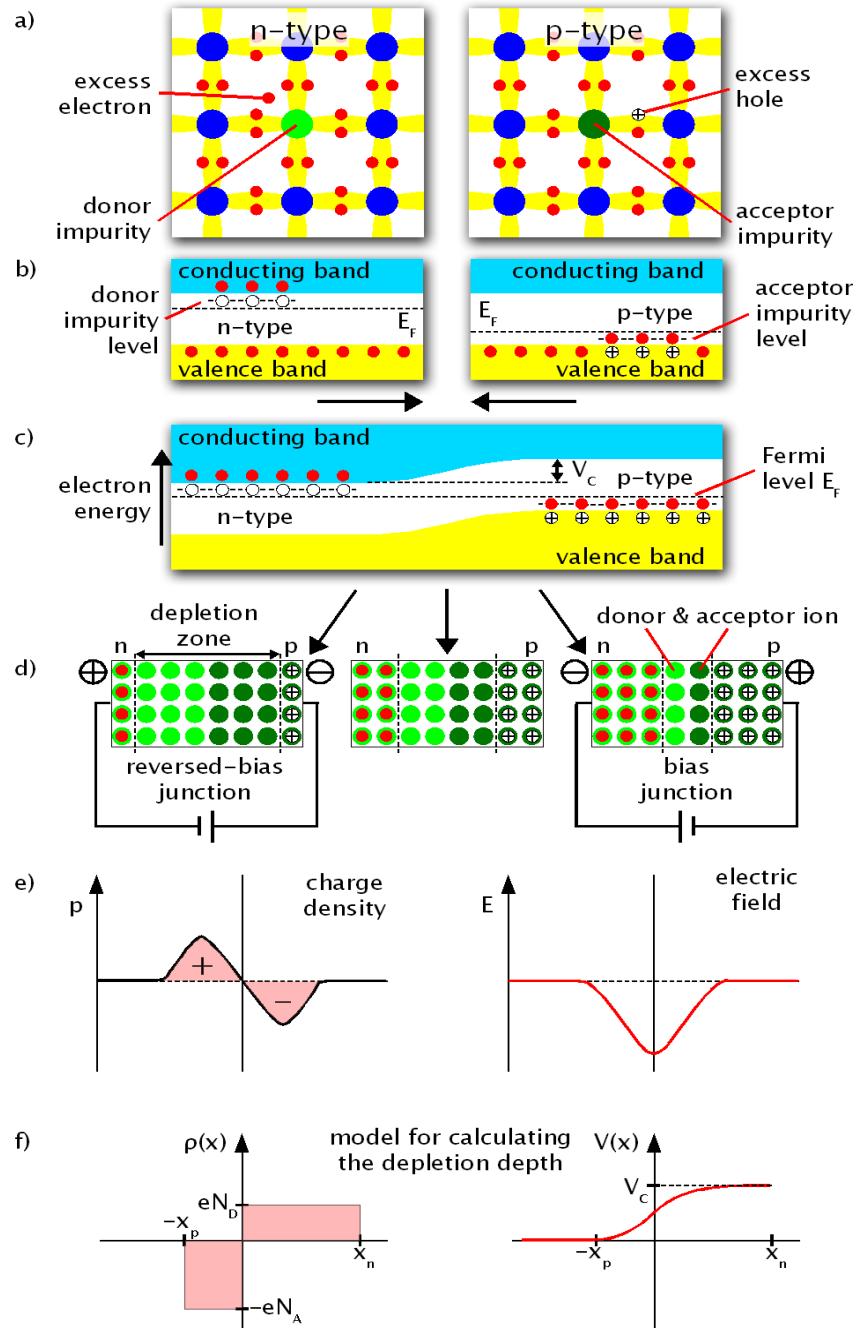


Figure 2-5 a) Donor and acceptor impurity atoms in silicon crystal lattice forming n-type and p-type semiconductor **b)** Creation of donor and acceptor impurity levels in the energy gap **c)** Contacting the n- and p-doped semiconductor and creation of the contact potential **d)** Biasing the np junction **e)** Charge density and electric field intensity **f)** Model for calculating the depletion depth of a np junction

provide a more efficient charge collection due to a reduced charge trapping probability (see section 2.5). The applicable bias voltage is limited by the resistance of the semiconductor, because at some point the junction breaks down and becomes conductive.

Figure 2-6 illustrates the basic configuration and functionality of a semiconductor junction diode detector. Onto both sides of the semiconductor electrodes are fitted. Contacts between semiconductors and most metals form a rectifying junctions with depletion zones extending into the semiconductor. To inhibit this formation heavily doped regions of n^+ and p^+ material are used between the metal electrodes and the bulk semiconductor. Caused by the high dopant concentration the depletion depth, regarding [2.8], is approximatively zero and therefore the contact has an ohmic characteristic.

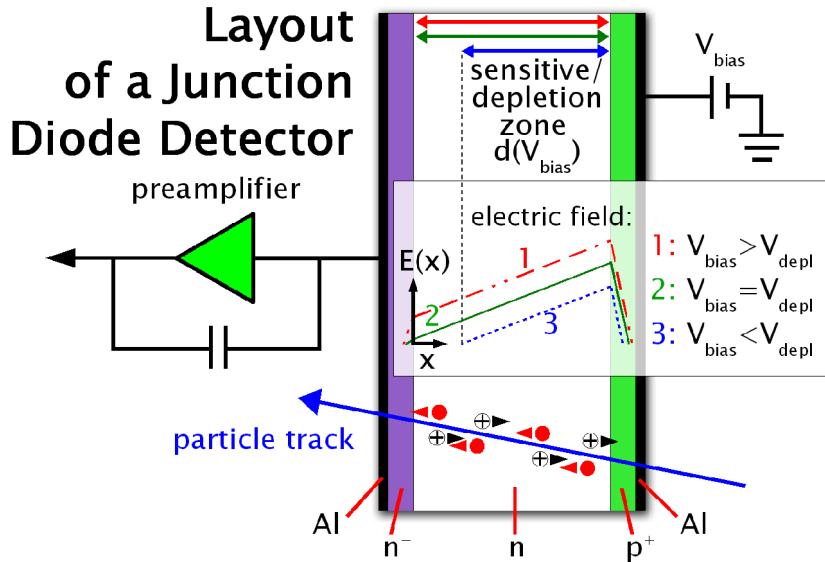


Figure 2-6 Layout and functionality of a semiconductor junction diode detector

The detector is reversed-biased through the p^+ side with a negative voltage, fully depleting the detector if the bias voltage is higher than the full depletion voltage V_{depl} . The sensitive volume does not contain majority charge carriers. The full depletion voltage can be (neglecting the contact voltage) calculated with:

$$V_{depl} = \frac{d^2 e}{2 \epsilon} \frac{N_A N_D}{(N_A + N_D)} ; \quad d : \text{thickness of detector (n layer)} \quad [2.9]$$

The electric field in the depletion zone is shown in Figure 2-6 as well. Its strength is:

$$E(x) = - \left[\frac{V + V_{depl}}{d} - \frac{2xV_{depl}}{d^2} \right] ; \quad x : \text{depth in detector} \quad [2.10]$$

If a particle penetrates the detector it creates electron-hole pairs in the depletion zone. Driven by the electric field the holes drift towards the p^+ side and the electrons in n^+ direction. By integration of the drift velocity:

$$v_{n/p} = \mp \mu_{n/p} E(x) \quad [2.11]$$

the depth of a charge carrier as a function of time can be obtained:

$$x_{elh} = \frac{d(V + V_{depl})}{2V_{depl}} + \left[x_0 - \frac{d(V + V_{depl})}{2V_{depl}} \right] \exp \left(\mp \frac{2\mu_{n/p} V_{depl} t}{d^2} \right) ; \quad x_{elh}(t=0) = x_0 \quad [2.12]$$

The related velocity is:

$$\frac{dx_{e/h}}{dt} = \pm \mu_{n/p} \left[\frac{2 V_{depl} x_0}{d^2} - \frac{V + V_{depl}}{d} \right] \exp \left(\frac{\mp 2 \mu_{n/p} V_{depl} t}{d^2} \right) \quad [2.13]$$

Electrons drift until they reach the surface $x_e(t_e) = d$, holes respectively the surface $x_h(t_h) = 0$. The resulting drift times are:

$$t_e = \frac{d^2}{2 \mu_n V_{depl}} \ln \left[\frac{V + V_{depl}}{V - V_{depl}} \left(1 - \frac{x_0}{d} \frac{2 V_{depl}}{V + V_{depl}} \right) \right] \quad [2.14]$$

$$t_h = \frac{d^2}{2 \mu_p V_{depl}} \ln \left(1 - \frac{x_0}{d} \frac{2 V_{depl}}{V + V_{depl}} \right) \quad [2.15]$$

The current induced by these moving charges (q) is:

$$i(t) = \frac{q}{d} \frac{dx}{dt} = \frac{q}{d} \left(\frac{-dx_e}{dt} + \frac{dx_h}{dt} \right) = \frac{q}{d^2} \left(2 V_{depl} \frac{x_0}{d} - (V + V_{depl}) \right) \\ \times \left[\mu_n \exp \left(\frac{-2 \mu_n V_{depl} t}{d^2} \theta(t_e - t) \right) + \mu_p \exp \left(\frac{2 \mu_p V_{depl} t}{d^2} \theta(t_h - t) \right) \right] \quad [2.16]$$

and can be measured by a charge sensitive preamplifier. Velocity saturation is neglected in this calculation.

2.5 Radiation Damages

High energy particles do not only lose energy by ionization. Their energy additionally decrease by NIEL⁸ processes. This means the particles transfer energy and momentum to a semiconductor atom as well. If the energy transfer is higher than the lattice binding energy of the atom, this PKA⁹ leaves its own lattice position. Basically an interstitial, a silicon atom on a non regular lattice position, and a vacancy, a hole in the lattice, are created. If the PKA energy is high enough it can remove further semiconductor atoms from the lattice and generates clusters of mentioned defects. The recombination of interstitials with vacancies is possible and depends on their mobility. Hence all lattice errors should more or less fast destroy each other, but stable lattice damages can develop for example with crystal impurities [WUN96a].

If donor or acceptor atoms are involved in crystal defects they lose their doping function. On the other hand additional donors and acceptors can develop if impurities like oxygen or carbon are forming crystal defects. These effects change the effective doping concentration of the semiconductor. Therefore the following dependence can be expected:

$$N_{eff}(\Phi) = N_{D,0} e^{-c_D \Phi} - N_{A,0} e^{-c_A \Phi} + b_D \Phi - b_A \Phi \quad ; \quad \begin{array}{lcl} N_{0,D} & : & initial N_D \\ N_{0,A} & : & initial N_A \end{array} \quad [2.17]$$

⁸ Non Ionizing Energy Loss

⁹ Primary Knock on Atom

Φ is the particle fluence normalized to an equivalent fluence of 1 MeV neutrons, b_A (b_D) the rate of radiation-induced acceptor (donor) increase and c_A (c_D) the acceptor (donor) removal rate. Measurements with n-doped silicon show that this formula can be simplified by neglecting the degradation of acceptors and combining the linear terms to a fluence proportional formation rate b of acceptor states:

$$N_{\text{eff}}(\Phi) = N_{D,0} e^{-c\Phi} - N_{A,0} - b\Phi \quad [2.18]$$

c is the donor removal rate. The detector and fluence independent constants b and c have been determined from fits to experimental data [WUN92]:

$$b = 7.94 \cdot 10^{-2} \text{ cm}^{-1} \pm 8.0\% \quad \& \quad c = 3.54 \cdot 10^{-13} \text{ cm}^2 \pm 4.5\% \quad [2.19]$$

As a consequence of the varying effective doping concentration, the depletion voltage [2.9] changes. With high enough fluences a type inversion of a n-doped semiconductor in an effective p-doped material occurs. This changes the entire detector behavior.

The leakage current is provoked by emission of electrons into the conducting and holes into the valence band. The probability of such emissions depends on the exponent of the defect energy level position in the gap. Thus energy levels in the middle of the gap (deep levels) preferably contribute to the leakage current. Due to the proportionality of the defect density to the fluence, a linear dependence can be found as expected [WUN96a]:

$$\frac{\Delta I}{V} = \alpha \Phi \quad \text{with} \quad \alpha = 8 \cdot 10^{-17} \text{ Acm}^{-1} \quad [2.20]$$

Increased leakage current leads to an increased noise and a high power consumption in the readout electronics, thus extended cooling is required.

Defect energy levels close to either the conduction or valence band (shallow traps) can either capture (trapping) or emit charge carriers. If such a shallow trap captures and emits a charge carrier delayed (detrapping), the charge carrier is lost for the signal and the signal height decreases. Depending on the detrapping delay time the signal-to-noise ratio can decrease significantly. The trapping and detrapping processes can be quantitatively described by the mean lifetime of charge carriers and the mean retention period in the defect [WUN92]. Effective trapping times τ_{eff} for electron and holes are used to characterize the trapping effect and to calculate the charge $q(t)$ which remains from the initial deposited charge q_0 after the time t :

$$q_{e,h}(t) = q_{0,e,h} \exp\left(-\frac{t}{\tau_{\text{eff},e,h}}\right) \quad \text{with} \quad \frac{1}{\tau_{\text{eff},e,h}} \propto N_{\text{defects}} \quad [2.21]$$

While the radiation-induced crystal damages in the bulk are caused by non-ionizing energy loss, the surface damages are caused by ionization within the passivation layers (IEL¹⁰). Surface damages include all radiation-induced damages in the surface passivation layers (e.g. SiO₂) and their interfaces. Electrons and holes created by ionizing radiation in the passivation have a high probability to recombine in the absence of an electric field. In the presence of an electric field the number of free charge carriers in the passivation increases with the field strength. Since in SiO₂ the electron mobility is about 10⁶ times higher than the hole mobility, the electrons are

swept out almost immediately leaving the holes behind. Depending on the electric field orientation more or less holes reach the Si/SiO₂ interface. If a hole is trapped at the interface it causes surface defects. Caused by the positive charging of the oxide, an electron accumulation underneath the interface occurs and therefore the electric field configuration at the interface is affected. The strength of this influence additionally highly depends on the sensor layout. A smart sensor layout can minimize the surface damage effect and improve the break-through stability [WUN96b].

Radiation damages in irradiated semiconductors anneal with time and temperature, caused by thermal excitation. This annealing changes the detector properties with a velocity depending on the temperature. Basically observed annealing effects in type inverted silicon detectors are decreasing of the effective doping concentration and thus decreasing of the depletion voltage, decreasing of leakage current [WUN96a] and change of the effective trapping times for electrons and holes [KRA04]. After a relative short period of beneficial annealing with decreasing effective doping concentration an increase of the effective doping concentration and the depletion voltage can be observed. This phenomenon is denoted as reverse annealing. To improve the radiation tolerance of semiconductor detectors, they are cooled after the beneficial annealing to increase the time constant of the reverse annealing (see section 4.3.2).

2.6 Strip and Pixel Detectors

With semiconductor detectors position information of traversing particles can be obtained by segmentation of one or both electrodes (the highly doped region contact implantations and the attached metal layer). Three types of position sensitive segmented semiconductor detectors are illustrated in Figure 2-7. A single sided strip detector provides only an one dimensional position information. If both electrodes are segmented into non parallel strips, two dimensional position information is available. This type of layout is called matrix detector as well.

Two dimensional position information can also be obtained if two single sided strip detector are mounted with a stereo angle behind each other. Since the two used strip sensors have to be processed only from one side this technique is cheaper than double sided processed matrix detectors. Typical strip widths (pitch) are 10-100 µm and the angle between the different oriented strips is typically 90°. Lower stereo angles can be used to increase the spatial resolution in one direction at the cost of the spatial resolution in the orthogonal direction. An advantages of strip detectors is that the readout electronics can be attached at one or two of the non-electrode faces of the sensor. This avoids expensive connection techniques at the electrode faces.

The usability of strip detectors for two dimensional position information is limited in high particle flux environments due to the ambiguity problem of multiple hit events. If $n = 2$ or more particles hit the same sensor without the possibility to separate the strip signals in time $p = n!$ possible hit allocations are possible. All possible hit allocations for the two and three hit case are represented by different colors in Figure 2-8. From boolean hit information it is not possible to distinguish between the n real and the $p-n$ ghosthits. If pulse hight information with equal amplification for each strip is

Position Sensitive Semiconductor Layout Examples

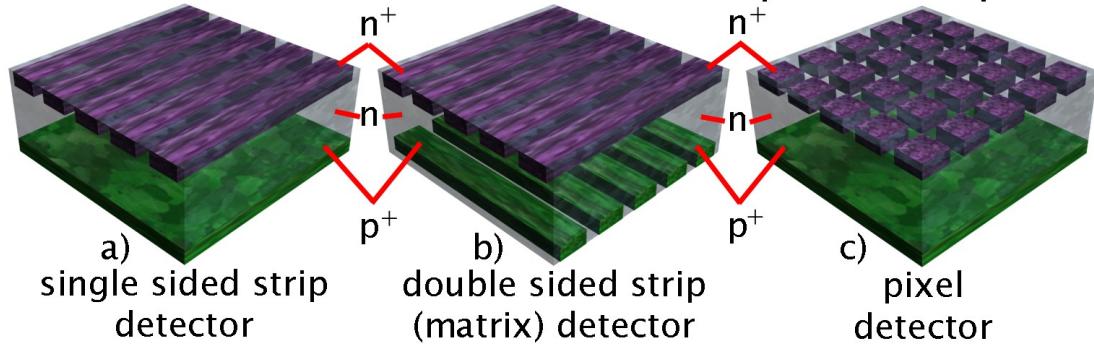


Figure 2-7 Improvement of space resolution: a) 1 dimensional space coordinates for single sided strip detector b) Pseudo 2 dimensional space coordinates for double sided strip detector c) Real 2 dimensional space coordinates for pixel detector

provided by the readout electronics, the ambiguity for small hit numbers can be resolved by comparing pulse heights. The crossings of equal pulse heights represent the realized hit allocation (black circles for $n=2$ case in Figure 2-8). The ambiguity can be solved even for high hit numbers with multiple layers of strip detectors but on the cost of high computational effort.

Ambiguity Problem of Strip Detectors

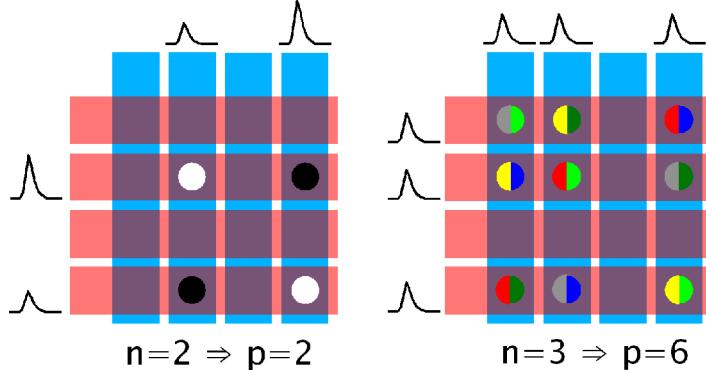


Figure 2-8 Ambiguity of particle hits with strip detectors

To obtain two dimensional information for high particle fluxes one of the electrodes has to be segmented in both directions. A main challenge of these pixel detectors is that the number of electronic channels does not only increase with one of the detector dimension (like for strip detectors) but with the area of the detector. Therefore the individual pixels have to be connected to the front-end amplifier and readout electronics at the segmented electrode face of the sensor. This layout is called hybrid pixel detector. Two connection techniques for hybrid pixel detectors are described in section 4.3.1. Another possibility is to directly integrate parts or the entire front-end electronics in the sensor. This technology is called monolithic pixel detector.

Additional advantages of pixel detectors are the distribution of the sensors leakage current to all pixels and the reduced capacity seen by the individual preamplifiers. Thus pixel detectors can cope with high leakage currents (e.g. induced by irradiation) and the noise of preamplifiers is reduced.

The expected spatial resolution for strip and pixel detectors can be calculated for the noiseless and single hit case as the standard deviation of a rectangular distribution with the width of the pixel or strip pitch:

$$\sigma = \sqrt{\frac{1}{p} \int \left(\frac{p}{2} - x \right)^2 dx} = \frac{p}{\sqrt{12}} ; \quad p : \text{pixel or strip pitch} \quad [2.22]$$

2.7 Induced Current and Charge on Segmented Detectors

The instantaneous induced current on a given electrode can be calculated with the Ramo method [RAM39]. This uses a weighting potential Φ , a solution of the Poisson equation $\nabla^2 \Phi = 0$ with the boundary condition $\Phi = 1$ for the considered electrode and $\Phi = 0$ for all other electrodes. This weighting potential depends only on the geometrical allocation of the electrodes.

The current induced by a moving charge carrier on the electrode is given by:

$$i = -q \left[\frac{\partial \Phi}{\partial x} \frac{dx}{dt} \right] = qvE_v ; \quad \begin{aligned} q &: \text{charge on charge carrier} \\ v &: \text{velocity of charge carrier} \\ E_v &: \text{electric field component in } v \text{ direction} \end{aligned} \quad [2.23]$$

Thus the induced charge can be calculated:

$$\Delta Q = q(\Phi_f - \Phi_i) ; \quad \begin{aligned} \Phi_i &: \text{initial charge carrier position} \\ \Phi_f &: \text{final charge carrier position} \end{aligned} \quad [2.24]$$

Chapter 3

LHC, ATLAS and its Sub-detectors

The frontier accelerator of particle collider physics is the LHC at CERN. It hopes to shed light on new physics around the TeV scale. Hopefully it will answer some of the open questions on the nature of particles and forces. The ATLAS detector is one of two multi-purpose experiments at the LHC. It is pioneering in size, new detector and trigger techniques, as well as high occupancy and radiation tolerances. Its tracking and vertex detector, the Pixel Detector, provides three high precision tracking space points closest to the particle interaction point. It uses silicon hybrid pixel modules which allow spatial and vertex resolutions of $O(10 \mu\text{m})$ with a radiation length of $X_0 < 10\%$. This chapter highlights basic design concepts of the LHC and the ATLAS detector as well as descriptions of the different ATLAS sub-detectors are presented.

3.1 Large Hadron Collider at CERN

The world's largest circular accelerator, the LHC [LHC95],[LHC04], plans to start operation in November 2007. It is located at the European laboratory for particle physics (CERN) astride the Franco-Swiss border near Geneva. The LHC is between 50 and 175 m underground and has a circumference of 26.7 km. CERN is an international particle physics laboratory with over 6500 researchers from 500 participating institutes in 85 countries. Such a colossal experimental setup can only be realized within the context of such a large and international collaboration, since it requires an immense amount of knowledge, manpower, time and financing.

The LHC is a superconducting proton-proton storage ring and will collide proton beams with a design energy of up to 7 TeV each and a bunch crossing frequency of 40 MHz. Its center of mass energy of $\sqrt{s} = 14 \text{ TeV}$ will be seven times higher than todays highest reached center of mass energy by the Tevatron¹¹ accelerator at Fermilab¹². Because the 'de Broglie' wavelength of particles decreases with E^{-1} and therefore the cross section of the particle decreases like E^{-2} , the luminosity of a collider should increase proportional to E^2 to maintain an equally effective physics

¹¹ derives from cyclotron and Bevatron » <http://www-bdnew.fnal.gov/tevatron/>

¹² **Fermi** National Accelerator laboratory » <http://www.fnal.gov>

program. The Tevatron is limited in its luminosity by the anti-proton production rate. Therefore the proton-proton collisions have been chosen on cost of more complex design, e.g. two magnetic fields in separate beam pipes. This way the LHC will reach an instantaneous luminosity of $\mathcal{L} = 1.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, two orders of magnitude above those of present accelerators. This luminosity is achievable by filling each of the rings with 2808 bunches of 1.15×10^{11} particles each. This results in a beam current of $I_b = 0.582 \text{ A}$ and a total stored energy in the beams of 724 MJ. This energy is sufficient to heat about 1.5 tonnes of copper from room temperature to its melting point. A conceptual overview of the LHC collider is shown in Figure 3-1.

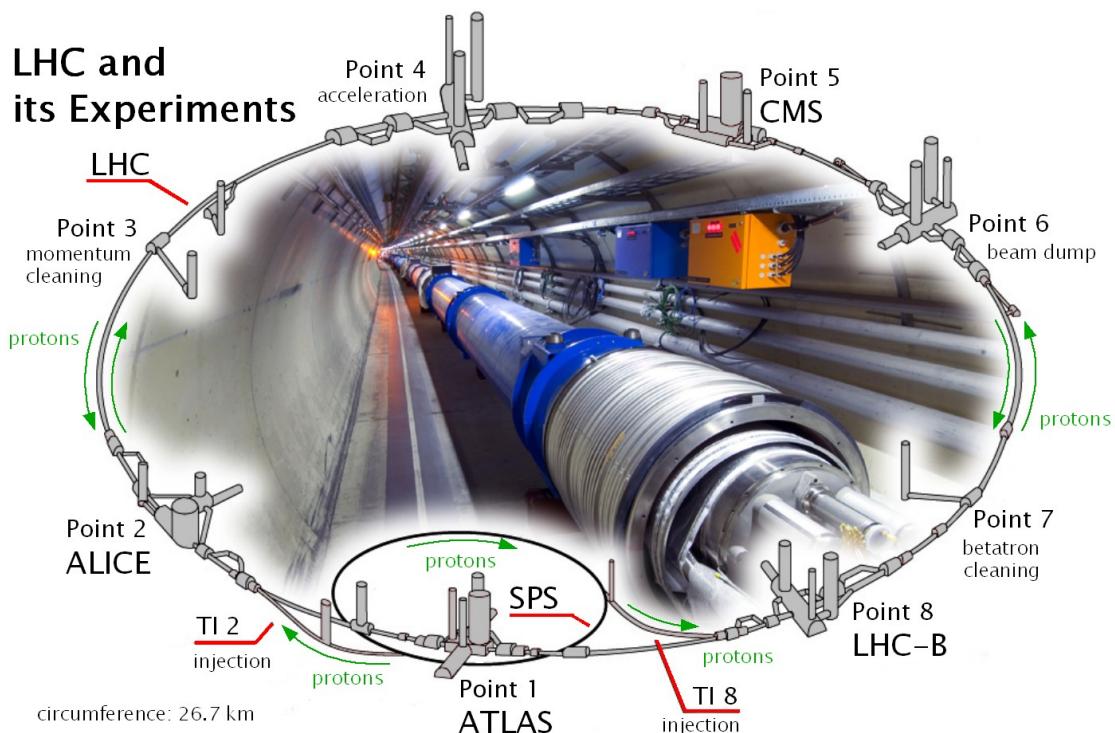


Figure 3-1 Overview of the LHC ring and its experiments

The 1232 main superconducting dipole magnets, illustrated in Figure 3-2, are cooled by superfluid He to 1.9 K. They provide magnetic fields of 8.4 T in each of the two beampipes to bend the two counter-circulating beams to their orbit. The beams are injected through the transfer tunnels TI 2 and 8 from the SPS¹³ ring, where they have been pre-accelerated to 450 GeV [COL97]. The beams are accelerated by superconducting RF cavities (Appendix A Figure A-1) at Point 4 [BOU99] up to 7 TeV in a half hour ramp up phase. To avoid magnet quench, induced by off-beam particles depositing their energy in magnets, collimator systems [ROB06] at Points 3 and 7 catch these off-beam particles before they reach the beam pipe wall and the superconducting NbTi coils behind. The beam dump system [SCH06] at Point 6 removes the two circulating proton beams from the collider in a single turn, 86 μs , and directs them to two external graphite beam dumps, which absorb the beam energy [ZGS95]. This becomes necessary after the beams have circulated for 10 hours and

13 Super Proton Synchrotron

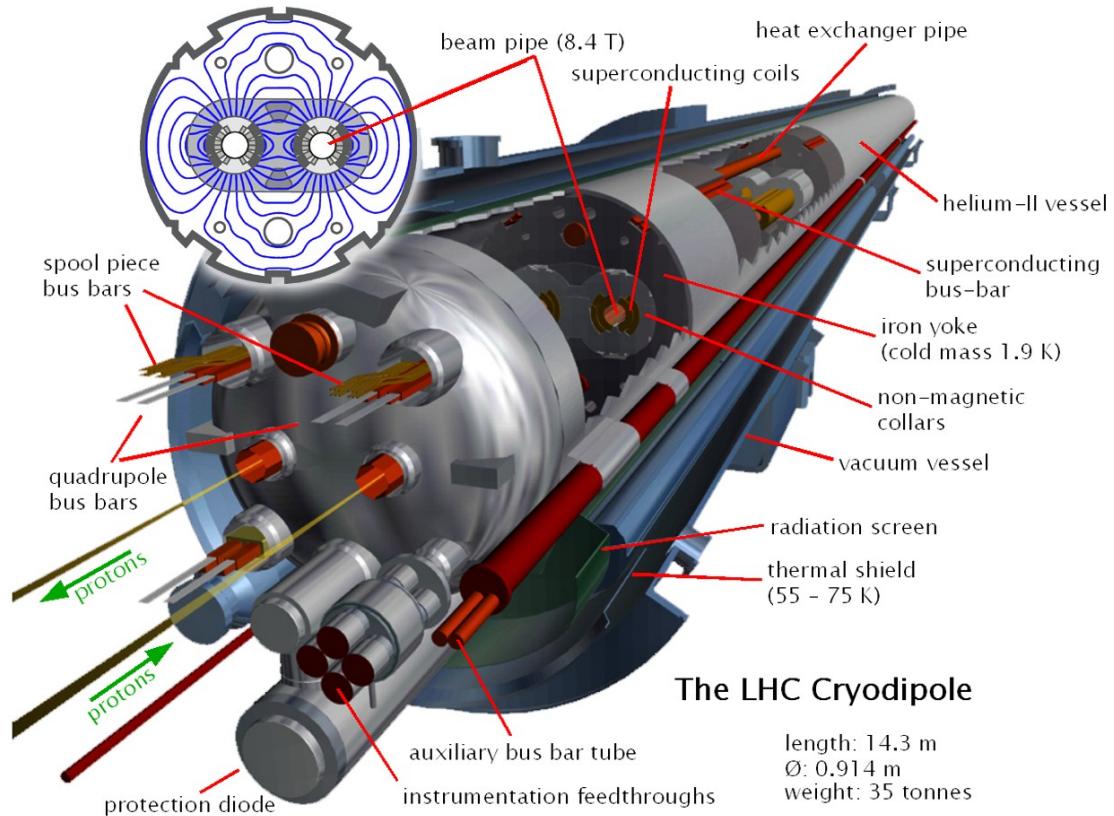


Figure 3-2 Schematic view of the superconducting LHC dipole

the beam intensity has decreased by particle loss and in quench, interlock or malfunction situations. After an 18 minutes magnet ramp down phase and 15 minutes of pre-injection a new LHC cycle can be started [BRÜ03]. Four experimental caverns are located at Points 1, 2, 5 and 8. Two multi-purpose detectors, the ATLAS experiment, detailed described in section 3.2, and the CMS¹⁴ experiment [CMS06] will mainly investigate the p-p collisions to search for answers to the mentioned particle physics questions. The LHCb experiment [LHC03] will concentrate on B-physics and ALICE¹⁵ [ALI95] will analyze collisions of heavy ions [ANG05], e.g. Pb-Pb, which can be accelerated to 5.5 TeV/nucleon in the LHC, too. The luminosity in Pb-Pb operation mode is limited by the quench limit of the magnets (5 mW/cm^3) to $\mathcal{L} = 1.0 \times 10^{27} \text{ cm}^{-2}\text{s}^{-1}$

3.2 The ATLAS Experiment and its Sub-detectors

The ATLAS experiment is placed in a cavern in the LHC ring about 80 m underground. It has an outer radius of 11 m, a distance of 46 m between the third layers of the forward muon chambers, mounted on the cavern wall, and an overall weight of about 7000 tonnes.

¹⁴ Compact Muon Solenoid

¹⁵ A Large Ion Collider Experiment

The overall detector layout is shown in Figure 3-3. It uses a cylindrically symmetric layered detector concept with highly specialized sub-detectors. The beam direction defines the positive z-axis, the positive x-axis is pointing from the interaction point to the center of the LHC and the positive y-axis is pointing upwards. The azimuthal angle ϕ is measured around the beam axis and the polar angle θ is the angle with respect to the beam axis.

ATLAS Layout Overview

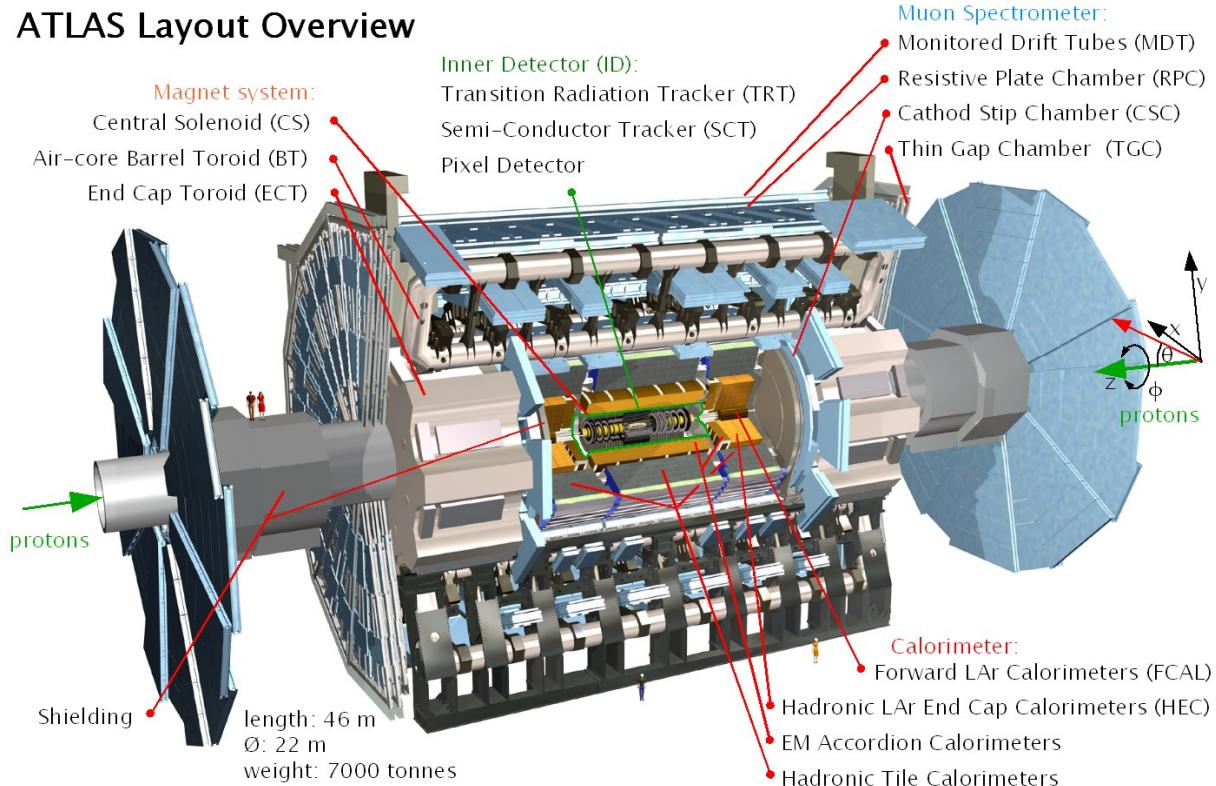


Figure 3-3 Overall detector layout of the ATLAS experiment

3.2.1 Concept and Magnet System

ATLAS [ATL99a] has a large acceptance in η^{16} . The muon spectrometer with its air-core toroid magnets (these have the advantage of reducing multiple scattering compared to a massive iron yoke) and a bunch crossing identification with a time resolution better than the LHC bunch spacing of 25 ns, provides high-precision muon momentum measurements (at the highest luminosity with the external muon spectrometer alone). ATLAS has very good electromagnetic calorimetry for electron and photon identification and energy measurement. Together with the full-coverage hadronic calorimeter it allows accurate measurements of jet energies and the missing transverse energy. Efficient tracking is necessary for high transverse lepton momentum measurement at high luminosities and at lower luminosities for electron, photon, τ -lepton and heavy flavor identification and full event reconstruction.

16 $\eta = \ln \tan \theta/2$ with **pseudorapidity** η and polar angle θ with respect to the beam axis

Triggering and measurements of particles with low transverse momentum thresholds (e.g. ~ 6 GeV muons for b-physics) are possible.

The magnetic field for the muon spectrometer is created by a system of superconducting air-core toroid magnets [ATL97a],[TEN05]. These magnets, the BT¹⁷ [ATL97c] with two ECTs¹⁸ [ATL97b] at its ends have a peak magnetic field at their superconductors of 3.9 and 4.1 T respectively. Together they generate the average tangential magnetic field of about 0.4 T for the muon detectors. Each of the three toroids consists of eight coils placed radially around the beam axis. To optimize the bending power in the overlap region the ECT coil system is rotated by 22.5° with respect to the BT coil system. Coils are indirectly cooled by a forced flow of helium at 4.5 K with the barrel coils housed in individual cryostats, whereas the ECT toroids are housed in two large cryostats. The CS¹⁹ [ATL97d] lines up with both ECTs and provides a central solenoid magnetic field for the ID²⁰ of 2.0 T with a peak field of 2.6 T at the coils. It shares a vacuum vessel with the EM calorimeter in order to minimize material usage and achieve the desired calorimeter performance. A quench protection system safely dissipates the stored energies without overheating the coil windings.

3.2.2 Muon Spectrometer

Within the toroidal magnetic field the bending of muon tracks and therefore their momentum is measured by the high particle flux optimized muon spectrometer [ATL97e],[PAL04]. Four different detector technologies are used. Three layers of high-precision tracking chambers are mounted in the barrel and end-cap region. Regions close to the interaction point or at high pseudorapidity layers consist of two multi-layers of CSCs²¹, whereas in outer regions three to four multi-layers of MDTs²² are used per layer.

The CSC system is designed to measure high momentum muons in the high radiation forward regions. CSC multi-wire proportional chambers with cathode strips (5.08 mm pitch) readout measure the induced charge formed by the avalanche on the anode wire. Charge interpolation allows a position resolution of 60 μm to be obtained. Advantages are small electron drift times (30 ns), low neutron sensitivity, good time (7 ns) and two-track resolution. High granularity make the CSCs suitable for high event rates. The front-end electronic consists of a charge-sensitive preamplifier driven pulse-shaping amplifier. During the Level-1 trigger (see section 3.2.5) latency the cathode peak pulse height is stored in an analogue buffer and afterwards multiplexed into a 10-bit ADC²³.

The 90 to 620 cm long MDTs are made of 30 mm diameter aluminum tubes of 400 μm wall thickness with a 50 μm diameter central gold-plated tungsten–rhenium anode wire and a 93%Ar-7%CO₂ gas filling. The single-wire resolution of ~ 100 μm can be

¹⁷ Barrel Toroid

¹⁸ End-Cap Toroid

¹⁹ Central Solenoid

²⁰ Inner Detector

²¹ Cathode Strip Chamber

²² Monitored Drift-Tube

²³ Analog Digital Converter

improved to 50 μm by combining single chambers to multi-layers. „Monitored“ refers to monitoring of position and deformations by an in-plane optical system. MDTs are read out at one end by a low-impedance current sensitive preamplifier followed by a differential amplifier, a shaping amplifier and a discriminator. A simple ADC is connected to the shaping amplifier to correct the drift-time measurement for time-slewing using the charge integrated signal. Multi-layer resolutions of 40-60 μm have been demonstrated in testbeam [PAL04]. This allows momentum resolutions below 10% at 1 TeV.

Fast trigger signals are provided by RPCs²⁴ in the barrel and TGCs²⁵ in the end-cap regions to obtain:

- bunch crossing identification with a time resolution better than 25 ns
- triggering with well-defined transverse momentum cut-offs in moderate magnetic fields with a required granularity of about 1 cm
- measurement of the second coordinate with a resolution of 5-10 mm in a direction orthogonal to that measured by the precision chambers

RPCs are narrow gas gap chambers, formed by two high-resistive bakelite plates and separated by insulating spacers, filled with tetrafluoroethane ($\text{C}_2\text{H}_2\text{F}_6$) with an admixture of SF_6 . They are made of two rectangular layers with η -strips parallel and ϕ -strips orthogonal to the MDT wires. A uniform electric field of 4.5 kV/mm multiplies the primary ionization electrons into avalanches with typically 0.5 pC read out with metal strips on both sides of the detector via capacitive coupling. The front-end electronics contain a three-stage voltage amplifier followed by a variable threshold comparator mounted at the edges of the readout panels. A space-time resolution of about 1 cm \times 1 ns can be achieved. In testbeam operation trigger efficiencies about 95% have been reached with voltages above 9.4 kV [ETZ04] and trigger resolution better than 3 ns have been demonstrated.

TGCs are multi-wire proportional chambers with a larger anode wire pitch (1.8 mm) than the cathode-anode distance. The small wire distance leads to short drift times and thus a good time resolution. Signals from these anode wires, arranged parallel to the MDT wires, are generating the trigger together with the readout strips, orthogonal to the MDT wires used to measure the second coordinate. The chambers are operated at 3.1 kV with a highly flammable CO_2 and n-pentane ($n\text{-C}_5\text{H}_{12}$) mixture, permitting operation in saturated mode with many advantages:

- small mechanical deformation sensitivity
- small pulse height dependence on the incident angle
- Gaussian pulse height distribution with small Landau tails and without streamer formation

Between 4 and 20 anode wires, depending on the desired granularity as function of the pseudorapidity, are combined to a common readout channel. This ganged signal is read out by a low-impedance two-stage amplifier. Trigger efficiencies above 99.5% have been measured during 2004 testbeam. Tests performed at high rate have shown single-plane time resolution of about 4 ns RMS²⁶.

²⁴ Resistive Plate Chamber

²⁵ Thin Gap Chamber

²⁶ Root Mean Square

3.2.3 Calorimeter System

Particle and jet energies are measured in all ATLAS calorimeters using sampling technology with alternating layers of passive absorber material and active detector material. The choice of the absorber material and the active medium are mainly dominated by the desired particle fluxes and the required radiation hardness [ATL96a]. An overview of the calorimeter system is shown in Figure 3-4.

The 12.2 m long hadronic Tile Calorimeter [ATL96b] is divided in a barrel and two extended barrels. There are 68 cm wide gaps between them providing space for EM Calorimeter front-end electronics and ID, CS and EM²⁷ Calorimeter services. The Tile Calorimeter uses 14 mm iron plate absorbers. It incorporates 3 mm scintillating tiles radially placed and staggered in depth as active material. The barrel and extended barrels with an inner (outer) radius of 2.28 m (4.25 m) are azimuthally divided into 64 modules and placed around the EM calorimeter and the CS. Modules are longitudinally segmented in three sampling cells with $\sim 1.4\lambda^{28}$, 3.9λ and 1.8λ at $\eta=0$. The inner two layers have a $\Delta\eta \times \Delta\phi$ segmentation of 0.1×0.1 and the outer of 0.2×0.1 . In the gap the ITC²⁹ is used in order to maximize the active material, while still leaving room for the services. Two sides of the tiles are read out by wavelength shifting fibres guided to two separate PMTs³⁰ with rise and transit times of some few ns and very low dark current. Shapers generate unipolar pulses of 50 ns FWHM³¹ from the current pulses of the roughly 10000 PMTs. Energy resolutions of about $\sigma/E = 52\%/\sqrt{E[GeV]} \oplus 5\%$ have been measured in testbeam runs [GIA05].

The EM calorimeter [ATL96c] is similarly segmented into a barrel and two endcaps. It is a LAr³² detector with accordion-shaped Kapton® electrodes and lead-stainless-steel absorber plates. The LAr gap has a constant thickness of 2.1 mm in the barrel and varying thickness in the end-caps due to the increase of accordion wave amplitude with radius. The overall thickness of the EM calorimeter is $> 24 X_0^{33}$ in the barrel and $> 26 X_0$ in the end-caps. The total material seen by an incident particle before the calorimeter is about $2.3 X_0$ at $\eta=0$, increasing with pseudorapidity in the barrel and reaching its localized maximum of about $7 X_0$ at the transition between barrel and end-cap. The $\Delta\eta \times \Delta\phi$ readout cell dimensions are 0.025×0.025 . An active LAr layer presampler of 1.1 cm (0.5 cm) thickness in the barrel (end-cap) is used to correct for energy lost by electrons and photons upstream of the EM calorimeter. The roughly 190000 channels are read out by preamplifiers located outside the cryostats, but close to the feedthroughs. Every 25 ns sampled bipolar shapers are used to form the preamplifier outputs. During the Level-1 trigger latency, signals are stored in analogue SCA³⁴ memories. The corresponding samples (typically five) are extracted from the SCAs, digitized and read out by the data acquisition system for validated Level-1

27 Electro Magnetic

28 interaction length or mean free path λ of a particle before undergoing an interaction (neither elastic nor quasi-elastic)

29 Intermediate Tile Calorimeter

30 PhotoMultiplier Tube

31 Full Width at Half Maximum

32 Liquid Argon

33 $E = E_0 \exp(-x/X_0)$ with radiation length X_0 , original energy E_0 and material thickness x

34 Switching Capacitor Array

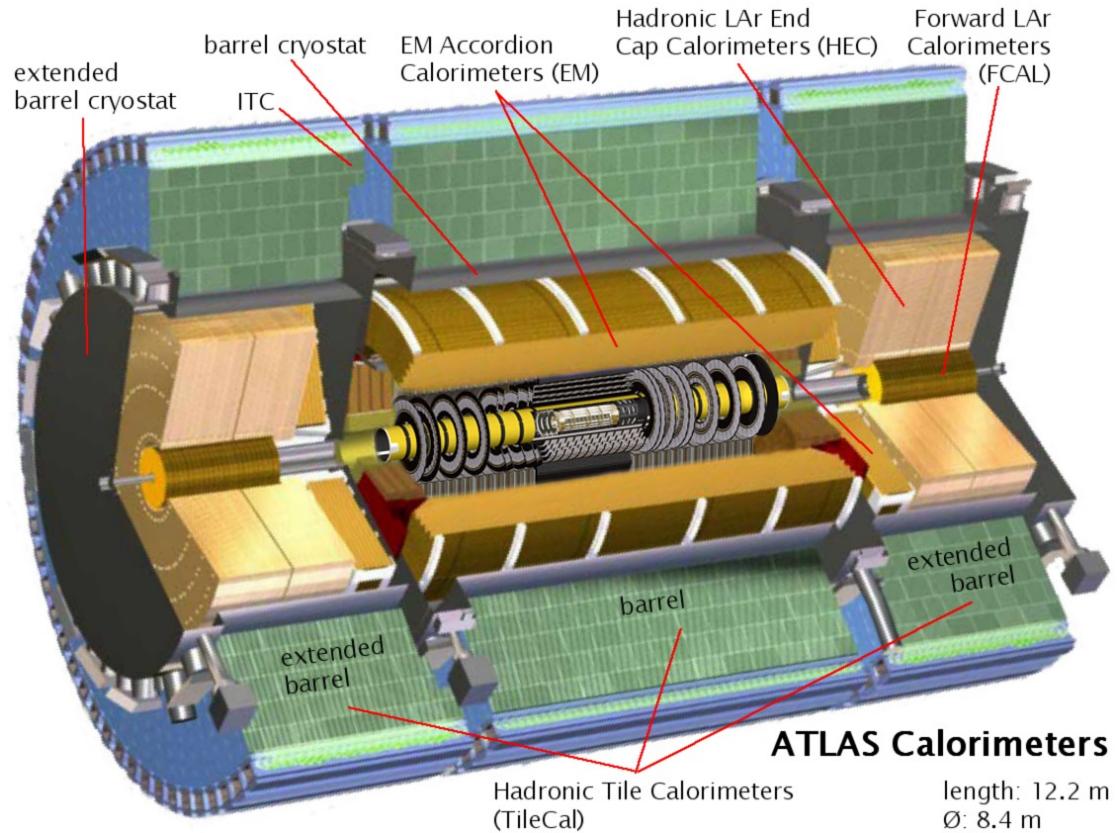


Figure 3-4 Overview of the ATLAS Calorimeters

triggers. In testbeam measurements with electrons energy resolutions of have been reached [BEN04].

Both HECs³⁵ [ATL96c] are built out of two independent wheels with an outer radius of 2.03 m. The more expensive upstream wheel uses 25 mm copper plates whereas the outer wheel uses 50 mm copper plates. In all wheels the 8.5 mm gaps between the copper plates are divided into four drift spaces of 1.8 mm by three parallel electrodes. The central three-layer printed circuit electrode serves as readout and the other two-layer printed circuit electrodes only carry the high voltage of 4 kV. Each wheel is made of 32 identical modules. For fast response and limited capacitance seen by a single preamplifier only two gaps are connected with a miniature coaxial cable running through the sectors to the preamplifiers boards located at the wheel periphery. Signals of typically four preamplifiers are summed on a board, and a buffer stage drives the 5888 output channel signals to the cold-to-warm feedthroughs. $\sigma/E = 21.7\%/\sqrt{E[GeV]} \oplus 0\%$ energy resolution has been measured with electrons in testbeam runs [BEN04].

The FCAL³⁶ [ATL96c] is integrated into the end-cap cryostat. Due to its relatively small distance of 4.7 m to the interaction point, compared to the forward calorimeters in other experiments, it has to cope with high level radiation. On the other hand the advantages of higher calorimeter coverage uniformity and reduced radiation

³⁵ Hadronic End-cap Calorimeter

³⁶ Forward CALorimeter

background levels in the muon spectrometer dominate. Strongly limited longitudinal space for the FCAL caused a high-density design in order to reach 9.5λ . The inner 45 cm depth and 90 cm diameter EM FCAL section is made of copper, the two outer hadronic sections use tungsten. Building a tungsten calorimeter is a rather new and challenging task and the technique used is based on assembling small sintered tungsten alloy pieces. All three sections consist of metal matrices with regularly spaced longitudinal channels filled with concentric rods at a positive high voltage and grounded tubes. LAr in the 250 μm gaps is used as the active medium. Four rods are ganged and their combined signal is carried out by polyimide insulated coaxial cables resulting in total 3584 channels. In testbeam runs a pion energy resolution of $\sigma/E = 90.4\%/\sqrt{E[\text{GeV}]} \oplus 2.7\%$ has been measured [SCH05].

3.2.4 Inner Detector

The Inner Detector (ID) [ATL97f], shown in Figure 3-5, combines high-resolution tracking sub-detectors closest to the interaction point with a continuous tracking sub-detector at the outer radius all in the CS magnetic field with 2 T nominal strength. With its total length of 7 m and an outer radius of 115 cm the ID provides:

- full tracking coverage over $|\eta| \leq 2.5$
- impact parameter measurement
- vertexing for heavy-flavor and τ -tagging
- secondary vertex measurement enhanced by innermost Pixel layer at 5 cm radius
- B sector physics in the initial lower-luminosity LHC run
- good b-tagging performance during all LHC operation phases, e.g. Higgs and supersymmetry searches

The TRT³⁷ [ATL97g] is divided in a barrel and two end-caps. Due to the small straw diameter and the isolation of sense wires within individual gas volumes the used straw detectors can cope with high particle rates and large occupancy. By detecting transition-radiation photons created in a radiator (polypropylene foils or fibres) between the straws and a two threshold system it is in addition possible to identify electrons. A charged particle passing through a medium with discontinuous dielectric constant can be considered to form together with its mirror charge an electric dipole when it is moving towards a boundary where the dielectric constant changes. The emission of transition radiation is therefore caused by this time dependent dipole field. Each Kapton® straw has a diameter of 4 mm and is operated with a non-flammable gas mixture of 70% Xenon, 27% CO₂ and 3% O₂. A 30 μm diameter gold-plated tungsten sense wire with fast response, good mechanical and electrical properties allows straw lengths up to 144 cm in the barrel. This layout is intrinsically radiation hard.

In total 370,000 cylindrical drift tubes typically provide 36 space points per track. In order to reduce the occupancy straws in the barrel part are divided into two at the center. They are read out at each end whereas the readout for the end-cap straws is localized at their outer end. Each channel can carry out a drift-time measurement. In testbeam maximum drift times of 40 ns, resulting in a resolution of $\sim 130\mu\text{m}$ have been achieved with $\sim 87\%$ efficiency and a 250 eV threshold [MIT03]. Basic straw hit

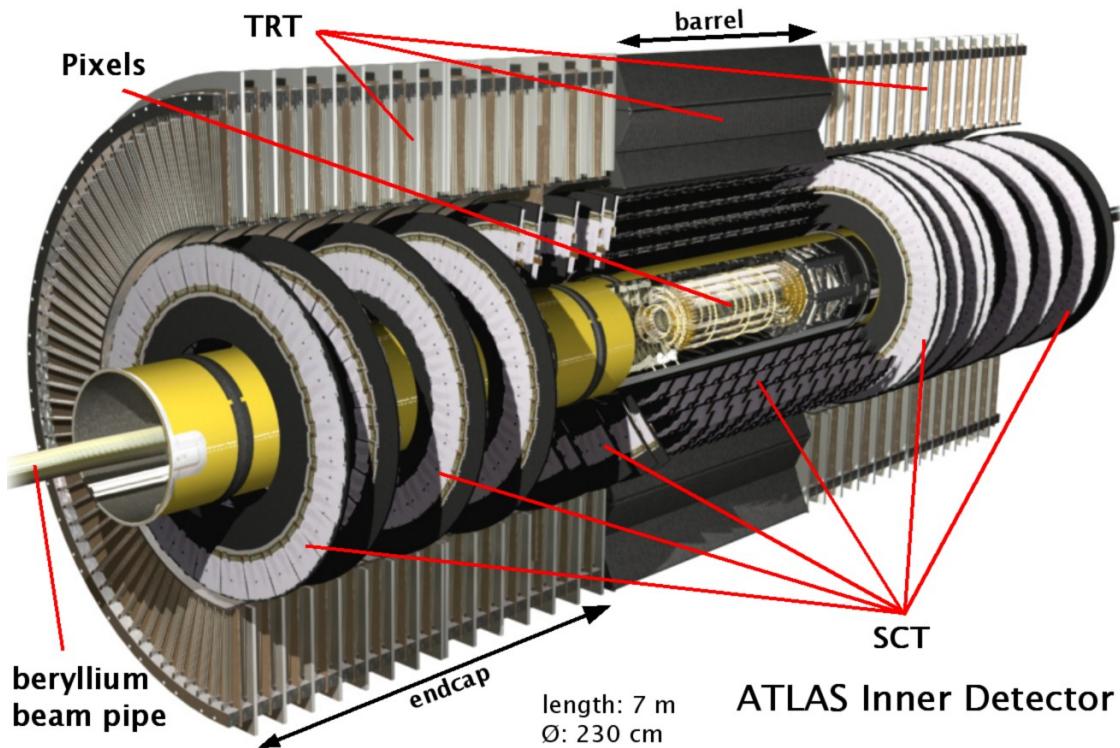


Figure 3-5 The ATLAS Inner Detector with the sub-detectors: TRT, SCT and the Pixel Detector

efficiencies have been measured at 96%. Two different thresholds allow discrimination between tracking hits, passing the lower threshold and transition-radiation hits, passing the higher one. The rate of hits for the lower thresholds varies in the barrel with radius from 6 to 18 MHz, while in the end-caps the rate varies with z from 7 to 19 MHz. The maximum rate at high threshold is 1 MHz. Good performance at these high counting rates and occupancies was one of the basic design aims. Shadowing effects mean that only about 70% of the straws provide correct drift-time information but the large number of space points per track ensure a combined measurement accuracy of better than $50\text{ }\mu\text{m}$ including a systematic alignment error of $30\text{ }\mu\text{m}$. For 90% electron efficiency, pion efficiencies of 1.2% have been measured, this means a rejection factor of 75 against 20 GeV pions.

The SCT³⁸ [ATL97g],[DON06] provides four high-precision spacepoint measurements per track in the intermediate radial range. It is divided into 4 barrels with 30.0, 37.3, 44.7 and 52.0 cm radii and on both sides nine wheels with up to three rings of modules each. In total 4088 SCT modules with an overall active surface of 61 m^2 are used. The basic tasks of the SCT are:

- contributing to the measurement of momentum, impact parameter and vertex parameter
- providing good pattern recognition by use of high granularity

To fulfill this tasks the SCT uses eight layers of silicon microstrip detectors with 768 readout strips of $80\text{ }\mu\text{m}$ pitch in each silicon detector of $6.36 \times 6.40\text{ mm}^2$ size. Each

barrel module consists of four single-sided p⁺-on-n sensors. Pairs of sensors are wire-bonded together to form 12.8 cm long strips. Two such detector pairs are glued back-to-back with 40 mrad stereo angle to a heat transport plate in between. SCT end-cap modules use tapered strips with the front-end electronics attached either to the inner or outer end. End-cap modules consist of strips of either ~ 6 + 6 cm length at the outer radii or 6-7 cm length at the innermost radius. The front-end electronics is attached to the detectors on a hybrid. The first component of the readout chain is a front-end amplifier followed by a discriminator. During the Level-1 trigger decision hit signals above threshold are stored in a binary pipeline. In total SCT uses 6.2 million channels to reach a spatial resolution of 16 μm in Rφ direction and 580 μm in z direction. So, it is possible to distinguish tracks separated more than ~ 200 μm [ABD06].

The innermost tracking sub-detector, the Pixel Detector [ATL98a], is described in detail in chapter 4.

3.2.5 Trigger and Data-acquisition System

The Trigger and DAQ³⁹ system is divided into three levels of online event selection. Each trigger level refines the decision of the previous level and applies sharper and more complex selection criteria [ATL98b],[ATL98c],[ATL98d],[ATL02]. A basic functional view of the trigger and DAQ system is shown in Figure 3-6. To reduce the event rate from the initial bunch crossing rate of 40 MHz with an interaction rate of ~ 10⁹ Hz at a luminosity of 10³⁴ cm⁻²s⁻¹ to a permanent storage rate of O(200 Hz) a rejection factor of more than 10⁵ against 'minimum-bias' events is required. With an event size of ~ 1.6 MB this still gives a required storage capability of a few hundred MB/s. Nevertheless excellent efficiency has to be retained for the rare new physics processes, e.g. Higgs boson decays.

The hardware based LVL1⁴⁰ trigger [ATL98b] uses muon spectrometer (L1Muon) and granularity-reduced calorimeter (L1Calo) information. Trigger Chambers (RPC in barrel and TGC in end-caps) of the muon spectrometer identify high transverse momentum muons while the granularity-reduced calorimeter data are searched for objects like:

- high transverse momentum electrons and photons
- τ-leptons decaying into hadrons
- jets
- large missing transverse energies

Summing over trigger towers ($\eta \times \varphi$ segments) determines the sum of jet transverse energies, the missing and total transverse energies. Trigger candidates of the L1Muon and L1Calo triggers are forwarded to the CTP⁴¹, which uses logical combinations of objects in coincidence or veto to create up to 256 triggers according to a trigger menu. Deadtime and prescale factors are applied depending on the trigger type. The CTP is flexibly implemented and can be reprogrammed during operation. LVL1 triggers are

39 Data-AcQuisition

40 LeVeL-1

41 Central Trigger Processor

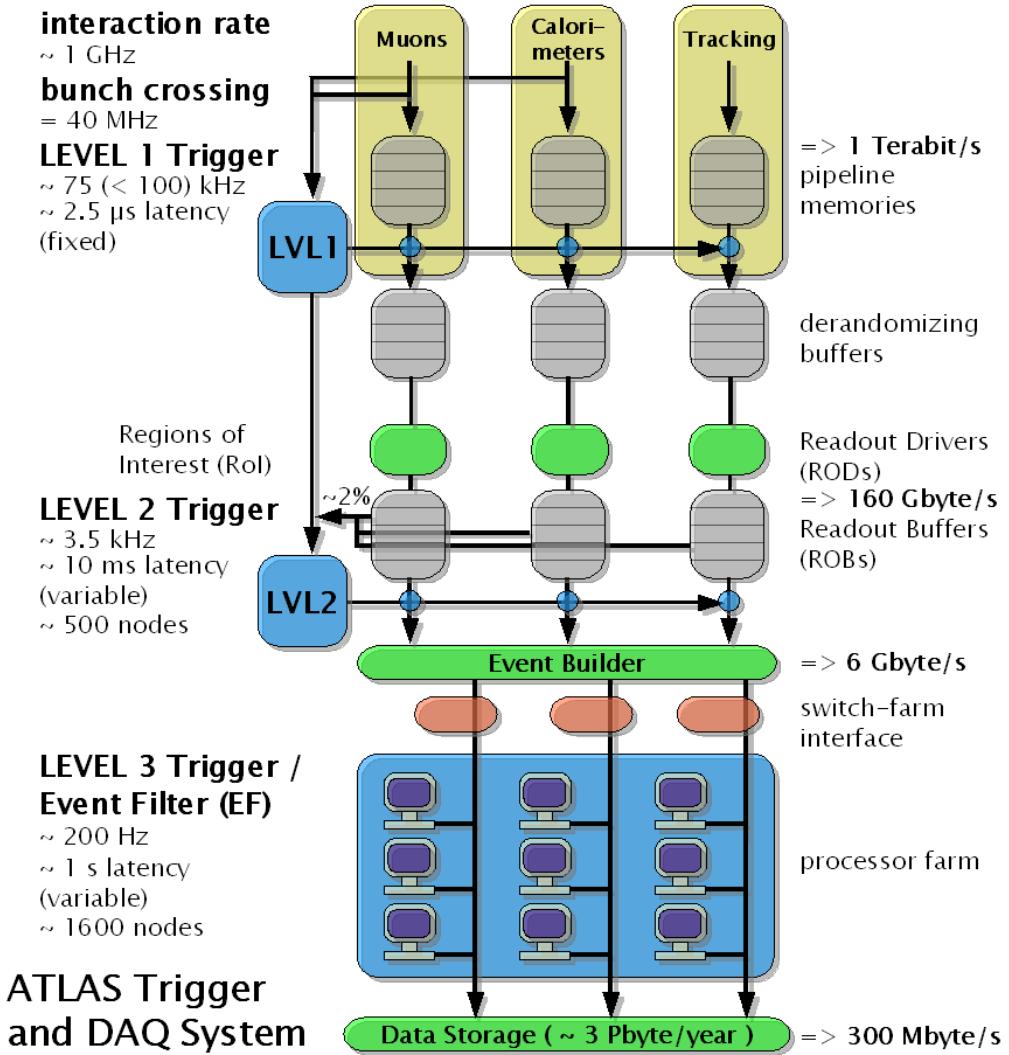


Figure 3-6 Functional view of the ATLAS trigger and DAQ system

distributed to the sub-detectors via LTP⁴²s. The ATLAS front-end electronics of the different sub-detectors can accept LVL1 trigger rates up to 75 kHz but up to about 100 kHz are possible with somewhat increased deadtime. The basic task is to uniquely identify the bunch crossing of interest. This is a non-trivial consideration because the physical size of the muon spectrometer implies TOF⁴³s comparable to the bunch crossing interval and the pulse shape of the calorimeter signals extends over many bunch crossings. Another important task is to keep the LVL1 latency (time to collect information from the sub-detectors, form and distribute the decision) as short as possible. During this latency information of all about $8 \cdot 10^7$ detector channels have to be conserved in pipeline memories localized on or close to the corresponding sub-detector in high-radiation regions. Thus these memories have to be radiation hard. The innermost memories need to have protection techniques against SEUs⁴⁴. The target latency for the LVL1 trigger is 2.0 μ s and may not exceed 2.5 μ s. Extrapolations from

42 Local Trigger Processors

43 Time-Of-Flight

44 Single Event Upset

Testbeam runs indicate a latency of 2.13 μ s [HAL05].

Events selected by LVL1 are read out from the front-end electronics into RODs⁴⁵. De-randomizer buffers average out the high instantaneous data rate of the detector pipeline memories to match the available input bandwidth of the RODs. Events are transferred into ROBs⁴⁶ with a total throughput of \sim 160 GB/s. A large number of front-end channels is multiplexed into each ROB and the data of an event is stored distributed to all ROBs.

The LVL2 trigger uses the RoI⁴⁷ information provided by the LVL1 trigger including information on the position, transverse momentum and energy sums of candidate objects to selectively access data from the ROBs and make the LVL2 decision. Through this method in average only \sim 2% of the total available data are requested by the LVL2 with a data throughput of about 3 GB/s. If necessary the LVL2 trigger has access to all event data with full precision and granularity but usually only these few percent are used by LVL2. It reduces the rate to \sim 3.5 kHz with a data throughput of 6 GB/s and the latency is variable from event to event up to 10 ms. The computing power for the LVL2 decision is provided by \sim 500 dual-CPU nodes [GOR06].

The rejection power of LVL2 comes from:

- for muons: sharpening transversal momentum thresholds by using the precision muon chambers, the ID and calorimeter information around the muon candidate
- for isolated electrons: fully-granulated calorimeter information, matching high transverse momentum track in ID and transition-radiation signature
- for photons: small rejection power, since the ID cannot be used due to high probability of photon conversion in the ID volume
- for hadrons/ts: full-granularity calorimeter information, ID and isolated high transverse momentum track in the hadronic calorimeter
- for jets: small rejection power, because the LVL1 high transverse momentum threshold is reasonably sharp. To reduce the trigger rate LVL2 must either increase the threshold or apply additional selection criteria

An event is held in the ROBs either until it is rejected by the LVL2⁴⁸ trigger or until the event has been successfully transferred to a storage associated with the EF⁴⁹ after being accepted by LVL2 [ATL98c]. After the so-called 'event building' of moving data from the ROBs to the EF the full event is stored in a single memory block accessible by an EF processor. The event building is realized by the SFI⁵⁰ farm, which consists of \sim 50 standard PCs.

The last online selection of the HLT⁵¹ (LVL2 and following trigger components) is performed by the EF. It uses offline algorithms and methods as well as the most up to date magnetic field map, calibration and alignment information. It consists of about 1600 dual-CPU nodes. The first task of the EF is to confirm the LVL2 results and afterwards carrying out its own analysis. The rejection power of the EF is based on:

⁴⁵ Read-Out Driver

⁴⁶ Read-Out Buffer

⁴⁷ Region-of-Interest

⁴⁸ LeVeL-2

⁴⁹ Event Filter

⁵⁰ Sub-Farm Interface

⁵¹ High Level Trigger

- using refined algorithms and tighter transverse momentum thresholds
- availability off all data relevant to the specific event in calculations and selection criteria
- due to processing time limits in the LVL2 trigger, complex and long algorithms can only be performed in the EF, e.g. vertex and track fitting using bremsstrahlung recovery for electrons

After this final selection with a latency up to many seconds the entire event data is written to mass storage by the SFO⁵² node. The output data rate after the EF is about 300 MB/s which corresponds to a rate of ~ 200 Hz. This results in about 3 PB (10^{15} Bytes) of collected data per year. The reconstructed tracks and measured energies of a simulated Higgs boson decay is visible in Figure 3-7.

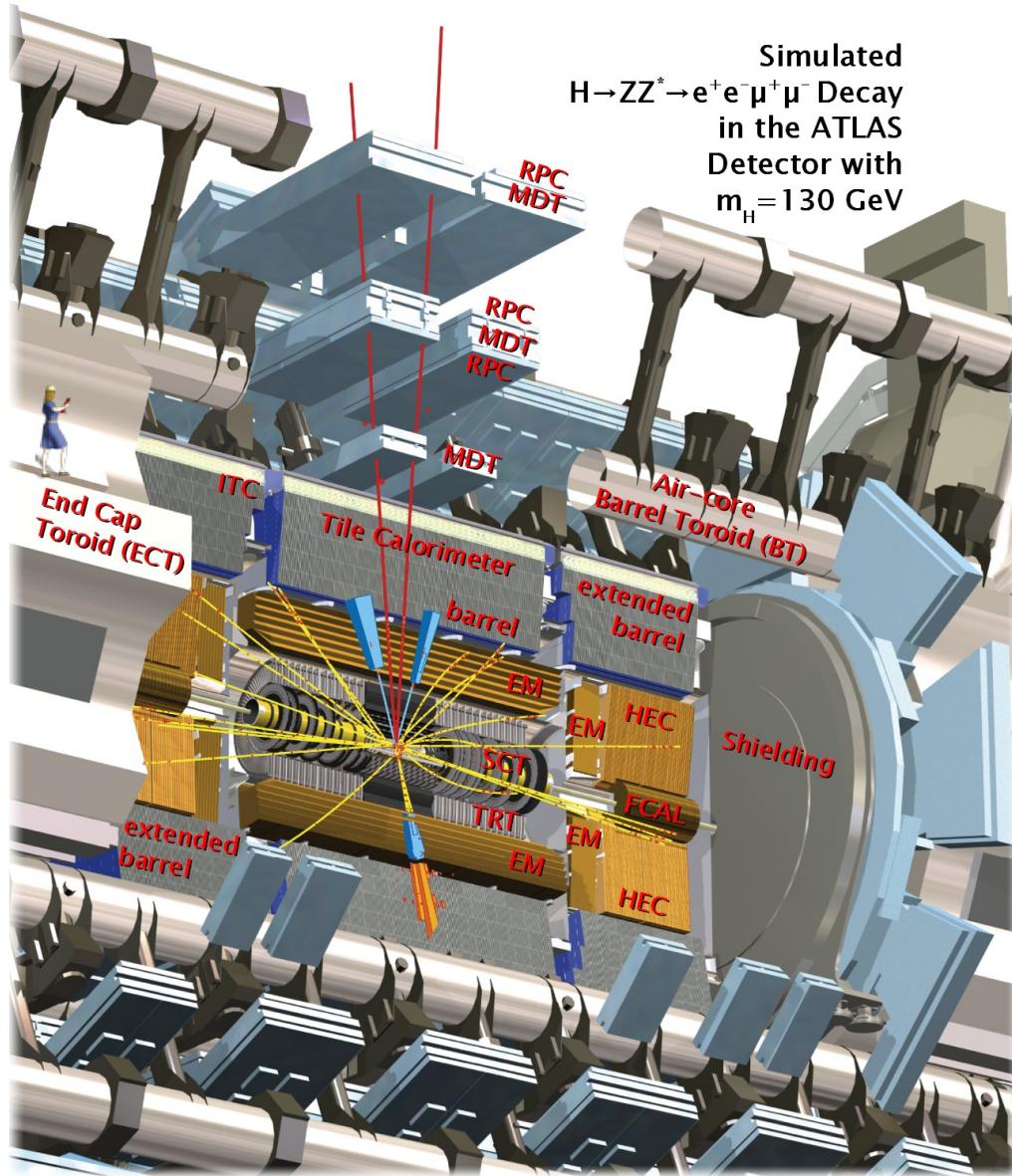


Figure 3-7 Simulated Higgs boson decay in the ATLAS experiment

Chapter 4

ATLAS Pixel Detector

The basic goal of the ATLAS Pixel Detector [ATL98a] is to provide three high resolution ($12\text{ }\mu\text{m}$ in $r\text{-}\phi$ and $100\text{ }\mu\text{m}$ in z direction) space points over a pseudo rapidity range of $|\eta| < 2.5$ for all tracks generated within $|z| < 11.2\text{ cm}$ of the nominal interaction point with an overall efficiency of more than 97%. It needs good charge collection even after a radiation lifetime dose of $1 \cdot 10^{15} n_{\text{MeV eq}}/\text{cm}^2$ to fulfill this task and achieve excellent b-tagging and high 3D-vertex resolution [HÜG01]. The Pixel Detector has been optimized for smallest possible pixel area and pixel size in $r\text{-}\phi$ direction. In order to optimize the pattern recognition and stand-alone trigger performance it has the smallest possible radius for the innermost layer. To minimize multiple scattering, which decreases the other sub-detector's performances, the lowest possible amount of material was used resulting in a radiation length of $X_0 < 10\%$. Mechanical and thermal stability are guaranteed despite this.

4.1 Pixel Package

The complete Pixel Detector is integrated together with the central beampipe section in the so-called Pixel Package. It consists of the beryllium beampipe, the Pixel Detector (see section 4.2) mounted in the central section of the beampipe, the BPSS⁵³ connected to the Pixel Detector in the forward sections and the Service Panels mounted on the BPSS. An exploded view of the ATLAS Pixel Package is shown in Figure 4-1.

The beampipe [OLC02a], [OLC02b] is made of a 0.8 mm thick beryllium tube with an inner diameter of 5.8 cm . It is surrounded by Kapton® heaters to allow a bake out of the beampipe at 250°C . For thermal isolation the heaters are surrounded by a 4 mm thick silica aerogel layer and an outer aluminized Kapton layer. The outer diameter of the isolated beampipe is 6.92 mm and it has a total radiation length of $X_0 = 0.49\%$.

The BPSS [HAR03a],[HAR03b] supports the beampipe and the forward Pixel Services. It consists on each side of three carbon fiber facesheets and honeycomb core cruciform panels. Each panel supports the beampipe through four adjustable

orthogonal wires. Panels are connected through four carbon fiber tubes. BCM⁵⁴ stations are mounted to the middle cruciforms panels. Each station consists of four double sensor $1\text{ cm}^2 \times 520\text{ }\mu\text{m}$ pCVD⁵⁵ diamond pad detectors mounted under an angle of 45° to the beam axis with a radius of $\sim 55\text{ mm}$. High signal speed and radiation hardness of the diamond sensors combined with a fast two-stage RF current amplifier allow separation between beam-beam collisions from beam-gas or beam accident background events by timing coincidences between the two stations [MIK05],[GOR07].

The BPSS is the sole support for the $\sim 3\text{ m}$ long forward pixel service panels [AND04a] which are divided into quadrants. Each SQP⁵⁶ consists of two ISP⁵⁷'s and two OSP⁵⁸'s separately mounted to a backbone structure. They provide 'Type1' services (see section 4.8), which contain electrical wiring for power supply, optical fibers for

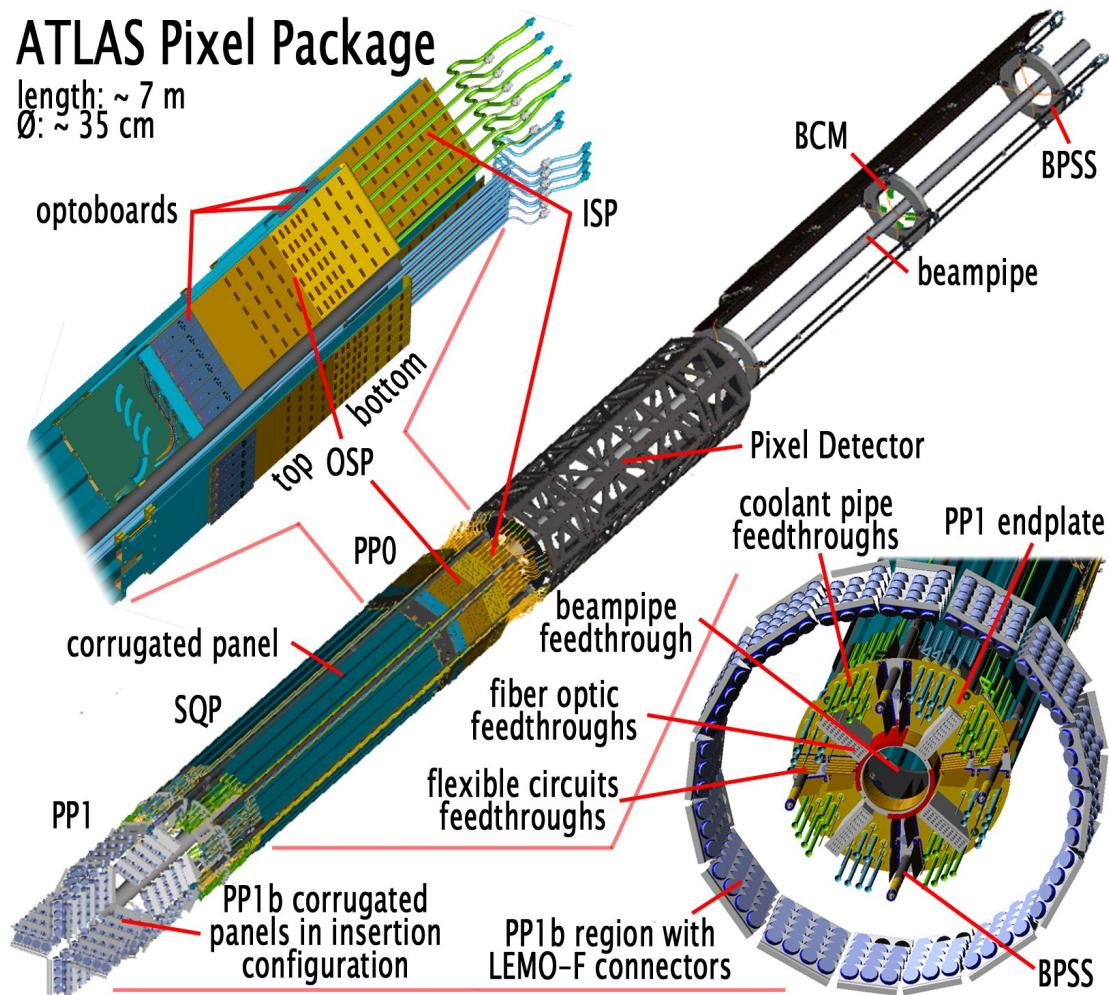


Figure 4-1 Exploded view of the Pixel Package with the PP0 and PP1 region

54 Beam Condition Monitor

55 poly-crystalline Chemical Vapor Deposition

56 Service Quarter Panel

57 Inner Service Panel

58 Outer Service Panel

data transmission, coolant fittings and pipes for the Pixel Detector. Inlet and outlet cooling tubes are connected with fittings to the detector cooling pipes and are joined in the service panels to form a heat exchanger, enhancing the overall efficiency of the cooling circuit. Due to an asymmetry in the coolant pipe routing (see section 4.2) there are 55 inlet and 55 outlet pipes on one detector side (C side) and 45 inlet and 45 outlet pipes on the other side including two spare supply and two return pipes on each side.

Electrical cables (Type0) from the Pixel Detector modules (see section 4.3) plug into PP0⁵⁹s [AND03],[AND07], flexible printed circuits glued to a carbon fiber support. ISPs provide six rows of seven module connections each, whereas OSPs provide six double-rows (top and bottom) with seven and six module connectors, respectively. In each row the data lines of six or seven module Type0 connectors are routed to optoboards, which provide an electrical-optical data conversion (see section 4.4). The optoboards are plugged into 80-pin SMT⁶⁰ connectors on the PP0s. A dedicated opto-cooling circuit and resistor heaters on the optoboards are used to control their temperature. Radiation hard Fujikura⁶¹ SIMM50 (core diameter of 50 µm) optical 8-way bare fiber ribbons with MT-8 connectors on the optoboard side are held on the SQPs together with wire bundles. The bundles carry power, control and environmental monitoring signals in corrugated carbon fiber panels and are routed to the PP1⁶² region. This corrugated panels lend bending stiffness to the SQPs, as well.

All services pass through the PP1 endplate [AND04b], which is supported by the BPSS. Power and monitoring signals of the wire bundles are soldered to flat copper-on-Kapton® circuits routing them through PP1. This transition from wires to flexible circuits and back is necessary to meet the tight space requirements, the need for a gas seal at PP1 and incompatibility of the SQP copper clad aluminum wires (power) and very fine copper wires (sense lines) with standard connector technologies. Copper cables soldered to the flexible circuits outside of the PP1 endplate route the signals to the PP1b regions with 64-pin LEMO-F⁶³ connectors. One HV LEMO connector is needed per four PP0 rows, one module temperatures and optoboard supply voltages (NTC/Opto) connector per two PP0 rows and one LV connector per PP0 row. In total 296 LEMO-F connectors per detector side are arranged in the PP1b region including additional connectors for environmental monitoring signals. In Figure 4-1 the final configuration as well as the insertion configuration of the corrugated PP1b panels is shown. PP1 coolant feedthroughs provide a gas seal for cooling pipes, provide an electrical break in the pipes and contain a bellow to allow axial movement of the cooling pipes when cooled down from room temperature to the operating temperature. Due to the limited available space in the PP1 endplate a space saving layout of a fiber optic feedthrough from Ericsson⁶⁴ is used. Two 8-way ribbons are terminated by a MT16 connector, which are inserted in a housing in the PP1 endplate. One housing for 40 MT16 exists per SQP.

The entire ~ 7 m long package will slide on rails into the PST⁶⁵, which is installed in the Inner Detector. The PST consists of a carbon fiber central barrel and two

59 Patch Panel 0

60 Surface Mount Technology

61 Fujikura Ltd., Tokyo, Japan » <http://www.fujikura.co.jp>

62 Patch Panel 1

63 LEMO S.A., Ecublens, Switzerland » <http://www.lemo.com>

64 Telefonaktiebolaget LM Ericsson, Stockholm, Sweden » <http://www.ericsson.com>

65 Pixel Support Tube

fiberglass/carbon fiber forward shells. All sections contain a 50 μm aluminum EMI⁶⁶ shield layer directly bonded to the shells. The PST serves as a support structure for the Pixel Detector as well as for the BPSS. It allows an individual installation of the Pixel Package and keeps the Pixel volume environmentally (gas sealed and thermal isolated) and electrically (Faraday cage) independent from other sub-detectors. The PST volume is flushed with N₂ ($\sim 0.5 \text{ m}^3/\text{h}$) and is kept on a slightly higher pressure (up to 4 mbar) compared to its air surroundings. Therefore the PP1 endplates provide gas inlet and outlets for dry nitrogen as well. The PST external surface incorporates copper-on-Kapton® heaters designed to keep the outer temperature above dew point in case of Pixel access and failure of the primary Inner Detector dry containment [AND02a],[SMI03].

4.2 Pixel Detector Layout

The sensitive part of the detector is about 1.3 m long, 35 cm in diameter and has a weight of 4.4 kg. It consists of three coaxial cylindrical barrel layers (B-layer, Layer-1 and Layer-2 from inner to outer one) with nominal radii of 50.5, 88.5 and 122.5 mm, respectively [BAR02]. All support structures are made of carbon composite materials. The global carbon-carbon honeycomb core support structure is locating the layers, holding 22, 38 and 52 structural elements, so-called staves. Staves of a layer overlap along a tilted sequence with a tilt angle of 20°. Each layer consists of two half-shells.

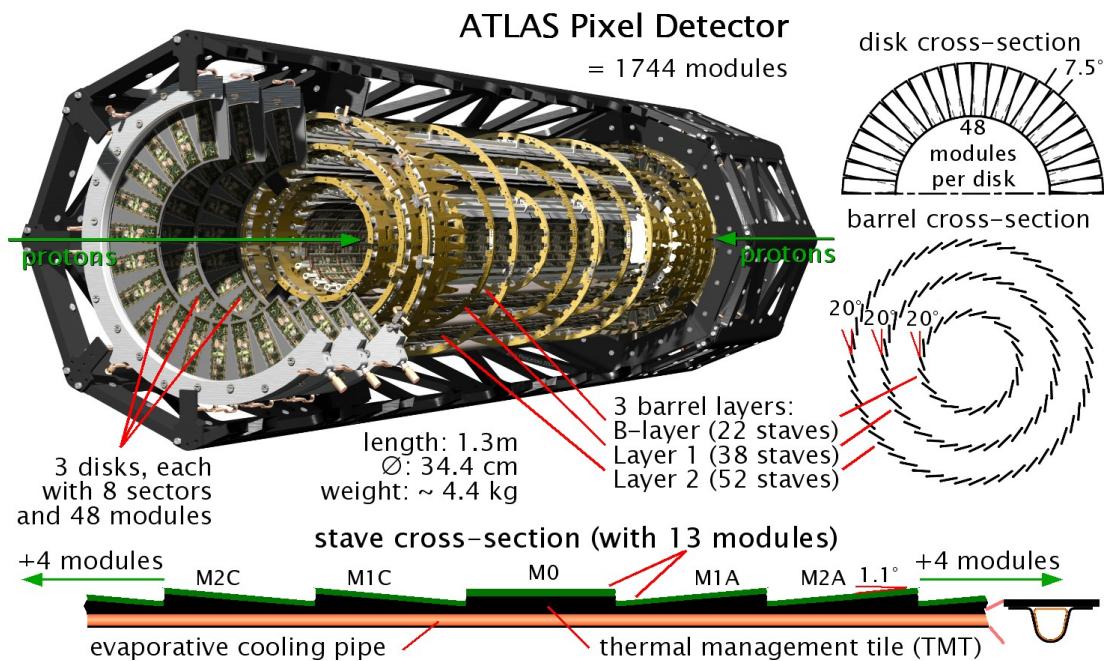


Figure 4-2 Layout of the ATLAS Pixel Detector with three barrel layers and two disk regions, one at each end, containing three disk each

A stave [OLC04a],[GLI06] consists of an aluminum cooling pipe glued with a carbon-epoxy omega profile to a carbon-carbon TMT⁶⁷. The aluminum tubes with a wall thickness of 0.2 mm are shaped to fit in the omega profile and are coated by a thin ($\sim 15 \mu\text{m}$) layer of Parylene for electric isolation of the carbon from the aluminum tube. For an efficient thermal contact a layer of $\sim 200 \mu\text{m}$ thermal grease is introduced between the tube surface and the TMT. 13 modules (see section 4.3) are glued to the TMT and are arranged in a sequence of shingled steps (tilt angle of 1.1°) symmetric with respect to the stave mid module which is horizontal. Two ruby balls are incorporated in the ends of a stave to allow a precise survey of the stave position in the half-shells. The module positions can be derived from the stave survey and the module position survey during stave loading. This design guarantees a precise mechanical fixing and good thermal coupling of modules to the C_3F_8 evaporative cooling in the aluminum pipe. Aluminum fittings are laser-welded to the cooling pipes. The cooling pipes of two neighbored staves, a bi-stave, are connected by a so-called U-link to form a cooling loop [OLC04b]. Inlet and exhaust pipes of a bi-stave cooling loop are guided together alternately to the forward region of the detector (A and C side). Colling loops of the B-layer are all routed to the C-side.

Disk regions at both ends of the barrel contain three disks with z positions of 495, 580 and 650 mm and an active ring-shaped area for radii between 88.77 and 149.6 mm. Overall a disk contains 48 modules with a tilt angle of 7.5° between two modules. Disks are grouped in eight sectors, each with three modules glued to two carbon-carbon faceplates on both sides and an aluminum cooling tube loop mounted between both faceplates. Two neighbored sectors are connected two a bi-sector cooling loop.

The main sources for overall acceptance losses are gaps between the mid-stave module and its neighbors and between the next modules, small v-shaped gaps at the outer radii of the disks and small gaps between the outer barrel Layer-2 modules and the first disk. This layout results in a probability of 2.5% to have less than three hits in the acceptance region ($|\eta| < 2.5$) for high energy muons and increases up to 3.1% for muons with a transverse momentum of 0.4 GeV, which can additionally pass through the r- ϕ gaps between the staves.

4.3 Pixel Module

An exploded view of the basic components of an ATLAS Pixel module [BOY03a],[EIN03a],[DOB04] ($\sim 2 \times 6.3 \text{ cm}^2$ without pigtail) is shown in Figure 4-3. A bare module (see section 4.3.1) consists of a Pixel sensor (see section 4.3.2) bump bonded to 16 FE⁶⁸ chips (see section 4.3.3). It is glued to a so-called flex hybrid, which is loaded with passive SMD⁶⁹ components, a radiation hard $10 \text{ k}\Omega$ NTC⁷⁰ ceramic thermistor, an active MCC⁷¹ (see section 4.3.4) and for barrel modules a pigtail flexible circuit for external signal routing.

⁶⁷ Thermal Management Tile

⁶⁸ Front-End

⁶⁹ Surface Mounted Device

⁷⁰ Negative Temperature Coefficient

⁷¹ Module Control Chip

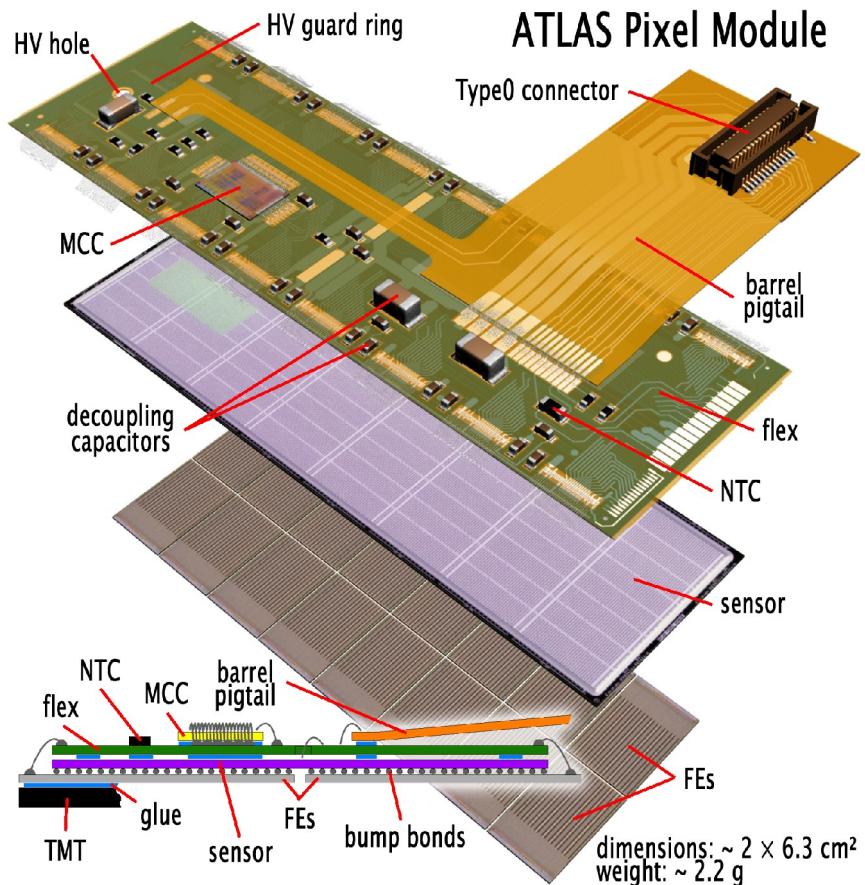


Figure 4-3 Exploded and cross-sectional view of the ATLAS Pixel Module

The flex hybrid provides signal routing between the MCC and the 16 FEs as well as the routing between the MCC and the outer electrical connection of a module. Interconnections for trigger and control signals follow a "H"-bus topology on the flex hybrid whereas the data signals from the FEs to the MCC utilize a star topology. The two supply voltages for a module are filtered by $10 \mu\text{F}$ 10 V ceramic capacitors near the pigtail bond pads. They are bussed starting between the middle FEs in order to balance the voltage drops at the corner FEs. Ceramic LDC⁷²'s ($0.1 \mu\text{F}$ 10 V) are used between each pair of FEs [BOY03b].

The flex hybrid consists of a $50 \mu\text{m}$ thick polyimide substrate with patterned copper traces on both sides and is based on FCB⁷³ technology. Polyimide substrate is used due to its low radiation cross section, low thermal expansion coefficient, excellent dielectric strength of $300 \text{ V}/\mu\text{m}$ and high radiation tolerance up to 100 kGy. The $15 - 20 \mu\text{m}$ thick copper traces are covered with a $2 \mu\text{m}$ electroless nickel plating layer and a $0.2 \mu\text{m}$ electroless gold plating layer. This platings allow soldering and aluminum ultrasonic wire bonding. On both sides cover layers are used to stabilize the traces and make the flex circuit more robust. The bottom layer must withstand sensor bias voltages up to 600 V.

72 Local Decoupling Capacitor

73 Flexible Circuit Board

Modules are cooled from the FE chips side, where they are glued to a stave. Therefore thermal conductive glue is used to attach the MCC to the flex hybrid and the flex hybrid under the MCC to the bare module. For the same reason thermal conductive glue is used underneath the NTC between the flex hybrid and the bare module. To ensure the mechanical stability of the bond pad regions, especially important for the wire bonding process, the flex hybrid is glued with adhesive tape to the bare module under the FE wire bond pads [RAJ07]. Additional stability is given to a module by thermal conductive glue spots underneath the pigtail bond pad region and around the HV hole.

The electrical outer connection of barrel modules is realized by the so-called pigtail, a single layer flex printed circuit made of Kapton®. It is glued to the flex hybrid under its main bond pad region and under its HV⁷⁴ extension close to the HV hole. The module is electrically connected to the PP0 and the following readout chain (see section 4.4) by an aluminum Type0 cable. This cable supplies all power, sensor bias voltage and communication to the module through a SMT Type0 connector, soldered to the pigtail. Disk modules have copper-aluminum Type0 cables with a silicone tube protective sheathing. They are soldered without an intervening connection to the bump pads at the lateral side of the module and close to the HV hole.

The flex hybrid is connected to each FE with 30 25 µm aluminum wire bonds. Double wire bonds are used for the 71 connections to the MCC from three sides. Pigtail data bond pads are connected with the corresponding bond pad at the flex with three wires whereas the four power supply pads are bonded with 14 wires each. These wires have three different lengths to avoid breaking by resonances, which could be caused by Lorentz force in the CS field during power cycling or fixed frequency data transmission. For the same reason each of the HV pads is bonded with three bonds of different length and FE wire bonds are potted at their bond feet. Three sensor bias wire bonds are made through an 1 mm HV hole exposing a pad on the sensor. The HV hole and other HV traces and components on the flex hybrid are isolated from the rest of the flex hybrid by an 100 µm wide “guard ring” trace connected to analogue ground and the detector bias return. The guard ring is located at least 1 mm away from any HV carrying trace or component. A separate HV filter capacitor is used in addition.

4.3.1 Bare Module

In each module more than 46,000 electrical connections have to be realized between the sensor and the 16 FEs. This corresponds to a connection density of about 4,800 cm². To reach this density without degrading the detector performance, surface connections between the sensor and the FE chips are necessary and connections at the edges of the devices are not practicable. Each connection between a sensor pixel and its FE readout channel is made through a bump bond with a minimal pitch between two connections of 50 µm. These bump bonds are also the only mechanical interface between the sensor and the FEs. The importance of this technology, called bump bonding, for consumer electronic products increased during the last years, but with this high density and fine pitch it was a challenging task. To have a technical redundancy during development and to use multiple sources to fill the needed

⁷⁴ High Voltage

quantities, two different manufacturers of bare modules were used. IZM⁷⁵ uses a bump bonding technique with solder bumps whereas AMS⁷⁶ uses indium bumps for the interconnections.

The course of process for both technologies is shown in Figure 4-4 and can be simplified to five process steps:

1. Deposition of a UBM⁷⁷ on the sensor and FE wafer
2. Deposition of bumps either only on the FE wafer or on the FE and sensor wafer
3. Thinning of the FE wafer down to about 180 µm
4. Cutting (dicing) of the sensor and FE wafers and selection of good components by probing
5. Flip chipping of FE chips to the sensor after precision alignment and formation of electrical and mechanical connection at appropriate temperature and pressure

Both manufacturers get the FE and sensor wafers provided with aluminum bump pads. Besides opening for the bump pads, the rest of the wafer is covered with a SiO₂ and Si₃N₄ passivation layer. The five process steps, correspond to the list above, are:

- (1.) To ensure good adhesion, at IZM, the wafers are sputter etched before sputtering of an adhesion layer (200 nm TiW) and the plating base (300 nm Cu) by electroplating. Photoresist is spin coated on the wafer and patterned by exposure to UV light through a high precision contact mask followed by an etching process. A wettable UBM (5 µm Cu) is plated followed by an 100-200 nm gold oxidation protection layer. At AMS photosensitive photoresist is spin coated on the wafers and patterned with the conventional photolithography process described above. A proprietary UBM is deposited.
- (2.) At IZM solder (37 % Pb 63 % Sn) is electroplated. It remains as 30 µm high cylindrical bumps after photoresist removal. The cylindrical bumps turn, caused by surface tension, into spherical bumps during a first reflow process. At AMS the UMB is cleaned with a plasma etching process immediately before the deposition of indium, obtained by electron beam evaporation of indium under vacuum ($\sim 10^{-6}$ Torr). The photoresist is removed by a wet lift-off process and indium cylinders of about 20 µm in diameter and ~ 8 µm in height remain.
- (3.) Since many processing steps of the bump deposition are hard to carry out with thinned and fragile wafers, thinning takes place after bump deposition. The FE wafers are completely coated with a thick photoresist layer to protect the bumps. They are thinned to ~ 180 µm by backside mechanical grinding at GDSI⁷⁸.
- (4.) The fragile wafers are diced immediately after thinning to minimize the risk of breaking by handling. To ensure that FE chips have not been damaged the diced and bumped single chips are held by custom carriers and tested with probe stations.
- (5.) Photoresistive protection cover layers are removed by the described lift-off process. At IZM all 16 FEs are tacked together to the sensor UBM by solder flux using a precision pick and place bonder. The entire bare module is placed in a reflow

⁷⁵ Frauenhofer Institut für Zuverlässigkeit und Mikrointegration, Berlin, Germany » www.izm.fhg.de

⁷⁶ Alenia Marconi Systems, Roma, Italy » www.amsjv.com

⁷⁷ Under Bump Metalization

⁷⁸ Grinding and Dicing Services Inc., Sunnyvale, CA, USA » www.wafergrind.com

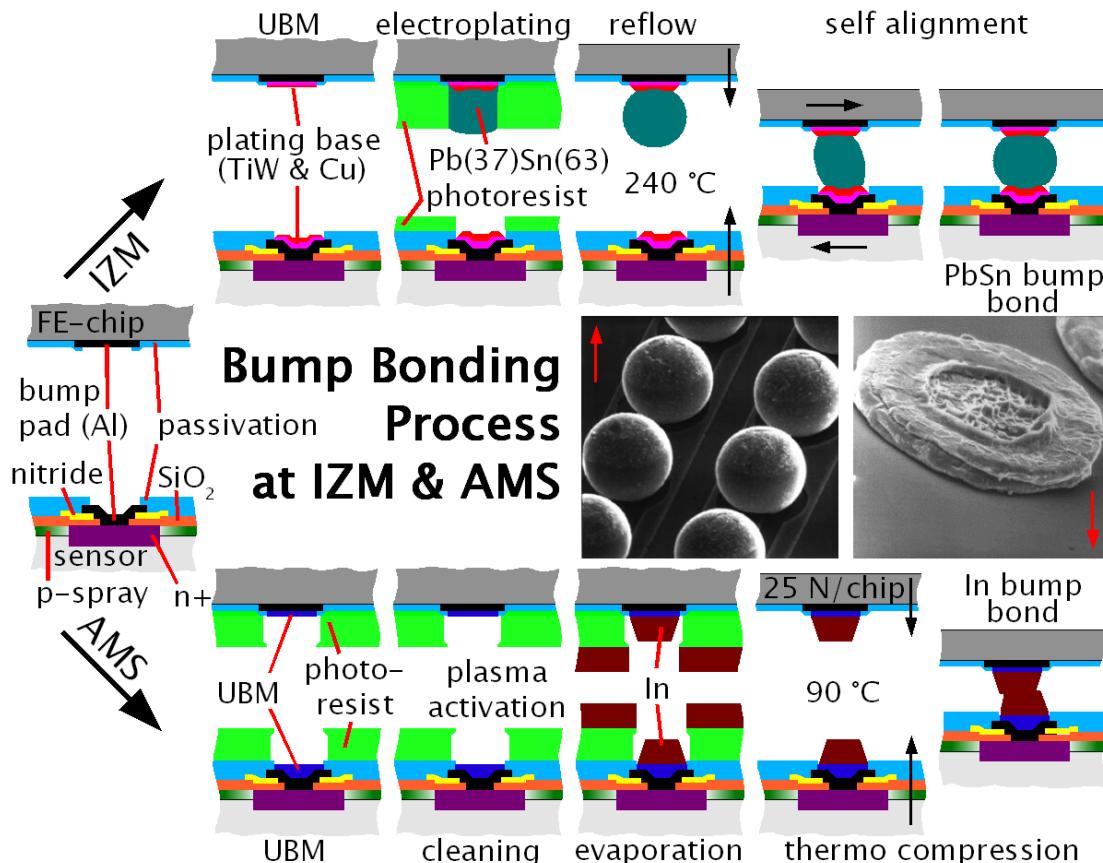


Figure 4-4 The two bump bonding processes used to connect the ATLAS sensors and FE chips

oven. It undergoes a 4 minutes heating cycle with a maximum temperature of 240°C for a few seconds in an activated atmosphere. The bumps and the UBM are solder merged. Caused by surface tension of the bump balls the FEs align themselves. At AMS a single automated machine is used to precisely align, flip and bond the FEs one-by-one onto the sensor. The bonding process itself is a thermo compression at 90°C for a couple of minutes with an applied force of 25 N per FE. Since no self alignment happens for indium bumps, the alignment and planarity of the applied pressure have to be more accurate than for solder bumps [WEB04],[AND02b].

An advantage of indium bumps is the much lower required flip-chip temperature. A significant difference between the two technologies is the electrical resistance of the interconnection. Solder bumps have a constant resistance of about 0.5Ω , whereas indium bumps have resistance of $\sim 10 \Omega$. Increased resistance of up to $500 \text{ k}\Omega$ has been observed on $\sim 10\%$ of the indium bumps. This is caused by In_2O_3 oxidation layers on the bumps which can be broken automatically by applying a 3 V bias voltage to the electronics [GEM01]. Bump resistances have to be kept small to avoid a significant contribution to the FE preamplifier noise.

X-ray inspections with a high resolution ($2\text{-}5 \mu\text{m}$) phosphor screen CCD system and pattern recognition are used to detect merged and missing bumps. The results are crosschecked with further electrical tests (see e.g. section 5.2.2). FEs with bump defects like missing or merged bumps, residue between bumps or damaged FEs can be

replaced by a new one. Reworking of FEs has been successfully demonstrated for both technologies.

4.3.2 Pixel Sensor

The ATLAS Pixel sensor [HÜG01],[KLA05] has an active area of $16.4 \times 60.8 \text{ mm}^2$. It exceeds the size of common consumer microelectronic chips by an order of magnitude. High demands on production quality are necessary to achieve an acceptable production yield. Additional challenges, compared to industrial microchip production, are the required high purity of the silicon, the structuring of the wafer from both sides and the required radiation hardness of the sensor. The required spatial resolution of $12 \mu\text{m}$ in $r\text{-}\phi$ and $100 \mu\text{m}$ in z direction defines with [2.22] the size of a pixel of $50 \times 400 \mu\text{m}^2$. On one hand the sensor needs to be thick enough to obtain a high charge signal to be easily detected by the FE electronics and have a high signal-to-noise ratio. On the other hand it should be as thin as possible to minimize multiple scattering in the Pixel Detector. A compromise between this two demands is the used sensor thickness of $250 \mu\text{m}$. It leads to a mean MIP signal of about 25 k electrons.

Acceptable production yields can only be achieved if the design, handling, testing and each production step is as fault-tolerant as possible. High purity of the silicon is necessary to ensure a full depletion of the sensor and to allow defect engineering. Typically silicon with a resistance between 2 and $5 \text{ k}\Omega\text{cm}$ is used. The purity of the sensor surfaces and the environment are especially important during high temperature processes to avoid the diffusion of impurity atoms into the sensor. In commercial integrated microchips the silicon is just the substrate of the active surface structures. Hence the purity of the silicon and the quality of the non-patterned side are less important. Both sides of the Pixel sensor are patterned. Thus surface damages on both sides can affect its functionality and special care and techniques are required during production, handling and testing.

A n^+np^+ -type sensor design is used. This indicates n^+ patterned implantations in n-substrate on one side and p^+ implantations on the other side. This layout has advantages after irradiation of the detector sensor. The growth of the depletion zone for n^+np^+ -type sensors before and after radiation induced type inversion is shown in Figure 4-5. Bulk type inversion in this case happens when the n-substrate turns into effective p-doped silicon, so called “p”-substrate. Before type inversion the depletion zone grows with increasing bias voltage from the p-side towards the n-side. The usage of the sensor is only sensible when it is fully depleted and the depletion zone reaches the patterned n-side. After type inversion the depletion zone grows with increasing bias voltage from the n-side towards the p-side, thus the sensor is usable if it is not fully depleted. This is important as with increasing irradiation the necessary bias voltage to fully deplete the sensor is increasing as well and possibly excludes a full depletion. In either case a maximal possible depletion is preferable to achieve the maximal possible signal-to-noise ratio.

To avoid low-resistance connections between pixel implantations, induced by positive oxide charges at the Si-SiO₂ interfaces, it is necessary to isolate them. On one hand the isolation has to be good enough to cope with an increased amount of oxide charges induced by irradiation. On the other hand it may not produce too high lateral

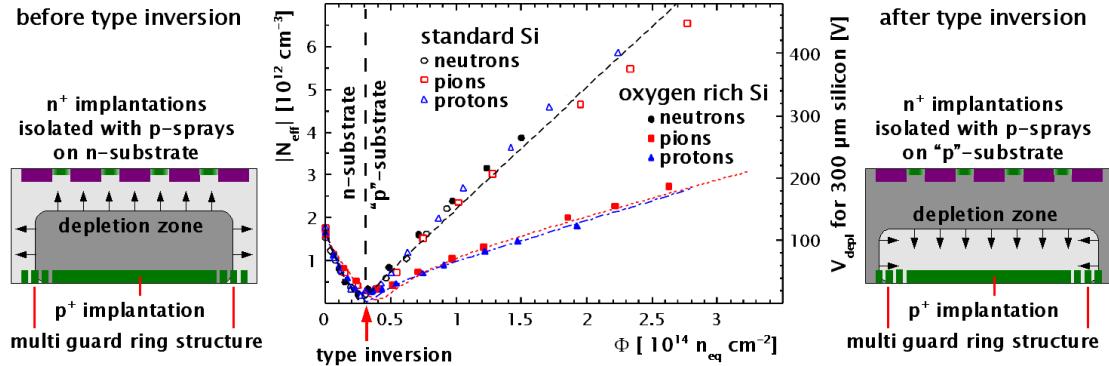


Figure 4-5 Comparison of the effective impurity concentration and depletion voltage between standard and oxygen rich silicon after irradiation with neutrons, pions and protons [FEI00]

maxima in the electrical field (see Appendix A Figure A-2), which would influence the voltage tolerance of the sensor. P-stop implantations, limited p⁺ implantations between the n⁺ pixel implantations, with doping concentrations close to that of the p-side p⁺ implantations ($\sim 10^{14} \text{ cm}^{-2}$) are commonly used for this purpose. They have the disadvantages of an additional necessary lithographic process, risking wrong alignment, and high lateral maxima of the electric field at the bulk-oxide-p⁺ junctions. Thus a p-spray layout is used for the sensors with a mask-less low concentration ($\sim 10^{12} \text{ cm}^{-2}$) boron p⁺ implantation on the n-side. The n⁺ pixel implantations ($> 10^{14} \text{ cm}^{-2}$) locally compensate the p⁺ implantations. They can have a smaller pitch with this layout, hence alignment safety distances are not necessary. The doping concentration of the spray has to be chosen carefully. On one hand the concentration must be high enough to isolate the pixels even after maximal irradiation. On the other hand too high concentration lowers the voltage hardness of the sensor, because the maximal lateral electric field strengths are located at the bulk-p⁺-n⁺ junctions. A major advantage of the p-spray design is that the radiation hardness concerning breakdown grows with irradiation, hence the sensor can be tested and qualified easily before irradiation [KLA04].

A modified p-spray layout, so-called moderated p-spray, has been tested [LUT97] and implemented in the Pixel sensor. This layout is characterized by reduced electric field maxima by using a doping profile for the p-spray implantation with an increased concentration in the center. Therefore the doping gradient and thus the electric field maxima are reduced at the p⁺-n⁺ interfaces. The concentration in the center is comparable to normal p-spray concentrations to ensure the interruption of the conductive electron accumulation channel. Optimal doping profiles have been studied in simulations [ROH99]. The relative doping concentration of the moderated region with respect to the center concentration decides about the character of the isolation, whether it behaves more like a p-stop or more like a p-spray implantation. To obtain such doping profiles a nitride layer is used to moderate the p-spray implantation. The p-spray implantation process is shifted after the deposition and structuring of the nitride. The nitride is a mechanical protection and additionally, since it is a high-resistance conductive layer, increases the speed of potential forming in the oxide. The openings in the nitride are smaller than the width of the inter pixel gap, so only the center receives the full dose and the concentration decreases towards the pixel edges.

The bias voltage is connected to the p⁺ implantation, thus the n-side of the sensor has ground potential. This is important for hybrid pixel detectors, since a potential difference between the sensor and the FEs could lead to a flashover in the 25 µm gap. A flashover could also happen at the edge of the sensor, if the pn junction on the p-side reaches the cut edge of the sensor. Thus a multi guard ring structure, metallized isolated floating p⁺ implantations, is implemented around the main p⁺ implantation close to the edge of the sensor to lower the bias potential step by step to zero. It also prevents the depletion zone from reaching the cut edge of the sensor, where crystal defects would inject charge carriers to the bulk and therefore increase the leakage current. A cross-section of the guard rings and the controlled potential reduction is shown in the lower left corner of Figure 4-6.

Two manufactures, CiS⁷⁹ and ON⁸⁰, produced the ATLAS Pixel sensors. The production can be basically summarized in 10 steps [HÜG01]:

1. thermal oxidation of both wafer sides and bulk oxygenation
2. spin coating of photoresist on the n-side; patterned with n⁺ implantation mask by photolithography process; etching to allow alignment of following masks
3. n⁺ implantation on the n-side with phosphorus
4. spin coating of photoresist on the p-side; patterned with p⁺ implantation mask by photolithography process; etching to allow alignment of following masks
5. p⁺ implantation on the p-side with boron; activation by tempering with inert gas
6. deposition of nitride layer on both wafer sides
7. mask-less low dose implantation on n-side with boron (p-spray); activation by tempering with inert gas
8. etching contact holes into nitride layer on both wafer sides; same for oxide layer
9. deposition and structuring of the aluminum on both wafer sides; alloying of aluminum
10. deposition and structuring of the passivation on both wafer sides

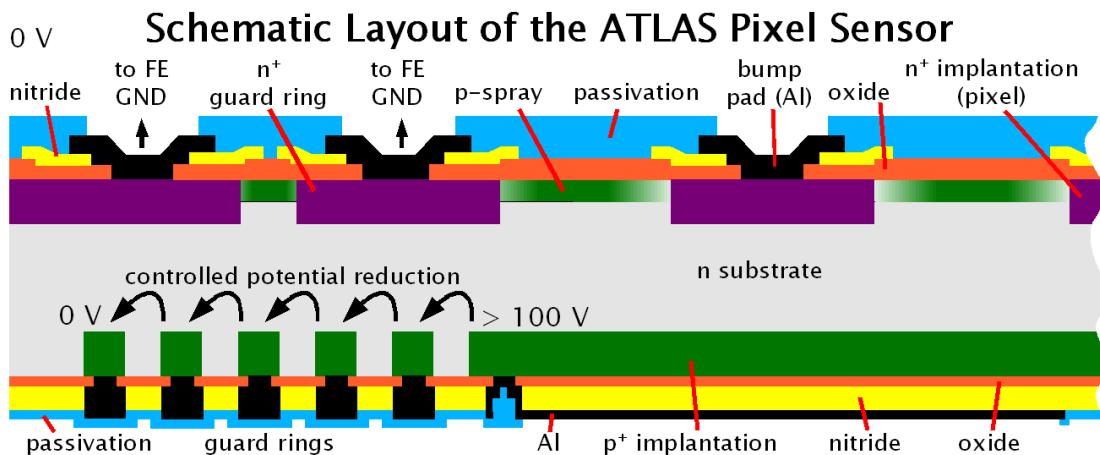


Figure 4-6 Cross-section of the ATLAS Pixel sensor at its cut edge

79 CiS Institut für Mikrosensorik gGmbH, Erfurt, Germany » www.cismst.de

80 ON Semiconductor Czech Republic a.s., Roznov, Czech Republic » www.onsemi.cz

A cross-section of the sensor is illustrated in Figure 4-6.

The production is characterized by the single thermal oxidation step, defining the quality of the Si-SiO₂ interface and therefore the quality of the entire sensor. The oxide quality is high enough to remain on the substrate during the complete production and all implantation processes can be realized through the oxide with increased energy.

Radiation hardness was a basic design criterion of the sensor. In the high fluence environment of the Pixel Detector (up to $10^{15} n_{eq}(1 \text{ MeV}) \text{ cm}^{-2}$ for the B-layer) the usage of standard silicon would lead to depletion voltages of 600 V for the B-layer only after three years of operation. Since 600 V is the design maximum operation voltage of the Pixel Detector, the depletion depth would decrease starting after three years. After about five years of operation the depletion depth of the B-layer would get too low to detect a traversing MIP, due to the fact that the front-end electronics do have a non-zero threshold and noise. Hence the sensors of the B-layer would need to be changed after five years.

Radiation damages in bulk are caused by defects in the silicon lattice. The ROSE / CERN RD 48 collaboration investigated the possibility to change the defect kinetics of silicon by increasing or decreasing the concentration of impurities like oxygen or carbon [LIN01]. The absolute effective impurity concentration and the depletion voltage of 300 μm thick standard silicon and silicon with an oxygen concentration of few 10^{17} cm^{-3} versus the fluence of neutrons and the 1 MeV neutron equivalent fluence of pions and protons are shown in Figure 4-5. The effective impurity concentration of oxygen rich silicon increases much slower after type inversion with respect to standard silicon if the silicon is irradiated with charged hadrons. No change is visible for neutron irradiation or the behavior of leakage current [MOL99].

The depletion voltage of standard and oxygen rich silicon sensors in the B-layer for ten years of ATLAS operation are illustrated in Figure 4-7 (left plot). An annual fluence of $\Phi = 3.5 \times 10^{14} n_{eq}(1 \text{ MeV}) \text{ cm}^{-2}$ within the first 100 days of a year at high luminosity with 85% charged hadrons has been assumed. Three different temperature scenarios have been simulated (lower to upper curves): three days at 20°C + 14 days at 17°C, 30 days at 20°C and 60 days at 20°C. In all cases a temperature of -10°C is

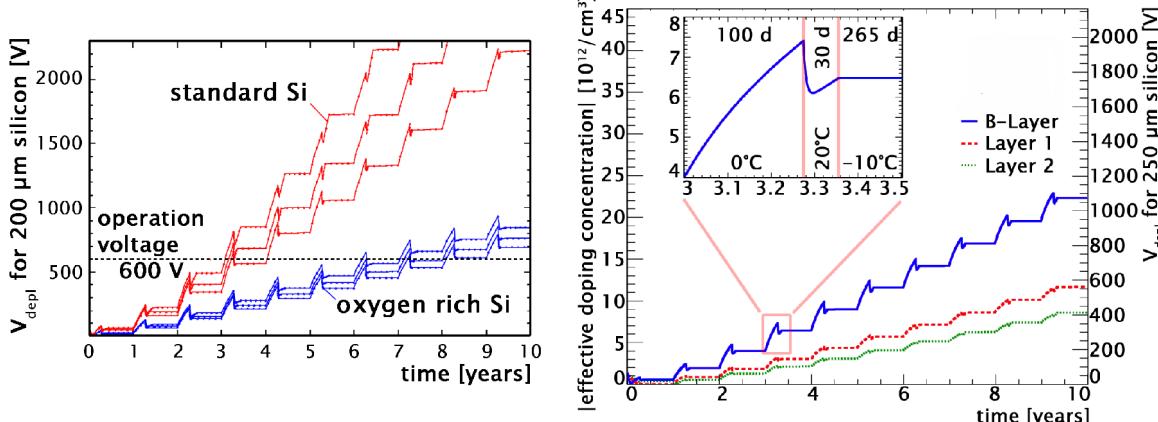


Figure 4-7 Depletion voltage of standard and oxygen rich sensors (200 μm) [LIN01] & effective doping concentration and depletion voltage for Pixel sensors (250 μm) during 10 years of LHC operation [WEB07]

assumed for the rest of the year. The effective doping concentration and depletion voltage for the used 250 μm Pixel sensors for all three layers with 30 days at 20°C per year is shown in the right plot. The usage of oxygen rich silicon allows to operate the B-layer fully depleted for five years and furthermore the sensors tolerate longer maintenance periods before reverse annealing significantly contributes to sensor damages. A replacement of the B-layer is planned after five years of operation.

To achieve such high oxygen concentrations in the sensor substrate oxygen atoms are let to diffuse from the oxide layer to the bulk. Therefore in the first production step after the thermal oxidation the sensor is stored at high temperatures for several hours.

Between neighboring FE chips exists an up to 400 μm gap. In this interchip region so-called long pixels have a length of 600 μm to avoid non sensitive areas in the long pixel direction. In the short pixel direction the eight pixels per column which cannot be connected directly to a FE by a bump bond are ganged by an additional metal layer on the sensor to bump bonded pixels. To minimize the ambiguity of track reconstruction two neighboring of these so-called ganged pixels are connected to the next but one neighboring bump bonded pixels. If two neighboring ganged pixels in the interchip region are hit by a charged particle two non neighboring bump bonded pixels show a hit and this event can be distinguished from a double hit in the bump bonded pixels. For single hit events the ambiguity remains and can only be solved by track reconstruction with additional information from other Pixel Detector or Inner Detector layers. Pixels between two ganged pixels are called inter-ganged pixels. So-called long+ganged pixels are used to cover the interchip region between four FEs. The structure of the interchip region with the six different pixel types is shown in Figure 4-8. Disadvantages of this design are a more difficult track reconstruction, caused by the different pixel types, and the increased capacitance of the non standard pixels, resulting in increased noise of these pixels.

ATLAS Pixel Sensor Interchip Region

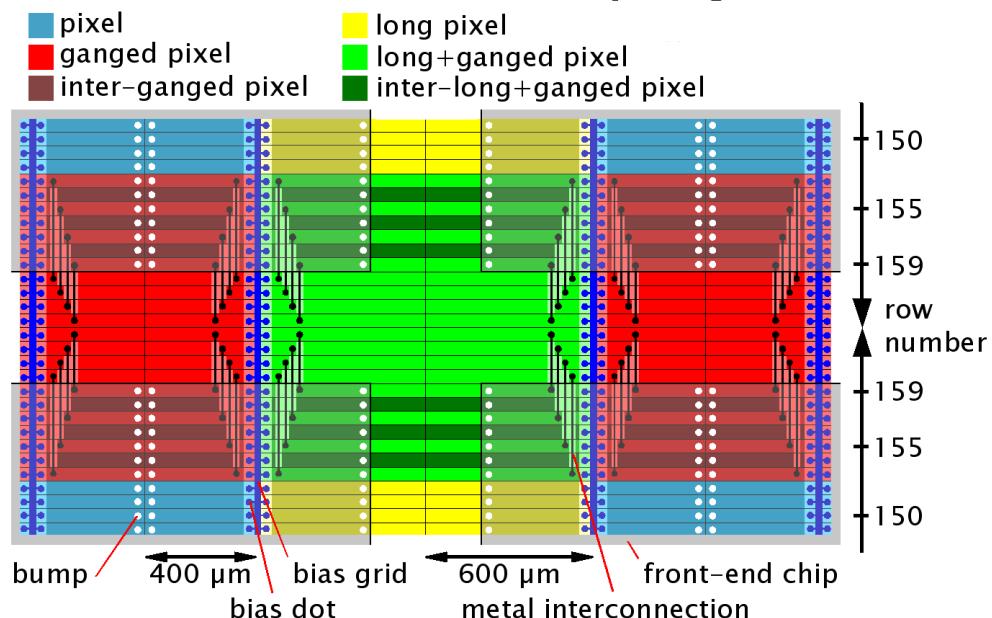


Figure 4-8 Layout of the different pixel types in the interchip region

To allow testing of sensors under operation conditions a punch-through bias grid is implemented in the sensor design. Opposite to the bump bond pad side of each pixel a n⁺ dot implantation, the so-called bias dot, is incorporated. It is surrounded by the pixel n⁺ implantation as shown in Figure 4-9. All bias dots are connected to metal traces on top of the oxide. These traces are connected to a 90 µm n⁺ ring implantation surrounding the entire n-side of the sensor. All pixels can be connected simultaneously to the ground potential, by the punch-through-effect (e.g. [KLA05]), with a single probing needle placed on this ring. The p-side can be connected by another probing needle. The bias grid ensures a homogeneous electric field in the sensor similar to during operation when the pixels are connected to the ground potential through the bump bonds. After bump bonding the sensor to the FEs the bias grid is inactive, but it holds pixels which are not connected by fault with a bump bond to a FE pixel close to the ground potential. Hence the risk of flashovers is minimized. A disadvantage of this design is a reduced average charge collection up to 33% at the bias dot due to direct charge collection onto the bias dot for unirradiated sensors. For end-of-lifetime dose irradiated modules a 20% reduced average charge collection at the bias dot and the bias grid region with maximal reduction of up to 33% in the bias grid pixel corners have been measured. The charge collection at the bump bond pad pixel corners in contrast is only reduced by 14%. Average charge collection maps for both cases are shown in Figure 4-9. Nevertheless the detection efficiency is not significantly affected [DOB04],[LAR06].

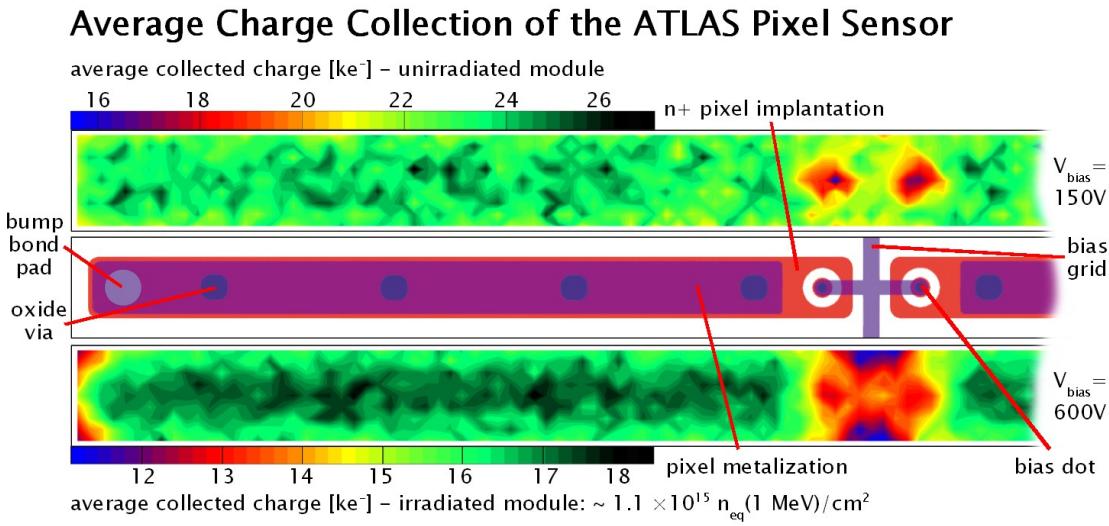


Figure 4-9 Design of the ATLAS Pixel Detector pixel implantation and average charge collection for an unirradiated module at 150 V bias voltage and for an end-of-lifetime dose irradiated module at 600 V bias voltage [DOB04]

4.3.3 Front-end Electronics

In order to measure in each sensor pixel the amount of charge deposited by the passage of a charged particle and to digitize the hit information FE-I3 chips [EIN02],[EIN03a-c],[BLA02],[FIS02] are used. Each chip has 2880 pixel readout cells, covers an active area of the sensor tile of $7.2 \times 10.8 \text{ mm}^2$ and contains about 3.5 M transistors. FE chips are produced in a $0.25 \mu\text{m}$ DSM⁸¹ technology with radiation tolerant layout rules and the 6-metal IBM CMOS6SF process. They need to have the same lifetime ionizing radiation dose tolerance of 50 Mrad as sensors. The radiation hardness of this technology has been verified by the RD49 collaboration [ADA00]. Advantages of the $0.25 \mu\text{m}$ technology are a very high yield, a decreased layout effort and a factor six gain in density compared to other radiation hard technologies (DMILL and Honeywell SOI) used during prototyping.

The radiation tolerant design rules for the $0.25 \mu\text{m}$ DSM technology are [FIS01]:

- usage of annular NMOS, individually surrounded by guard rings in order to control any leakage current around the gate (bird's beak) developing during irradiation in the field oxide
- high quality of the oxide interface to achieve low activation of interface states
- usage of a thin gate oxide of about 5 nm so that holes created by ionizing radiation can tunnel out of the gate oxide, therefore threshold shifts become small
- usage of p⁺ guard rings to eliminate currents between devices

A FE-I3 chip consists of three functional sections. They are shown in Figure 4-10. The biggest part of the chip is used by a matrix of 160×18 readout channels. The middle part, so-called bottom of column region, contains the end of column logic and LVL1 buffers and the bottom part of the chip contains the data serializers and the pad frame.

The FE is powered by the two module supply voltages. The digital supply VDD is referenced to DGND and has a nominal value of 2.0 V with a working range from about 1.5 V to 2.5 V. The analogue supply VDDA is referenced to AGND with a nominal value of 1.6 V. The VDDREF power net is used to provide power only to the preamplifiers, serves as reference for the preamplifier inputs and is the final shield layer for the FE chip. It is connected to VDDA outside the FE. The current consumption is roughly 75 mA on VDDA and 35 mA on VDD. AGND and DGND are connected together outside the FE.

The dimensions of a FE pixel cell correspond to the sensor pixel dimensions with $50 \times 400 \mu\text{m}^2$. FE channels incorporate a high gain, fast preamplifier with a feedback capacitance of nominally 5 fC. A DC-coupled second stage and a fast differential discriminator are following the preamplifier for zero suppression. Eleven 8-bit current mode DAC⁸²'s, in turn supplied by a current reference, are used to control the biasing of critical nodes in the preamplifier and the discriminator, as well as threshold adjustment of the discriminator.

Figure 4-10 shows the layout of a pixel cell and its block diagram and digital readout

⁸¹ Deep-SubMicron

⁸² Digital Analogue Converter

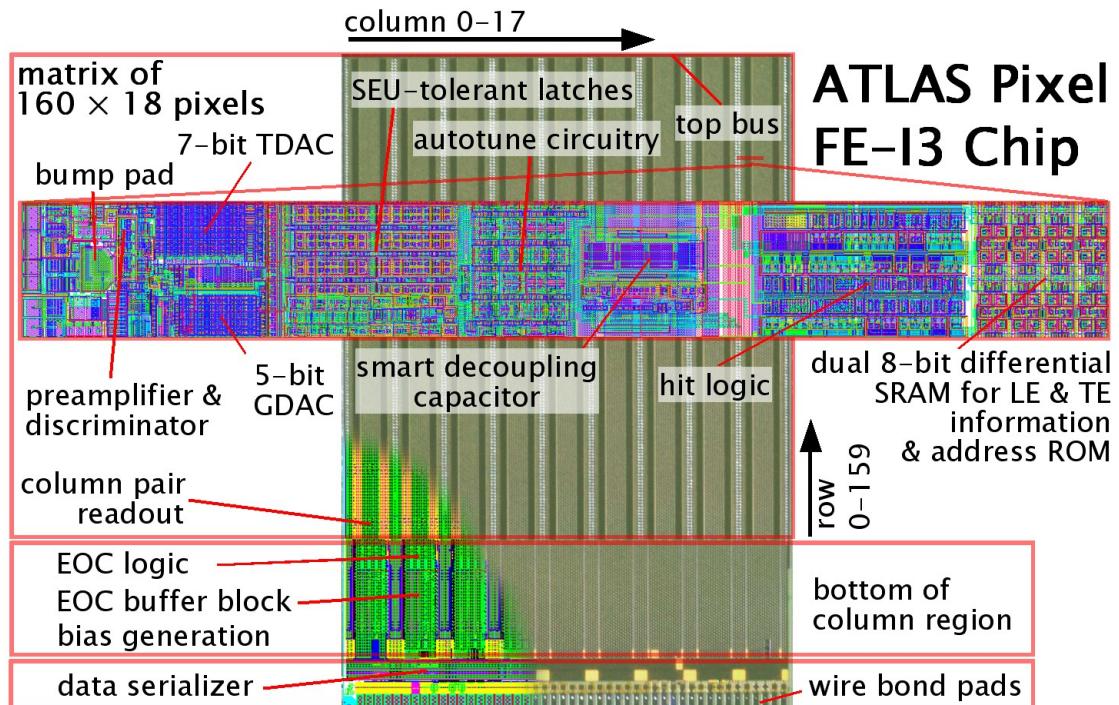


Figure 4-10 Layout of the ATLAS Pixel FE chip and a single pixel channel

can bee seen in Figure 4-11. A more detailed pixel cell schematic is given in Appendix A Figure A-3. The bump bond pad connects the sensor pixel with the inverting folded cascode preamplifier, which has the bias connections IP, IL and IVDD2. A DC feedback scheme can compensate DC leakage currents of more than 100 nA on the preamplifier input. The kill bit allows to disable the preamplifier without changing its power consumption. A 3-bit local FDAC⁸³ allows to separately regulate the feedback current for each pixel, whereas the bias currents IF and ItrimIF are used to globally adjust the feedback current for all pixels. The feedback capacitor is discharged by the constant current so that a triangular pulse shape is obtained.

The second stage differential pair amplifier and the discriminator follow the preamplifier. A 5-bit GDAC⁸⁴, its digital setting is distributed to local 5-bit DACs in each pixel, allows to adjust the overall threshold for a FE very linear and fine-grained. A 6-bit local TDAC⁸⁵ in each pixel (a 7th bit is used to choose in which of the two nodes to inject the current) is used to increase the threshold of a pixel with about 75 e⁻ per DAC count in the mid-range. These local trim bits affect both sides of the differential pair amplifier, resulting in a linear threshold vs. DAC behavior. The threshold can be varied from 0 to about 1 fC. The normal operation threshold is about 0.7 fC or 4 ke⁻ equivalent. Typical (most probably) MIP signals from the sensor are about 3.5 fC or 20 ke⁻ equivalent. After the lifetime dose of 10¹⁵ NIEL equivalent the sensor MIP signal decreases to 10 - 15 ke⁻. The width of the discriminator output signal is called TOT⁸⁶. Due to the linear discharge of the feedback current it is

⁸³ Feedback DAC

⁸⁴ Global DAC

⁸⁵ Trim DAC

⁸⁶ Time Over Threshold

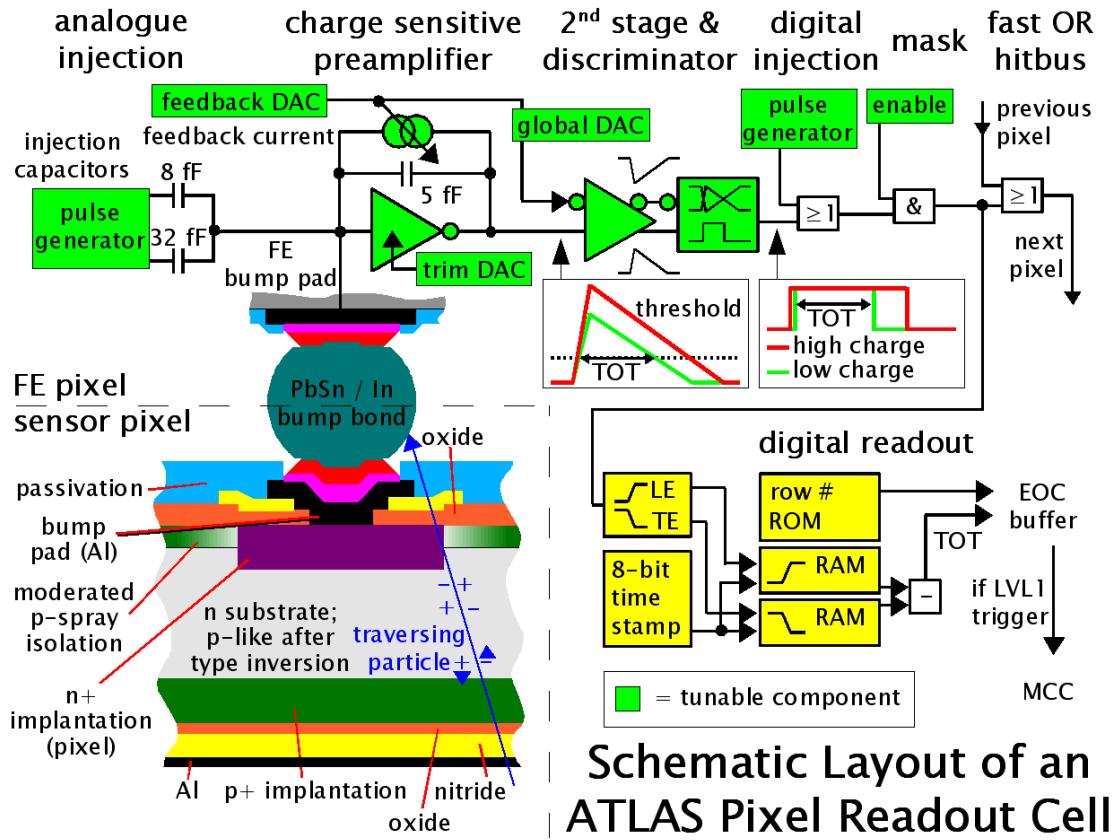


Figure 4-11 Block diagram of the FE pixel cell, its control blocks and its digital readout

proportional to the deposited charge in the sensor. The feedback is adjusted so that it's a good compromise between high TOT resolution and a small pixel dead time. The preamplifier and discriminator output signal shapes as well as their threshold and feedback current dependences are shown in Figure 4-12.

An analogue injection circuit is implemented in each pixel to test the pixel readout cell, tune the threshold and calibrate TOT. Two separate injection capacitors with nominal values of 8 fF for C_{lo} and 40 fF for $C_{lo} + C_{hi}$, are used. Either direct pulses on the external ExtInj line can enter into the capacitors or a voltage step is generated by using the Str signal to switch the capacitors from VDDREF down to VCAL, which is a voltage provided by a DAC in the bottom of column region.

If the digital hit injection circuit is enabled, the StrDig pulse is routed into the pixel control logic where it replaces the discriminator output signal. It can be used to test the pixel hit logic, the fast OR hitbus logic and the following readout. The TOT of the hit can be varied by changing the width of the injected pulse. The fast OR hitbus can be used to operate the FE in a self-triggering mode, for example to trigger on radioactive source hits. In this mode the FE generates LVL1 triggers by itself with a programmable latency.

To measure the deposited charge of a hit the TOT for the discriminator output pulse is measured in units of the 40 MHz crossing clock. The leading edge (LE) of the

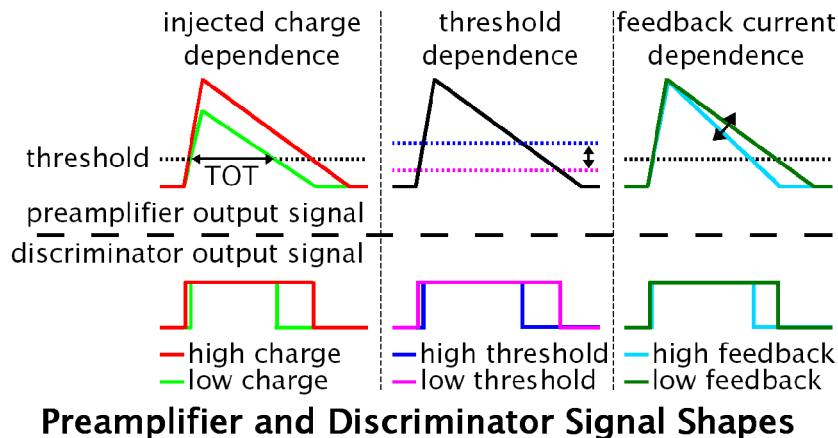


Figure 4-12 Injected charge, threshold and feedback current dependences of the TOT in the FE preamplifier and discriminator

discriminator output pulse triggers the storage of a timestamp in a 8-bit SRAM⁸⁷ cell. The timestamp is provided by a 8-bit wide Gray-coded [HAY01] counter incrementing each 25 ns beam crossing. The counter allows a maximal LVL1 latency of 6.4 μ s. The timestamp of the trailing edge (TE) is stored in a second SRAM cell and a busy and hitbus latch are set to active. These prevent an overwriting of SRAMs until the hit has been read out, since the ReadPixels line is used as the clock for both latches. The hitbus indicates to the EOC⁸⁸ logic in the bottom of column region that a hit occurred in the column pair. The CEU⁸⁹ state machine of the EOC freezes the column pair and the busy and hitbus latches are separated. It also starts the readout of pixels with hits into the 64 EOC buffers at the bottom of each column pair. Since each pixel only sends its hit information to the EOC buffers if no other pixels in front of the column pair readout chain show a hit the EOC buffers are filled sequentially.

Before written to the EOC buffers the hit data from the SRAMs are processed by a pipelined TOT processor. It converts the Gray-coded leading and trailing timestamp to binary values and subtracts the LE from the TE to get the TOT. The TOT processor can additionally apply single-crossing time slewing correction for hits below a settable TOT threshold or discard them. This is necessary since small charges undergo more time slewing. The time slewing correction copies hits below the settable TOT threshold and reduces the LE timestamp by one in the copy. The threshold correction suppresses writing of hits that are under a second settable TOT threshold to the EOC buffer [EIN03b].

A threshold autotuning block is implemented in each pixel. It contains a 5-bit up/down counter. It counts up/down for each injection with the requested threshold charge which passes/does not pass the discriminator. The counter is preset to its mid-point. If the counter is above its mid point after a number of injections the corresponding pixel is flagged above threshold and the counter is preset to its mid-point again. The threshold setting is scanned downwards and the autotuning block of each pixel separately and automatically stops to lower the threshold setting for this

⁸⁷ Static Random Access Memory

⁸⁸ End Of Column

⁸⁹ Column Extractor Unit

pixel when it is not flagged anymore.

A 16-word trigger FIFO⁹⁰ allows the FE to concurrently process hits from up to 16 different external LVL1 triggered bunch crossings. The timestamp of a second timing bus is delayed to the Gray-counter by an adjustable latency. It must be equal to the LE time of a hit to start its readout from the EOC buffer. If a LVL1 trigger exists for this hit, it is sent by the readout controller through the data serializer to the MCC. Therefore hits with a LE timestamp equal to the second timing bus are deleted from the EOC buffers if no LVL1 trigger arrived for them during the latency.

Three registers are used to control the FE chip. These are the global register, the command register and the pixel register. They have a common interface with three CMOS⁹¹ inputs and are based on a simple serial protocol. The inputs are the data input (DI) line, the load (LD) signal and a 5 MHz CCK⁹², whose presence activates the command decoder. A 29-bit command field is transmitted to the FE when LD is low. It is stored in a command shift register, which is formed by a series of standard DFF⁹³ cells. The shift register data is latched into the SEU-tolerant command register latches when LD rises. The command field determines whether the FE is addressed by a 4-bit geographical address and whether a data field is expected. A data field of arbitrary length is transmitted during LD is high.

The data field can be shifted to the global register, which contains a 231-bit global shift register. It is also formed by standard DFF cells. The data can be transferred from the shift register into the SEU-tolerant global register latches by a 'WriteGlobal' command. A read-back to the shift register is possible by a 'ReadGlobal' command. The bits of the global register are distributed throughout the bottom of column region, in order to have them close to circuits they control.

The data field can also be transferred to the pixel register. It is first shifted to a pixel shift register, which consists of nine 320-bit MUX⁹⁴ cell registers corresponding to one column pair each. This nine segments can be individually enabled or disabled by setting the corresponding bit in the global register. 14 SEU-tolerant configuration latches in each pixel form the pixel register. 14 different 'Load' commands can be used to simultaneously transfer the data from the pixel shift register to the corresponding set of latches in the pixels. A read-back to the pixel shift register by another set of 14 commands is implemented as well. The structure of the three registers and their writing and readout is shown in Figure 4-13.

If a SEU occurs in one of the three registers, the corresponding register has to be refreshed. Since writing to the global and pixel register is only possible when the data-taking of the FE is disabled this leads to a dead time for the entire FE. The refresh time for an entire module is roughly 1 ms for the global registers and 200 ms for the pixel registers. To minimize the risk of SEUs in the registers SEU-tolerant latches, so-called DICE⁹⁵ cells [CAL96], are used for the 14 pixel register latches in each pixel. The schematic of a DICE cell is illustrated in Appendix A Figure A-4. To flip this latch a simultaneous writing to two nodes is necessary. Thus, to reduce the SEU

⁹⁰ First-In, First-Out

⁹¹ Complimentary Metal-Oxide Semiconductor

⁹² Command ClocK

⁹³ Delay Flip-Flop

⁹⁴ MULTipleXer

⁹⁵ Dual Interlock Storage CELL

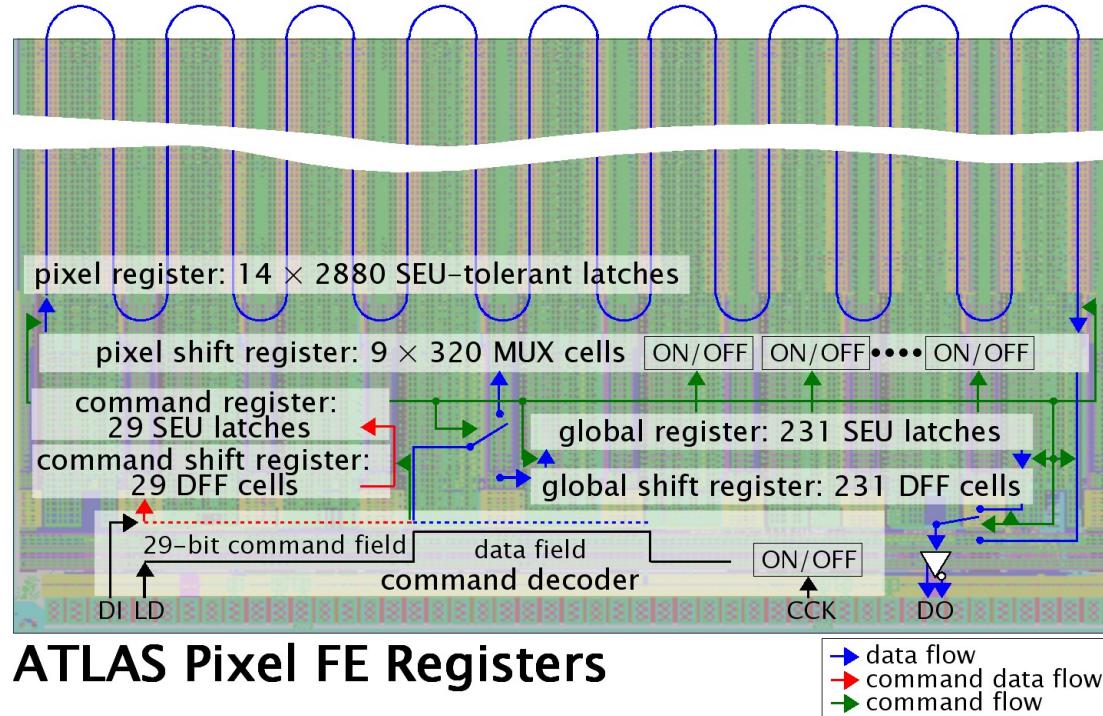


Figure 4-13 The three different FE registers and their shift registers

probability both sensitive nodes are separated about $5\text{ }\mu\text{m}$. Additional redundant reset signals are implemented for the global and command register latches. Both registers use a triple-redundancy scheme to improve their SEU-hardness. A majority-logic is used in each bit-slice to determine the combined output of the three cells and to provide a bit-flip flag if the three storage cells do not have identical values. This bit-flip flag allows to measure the single DICE cell upset rate. An overall parity is defined for the combined global and command register and allows to measure the upset rate of the triple-redundant DICE cell. It can be used to trigger a refresh of the register.

The preamplifier of a standard pixel readout cell sees a capacitive load of about 300 fF from the sensor. Increased preamplifier input capacitive loads of about 450 fF for long pixels are not large enough to need a design change. For ganged and long+ganged pixels with capacitive loads of about 1000 fF a change is necessary in order to achieve an acceptable timewalk for all pixels. The timewalk is the dependence of the TOT value from the analogue injected charge. In row 153, 155, 157 and 159 readout cells have four times the nominal preamplifier control current (IP) and an input transistor that is three times the nominal size. Inter-ganged and inter-long+ganged pixels also see an increased capacitive load of about 700 fF due to the metal interconnections on the sensor. Therefore the pixels in row 152, 154, 156 and 158 have two times the nominal IP current and an input transistor that is two times the nominal size. Although pixels in row 152 are not inter-ganged the row was modified to preserve the symmetry of the layout.

All bias generating circuits are located in the bottom of column region. The bias voltages are distributed throughout the pixel matrix of a FE using horizontal buses.

This so-called top bus is located at the top of the chip. This layout avoids interference between the analog biasing and the fast digital signals. The biases are distributed as the $V_{\text{gate-source}}$ of a diode-connected FET⁹⁶ in the bottom of column region. In each pixel a matching mirror transistor is used to regenerate the current. A single active voltage drop compensation circuit is implemented in each pixel. Even rows have a second stage amplifier (IL2) compensation circuit, odd rows an IP one. A monitoring scheme allows to multiplex out the IP or IL2 current from each individual pixel.

The pad frame of the FE-I3 chip contains 47 I/O pads of $100 \times 200 \mu\text{m}^2$ on a $150 \mu\text{m}$ pitch. It is located at the bottom of the chip. For redundancy and reduced internal voltage drops the three power supplies have all two input pads. LVDS⁹⁷ compatible differential drivers and receivers are used to perform all high-speed I/O from and to the FE. The output drivers use a reduced output current of 0.5 mA instead of the standard 3.5 mA. A 600Ω terminator resistor is used in the receiver to produce the standard 300 mV signal swing. CMOS pads are used for less critical I/O. Some of them use pull-up or pull-down resistors to determine their default state.

4.3.4 Module Controller Chip

The MCC performs the task of the module event building, controls the 16 FEs, is responsible for compressed data transfer out of the module and provides error detection for data overflows. The MCC-I2.1 [BEC03a-b],[DAR03] is produced in $0.25 \mu\text{m}$ DSM technology as well. It consists of about 880 k transistors and its dimensions are $6.84 \times 5.14 \text{ mm}^2$. A block diagram of the MCC and its connections to the FEs are shown in Figure 4-14.

The 40 MHz CK clock is synchronous with the LHC bunch crossing. It is used by the MCC to synchronize the data input line DTI and the two MCC output lines DTO and DTO2. For data and CK transmission between the module MCC and the optoboard LVDS differential signals are used. The so-called module port in the MCC is the driver and receiver block for the optoboard communication. The output bandwidth of the MCC can be set to 40 Mbit/s or 80 Mbit/s single-link mode. In 40 Mbit/s mode only the rising edge of the 40 MHz clock indicates a bit, whereas in 80 Mbit/s the falling edge indicates a bit as well. In both modes the same data is synchronously transmitted on DTO and DTO2. In 80 Mbit/s or 160 Mbit/s dual-link mode the data is bit-wise alternately distributed between DTO and DTO2. The dual-link bandwidths are necessary for modules in the B-layer, which have to cope with high event rates. Therefore the B-layer modules are connected to 'B-layer' optobooks, which support dual-link data transmission (see section 4.4). From the CK the MCC generates the XCK clock with the same frequency and the CCK clock with 5 MHz. XCK is used to clock the FEs and serves via the external XCKIN connection as main clock for the MCC itself. This layout minimizes the skew of the clock between all FEs and the MCC of a module. The CCK is used for data transfer from the MCC to the FEs.

Unidirectional interconnections are used between the 16 FEs and the MCC. The driver and receiver block for the FEs is the so-called FE port. 16 separate LVDS serial data links with up to 40 Mbit/s transfer rate each are used for data transmission from the

⁹⁶ Field Effect Transistor

⁹⁷ Low Voltage Differential Signaling

FEs to the MCC. They are in phase with the XCK clock. This star topology has a higher failure tolerance and allows smaller FE buffers, due to a lower FE buffer occupancy. A 'data push' protocol is used. After a LVL1 the FEs send data exactly after a (settable) latency has elapsed. The hits from the FE EOC buffers are ordered by event number and are followed by an EoE⁹⁸ word to keep event synchronization. The EoE word is submitted even if a FE doesn't have any hits for the LVL1 triggered timestamp. In the MCC the hit data is written into the 27-bit shift register of one of the 16 identical receiver blocks [BEC02a]. The shift register flags to a control state machine if the stored word is a hit or an EoE word. The control state machine keeps track by two up-down counters how many hits and EoE words are currently stored in a receiver FIFO. If less than 16 EoE or 112 hit words are stored in the FIFO the control state machine shifts the word from the shift register to the receiver FIFO. Otherwise it drops the word, but sets a 'HitOverflow' or 'EoEOverflow' warning flag in the next EoE word in order to keep up with event synchronization. The receiver FIFO is a 128×27 -bit wide dual port SRAM full custom block. It is necessary to derandomize the hit data, which are send with random fluctuations of data rate by the FEs. 7-bit read and write pointers for the FIFO are provided by the control state machine as well. The control state machine cannot stop the FE from transmitting data, but it blocks the LVL1 trigger to the FEs to avoid mixing of hits belonging to different events, whenever an EoE overflow has been recognized.

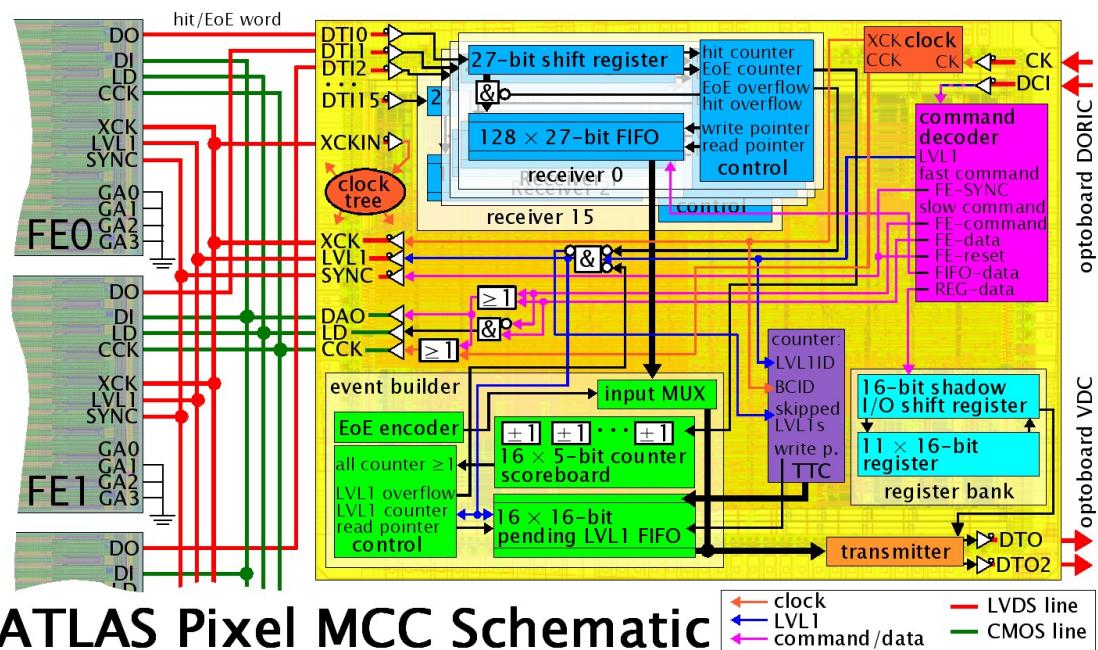


Figure 4-14 MCC block diagram and routing to the FEs

Each time an EoE word is detected in one of the receiver blocks the scoreboard formed by 16 individual 5-bit up-down counters in the event builder [BEC03c] block is updated. This means the counter for the corresponding receiver channel is incremented. As soon as the control state machine of the event builder block finds a complete event (all counters are not zero) it shifts the last word from the pending

LVL1 FIFO to the transmitter. The fully synchronous and single-clocked LVL1 FIFO is 16-bit wide and 16 word deep. It contains the last 4 significant bits of the 8-bit LVL1ID⁹⁹ counter, the 8-bit value of the BCID¹⁰⁰ counter and the number of skipped LVL1s in the remaining 4 bits. These counters are implemented in the TTC¹⁰¹ block. The BCID counter is incremented at each XCK clock cycle and the LVL1ID counter each time a LVL1 is detected by the MCC. The write pointer to the pending LVL1 FIFO is provided by the TTC, whereas the read pointer is provided by the event builder control state machine. After the transmission of the pending LVL1 FIFO word the receiver FIFOs are read out sequentially. The EoE word is used to stop the readout of each FIFO. The receiver FIFO output data streams are multiplexed by the input multiplexer to the transmitter. The address of the next FIFO depends on which FEs are activated in the register bank and is provided from the EoE encoder. All scoreboard counters are decremented after the entire serial data stream has been sent by the transmitter throughout DTO and/or DTO2. The LVL1 counter in the control state machine of the event builder keeps track of the number of LVL1s send to the FEs and can block the LVL1 output to the FEs if more than 15 LVL1s are still pending.

Eleven 16-bit configuration and status registers have been implemented in the register bank [BEC03d]. Some of them can be modified by the MCC itself. They are readable and writeable through DTO and DCI and the commands described below. The configuration and status registers contain for example the bandwidth mode of both DTOs, the activation status of the FEs and the detection of a SEU in one of the MCC blocks. The shadow I/O shift register in the register bank avoids any temporary change of bits that would not be changed by a read or write command. This allows to read back the register contents to the shift register and submit it via DTO and/or DTO2.

The command decoder [BEC03e] interprets the DCI data stream coming from the optoboard. All commands belong to one of the three groups: LVL1, 'Fast' or 'Slow'. A 5-bit LVL1 trigger word command can be issued every 125 ns. 'Fast' commands consist of 5 header and 4 body bits and can be transmitted to the MCC in the absence of a LVL1 command without stopping the data acquisition. They are used to reset the BCID and LVL1ID counters or to generate a pulse on the 'Str' line, which provides the timing for calibration strobes of the FEs. A 'Fast' command can be used as well to generate a SYNC signal, which provides a hierarchy of synchronous resets to the FEs. 'Slow' commands are subdivided into a 9-bit header, an 8-bit body and eventually a data field of arbitrary length. As soon as a 'Slow' command is detected by the command decoder the data acquisition is blocked. 'Slow' commands are used to reset the MCC. This means all registers, FIFO pointers and status flags are set to their default value. 'Slow' commands also allow to globally reset all FEs of a module, to read (write) data from (into) the register bank or the receiver FIFOs and to transmit configuration data to the FEs. Since the DI line of the FEs is referenced to the 5 MHz CCK each bit of the FE configuration data in the MCC DCI stream, which is referenced to the 40 MHz CK, has to be repeated eight times. Two further 'Slow' commands allow to send commands to the FEs. They allow to read back the FE configuration data, which is transmitted unchanged throughout both DTO lines, and to start the data acquisition again.

⁹⁹ LeVeL 1 IDentification

¹⁰⁰ Bunch Crossing IDentification

¹⁰¹ Trigger, Timing and Control

Each FE is addressed by a 4-bit geographical address (GA). The FEs have four CMOS inputs with pull-up resistors, which provide a 'one' for the address bit in the default state. All four GA pads on the FEs are wire-bonded to the corresponding pads on the module flex. Appropriate to their FE position some of these pads are connected to digital ground (DGND) which provides a 'zero' bit for the address.

To avoid errors caused by SEUs the command decoder has been triplicated with a majority logic on all outputs. Triple-redundant bits with majority logic are used for the register bank and the event builder control state machine as well. Three separate SEU warning bits, one for each of the three blocks, are set whenever a SEU is detected in the corresponding block. This warning is most important for the register bank since no automatic SEU correction has been implemented here. Therefore the correct values should be rewritten to the register bank as soon as possible. All FIFO pointers and control signals provided by the receiver blocks have been triplicated but no SEU warning bit is set in case of a SEU. Due to their size it was not possible to triplicate the scoreboard and the transmitter.

4.4 Optoboard

Optical links are used for all data transfer from and to the modules to avoid problems caused by ground loops and electromagnetic interference. Additionally they have the advantage of high bandwidth and low radiation length. Conversions between optical and electrical signals are provided by an optoboard [GER03],[CHU03] attached to each PP0 row. Either six or seven modules are connected through 70 to 130 cm long Type0 cables to one optoboard. Modularity six is used to read-out disk sectors and one barrel stave side. Modularity seven is used by the other half-stave, whereas the higher modularity is alternated between the two detector sides. For the readout of the entire detector 288 optoboards (including spares) are mounted on the PP0s. Type0 cables for barrel modules are made of 100 µm polyurethane isolated aluminum wires for signal and sensor bias voltage lines. Both have a 25 µm thick insulation. For twisted-pair signal lines this provides the desired impedance of 75Ω and for the HV lines a electrical insulation of more than 2.5 kV. For power and sense return lines 300 µm aluminum wires are used. The wires are micro welded to small PCB¹⁰²s with a soldered Type0 connector [EYR03] at both ends. Disk module Type0 cables are soldered directly to the module flex. On the other side they are soldered to the Type0 connector PCBs. They use 400 µm polyurethane isolated copper clad aluminum wires for power and sense return lines and 62 µm pure copper wires for signal and sensor bias voltage lines (polyimide insulation). Disk Type0 cable bundles are surrounded by a silicone tube. In both designs each Type0 cable bundle consists of 21 wires and the data wires are twisted-pair.

Optoboards are $2 \times 6.5 \text{ cm}^2$ beryllium oxide printed circuit boards. Beryllium oxide is used due to its low radiation length and high thermal conductivity while being a good electrical insulator. The two sides of an optoboard are shown in Figure 4-15. On the bottom side a 80-pin SMT connector, a PiN¹⁰³ diode array with MT-8 connector

¹⁰² Printed Circuit Board

¹⁰³ Positive-intrinsic-Negative

housing and two 4-channel DORIC¹⁰⁴ chips are mounted. The SMT connector provides all electrical connections from the PP0 to the optoboard. This includes the DCI, CK, DTO and DTO2 signal lines for seven modules and the power and control lines for the optoboard itself. The array of eight epitaxial silicon PiN diodes is used to receive the data sent by off-detector readout electronics (see section 4.6) to the modules. The PiN photodiodes are made from an n-type substrate. The substrate has a low doped background (intrinsic) n-type layer, followed a p-type layer grown epitaxially on top. The intrinsic layer provides a thin active layer, which allows fast operation at low PiN bias voltage. The nominal PiN bias voltage (V_{PiN}) is -10 V. The circular active area of the PiN diode has a diameter of 130 μm and the depth of the intrinsic region is 35 μm . The responsivity was measured to about 0.6 A/W before irradiation. It linearly degrades during irradiation with 30 MeV protons to 50% at fluences of $5.7 \times 10^{14} \text{n}_{\text{eq}}(1 \text{ MeV}) \text{ cm}^{-2}$, which is about double of the end-of-lifetime dose for optoboards [HOU05].

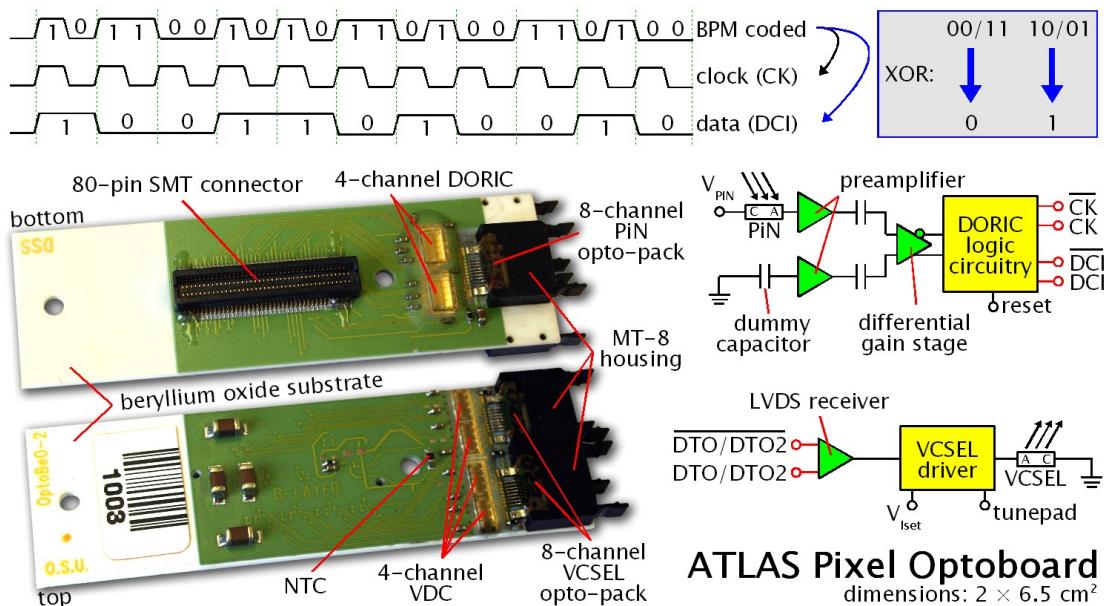


Figure 4-15 Optoboard, block diagrams of the DORIC and VDC circuits and an example of a BPM coded signal and there decoded clock and data signals

The DORICs are produced in 0.25 μm DSM CMOS technology. They are implemented as 4-channel chips handling four input signals in parallel. They decode the BPM¹⁰⁵ encoded clock and data signals received by the PiN diodes to recover the 40 MHz CK clock and the 40 Mbit/s DCI data stream, which are provided to the modules. Figure 4-15 shows an example of a BPM coded signal. It can be encoded from the 40 MHz clock and the 40 Mbit/s data signal by always sending transitions corresponding to clock leading edges and to clock trailing edges only if data is on logic level one. This results in a 20 MHz square wave in absence of data bits (string of logic level zeros) and for a string of logic level ones in a 40 MHz square wave. BPM coded signals provide better synchronization since a change of polarity happens at least every two bits and synchronizations problems with long series of ones or zeros

104 Digital Optical Receiver IC

105 Bi-Phase Mark

are avoided. Another advantage is that the clock can be recovered from the BPM coded signal as well. Additionally the duty cycle of the BPM signal is 50%, thus there is no baseline shift due to a different number of transmitted data bits. A drawback is the necessary doubling of the clock frequency.

The amplitude of the current from the PiN diode can be between 40 to 1000 μ A. In order to keep V_{PiN} off the DORIC a single-ended preamplifier is used to amplify the current produced by the PiN. For noise cancellation an identical preamplifier with a dummy capacitance, which matches the PiN capacitance, is used. The noise is subtracted from the signal in a differential gain stage. The gain stage incorporates internal feedback to adjust its threshold to maintain 50% duty cycle over the entire current input range. It is basically a comparator, which converts the linear output of the preamplifiers to logic units for the DORIC logic circuitry. The schematic of the DORIC logic circuitry is shown in Appendix A Figure A-5.

During an initialization period after power-up only logic level zero are transmitted. This results in a 20 MHz square wave. An edge-detect circuit in the DORIC logic circuitry produces a short pulse from each input transition, resulting in a 40 MHz train of short pulses. A D flip-flop is connected as toggle with 18.75 ns delayed feedback, resulting in a 20 MHz square wave. The delay is achieved by three identical delay stages with a nominal delay of 6.25 ns each. The inputs of a 'XOR' are connected to the output of the first and third delay, so that they are about 90° out of phase. The output of the 'XOR' is the recovered clock. The duty cycle is correlated with the exact delay of the second and third delay stage. Thus the recovered clock is the input to a delay control circuitry, which converts the duty cycle to a DC voltage used to control the delay of the three delays and the output pulse width of the edge-detect circuitry. The duty cycle of the recovered clock is kept close to 50% by this delay-lock-loop, formed by the two delays, the 'XOR' and the delay control circuit. The settling time of the delay-lock-loop during the initialization is about 1 ms. A reset line allows to restart the delay-lock cycle without power cycling the DORIC.

When the loop is locked edge detect pulses belonging to data are ignored by the first D flip-flop. All edge detect pulses are sent through a short edge delay to the 'clk' input of a second D flip-flop. The flip-flop 'd' input is connected to the recovered clock. The output of the flip-flop are recovered data pulses. A third D flip-flop synchronizes the recovered pulses with the recovered clock and increases their width to 25 ns. The recovered clock and data are send throughout a LVDS driver to the module CK and DCI inputs.

On the top side of an optoboard two VCSEL¹⁰⁶ laser arrays with MT-8 connector housings, four VDC¹⁰⁷s driver chips and a NTC are mounted. This full equipped version of the optoboard is called B-board and allows data transmission from the modules up to 160 Mbit/s dual-link mode (see section 4.3.4). These optobards are used for B-layer modules since their high hit occupancy requires high bandwidths. Optobards for Layer-1, Layer-2 and disk modules are equipped with one VCSEL array and two VDCs only and are called D-board. They support data bandwidths up to 80 Mbit/s single-link mode. Depending on which of the VCSEL array and belonging VDCs are mounted either the DTO or DTO2 module data stream is transmitted to the off-detector readout electronics. Since in single-link mode the MCC submits the same

106 Vertical Cavity Surface Emitting Laser

107 VCSEL Driver Chip

data throughout both output lines the usage of DTO or DTO2 D-boards can be freely decided by mechanical constrains.

The VDC chip is implemented in 25 μm DSM CMOS technology with four channels per chip. It is used to convert DTO or DTO2 LVDS input signals into a single-ended current signal, which is able to drive a VCSEL of a common cathode array. An LVDS receiver converts the differential signal into a single-ended input signal for the VCSEL driver. The current flow from the positive power supply voltage into the anode of the VCSEL is controlled by the driver. The amplitude of the VCSEL current can be set by a control current (I_{set}), which is determined by an external control voltage ($V_{I_{\text{set}}}$). The dim current can be set through an external tunepad voltage. The tunepad is the junction of a resistor from the positive VVDC supply and a diode-connected FET, which sets a dim current of about 1 mA. This dim current is set to improve the VCSEL switching speed. Since this default dim current is satisfactory the pad is left floating and no external voltage is applied. The VDC output current can be varied between 0 and 20 mA with a nominal value of 10 mA. A dummy driver circuit is implemented to assure constant current consumption of the VDC. It draws the same current through the VCSEL in the dim and bright state. VDCs and DORICs use the same VVDC supply voltage with a nominal value of 2.5 V. Both optoboard chips show no radiation damage with up to ~ 61 Mrad of irradiation.

Advantages of the used 8-channel common cathode VCSEL arrays are the fast rise and fall times and the high light output at very low currents. VCSELs with an oxide implant are used to achieve current confinement, which produces lower thresholds and allows higher bandwidths. At a drive current of 10 mA the typical fiber coupled power per channel is greater than 1 mW. Irradiations with 24 GeV protons up to $(8\text{-}12) \times 10^{14}$ p/cm² show degradation of the light power down to about 60% during irradiation, but also return to almost the original power after long annealing. The optical rise and fall times are about 400 ps and do not significantly change with irradiation [ARM05].

4.5 Optical Connection

The length of the optical cables from PP1 to the off-detector readout electronics is roughly 80 m. At PP1 two 8-way ribbons are terminated with one MT-16 connector. Eight TTC ribbons (CK and DCI signals to the modules) are bundled to one optical TTC cable and eight module-data ribbons (DTO and DTO2 signals from the modules) to one optical module-data cable. For the inner ~ 12 m radiation hard SIMM¹⁰⁸ fibers, same type as for the optical connection between the optoboards and PP1, are used. They are spliced to radiation tolerant Draka¹⁰⁹ GRIN¹¹⁰50 (50 μm core diameter) fibers for TTC and to GRIN62.5 fibers (62.5 μm core diameter) for module-data. The radiation hard and radiation tolerant fibers are spliced together at PP2¹¹¹ just outside the innermost muon spectrometer layer. At the off-detector readout electronics the

¹⁰⁸ Stepped Index MultiMode

¹⁰⁹ Draka Comteq Optical Fibre, Eindhoven, Netherlands » www.drakafibre.com

¹¹⁰ GRAded INdex

¹¹¹ Patch Panel 2

cables are fan-out two single 8-way ribbons, each terminated with a MT-8 connector. A schematic view of the readout chain [GER03],[BEC02b] is shown in Figure 4-16.

4.6 Readout Electronics Crate

The Pixel off-detector readout electronics is arranged in the counting room in nine 9U VME64¹¹² crates with custom backplanes. A crate contains up to 16 BOC¹¹³ cards [FLI06a-b], which are the opto-electrical interfaces in the counting room. Each BOC is paired with a ROD [JOS06], which is the main data taking and control card of the readout electronics. A TIM¹¹⁴ [WAR05] in the crate is the interface to the ATLAS TTC signals from the CTP. The RCC¹¹⁵ [HIL00] single board computer of a crate is used to control and configure the up to 16 ROD/BOC pairs. The layout of a Pixel crate and its connection to the ROS¹¹⁶ [CRA02] are shown in Figure 4-17.

4.6.1 Back Of Crate Card and Optical Plugins

The TTC ribbons are connected to so-called TX-Plugin boards and the module-data ribbons to RX-Plugin boards [CHU04]. Both plugin board types are attached to a BOC. Depending on the hit occupancy of the connected modules 1, 2 or 4 TX-Plugins and 2 or 4 RX-Plugins are connected to a single BOC. B-layer modules are read-out in 160 Mbit/s dual-link mode and the corresponding BOCs are equipped with one TX-Plugin and two RX-Plugins, thus one BOC can readout one half-stave. BOCs for Disks and Layer-1 modules work in 80 Mbit/s single-link mode and have two TX-Plugins and two RX-Plugins connected. Therefore each BOC reads-out two half-staves or sectors. For Layer-2 modules 40 Mbit/s single-link readout is used and the BOCs have four TX-Plugins and four RX-Plugins to readout four half-staves.

The transmitter (TX) plugin boards contain a BPM ASIC¹¹⁷, which is used to BPM encode the common input 40 MHz P-clock with the individual 40 Mbit/s TTC data streams. The P-clock and other clocks are generated by the BOC (see below). Each channel incorporates a VCSEL driver circuitry as well. The VCSEL laser current can be controlled by two MDAC¹¹⁸'s on the TX-Plugin in 256 steps from 0 to 18 mA. Since the MDAC registers are not readable, a copy of the setting value is stored in a readable RAM¹¹⁹ additionally. The BPM allows to individually delay TTC data streams with a coarse delay (0 to 775 ns with 25 ns stepsize) and a fine delay (0 to 35.56 ns with 280 ps stepsize). These delays allow an individual module timing and compensation of different optical fiber and Type0 cable lengths, thus a synchronization of the modules to the bunch crossing is possible. Masking the

¹¹² Versa Module Europa

¹¹³ Back Of Crate

¹¹⁴ TTC Interface Module

¹¹⁵ ROD Crate Controller

¹¹⁶ Read-Out Subsystem

¹¹⁷ Application Specific Integrated Circuit

¹¹⁸ Multi channels DAC

¹¹⁹ Random Access Memory

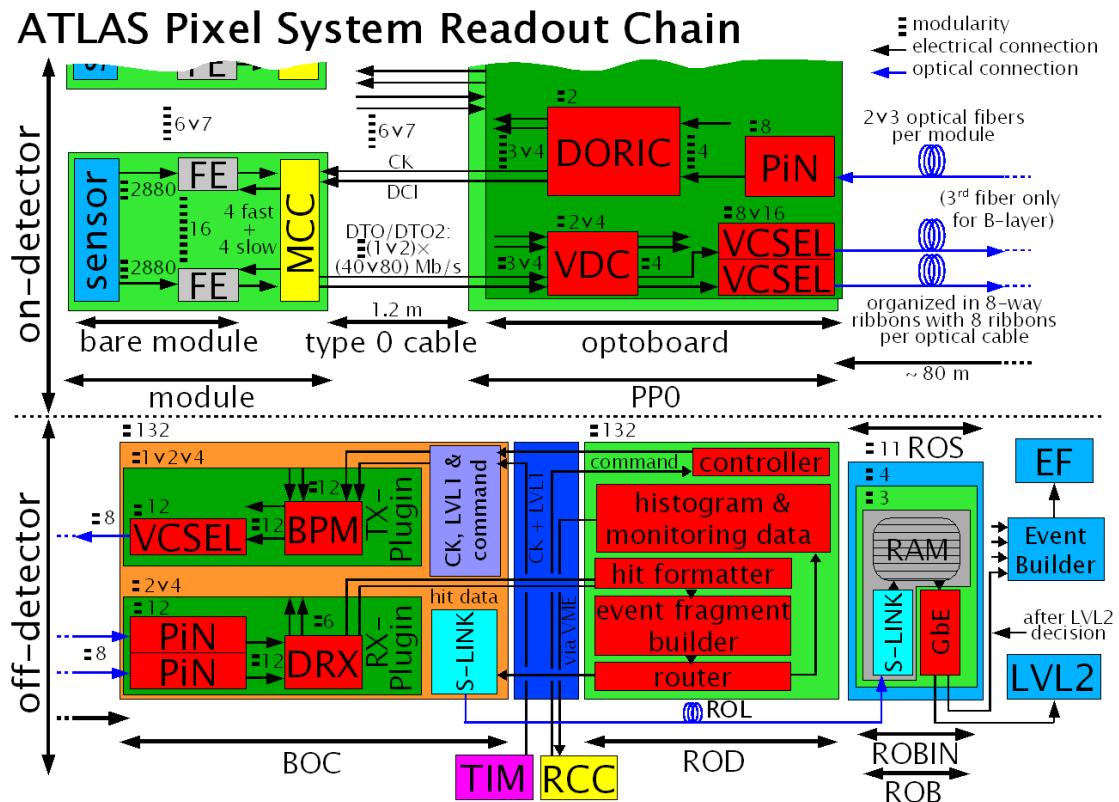


Figure 4-16 Readout chain with on- and off-detector readout electronics

encoding of data for individual TTC data streams is provided by the BPM, as well as the individual adjustment of the output signal mark space ratio from 30:70 to 70:30 in 32 steps. Up to seven individual module TTC data streams are submitted via an 8-channel VCSEL array on the TX-plugin to an optoboard.

The receiver (RX) plugin boards incorporate an 8-channel PiN array. A DRX¹²⁰ ASIC is used to reproduce the data signals received from an optoboard by discriminating the electrical signals from the PiN array. Each channel consists of a DC coupled comparator and has an individually adjustable threshold. The thresholds can be set by MDAC controlled reference voltages to corresponding input signal amplitudes between 0 and 255 μ A in 256 steps. A LVDS driver per channel provides the recovered module data stream to the BOC. The BPM and DRX ASICs can cope both with up to 12 channels. They have been designed with modularity 12 for SCT, but are only used with modularity eight for the Pixel Detector.

The BOC, as shown in Appendix A Figure A-6, interfaces the ROD to the on-detector electronics and to the following readout electronics (ROS). Its functional sections are a clock section, a clock and command section, a data receiver section and a S-LINK¹²¹ module. All sections are controlled by a control CLPD¹²², which is also responsible for the ROD-BOC communications through the so-called setup bus.

120 Driver Receiver IC

121 Simple-LINK » hs1.web.cern.ch/HSI/s-link

122 Complex Programmable Logic Device

The clock section receives the 40 MHz system clock via the back plane from the TIM and multiplexes it to five clocks. The ROD-clock is a direct copy of the system clock and is passed to the ROD. Another clock copy (A-clock) serves as clock source for all delay circuits (PHOS4) on the BOC. The P-clock can be delayed in 1 ns steps between 0 and 24 ns and is sent through the clock and command section to the TX-Plugins. This is the clock the modules see as the CK clock. The B-clock can be delayed between 0 and 24 ns as well and is used for the module data recovery in 40 Mbit/s sampling mode. Since the B-clock sampled data is sent to the ROD, the B-clock has to have an optimal and fixed phase to the ROD-clock. The second data recovery clock, the V-clock, is additionally used for the data recovery sampling in 80 Mbit/s mode. It can be delayed between 0 and 49 ns in 1 ns steps and additionally in 40 ps steps between 0 and 10.2 ns.

The clock and command section on the BOC receives the P-clock from the BOC clock section and module command data streams from the controller FPGA¹²³ of the ROD and passes them to the TX-Plugins. The data receiver section on the BOC uses 4-channel PHOS4 [CER00] ASICs to delay the RX-Plugins output signals between 0 and 24 ns in 1 ns steps to be in correct phase with the ROD-clock. Each of the four receiver section CPLDs can be used to handle up to eight data streams from one RX-Plugin. In the CPLDs the data stream is sampled with the B-clock and clocked out to the ROD with the B-clock as well. Thus the output data has a stable phase to the ROD-clock. For 80 Mbit/s streams the CPLDs perform a split into two 40 Mbit/s streams. For the second sampling the V-clock, which is adjusted to be the inverted B-clock, is used and clocked out with the B-clock as well. Thus the 80 Mbit/s bits are distributed in turn to the two 40 Mbit/s streams. This results in one output stream per 40 Mbit/s module, two per 80 Mbit/s module and four per 160 Mbit/s module. The doubling of the output streams is the reason for the connection of less module to BOCs that are readout in higher bandwidth modes. To equally balance the load of CPLDs in different readout bandwidths, a routing board (piggy-back) is attached to the BOC card. It allows a routing between the CPLDs so that in 40 Mbit/s mode each CPLD processes up to eight input streams and in 80 or 160 Mbit/s mode each CPLD processes up to four 80 Mbit/s streams. To avoid a timing difference between streams that are rerouted to another CPLD and streams that are not, the not rerouted streams are clocked out and received by the CPLD as well.

The HOLA¹²⁴ S-LINK module on the BOC is used to transfer event fragments from the ROD via the ROL¹²⁵ to a ROB in the ROS. It is a standard implementation of a 2 Gbps S-LINK transceiver which can transfer data at the full S-LINK bandwidth of 160 MB/s with only one duplex fiber.

The current consumption and voltage of the PiN diode arrays on the RX-Plugins can be measured. The PiN current measurements on the BOC is realized with low pass filters and ADCs. This allows the measurement of the average PiN current produced by all incoming optical signals of a PiN array. The temperature of the BOC is monitored at the TX- and RX-Plugin region with two NTCs. The BOC additionally provides laser interlock functionalities (see section 4.8.2), which switch off the TX-Plugin lasers if an interlock occurs.

¹²³ Field Programmable Gate Array

¹²⁴ High-speed Optical Link for Atlas » <http://hsi.web.cern.ch/HSI/s-link/devices/hola/>

¹²⁵ Read-Out Link

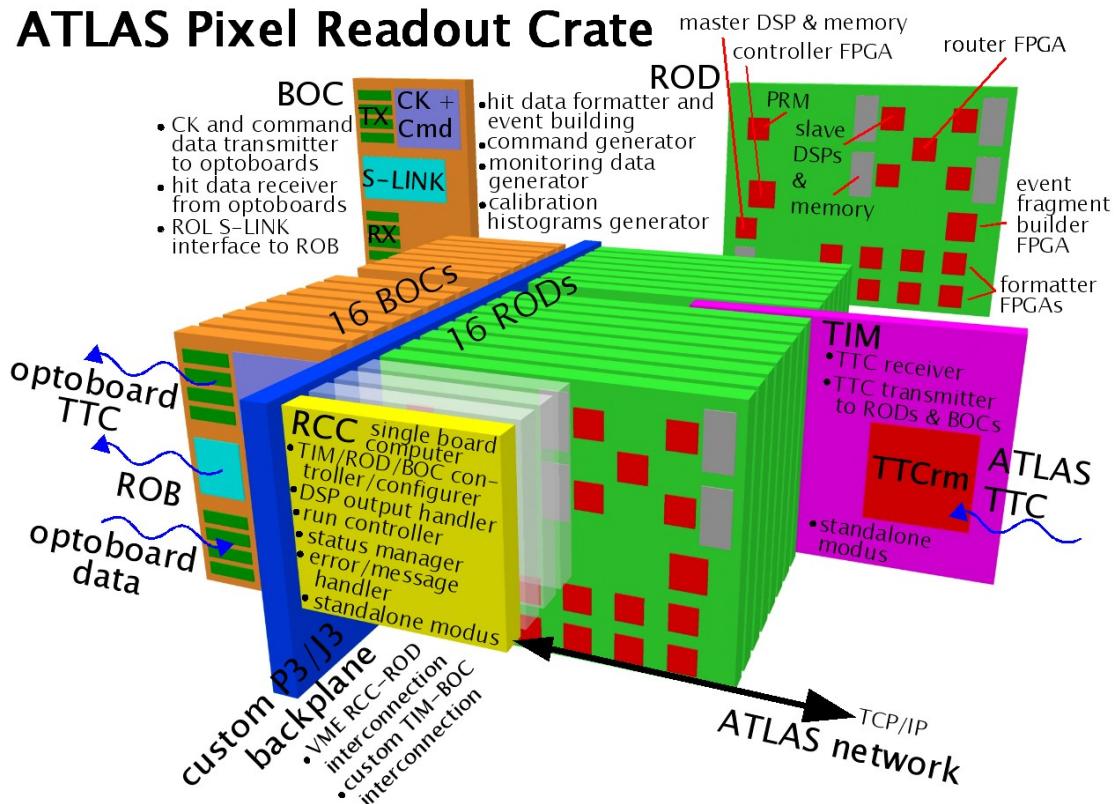


Figure 4-17 The ATLAS Pixel readout crate and its components: BOCs, RODs, TIM and RCC

4.6.2 Readout Driver

The ROD is the main Pixel module control and module-data receiver electronics (see Appendix A Figure A-7). It sends control commands to the modules as serial data streams. These commands include LVL1 triggers, BCID and LVL1ID counter resets, calibration commands and module register data. The serial return module-data stream includes event data and module register data. The event building combines several module-data streams to an event fragment. The ROD is able to detect and mark formatting errors in the return data stream and provides event data monitoring and module calibration functionalities for the return data.

Main control of the ROD is performed by a controller FPGA and a master DSP¹²⁶. The FPGA performs real time functions whereas the master DSP runs software to perform system functions. Both are initialized by the PRM¹²⁷, which loads the FPGA and master DSP boot code from flash memories. The flash memories can be read and written by the RCC readout crate single board computer through the VME bus. The basic task of the controller FPGA and the master DSP is the configuration of ROD, BOC and Pixel modules as well as the propagation of LVL1 triggers received from the TIM to the modules. The master DSP is equipped with 2 × 64 KB fast internal and

126 Digital Signal Processor

127 Program Reset Manager

32 MB external SDRAM¹²⁸ memory. It has access to the FPGAs and the BOC through a register bank connected to one of its external memory interfaces. The setup bus is used for communication with the BOC controller CPLD.

Trigger and event description (BCID, LVL1ID and trigger type) from the ATLAS LVL1 trigger system are provided to the ROD through the TIM. The controller FPGA detects trigger signals, calibration strobes and Pixel module reset commands and expands them to commands in the module format. The commands are sent to the clock and command section of the BOC through a 48-bit wide mask gate, which allows to send the commands to activated modules only. The mask of active modules is set by the master DSP. The controller FPGA configures the components of the readout described below and receives additional serial data from the TIM that describes the ATLAS trigger. Alternatively a TIM FIFO in the controller FPGA or a serial data stream from the master DSP can be used as trigger and data source for data calibration, for tests of the ROD with high trigger rates or in absence of a TIM. Calibrations of modules is performed by the master DSP sending calibration data through the controller FPGA mask gate to the BOC clock and command section.

Each of the eight identical formatter FPGAs can receive up to four 40 Mbit/s module data streams (links) from the BOC receiver section CPLDs. The data streams are routed to the FPGAs through data receivers, which can be used to route data streams to two 48-bit wide and 32 k-word deep diagnostic FIFOs. This FIFOs can be used to trap and inspect module event or calibration data. Additionally the FIFOs can be filled with test event data to test ROD functionalities without connected modules. The formatters perform a serial to parallel (word) format conversion of the data streams. The serial input format, as sent by the MCC, can be seen in Appendix A Figure A-8 and the parallel output format is close to the module format shown on the right side of Appendix A Figure A-41 (slightly different header format). At the output of the formatter FPGAs 2048-word long de-randomizing FIFOs are located to queue events for transmission to the EFB¹²⁹. The formatters indicate to the controller FPGA that all module-event trailers have been received. The controller has a counter for each link, which is incremented for each LVL1 trigger sent to a module and decremented when a trailer has been transmitted to the de-randomizing FIFO for each link. This allows to keep track of the amount of LVL1 triggers present in the modules.

The formatter are additionally used to check and mark data formatting errors. This includes header 1-bit errors, synchronization errors, link readout timeout errors and header trailer limit errors. Header with one of the five bits flipped are accepted, but flagged. Synchronization errors occurs when one of the field separator synchronization bits sent by the MCC is not detected in the data stream. The formatter changes to raw data mode until the next trailer is recognized. This allows to investigate and reconstruct the event information from the raw data. A header, a timeout-word and a trailer is written to the de-randomizing FIFO, if a link does not receive data during a settable timeout. If the programmable header trailer limit occupancy of the de-randomizing FIFO is reached (at about 4/5 of the FIFO size), the formatter stops writing to the FIFO until a trailer is detected. The trailer is written to the FIFO with the header trailer limit error bit set. Until the FIFO occupancy is above the header trailer limit only header and trailers are written to the FIFO. Thus only the

128 Synchronous Dynamic Random Access Memory

129 Event Fragment Builder

event data but not the event synchronization is lost. At another programmable FIFO occupancy limit (about 9/10) a ROD busy signal is sent to the ATLAS LVL1 CTP via the TIM. This busy signal can be used to stop the flow of LVL1 triggers to the TIM, giving the ROD time to process the data stored in the FIFO and preserve the readout synchronization. The formatter stop data transmission as well in case of back pressure from the EFB.

The EFB contains two identical engines, each receiving data of four formatters. The EFB receives from the TIM through the controller FPGA the ATLAS event ID data. After the mode and header information are provided to the EFB by the controller FPGA, the FPGA triggers a data push from the formatter de-randomizing FIFOs to the EFB. There it is possible to increment or decrement the LVL1ID by one for links, which are selected with a dynamic mask provided by the controller FPGA. The EFB checks the BCID and LVL1ID information of the received data against the ATLAS BCID and LVL1ID information. Errors are recorded together with errors flagged by the formatters. A static mask provided by the controller FPGA determines if a formatter is to be processed. Data of enabled formatters are combined to an event fragment and organized in 32-bit words. The EFB frames the event fragment by a 10-word event header and a 6-word event trailer (see Appendix A Figure A-41 left side). The event header contains event ID information and the event trailer mainly summary error flags as well as error and word counts for the entire event fragment. The event fragment is stored in two 46-bit wide 16 k-word link output FIFOs. The link output FIFOs can be loaded with test data like the receiver FIFOs. As soon as both EFB engines provide the word count the event format is pushed to the router. The transmission is stopped when the router applies back pressure to the EFB.

Event data is passed through the router to the S-LINK module with only minor format change to the format shown in Appendix A Figure A-41 and explained in section 7.1. The second aim of the router is to trap event data and pass it to four slave DSPs not interfering with the normal data taking. A filter can be used to trap only special event types and a division factor can be applied to send only a fraction of events to the slave DSPs. Four 1024-word data buffers are used to de-randomize the trapped events and DMA¹³⁰ transfer data frames to the four slave DSPs through individual pipelines.

Each of the four slave DSPs has two 64 KB internal memory blocks and 256 MB external SDRAM memory. The slave DSPs are used for event analysis during data taking and detector calibration. They monitor and histogram event data during data taking and can be used for fitting of histogrammed detector calibration data as well. Operations in the slave DSPs are controlled by the master DSP, which also serves as a way point for slave DSP memory readout from the RCC via the VME bus.

4.6.3 TTC Interface Module

The TIM [POS01] (see Appendix A Figure A-9) interfaces the Pixel readout crate to the ATLAS LVL1 trigger system. The optical ATLAS TTC signal is received by a receiver module (TTCrq) on the TIM. It contains a receiver chip (TTCrx) with an associated PiN diode and a preamplifier to decode the TTC information into electrical signals. The decoded BC clock can be adjusted and is provided to clock-multiplexer

¹³⁰ Direct Memory Access

devices, which automatically switch without a glitch to a backup clock in case of clock failure and can be used to select the clock source. The selected clock is passed via differential PECL¹³¹ drivers to the clock sections of the BOCs. Equal length point-to-point parallel impedance matched tracks are used to provide a synchronous timing marker for all BOCs. Decoded TTC event information and fast commands (see Appendix B Table B-3) are provided to the ROD controller FPGA via a FIFO buffer and are sent with minimum latency. In stand-alone mode the BC clock can be generated by a crystal oscillator on the TIM. TTC event IDs and TTC fast commands can be generated in stand-alone mode on one of the two FPGAs on request of the RCC through the VME bus. A sequencer with 8×32 kbit RAM can be filled with TTC commands and event ID data by the RCC and used to test the readout chain with long trigger sequences and high trigger rates. Another possibility to trigger TTC command generation and provide the BC clock to the readout crate are external ECL¹³² and NIM¹³³ standard input lines on the front plate. The other FPGA is used for generic board functions like VME interface, local bus control and board reset. From the individual ROD busy signals the TIM creates a busy signal, which can be returned to the ATLAS LVL1 CTP to stop the LVL1 trigger flow to the TIM. Wire bond breaks in the detector can be caused by resonances in the Inner Detector magnetic field due to trigger rates close to the mechanic resonant frequency. For physics triggers the probability of fixed frequency triggers is very low, but for test runs and calibration runs fixed triggers can easily occur. A fixed frequency trigger veto module can be used to identify fixed frequency triggers and to assert a crate busy signal to the CTP as well. Intensive resonance tests of the Pixel wirebond connection indicate that this resonance protection is not necessary for Pixel operation but the results have to be verified in the final detector environment.

4.6.4 ROD Crate Controller

The RCC is a commercial single board computer connected to the ATLAS Run Control over the TCP/IP ATLAS network. It is used to configure and control the TIM, BOCs and RODs. Hence the RCC has access to several databases, containing connectivity and calibration information for each TIM, ROD, BOC and Pixel module. The RCC receives commands from the Run Control, reads histograms from the slave DSP memories and provide them to a histogram service, handles errors and messages from the readout crate components and manages their status. For calibration runs data taking software can be executed on the RCC directly.

4.7 Readout Subsystem

The event fragments (ROD fragments) are optically transferred from the BOCs over the optical S-LINK interconnection, to the ROS. The readout data flow through the ROS is shown in Figure 4-18. The ROS is a commercial high performance server PC

¹³¹ Positive Emitter Coupled Logic

¹³² Emitter Coupled Logic

¹³³ Nuclear Instrumentation Module

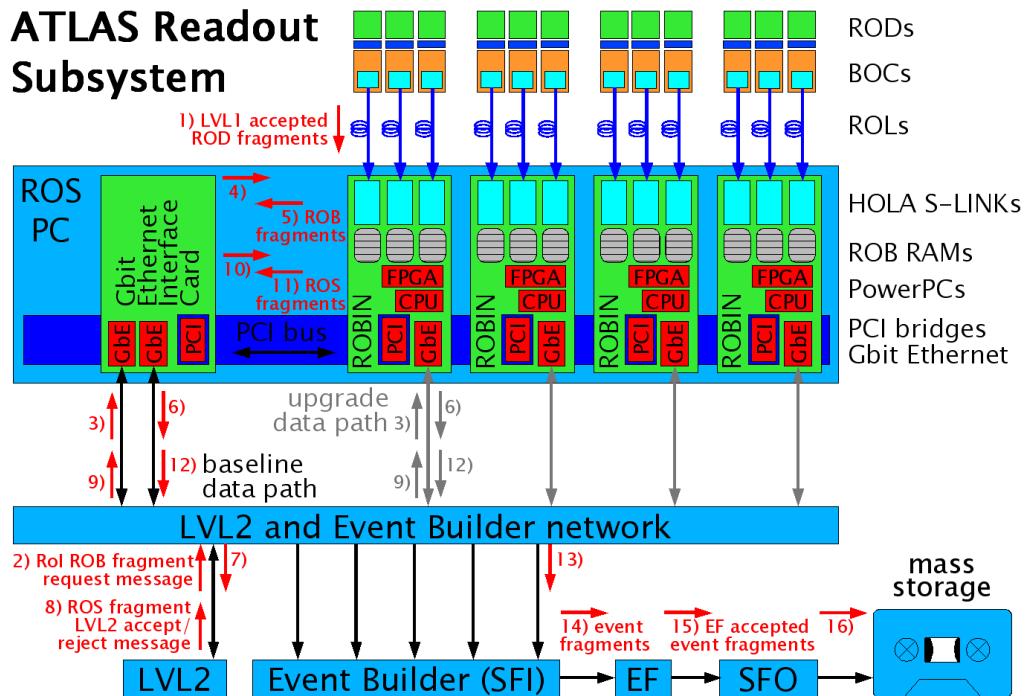


Figure 4-18 The ATLAS readout subsystem PC with its connections to the readout crate and the baseline and upgrade option data path

with four PCI buses. It contains four ROBIN¹³⁴ PCI cards [KIE05],[KUG05] (see Appendix A Figure A-10). Each ROBIN has three HOLA 2 Gbit/s readout links (ROL) which are controlled by a FPGA. 'Beginning'- and 'End of Fragment' markers used for ROL transmission of ROD fragments are deleted (see Appendix A Figure A-41). S-LINK status words in the lower 16 bits of the markers are added to the first status element of the ROB fragment. The FPGA writes the ROD fragments, which may arrive with a maximum rate of 100 kHz, into one of the ROL corresponding independent 64 MB SDRAM buffer memories (ROB). A paged memory layout with a PowerPC processor with a free page FIFO and a used paged FIFO in the FPGA is used. ROD fragments are identified by their 32-bit extended BCID. For fast LVL1ID searches a hash-key is created from the LVL1ID and all pages with the same key are stored in a linked list in 128 MB DDR¹³⁵ SDRAM CPU memory.

The LVL1 trigger provides RoI information to the LVL2 trigger. Through this limitation, the data fraction, which the LVL2 trigger has to evaluate to make its decision, can be reduced to about 2% of the ROB data, but can be up to 7% of a ROL. Incoming RoI ROB data fragment requests from the LVL2 trigger are processed by the ROS PC. The request messages are distributed to the ROBINs through the PCI buses to the ROBIN CPU, which collects the required event data. The fragments are sent through the PCI bus and Gbit Ethernet to the LVL2 trigger farm. As soon as a LVL2 decision has been taken a LVL2 reject or accept message is sent for the event to all ROS PCs. The former initiates the deletion of all event corresponding ROB fragments, whereas the latter starts the ROS event building of them. The ROS collects

134 Read-Out Buffer INput

135 Double Data Rate

through the PCI buses all corresponding ROB fragments and adds a ROS header (see section 7.1). The event is assigned by the DFM¹³⁶ to one of the about 50 SFI nodes, which collects all ROS fragments. The SFI node groups all ROS fragments belonging to one sub-detector into a sub-detector fragment with a dedicated header. All sub-detector fragments are combined to an event fragment and provided to the EF, where the last online decision about keeping or dropping the event is made. Events passing the EF are written to the ATLAS Data Storage and can be used for physics analysis. More details about the HLT with the EF and LVL2 trigger are presented in section 3.2.5.

4.8 Pixel Detector Services

In addition to the data path described in the above sections a large number of other components are necessary to supply the detector and the readout devices with the necessary voltages. The detector environment, the detector itself as well as power supply devices have to be monitored carefully to guarantee the safety of the detector under all possible operation conditions. These two aims are taken care by the Pixel Detector services [OLC04c]. For an overview of the Pixel services see Figure 4-19.

Due to the fact that the Pixel Detector is the innermost ATLAS sub-detector and that it is integrated into the experiment as one of the last components, the routing of its

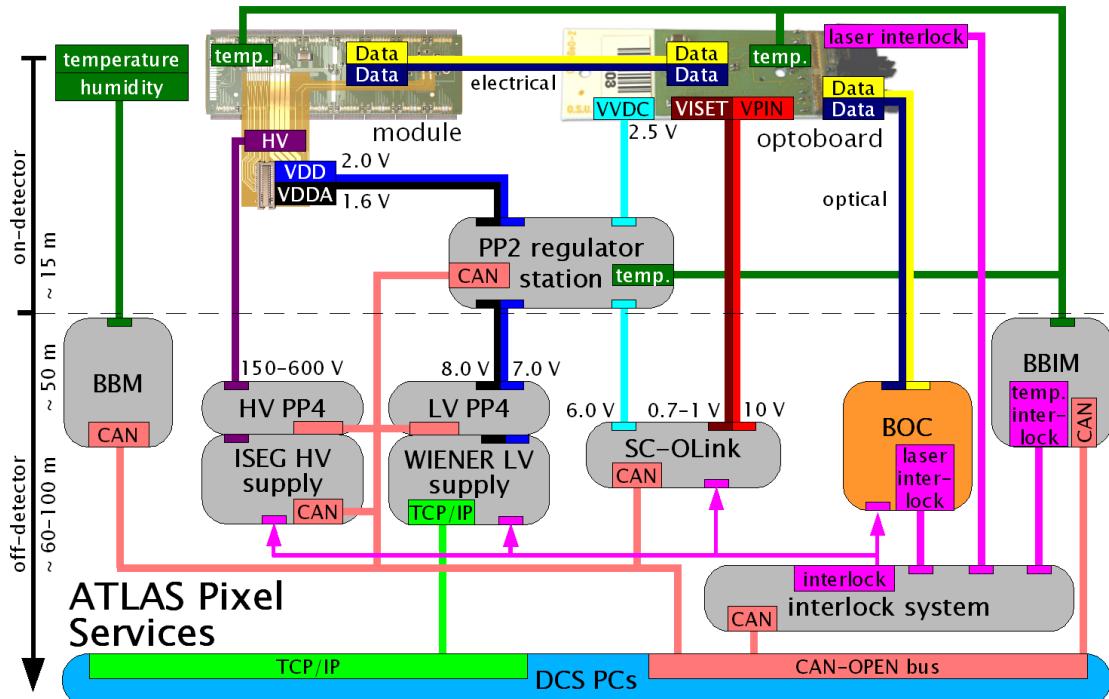


Figure 4-19 Overview of the Pixel Detector services with data path, power supplies and interlock system

services is highly constrained by the geometry of other detectors and of the available service gaps between them. The services have to pass the gas sealed thermal barrier Faraday cage of the Pixel Detector (see section 4.1) as well. Therefore at several points in the services break points are implemented. The different break points of the Pixel services and the optical data path, as well as their naming are shown in Figure 4-20. At this break points the service cables are terminated and are connected to patch panels (PP) with increasing numbering starting from the detector. Cables connected to the PPs are named after the lower of the two PPs they are connected to with the number increased by one. For example the cables from the modules to the PP0s are called Type0. They are described in section 4.4. Analogously the cables from PP0s to PP1s are called Type1. They are integrated together with PP0 and PP1 in the Pixel Package and are described in detail in section 4.1. All services, optical fibers and cooling pipes break at PP1 since the Type2 cables, fibers and tubes are installed in the ATLAS experiment before the Pixel Package is integrated. This also allows to disconnect the Pixel Package for maintenance later on. Electrical services [CIT04] are connected to PP1 by radiation hard Type2 cables with LEMO-F connectors. A star-topology grounding scheme with the common ground point located at PP1 is used.

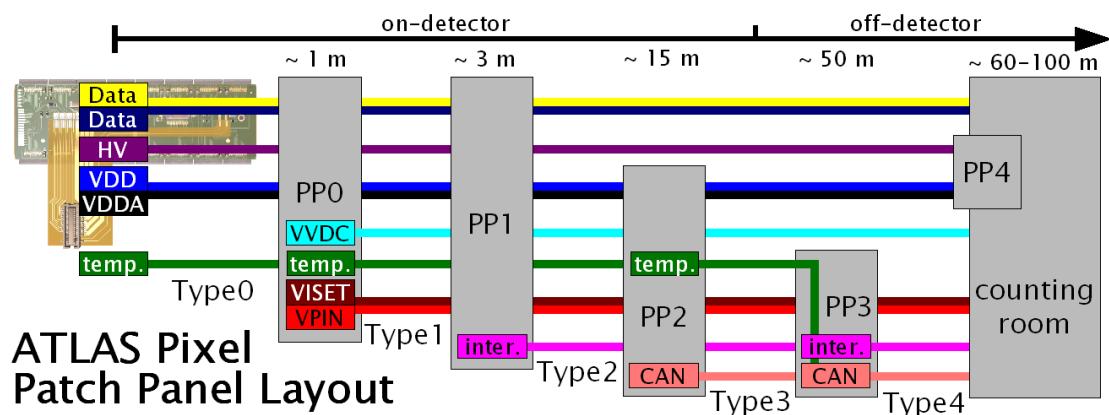


Figure 4-20 Layout of the Pixel service break points and the different cables between them

LV, NTC/Opto and environmental sensor services break at PP2 [CIT03] about 15 m away from the Pixel Detector. PP2 boxes are located at different points in the experiment between the innermost and middle muon spectrometer layer. In total 26 LV, 24 NTC/Opto and eight environmental boxes are distributed to six positions. The NTC/Opto and environmental boxes provide passive connections of the radiation hard Type2 cables to the radiation tolerant Type3 cables. The LV PP2 regulator boxes contain voltage regulation boards for the high current supply voltage services VDD, VDDA and VVDC. Voltage regulation is necessary at this point for high current supply voltages to compensate the voltage drop over Type0, Type1 and Type2 cables with remote sensing. The PP2 regulators are controlled and monitored via CAN¹³⁷-bus. More details about the PP2 voltage regulation are given in section 4.8.1. The HV sensor bias cable and optical fibers do not have a break point at PP2, but the fibers are spliced close to PP2 (see section 4.5).

Type3 NTC/Opto, Module-NTC, PP2-NTC and environmental cables are connected to PP3 crates [KER05a] at six positions on the service platforms around the ATLAS experiment. The PP3 crates for the optoboard services (Opto PP3) are only passive and extract the Opto-NTC temperature signal lines from the NTC/Opto Type3 cables. The other opto services (V_{Iset} , V_{PIN} and DORIC reset lines) are routed to the counting room in a common Type4 cable. The Opto-NTC, Module-NTC and PP2-NTC cables are connected at PP3 to BBIM¹³⁸s, which provide the digitization of the NTC thermistor signals. The readout of the digitized temperatures is provided via CAN-bus. Additionally the BBIMs provide digital interlock signals if the measured temperatures exceed or fall below fixed thresholds. Environmental-NTC cables are connected to BBM¹³⁹s, which have the same temperature digitization components as the BBIMs, but do not provide interlock functionality. The BBIM and BBM are described in the section 4.8.2. In total 14 BBIMs, four BBMs and 16 Opto PP3 crates are needed for the Pixel Detector. HV cables, optical fibers and the high current LV service cables do not have a break point at PP3.

The optical fibers are connected in the counting room to BOCs as described in section 4.6.1. HV Type2 and LV Type3 cables are connected in the counting room to PP4s. The PP4s provide voltage distribution for the two module low voltages VDD and VDDA as well as for the module HV bias voltage. They support the measurement of the individual module currents and sensor leakage currents. LV PP4s [KER07a] are powered by commercial WIENER¹⁴⁰ power supplies and distribute one VDD or VDDA power supply channel to six or seven channels, supplying a module each. The HV PP4s distribute each commercial ISEG¹⁴¹ power supply channel to six or seven individual sensor bias channels. Due to the current limitation of the ISEG channel of 4 mA and increasing sensor leakage currents with irradiation the modularity will be reduced with increasing operation time of the detector. The HV PP4 provides the possibility to change the modularity dynamically. The Type3 VVDC as well as the Type4 V_{Iset}/V_{PIN} cables are connected to SC-OLink¹⁴² power supplies. Interlock cables for module, optoboard and PP2 temperature interlocks are connected to Logic Units, which combine the interlocks and switch off the corresponding power supplies. The power supply and the interlock system are described in the following two sections.

4.8.1 Power Supply System

Each of the 1744 Pixel modules needs to be supplied with +2.0 V VDD for the MCC and the FEs and +1.6 V VDDA for the FEs. VDD and VDDA have separate return lines DGND and AGND. Typical VDD currents for unconfigured modules are ~ 320 mA, ~ 150 mA for unconfigured modules without clock, ~ 250 mA for unconfigured modules with 20 MHz clock and up to ~ 900 mA for configured modules. The VDDA currents are typically ~ 90 mA if the module is unconfigured and up to ~ 1300 mA for configured modules. A first grounding reference point is the connection of the digital and analogue supply voltage grounds on each Pixel module

¹³⁸ Building Block Interlock and Monitoring

¹³⁹ Building Block Monitoring

¹⁴⁰ WIENER Plein und Baus GmbH, Burscheid, Germany » www.wiener-d.com

¹⁴¹ ISEG Spezialelektronik GmbH, Radeberg, Germany » www.iseg-hv.de

¹⁴² Supply and Control for Optical Link

flex hybrid. The HV bias voltage for the sensor depletion is required as well. Before irradiation the sensors draw well below 1 μA at 150 V. To avoid potential differences between the sensor and the FEs, the return line of the sensor bias voltage is connected via a 10 $\text{k}\Omega$ resistor to VDDA. Thus both sides of the sensor-FE gap are on the same potential. The optoboard (see section 4.4) needs to be supplied with +2.5 V VVDC for the powering of the DORIC and VDC chips as well as for the VCSEL array. Typical current consumption on the VVDC line is around 240 mA. All module DGNDs are connected on the PP0s to the corresponding VVDC ground. This provides a reference for the LVDS signals between the modules and the optoboard. The -10V V_{PiN} is required as depletion voltage for the PiN array and has a receiving laser power dependent current of $\sim 1\text{-}3$ mA for seven lasers on. The voltage $V_{\text{Iset}} \sim 0.8$ V provides the laser output power control current I_{set} , multiplied by a factor of ten, to the VDC. Typical V_{Iset} currents are about 1 mA. A reset line is used to reset the delay-lock-loop of the DORIC. It is kept on +2.5 V and short 0 V pulses are used to reset the DORIC. The power supply system [KER05b] needs to provide and control all these voltages. An overview of the power supply system is shown in Figure 4-21. The VDD/VDDA ground on the PP0s is connected at PP1 to the Pixel Detector ground, formed by the PP1 endplates, the aluminum EMI shields of the PST and the beampipe. All power supply channels are floating so that the grounding scheme follows a star topology. The Pixel Detector ground is connected at a single point (on the A side of the detector) to the Inner Detector ground.

For the high current supply lines VDD, VDDA and VVDC the about 100 m distance to the power supplies in the counting room would lead to intolerable high voltage drops and thus high power dissipation in the service cables. A voltage drop compensation at the power supplies over this long distance would be risky, since a sudden current decrease, faster than the regulator reaction time, could lead to voltages above the 0.25 μm DSM CMOS breakdown voltage of 4 V. Therefore power supply regulator stations are used closer to the detector at PP2. The voltage drop over the remaining ~ 15 m supply cable is still significant and is compensated by remote sensing. Two remote sense lines per module high current supply voltage are connected to the positive line and the return line at the Type0 connector on the module pigtail for barrel modules. On disk modules the sense lines are soldered together with the power lines to the module flex hybrid. For the optoboard high current supply VVDC the sense lines are connected to the supply and return line on the optoboard. The voltage regulation is taken care by STMicroelectronics¹⁴³ LHC4913 [STM02] radiation hardened voltage regulators, which have been developed in collaboration with the CERN RD49 collaboration [BOE00]. They feature remote sensing operation, adjustable current limitation, inhibit capability, output short circuit monitoring as well as overtemperature and overcurrent protection. Their radiation hardness has been tested up to 2 Mrad with gammas and $1\cdot 10^{14} \text{n}_{\text{MeV}}/\text{cm}^2$ neutrons [JAR04]. A simplified schematic of the voltage regulation loop with current compensation over two low resistance power lines and two high resistance sense lines is shown in Appendix A Figure A-11. A voltage divider with a 100-step trimmer potentiometer (R_{Trim}) is used to set the output voltage, which is corrected depending on the current consumption. Since the sense return line is current carrying a current compensation circuit is used to compensate the voltage drop over the sense return line. A resistor is added between the power return and the sense return line. Thus the voltage drop in the power wire is

¹⁴³ STMicroelectronics, Geneva, Switzerland » www.st.com

used to generate a current flowing through the ground sense wire opposed to the base current. To avoid overvoltage in case of a broken sense line the potential difference between the power line and the sense line is limited by a guard diode, which is implemented using a yellow LED¹⁴⁴.

The voltage regulators for a half-stave or disk sector are mounted on a regulator PCB. For each VDD and VDDA voltage a single regulator is used, resulting in 14 regulators. For the VVDC voltage two regulators are used in parallel to provide redundancy, since a failure in this supply voltage would cause the loss of the entire half-stave or disk sector. Thus each regulator board provides 15 galvanic isolated channels. The digital trimmer potentiometers are mounted on a so-called daughter board, which is attached to the regulator board. A trimmer is used for each VDD or VDDA regulator and the two VVDC regulators are adjusted by a single trimmer. Supply voltage for the trimmers is generated from the corresponding input voltage, thus the trimmers can only be set if a channel is switched on. The output voltages are measured as potential differences between the two corresponding sense lines and the output currents are measured as the potential difference between the power line and the sense line with an ADC mounted on the daughter board. With calibration and measured cable resistances accuracies of 20 mV and 100 mA have been reached.

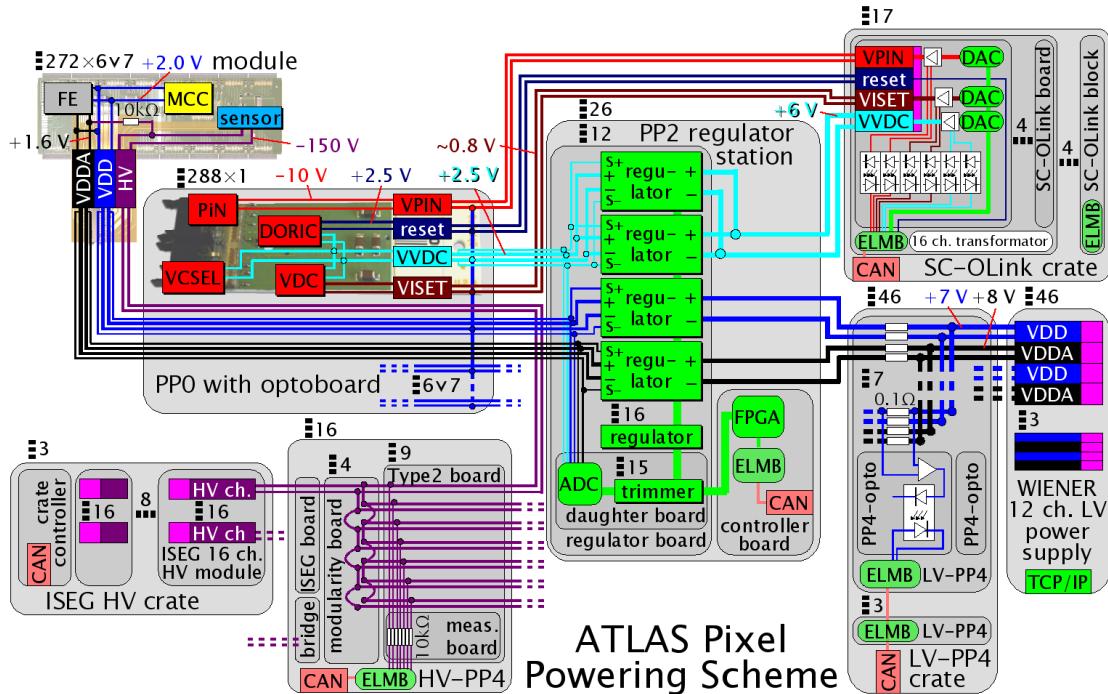


Figure 4-21 Schematic view of the Pixel powering

Up to 12 regulator boards can be controlled and monitored by one PCB referenced as controller board, which has separate external supply voltages. The controller board uses a FPGA for the setting of the trimmers, readout of the ADCs and disabling the output of the regulators. Two independent signals can be used to switch off the voltage output of the regulators. Only if none of them is active a regulator channel is switched on. The INHIBIT signal can be applied by the FPGA to individual regulator channels,

whereas the KILL signal affects all regulators of a regulator board. The individual INHIBIT and global KILL signals are latched on the daughter boards. To clock the latches the signal to change the setting of the trimmers is used. Therefore the detector supply voltages are not affected in case of a power cut of the controller board supply voltages. If input voltages are switched off or have a power cut the regulators receive an INHIBIT signal and the daughter board latches store the INHIBIT signal even if the input power is switched on again. The output voltage can be switched on again by issuing the trimmer set signal to clock the latches. For communication of the FPGA with the DCS¹⁴⁵ (see section 4.9) via CAN-bus an ELMB¹⁴⁶ on the controller board is used.

The 12 regulator boards, a controller board, an output board with Type2 connectors, an input board with Type3 connectors and an aluminum crate form a regulator station. In total 26 stations are necessary for the power supply of the Pixel Detector. A regulator station has a power dissipation of up to 600 W. Therefore active cooling is necessary. The regulators of a regulator board are thermally coupled with conducting paste to an aluminum plate, which has thermal contact to the regulator station aluminum frame. In the top and bottom plate of the frame copper cooling loops are incorporated, which are connected to a monophase room-temperature C_6F_{14} cooling system. To minimize the power dissipation in the regulator stations and the Type3 supply cables the regulator input voltages are set as low as possible.

The 7 V VDD and 8 V VDDA regulator input voltages are provided by two neighbored channels of the 12-channel WIENER power supplies. The galvanically isolated channels can provide 0-12 V with up to 15 A. They have individual interlocks, remote sensing (not used), temperature controls, voltage and current limit settings as well as output voltage and current measurements. Two WIENER channels provide the module LVs for one half-stave or disk sector, thus six half-stave or sectors can be supplied by one WIENER and 46 power supplies are required for the entire Pixel Detector. The power supplies are controlled and monitored by the DCS via TCP/IP. The 12 channels of a WIENER are connected with short pigtails to a LV-PP4 crate [KER07a]. Each LV-PP4 crate consists of three identical LV-PP4 blocks with a backpanel board each, which carries the pigtails and Type3 connectors, two PP4-opto cards, a WUPP-ELMB board and an PP4-inter card for routing between the opto cards and the ELMB board. Each LV-PP4 block provides a fanout for four WIENER channels to 4×7 channels connected to two PP2 regulator boards via Type3 cables. The current measurement of the individual output and return lines is performed via a voltage drop on a 0.1Ω resistor. Op-Amps¹⁴⁷ and linear optical couplers for isolation of the measurement circuits are mounted on two PP4-opto cards. The Op-Amps and opto couplers are supplied by separate power supplies on the HV-PP4 crate frontpanel. An ELMB is used for the measurement of the output and return currents and transmitted via CAN-bus to the DCS.

The +6 V VVDC PP2 regulator input voltage, the low current optoboard supplies V_{PiN} and V_{Isset} as well as the DORIC reset signal are provided by SC-OLink power supplies [KER05c] in the counting room. Since the drawn current on the V_{PiN} , V_{Isset} and the reset line are very low, the voltage drop on the cables to the optobards are negligible

¹⁴⁵ Detector Control System

¹⁴⁶ Embedded Local Monitor Board

¹⁴⁷ Operational-Amplifier

and their output voltage is set at the power supplies and no remote sensing is necessary. A SC-OLink crate consists of four identical blocks with four SC-OLink boards each. In total 17 crates are necessary for all Pixel Detector optoboard. Each board provides four galvanically isolated supply voltages for one optoboard. The power channels have their own opto coupler isolated 12-bit DAC, which are daisy chain controlled by an ELMB on a WUPP-ELMB board per SC-OLink. The DACs are supplied by isolated transformer coils of a 16 channel 64 VA ground shielded toroidal transformer providing all supply voltages for four SC-OLink boards. With the three DACs the output voltages are settable over the full output range between 0 V and 20 V / 10 V / 5 V for V_{PiN} / VVDC / V_{Iset} with hardware current limits of 20 mA / 800 mA / 20 mA. If the current limit is reached the channel behaves as a current source and returns to normal operation as soon as the current decreases below the limit. The output voltages and currents are measured with the 64 ELMB ADC channels, which are galvanically separated from the outputs with linear opto couplers. The DORIC reset line provides fixed 2.5 V. Controlled by a digital output line of the ELMB a 10 μ s long 0 V pulse is generated to reset the DORIC on the optoboard. A simultaneous interlock uses relays to cut the power to all DACs of a SC-OLink board. Due to a power-on-reset feature of the DACs, the output voltages stay off after an interlock or power cut until the DACs are set again by the DCS through the ELMB.

The bias voltage for the module sensors are generated by commercial 16-channel 700 V 4 mA ISEG HV power supply modules. Eight modules are housed in a crate together with an ISEG crate controller with CAN-bus interface for DCS communication. Altogether three ISEG crates are used for all Pixel Detector HV channels. The HV channels provide individual interlocks, individual output voltage and current monitoring, individual voltage and current limits. If the current limit is reached the channel switches to current source mode or switches off. The ramp speed can be set per half-module. Typically \sim 15 V/s are used to limit the electric field gradients in the sensors. Channels are galvanically isolated up to ground potential differences of 20 V.

HV-PP4s [MET07] are used to fan out the ISEG HV channels to modularities six and seven for the first years of operation. Later on, when the sensor leakage currents exceed the 4 mA that can be provided by a single ISEG HV channel, a modularity two will be used. A HV Type5 cable with 16 HV channels arrives from an ISEG module on an ISEG board in the HV-PP4. A second Type5 cable is connected to a bridge board, which only receives two of the HV channels and outputs the remaining channels to the neighboring HV-PP4. Thus a total of 18 input channels exist per HV-PP4. On four modularity boards the 18 HV channels are fanned out with modularity six or seven. The modularity can be changed to two by replacing of modularity boards with ISEG boards, resulting in 63 HV input channels from four ISEG modules. The voltages are distributed to the modules throughout nine Type2 boards with a HV Type2 cable connected each. Attached to the Type2 boards, measurement boards measure with $10\text{ k}\Omega$ resistors the individual output currents on the return lines and route them to an ELMB for digitization and readout through DCS.

4.8.2 Interlock Matrix

A so-called I-Matrix [KER04a],[KER07b] is used to switch off interlock controlled devices in case of over heat of detector or supply components, failure of the cooling or N₂ system, risky radiation levels detected by the BCM, smoke in the PP2 region detected by the sniffer system or risk of laser exposure to humans detected by laser interlock switches. This dedicated pure hardware interlock logic is aimed to switch off only devices directly involved in the interlock situation to keep as many parts of the detector in operation as possible. Although its functionality is independent of the DCS software it can be monitored and tested by DCS. To make sure that disconnected cables and local power cuts cause interlocks the entire interlock circuitry uses a negative logic with the interlock inactive at 3.3 V and pull down resistors at all interlock inputs. A schematic view of the interlock system is shown in Figure 4-22.

The front-end part of the interlock system is integrated in the BBIM crate at PP3. A BBIM crate houses four individual BBIMs. Each BBIM consists of one ELMB [ELM02] and four I-box¹⁴⁸s [KER04b]. A BBIM front panel board is used to route 14 incoming NTC lines per I-box on two Type3 cables with 15-pin sub-D connectors to the I-boxes and the ELMB. The analogue supply voltage for the I-boxes is connected through the front panel board as well. A WUPP-ELMB board connects the NTC lines via 1 kΩ and 1 nF to the 64 analogue input channels of the ELMB, which are multiplexed to a 16-bit (and seven bits for dynamic range from 25 mV to 5 V and bipolar/unipolar mode) ADC with programmable gain amplifier. The ELMB is used to monitor a reference voltage, which is created by the I-boxes, as a voltage drop across a 10 Ω series resistor. The reference voltage is applied to the module, optoboard and PP2 high precision 10 kΩ NTCs and the voltages across the individual NTCs are measured by the ELMB. For the Pixel system the ADC is used in the unipolar 5 V measurement range with 15 Hz multiplexing, which allows to measure all 64 input channels in ~6.5 seconds with a precision of ±0.2 mV. The ELMB sends the measured voltages via CAN-bus to the DCS where the individual NTC resistances and thus the temperatures can be calculated from the voltage drop across the NTCs. In parallel an I-box can compare up to 16 NTC input signals (only 14 used) to different thresholds, which can be set by a small attached shooting-point PCB. Four Op-Amps per channel are used as two discriminators and two NOR-gates create the interlock signals T-high and T-low. If the temperature is between the thresholds both signals are in interlock inactive state (3.3 V). If the temperature is too high or in case of a shortcut on the NTC line the T-high signal is in interlock active state (0 V), if the temperature is too low the T-low signal is in interlock active state. In case of a broken NTC sensor or power failure both interlock signals are in interlock active state. A passive back panel board is the adapter for the four BBIM I-boxes with 2 × 14 interlock signals each to Type4 interlock cables with 15-pin sub-D connectors. The Type4 interlock cables are connected to Logic Units in the counting room.

A Logic Unit consists of three identical Tmod blocks and a 'FPGA' block. Tmods consist of a front panel board, an ELMB board and two latch boards. Each Tmod has four 25-pin sub-D connectors for the Tmod high and low interlock signal inputs from the BBIM. They can handle therefore up to four half-staves or disk sectors. The input

ATLAS Pixel Interlock System

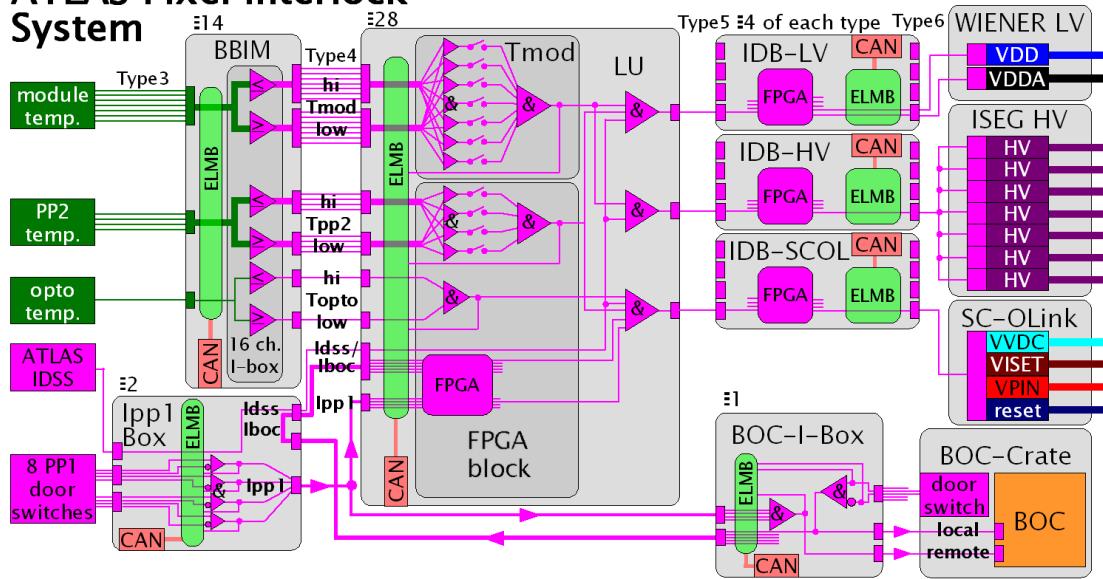


Figure 4-22 Schematic view of the Pixel interlock system

module temperature interlock signals are separately latched and can be monitored with the ELMB. A logic AND is created for all high and low interlock signals of each module of a sector or half-stave and their consideration in the AND can be independently selected via a dip switch on the back panel board. The result of the logic AND is monitored via the ELMB as well. Tmod high and low interlocks cause an interlock of the corresponding HV and LV interlock output channels. One 25-pin sub-D connector is used for the 12 HV interlock signals and two connectors for the 24 LV interlock signals. The 'FPGA' block consists of a Tpp2 front panel-board, two latch boards, an ELMB and a FPGA board. It handles all interlock inputs which are not related to module temperatures. It has two 25-pin sub-D input connectors for the Topto and one each for the Tpp2 high and for low temperature interlock signal inputs from the BBIM. The high and low interlock signals of the 12 Optoboard are monitored and the corresponding low and high signals are combined. Topto interlock signals cause an interlock on the corresponding SC-OLink interlock output channels which are connected to a 25-pin sub-D connector. To guarantee that SC-OLink and HV supply channels stay off after an interlock is gone, the interlock signals need to last at least 1 second. Thus the interlock signals are stretched to about 2 seconds. All seven Tpp2 interlock input signals are monitored and four of them are combined to give an interlock to all 24 LV, all 12 SC-OLink and all 12 HV interlock output channels. With a dip switch on the back panel board the combination of Tpp2 channels can be selected. In addition to the temperature interlocks the Logic Unit uses interlock inputs from the Ipp1 Box¹⁴⁹ and the BOC-I-Box¹⁵⁰. Two Idss interlock signals (one per detector side) are provided by the ATLAS Detector Safty System (DSS). For the Pixel system DSS interlocks are generated in case of failure of the cooling or N₂ system, risky radiation levels or smoke in the PP2 region and routed through the Ipp1 Box to the Logic Units. The Ipp1 and Iboc interlock signals indicate

149 Interlock patch panel 1 Box

150 BOC-Interlock-Box

a risk of laser exposure to humans detected by laser interlock switches at PP1 and at the BOC rack doors (a rack door switch interlocks both BOC crates of a rack) and are provided by the Ipp1 Box and the BOC-I-Box to the Logic Units. One 25-pin sub-D input connector is used for the four Ipp1 interlock signals from the Ipp1 Box and one for the Idss and the five Iboc interlocks, which come from the Ipp1 Box as well. The four ELMB monitored Ipp1 interlocks are causing an interlock on all SC-OLink interlock output channels whereas the monitored Idss interlock creates an interlock on all LV, SC-OLink and HV interlock output channels. If one of the five Iboc interlock signals is in interlock state only interlocks for SC-OLinks belonging to a specific Iboc interlock block are generated. Iboc interlock blocks represent a BOC crate each. A FPGA is used to determine which SC-OLink needs to be interlocked for which Iboc or Ipp1 interlock signal. It is equipped with all possible interlock schemes and the necessary program can be selected with a dip switch at the back panel board.

Two Ipp1 Boxes, one for each detector side, are used as interface from the ATLAS Detector Safety System and the PP1 laser interlock switches to the interlock system. They consist of a front and back panel board, a PP1 logic board, a WUPP-ELMB board and a latch board. Each Ipp1 Box is connected by two Type2 PP1 interlock cables with 15-pin sub-D connectors to the eight PP1 laser interlock switches on the corresponding detector side. Two switches per PP1 quarter, one normally open and one normally closed, are used and the Ipp1 box combines the two signals to a single interlock not active signal when both switches are in their not normal state. The resulting four Ipp1 interlocks are distributed to the Logic Units and the BOC-I-Box to generate the interlock acting on the BOCs. Since the connection scheme of the PP1 quarters and of the readout crates follow completely different rules, thus a interlock of one PP1 quarter would require an interlock of up to seven of the nine readout crates, it was decided that a interlock of any PP1 causes a interlock of all BOC crates and all SC-OLinks. The Iboc cable coming from the BOC-I-Box is going through the Ipp1 Box, which adds the Idss interlock signal to the cable going to the Logic Units. All Ipp1 interlock signals are latched by a latch board and can be monitored by an ELMB.

The BOC-I-Box consists of a front and a back panel board, a latch board and an ELMB board. It is used to transfer the door switch status of the five BOC racks to interlock signals. The five rack switches are connected to the BOC-I-Box with five individual 9-pin sub-D connectors. The same 'normally open - normally closed' double switches as for the PP1s are used. Nine 9-pin sub-D output connectors serve to route this local interlock signals directly back to the BOCs of the corresponding crate to block the laser output of the BOC TX-Plugins. Additionally the five Iboc interlocks are routed via two 25-pin sub-D connectors to the Ipp1 Box of each detector side to cause an interlock of the corresponding SC-Olinks in the Logic Units. In the opposite direction Ipp1 signals are coming from the two Ipp1 boxes via two 15-pin sub-D connectors, each containing four Ipp1 interlocks and one Idss interlock for one of the detector sides. These interlocks are combined with a logical AND and the resulting remote interlock is routed to all BOCs through the same output connectors used for the local interlocks. As for the other interlock devices the interlock signals are latched and are monitored via the ELMB.

The Logic Unit outputs are connected by Type5 cables to three different kind of IDB¹⁵¹s, which distribute the interlock signals to the WIENER LV, ISEG HV and the

SC-OLink power supplies. The IDBs generate specific interlock signals depending on the power supply needs which are routed to the power supplies through Type6 cables. All IDBs consist of a front panel with seven 25-pin sub-D input connectors, a FPGA board, a latch board to latch all input signals, an ELMB board to monitor the interlock signals and a back panel with different amount and type of output connectors. The first five input connectors have 12 interlock input channels, matching a full Logic Unit, whereas the two last input connectors have only six interlock channels, corresponding to a half Logic Unit. The FPGAs contains all possible interlock programs and the specific program can be selected via a hex switch on the FPGA board. IDB-LVs have six 25-pin sub-D output connectors and thus it can be connected up to six WIENER LV power supplies. Ten 9-pin sub-D output connectors, containing interlock signals for eight ISEG HV supply half-modules (8 HV channel modules) each, exist on the IDB-HVs. Therefore up to five ISEG HV crates with 40 ISEG modules could be connected, but only interlock input signals for up to 36 ISEG modules can be connected at the input side. IDB-SCOLs have 20 9-pin sub-D connectors with four interlock signals each. Thus 20 SC-OLink power supplies could be connected, nevertheless only inputs for 18 exist.

For the interlock system of the entire detector 14 BBIMs, 28 Logic Units, four of each IDB type, two Ipp1 boxes and one BOC-I-Box is required.

4.9 Detector Control System

The control and monitoring of the power supply and interlock components as well as the monitoring of the detector voltages, currents and environmental sensors are the task of the DCS. The DCS allows an automated and flexible control, monitoring and archiving of the about 50,000 parameters describing the state of the detector, checks that the parameters are in expected ranges and informs the operator in case of unexpected parameter values. It mainly uses CAN-bus connected ELMBs for the communication with the hardware components. The DCS software uses the commercial PVSS¹⁵² II framework, which provides object oriented data management, scalability and redundancy by supporting distributed system operation and a C++ related scripting language with GUI¹⁵³ support. For the software-hardware communication open standard OPC¹⁵⁴ server drivers are used, which provide the universal communication interfaces for the hardware device integration.

The Pixel DCS project is structured in different modules which serve different purposes. The structure of the Pixel Detector DCS is shown in Figure 4-23. The FIT¹⁵⁵ provides a functional structuring of the service components. It is used to integrate, represent and group parameters of hardware devices. The integration part of the FIT allows the integration of devices and the specification of their communication parameters like device type, serial number, communication bus and device address. It takes care of the creation of all necessary data elements representing the parameters of

¹⁵² Prozess Visualisierungs- und Steuerungs-System, ETM professional control GmbH, Eisenstadt, Austria » www.etm.at

¹⁵³ Graphical User Interface

¹⁵⁴ Object Linking and Embedding for Process Control

¹⁵⁵ Front End Integration Tool

the hardware device, the starting of necessary software modules and is responsible for the management of the hardware components. The control part of the FIT provides for each device a control panel which views and allows to set all parameters belonging to this device. Control buttons in the panels for example allow to switch specific or groups of power supply channels or to reset the device. Control panels of different devices are grouped following their device type and the communication architecture. A watchdog service periodically checks with cyclically changed parameters and comparison of timestamps, if all integrated hardware components are accessible and informs the user in case of lost communication to a device.

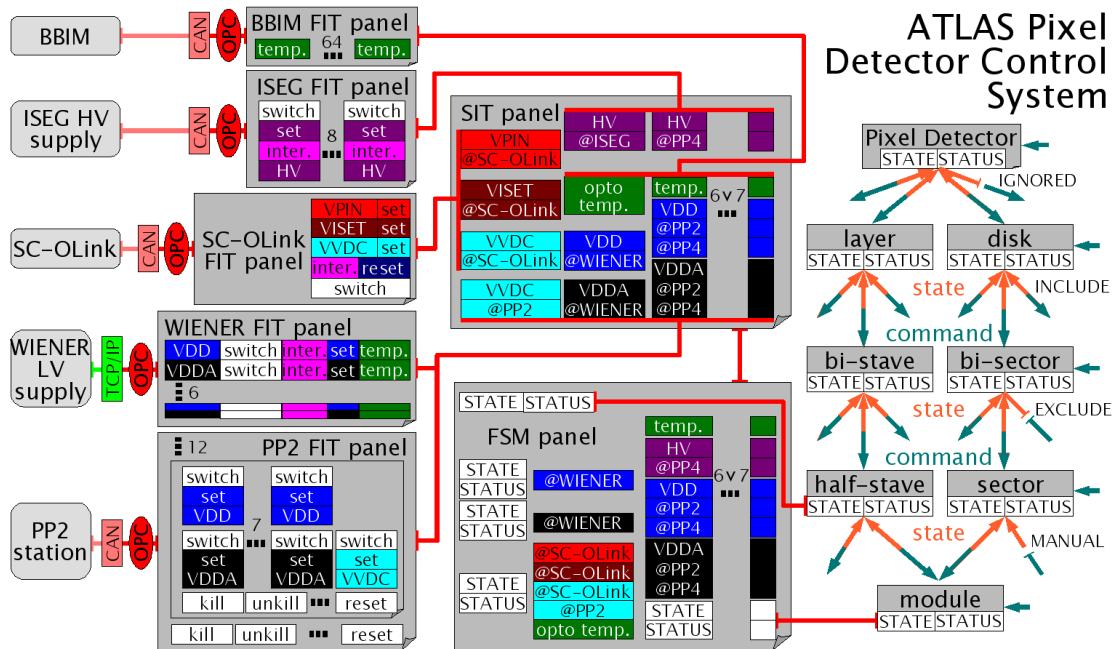


Figure 4-23 Structural view of the Pixel DCS with FIT, SIT and FSM

The SIT¹⁵⁶ is detector geographically structured. It assigns parameters and control buttons of different FIT control panels according to the detector geographical structure and combines them in a panel representing a half-stave or disk sector. For example all power supply channels with their voltages and current consumptions of the modules of a disk-sector and their belonging temperature are shown in one panel and can be controlled from this panel. Navigation panels show the Pixel Detector geometry and allow to hierarchically navigate to a specific half-stave or disk sector. The integration part of the SIT flexibly allows to assign the FIT devices and channels to a geographical position via a GUI panel or via xml configuration files.

To guarantee a safe operation of the Pixel Detector the operator needs to have an overview of the detector and services status at all times. Therefore a FSM¹⁵⁷ [SCH07] is used to summarize and rate the status of the detector. It is required that the operator can easily and flexibly change the state of detector or parts of it. Therefore the FSM is hierarchically structured with the possibility of partitioning.

156 System Integration Tool

157 Finite State Machine

In the FSM the hierarchical structure for the barrel part of the detector is organized in 'barrel module' ∈ 'half-stave' ∈ 'bi-stave' ∈ 'layer' ∈ 'Pixel Detector' and for the disk part in 'disk module' ∈ 'sector' ∈ 'bi-sector' ∈ 'disk' ∈ 'Pixel Detector'. Each of this hierarchical elements is described by a finite number of states and transitions between them, which are triggered by commands. Commands can be applied at each hierarchy level and are distributed downwards in the hierarchy, whereas the state of an element is propagated upwards in the hierarchy. On the 'half-stave', 'sector' and 'module' level commands perform power supply switches in a defined sequence. This allows to switch-on, switch-off or reset on all levels from the entire detector to one module with a single action. The partitioning of the FSM in different not-interfering partitions with individual operators is possible by setting each hierarchical element in one of four partition modes. The 'INCLUDED' mode is the default and the command distribution and state propagation happens as described above. In the 'EXCLUDED' mode a hierarchical element neither accepts commands from its parent element nor propagates its state to the parent element. In the 'MANUAL' mode the element blocks commands from its parent but propagates its status to the parent, whereas in 'IGNORED' mode the behavior is vice versa. This allows to separate detector parts, which can be controlled by different operators. A 'SHARED' mode allows control over a detector part by more than one operator. Modules cannot be partitioned but can be disabled, which switches and keeps their power supply channels off.

The FSM uses two state indicators for each hierarchical element. The STATE describes the operation mode (e.g. 'RUNNING', 'READY/ON' or 'NOT_READY') of the element and STATUS one of the four alarm states: 'OK', 'WARNING', 'ALARM' and 'FATAL'. The 'WARNING' indicates a low priority problem without risk for the detector safety, an 'ALARM' points at a high priority problem with potential risk for the detector safety which requires quickest trouble shooting and a 'FATAL' indicates a highest priority error with an acute danger for the detector or the services that may require an emergency cutout. The module STATE and STATUS are determined from the VDD and VDDA current consumption, PP2 channel states, HV sensor bias voltage current and module temperature. Dependent on the analogue and digital module currents combination a STATE and STATUS is assigned to the module. Configured modules are in the 'RUNNING' STATE and unconfigured modules in 'READY/ON' STATE. Modules with discrepancies from the expected currents are in 'NOT_READY' or 'UNKNOWN' STATE, which covers for example cases of over-currents, no clock on the module or not all expected power supply channels are switched on. For the 'OFF' STATE it is expected that all module related channels are switched off and their current measurements are consistent with zero. If the module temperature or current exceeds settable thresholds the STATUS may be increased to 'WARNING' or 'ALARM'. For the determination of the disk sector or half-stave STATE additionally the STATE of the corresponding WIENER and ISEG power supply channels ('ON', 'OFF' or 'UNKNOWN') as well as the optoboard STATE ('ON', 'OFF', 'UNKNOWN', 'RUNNING' or 'NOT_READY') are used. The optoboard STATE and STATUS are determined using the SC-OLink voltages and currents, information from the corresponding PP2 channels and the optoboard temperature. The STATE and STATUS of all higher hierarchical elements are decided on their child elements STATES and STATUSES only.

The communication between the DCS and the online DAQ software, which controls the devices of the readout chain (ROB, ROD, ROS, ...), is realized via DDC¹⁵⁸. This interface allows to synchronize the state machines on both systems, allows to request the state of hierarchical elements or device parameters from DCS, allows to send FSM commands to the DCS or change device parameters in DCS. DDC is for example used to check from DAQ that all detector components are ready for data taking or to transfer the BOC temperature and currents, which are readout by the DAQ software, to DCS. Another use case for the DDC are calibration runs where DCS parameters need to be varied, which can be automated.

¹⁵⁸ DAQ-DCS Communication

Chapter 5

Integration at CERN

The assembly of ~2300 Pixel modules was distributed between the Lawrence Berkeley National Laboratory, the Universität Bonn, the Universität Dortmund, the Universita' di Genova and the Universität Siegen. Integrated in the assembly procedure the modules have been tested electrically and with a radioactive source to guarantee their operability and measure their performance. In a ranking procedure the quality of each module was evaluated and ~2100 have been accepted for loading on staves and disk sectors. The module loading of the disk sectors, the assembly of the disks and the endcaps was performed at Berkeley. Thus both endcaps have been shipped fully assembled to CERN. The barrel modules have been glued with automated loading robots to staves at Genova, the Centre de Physique des Particules de Marseille and the Universität Wuppertal. The performance of the loaded modules have been verified with electrical tests (LOAD and STAVE measurement) before shipment of the staves to CERN.

As for the module and stave assembly the Pixel barrel integration was accompanied by measurements of the component integrities and performances to ensure that no affected components were used. For the integration of bi-staves into the half-shells this was especially important since the bi-staves cannot be exchanged individually. In the extreme case the entire half-shell has to be disassembled to exchange one bi-stave. The developed test procedures, the layout of the used measurement setup, extensions of the measurement software as well as the results for the Pixel barrel are presented in this chapter.

5.1 Stave Cabling

The integration and testing of the ATLAS inner sub-detectors took place in a 700 m² cleanroom (SR1) at CERN. SR1 is located close to the ATLAS pit to minimize the transportation risk from the cleanroom to the experiment. After a visual inspection of the received staves, GF PEEK¹⁵⁹ stave end supports were mounted on staves foreseen for 'down' position in the bi-stave. The stave positions in a bi-stave are referenced as

159 Glass-Fiber reinforced PolyEtherEtherKetones

'down' and 'up' as seen from the module loaded side of the bi-stave. The stave was mounted on a special support structure, which allowed to turn around the stave, so that the modules were pointing downwards and the stave carbon omega was accessible. Another tool was aligned at the stave support structure and provided bending support fingers for all 13 module pigtails. Successively the pigtails were bent around the bending fingers, so that the corners of the pigtail was placed on the stave carbon omega. The pigtail was temporarily fixed in this position by a third tool, which allowed fine adjustment of the pigtail position by a micro-manipulator. UV-light curing DYMAX¹⁶⁰ 9001-E-v3.7 chip encapsulant dots were placed at the corners of the pigtail and the glue was cured with an UV-light lamp for 2×30 seconds. After all pigtails were bent and glued, Type0 cables were connected to the Type0 connectors on the pigtails. Depending on the module's stave position, the foreseen stave's bi-stave position as well as the foreseen bi-stave's layer, Type0 cable lengths vary from 81 to 142 cm. The lengths of the cables were checked with dummy PP0s mounted in the right distance from the stave. Depending on the foreseen bi-stave position of the stave, the middle module (M0) cable is routed either to the A-side ('up' stave) or the C-side ('down' stave). Other module cables are always routed to the side the module is located on. Starting from the middle module the plugged connectors are secured by a Supramid® polyamide suture thread, which is wrapped twice around the connectors, the pigtail Kapton® and the Type0 cable connector PCB and is fastened with a knot. Towards the ends of the stave more and more Type0 cables from more central modules are integrated in the connector securing. The cable bundles are fixed with the polyamide thread to the GF PEEk bi-stave half-shell interfaces and stave end supports as well. All bi-stave assembly related information, like used stave serial numbers, Type0 cables, performed measurements and observed problems, are stored in quality control documents.

5.2 Connectivity Test

5.2.1 Connectivity Test Setup

The dummy PP0s used to verify the Type0 cable lengths also provide electrical connections between the modules and a connectivity setup, which was used to check the module and Type0 cable integrity. The setup (see Figure 5-1) consists of readout components, which have been used for module production measurements. A TPCC¹⁶¹ is used for regenerating clock and data signals, generating serial commands by a FPGA and charge calibration pulses. It multiplexes commands and sends the clock simultaneously to four SURF¹⁶² boards and receives upstream measurement data from one SURF board at a time. The SURF boards are connected to the two PP0s. Each SURF multiplexes, as the TPCC, commands and clock simultaneously up to four modules, but routes upstream measurement data for only one module at a time to the TPCC. Thus up to 16 modules can be connected to a single TPCC and successively measured. The sensor bias voltage can be switched and both module supply voltages

¹⁶⁰ DYMAX Corporation, Torrington, CT, USA » www.dymax.com

¹⁶¹ Turbo Pixel Control Card

¹⁶² Supply and Readout/Fanout

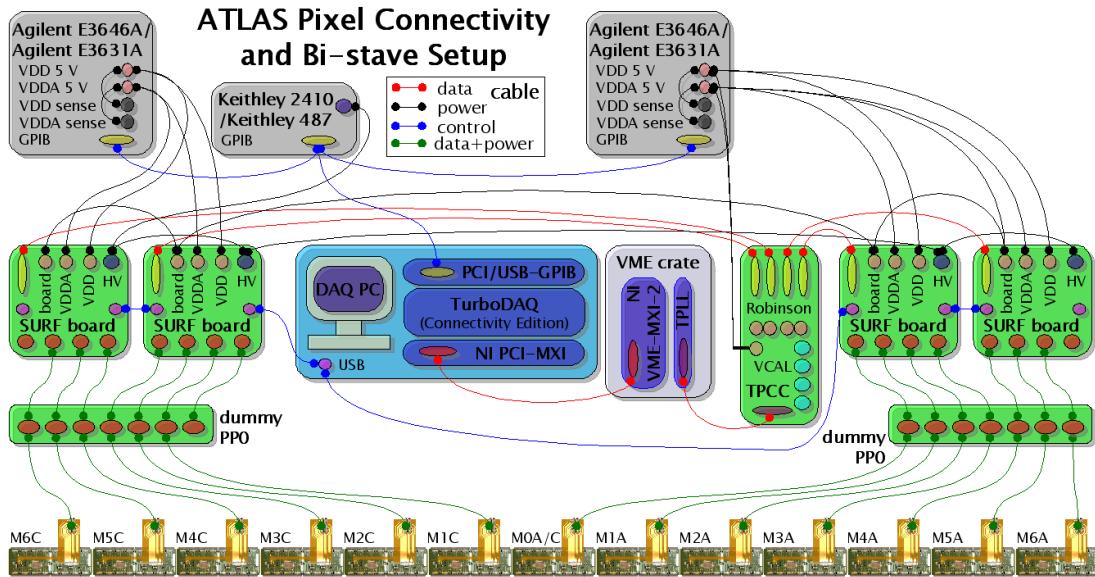


Figure 5-1 Readout and power supply components of the connectivity and bi-stave setup

are separately regulated for each module. The SURF boards support temperature measurements with the module NTCs. The TPCC communicates with a PLL¹⁶³ VME card, which generates the clock, de- and encodes the MCC serial data protocol, histograms measurement data and synchronizes the communication. Communication between the PLL and a DAQ PC is realized by a MXI-2¹⁶⁴ bus. GPIB¹⁶⁵ controlled power supplies are used to supply the TPCC and SURF boards with low voltage powers (Agilent E3631A and Agilent E3646A) and to generate the sensor bias HV (Keithley 2410 or Keithley 487). An extended version of the collaboration common DAQ software TurboDAQ is used for readout and control of the setup components and supplies. More details about the setup components can be found in [DOB04]. To allow easy and comfortable cabling of the Type0 cables, ribbon cables are used between the dummy PP0 and the SURF boards. Different ribbon cable types (e.g. straight and twisted pair) with different lengths were tested with digital injection scans to verify the error-free data transmission. The use of impedance adjustment resistors was investigated on different cables and the signal shapes of the data lines DTO and DTO2 were measured at both ends of the ribbon cable using an oscilloscope with differential probes. Data transmission errors and affected signal shapes were observed for ribbon cables with not adjusted impedance and long cable lengths. The connectivity setups with up to ~ 1 m 0.05 inch spacing straight ribbon cable extensions without impedance adjustment resistors were qualified in the scope of this work for the barrel assembly quality assurance measurements.

¹⁶³ Turbo Pixel Low Level

¹⁶⁴ Multisystem eXtension Interface

¹⁶⁵ General Purpose Interface Bus

5.2.2 CONN Measurement Program

The aim of the so-called connectivity (CONN) test is to verify all electrical connections at the module Type0 connector as well as the Type0 cable and module integrity. Connectivity data and module configurations for a bi-stave are downloaded from the Pixel production database and are combined to a SURF configuration file for TurboDAQ by an automated script. A measurement of the module NTC temperature with power off is used to test the NTC connectivity. A measurement of the sensor leakage current with the pico-amperemeter applying a sensor bias voltage of -150 V tests the HV lines and wirebonds. The module power currents IDD and IDDA after power on are measured to check for open or short power lines as well as for abnormal FE power consumption caused by FE damages. The CONN test includes adjustment of the XCKr¹⁶⁶ phase, which determines the data sampling timing off the module DTO lines with respect to the XCK on the TPLL and thus depends on the cable length. In the module configuration file the optimal XCKr phase is updated. The MCC FIFOs, receivers, registers and the MCC event building are tested in dual 40 Mbit/s and 80 Mbit/s mode to prove an error-free communication with the MCC and connection of the CK, DCI, DTO and DTO2 lines. A read-write test of the FE global and pixel registers as well as a digital injection scan with one mask-step of a 32-stage-mask in FE-by-FE mode are performed to verify the error-free communication with the FEs. The digital scan consists of 100 pulse injections into the digital logic of each pixel simulating the output signal of the discriminator. It tests the entire digital readout chain and missing or additional hits indicate a readout problem in the pixel, the FE or MCC logic or the data transmission. Since a simultaneous injection in all 2880 FE pixels would cause buffer overflows in the FEs and the MCC, staged masks (typically with 32 mask-steps) are used to sequentially inject into subsets of pixels. During the scans the NTC temperature stability is checked. The analogue currents are measured individually for FEs after configuring the corresponding FE and after issuing a FE reset command to ensure that all FEs can be configured and reset. An IDDA current of > 140 mA is expected for a configured FE and < 90 mA for a reset FE. With two short threshold scans (one mask-step on FE0) with HV on and off the noise difference between the scans is measured.

A threshold scan measures the threshold and noise of each pixel and verifies the pixel preamplifier and discriminator function. A chopper on the FE is controlled by the VCAL DAC and generates a voltage pulse V_{pulse} , which is injected into the injection capacitor C_{lo} or C_{hi} of each pixel. Thus the pixel preamplifiers see a signal equivalent to a signal generated by a charge $V_{pulse} \times C_{lo/hi}$. For each injected charge value between 0 e⁻ and 9000 e⁻ in ~45 e⁻ steps, 100 injections are performed for each pixel. The number of collected hits for each pixel and each injected charge are recorded. A schematic result of a threshold scan is presented in Figure 5-2. Injected charges above the set discriminator threshold create a preamplifier output signal which can pass the discriminator and are detected as a hit. Injected charges below the threshold should not be detected. For the ideal case a step function with an immediate detection efficiency change from 0% to 100% at the threshold is expected. In the real case the pixel noise, e.g. preamplifier noise, causes that some injected charges below the

¹⁶⁶XCK return

threshold are detected and some injected charges above the threshold are not detected. Thus the error function, a convolution of the ideal step function with the Gaussian pixel noise distribution, describes the discriminator output. It is the integral of the Gaussian function:

$$f_{error}(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^x \exp(-t^2) dt \quad \text{with} \quad t = \frac{x-\mu}{\sigma} \quad [5.1]$$

The error function is fitted (so-called S-curve fit) to the threshold scan result of each pixel. The threshold value of a pixel is defined at 50% efficiency value of the S-curve.

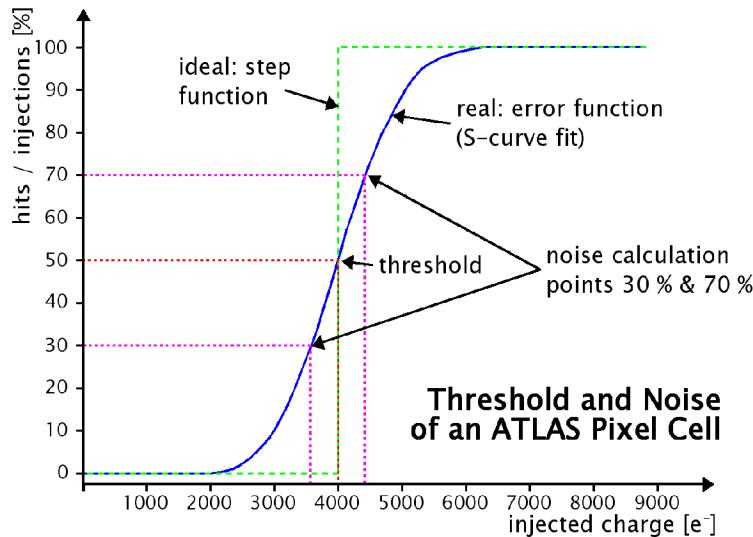


Figure 5-2 Schematic result of a Pixel cell threshold scan with the ideal step function and real error function

The noise of a pixel is inversely proportional to the steepness of the transition from no detected hits to full efficiency and can be calculated by using the 30% and 70% efficiency values of the S-curve with:

$$\sigma = \frac{Q_{70\%} - Q_{30\%}}{f_{error}^{-1}(70\%) - f_{error}^{-1}(30\%)} ; \quad \begin{aligned} \sigma &: \text{pixel noise} \\ Q &: \text{injected charge} \\ f_{error} &: \text{error function normalized to 1} \end{aligned} \quad [5.2]$$

The measurement of the noise difference between biased and unbiased Pixel sensor can be used to identify disconnected bump bonds or verify that the bias voltage is seen by the sensor. It is a more reliable method than just measuring the HV current consumption since the depletion of the sensor is directly checked. In the biased case the sensor is fully depleted and the pixel implantations are isolated. Normal noise values ($\sim 160 \text{ e}^-$) are measured. In the unbiased case all pixel implantations are short circuited through the sensor bulk and thus the pixel preamplifiers see a very high capacitive load. Therefore increased noise values are measured. Since the AMS bump bond resistivities are higher than the IZM bump bond resistivities (see section 4.3.1) higher noise values ($\sim 700 \text{ e}^-$) are measured for unbiased IZM modules than for unbiased AMS modules ($\sim 350 \text{ e}^-$). No significant noise difference between biased and unbiased measurement with high noise values indicates that the HV bias voltage is not

seen by the sensor. No noise difference or slightly decreased noise values indicate that the bump bond is disconnected and the corresponding preamplifier is not connected to the sensor pixel. A significant noise difference of $> 110 \text{ e}^-$ proves that the sensor sees the bias voltage and the preamplifier has electrical connection to the sensor pixel.

The scan results are analyzed and the connectivity TurboDAQ panel indicates to the operator the result of each individual test. The measurement results are analyzed and summarized by an automated script and stored in the bi-stave quality assurance document.

5.2.3 Connectivity Test Results

Observed problems during the CONN tests include broken lines in the Type0 cables and a insufficient test procedure for the connectivity of sense lines. Therefore a comparison of the sensed voltages with the set voltages was included in the CONN test to verify the electrical connection of the sense lines. Voltage differences up to 250 mV between the set and the sensed voltage are accepted. A typical broken aluminum wire in the Type0 cable close to the heat shrinking tubing is shown in Figure 5-3. A reason for the fragility of the Type0 cable was found in their production procedure. During the etching of the Type0 wire ends to remove the polyurethane isolation some wires are bent with a small radius. The etching in $\sim 400^\circ\text{C}$ NaOH causes a warming up of the isolation at the bend, which is heated above $\sim 250^\circ\text{C}$.

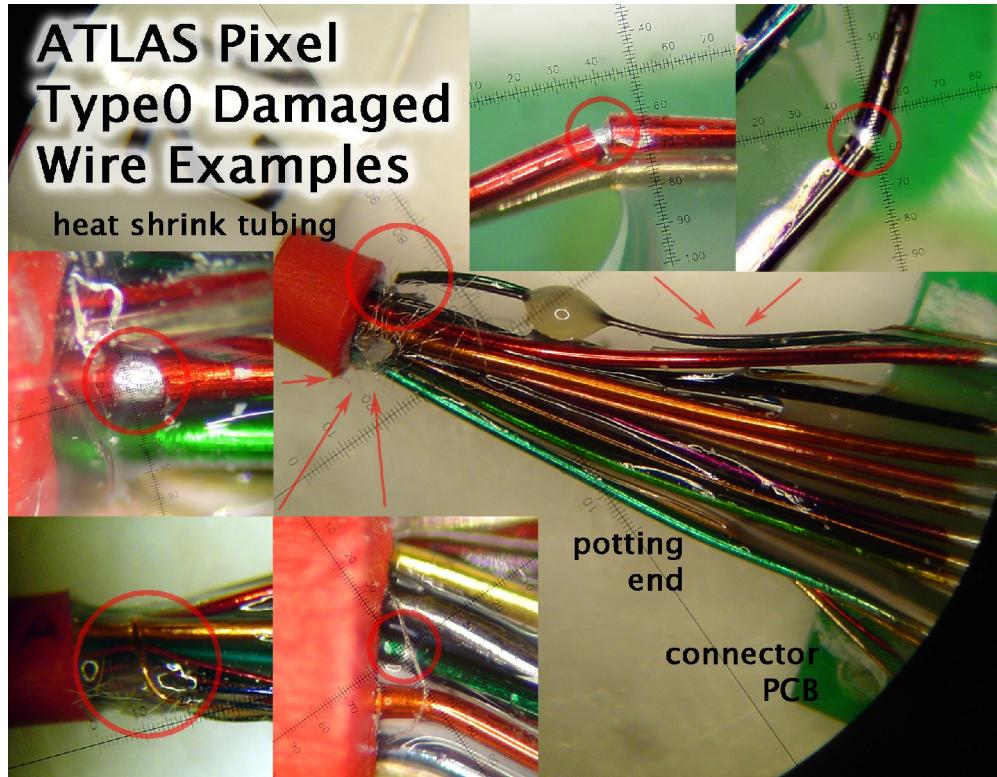


Figure 5-3 Example of broken Type0 wires as well as examples of cracked polyurethane isolation of wires

When the wire is straightened this can cause cracks of the polyurethane isolation, which also gives mechanical stability to the wire. To guarantee that no affected Type0 cables were integrated an intensive visual inspection of the connector regions was introduced to identify cables with isolation cracks. Additionally an electrical test was introduced which tests the connectivity during the cable ends are bent several times in all directions and rapidly cooled down by cooling spray to provoke the observation of loose connections. A more soft potting was added to the connector potting to avoid hard bending of the wires at the end of the potting and it was ensured that no single wires stick out of the potting. New cables were produced to replace affected cables and as far as possible also cables from the original production.

5.3 Bi-Stave and Half-Shell Assembly

A 'down' stave was screwed to a bi-stave tool and an 'up' stave was screwed with aluminum screws to the stave end supports of the 'down' stave. Depending on the bi-stave position in the half-shell the stave cooling tube fittings of the A- or C-side were fixed with the bi-stave tool to avoid torsion forces on the cooling tubes during the U-link mounting. The vacuum grease lubricated U-link was mounted and the U-link nuts were tightened with a defined force. The leak tightness of the bi-stave was verified. The bi-stave was mounted into a half-shell and was fixed with aluminum screws in the carbon-carbon half-shell. Some snapshots of the stave cabling, bi-stave mounting, half-shell integration and clamping as well as some of the test procedures are shown in Appendix A Figure A-12.

5.3.1 BIST Measurement Program

After the integration of a bi-stave in the half-shell the integrity of the installed and the previously installed bi-stave was verified. Therefore the 13 Type0 cables of a bi-stave side were connected to a mobile version of the connectivity setup. The connectivity and configuration files were produced by the same automated script used for the CONN configuration files. A connectivity test equal to the CONN test was performed on the previously installed bi-stave to ensure that no wirebonds or Type0 cables were damaged during the installation of the new mounted bi-stave. Additionally to the connectivity test on the new installed bi-stave a more extensive measurement of the module performance was done. The bi-stave measurement (BIST) includes a digital scan with all 32 mask-steps in concurrent FE mode as well as HV on and HV off threshold scans with 32 mask-steps in concurrent mode. This allows to measure the amount of digital and analogue bad pixels and to identify disconnected pixel. Since the 32 mask-step scans require several minutes of module operation a fan array was used to keep the module temperatures below the 39°C temperature interlock. Besides the verification of the connectivity of the mounted stave and the integrity of its modules, the aim of the BIST measurement is to allow performance comparisons with the LOAD measurements and check for module damages on the pixel level.

5.4 Pixel Barrel Performance

A comparison between the LOAD, CONN and BIST measurements allows to verify the production performance of the Pixel barrel section and to check for damages that may have occurred during the assembly. The distribution of barrel module sensor leakage currents can be seen in Figure 5-4 for the LOAD, CONN and BIST measurements. Normalized amounts of entries are used, because for CONN measurement almost all 1465 barrel modules are considered but for the LOAD and BIST measurements only about half of the module leakage currents were analyzed for the quality assurance documents. The mean value slightly increases from $1.06 \pm 1.6 \mu\text{A}$ for the LOAD measurement, $1.83 \pm 1.6 \mu\text{A}$ for the CONN test to $3.15 \pm 2.5 \mu\text{A}$ for the BIST measurement. The reason for this increase are quite different temperature and light conditions for the different measurements. The LOAD measurements were performed in a dark cold box. Thus no photo current contributes to the measured LOAD HV current. The staves were cooled with a chilled coolant to module NTC temperatures between 15 and 25°C. For the first CONN tested staves the modules were not light covered besides the covering of the sensor by the flex hybrid. Thus an influence of the ambiguous light amount was seen on the measured CONN HV currents. With CONN tests progress measurement problems of the used Keithley 2410 pico-ampermeters around $1 \mu\text{A}$ were observed. To reduce the photo-current a light cover was used to shadow the modules with the drawback that different modules have seen different amounts of light in the CONN test. No special module cooling was necessary since only short FE-by-FE scans sequentially on the modules were performed and the module NTC temperatures reached between 22 and 32°C. For the longer and concurrent BIST measurements the modules were cooled with the fan array to module NTC temperatures between 27 and 37°C. The modules were shadowed by

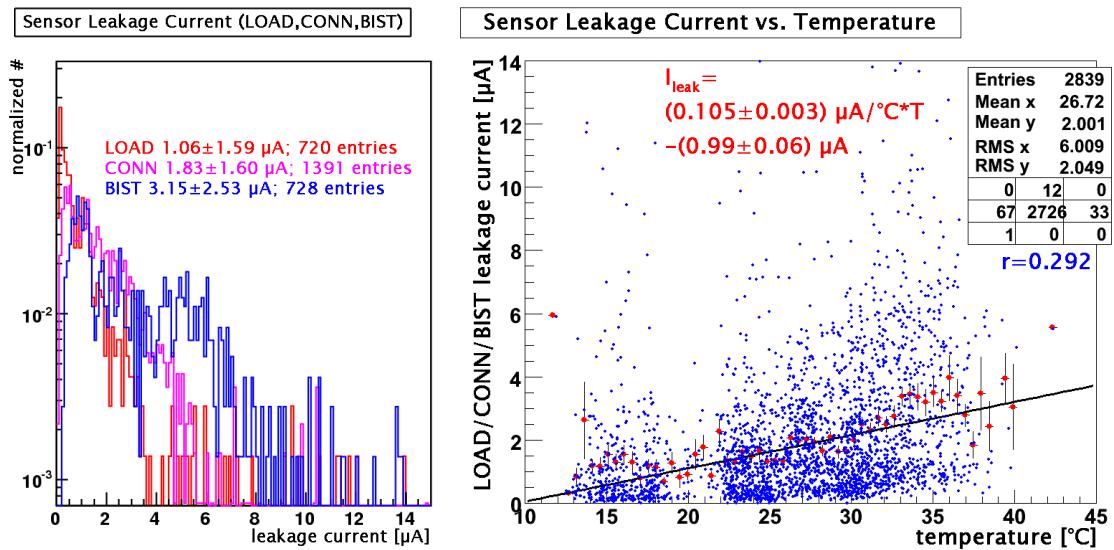


Figure 5-4 Leakage current distribution of the LOAD, CONN and BIST measurement (left) as well as temperature dependence of the mean leakage current (right)

this fan array and more constant light conditions can be assumed. Due to these different measurement conditions only relative weak correlations can be seen between the different measurements in Figure 5-5. Best correlation is observed between the CONN tests and the BIST measurements, most probably due to similar light conditions. The best linear fit of the mean leakage current versus module NTC temperature results in temperature factor of $\sim 0.1 \mu\text{A}/^\circ\text{C}$. If the measurements would have been performed at equal light conditions a measurement of the silicon band gap width from the temperature dependence [KLA05]:

$$I(T_N) = I(T) \left(\frac{T_N}{T} \right)^2 \cdot e^{-\frac{\Delta E_G}{2k} \left(\frac{1}{T_N} - \frac{1}{T} \right)} ; \quad \begin{aligned} k &: \text{Boltzmann constant} \\ \Delta E_G &: \text{silicon band gap width} \\ T_N &: \text{normalization temperature} \\ T &: \text{temperature} \end{aligned} \quad [5.2]$$

would have been possible.

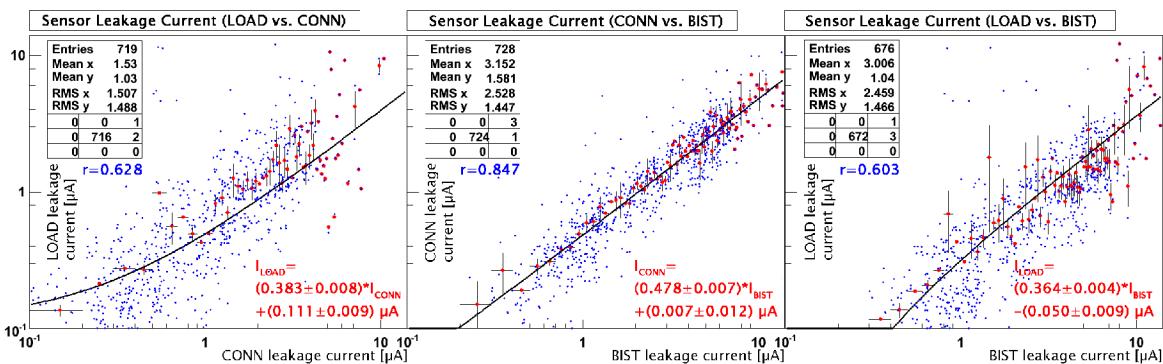


Figure 5-5 Correlations of the LOAD, CONN and BIST leakage current measurements

Lower leakage currents in the B-layer modules compared to the Layer-1 modules in the LOAD measurements (see Figure 5-6) can be explained by the module ranking procedure, which assigned high quality modules to the B-layer. Lower statistics for Layer-2 do not allow a comparison with the other layers. Due to the mentioned measurement condition differences, the lower B-layer leakage currents are less clear

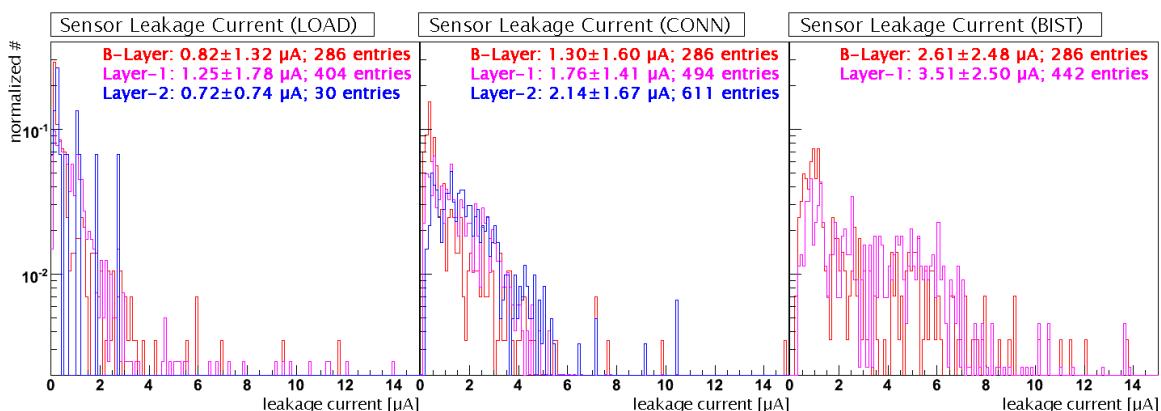


Figure 5-6 Layer dependence of the LOAD, CONN and BIST leakage current measurements

for the CONN tests and BIST measurements. In the CONN tests, where sufficient Layer-2 leakage current measurement statistics exists, slightly higher leakage currents in Layer-2 than in Layer-1 are visible. Even though the CONN and BIST leakage current measurements do not allow precise sensor quality conclusions, they serve the main aim to prove the HV line connectivity and would show dramatically increased leakage currents caused by sensor damages.

The temperature distributions for the LOAD measurement, CONN test and BIST measurement are shown in Figure 5-7. The different mean temperatures are caused by the different cooling conditions of the tests. The structure in the LOAD temperature distribution is caused by different module temperatures from the different stave assembly sites (Genova $16.6 \pm 3.2^\circ\text{C}$, Marseille $23.4 \pm 2.5^\circ\text{C}$ and Wuppertal $18.6 \pm 2.66^\circ\text{C}$) and temperature dependences on the modules stave position (see Figure 5-8). Temperature dependence from the modules stave position is also visible for the CONN test and is caused by the sequence in which the modules are tested. For the BIST measurement where the modules are operated for longer time and are cooled by the fan array the stave position dependence is also visible, but the modules show

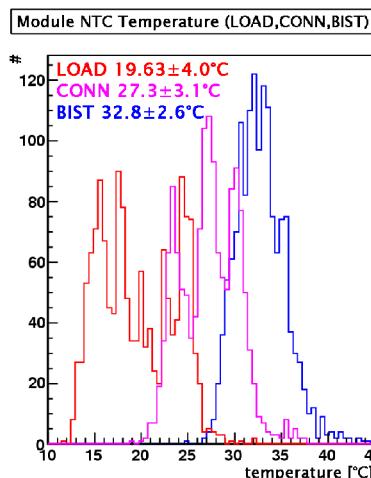


Figure 5-7 Module temperature distributions for the LOAD, CONN and BIST measurements

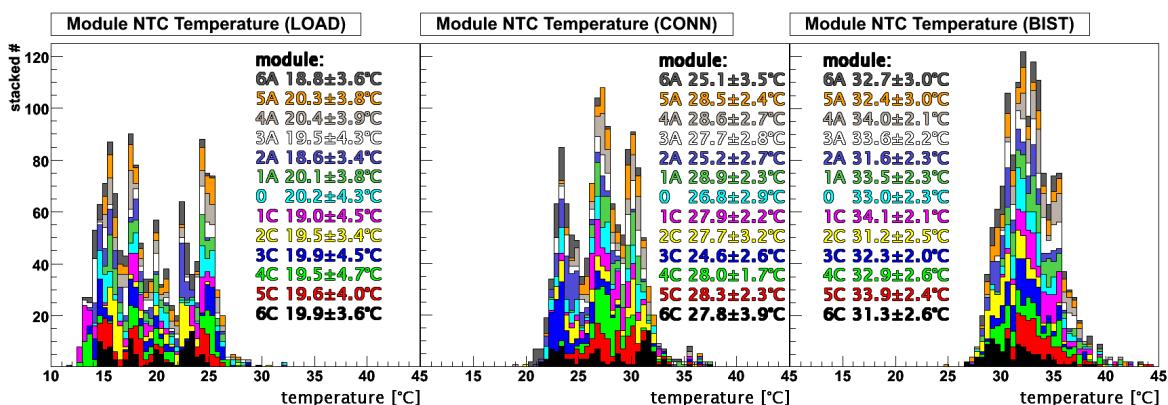


Figure 5-8 Stacked temperature histograms for the different module position on the stave for LOAD, CONN and BIST

more similar temperature distributions. The same behavior can be observed for the modules layer position as well (see Appendix A Figure A-13).

The distribution of the total bad pixel number per module is shown in Figure 5-9. A slight increase between the LOAD (63 ± 99 mean bad pixel per module) and the BIST (68 ± 105 mean bad pixel per module) measurement is observed.

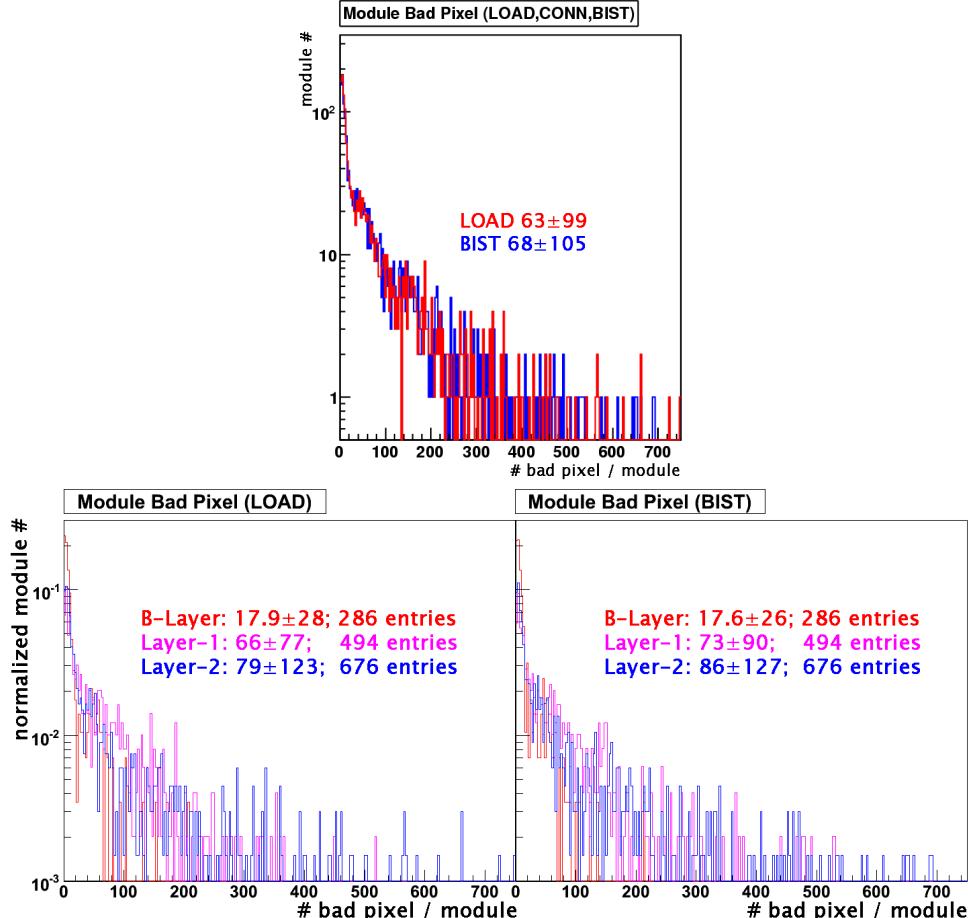


Figure 5-9 Module total bad pixel distribution and layer dependence for LOAD and BIST measurement

Lower mean values for the B-layer and Layer-1 are caused by the ranking procedure of modules and staves, which assigns modules and staves with lower amount of bad pixel to inner layers. The correlation of analogue injection bad pixel, disconnected pixel and total bad pixel between LOAD and BIST measurement are shown in Figure 5-10. Linear fits of the correlations result in a 1% decrease of analogue bad pixel, a 7% increase of disconnected pixel and a 2% increase of total bad pixel. A breakdown of the total bad pixel into digital injection bad, analogue injection bad and disconnected pixel distributions is presented in Figure 5-11. The amount of digital bad pixels is negligible (~1% of total bad pixel) and only one module with a high number of digital bad pixels (~375) exists. The respective module has one FE column pair not working which causes 320 not working pixels. About 37% of the total bad pixels are caused by analogue bad pixels and ~62% are caused by disconnected pixels. No indication for a significant change of the fraction between these two bad pixel causes

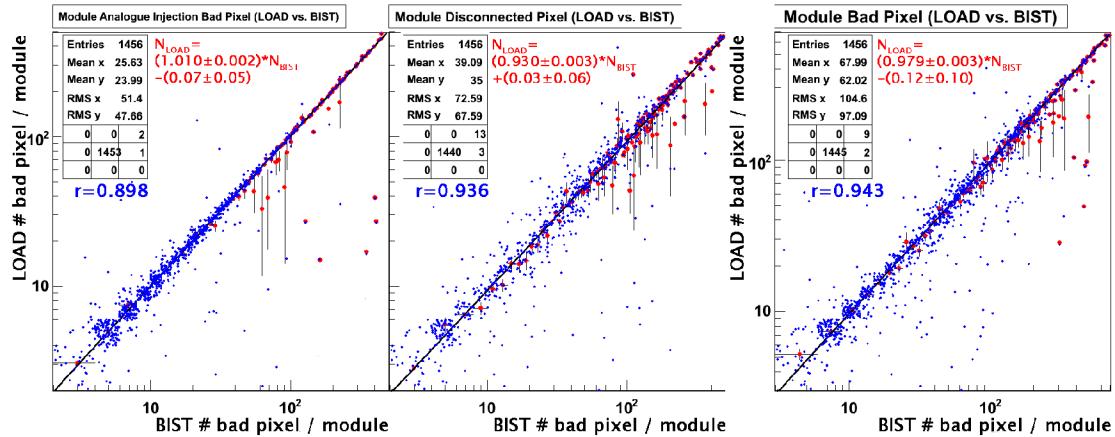


Figure 5-10 Module bad pixel correlations between LOAD and BIST measurement for analogue bad pixel, disconnected pixel and total bad pixel per module

in dependence of the total bad pixel amount is visible. The total amount of bad pixels, the fraction of the different bad pixel causes as well as their fraction of the total amount of pixels in the Pixel barrel are given in Table 5-1. The total bad fraction increases from 1.5% for LOAD to 1.6% for BIST, which is mainly caused by an increase of disconnected pixels. Since this damage can affect the module sensor to FE mechanical connection stability it can provoke additional disconnected pixels. Thus an increase of the disconnected pixel amount for modules with a contiguous region of disconnected pixels is expected when mechanical stress, e.g. thermal cycling, is applied on these modules. Therefore especially the disconnected pixel amount should be monitored against time and temperature cycles. However the fraction of total bad pixel for the Pixel barrel is with 1.6% well below the aimed <1% affected pixel fraction. As targeted by the module and stave ranking procedure the fraction of bad

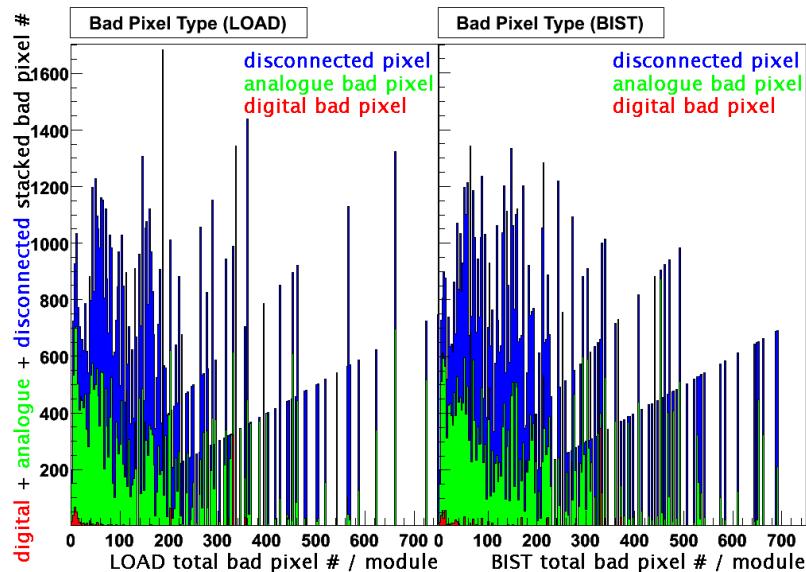


Figure 5-11 Breakdown of the total bad pixel number into digital bad, analogue bad and disconnected pixel for the LOAD and BIST measurement

pixel on the B-layer ($\sim 0.4\%$) is clearly below the mean bad pixel fraction and is for the Layer-2 ($\sim 2\%$) slightly above the mean fraction. The Layer-1 bad pixel fraction is very close to the barrel fraction. It has to be mentioned that other possible pixel damages like for example merged pixels and noisy pixels are not included in these measurements, but their fraction can be expected to be small due to previous measurements.

Bad pixel type:	LOAD bad pixel amount (fraction):	BIST bad pixel amount (fraction):	LOAD total fraction:	BIST total fraction:
digital injection	875 (0.9%)	1047 (1.0%)	0.013‰	0.016‰
analogue injection	36542 (36.9%)	40518 (37.1%)	0.54‰	0.60‰
disconnected	61618 (62.2%)	67760 (61.9%)	0.92‰	1.00‰
barrel sum (~67.1M pixel)	99035	109325	1.5‰	1.6‰
B-layer ($\sim 20\%$)	5105 (5.2%)	5033 (4.6%)	0.39‰	0.38‰
Layer-1 ($\sim 34\%$)	32371 (32.7%)	36850 (33.7%)	1.42‰	1.62‰
Layer-2 ($\sim 46\%$)	61559 (62.1%)	67442 (61.7%)	1.98%	2.17‰

Table 5-1 Pixel barrel bad pixel numbers and fractions

The integrated fraction of usable modules and bad pixel amount fractions for the different bad pixel types and the total bad pixel up to a total bad pixel amount per module cut are presented in Figure 5-12. The plots illustrate the effect of a total bad pixel per module production assembly cut on the amount of bad pixels and the amount

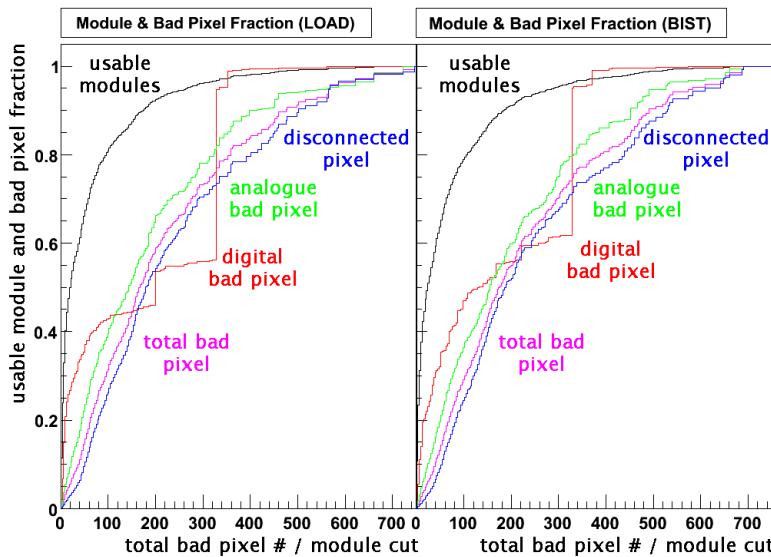


Figure 5-12 Integrated fraction of the usable modules and bad pixel types up to a total number of total bad pixel / module cut

of usable modules. For example it shows that $\sim 10\%$ of the total bad pixel are on the worst $\sim 1\%$ of the modules, which have more than 490 bad pixel. The worst 5% of the modules (above 290 bad pixel) are causing $\sim 1/3$ of all bad pixel. This shows that a significant amount of bad pixel are located on a relatively low amount of modules and that the production quality of the modules allow a more tighter total bad pixel number cut with a justifiable amount of modules to replace. It also shows that a total bad pixel number cut below 160 pixels is not reasonable since the number of usable modules disproportional highly decreases with respect to the decrease of total bad pixels.

Threshold distributions for LOAD, CONN and BIST are shown in Figure 5-13. For all three measurements a split-up of the thresholds can be seen in a higher populated group with threshold values around 4200 e^- and in a less populated group with threshold values around 4600 e^- (green dots). A vast fraction of the modules showing high threshold values are LOAD tested in Marseille (see Figure 5-15). For the LOAD scans in Marseille module configuration files with a 'cold' threshold tuning at $\sim -5^\circ\text{C}$

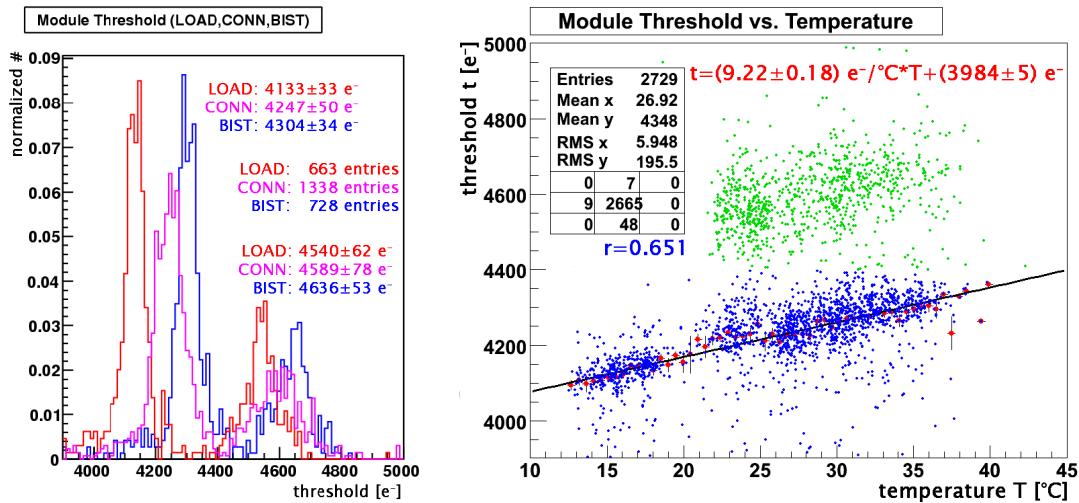


Figure 5-13 Threshold distributions for LOAD, CONN and BIST and threshold vs. temperature (only blue threshold values ($< 4400 \text{ e}^-$) are considered in the fit)

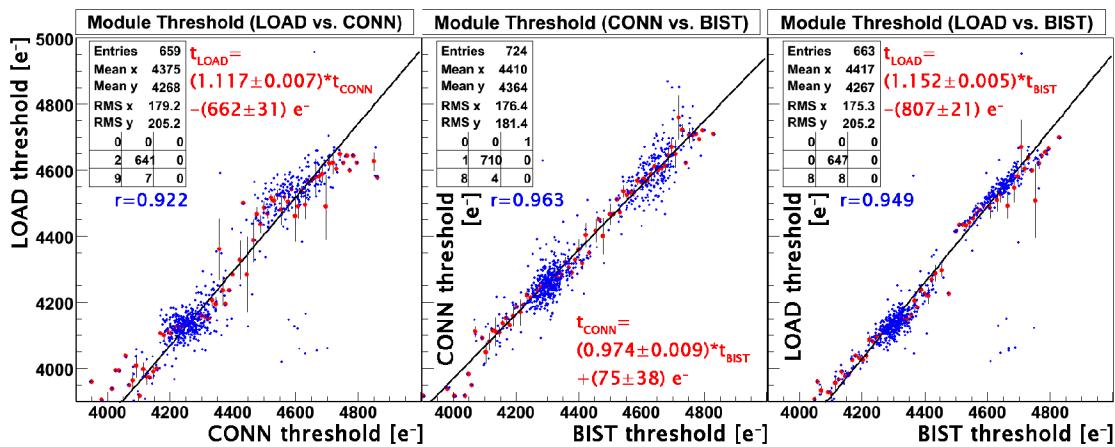


Figure 5-14 Threshold correlations

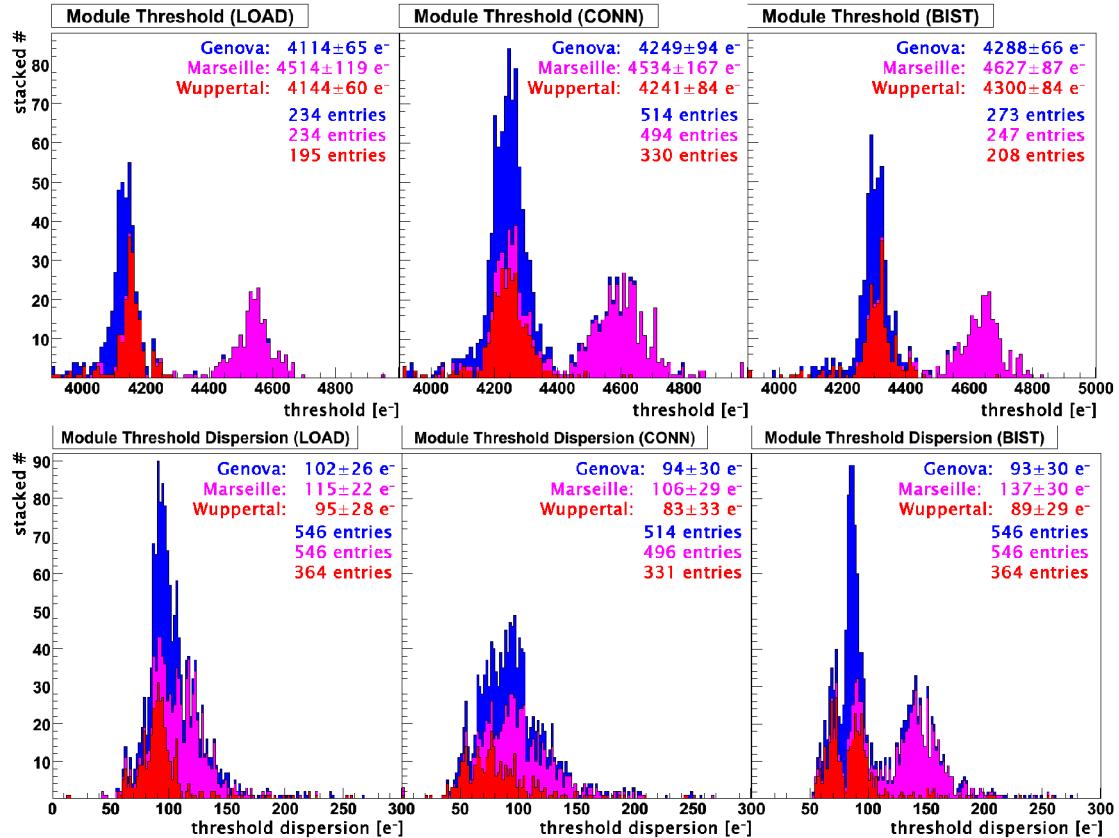


Figure 5-15 Threshold and threshold dispersion stave loading site dependencies

have been used, whereas in the other two stave assembly sites the LOAD configuration files are based on room temperature threshold tunings. The threshold versus temperature correlation of all scans can be seen in Figure 5-13 as well. A linear fit to all thresholds below 4400 e⁻ (blue markers) indicates a temperature dependence of about 9.2 e⁻/°C. Thus the shift in the thresholds for the magenta threshold values is consistent with a temperature difference between threshold tuning and measurement of about 30°C. The LOAD configuration files have been used for the CONN and BIST measurements as well. Therefore the correlations between the threshold scans in Figure 5-14 show that modules of the high threshold group have high thresholds in the CONN and BIST measurements as well. About ten outliers in the LOAD vs. CONN and LOAD vs. BIST correlations mainly change from the low threshold to high threshold group. Only for one module a change from the low threshold to the high threshold group is seen in all three correlations. Even though only a very limited amount of pixel per module is considered in the CONN scan it gives a sufficient threshold value to detect significant changes.

The threshold dispersion distributions for the different measurements are presented in Figure 5-16. For the LOAD measurement the mean threshold dispersion has a value of 105 e⁻ with a tail of the distribution up to about 250 e⁻. With the reduced statistics in the CONN test the shape of the distribution is similar, but has a ~5 e⁻ higher width and a ~5 e⁻ lower average value. In the BIST measurement a split up into two groups can be observed. The group of modules with increased threshold dispersion values

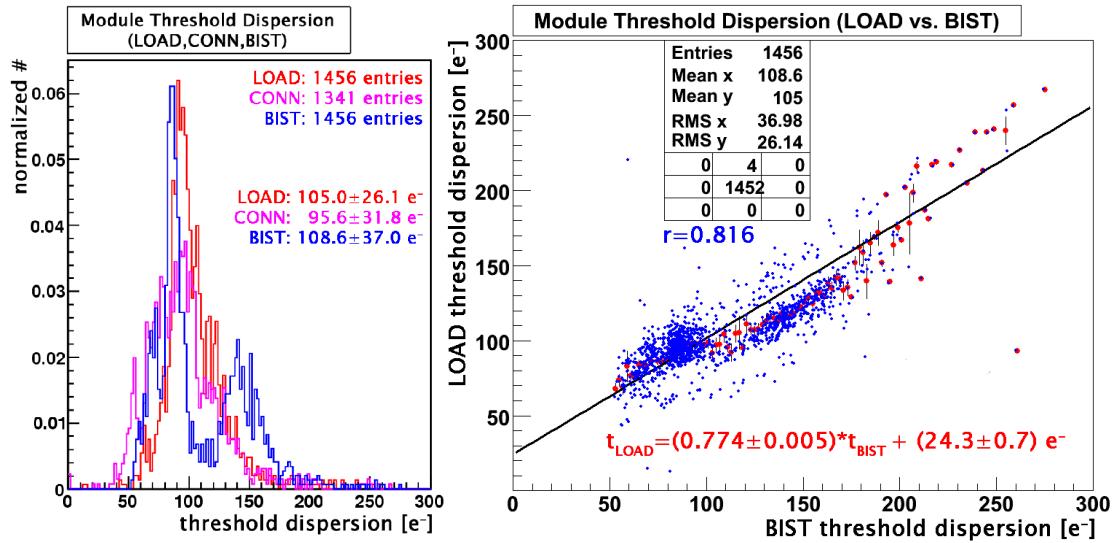


Figure 5-16 Threshold dispersion distributions and the LOAD versus BIST correlation

around $150 e^-$ is mainly located on staves LOAD tested in Marseille as shown in Figure 5-15. The tendency of higher threshold dispersion values of modules LOAD tested in Marseille is visible in the LOAD and CONN distributions as well. A split-up into two groups can also be observed for modules LOAD tested in Wuppertal, but these groups are separated by only $\sim 20 e^-$. The correlation in Figure 5-16 shows that for the BIST lower threshold dispersion group the threshold dispersion values decreased compared to the LOAD measurements, whereas for the high threshold dispersion group the threshold dispersion values increased. No temperature dependency is observed that could explain this behavior.

The noise distribution for the three measurements and the correlation between LOAD and BIST are shown in Figure 5-17. In the CONN measurement $\sim 10 e^-$ lower noise

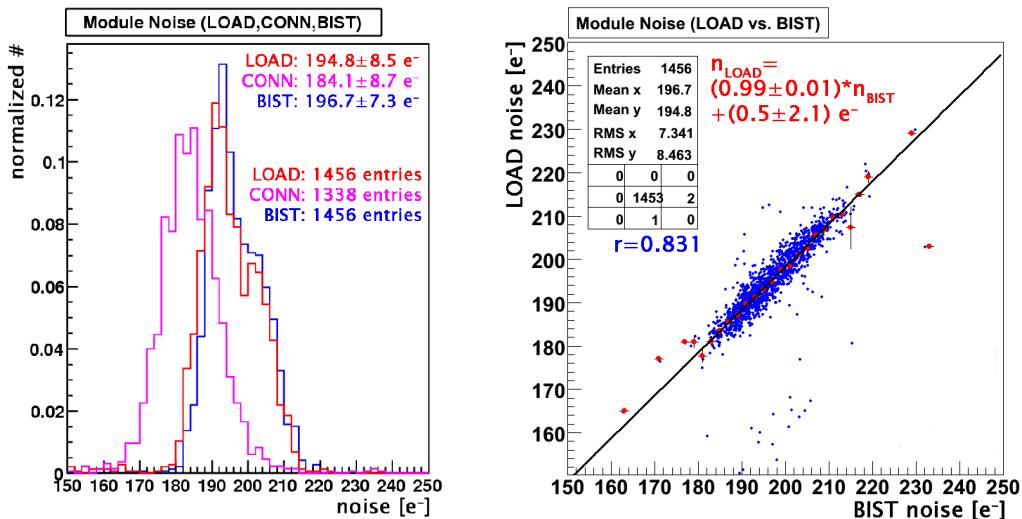


Figure 5-17 Noise distributions and the LOAD versus BIST correlation

values are measured. In difference to the LOAD and BIST measurement the CONN threshold scans used to determine the noise are performed with only one of the FEs configured. Between LOAD and BIST the measurements are consistent with no change of the module noise. About 20 outliers are mainly caused by modules that show low noise values below 180 e⁻ in the LOAD measurement.

Slightly higher (one sigma) module digital and analogue currents are measured in the BIST measurement compared to the LOAD measurement (see Figure 5-18). This can be explained by longer Type0 cables, ribbon cable extensions, remote sensing and current measurement at the SURF board. Due to the increased currents the module power is about one sigma higher as well as shown in Figure 5-19. The measure for the

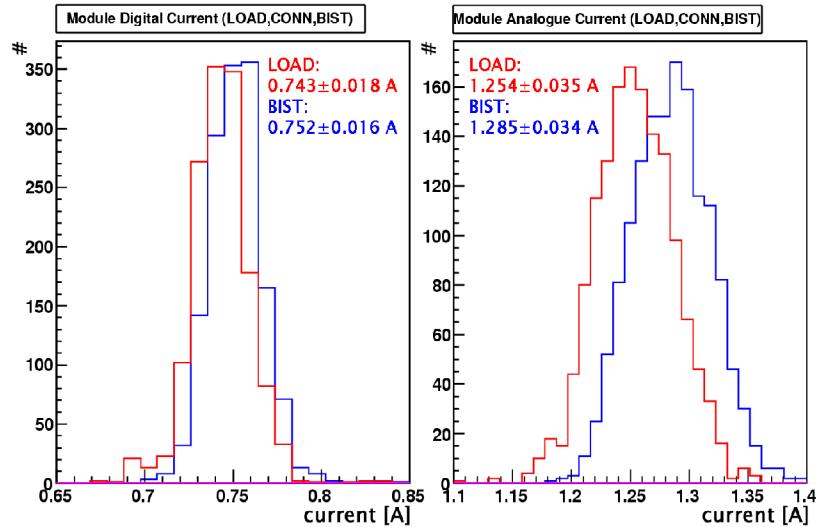


Figure 5-18 Module digital and analogue supply voltage current distributions

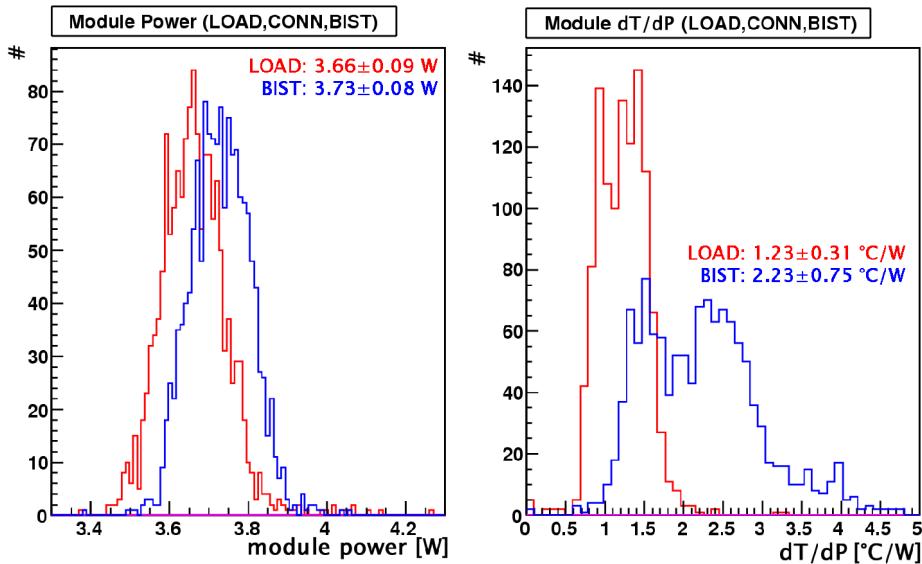


Figure 5-19 Module power and module dT/dP distributions

thermal coupling to the cooling system, the thermal resistance dT/dP , is presented in Figure 5-19 as well. For LOAD measurements with chilled coolant module cooling through the aluminum stave cooling pipes the mean value for dT/dP is $1.23 \pm 0.31^\circ\text{C}/\text{W}$. The dT/dP measurement allows to identify modules with poor thermal coupling to the stave TMT and can indicate poor thermal coupling between the TMT and the cooling pipe by delamination of the TMT from the stave omega and the cooling pipe. Modules LOAD tested in Marseille have a tendency to lower dT/dP values around $1^\circ\text{C}/\text{W}$, modules LOAD tested in Wuppertal have mainly higher dT/dP values of about $1.5^\circ\text{C}/\text{W}$ and modules LOAD tested in Genova mainly values at $1.25^\circ\text{C}/\text{W}$. Since different coolants and different chillers have been used at the different stave assembly sites this does not indicate different thermal coupling qualities. No significant module on stave position dependency is visible. The BIST average dT/dP value of $2.23 \pm 0.75^\circ\text{C}/\text{W}$ shows the cooling performance of the module air convection cooling by the fan array. An observed module on stave position dependency with high dT/dP value for the outer stave positions and decreasing values towards the inner positions are caused by worse cooling at the border of the fan array and the sequence of the module testing, which causes increased module temperatures for later tested modules of a stave.

In all measurements, where not explicitly mentioned, no significant layer, temperature, module position on stave or stave assembly site dependency is visible. In summary no significant worsening of the Pixel Detector barrel performance is observed and no indication for damages caused by the assembly procedure are visible. The slight increase of the number of bad pixel might possibly be caused by mechanical stress on the modules during the assembly and should be monitored as it may increase with additional mechanical stress, like temperature cycling.

5.5 Pixel Package Assembly

The stave loaded and BIST tested Layer-1 and Layer-2 half-shells were clamped together to the layer shells and the integrity of the edge stave modules was verified by a short connectivity test after the clamping. Type0 cables were fixed to temporary support structures, which were used for cable support during the stave loading. The Layer-1 and Layer-2 shells were mounted on the ITT¹⁶⁷, a support structure which allows to slide Pixel Package components into each other by a rail system and to rotate the Pixel Package for access from all sides. The Layer-2 shell was mounted into the barrel carbon-carbon global support structure and its Type0 cables were fixed to a temporary support structure around the global support. After the Layer-1 was moved into the Layer-2 shell, the Layer-1 Type0 cables were attached to the temporary cable support around the global support as well. The beryllium beampipe was mounted to the ITT and the B-layer half-shells were clamped together directly around the beampipe, since the distance between B-layer and beampipe is too low to allow another mounting procedure. In the next assembly step the outer layer package was slided over the B-layer. This is only possible from the B-layer side where all stave cooling loop U-links are mounted (see section 5.2). The global support was connected to the B-layer and the Type0 cables were fixed to the temporary support. Cooling

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capillaries and exhaust tubes for the barrel layers were connected to route them outside of the endcaps through a gap between the barrel and the endcaps (see Appendix A Figure A-14). This allowed in the next step the attachment of the endcaps to the barrel with Type0 cable and cooling tube routing outside of the endcaps. After the System Test (see chapter 6) of the endcap A and a receive connectivity test of the endcap C, their global support structure segments were attached to the barrel global support (see Appendix A Figure A-15). Short connectivity tests were performed after installation steps which might apply mechanical stress to modules. The BPSSes with installed BCM detectors were mounted on the beampipe at both ends of the Pixel Detector. SQPs were sequentially mounted to the BPSSes. The SQP cooling capillaries and exhaust tubes were connected to the layer and disk cooling tubes. Barrel and disk Type0 cables were connected to the PP0s on the SQP. A Connectivity Test (CT) with the final readout system used in the System Test was performed. It verified the module integrity, proved their connectivity through the Type0 cables and SQP as well as it ensured the integrity and tunability (see section 6.3.5) of the optoboards mounted on the SQP. After the installation of all SQPs the Pixel Package was moved from the ITT to the DST¹⁶⁸, which was used for the transport from SR1 to the ATLAS pit. The DST was used as well to slide the Pixel Package into the PST installed in the SCT Detector in ATLAS.



Figure 5-20 Insertion of the Pixel Package into the DST

168 Dummy Support Tube

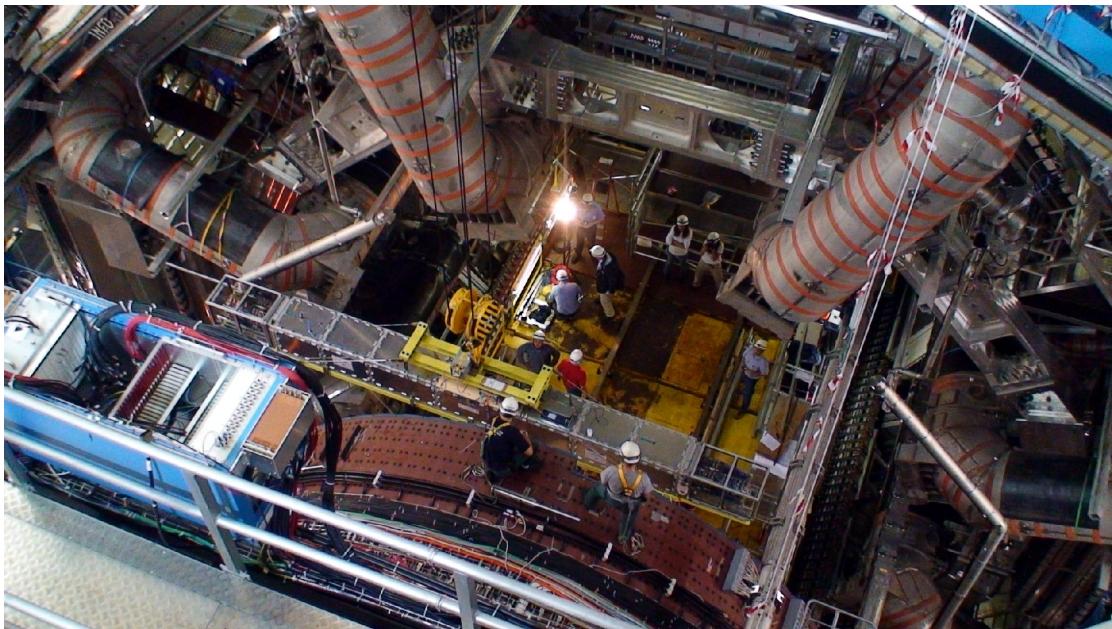


Figure 5-21 Descent of the Pixel Package into the the ATLAS experiment

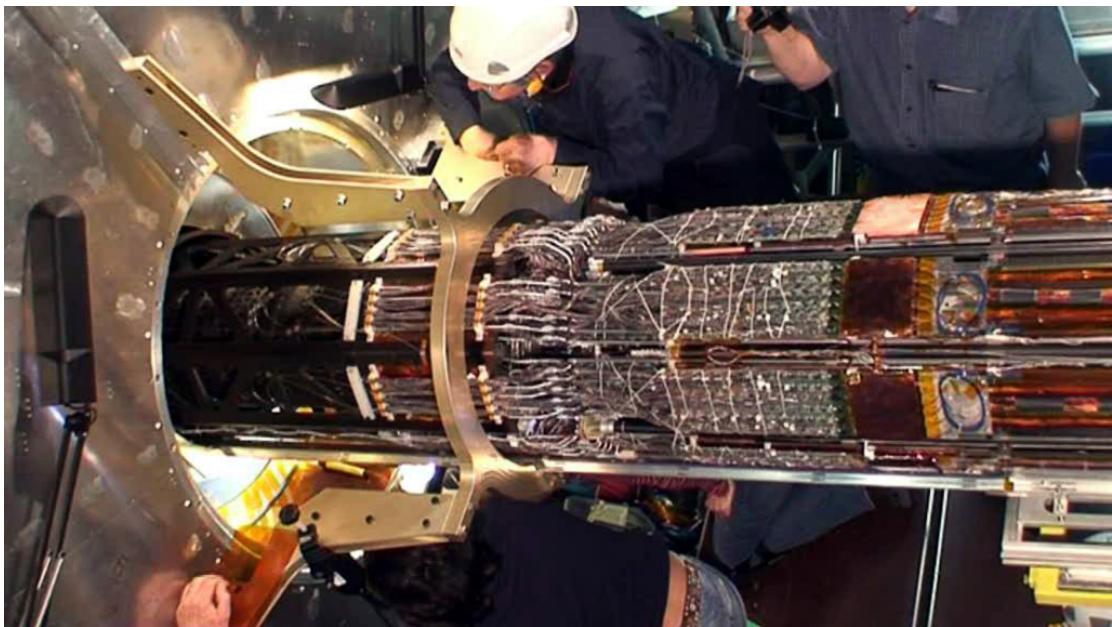


Figure 5-22 Installation of the Pixel Package into the PST in the ATLAS experiment

Chapter 6

System Test

To verify that the Pixel Detector integrated assembly, its DAQ readout chain and its auxiliary services perform as expected, an ~8% fraction of the detector system was assembled and operated in a laboratory setup in SR1. The aim of the Pixel System Test is to use a setup with components as close to final as possible and to understand their interplay. It is used to test and debug the hardware and software components in parallel and allows operator feedback to the experts. The detector is operated under realistic conditions in long-run mode to test its stability and to allow tracking of its performance over a long term. An additional important goal is to define, qualify and learn operation procedures for the switch-on, switch-off, calibration and data taking in the experimental setup. Non-expert operator runs allow weak spots and too complicated operation procedures to be identified as well as they are used to drive the knowledge transfer from the different component experts to the collaboration. A common naming convention is forced and missing tools and documentation can be discovered. The scalability of the system is checked and stress tests can be performed.

To study the basic parameter dependencies of the optical link a laboratory setup with a PP0 test board, a single optoboard and up to seven concurrent readout modules was used. The operation of a bi-stave with the evaporative cooling system, the operation of modules in 160 Mbit/s mode, the operation of detector and service components with the DCS and calibration of the detector with the STcontrol software as well as the interaction of service components were investigated in a so-called bi-stave System Test setup. It allowed the concurrent operation of up to 13 modules and consisted of a C_3F_8 cooled bi-stave, two PP0 test board attached optoboards, cable fan-outs to replace the SQP connections as well as production and prototype components of almost all service elements. The setup was extended to concurrently readout one of the Pixel endcaps with 144 modules through a prototype SQP with 24 attached optoboards under realistic environmental conditions. The endcap and the optoboards on the SQP were chilled with the evaporative cooling system. For almost all service elements production components could be used. Even though all on- and off-detector components have been tested on their production sites and in smaller System Test setup in various labs the interaction of all detector elements and the scalability of the service and readout chain was reasonably tested the first time. To investigate the data taking operation and software as well as the trigger components scintillators were integrated in the System Test setup for triggering of cosmic muons.

6.1 Optical Link Tuning

An error-free data transmission via the optical link between the BOC and the optoboard (see section 4.4, 4.5 and 4.6.1) is essential to guarantee precise module configuration and triggering as well as to allow a sensible readout of module hit and calibration information. In the scope of this work the influence of the different optical link parameters was investigated and a procedure for the tuning of the optical link parameters was developed for the Pixel Detector.

The readout chain parameters influencing the optical data transmission quality are shown in Figure 6-1. On the BOC to optoboard transmission (TX) side the VCSEL laser current, determining the VCSEL light output power, can be controlled per channel in 256 steps by the BPM. The BPM also allows channel-wise adjustment of the output signal mark space ratio in 32 steps. The mark space ratio of the laser signal decides about the mark space ratio of the recovered clock on the DORIC and therefore influences the module timing. Due to the PiN gain stage internal feedbacks on the DORIC, which automatically adjust the PiN signal discriminator thresholds by maintaining a duty cycle of 50% and due to the DORIC delay-lock-loops, which automatically adjust the data recovery sampling positions by keeping the recovered clock duty cycle close to 50%, only laser current and MSR settings have to be adjusted to reasonable values.

On the optoboard to BOC optical transmission (RX) side the VCSEL light output powers can be steered by the VDC control current I_{set} , which is determined by the control voltage V_{Iset} . Since a common V_{Iset} is used for all VCSEL diodes of an optoboard the laser output power cannot be controlled per channel, but per optoboard. The data sampling positions for the PiN signal are determined by a RX delay

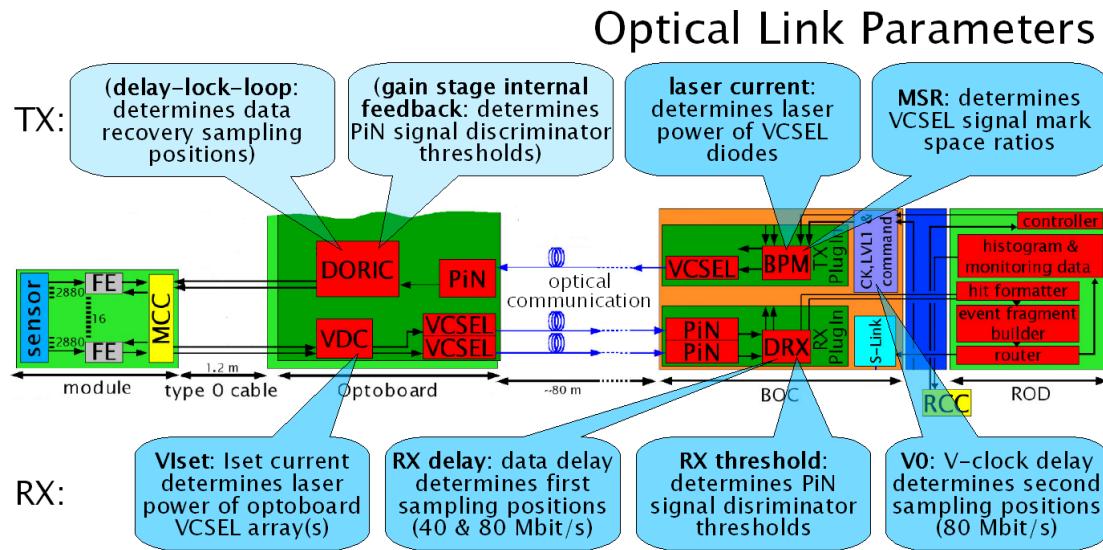


Figure 6-1 Parameters of the readout chain influencing the optical data transmission quality

parameter per channel, which delays the corresponding data stream on the DRX with respect to the sampling position in 25 steps. The RX threshold parameters on the DRX are used to set the PiN signal discriminator thresholds per channel in 256 steps. The second data sampling positions of the PiN signal, which are only used in 80 Mbit/s transmission mode, are determined by the BOC common V0 parameter. It allows to delay the BOC V-clock, which determines the second sampling position, with respect to first sampling position determining B-clock in 50 coarse and 256 fine grained steps.

The channel-wise adjustable TTC data delays (not shown in Figure 6-1) on the BPM influence the phase of the TTC data going to the modules and thus also the phase of the data coming from the modules. They allow individual module timing, but the RX delay parameters have to be readjusted if the module timing is changed. Since the second sampling position is tuned with respect to the first sampling position a readjustment of the V0 parameter is not necessary if the module timing is changed and the RX delay is adapted.

6.1.1 BOC Scans and Laser Signal Shape

Basic study of the optical link influences of these parameters was performed on a laboratory setup similar to the sketched in Figure 6-1. Modules, which have been mounted in a test box for the ATLAS Combined Testbeam (CTB), are connected by Type0 cables to a PP0 test board. The CTB modules are cooled by a chiller through cooling loops integrated into the test box. More details about the CTB test box can be found in [REI06]. As alternative to the CTB modules also single modules with thermal coupling to a metal base are used. The PP0 test board provides passive electrical connections between the modules, an optoboard mounted on the PP0 test board as well as LV, HV and optoboard power supplies. An extended description of the PP0 test board is given in [DOB04]. An Agilent E3646A remote sensing power supply is used to provide the LV to each module and an eight channel ISEG HV module is used to provide the sensor bias voltages. Optoboard supply voltages are provided by a SC-OLink. The SC-OLink and the ISEG module are controlled by a DCS PC. Three 32 m long radiation tolerant optical Draka GRIN50 8-way fiber ribbons are used to connect the optoboard with the readout crate. The readout crate is equipped with a RCC, a ROD and a BOC with two RX and one TX-Plugin. To operate the setup the Pixel Calibration Software STcontrol is executed on the RCC.

The optical data transmission from the ROD TX-Plugins to the optoboards is very robust due to gain stage internal feedback and delay-lock-loop features of the DORIC. A measure for the output laser power of the TX-Plugin VCSEL array is the optoboard PiN current. As the PiN current is measured per optoboard it gives the sum of the 8-way PiN array light powers. Measurement of the individual laser powers is possible by switching on individually the VCSEL channels. Input shape measurements with a loop-back connection [DOP07] show that laser current setting between 0x80 and 0xFF result in usable laser signal shapes. To increase the VCSEL lifetime a standard value of 0xA0 is used instead of the highest laser power. This results in an average optoboard PiN current of ~ 0.65 mA per channel. Due to the decreasing responsivity of the optoboard PiN diodes with irradiation an increase of the TX-Plugin VCSEL laser output power will be necessary.

A measurement of the maximal difference in the positive pulse width of the DORIC output clock versus the BPM MSR setting [DOP07] shows a dependency of the optimal MSR setting with minimal positive pulse width difference from the TX-Plugin VCSEL laser power. For the standard VCSEL setting value 0xA0 an optimal MSR setting of 0x13 was determined. In the final system the verification of an error-free TX-Plugin to optoboard optical communication, independent of the optoboard to RX-Plugin optical data transfer is not straight forward, since only the module LV currents can be used for feedback. High transmission error rates can be diagnosed by abnormal module LV current consumptions for configured modules, caused by faulty configuration data received by the module. However a small amount of bit-flips in the configuration data (if not at certain positions) do not change the current consumption significantly. Thus only a non-ambiguous sequence of bits that dramatically changes the module current consumptions (like the reset of a configured module) can be used to precisely measure the error rate. The drawback is that these bit patterns are short and should be repeated many times to determine the error rate accurately.

With a working TX-Plugin to optoboard optical communication the measurement of the optoboard to RX-Plugin error rate is much easier. A bit pattern can be sent to the MCC FIFO. By setting the MCC into data taking mode and sending a trigger command the MCC is initiated to build an event from the FIFO bit pattern by adding a module header, the BCID counter value and headers for the 16 FEs. Due to the added BCID this method has the drawback that the returned pattern is not fully predetermined and the BCID should be ignored in the error rate analysis. This can be avoided by resetting the MCC after sending the bit pattern to the MCC FIFO. This ensures the MCC is not in data taking mode and ignores the sent trigger. In this procedure the trigger is only used to start the ROD data taking. Sending a 'readFifo' command to the MCC causes the FIFO content to be sent out through the optical link and can then be compared to the reference bit pattern on the ROD. This method has the drawback that the FIFO content can be transmitted only in 40 Mbit/s mode, but not in 80 Mbit/s or 160 Mbit/s. Thus the standard BOC scan implemented in STcontrol uses the first method with ignoring the BCID bits. It results in a reference bit pattern of 1600 bits, ten times repeated, giving a minimal error rate limit of $\sim 6 \times 10^{-5}$.

In Figure 6-2 an example of a reference bit pattern sent to the MCC is shown. Each of the three histograms on the left shows the ten overlayed bit patterns received by the ROD for the 25 possible RX delay settings on the y-axis. The number of '1'-bits is color coded so that a yellow-white bit patterns means that the same bit pattern was read back ten times. Other colors in the bit pattern indicate bit-flip errors in the data transmission. The lower histogram shows the results for a RX threshold value of 50, the middle one for a threshold value of 130 and the upper one for 250. The lower histogram shows mostly '0→1' bit flips as the discriminator threshold is set too low. In the middle histogram bit-flips are observed in a limited RX delay range and the optical data transmission is error-free outside of this range. In the upper histogram mostly '1→0' bit-flips can be observed due to an excessive threshold setting. By comparing the reference bit pattern to the ROD measured bit patterns the total number of bit-flips can be calculated for each RX delay and RX threshold setting combination. The RX threshold versus RX delay BOC scan histogram on the right side of Figure 6-2 shows color-coded the amount of bit-flip errors for the scanned {RX delay, RX threshold} combinations. The white error-free regions indicate {RX delay, RX threshold} combinations with a bit-flip error rate $< 6 \times 10^{-5}$.

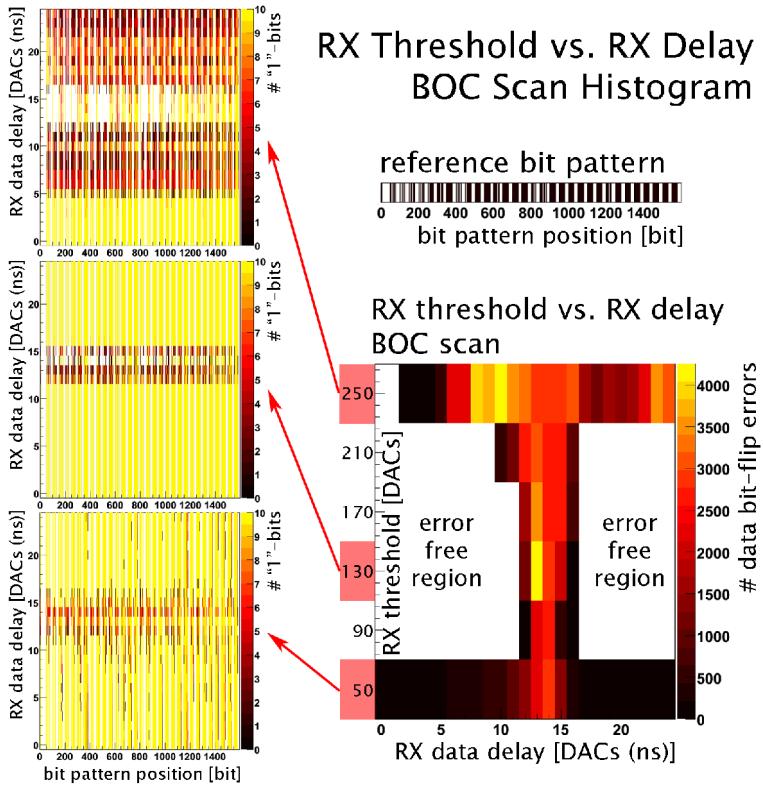


Figure 6-2 Measurement of the optical communication data quality with a RX threshold versus RX delay BOC scan

The pattern of the BOC scan histogram is illustrated in Figure 6-3. The upper and lower threshold error bands are caused by bit-flips if the discriminator threshold is close to the low plateau ($0 \rightarrow 1$) or close to the high plateau ($1 \rightarrow 0$) of the PiN output signal. Using a RX delay, which sets the sampling position to the edges of the PiN laser signal is the reason for the delay error band. Here bit-flips in both directions are possible. The saturation error regions are a consequence of the not rectangular PiN output signal. Out of the form of the error-free region, limited by the different error regions, it is in principle possible to extract the laser signal shape as measured by the PiN diode. The vertical flip between the signal shape shown in the BOC scan and the signal shape shown on the right side of Figure 6-3 is caused by an increasing data delay with increasing RX delay value. This effectively shifts the sampling position to an earlier sampling time with increasing RX delay value.

Increasing V_{Iset} increases the VCSEL laser output power, leading to an increase of the amplitude of the RX-Plugin PiN output signal. The dependency of the different BOC scan error regions and the error-free region from the optoboard V_{Iset} is shown in Figure 6-4. For this optical link the pulse shape is slightly different from the pulse shape presented in Figure 6-3, since an additional error region similar to the saturation error regions exists right of the delay error band at the high threshold error band. This indicates that the falling edge of the pulse falls less steeply at the beginning before it falls as steeply as in the Figure 6-3 pulse shape. For the two lowest V_{Iset} settings all error regions are visible in the BOC scan histograms, whereas in the histograms at higher V_{Iset} the high threshold error band is out of the RX threshold dynamic range.

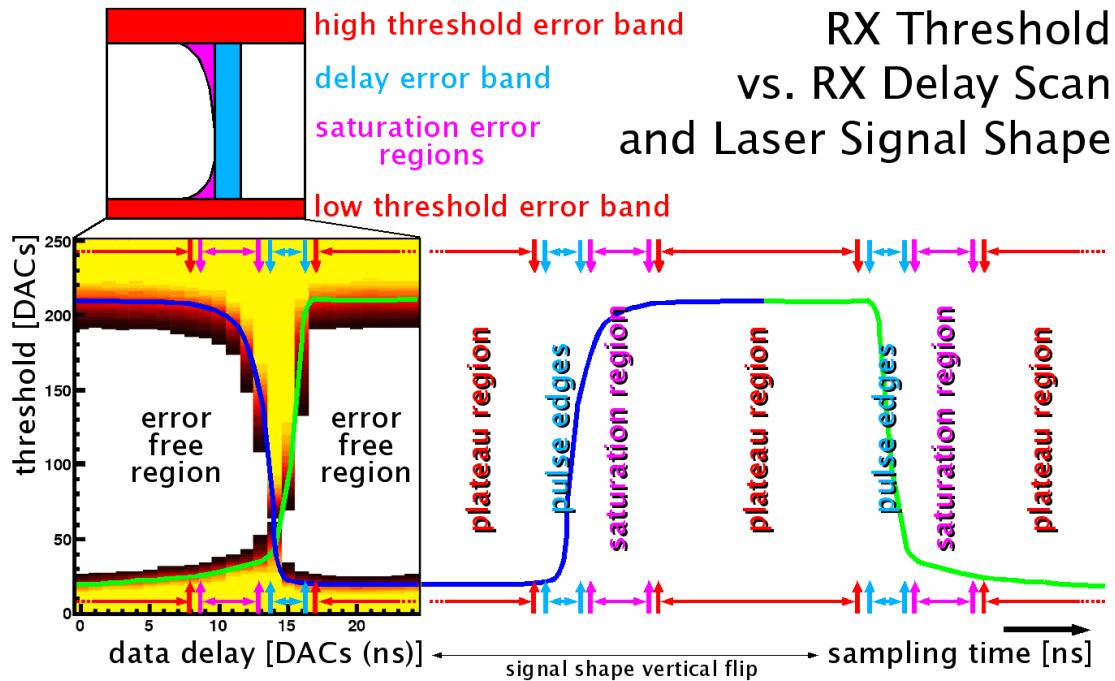


Figure 6-3 Laser signal shape of the optoboard to RX-Plugin optical communication measured with the BOC RX-Plugin

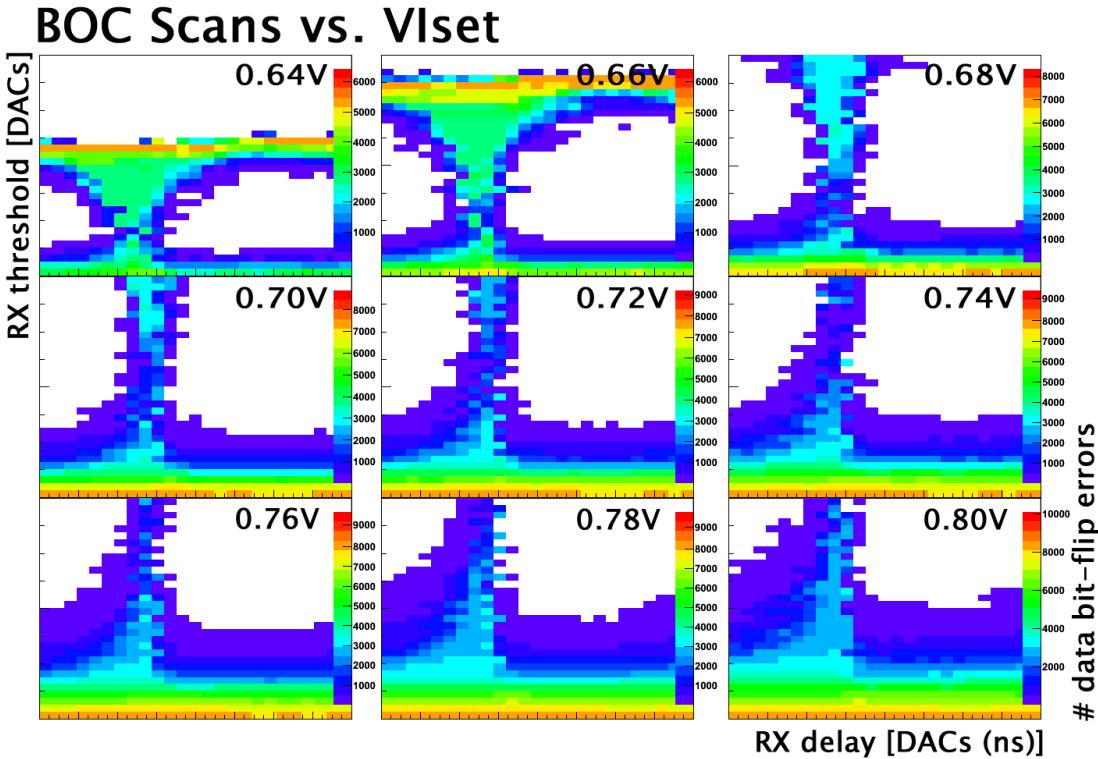


Figure 6-4 Change of the error regions and the error-free region of BOC scans with V_{lset}

The high threshold error band increases for the possible measurement region (0.63 – 0.67 V) linearly with ~ 3600 DACs/V. A 3D contour plot illustrating the surface of the error-free region in the {RX delay, RX threshold, V_{Iset} } parameter space is presented in Appendix A Figure A-16. The position of the delay error band is stable against changing V_{Iset} . This means the phase of the PiN signal does not change with increasing laser power. In the left plot of Figure 6-5 the delay error upper edge positions of four different modules, each measured at two different PP0 test board channels, are presented for V_{Iset} values between 0.63 and 0.8 V. Due to the change of the PP0 channels the two measurements of a module use the same Type0 cable but different optoboard channels, different optical fibers and different RX-Plugin channels. The results indicate a module dependency of the delay error band due to the different Type0 cable lengths but no optoboard channel dependency. BOC scan measured with different Type0 cable lengths [ROT06] (see Appendix A Figure A-17) result in slope of ~ 6.6 ns/m. No significant module, optoboard or RX-Plugin channel dependencies are visible in these measurements.

The right plot of Figure 6-5 shows the increase of the minimal error-free threshold value with increasing V_{Iset} for four modules, each measured at two different optoboard and RX-Plugin channels. This shows that the low level of the PiN diode signal increases linearly with the laser power. A linear fit results in a slope of ~ 800 RX threshold DACs/V. Besides for PP0 channel 4 the curves of the optical links show low differences between the two different connected modules with different Type0 cable length measurements. To investigate the dependency of the laser power seen by the PiN diode from the length of the optical fiber the 32m fiber is replaced with a ~ 12 m long fiber and the measurement of module 510532 is repeated for three V_{Iset} values. No significant increase of the laser power from the low level PiN signal is observed.

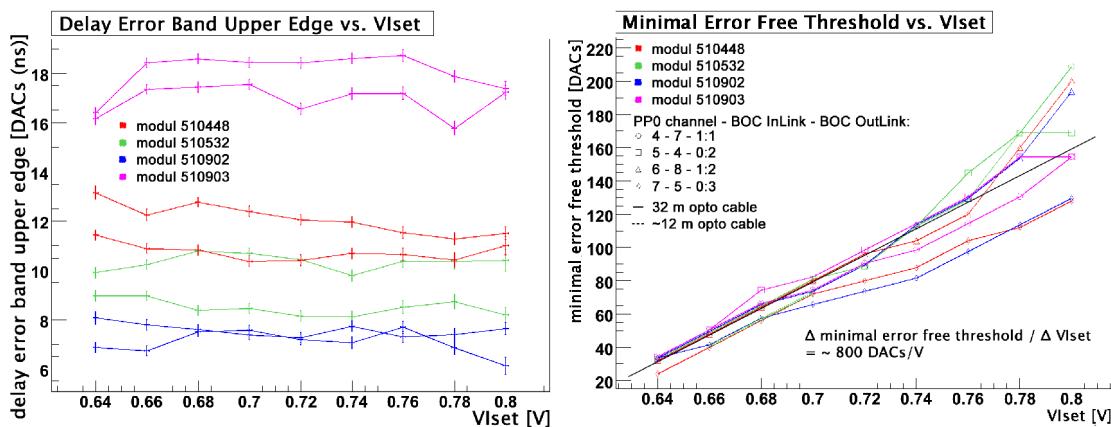


Figure 6-5 Delay error band and low threshold error band dependency from V_{Iset}

A Tektronix¹⁶⁹ oscilloscope with P6701B optical to electrical converter and a MT-8 to single fiber fanout were used to measure the laser power dependency from V_{Iset} . The investigated modules were set to XCK/2 mode returning a 20 MHz clock on the DTOs. The measured values were averaged over 10,000 signal cycles. In the top plot of Figure 6-6 the power amplitude of the laser signal versus V_{Iset} is shown for four optical links measured twice with different channels of the optical fanout. Excluding

169 Tektronix Inc., Beaverton, OR, USA » www.tek.com

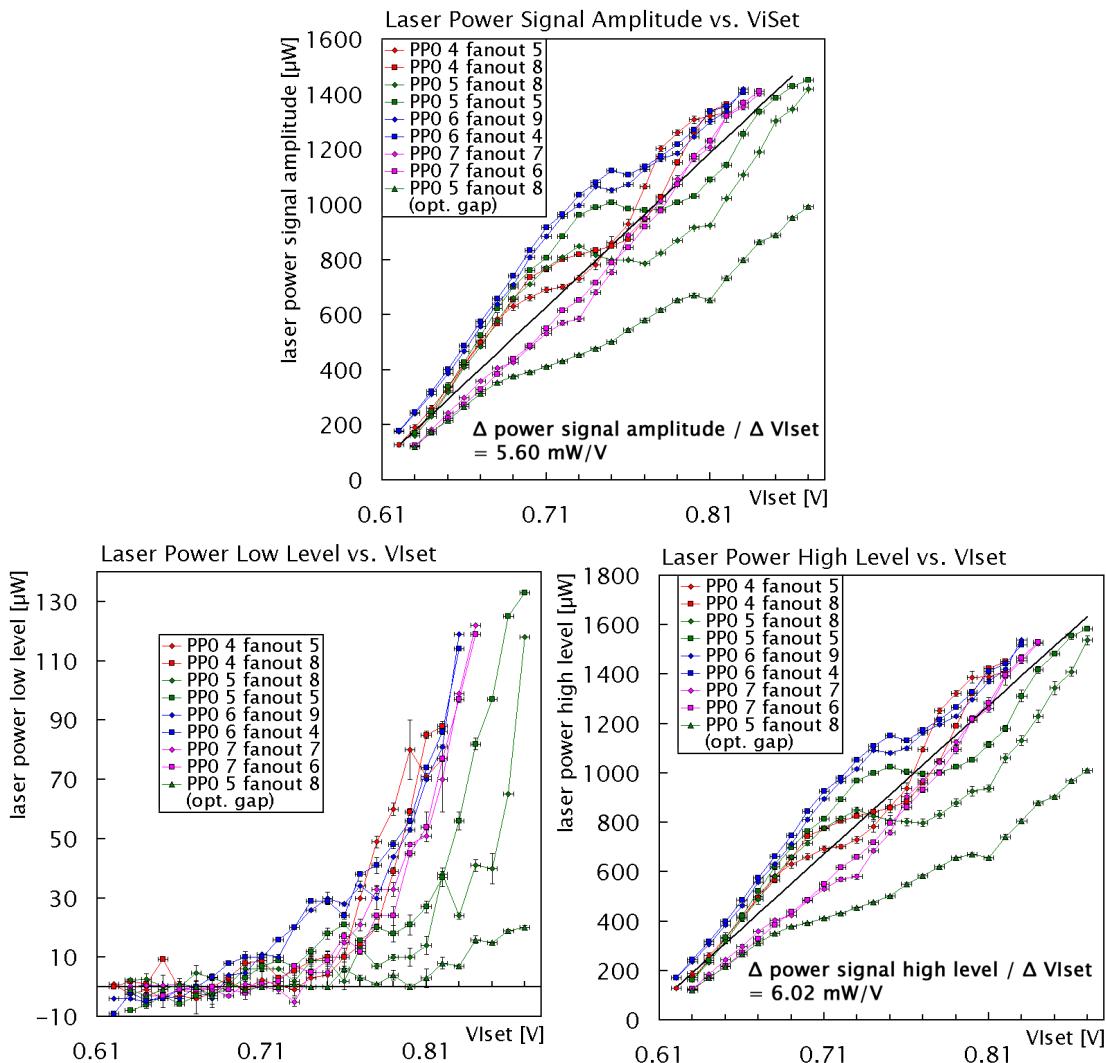


Figure 6-6 V_{set} dependence of the laser power signal amplitude, low level and high level

PP0 5 only small differences for different fanout channels for the same PP0 channel are observed. Probably, a non optimal optical coupling (dust or different distance) between the fanout and the fiber is responsible for the difference. For PP0 7 the laser amplitude increases linearly with V_{set} , whereas PP0 4-6 show between 0.73 and 0.77 V a kind of saturation effect at power levels of about $1.0 \pm 0.20 \text{ mW}$. Since the maximal average operating input optical power of the optical probe is 1 mW probe saturation can be assumed. An additional measurement of PP0 5 is performed with an optical gap between the fiber and the fanout to limit the maximal power amplitude to 1 mW. The saturation effect is not visible in this measurement indicating that the measurement problem around 1 mW is not caused by the laser signal itself. Why the temporary saturation effect is not observed for PP0 7, why the curves continue above the effect with the same slope as below and why for different PP0s the effect is observed at different powers is not understood yet. Repetitions of the measurements in decreasing V_{set} direction show no significant differences to the presented results nor indications for a hysteresis effect. A linear fit to all curves without the optical gap

measurement results in a slope of 5.60 mW/V. For only PP0 7 measurements the fit results in a slope of 6.22 mW/V. The lower plots in Figure 6-6 show the laser power signal low level and high level. From the BOC scan minimal threshold measurement a linear increase of the laser signal low level is expected. But the shown non-linear increase is not responsible for the effect seen in the amplitude. The signal high level clearly shows the effect with the same characteristics described for the amplitude. The linear fit without the optical gap measurement gives a slope of 6.02 mW/V and a value of 6.69 mW/V for PP0 7 only.

The V_{Iset} dependency of the laser signal low and high level widths are shown in Figure 6-7. A slight decrease of the low level width and a slight increase of the high level width with increasing V_{Iset} are observed. The absolute slope for both cases is about 4.7 ns/V above 0.65 V. The errors of the average low level and high level widths indicate a jitter of the 20 MHz signal of about 1 ns. Below V_{Iset} values of 0.65 V the jitter increases with decreasing V_{Iset} . A summary of the BOC scan measurement and the optical probe measurement results is presented in Table 6-1.

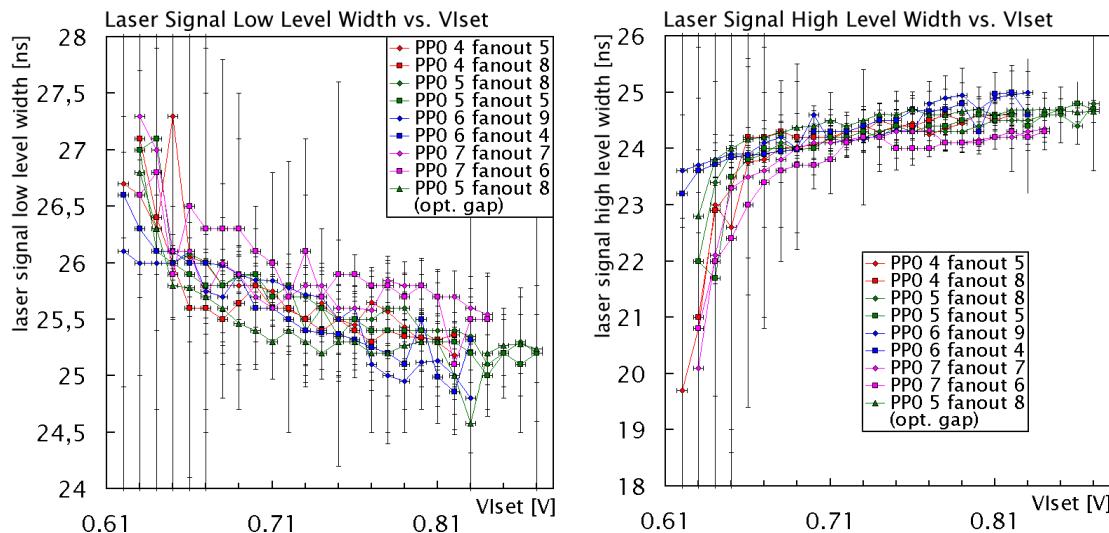


Figure 6-7 V_{Iset} dependence of the laser power signal low level and high level widths

error region:	BOC scan measurement slope:	signal shape measurement slope:
high threshold error band	~ 3600 DACs/V	~ 6.02 mW/V
low threshold error band	~ 800 DACs/V	not linear
delay error band	~ 6.6 DACs(ns)/m	~ 4.7 ns/V

Table 6-1 Summary of BOC scan and optical probe laser signal measurement results

6.1.2 Optical Parameters Tuning Strategies

The choice of the {RX delay, RX threshold, V_{Iset} } operation combination in the error-free region is driven by the most sensitive parameter V_{Iset} . Due to the high V_{Iset} dependency of the high threshold error band, V_{Iset} is adjusted to a value which sets the high threshold error band position away from the threshold dynamic range, but makes sure that the low threshold error band and the lower saturation error region limit the error-free region in the threshold dynamic range as little as possible. A large error-free region in the threshold dynamic range and stability with V_{Iset} changes can be expected. The stability of the delay band error and growth of the low threshold error band and the saturation error region with increasing V_{Iset} are shown in Figure 6-8.

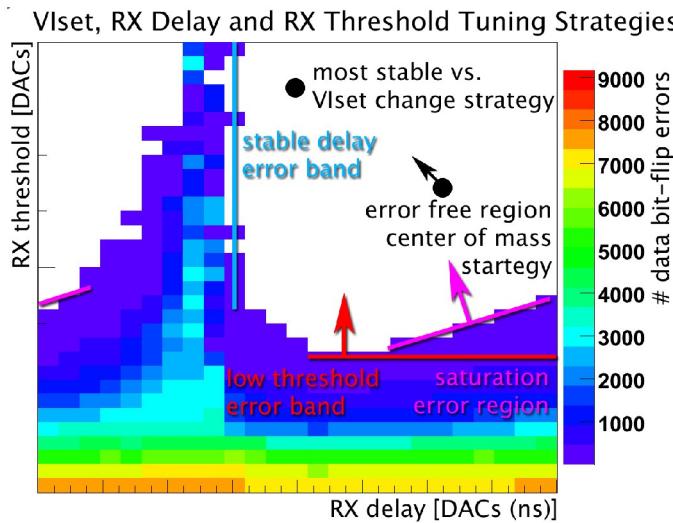


Figure 6-8 Change of the error-free region with increasing V_{Iset} and two different tuning strategies

Two different strategies to automatically adjust RX delay and RX threshold were investigated. The first method sets both values into the center of mass of the measured error-free region. This combination is as far as possible away from all combinations with data transmission errors. Unmeasured threshold values above the dynamic range are assumed not to be error-free. As the error-free region shrinks from the low threshold and high delay direction with increasing V_{Iset} this combination is not the most stable. If V_{Iset} increases too much the parameters must be readjusted to lower delay and higher threshold. The second strategy sets the operation point directly to higher threshold and lower delay values and thus provides higher stability against V_{Iset} changes. Since the delay error band is stable against V_{Iset} and only changes with changing TTC delay, Type0 cable or optical fiber length, the delay setting can move without problems close to the delay error band. Therefore the upper edge of the delay error band is determined by searching the threshold with minimal delay error band width and determining at this threshold the delay at the transition from error to error-free. The RX delay is set typically 4 ns higher of this edge. The threshold is set to the minimal delay error band width threshold. The minimal width of the delay error band

close to the upper threshold dynamic range edge shows that the high threshold error band is not directly above the dynamic threshold range. The increase of the threshold setting lowers the tolerance against decreasing V_{Iset} values and increases the tolerance against increasing V_{Iset} values. Due to the higher V_{Iset} dependency of the high threshold error band compared to the low threshold error band dependency, the increasing V_{Iset} tolerance benefit is higher than the decreasing V_{Iset} tolerance loss. Thus this tuning strategy is used as default.

6.1.3 80 Mbit/s BOC Scan

Operation of the optical link in 80 Mbit/s mode requires tuning of the V0 parameter, which delays the BOC V-clock versus the B-clock, setting the second sampling position with respect to the first sampling position. A 40 Mbit/s RX threshold versus RX delay BOC scan and the corresponding 80 Mbit/s BOC scan histograms are presented in Figure 6-9. In the previously discussed 40 Mbit/s RX threshold versus

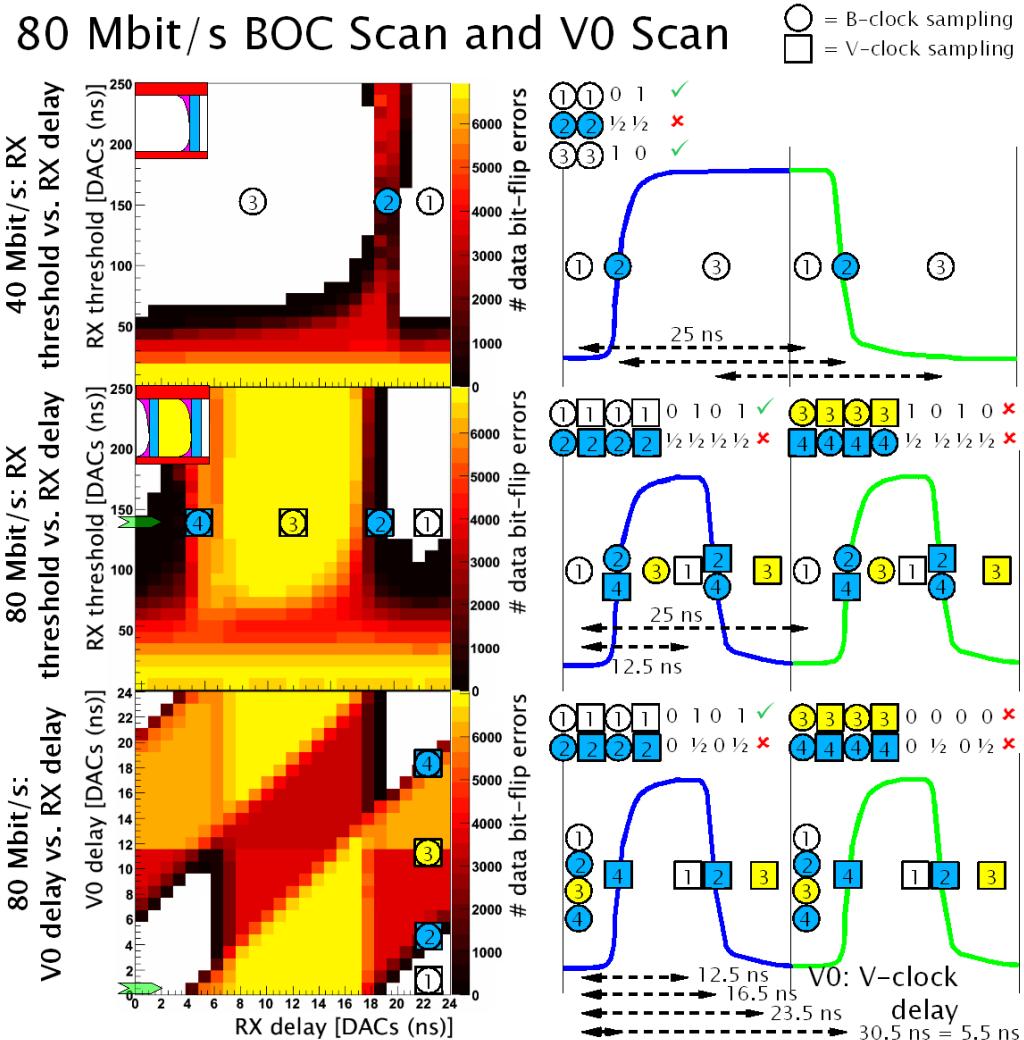


Figure 6-9 Schematic view of the 80 Mbit/s BOC scan and the V0 scan

RX delay threshold scan on the top left the working points ① and ③ result with a reasonable RX threshold in an error-free optical communication. The sampling position of the laser PiN signal are sketched on the top right. As only the rising edge of the 40 MHz B-clock is used for sampling the bit shift between ① and ③ conserves the data stream order. The start of a data stream is indicated by a header bit sequence thus the bit shift does not matter. Only if the RX delay is set into the delay error band (②) the laser data stream cannot be converted correctly, since the sampling is performed on the signal edges.

In the 80 Mbit/s mode the pulse length of a bit is only 12.5 ns instead of 25 ns for 40 Mbit/s. This means that two signal transitions fit into the 25 ns BOC scan time window. Therefore also the raising edge of the V-clock is used for data sampling. With default settings (V_0 delay = 0) the V-clock is the inverse B-clock, thus the difference between the two clock trailing edges is 12.5 ns. In the middle right sketch the B-clock sampling position is indicated by ① and the corresponding V-clock sampling position by ①. It results in the correct conversion of the data stream. If the RX delay is adjusted in a way that ② is sampling at the edge of the signal the second sampling ② is performed on the 12.5 ns delayed signal edge. As a consequence a second delay error band with 12.5 ns lower RX delay value can be observed in the middle left BOC scan histogram. However the sampling positions ③ and ④ are sampling on the signal plateaus, but the order of the sampling position is reversed compared to ① with a 12.5 ns higher RX delay setting. For the sketched '0101' bit pattern this looks like a bit shift as in 40 Mbit/s mode, but the output bit pattern of the serial formatter FPGA '1010' is the result of a pairwise bit swap. For example the data stream linker header '111010' gives the formatter output '110101' if the order of sampling positions is swapped. In which order the sampling positions are combined in the formatter can be changed by the BOC mode. This allows to reconstruct correctly the bit pattern from sampling positions ③ and ④, but at the same time the serial formatter output bit pattern from sampling positions ① and ① is pairwise swapped. Sampling positions ④ and ④ are set by a RX delay value 12.5 ns lower than for ② and ②, thus both samplings are performed at the signal edges as for ② and ②, but the B-clock and V-clock sampling positions are swapped.

A V_0 delay versus RX delay BOC scan histogram at a fixed RX threshold is shown at the bottom left. The histogram slice at $V_0 = 0$ is the same slice of the 80 Mbit/s RX threshold versus RX delay histogram at the chosen RX threshold. Therefore the sampling positions ① and ① are identical to the 80 Mbit/s RX threshold versus RX delay scan positions. With changing V_0 delay the B-clock sampling position is stable and only the V-clock sampling position changes as shown in the bottom right sketch. At a V_0 delay value which results in sampling positions ② and ② the V-clock sampling is performed at the signal edge leading to errors in the data stream. At the V-clock sampling position ③ the second data signal pulse (in this case a '1') is not sampled at all and the resulting formatter data stream is 1st, 3rd, 3rd, 5th, 5th, ... bit of the PiN data stream. The change of the number of data bit-flip errors next to ③ and ③ in the V_0 scan histogram is caused by B-clock to V-clock raising edge delays of higher than 25 ns (V_0 delay > 12.5 ns) which result in effective delays < 12.5 ns and a formatter data stream of 1st, 1st, 3rd, 3rd, 5th, ... bit of the PiN data stream. At ④ the V-clock sampling is on the edge of the PiN signal. For higher V_0 delay values the V-clock sampling position is again on the B-clock opposing PiN signal plateau resulting in an error-free optical communication. The combined error-free regions of the V_0

BOC scan form a parallelogram with the optimal working point at the center of mass of the parallelogram. For the shown example the optimal tuning is a RX delay value of 0x18 and a V0 delay value of 0x1. For the BOC B-clock phase 0xB the V0 delay value 0x1 is the expected value, whereas V0 delay values 0x0 are seen for B-clock phases of 0xC.

6.2 Bi-stave System Test

The first phase of the ATLAS Pixel System Test began in spring 2006 and a setup, capable of operating the modules of one stave in parallel, was assembled in the SR1 cleanroom at CERN. A schematic view of the setup components is presented in Figure 6-10. A bi-stave is placed in a heat isolated dry box, which is flushed with dry air to prevent condensation on the chilled staves. The cooling of the bi-stave is provided by a connection to the SR1 evaporative C_3F_8 cooling plant (see section 6.2.1). The C-side of the 'down' stave (S1) is connected to a capillary and serves as inlet for the C_3F_8 coolant. The C-side of the 'up' stave (S2) serves as exhaust and the two cooling pipes are connected at the A-side. Four pressure sensors are measuring the coolant pressure at all four stave cooling pipe ends. Humidity and temperature in the box are monitored with Xeritron and Honeywell humidity sensors connected to an ELMB, which is readout by the DCS.

Two approximately 80 cm long Type0 cables, connected through a passive extension board, are used to link each module of a half-stave to the corresponding PP0 test board Type0 connector. The PP0 test boards replace the PP0 in the final detector and are used to route data lines between modules and the optoboard as well as the supply voltages and NTC lines to the optoboard and the Type0 connectors for up to seven modules. The six modules of the C-side are connected to the PP0 test board equipped with a D-type optoboard, whereas the six A-side and the central module to a PP0 test board equipped with a B-type optoboard. Therefore the C-side modules can be readout in 40 and 2*40 Mbit/s mode and the other modules additionally in 80 and 2*80 Mbit/s mode. The PiN arrays of the optoboards are connected with MT-8 connectors via ~2 m optical 8-way ribbon fibers to a 16-way MT-16 connector in the laser interlock box. The door of the interlock box closes an interlock switch, which is connected in series to additional interlock switches in laser safety covers for the optoboards. About 50 m long radiation tolerant optical cables are used to complete the data connection between the laser interlock box and the readout crates.

The electrical connections between the PP0 test boards and the NTC/OPTO, LV and HV Type2 Lemo-F connectors are provided by ~4 m long so-called 'poor-man service quarter panel' cables. The PP2 NTC-MOD/OPTO box and the LV-PP2 regulators are located about 12 m away from the dry box in a PP2 station, whereas the HV Type2 cables are directly routed to the rack area outside of SR1. The rack area consists of the Pixel readout, interlock and power supply components (see sections 4.6, 4.7 and 4.8) as they are installed in the ATLAS PP3 stations and the ATLAS counting room racks. For the bi-stave setup a readout crate with four BOC/ROD pairs is used, even though only two pairs are necessary to readout the stave in all possible bandwidth modes. For the sensor bias voltage generation two ISEG HV supplies with in total twelve 16-ch

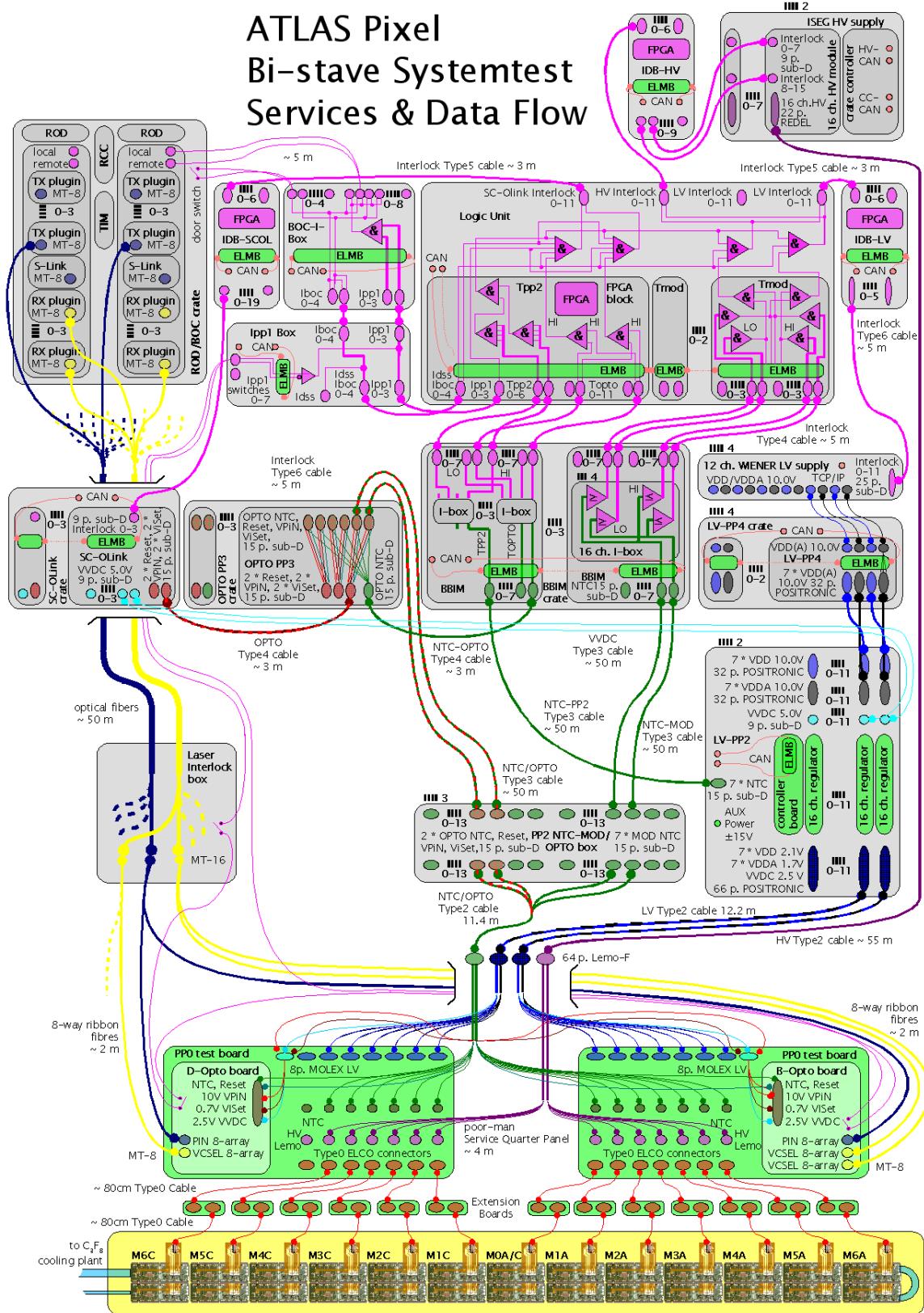


Figure 6-11 Schematic view of the Pixel bi-stave System Test setup

modules are used, but only one module is necessary for the connected stave. Since no HV-PP4 was available for the System Test the HV Type2 cables are connected to the ISEG modules resulting in a modularity one instead of modularity six or seven as with the PP4. In the rack area in total four LV-PP4s with attached WIENER power supplies are tested with four WIENER channels of one power supply and one PP4 necessary for the stave operation. For the supply of the optoboards the Type2 power supply lines are separated in one of the four OPTO PP3s in the OPTO PP3 crate and are routed through OPTO Type4 cables to one of the four SC-OLinks. VVDC is routed through Type3 cables to the LV-PP2, which contains the two necessary regulator boards.

The monitoring of the module, optoboard and PP2 temperatures as well as the interlock signal generation is provided by a BBIM. For the monitoring of the environmental sensor a BBM is used. The interlock signals are assigned to power supply channels by a logic unit and an IDB of each type. The laser interlock switches are integrated into the interlock system by the BOC-I-Box for the readout crate door switches and the Ipp1 box for the laser interlock box and the optoboard cover switches. Four DCS PCs are used to control and monitor the services. One PC runs the ISEG HV OPC server/client and the FSM. On a second machine the WIENER LV OPC server/client and the entire DCS project is running. The complete DCS project is executed at the third DCS computer as well, but is mainly used as interface only. ELMB OPC server/clients for the BBIM, the PP4s, the PP2s and the SC-OLinks are executed on the third PC, which runs also the RDB¹⁷⁰ manager for archiving of the DCS datapoints. The fourth DCS computer runs ELMB OPC server/clients for the interlock IDBs, the logic unit, the BOC-I-Box and the Ipp1 box. A fifth PC is used to display the DCS GUI¹⁷¹ which is used to operate the DCS and provides steering of the FSM, FIT and SIT. The readout and calibration software STcontrol is executed on the RCC of the readout crate.

6.2.1 Bi-phase Evaporative Cooling System

The cooling of Pixel modules in the System Test is realized with a scaled down version of the ATLAS C₃F₈ bi-phase evaporative cooling system. An evaporative cooling system is mainly used due to the minimal material requirements in the active volume. Advantages of the C₃F₈ coolant are its good thermal transfer coefficient, low vapor specific volume, radiation hardness and that it is non-conductive and non-flammable. The cooling plant is controlled by a PLC¹⁷² and consists of a liquid storage tank, a buffer tank, a compressor and a condenser. The C₃F₈ coolant is held at ~13 bar absolute in the liquid storage tank, cooled by chilled water to ensure that the liquid C₃F₈ is above its saturation point. The amount of the stored coolant is monitored by the PLC with a scale. A filter is used to remove from the coolant any particulate material, which could harm the detector cooling tubes. The cooling plant output pressure is monitored with a pressure sensor. A PLC controlled pneumatic valve allows to cut the C₃F₈ flow in case of a cooling plant alarm condition. Manual valves are used to individually control the flow to three different distribution racks. Two distribution racks are used for SCT assembling and testing and one for the Pixel

¹⁷⁰ Remote DataBase

¹⁷¹ Graphical User Interface

¹⁷² Programmable Logic Controller

System Test. The input pressure to the Pixel distribution rack can be lowered by a manual pressure regulator valve and is monitored with a PLC connected pressure sensor and a gauge. The Pixel distribution rack is typically operated at full cooling plant output pressure of ~13 bar absolute and the input pressure is only reduced by the input pressure regulator if higher cooling plant pressures are required for the SCT cooling loops. In the distribution rack the inlet coolant runs through an exhaust recuperative heat exchanger, which uses the exhaust vapor-liquid to sub-cool the inlet liquid. This increases the inlet coolant liquid/vapor fraction and thus reduces the necessary liquid mass flow. A manifold with separate mechanical valves provides in total 13 cooling loops. To one of the cooling loops the bi-stave setup is connected with a capillary at the inlet. The sub-cooled coolant evaporates in the bi-stave cooling pipes and the evaporation heat of the vapor/liquid mixture provides efficient cooling of the bi-stave modules.

ATLAS Pixel C_3F_8 Cooling in SR1

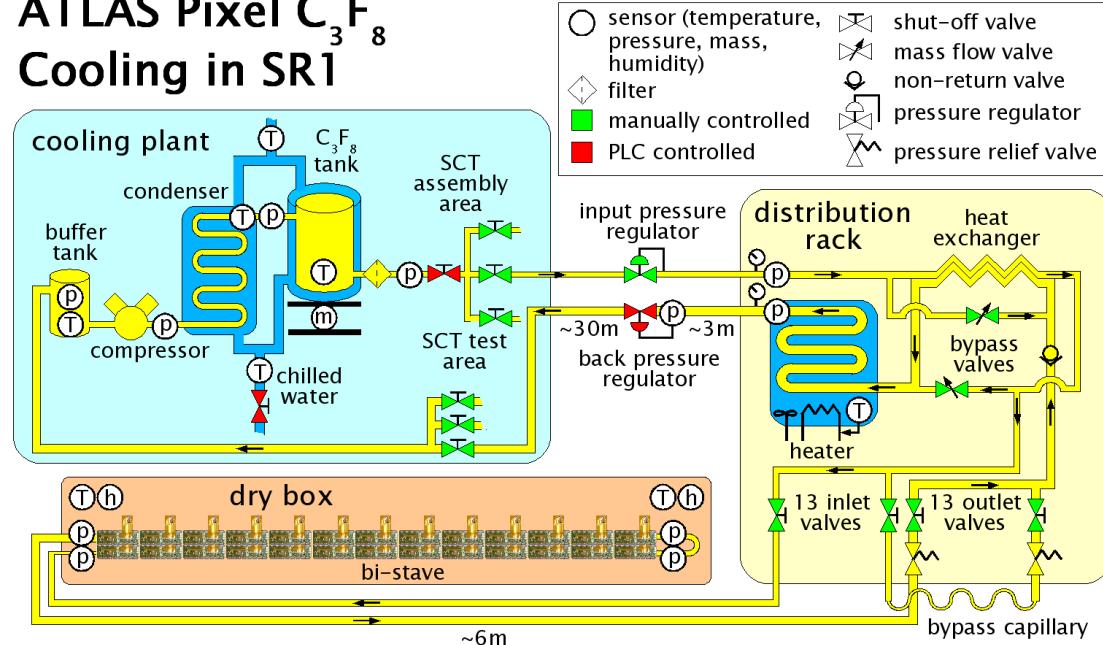


Figure 6-11 Pixel evaporative bi-phase cooling schematic view

The temperature and humidity of the dry box and the pressure at the four bi-stave cooling loop ends are monitored with DCS. Pressure relief valves at the distribution rack outlets are adjusted to a relief pressure of 4 bar absolute to avoid over-pressures at the thin detector cooling pipes. In order to meet the mass flow requirements of the cooling plant another cooling loop is used with a bypass capillary to increase the total mass flow especially during the startup of the bi-stave cooling loop and when the SCT cooling loops are closed. Two bypasses in the distribution rack with mass flow valves serve the same purpose. One bypass leads from the rack inlet to the inlet of the heat exchanger on the exhaust side. The second bypass is located between the heat exchanger exhausts of the inlet and exhaust side. A non-return valve between the bypasses and the outlets protects the cooling loops from pressurization through the exhaust side. At the exhaust of the distribution rack a heater is used to evaporate the remaining liquid in the vapor/liquid mixture. This prevents evaporation in the exhaust

tubes back to the cooling plant by increasing the vapor temperature above the room temperature dew point. A heat exchanger is placed in a coolant liquid, which is warmed by an electric heater. The temperature of the heater and the heating circuit are controlled and monitored by the PLC. The back pressure of the rack can be monitored with a gauge and is measured with a pressure sensor, which is used by the PLC to steer the back pressure regulator. By adjusting the back pressure the saturation pressure in the bi-stave and thus the evaporation temperature can be set to steer the cooling power. For the Pixel cooling loop back pressures between 2.1 bar and 1.4 bar absolute are used.

The superheated vapor is received at the cooling plant by the buffer tank, which is hold by a 22 kW oil-free compressor at about 0.7 bar absolute. The room temperature low pressure C_3F_8 vapor from the buffer tank is compressed and the hot high pressure vapor is condensed in a chilled water condenser. The obtained liquid C_3F_8 is stored in the liquid storage tank. The temperature of the storage tank, the buffer tank, the chilled water input and output as well as the pressures in the condenser, compressor and buffer tank are monitored by the PLC. More details about the cooling system, its performance and operation experiences made with the evaporative cooling system are presented in [WEI07].

6.2.2 Bi-stave Operation and Results

The aim of the bi-stave System Test was to debug in parallel all hardware and software components of the readout chain as well as to understand the mapping of channels through the entire readout and interlock system using a setup as similar to the final system as possible. It was also used to test and qualify the operation of the bi-phase cooling system for the endcap operation, to test the readout in all possible bandwidth modes and to test and extend the DCS and DAQ software to ensure the necessary functionality for the endcap operation is in place. The bi-stave was operated about four months with about ten hours of operation per working day including two hours for starting and stopping the evaporative cooling plant. About one hour after the starting of the cooling plant the input- and back-pressure stabilized, so that the cooling of the bi-stave could be started. After the stopping of the cooling plant about one hour of coolant recovery was necessary to evacuate the coolant from the distribution rack, inlet and exhaust cooling tubes. For the bi-phase cooling system good stability and reliability was experienced. Switch-on, switch-off and emergency switch-off procedures were defined and tested for the cooling operation.

About 2/3 of the operation time was used for debugging of the system including hardware and software problems. The electrical NTC Type1 and module Type0 cable connections at the PP0 test board as well as the Type0 extension boards showed fragile connectivity. Since another connection scheme was foreseen for the endcap System Test the connection were mechanically fixed and no further action was necessary. On the other side several missing and loose electrical connections, for example at the BOC-I-Box, in the rack area could be identified and fixed before the endcap operation started. The mapping of the readout and service chain was understood and inconsistencies with existing documentation solved. In total three staves of two bi-staves where sequentially connected to the bi-stave setup. During the

switch-on of modules peaks with amplitudes up to 1.3 A in the digital current were observed. This behavior was already known from production measurements, but the time constant was prolonged (about seven seconds) compared to the peaks seen during the production. Most probably the current peak is caused by an increased current consumption of the FE inverter blocks (see also section 6.3.1) but the reason for the time constant prolongation, for example if it is caused by a changed RC time-constant or by the PP2 regulating circuit, was not completely understood. Several problems were found with the PP2 regulators. For open sense lines the output voltage of the regulators was equal to the 10 V regulator input voltage. In this state it was not possible to disable the concerning channel by the global KILL or the channel INHIBIT signal. The protection diodes on the regulators did not provide the expected limitation of the output voltage. Thus the risk of applying more than the 4 V CMOS breakdown voltage to the modules existed. These problems of the prototype regulator boards were solved by a revised circuitry on the production PP2 regulator boards. An additional problem of lost synchronization between the FIT DCS regulator trimmer settings and the actual PP2 regulator trimmer settings on the controller board, thus wrong regulator board output voltages, was eliminated by a revised controller board FPGA programming and enhanced DCS FIT command sequences. Good reliability and stability was experienced with the interlock system and DCS. Occasionally a WIENER supply channel switched off and it was shown that the switching was not caused by an interlock signal or short interlock signal peaks but was later identified as a problem of the power supply. The prototype of the FSM was successfully tested and necessary extensions for the endcap operation were defined.

The full readout chain was built and tested up to the ROS. The functionality and stability of the DAQ software was continuously improved and adapted to the needs of the System Test. A new implementation of the BOC scan was successfully tested. The so-called 'fast' BOC scan sets the module into XCK/2 mode and counts during scanning over the RX Threshold and RX delay parameters the logic high to logic low ratio. It is about a factor 25 faster than the 'slow' BOC scan described in section 6.6.1. A comparison between both is presented in section 6.3.4. During calibration scans on some modules it was observed that the digital current of all modules connected to the same optoboard dropped to ~ 450 mA. This current value is different to a module not seeing XCK (~ 250 mA) and a reset of the DORIC recovered the normal digital currents (~ 700 mA). The analogue module currents stayed stable indicating that the modules did not lose their configuration. This effect happened only if particular modules were scanned and returned data to the readout crate. The occurrence probability of this effect was experienced to increase with the data amount returned from this modules. It was mostly seen in 80 Mbit/s readout mode and both, happening for one module at a time and for all modules at the same time, were observed. By exchanging readout components it was figured out that the problem stayed with the formatter 5 in the ROD with exchange of modules, the optoboard, optical fiber routing and BOC. Measurements of the XCK lines at the PP0 Type0 connector showed that the current change is caused by a transition of the 40 MHz XCK to '20 MHz' with a non uniform duty-cycle. This indicated that the DORIC delay-lock-loop lost its lock to the 40 MHz XCK and locked to a non 40 MHz signal. No coincidence of the transition with activity on the laser interlock, DORIC reset, V_{PIN} or VVDC lines were found. Comparing the XCK of different modules showed that the transition happened simultaneously for all XCK signals of an optoboard, but sometimes individual

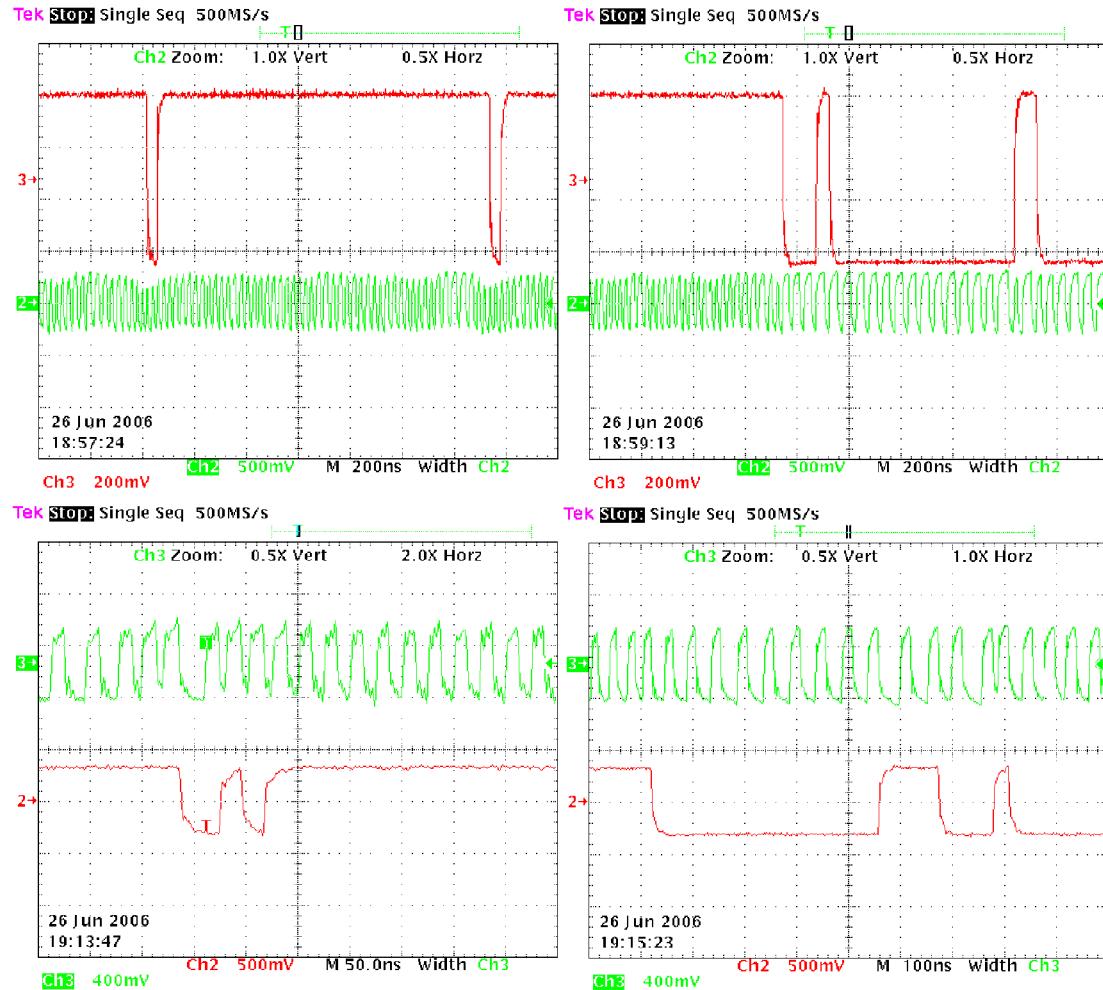


Figure 6-12 Differential probe signal shape measurements of the XCK (green) and DTO (red) lines of a module routed through formatter 5 at the ROD. Left screenshots show the signal shapes before a transition from 40 MHz XCK to '20 MHz' XCK and the right screenshots at the transition caused by a crosstalk between the XCK and formatter 5 data line in the ROD

channels could recover to the 40 MHz signal. In Figure 6-12 differential probe signal shape measurements of XCK and the DTO line of a module connected to formatter five are shown. In the top left screenshot glitches are visible in the XCK signal shape, which coincide with short activity (logic high pulses) on the DTO line. A transition to the '20 MHz' XCK occurs in the right top screenshot in coincidence with a ~ 120 ns long logic high on the DTO line. No effect of a ~ 60 ns long logic low pulse is observed, but the following ~ 100 ns logic low pulse causes a 40 MHz XCK pulse for one clock cycle. The bottom screenshots show closeup views of short logic high DTO pulses before the transition (left) and of longer logic high pulses at the XCK frequency transition. Irregularities in the XCK frequency coincide with logic state transitions of the DTO signal. It was found that a crosstalk between the formatter 5 data line and the XCK line on the BOC causes the XCK irregularities. The XCK line is only used if the XCK is generated by the BOC, thus the effect is not observed if the XCK is distributed to the BOCs by a TIM in the readout crate. As the latter is the only sensible

use case for the detector readout no design changes were necessary and TIMs were installed in the System Test readout crates to solve the problem.

Another readout problem was observed for analogue injection scans. In analogue injection scans with 20 ke^- five of the 13 stave modules showed missing hits in the first mask-step, especially in high FE rows, but not in the ganged pixels of the first mask-step. Two examples of analogue injection scan results are given in Figure 6-13. In both cases some extra hits and occasionally missing hits out of the first mask-step are visible. Since in the FE readout logic hits are read out in decreasing FE row order and missing hits were only observed for the first mask-step the responsible error occurs only in the beginning of a scan, but this is in conflict with no observed errors in the first mask-step ganged pixels with the highest row numbers. In the Connectivity Test after the detector assembly a similar missing hit and extra hit error pattern was found in digital scans, which only occurs at the first digital scan after the optoboard is switched on. For digital scans missing hits are more probably in low FE rows. Thus filling of some module buffers during the optoboard initialization with an improper reset of the module before the scan or data transmission problems at the beginning of scans can be suspected in both cases, but could not be comprehensively proved.

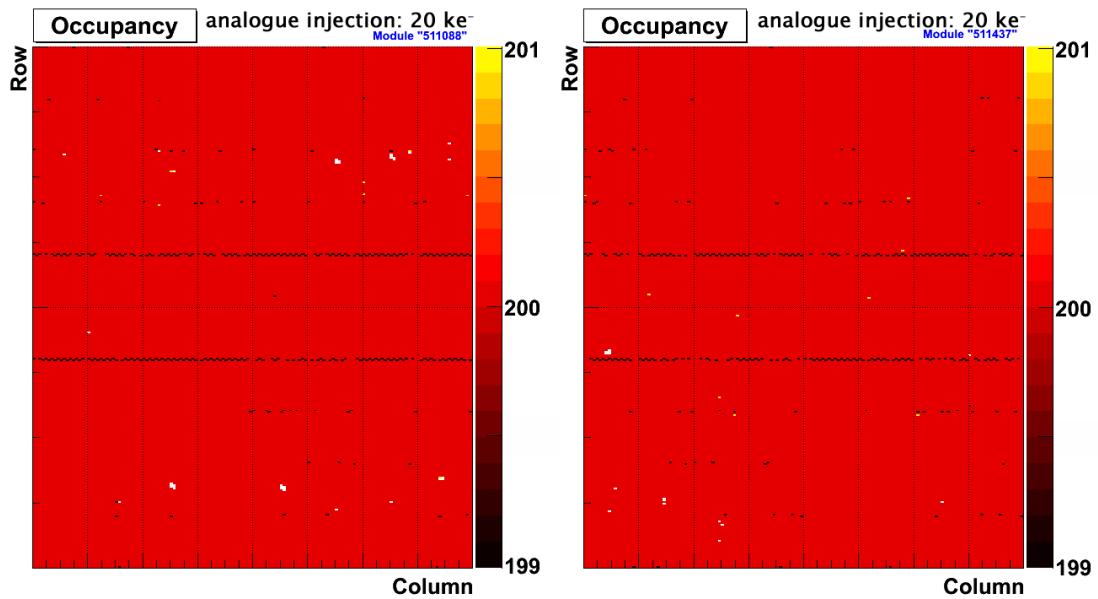


Figure 6-13 Analogue injection scans of two bi-stave modules with missing hits (black spots) in the first mask-stage, some extra hits (yellow spots) and dead pixels (white spots)

Of the available operation time about 14% could be used for system performance analysis involved data taking. This includes tuning of the BOC parameters and digital scans to test the functionality of the system and the modules. Threshold scans were performed with production module calibrations. The complete tuning sequence including GDAC, IF DAC, TDAC and FDAC tuning was performed and threshold scans were taken to verify the tuning results. In Figure 6-14 the threshold tuning results of a module tuned with a TurboDAQ setup, as used in production measurements and described in section 5.2.1, and with the bi-stave System Test setup are shown. The TurboDAQ tuning and threshold measurement were performed at the stave production site in Wuppertal at 5°C . The threshold map shows uniform

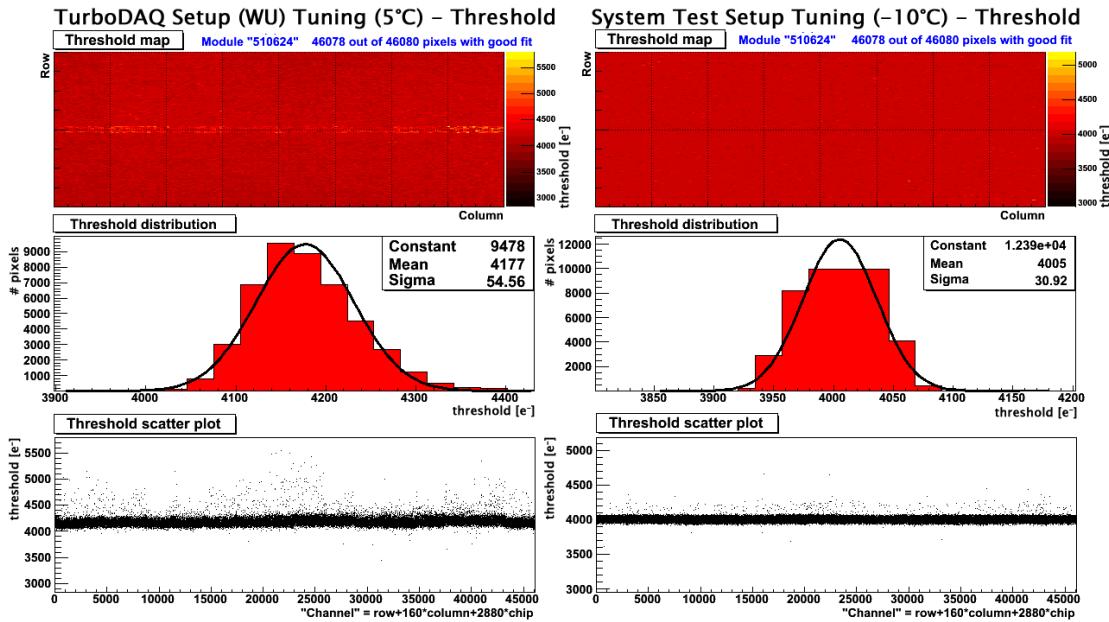


Figure 6-14 Threshold maps and distributions for Module 510624 tuned and measured with a TurboDAQ setup (in Wuppertal) at 5°C (left) and tuned and measured with the System Test setup at -10°C (right)

threshold values, apart from some ganged pixels for which the tuning failed and high thresholds are observed. The threshold distribution shows an average threshold value of 4177 e⁻ with a dispersion of 55 e⁻. The 200 e⁻ excess after tuning, with respect to the intended 4000 e⁻ threshold, are caused as the tuning was performed in antikill mode (see section 6.2.2) but the threshold measurement in normal threshold scan mode and a known tuning problem of TurboDAQ. The scatter plot is flat and shows a tendency to higher threshold outliers to the border FEs, as seen in production measurements. The threshold map of the System Test setup tuned and measured configuration do not show higher threshold values for ganged pixels and is more uniform with a mean threshold value of 4005 e⁻ and a dispersion of only 31 e⁻. This indicates stable voltage supply and temperature conditions during the tuning and the subsequent threshold scan. The distribution of the set TDAC values shows that odd DAC values are not used between 55 and 85 DAC counts, thus a slightly lower threshold dispersion with an improved tuning algorithm may be possible. The noise map and distribution are shown in Figure 6-15 for both tunings. For standard pixel, noise of 181 ± 12 e⁻ is measured with the TurboDAQ setup and due to increased preamplifier capacitive loads higher values for long (200 ± 14 e⁻), ganged (307 ± 35 e⁻) and inter-ganged (202 ± 16 e⁻) pixels. The slight m-shape (over the entire plot width) of the scatter plot indicates higher pixel noise for central FEs known from production measurements. For the System Test setup significantly lower noise values (up to about 30 e⁻) and noise dispersions were measured. The measured standard pixel noise (155 ± 9 e⁻), long pixel noise (181 ± 12 e⁻), ganged pixel noise (302 ± 26 e⁻) and inter-ganged pixel noise (171 ± 14 e⁻) are representative for all seven stave modules for which the entire tuning procedure were performed. The threshold and noise distributions of all these seven modules are shown in Appendix A Figure A-19. In addition to normal threshold scans antikill mode threshold scans were performed. In antikill mode all preamplifiers

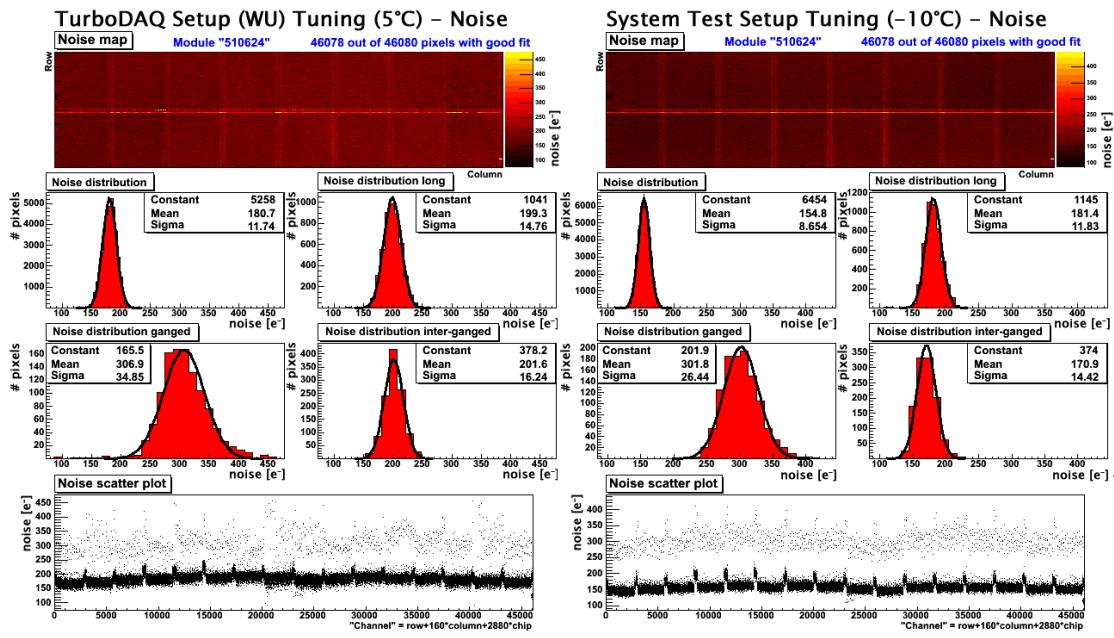


Figure 6-15 Noise maps and distributions for Module 510624 tuned and measured with a TurboDAQ setup (in Wuppertal) at 5°C and tuned and measured with the System Test setup at -10°C

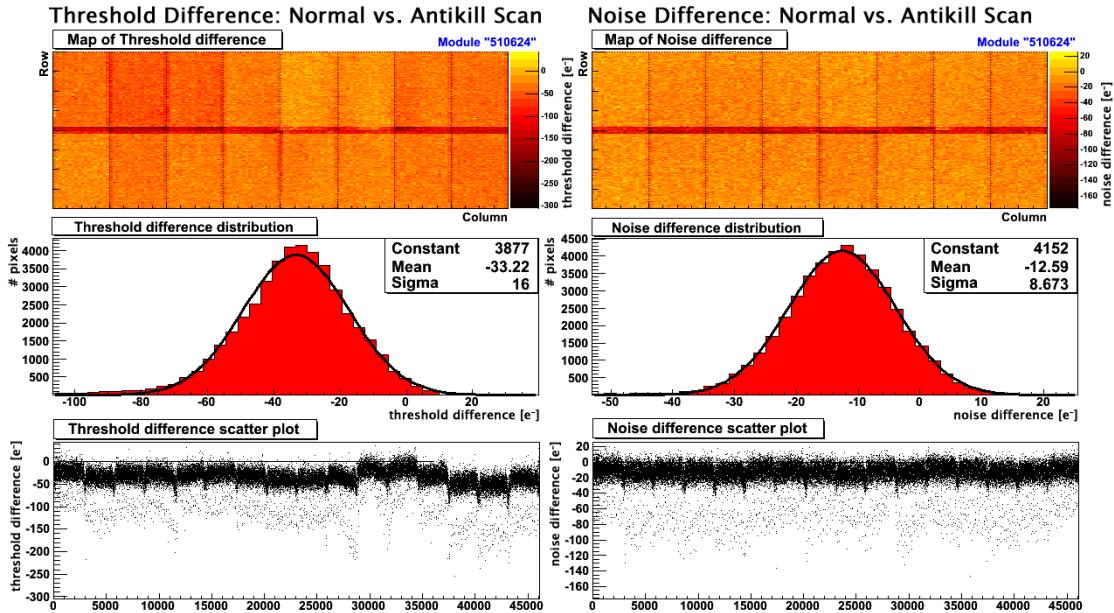


Figure 6-16 Threshold and noise difference maps and distributions between a normal and an antikill threshold scan for Module 510624

besides of the active mask-stage pixels are disabled, thus the digital and analogue activity on the FE is reduced to a minimum. Threshold and noise difference maps and difference distributions between the normal and the antikill mode threshold scan are shown in Figure 6-16. For standard, long and inter-ganged pixels the threshold decreases by 33 ± 26 e $^-$ and up to 150 e $^-$ for ganged pixels. The noise for standard, long and inter-ganged pixels differs by -13 ± 9 e $^-$ and up to about -90 e $^-$ for ganged pixels.

That the presented values are representative for all seven tuned modules can be seen in Appendix A Figure A-19. No significant noise differences and only small threshold differences between the two threshold scans are observed in disconnected bump bond regions in additional measurements, thus it can be concluded that the crosstalk responsible for the threshold and noise shift mainly occurs between sensor pixels. Figure 6-17 shows threshold and noise distributions for a TurboDAQ tuned and measured configuration at 5°C (red), for the same tuning measured with the System Test setup and STcontrol at -10°C (blue), for a System Test setup and STcontrol tuned and measured configuration at -10°C (green) and for the same tuning measured in antikill mode. Besides the 5°C TurboDAQ tuned and -10°C System Test measured threshold and noise distributions (blue) all other measurements are already discussed and are plotted to allow direct comparison. The 335 e⁻ difference in the average threshold between the TurboDAQ tuned and TurboDAQ tuning measurement can only partially explained by the 15°C temperature difference, which is expected to cause a threshold shift of ~138 e⁻, and the fact that the TurboDAQ configuration was tuned in antikill mode but the threshold values were measured in both cases in normal threshold scan mode (expected shift ~30 e⁻). TOT calibration were performed for all modules and with analogue injections scans of 20 ke⁻ TOT values of 30 bunch crossings (750 ns) were measured. For two modules (M511308 and M511384) of a stave with delaminated TMT (stave 4030) regions of several hundred analogue dead pixels were found in the A side module corners (FE7 & FE8) of AMS modules, which were not observed in the previous BIST measurement. Similar damages were observed in the barrel assembly Connectivity Test measurements for four staves with AMS modules on 6A and 5A stave positions. It is assumed that these damages are

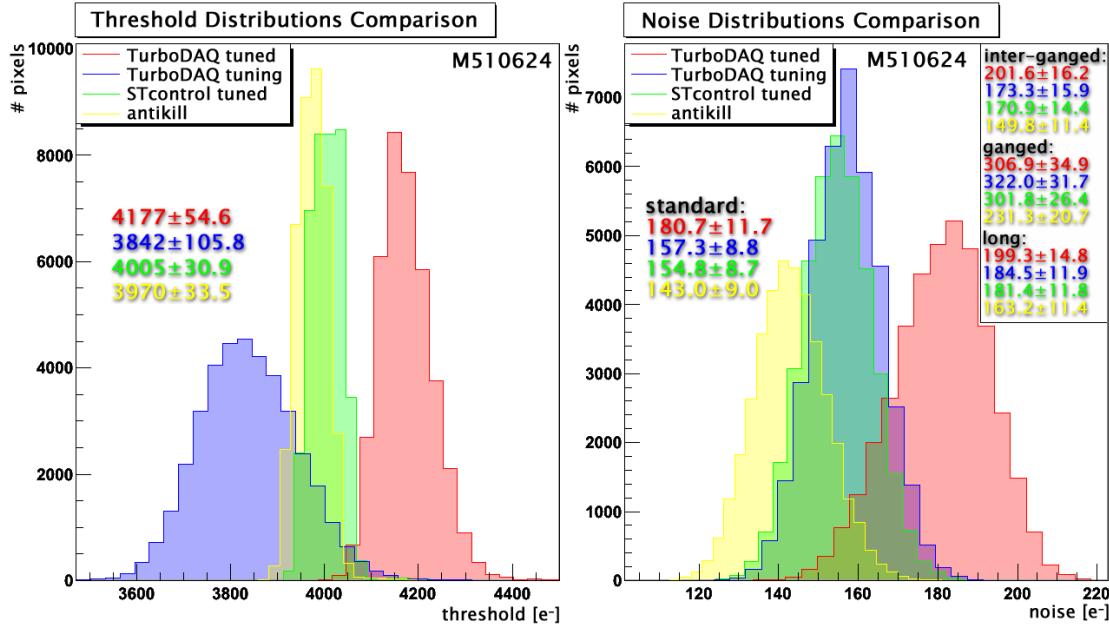


Figure 6-17 Threshold and noise distributions comparisons between the TurboDAQ tuned and measured module configuration at 5°C (red), the TurboDAQ tuning measured with the System Test setup at -10°C (blue), the System Test (STcontrol) tuned and measured module configuration at -10°C (green) and the threshold scan of the latter configuration in antikill mode for Module 510624

caused by mechanical stress applied to staves either by mechanical handling or fast temperature changes. With the C_3F_8 bi-phase cooling dT/dt values of about $35^\circ C/5\text{ s}$ were measured but cannot be significantly lowered with the existing cooling scheme.

The readout of modules was tested in the 40 Mbit/s and 80 Mbit/s mode for the D-type optoboard and additional in 160 Mbit/s mode for the B-type optoboard. For the 160 Mbit/s or more precise 2*80 Mbit/s readout mode the two module data links were tuned and tested individually in 80 Mbit/s mode and the BOC/ROD pair was set to 160 Mbit/s mode. To ensure the intended readout mode were used signal shapes of the DTO lines were measured at the PP0 test board Type0 connectors. For example the signal shapes of DTO and DTO2 are shown in Appendix A Figure A-18.

6.3 Endcap System Test

To test a higher fraction of the detector with more realistic services, readout chains and environmental conditions one of the detector endcap segments, corresponding to about 8.3% of the entire detector, was connected in SR1. In this setup endcap A was mounted together with a prototype SQP in a 4 m^2 dry box. The box was flushed with dry air, demoisturized with a regenerative compressed air dryer to a dew point of about $-40^\circ C$. The air humidity in the box was monitored with a chilled mirror hygrometer at the opposing box side of the air inlet to ensure that no cooling operation was performed if the dew point is not below $-30^\circ C$. Additionally the box air humidity and temperature were monitored by DCS controlled Xeritron, Honeywell and NTC sensors. The endcap with 144 modules was mounted in the box with the disk planes parallel to the ground and disk 1 facing upwards for cosmic data taking. The prototype SQP consists of two OSPs and provides services for up to 156 modules and 24 optoboards. It was mounted horizontally in the box with the outer side facing upwards. The SQP PP1 region was located in a separated part of the dry box to minimize air exchange by access to the PP1 region.

Production coolant capillaries and copper exhaust adapter tubes, which provide the necessary 90° tube bend, were used to connect the endcap and SQP coolant tubes. The thermal contact between the inlet and exhaust tubes in the SQP provides sub-cooling for the inlet liquid (see sections 4.1 and 6.2.1). The SQP inlet pipes, including the optoboard cooling circuit inlets, are connected per SQP side to a manifold with a manual shut-off valve to allow separate cooling operation of the SQP sides. Pressure sensors are attached to the manifolds to measure the coolant inlet pressure. A single coolant inlet line is used to connect the two manifolds to four distribution rack inlets. Close to the PP1 manifolds an electromechanical solenoid valve is installed to interlock the coolant inlet if pressure sensors at the exhaust side exceed 3 bar absolute, the cooling plant is in an error state or the communication with the cooling plant monitoring PC is lost. If the valve is closed an Idss interlock signal, connected to the Ipp1 box in the rack area, assures that all LV, HV and optoboard supply voltage channels are switched-off. Module cooling loop SQP exhaust lines are connected to two manifolds with back pressure sensors at PP1 and separate exhaust lines are used to connect them to the distribution rack. The exhaust line of the optoboard cooling loops has a manual pressure regulator valve close to PP1 to set its back pressure

independently of the rack back pressure. The rack bypasses and the bypass capillary are used to stabilize the cooling plant conditions before starting the endcap cooling and to evacuate the distribution rack after stopping the endcap cooling.

Besides minor problems with leak tightness of coolant pipes the cooling system showed stable performance and reliability. During cooling the entire endcap a pressure drop of about 0.8 bar absolute in the distribution rack heat exchanger (not in final cooling layout) was measured. It was removed to allow operation at the intended 2.0 bar absolute back-pressure and have a high enough safety margin to the 3 bar absolute maximal back pressure limit. For a measured inlet pressure of 12 bar absolute and for configured modules with a power dissipation of ~ 3.5 W per module an average temperature of -17°C is reached. Oscillations with amplitudes up to 1 bar in the inlet pressure are observed for low coolant mass flows caused by the inlet pressure regulation loop by the condenser cooling. If low mass flow through the Pixel distribution rack is necessary the total cooling plant mass flow is increased through one of the other distribution racks. High back pressure settings cause oscillations in the back pressure most probably due to formation of vapor bubbles in tubes constrictions. These provoke oscillations in the readjust loop of the BPR. For the thermal resistance between modules and the cooling system sector average values vary between 1.5 and 2.5 $^\circ\text{C}/\text{W}$ and a total disk average value of $2^\circ\text{C}/\text{W}$ is measured.

For electrical connections the disk module Type0 cables are connected to the SQP PP0 connectors. The six modules of one disk sector are connected to each PP0 row. The SQP replaces all power and signal routing of the PP0 test boards and poor-man SQP cable adapters of the bi-stave setup. Type2 cables and optical fibers are connected to the SQP PP1 endplate. In total three TX TTC and four RX data optical cables are used for the data transmission between PP1 and the rack area. They are connected to 12 BOC/ROD pairs distributed in two readout crates. One crate is equipped with eight, the other with four BOC/ROD pairs to test readout performance with a high number of BOC/ROD pairs as well as multi crate operation. The readout crates are connected via S-LINK in four groups of three BOCs each to four ROBINS of a ROS PC. An EventBuilder PC is used to combine all ROB fragments and save them as full events in bytestream format (see chapter 7) on CASTOR¹⁷³. Six HV Type2 cable are connected to twelve 16-channel ISEG modules in two ISEG crates with a four to eight distribution as well. Two PP2 NTC-MOD/OPTO boxes are connected to PP1 with 12 NTC/OPTO Type2 cables. For the connection to four Opto PP3s in one Opto PP3 crate 24 NTC/OPTO Type3 cables are used. Two SC-OLink crates, one with four the other with two SC-OLinks, are used to generate the supply voltages for the 24 optoboard. They are connected to the Opto PP3s with 12 OPTO Type4 cables. One BBIM is connected to the PP2 NTC-MOD/OPTO boxes using 24 NTC-MOD Type3 cables. Four NTC-OPTO Type4 cables and two NTC-PP2 Type3 cables are used to route the Opto PP3s and PP2 crates temperature lines to the same BBIM. PP1 is connected with 24 LV Type2 cables to two PP2 crates equipped with 12 regulator boards each. They are connected with 24 VDD and 24 VDDA Type3 cables to 12 LV PP4s equally distributed to four LV PP4 crates with an attached WIENER power supply each. The connection between PP2 and the Opto PP3 is realized with 24 VVDC Type3 cables. The interlock system contains two LUs, which are connected by 48 Type4 interlock cables. One of each IDB type, a BOC-I-Box and an Ipp1 box are used to distribute the interlock signals to the power supplies and

¹⁷³ Cern Advanced STORage manager

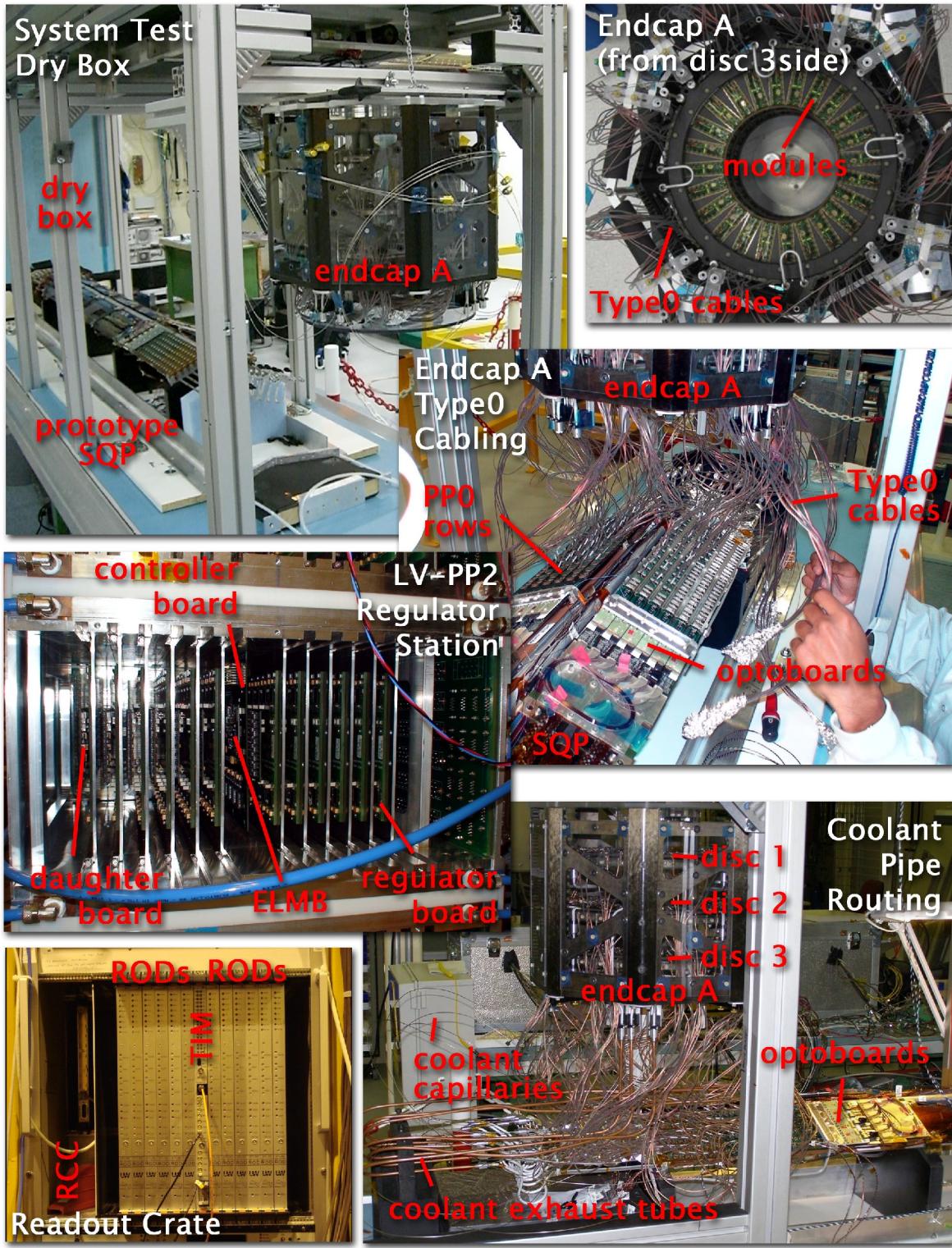


Figure 6-18 Snapshots of the System Test setup with the dry box containing the endcap A, the PP2 regulator station and a readout crate in the rack area

integrate the Iboc, Ipp1 and Idss interlock signals into the interlock system.

A connection database was implemented in the scope of this work. It contains for each module, the geographical position in the endcap, the PP0 connection position, the optoboard, the DCS name and DAQ information. Information about all service connections, channels and cables allows the complex connection chain for each module to be easily followed. The possibility of filtering the database information for each field and with different filter combinations allows to identify all modules connected to a specific cable, connection or service component. It serves as one of the most important mapping and debug tools for the System Test. Experience with the connectivity database and the developed data structure served as the base for the Pixel connectivity database as it is used for the Connectivity Test after the detector assembly and for the service assembly in the pit.

A so-called Service Test was performed before the endcap is connected to verify the continuity of all connections and their correct mapping up to the SIT mapping in the DCS, to ensure that all power supply channels deliver the correct voltages and that the interlock system switches off the correct supply channels in case of an over-temperature. The GPIB controlled Service Test setup consists of a programmable DC electronic load, two switching matrices with a relay and a multiplexer card each and two digital multimeters with two switching boards each. A Type2 cable with the LEMO-F interface (PP1) of each flavor can be connected to the setup at a time. For the optoboard the consistency between SC-OLink and Connectivity Setup measured voltage and current measurement of V_{PiN} and V_{Iset} are checked at nominal 0.7 V and 10 V as well as at 2.5 V for the DORIC reset. The DCS temperature readout is compared to the expected temperature for a 'nominal temperature' and an 'over-temperature' simulated by resistors. For modules the corresponding WIENER and ISEG channel interlock status is verified for both temperature cases, for optoboard the same is performed with the corresponding SC-OLink channel. It is verified that unconnected PP0 channels do not cause an interlock in the 'over-temperature' case. The HV and current values measured with the setup over a voltage divider are compared to expected values at 600 V. PP2 regulator trimmer positions are verified and if necessary readjusted to the nominal output voltage at load currents of 750/1200/400 mA for VDD/VDDA/VVDC. The load current measurements are compared to the LV PP4 and SC-OLink VVDC current measurements. To test the current compensation the load voltage measurement for two different load currents are compared (100;1000/100;1300/100;500 mA for VDD/VDDA/VVDC). The PP2 voltage monitoring circuit and current monitoring circuits are calibrated against output voltage and load current and are compared to the voltage and current measured by the load. At nominal load currents the output voltage at the load are measured with all combinations of closed and open high and low sense lines to ensure that voltages applied to the modules stay below the 4 V CMOS breakdown voltage (see section 4.8.1) in case of an open sense line. The transient voltage pulse shape is recorded for current steps from 100 mA to 800/1200/500 mA for VDD/VDDA/VVDC to check the transient voltage behavior. A detailed description of the Service Test setup and functionality can be found in [LEY07].

The trigger system for data acquisition runs are provided to the two TIMs by a LTP crate, which contains besides a LTP also a TTCvi¹⁷⁴, a TTCEx¹⁷⁵ and a ROD busy module. The LTP is in the experiment the receiver of TTC signals from the CTP and receives in the System Test setup random triggers signals with an adjustable trigger frequency from an external HP 8110A pulser with a pulse width of 40 ns and 2 ns transition time. The maximal Level-1 trigger rate depends on the amount of connected modules to a ROD and their occupancy. For excessive trigger rates RODs start to send BUSY signals through the TIM and ROD busy module to the LTP, which blocks further triggers to be issued to the readout crates until the BUSY signal is deactivated. Continuous data taking with random trigger rates up to ~ 50 kHz was achieved in the System Test. For cosmic data acquisition a system of four scintillator panels is used. The arrangement of the panels around the endcap A is shown in Figure 6-19.

Three panels are located below the dry box and one panel in the box above the endcap. Each panel is equipped with four PMTs from two sides. The used PMTs signals of a panel are logically combined (AND), a logical OR is applied to the lower

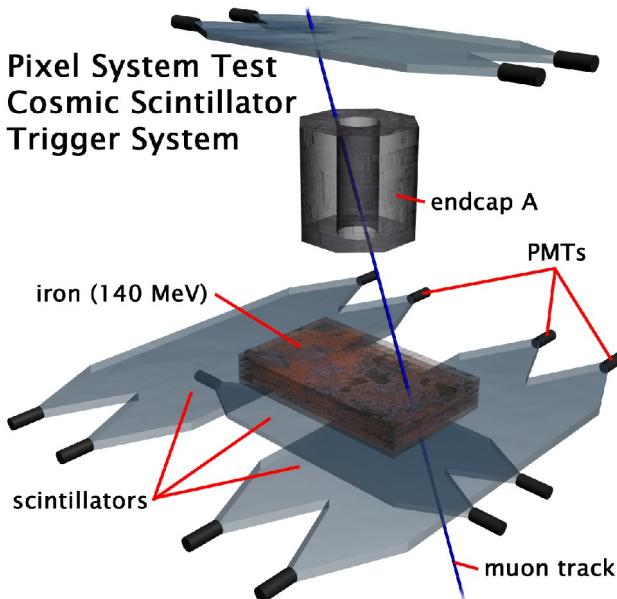


Figure 6-19 Scintillator trigger system for the Pixel System Test cosmic data acquisition

panels and the result is logically combined (AND) with the upper panel by a coincidence module. The resulting cosmic trigger is provided to the trigger input of the LTP. Iron plates above the middle lower panel are used to create a low threshold of ~ 140 MeV for muons triggered by the middle lower panel. An average cosmic trigger rate of 13 Hz was measured in the System Test with the shown scintillator configuration. The LTP generates the BC clock and LVL1 trigger as well as it allows to configure the trigger type. It incorporates the busy scheme for the ROD busy signals, which can be logically combined in the ROD busy module. The TTCvi serves as interface to the crate VME bus. It is responsible for the generation of BCR¹⁷⁶ and

¹⁷⁴ TTC vmeBUS interface

¹⁷⁵ TTC encoder/transmitter

¹⁷⁶ Bunch Counter Reset

ECR¹⁷⁷ synchronization signals which can be addressed individually to each TIM. These signals reset the LVL1ID and BCID counters on the TIM. The TTCex module encodes the BC, trigger, trigger type, BCR and ECR signals and transfers them optically to the TIMs. The trigger signals are delayed on the TIM to provide the necessary trigger latency for the detector readout.

6.3.1 Power-up and switch-off procedures

The operation of the Pixel Detector includes several transitions between detector states. The power-up and switch-off of the on-detector components belong to the more dramatic state transitions. Therefore at all steps of these procedures the safety of the detector and service components needs to be ensured. Different procedures were tested in the System Test and it was agreed on procedures for the power-up and switch-off procedures.

First it is ensured that the readout crate with the BOC/ROD pairs are switched on, are initialized, the lasers are switched-on and are not interlocked by a PP1 or BOC door interlock. It is necessary to have the XCK laser signal transmitted to the optoboard PiNs before the optoboard and modules are switched-on due to threshold adjustment circuitry of the DORIC. If no laser signal is seen by the powered optoboard PiNs the DORIC reduces its discriminator threshold until it sees a duty cycle of 50% of the noise floor. This results in a random DORIC output data stream with a high probability that a MCC command with a five or nine bit header is received by the powered module and a variating module power consumption. Especially if a slow command is recognized and the following random data stream is used to set FE DACs, configure or reset FEs the module power consumption can vary dramatically. This can be avoided for powered modules if the optoboard is switched-off, as it is in the case of a safety laser interlock, but the settlement of the delay-lock-loop with powered modules is suboptimal due to imperfect reconstructed XCK signal.

Next the SC-OLink and WIENER LV supply channels are switched-on as the LV channels and VVDC are used to power the daughter boards of the PP2 voltage regulators. Therefore they need to be switched-on before the regulator channels are activated. The regulator trimmers are set to the corresponding output voltages, but the individual INHIBIT of the regulator channels and the global KILL of the regulator board avoid that the modules are powered and VVDC is applied to the optoboards. Since V_{Iset} and V_{PIN} are activated together with VVDC they are applied to the optoboards, but no adverse effect of this was observed.

The ISEG HV channels are ramped-up in the third step. The applied depletion voltage results in the isolation of the n^+ pixel sensor implantations so that the pixel preamplifiers do not see a high capacitive load and have no increased noise at their inputs. If the sensor bias voltage would be ramped-up after the module LV are switched-on the high preamplifier noise would cause high digital activity in the FEs and MCCs resulting in significant increased digital power consumption of the modules. Since the HV channels are floating the connection of the HV ground to the switched off, thus not yet defined, VDDA on the flex does not cause ground loops.

¹⁷⁷ Event Counter Reset

The activation of the regulator channels in the fourth step starts with the switch-off of the global KILL followed by uninhibiting the two VVDC channels. A reset is applied to the optoboards by the SC-OLink to ensure the DORIC delay-lock-loop correctly reproduces the XCK. After a short O(ms) delay the VDD regulator channels are inhibited and an longer O(s) delay the VDDA channels. VDD needs to be switched-on before VDDA since otherwise the FE power-on reset circuitry does not reset the FE DACs, which leads to significant increased VDDA power consumption. The delay between the VDD and the VDDA turn-on is used to reduce the amplitude of a VDD current overshoot and its duration. The observed digital current peak is most probably caused by increased current consumption of the FE inverter blocks and has an amplitude of up to ~ 1 A for about one second. With the bi-stave setup and cold modules around -20°C current overshoot amplitudes up to 1.6 A with increased duration of up to 15 seconds are observed. The increase of the effect with low module temperatures was mainly observed with the bi-stave setup and is less dramatic with the endcap setup with the prototype SQP replacing the PP0 test board. Additionally to the temperature the amplitude and duration of the overshoot peak depends on the order and delay between the VDD and VDDA switch-ons. Minimal amplitudes and durations are found for a delay of few seconds for the VDDA switch on after the VDD switch-on. The reason for the overshoot and its dependencies could not be completely clarified. The power-up and switch-off (reverse order) procedures are implemented in the FSM (besides the initialization of the BOC/ROD pairs and verification of the laser status in the first step) and could be qualified in the endcap System Test.

6.3.2 Optoboard Low Temperature Behavior

The endcap System Test setup was used to systematically investigate the performance of optoboards below and at their design operation temperature of 10°C . Five optoboards, which were chilled by a bi-phase optoboard cooling loop in the SQP, were adjusted to four different temperatures between -11°C and 10°C by changing the back-pressure of the optoboard cooling loop. The optoboard temperature course during the performed BOC scans is illustrated in Figure 6-20. The temperature beside the curves indicate the approximate temperature at which the BOC scans were taken. At 10°C the optoboard back-pressure valve is closed and cooling is only provided by the liquid coolant in the cooling tube. The optoboard temperatures variate only in a 2°C range. For other temperatures the evaporative cooling comes into operation. A temperature difference of about 8°C is observed between the two optoboards (2091 & 2029) mounted at SQP top positions and the three optoboards (2019, 2008 & 3019) mounted in SQP bottom positions. The mechanical back-pressure regulator was experienced to be very sensitive and long stabilization times were found. Thus the adjustment and stabilization of intended optoboard temperatures was difficult. An expected temperature change of lower than 2°C during the BOC scans was accepted to be enough stable. The modules connected to the five optoboards were BOC scanned with five RX delay settings (0, 6, 12, 18 & 24 DACs [ns]) to be sure that most of the threshold scans were done outside of the delay error band. The threshold was scanned in six steps (50, 90, 130, 170, 210 & 250 DACs), which was found to be sufficient to determine stable operation points. Each BOC scan was performed at five V_{Iset} settings (0.75 , 0.80 , 0.85 , 0.90 & 0.95 V) to study the V_{Iset} dependency at lower temperatures.

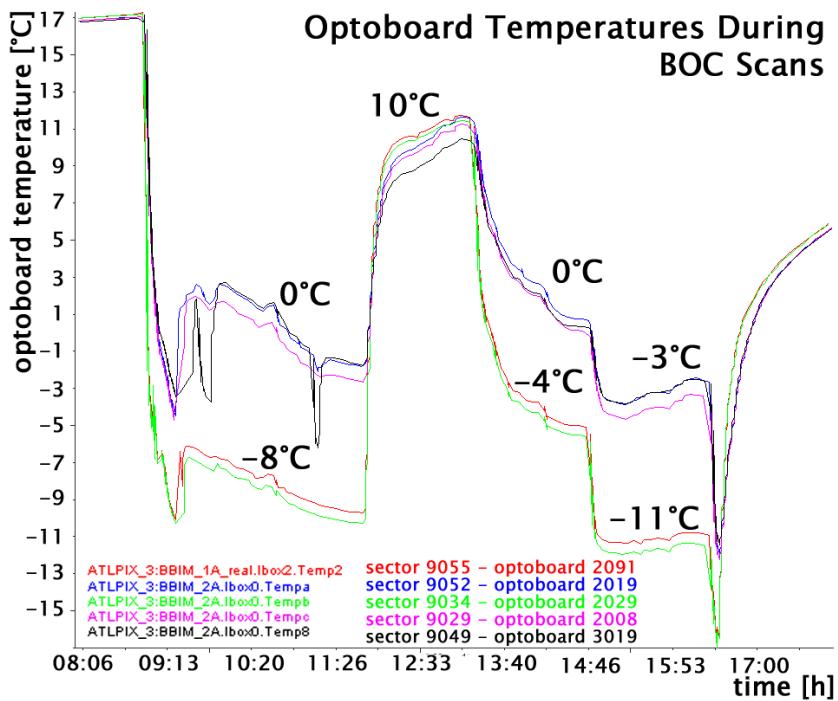


Figure 6-20 Temperature course of five optoboards during BOC scans performed at four different temperatures. Optoboard 2091 (red) and 2029 (green) are mounted at top SQP positions (5LT & 3LT) and optoboards 2019 (blue), 2008 (magenta) and 3019 (black) at bottom SQP positions (2LB, 3LB & 1LB)

The results of all BOC scans at four different temperatures for optoboard 2091 are shown in Figure 6-21. Each quadrant shows the BOC scan results of one temperature range with indicated minimal and maximal optoboard temperatures during the scan. The BOC scan histograms in a column belong to the same module and thus also to the same optical readout link. The BOC scan histograms in a row are measured with the same V_{Iset} . At the highest temperature all optical data transmission channels show uniform results from which uniform VCSEL light output powers can be concluded. The optimal operation point is found at a V_{Iset} value of 0.85 V with the minimal delay error band width close to the upper border of the threshold dynamic range. For lower temperatures the light output power slightly decreases as visible on the optimal V_{Iset} working point of 0.90 V for the lowest temperature but there is no big light output spread between the different optoboard channels. For all four temperatures a V_{Iset} value can be found which allows to operate all optoboard channels. This optoboard has adequate stable light output power with temperature changes and low light output power spread down to -11°C.

The BOC scan results of optoboard 2029 are presented in Figure 6-22 in the same way. For the highest temperature the VCSEL light output power is less uniform and two optoboard channels (connected to modules M1 & M5) have significantly higher light output power and show steeper increase of the low threshold error band than the other four channels. For these four channels higher V_{Iset} values above 0.85 V would be preferable to have the minimal delay error band width close to the threshold dynamic range upper edge, but the low threshold error band of the two high light power channel would fill out the entire threshold dynamic range and make those two

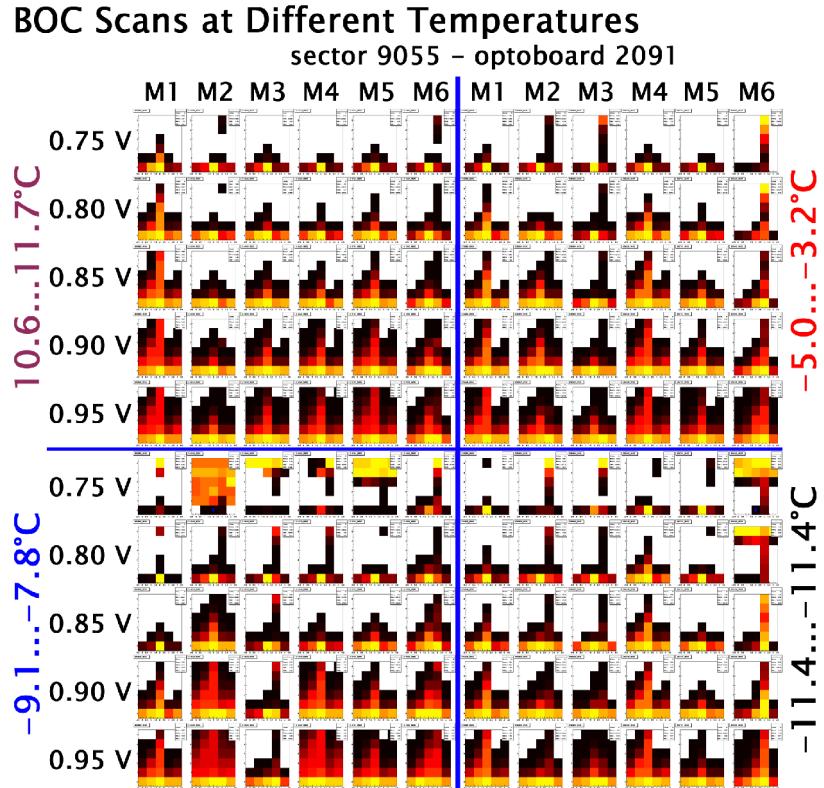


Figure 6-21 BOC scans at different temperatures for optoboard 2091

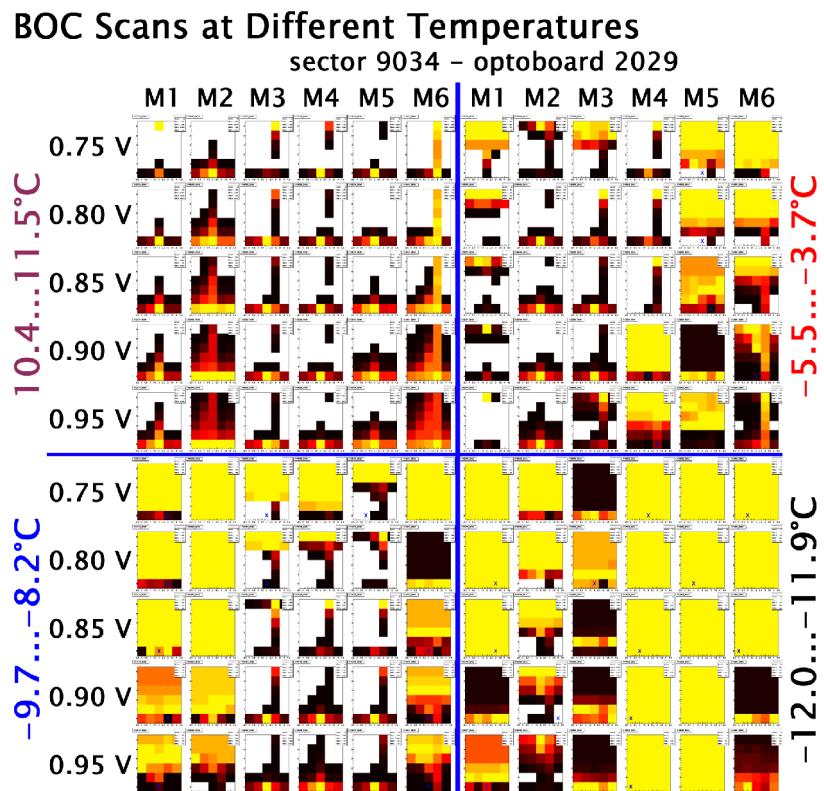


Figure 6-22 BOC scans at different temperatures for optoboard 2029

channels unusable. At about -5°C the light output power spread is significantly higher and especially two channels (M1 & M2) show very low light output powers even at high V_{iset} values. At about -9°C the optoboard channel at M2 has a light output power that provides an overlap between the error-free region and the RX-Plugin threshold dynamic range but the output power of two other channels (M5 & M6) decreased so much that an overlap seems to exist only for V_{iset} values above 0.95 V. For the lowest measured temperature of $\sim -12^{\circ}\text{C}$ only one optoboard channel has an overlap between the error-free region and the RX-Plugin threshold dynamic range at high V_{iset} values. Improvement with higher V_{iset} values and adding the low RX threshold range down to 0 DAC counts might improve the overlap, but the necessary temperature stability and further decreasing light output powers by irradiation of the optoboard dramatically limit the reliability of the optical data transmission. This optoboard shows an unacceptable decrease of light output power with decreasing temperature and high light output power spread and variation below 10°C .

The number of 'tunable' optoboard channels versus V_{iset} for the two selected (best and worst) optoboards and the four temperatures are shown in Figure 6-23. For this analysis a very loose 'tunable' criteria of two neighboring scan-points indicating an error-free communication was chosen. It does not provide a stable working point with changing V_{iset} or temperature. For optoboard 2091 all six optoboard channels are 'tunable' at V_{iset} values of 0.8 and 0.85 V in the measured temperature range whereas for the optoboard 2029 the number and V_{iset} working range decreases with decreasing temperature. From the other three optoboards two show decreasing light output powers and spreads below 10°C which can be partially compensated by higher V_{iset} values. The last optoboard shows high power spread already at 10°C with only three out of five working channels. At lower temperatures the non working channels have error-free regions but at the expense of other channels. The BOC scans results at different temperatures and the number of 'tunable' channel plots for the three optoboards are shown in Appendix A Figures A-20 to A-23. In total 27 out of the 29 available optical channels on five optoboards could be acceptably tuned at 10°C in the manner that a digital scan could be successfully performed. The two untunable channels appear to have high light output because they have error-free regions at

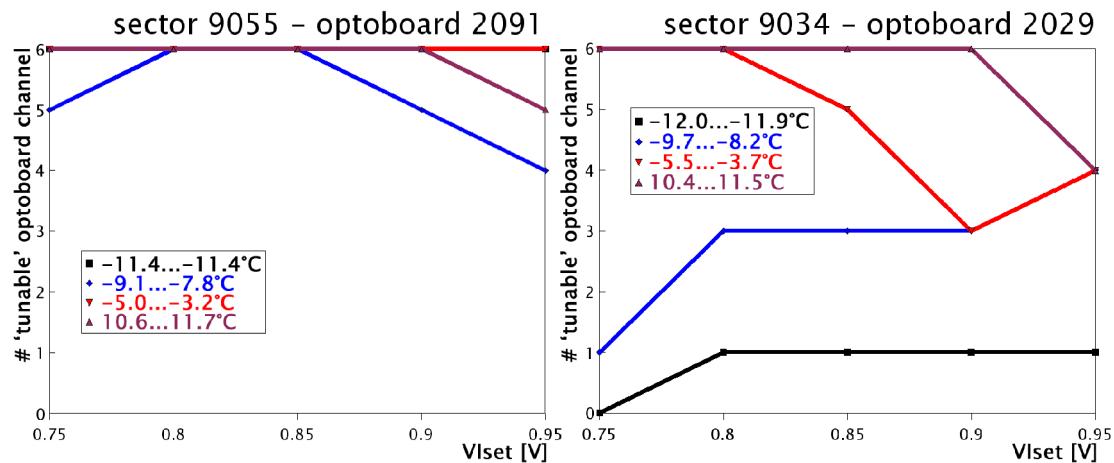


Figure 6-23 Number of 'tunable' channels versus V_{iset} at different optoboard temperatures

lower temperatures. The low temperature light output power decrease and spread behavior of the investigated optoboards variates from low decrease and spread down to -10°C to very high spread already at 10°C and high power decrease and increase of power spread with decreasing temperature.

For 11 optoboards further BOC scans with optoboard temperatures between 5°C and 15°C were performed. The RX delay and RX threshold steps were not changed but the V_{Iset} range was increased from 0.7 V to 1.2 V and scanned in 50 mV steps. Two of in total 66 modules were not usable due to a PP2 regulator channel and a PP1 cable retracted pin problem. The BOC scan results for eight optoboards, including two previously scanned, are presented in Figure 6-24. From in total 46 shown optoboard channels eight channels have no error-free region in the scanned V_{Iset} range. Five channels have an error-free region, but at V_{Iset} values for which the majority of other channels on the same optoboard are not usable. A noticeable fact is that some channels show a discrepancy to the expected linear light output power increase with increasing

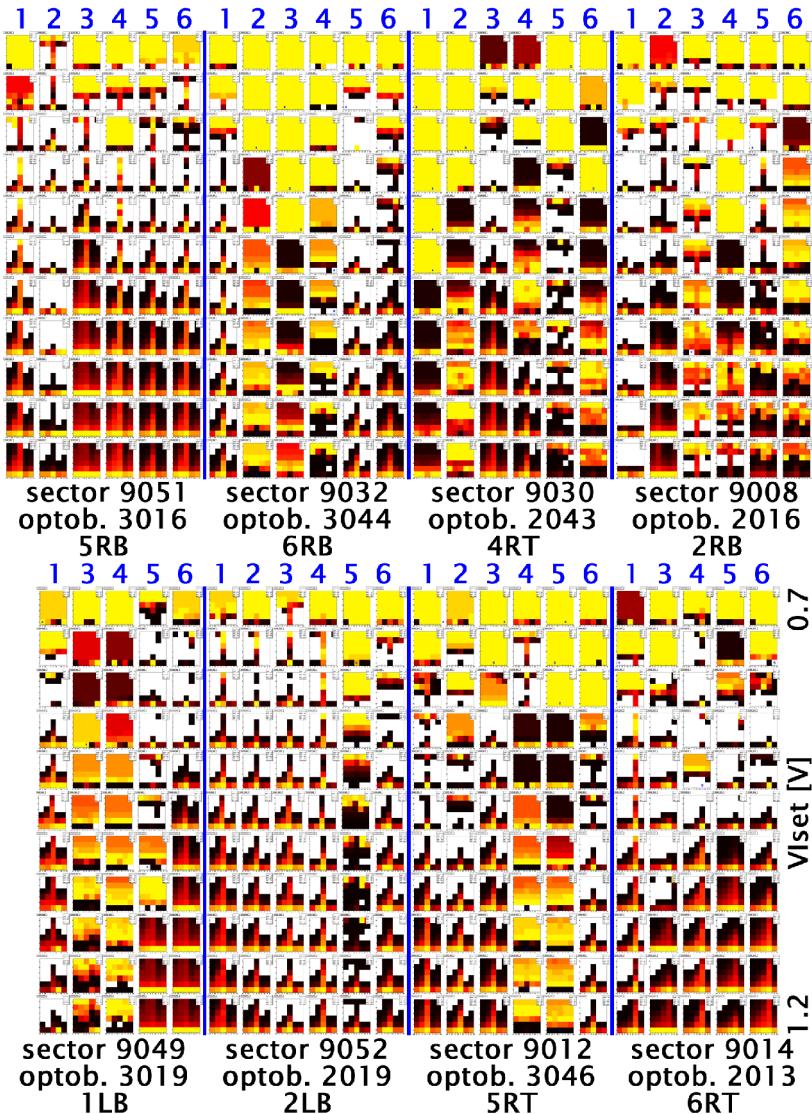


Figure 6-24 BOC scans for eight optoboards with increased V_{Iset} range: 0.7...1.2 V

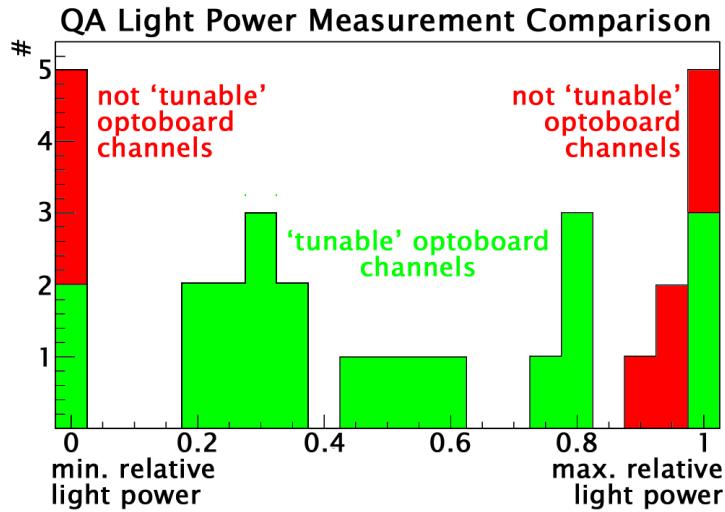


Figure 6-25 Comparison of eight not 'tunable' optoboard channels and 24 'tunable' channels to their quality assurance relative optoboard light output power measurements

V_{Iset} . For example module M4 of optoboard 2043 or module M4 of optoboard 2016 show error-free regions at 0.75 V and 0.8 V as well as error-free regions at 1.15 V and 1.2 V but no error-free region in-between. This indicates that for these channels an additional data transmission error source exists (see section 6-3-4). For the eight not 'tunable' optoboard channels and 24 'tunable' channels a comparison to their production quality assurance relative optoboard light output power measurement is presented in Figure 6-25. All problematic optoboard channels have either the dimmest VCSEL laser diode on the optoboard or have very bright laser diodes. It confirms that the high VCSEL laser output power spread is responsible for the tuning difficulties. In summary 54 out of 64 optoboard channels could be tuned at 10°C and it was shown that a high light power spread exists for some optoboards even at 10°C optoboard temperature.

An additional possibility to measure the VCSEL light power spread is to use the PiN array current (I_{PiN}) on the BOC RX-Plugins. Since the current of the PiN diodes cannot be measured individually the STcontrol implemented light power measurement scan measures the noise floor with all connected modules not sending any data. The noise floor is mainly provoked by optoboard channels without connected modules. Individually the connected modules are set to XCK/2 mode, I_{PiN} is measured and the noise floor is subtracted. Examples for two optoboard I_{PiN} light output power measurements at three different temperatures are shown in Figure 6-26. The results of three additional optoboards are presented in Appendix A Figure A-24. For optoboard 2043 the PiN currents measured at about 22°C are very uniform and increase with increasing V_{Iset} . Factors between the minimal and maximal I_{PiN} are 1.9, 1.5 and 1.7 for V_{Iset} of 0.75 V, 0.85 V and 0.95 V. This contradicts with the 'slow' BOC scan results and confirms that an additional effect besides the light power spread may cause data transmission errors. For an optoboard temperature of ~6°C the I_{PiN} s decrease to ~0.5-0.2 of the 'warm' values and the max-to-min factor increases to 30 and 5.1 for 0.75 V and 0.95 V. At low optoboard temperatures of about -8°C the measured I_{PiN} values do not significantly differ from the subtracted noise floor and cannot be used for reliable

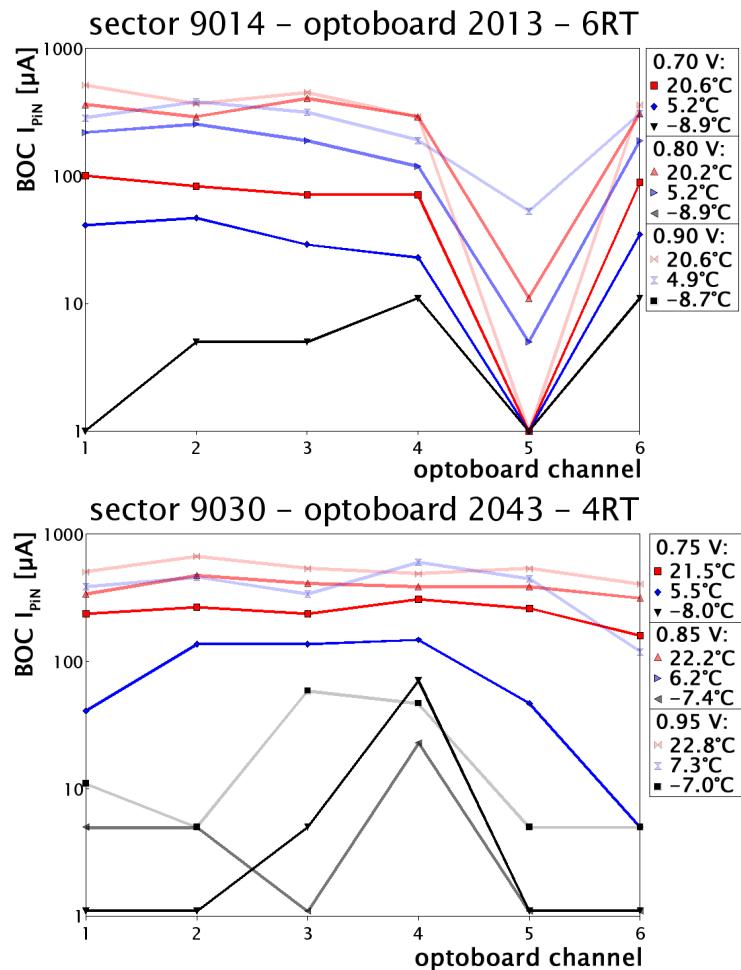


Figure 6-26 BOC I_{PIN} light power measurement for two optoboards (2043 & 2013) at three different temperatures and V_{Iset} values

light power conclusions. With optoboard channels which have no connected module, M2 (optoboard channel 5) on optoboard 2013 and M5 (optoboard channel 2) on optoboard 2075, show noise floor variations up to $50 \mu\text{A}$. Anyhow the decreasing light output power and increasing power spread effects with decreasing optoboard temperatures are confirmed.

The 24 optoboards used in the System Test were production optoboards but with the worst available quality assurance rankings to ensure that observed problems are over-rather than underestimated. To ensure that no optoboards with low temperature power decrease or high power spread problems are integrated into the detector the quality assurance procedures for the optoboards were adapted according to the System Test experiences. For example the procedure for light power measurement was changed from 10°C ambient air temperature to 10°C measured with the optoboard, additional power spread measurements at -25°C and power spread cuts were implemented. Bypass capacitors were added to the V_{Iset} lines on the optoboard to reduce the noise on V_{Iset} and thus noise of the optical power. Improved power stability of the dim and bright optical signal states were proved with optical probe measurements but no obvious effect of the capacitors was found in BOC scan measurements. Optoboard

heaters and covers were installed to allow operation of the optoboards in ATLAS at 10°C even with switched on bi-phase optoboard cooling as described in the next section.

6.3.3 Optoboard Heaters and Covers

Due to the observed decreasing laser output power and increasing laser output power spread of the optoboard VCSEL arrays with decreasing temperature, heaters and convection blocking covers have been installed on the optoboards. Their aim is to allow the operation of the optoboards above the VCSEL design operation temperature of 10°C. A cover is made of Kapton® laminated copper foil, covers all optoboards of a SQP PP0 row and thus limits the cooling of the optoboards by air convection. The optoboard heater consist of a flexible Kapton® PCB loaded with six groups of four $600\ \Omega$ 0.5 W resistors for the six optoboards of a SQP PP0 row. The four resistors of a group are connected in parallel to form a $600\ \Omega$ 2 W equivalent resistors and are glued to the corresponding optoboard. The six resistor groups are parallelly connected to make an effective $100\ \Omega$ 18 W heater array. From the specification of the heater resistors a safe operation up to 27 W can be expected. A NTC is mounted on the heater PCB close to the first resistor group. A heater PCB with the mounted resistors and the NTC is shown in Figure 6-27. The heaters are supplied by a switchcard system, which was developed for the thermal barrier heater pads as mounted on the PST. The switchcards are capable of providing 48 V DC and are controlled and monitored by an ELMB. With the switchcards the individual heater channels can be switched, can be operated with a programmable duty cycle, can be regulated by the ELMB depending on the NTC temperature measurement or can be set to follow the operation mode of the neighboring channel.

The results of optoboard temperature measurements for the prototype SQP with three different optoboard configurations versus the power of an installed heater array is shown in Figure 6-27. The optoboard cooling is effectively switched-off, since the exhaust valve of the optoboard cooling loop is closed. Two SQP PP0 rows (LB and LT) are uncovered and have no heater array installed. The optoboards of SQP PP0 row RT are covered and the optoboards of PP0 row RB have a cover and an optoboard heater array mounted. For the switched-off heater array the LB, LT and RB optoboard temperatures of about 15°C are achieved. The bottom optoboards show a tendency of roughly 2°C lower temperatures, since they are located closer to the SQP cooling tubes. This behavior is observed without installed covers as well, and the cover on the RB position does not significantly heat up the optoboards. Whereas the cover in the RT SQP position shows a significant effect and optoboard temperatures are $\sim 12^\circ\text{C}$ warmer compared to the LT optoboards, where no cover is installed. Temperatures for positions LB, LT and RT are slightly decreasing with increasing RB heater array power, which are measured in order of increasing power. This indicates that the thermal equilibrium is not fully reached, but more important it shows that very little thermal coupling exist between the different SQP PP0 rows. The temperature slope of optoboard positions 6RB-2RB can be approximated with 1.5°C/W . For the optoboard position 1RB a flatter slope with 0.9°C/W indicates a higher thermal coupling to the cooling circuit or the neighbored SQP panel.

Optoboard Temperature vs. Heater Array Power

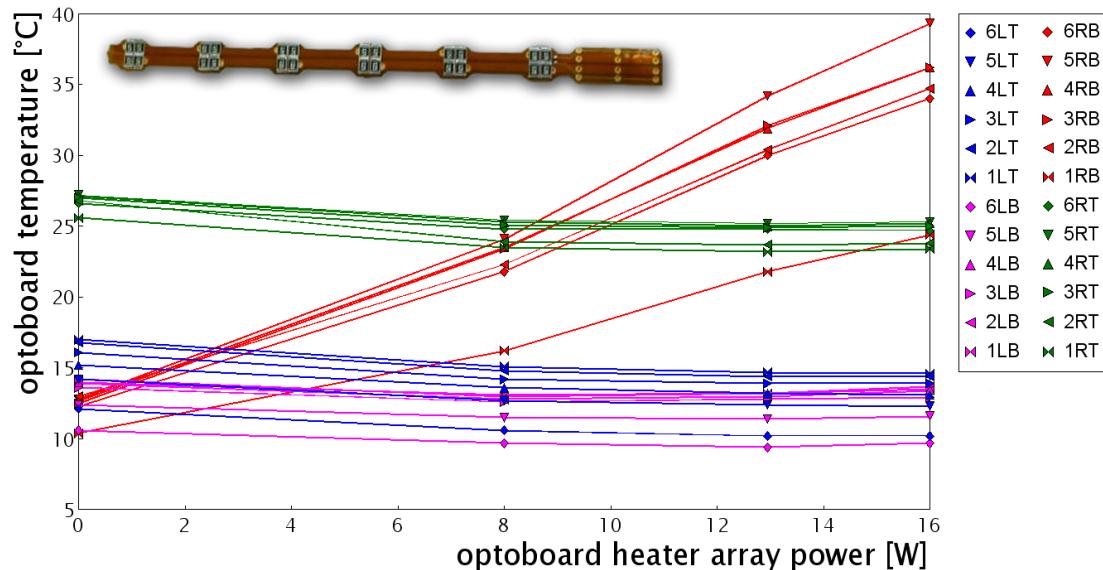


Figure 6-27 Optoboard temperature versus the heater array power applied to the 'RB' SQP PP0 row with installed optoboard covers for 'RB' and 'RT' but not for 'LB' and 'LT' PP0 rows

Measurements with an optoboard cooling loop operated at a back pressure of 4.2 bar absolute show that optoboard temperatures above 20°C are reachable with the heater array operated at 16 W. These values are measured at the RT SQP position, thus higher necessary heater power can be expected for bottom PP0 positions. Since the System Test can neither reproduce all detector SQP PP0 positions nor the heat convection conditions of the detector in the PST can be adequately simulated this measurements cannot be directly used to assure optoboard temperatures above 10°C. But due to the existing heater power safety margin high enough optoboard temperatures even with activated optoboard coolings loops can be expected.

6.3.4 'Slow' and 'Fast' BOC Scan and Slow Turn-on

As alternative to the BOC scan described in section 6.1.1 a BOC scan with a different measurement method was developed in the scope of the System Test [DOP07]. The original BOC scan uses a reference bit pattern of 1600 bits, which is typically sent ten times to a module and compared bit by bit to the bit stream received from the module to check the optical RX data transmission error rate. With typical parameters a minimal error rate limit of $\sim 6 \times 10^{-5}$ is reachable for each error-free tested {RX delay, RX threshold} combination. Typically the available {RX delay, RX threshold} parameter space is scanned in 25 delay steps (0-24 DAC counts) and in six threshold steps (50-250 DAC counts) in about 3 minutes for a single module. The new BOC scan switches the modules into XCK/2 mode, measures with a counter for about 64 kbits the amount of reconstructed '1's and calculates the ratio of '1' counts to the data stream length. A ratio of $\frac{1}{2}$ is expected for an error-free data transmission of the half clock and a deviation indicates bit-flips in the reconstructed data stream. If it is

assumed that bit-flips happen in a preferred direction ('0'→'1' or '1'→'0'), for example for too low or too high threshold settings, a minimal error rate limit of $\sim 1.6 \times 10^{-5}$ is reachable for an error-free tested {RX delay, RX threshold} combination as well. For error sources which have equal probability for both bit-flip directions, for example jitter of the optical signal, a lower minimal error rate needs to be assumed since bit-flips in opposite direction cancel out each other in the ratio result. The advantage of this method is that it can be performed with all possible 255 RX threshold steps and 25 RX delay steps in about 20 seconds for a single module. This 'fast' BOC scan shows due to its higher threshold resolution more precisely the laser signal shape. The results of 'fast' BOC scans for two optoboard at about 10-15°C optoboard temperature are shown in Figure 6-28. Additional four optoboard results are presented in Appendix A Figure A-25 and A-26.

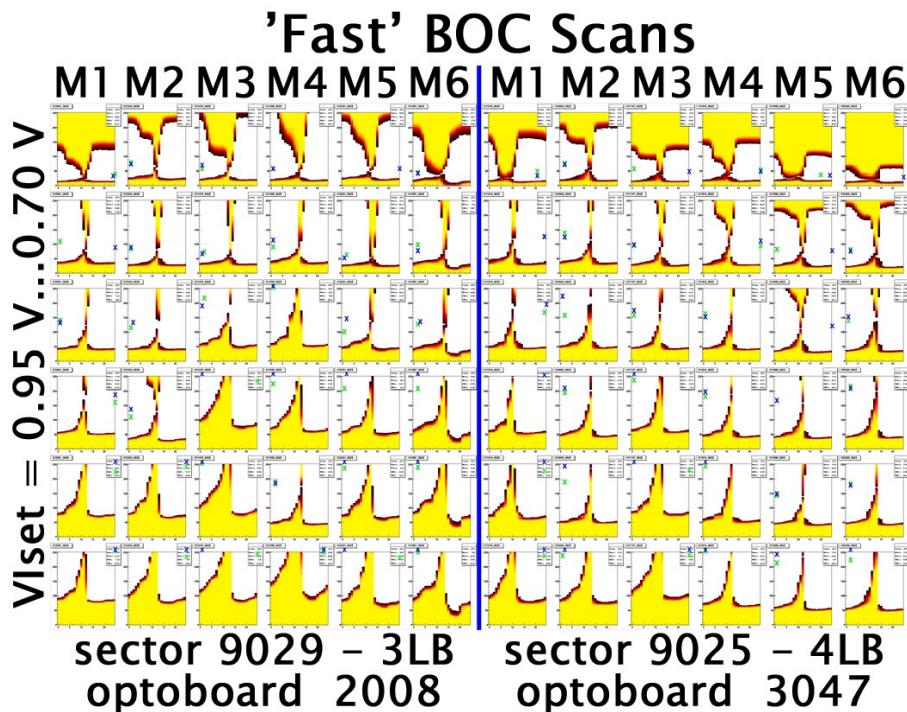


Figure 6-28 'Fast' BOC scans for two optoboards (2008 & 3047)

In comparison with 'slow' BOC scans the 'fast' BOC scan show less channels with small error-free region or not linear light output power increase with V_{Iset} increase. For most of the optoboard channels a deviation from the expected signal shape with a step in the light output power in the rising signal edge at low V_{Iset} values is visible. The relative height of the light power step decreases with increasing V_{Iset} . Especially for high V_{Iset} values a decrease of the light output power before the rising edge is observed for some optoboard channels. Both effects are not visible in 'slow' BOC scans due to the lower threshold resolution. In order to compare the 'slow' and 'fast' BOC scan results 21 optoboards of the endcap A with in total 125 optoboard channels were measured with both BOC scans at tuned V_{Iset} , at the same optoboard temperatures of 5-15°C and with the same RX threshold resolution. Channels which show a significant difference between both methods are shown in Figure 6-29 and the entire measurement results of the endcap are presented in Appendix A Figure A-27. The

'Slow' / 'Fast' BOC Scan Comparison

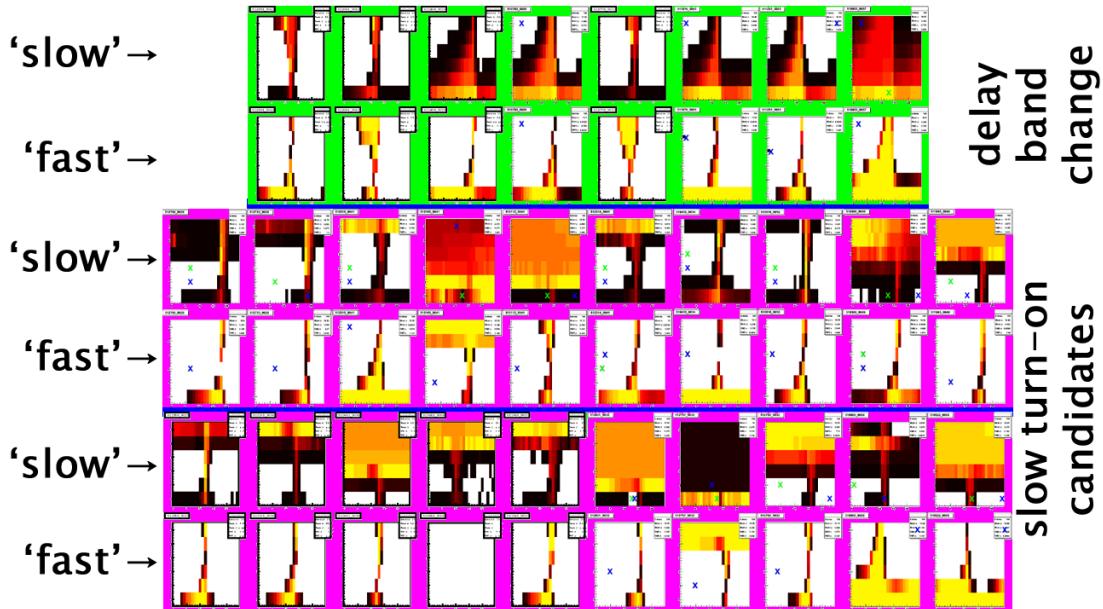


Figure 6-29 Comparison between the 'slow' and the 'fast' BOC scan. In total 125 optoboard channels were compared at tuned V_{Iset} . Twenty channels are slow turn-on candidates and eight show a significant change of the delay band structure

majority of compared channels has consistent results for the position of the low threshold error band as well as for the position and shape of the delay error band. Marginal differences can be ascribed to the different minimal error rate limits and cancellation of different bit-flip direction errors in the 'fast' BOC scan. Out of the 125 optoboard channels 28 show significant differences between the two BOC scan methods and the differences can be split up into two groups. Eight channels show significant differences in the width or structure of the delay error band with five of them have in general wider delay bands in the 'slow' BOC scan, two of them (2nd and 5th from left in Figure 6-29) have a wider delay band at high thresholds in the 'fast' BOC scan and one of them (first from left) has a wider delay band at high thresholds in the 'slow' BOC scan. These differences may be caused by error sources with equal probability for bit-flips in both directions but this is unproven. The other group consists of 20 channels showing a high threshold error band clearly observed in the 'slow' BOC scan but not visible in the 'fast' BOC scan. In comparison to the 'classical' high threshold error band, the error band which is only visible in the 'slow' BOC scan does not smoothly merge with the delay error band, but the error band sharply continues with about the same width in the high threshold error band (most obviously visible in the four leftmost magenta marked optoboard channels of Figure 6-29). This provides an indication that the high threshold error band is not consistent with the 'classical' high threshold error band, but an additional data transmission error source is limiting the error-free region. The ATLAS SCT detector uses the same VCSEL arrays as the Pixel Detector and observed a slow turn-on effect in the VCSEL laser output power [WEI06]. Figure 6-30 shows the 'slow' BOC scan result of a slow turn on candidate and the bit patterns for all 25 RX delay steps and three selected RX

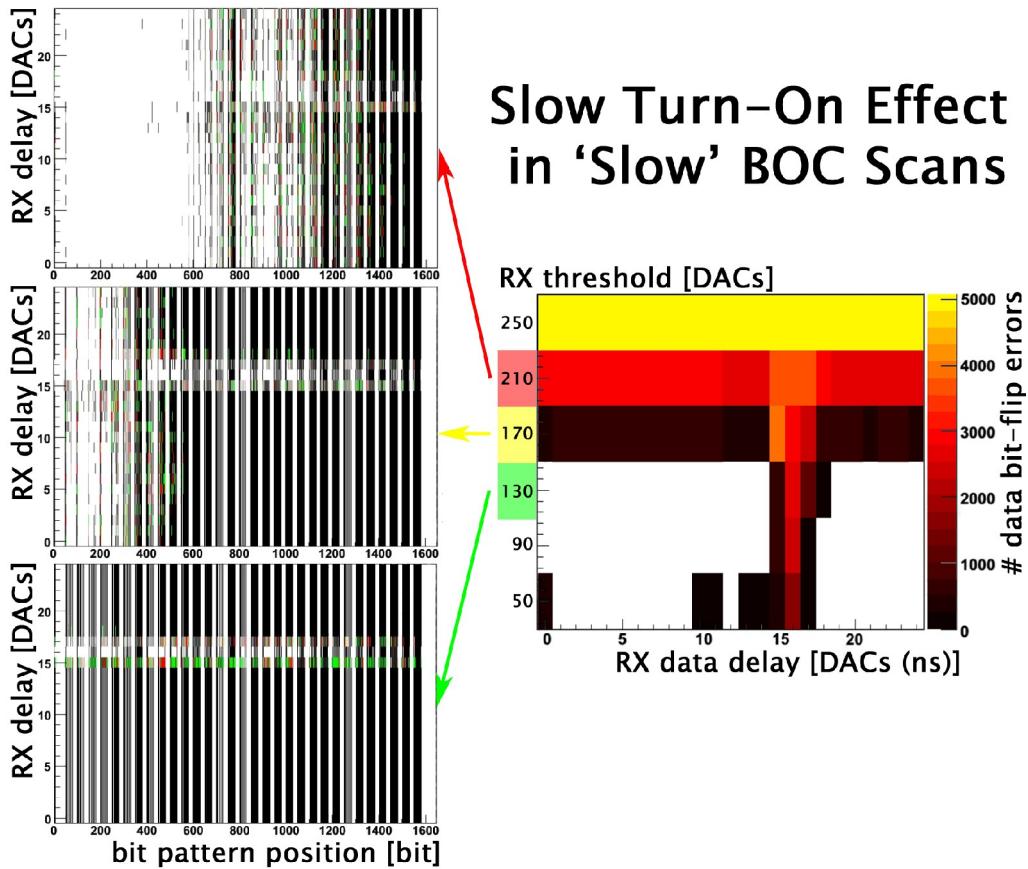


Figure 6-30 Slow turn-on in the 'slow' BOC scan

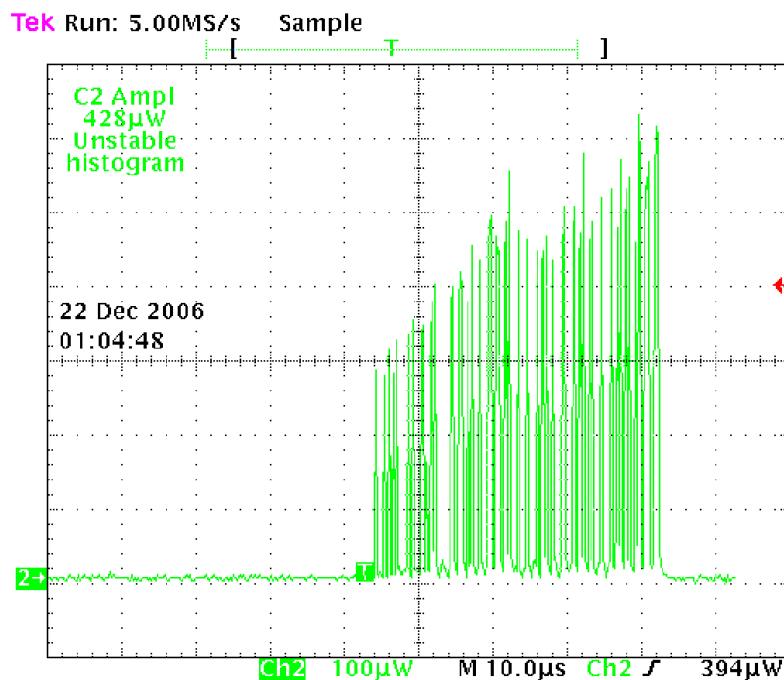


Figure 6-31 Oscilloscope screenshot of slow turn-on measurement with an optical probe

thresholds. For the lowest threshold (130 DAC counts) the entire reference bit pattern is reconstructed and data transmission errors occur only at the delay band. For a threshold of 170 DACs, bit-flips from '1'→'0' are additionally observed in the first ~500 bits for all RX delay setting. The number of bit-flips decreases with increasing bit position in the data stream. For the highest shown threshold (210 DACs) the bit-flips occur up to a bit position of ~1400. This measurement confirms the slow turn-on of the VCSEL channels as seen for the SCT with decreased light output after the channel is for longer time in dim state and only the slow increase of the laser power to its full value at data transmission. The slow-turn on is not visible in the 'fast' BOC scan because there exists a delay between the switching of the modules to XCK/2 mode and the start of the measurement. Thus the first '1's of the half clock which may be affected by the slow turn-on are not measured and the half-clock can be correctly recovered with high thresholds after the light power reached its full value. A modification of the 'fast' BOC scan to be able to measure the first bits of the half clock and thus to identify slow turn-on optoboard channels is in preparation. In order to prove that the observed effect is not caused by the receiver side (RX-Plugin) a Tektronix P6701B optical to electrical converter with a MT-16 to single fiber fanout were used to measure the VCSEL light output signal shape at the BOC end of the optical fiber. An oscilloscope screenshot of the optical signal shape for an optoboard channel with slow turn-on is shown in Figure 6-31. The light output power of the channel is after a longer dim state of only about the half of the power at the end of the ~40 µs data stream.

The module position, which is associated with the optoboard channel, of the 28 channels with discrepancies between the two BOC scan methods is presented in Figure 6-32. Both 'slow' to 'fast' BOC scan differences groups show a clear tendency to occur in middle optoboard channels. Additional production measurement of optoboards confirmed the slow turn-on hypothesis and the tendency to middle optoboard channels. They could show that slow turn-on occurs with beveled surface

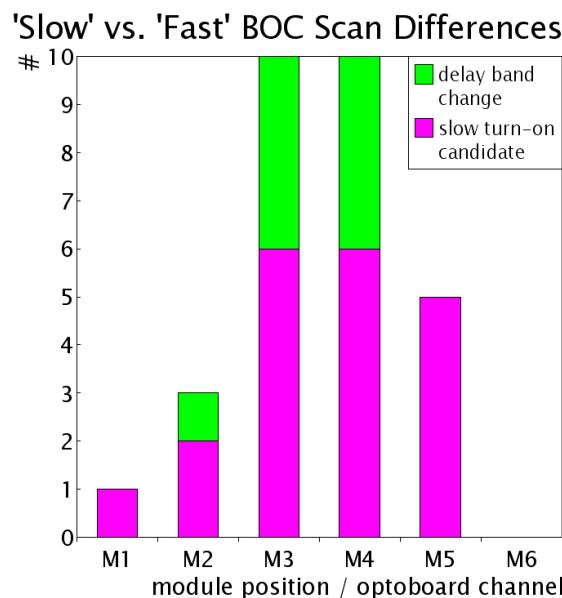


Figure 6-32 Module position (optoboard channel) of the delay band change and slow turn-on candidate 'slow' and 'fast' BOC scan differences

optical connectors but not with flat surface connectors [FIS07]. The strength of the slow turn-on effect depends among others on the distance of the optical fiber to the VCSEL array at the optoboard optical connector. Thus it can be assumed that the observed slow turn-on is caused by a mechanical misalignment which leads to coupling of different transverse laser modes into the optical fibers, but no fully plausible explanation for this behavior was found. Slow turn-on measurements and cuts were included into the optoboard production quality assurance measurements to ensure that no optoboards with significant slow turn-on are integrated into the detector.

6.3.5 Optical Link Tuning Procedure

In the scope of the System Test, a procedure for the tuning of the optical link parameters was developed. The procedure is optimized to ensure the correct mapping of the readout system, to set the best possible working points in the {RX delay, RX threshold, V_{Iset} } parameter space for the optical links of an optoboard and to cope as well as possible with the light output spread of optoboards at temperatures below 10°C and slow turn-on. It is developed for the chilled module case, in which the operation time is not strictly limited by the heat-up of modules. Since the parameter range and steps of the procedure scans are a compromise between speed and accuracy of the optimal working point it can be easily adapted for situations in which no cooling of the modules is possible and thus the operation time for scans is limited. Possible reductions in the scan step for such cases are pointed out.

In a first step it is ensured that the mapping between the modules and the BOC TX-Plugin channels (inlinks) is correct and that the TX side of the optical link works. It is assumed that the mapping of the NTC and LV channels is already checked by switching-on the modules one-by-one and checking that the corresponding PP2 and PP4 current values as well as the corresponding NTC temperature value increases. To check the TX communication to the optoboard the modules of a PP0 are sequentially configured, the increase of the corresponding LV and temperature values is checked and the module is reset before the next module is configured. In the absence of module cooling the heat of modules can be minimized by configuring only one of the 16 FEs per module and by powering sequentially only the module under test. The latter is an additional crosscheck that the mapping between LV, NTC and TX inlink is consistent. Modules which fail to be configured are marked as 'TX problem', excluded from further tuning process and need manual debugging.

Several causes can be responsible if a module cannot be configured. Besides trivial inlink mapping and switched off laser problems, non working TX-Plugin channels, broken optical fibers, problems with the optoboard PiN array, the DORIC delay-lock-loop or an open DTI line in the Type0 cable are more difficult to diagnose. From the VDD current consumption it is possible to distinguish (see section 4.8.1) if a module receives the correct 40 MHz XCK, a 20 MHz half-clock for example caused by a not correctly locked delay-lock-loop or if no clock is seen by the module. The second case can mostly be recovered by a reset of the DORIC on the optoboard. For the latter case it is possible to check if some light is seen by the PiN by varying the corresponding TX-Plugin laser output and monitor the optoboard PiN current for changes. Increasing

the laser output power might help in cases where a bad optical coupling causes low laser signal amplitudes seen by the optoboard PiN. If the lasers are switched-off or lowered to low laser power values for I_{PIN} comparison the module LVs should be switched-off to avoid that the DORIC threshold adjust circuitry runs into the noise floor and the module draws high VDDA currents (see section 6.3.1). If the module receives correct clock but does not configure a broken TTC data line in the TX-Plugin, a problem in the recovering of data in the DORIC or a broken DTI line between the optoboard can be expected. The first can be verified by the exchange of the TX-Plugin whereas the exact localisation of the problem in the other cases is due to the inaccessibility of the components impossible. As mentioned in section 6.1.1 the measurement of the TX data transmission error rate is not easy and fast to perform. Thus an automated and practicable scan should be implemented for debug purposes. For the standard procedure such a scan would be too slow and experience with the 144 System Test modules indicate that the TX data transmission is very robust so that the individual measurement is not necessary.

The second step of the procedure performs a fast RX threshold versus RX delay versus V_{iset} scan. For RX threshold a parameter range of 10-250 DACs scanned in seven steps is sufficient to set a reasonable threshold. A finer resolution can be used to understand the shape of the laser signal in problematic cases. As experienced in the System Test, a stable tuning requires an error-free threshold range of about 40 DACs above and below the working point, so that a finer resolution is not necessary in general. The RX delay parameter space is scanned in all 25 DAC(ns) steps to allow a precise determination of the delay error band. For uncooled module scenarios the scan step size may be doubled to halve the scan time. For the System Test with optoboard temperatures below room temperature V_{iset} is scanned in 50 mV steps from 0.7 V to 1.0 V. For warmer optobards where no high light power decrease and spread is expected the scan range can be reduced to 0.9 V.

The choice of the optimal working point is non-intuitive because several factors like stability against the most sensitive parameter V_{iset} or the shape of the laser signal have to be considered and balanced. Due to the different slopes of the low and high threshold error band a RX threshold setting at $\sim 1/5$ of the distance between the low and high threshold error band (closer to the low error band) provides equal stability against V_{iset} changes in both directions. The laser signal shape shows lower deviation from the optimal rectangular signal shape at the low plateau than at the high plateau. In the System Test the best working point is found with V_{iset} set to values where the minimal width of the delay error band is close to the upper border of the threshold dynamic range. The RX threshold working point set to this high values as well. This way it has a sufficient distance to the high threshold error band and is set roughly to the described distance even though the position of the high threshold error band cannot be measured due to the limited RX threshold dynamic range. The method ensures that the VCSEL arrays are operated as close as possible to their design light output power, which is not usable due to the limited RX threshold range.

An algorithm searches in each RX threshold versus RX delay scan histogram at different V_{iset} s the low threshold error band position, the high error band position, the delay error band position as well as the threshold with minimal delay error band width. The low error band position is defined as the lowest threshold value with an error-free entry, whereas the high threshold band position as the highest threshold

with an error-free entry if a higher measured threshold value exists with errors at all delays. The minimal width of the delay error band is defined as the threshold with minimal sum of errors over all delays. If no higher measured threshold value with a higher error sum exists the minimal delay width is flagged as 'dynamic range minimum'. At the minimal delay width threshold the maximal delay value with errors is defined as the delay error band position. The working point is set to the minimal width of the delay error band threshold value and the delay error band position shifted by 4 ns to higher RX delay values (see section 6.1.2). The surrounding phase space of the working point is investigated and is moved to a higher delay and threshold values if it is not error-free in a radius of 40 RX threshold DACs and 3 RX delay DACs. The V_{Iset} is then adjusted to maximal number of valid working points with high threshold values optimally at 210 DACs. Since the 'dynamic range minimum' tagged threshold working point values falsify the mean threshold working point calculation, a linear fit with extrapolation is used for the average threshold working point determination for tagged scans. This way ensures that low threshold outliers are not privileged over high threshold outliers.

If no error-free region exist for a module for all V_{Iset} values the module is marked as 'RX problem', is disabled for the further procedure and needs manual debugging. As for the TX data transmission on-detector problems of the RX data transmission are hard to locate. A broken DTO line, problems with VDC or the VCSEL diode or a broken optical fiber have similar symptoms. An open optoboard VDC input channel might result in the channel be stuck in laser dim current, high current or oscillating between both states. The latter two can be measured by an increase of the RX-Plugin PiN current with no RX data transmission (lasers in dim state) for all other channels. Optoboards for which no working point for all modules are found are marked as 'light power spread problem' and need manual intervention to reduce the light output power spread by increasing the temperature of the optoboard or possibly installation of light attenuators to effectively increase the RX threshold dynamic range.

As the 'fast' BOC scan is insensitive to the slow turn-on effect, a 'slow' BOC threshold scan is performed at the working point delays with the same threshold resolution as the 'fast' BOC scan. The results of the 'fast' and 'slow' BOC scans are compared especially for errors in the 'slow' BOC scan at high threshold values and modules with significant differences are marked as 'slow turn-on candidate'. In the 'slow' BOC scan it is verified, that the 40 DACs threshold surrounding of the working point threshold is error-free. If errors are found the threshold working point is shifted to lower thresholds with an error-free surrounding.

To verify the set working points a 40 Mbit/s digital scan with five mask-steps and 100 injections is performed giving a bit-flip rate limit of $< 6.5 \times 10^{-8}$. Modules with a perfect digital scan result are marked as 'OK' and are disabled for the further 40 Mbit/s tuning. Modules with a low amount of errors are marked as 'marginal tuning candidates' and are disabled as well. If all digital scans of a ROD are empty or show a low number of hits this may be caused by a feature of the ROD scan engine, which breaks a digital scan if an event is not received correctly within ten consecutive repetitions. This feature cannot be disabled at the moment but it is foreseen in the next DSP code version. Which module has transmission errors cannot be unambiguously determined but the module group (DSP slave) with the problematic module is indicated. To identify the problematic module a binary search is necessary. Half of the

ROD modules are set to status 'pending' and are disabled and for the other half a three mask-step digital scan is performed. Modules with correct results are marked as 'OK' and disabled, if all modules have faulty results the split-up is continued and single faulty modules are marked as 'digital problem'. Pending modules are activated and the procedure is repeated until no pending modules are left. For all modules with 'OK' status the 40 Mbit/s configuration is stored.

The found optical tuning should work in 80 Mbit/s mode as well without further adjustment (see section 6.1.3). To verify the tuning a V0 versus RX delay scan is performed in 80 Mbit/s mode and 80 Mbit/s outlink mapping. V0 and RX delay are scanned in 13 steps from 0 to 24 DACs. For unchilled module scenarios the V0 scan can be reduced to two steps from 0 to 1 DAC. If no error-free region exists the module is marked as 'no 80 EFR' and as 'small 80 EFR' if the error-free delay range is smaller than 8 ns. The V0 with the maximal error-free delay width for all modules of a ROD is chosen and modules with a maximal error-free delay width at a different V0 value are set into 'V0 warning' status. The RX delay is adjusted 4 ns higher than the lower border of the error-free delay range. The working point is verified with a 25 mask-step digital scan and the same binary search procedure as for problematic channels in 40 Mbit/s. The working points are saved in 80 Mbit/s configuration files.

For the System Test the RX delay and RX threshold tuning algorithms have been implemented in a standalone tool which also provides visualization of BOC scan histograms and of the chosen working points. The V_{iset} and V0 were chosen by hand, following the described strategy. In the Connectivity Test after the detector assembly an alternative approach was used. For the connectivity test after the cabling of the installed detector in the experiment the full implementation of the above described procedure into STcontrol and the Pixel analysis framework is prepared in scope of a summer student project [VER07]. The tuning result of the implemented algorithm for the optical channels of an optoboard is shown in Figure 6-33.

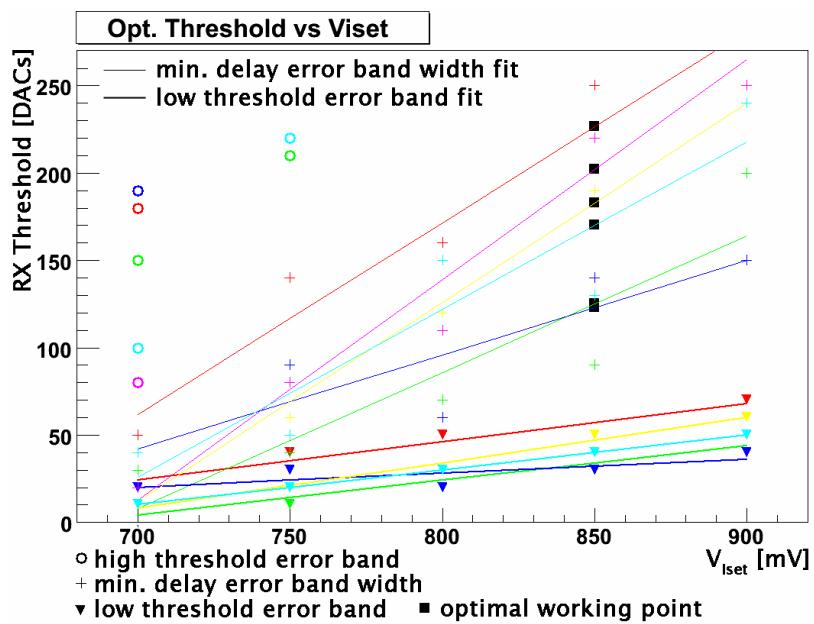


Figure 6-33 Low and high threshold error band and minimal delay error band width positions of an optoboard determined from BOC scans at different V_{iset} as well as optimal (minimal residual to 210 DACs minimal delay error band threshold position target) V_{iset} and RX threshold values [VER07]

6.3.6 Module Tuning Performance

In order to verify the threshold tuning performance of the FE pixel discriminators and to measure the noise of pixels with the System Test layout readout and service chain, threshold fine-tunings of the endcap A modules were performed and the results are compared to the production quality assurance measured thresholds and noises. Production measurements for the disk modules, to which the System Test results are compared, were performed at the Lawrence Berkeley National Laboratory after the modules have been loaded to the disk sectors in the scope of the sector quality assurance procedure. The so-called STAVE measurement is a repetition of the FLEX measurement (see e.g. [DOB04]), which were performed after the module assembly. Both check for sensor damages, abnormal FE power consumption, digital or analogue dead pixel or unconnected bumps by comparing pixel noise between biased and unbiased sensor. They perform a threshold fine-tuning and TOT calibration, measure the individual pixel threshold and cross-talk. A measurement with a ^{241}Am source is taken to verify the unconnected bump measurement and the TOT calibration. In addition the individual sensor pixel leakage currents, operational range of the module LV supply and clock, the timewalk (signal delay vs. charge) and the in-time threshold (charge at which signal is 20 ns later than at high charge) are measured. For the threshold tuning the antikill mode is used, which ensures that only the preamplifiers of the injected pixels are on and all neighboring pixel preamplifiers are off. Compared to normal threshold scans antikill threshold scans typically result, due to reduced digital crosstalk, in about 30 e^- lower threshold values and $\sim 13\text{ e}^-$ lower noise values. Since the STAVE threshold tunings were performed in antikill mode, the threshold values of antikill threshold scans are closer to the intended target threshold of 4000 e^- and have lower threshold dispersions. Therefore antikill threshold scan threshold and noise values are used as reference for the comparison. The tuning procedure used for the production tuning differs from the procedure used for the TDAC tuning in the System Test. For the production tuning a set of threshold scans with fixed TDAC values were performed with a TurboDAQ setup (similar to the setup described in section 5.2.1), the results were fitted for each pixel individually and the optimal TDAC setting was extrapolated. With the procedure used in the System Test a threshold scan is performed with a start TDAC value map and according to the result the individual pixel TDACs are incremented or decremented. The sequence is repeated until the discriminator thresholds iteratively reach their optimal setting. Since more similar to the experiment data taking scenario normal threshold tuning and threshold scans are chosen for the System Test performance analysis.

Of the 144 endcap A modules one module was disconnected due to a missing sense line, one module disconnected due to a missing NTC line, six modules not scanned due to a retracted VPIN pin at PP1, six modules not scanned because of a non-operational optical link and four modules taken out of the data set due to missing sensor HV bias voltage.

Both measurement sets have module temperatures close to the Pixel Detector design temperature of -10°C . For production tunings and threshold scans the module temperature are $-8.9 \pm 0.9^\circ\text{C}$ and for System Test tunings $-15.5 \pm 0.8^\circ\text{C}$ (see Appendix A Figure A-28). No significant dependency of the threshold, noise or their dispersions

on module temperature is observed.

The mean module threshold distributions for the endcap A modules for the TurboDAQ production tuning and the STcontrol System test tuning are shown in Figure 6-34. The fitted production mean module thresholds are $4068 \pm 28 e^-$ whereas the System Test tunings are with $4002 \pm 1.4 e^-$ much closer to the target threshold of $4000 e^-$. In Appendix A Figure A-29 and Figure A-30 the fitted production and System Test mean module threshold distributions are presented. The lack of correlation between both tunings in Figure 6-34 shows that the System Test tuning performance is independent of the tuning performance reached in production, which thus is not a module quality measure. About ten System Test tuning outliers are most probably caused by an early break of the tuning iteration since their TDAC maps show no indication of possible tuning problems and seven of the modules were readout by the same ROD and the three remaining are on another PP0. Therefore for these modules mean threshold values as good as for the majority of modules can be expected after a repeated tuning.

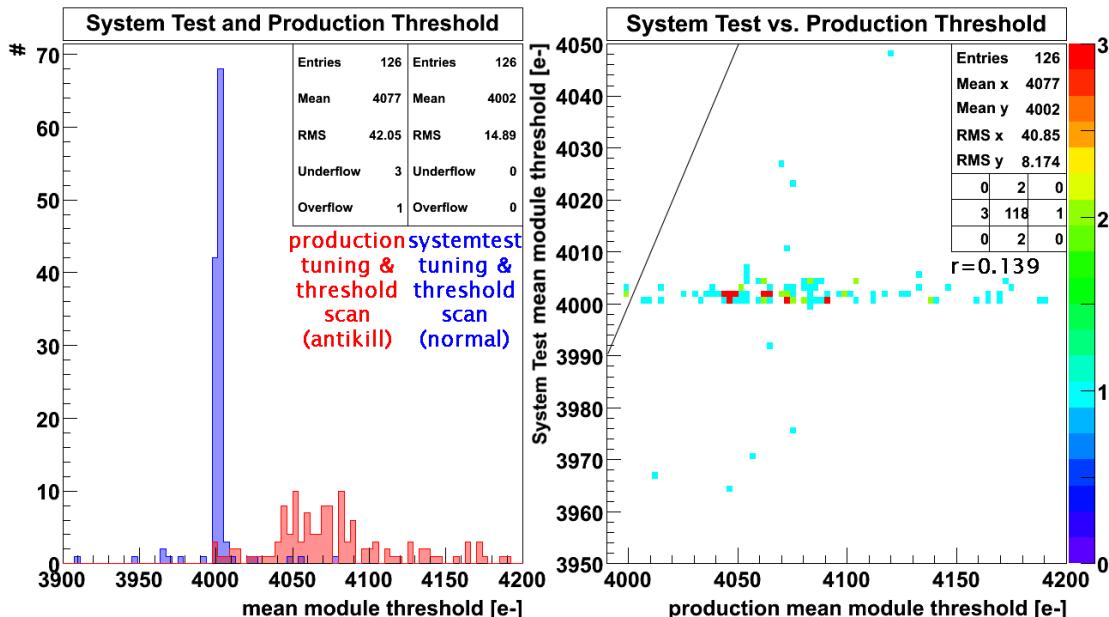


Figure 6-34 Mean module threshold comparison between the production TurboDAQ tuned and measured (antikill) thresholds and the System Test STcontrol tuned and measured (normal) thresholds of the endcap A modules

In Figure 6-35 the module threshold dispersion distributions for both tunings as well as their correlation are shown. The majority of the production tunings show a threshold distribution of $53.3 \pm 6.0 e^-$, but another about 1/3 group of modules have higher dispersions around $80 e^-$ with a tail up to $140 e^-$. With the System Test tuning about $20 e^-$ lower threshold distributions of $33.9 \pm 0.9 e^-$ are reached. The fitted dispersion distribution are shown in Appendix A Figure A-29 and Figure A-30. As for the threshold value correlation, the threshold dispersion correlations shows no dependency of the System Test threshold dispersions from the dispersion values measured during production for the majority of modules. The System Test outliers correspond to the outliers in the threshold correlation which confirms that the iterative

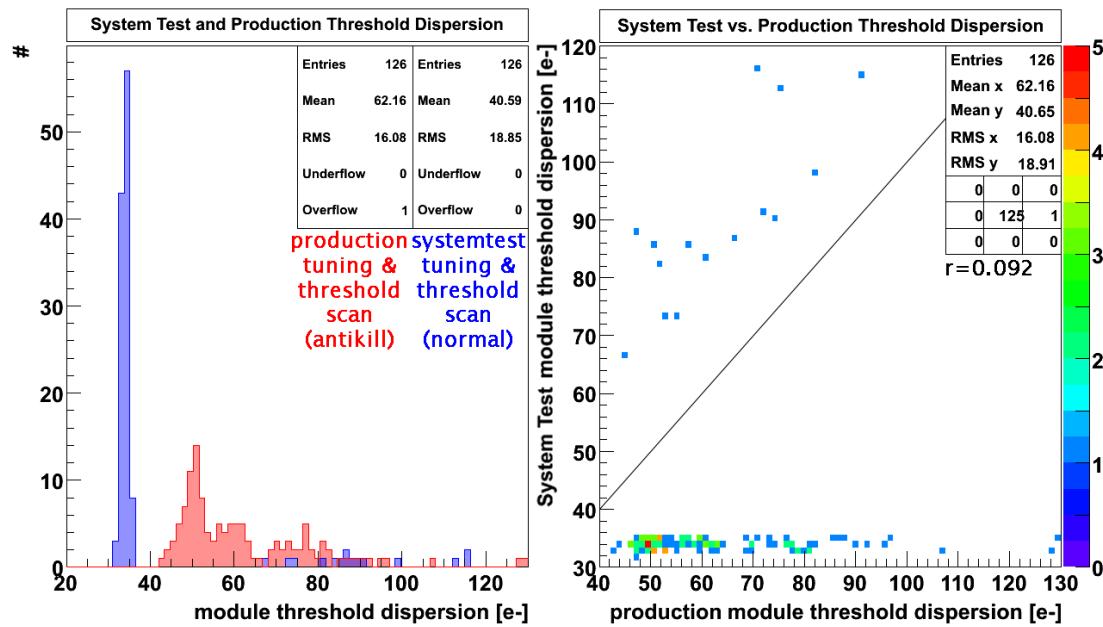


Figure 6-35 Module threshold dispersion comparison between the production TurboDAQ measured (antikill) threshold dispersions and the System Test STcontrol measured (normal) threshold dispersions of the endcap A modules

tuning was interrupted. Since the iterative tuning started from the production tuning for the outliers a correlation between the dispersions is visible. Dispersion values in the range of 30 e^- are expected for these modules with a repeated tuning.

As for the bi-stave tuning results (see section 6.2.2) the distributions of the set TDAC values show that odd DAC values are not used between 55 and 85 DAC counts. An improvement of the tuning algorithm last iteration step could make use of this untuned least significant TDAC bit to decrease the threshold dispersion further.

The noise of the pixel cells should be independent of the threshold tuning but can be measured with a threshold scan. A comparison of the noise distributions for both tunings is shown in Figure 6-36. The production measured noise of $157 \pm 5\text{ e}^-$ increases by about 10 e^- to $167 \pm 6\text{ e}^-$ which is consistent with about 13 e^- noise difference between antikill and normal threshold scan measured noise. The noise values of the two tunings measured with two different readout and service setups are well correlated with a correlation coefficient of $r=0.935$. A linear fit results in a slope of 1.15 ± 0.3 between the production and the System Test measured noises. Mean module noise values for the different pixel types are presented in Appendix A Figure A-31 for the production tuning and in Appendix A Figure A-33 for the System Test tuning. As expected due to increased capacitive load to the preamplifiers, higher noise values are observed for long, ganged and inter-ganged pixels. The gaussian fit results of the different pixel types are given in Table 6-2.

The module noise dispersion distributions for both tunings are compared in Figure 6-37. Slightly lower noise dispersion values are observed for the System Test setup for normal, long and ganged pixels, but slightly higher dispersion values for inter-ganged pixels. Fitted results for the different pixel type noise dispersion distributions (see

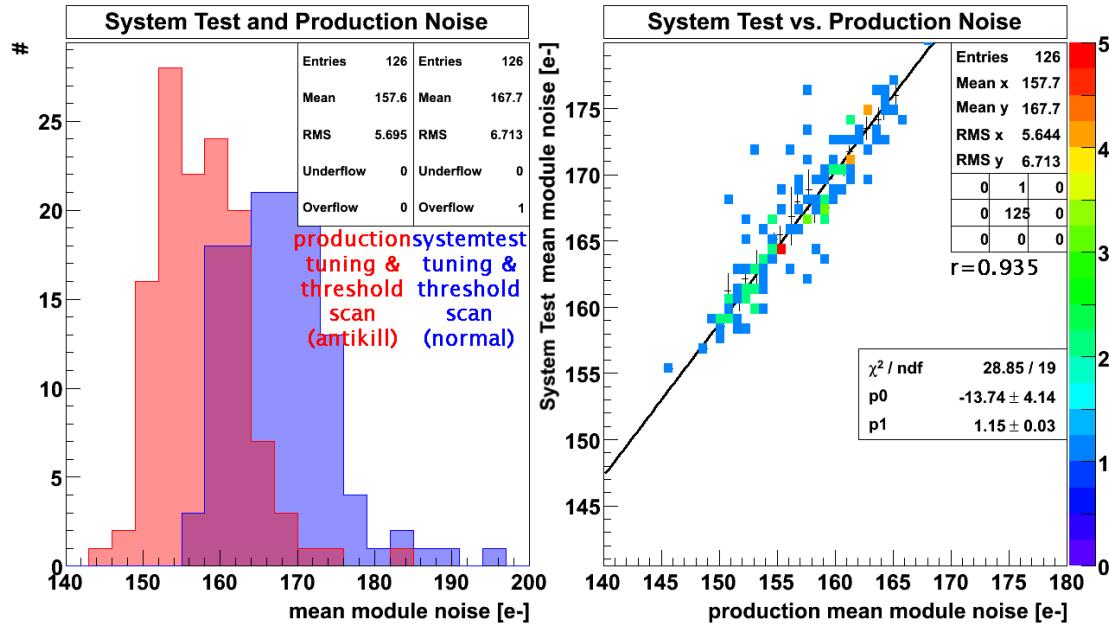


Figure 6-36 Mean module noise comparison between the production TurboDAQ measured (antikill) noises and the System Test STcontrol measured (normal) noises of the endcap A modules

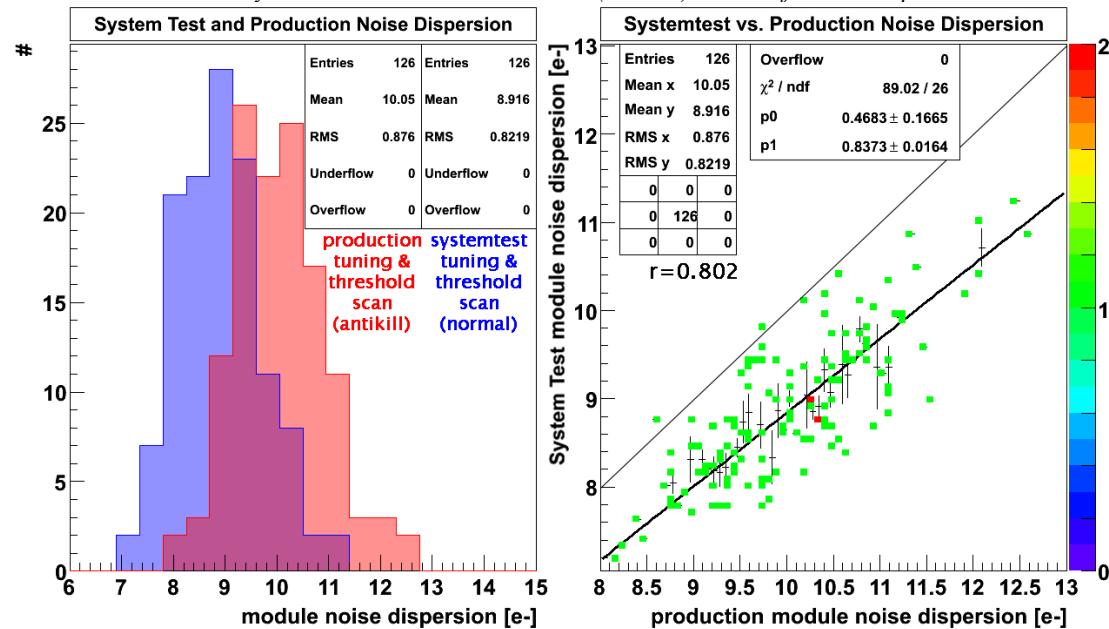


Figure 6-37 Module noise dispersion comparison between the production TurboDAQ measured (antikill) noise dispersions and the System Test STcontrol measured (normal) noise dispersions of the endcap A modules

Appendix A Figure A-32 and Figure A-34) are listed in Table 6-2. The noise dispersion values of the two measurement sets are reasonable correlated ($r=0.802$) and a linear fit shows a slope of 0.84 ± 0.02 between the production and the System Test measured noise dispersions. Typically noise dispersions of antikill threshold scans are slightly lower than dispersions measured with normal threshold scans and the same setup. Possible reasons for the lower System Test noise dispersions are

different power supplies and service chain as well as a different DAQ readout chain (e.g. optical link) and grounding scheme.

The System Test results verify an excellent threshold tunability of the Pixel modules with the final readout system and show no indication for a significant noise increase with the final detector services. The threshold dispersion could be additionally decreased by including the tuning of the least significant TDAC bit into the last iteration step. A direct comparison of module noise and threshold performance between the production and the System Test tuning (both threshold scans performed with the System Test setup) with similar results can be found in [WEI07].

<i>Value:</i>	<i>Production: (antikill)</i>	<i>System Test: (normal)</i>
mean module threshold	$4068 \pm 28 \text{ e}^-$	$4002 \pm 1.4 \text{ e}^-$
module threshold dispersion	$53.3 \pm 6.0 \text{ e}^-$	$33.9 \pm 0.9 \text{ e}^-$
module mean noise (normal pixels)	$157.2 \pm 5.1 \text{ e}^-$	$167.2 \pm 5.5 \text{ e}^-$
module mean noise (long pixels)	$179.3 \pm 8.5 \text{ e}^-$	$199.5 \pm 1.1 \text{ e}^-$
module mean noise (ganged pixels)	$216.5 \pm 17.9 \text{ e}^-$	$306.1 \pm 29.4 \text{ e}^-$
module mean noise (inter-ganged pixels)	$161.9 \pm 5.6 \text{ e}^-$	$182.7 \pm 6.9 \text{ e}^-$
module noise dispersion (normal pixels)	$10.1 \pm 0.9 \text{ e}^-$	$8.9 \pm 1.0 \text{ e}^-$
module noise dispersion (long pixels)	$11.9 \pm 1.3 \text{ e}^-$	$10.7 \pm 1.6 \text{ e}^-$
module noise dispersion (ganged pixels)	$37.4 \pm 12.6 \text{ e}^-$	$26.6 \pm 7.7 \text{ e}^-$
module noise dispersion (inter-ganged pixels)	$13.2 \pm 1.5 \text{ e}^-$	$14.55 \pm 2.3 \text{ e}^-$

Table 6-2 Production and System Test tuning comparison of module threshold and noise performance

6.3.7 Noise Occupancy at Low Sensor Bias Voltage

The production of the Pixel sensors was accompanied by intensive quality assurance measurements (see [WEB04] and [KLA05]). During the assembly of the bare modules and the assembly of the Pixel modules, sensor leakage current versus bias voltage measurements (IV-curves) were performed to ensure that the sensors were not harmed by mechanical stress. These measurements were repeated after mounting of the modules on staves. During the CONN stave cabling connectivity test (see section 5.2.2) the sensor leakage currents at a bias voltage of -150 V were measured to verify on one hand the connectivity of the HV lines to the sensor. On the other hand the measurements were used to check for an increase of the leakage current due to mechanical stress on the sensors. After the bi-stave assembly and their integration into half-shells the leakage current measurements were repeated (BIST measurement see section 5.3.1). Since in the System Test setup one ISEG HV supply channel was used per Pixel module, a measurement of IV-curves up to -600 V was possible. A

concurrent measurement of all endcap sensor IV-curves was implemented into the DCS. The IV-curve were measured in the dark System Test dry box, so that similar light conditions compared to the quality assurance STAVE measurements can be assumed. The HV was ramped up in 5 V steps from 0 to -600 V with a settling time of 10 s before each measurement and the ISEG channels were set to a current limit of 1 mA.

In Figure 6-38 the 144 IV-curves of the endcap A sensors are shown. On the right side of Figure 6-38 the correlation of the System Test leakage current measurements versus the STAVE leakage current measurements are shown. For both data sets the leakage currents at the nominal unirradiated operation voltage of -150 V were determined from IV-curves measured at about -15°C. The current resolution of the ISEG supplies used in the System Test is 100 nA. Thus, errors of 100 nA are assigned to the System Test measurements. Out of the 144 IV-curves 43 show zero current readings at -150 V, but sensible readout at higher voltages, therefore leakage currents below 100 nA can be assumed. In the final experiment layout up to seven sensors will be supplied by one ISEG channel and leakage current measurements will be provided by the HV-PP4s. The STAVE measurements were performed with a high precision pico ammeter and the errors are not visible in the correlation plot. None of the modules show an early breakdown below -150 V which could limit the operation range. Two sensors have leakage currents exceeding 20 μ A at the operation voltage. One of them had a high leakage current already at the STAVE measurement. The other one shows an ohmic (linear) IV-curve with high slope indicating a low sensor resistance not observed in the STAVE measurement. High leakage currents do not generally limit the operation range as early breakdowns, but may cause more noisy modules with increased power consumption. Other modules show up to three orders of magnitude higher leakage currents compared to the STAVE measurement and have only a very low correlation ($r=0.61$) between both measurement sets.

Besides the breakdown voltage, the depletion voltage of the silicon sensor is an important quality characteristic for the Pixel Detector. As pointed out in sections 2.5

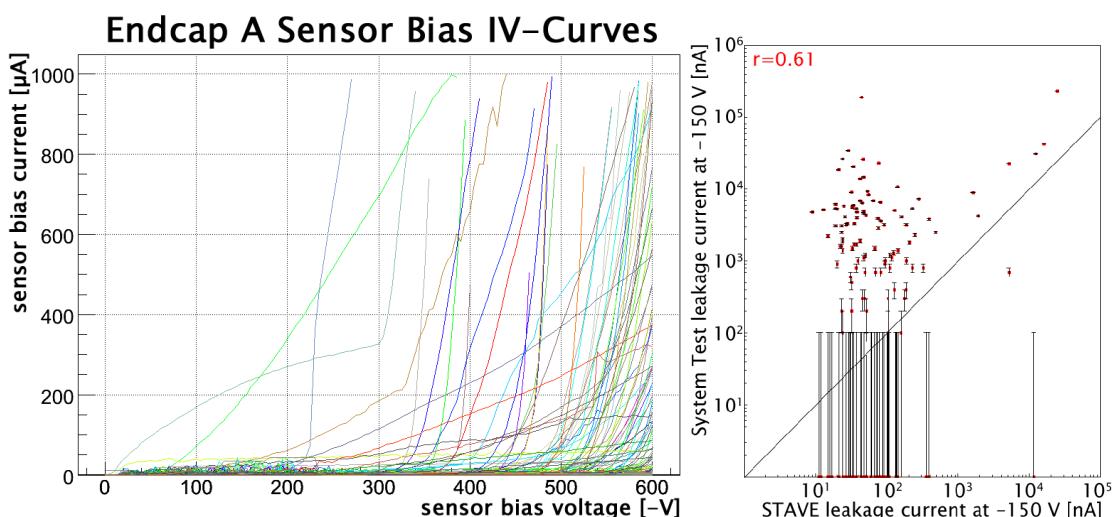


Figure 6-38 Endcap A sensor IV-curve leakage current measurements and correlation of sensor leakage currents at -150 V for the System Test versus the STAVE measurements

and 4.3.2 it changes with increasing irradiation of the sensor. Therefore, it is a measure for the integrated radiation dose seen by the sensor. Before the sensor bulk type inversion only full depletion allows a sensible space resolved particle detection, because below full depletion the pixels are shorted. With increasing radiation dose the depletion voltage decreases until type inversion. After type inversion the depletion voltage increases with increasing radiation dose and requires an increase of the operation voltage up to the maximal nominal operation voltage. Beyond this point the depletion depth decreases, which involves a decrease of the charge collection efficiency. During data taking phases the charge collection efficiency can be used to measure the depletion depth. Via the saturation of the depletion depth (or charge collection efficiency) with increasing sensor bias voltage the depletion voltage can be measured.

Before type inversion the depletion voltage is interesting to verify the integrated radiation dose and to check for annealing and reverse annealing during maintenance periods without beam collisions. A measurement of the module noise occupancy versus sensor bias voltage can be used to measure the depletion voltage and has the advantage over the charge collection efficiency method, that it can be performed in maintenance periods without beam collisions. The System Test setup was used to study this method with a fixed trigger frequency generated by the external HP 8110A pulser. The same trigger and readout chain as described for the cosmic data taking (see section 6.3) was used to readout noise hits from the endcap A modules. The modules were tuned to thresholds of $4000e^-$ (see section 6.3.6). A trigger frequency of 5 kHz allowed a stable module readout at the highest expected noise occupancy values (lowest bias voltage) and was not increased for higher bias voltages to maintain equal readout conditions. The noise occupancy versus sensor bias voltage curves for 117

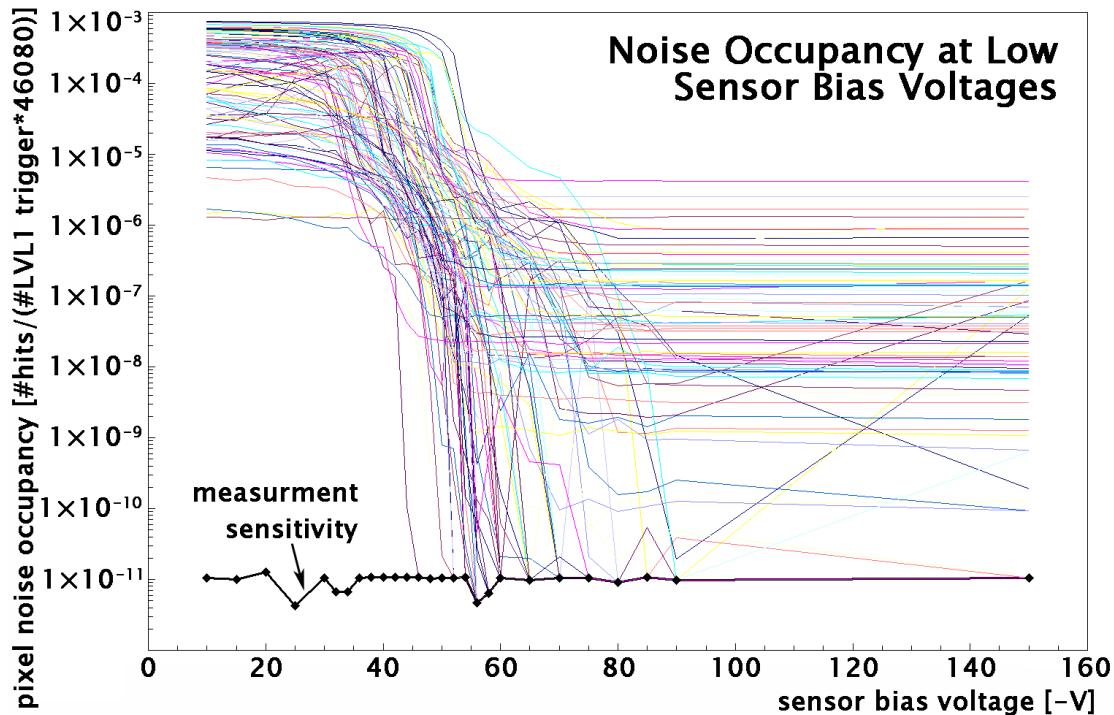


Figure 6-39 Noise occupancy measurement of the endcap A modules at the transition between fully depleted and partially depleted sensor

endcap A modules are shown in Figure 6-39. Between -10 V and -30 V as well as between -60 V and -90 V the bias voltage was scanned in 5 V steps, whereas in the expected depletion range between -30 V and -60 V 2 V steps were used. The black line at the bottom indicates the measurement sensitivity. For each bias voltage value between two and five million LVL1 trigger were recorded. This results in noise occupancy measurement sensitivities [68% C.L.] of:

$$O_{sensitivity} = \frac{1}{LVL1 \cdot pixel} ; \quad LVL1 : \text{number of LVL1 trigger} \\ pixel : \text{number of pixels in module 46080} \quad [6.1]$$

and in noise occupancies of:

$$O = \frac{\text{hits}}{LVL1 \cdot pixel} ; \quad \text{hits} : \text{pixel noise hits in module} \quad [6.2]$$

The standard deviation of hits is given by binomial statistics with:

$$\sigma^2 = LVL1 \cdot pixel \cdot O(1-O) \quad [6.3]$$

and the error of the noise occupancy measurement by:

$$\Delta O = \frac{1}{LVL1 \cdot pixel} \sqrt{LVL1 \cdot pixel \cdot O(1-O)} = \sqrt{\frac{O(1-O)}{LVL1 \cdot pixel}} \quad [6.4]$$

For low noise occupancies above the depletion voltage the binomial statistics can be assumed without restrictions. The individual pixels are isolated, no significant crosstalk between pixels exist and low module hit occupancies do not cause hit loss due to buffer overflows in the FE, MCC or ROD. Below the depletion voltage the pixels are shorted through the sensor and high module occupancies may cause hit loss. Therefore, the measurement of the individual pixel noise occupancies is not independent and in the calculation of the noise occupancy measurement error this effects would need to be taken into account. For the presented studies, which have the aim to verify the usability of the method for the Pixel Detector, the binomial errors are used for all noise occupancy values. For bias voltages above -70 V most of the noise occupancy curves are stable and only some few curves show single outliers or an unexpected step in the depleted noise occupancy values. Also most noise occupancies below -30 V are stable and only some few show decreasing noise occupancy with decreasing bias voltage most probably due to buffer overflows caused by too high occupancies.

It can be assumed that a pixel changes from its depleted noise occupancy to higher undepleted noise occupancies when it is shorted to neighboring pixels at a bias voltage threshold $V_{threshold}$. With the ansatz that the bias voltage thresholds of a module have a Gaussian distribution with a RMS V_{noise} , the module noise occupancy curves can be described by an s-curve:

$$O(V_{bias}) = O_{depl} + \frac{O_{undepl} - O_{depl}}{2} \int_{-\infty}^x e^{-t^2} dt \quad \text{with} \quad t = \frac{\langle V_{threshold} \rangle - V_{bias}}{\sqrt{2} \cdot V_{noise}} \quad [6.5]$$

In order to find appropriate fit parameter start values for the s-curve, constant value fits are performed for the depleted noise occupancy between -80 V and -150 V as well as for the undepleted noise occupancy between -10 V and -30 V. The results are set together with $V_{threshold} = -50$ V and $V_{noise} = 10$ V as start parameters for an s-curve fit of

the \log_{10} noise occupancy curves. For this first s-curve fit the errors of all histogram bins are set to equal values of one. This provides a robust fit and the fit is not dominated by the relative low errors at the depleted noise occupancy plateau. Examples of low χ^2 fit results and of histograms with derivation from the expected s-curve distribution shape are shown in Appendix A Figure A-35. The s-curve fit well describes the undepleted and depleted noise occupancy plateaus. For distribution shapes with outliers or not constant plateaus, the fit determines the plateaus more precise compared to the fixed interval constant fits, because the plateau interval is adjusted by the fit. The distributions of the \log_{10} depleted and undepleted noise occupancies are presented in the upper row of Figure 6-40. In the depleted noise distribution two groups of modules are visible. For 45 modules low noise occupancies of about 10^{-11} , which is consistent with the measurement sensitivity, are measured. These modules have no noisy pixels or they are masked in the modules by disabling the discriminator output for the corresponding pixels. Modules with noise occupancies between 10^{-9} and 10^{-6} have typically a small number of unmasked noisy pixels. For the realistic data taking case pixels with a single pixel noise occupancy above 10^{-5} can be expected to be masked in the FE but tighter cuts in the data analysis could be used to minimize the effect of the few noisy pixels on the mean module noise occupancy. For

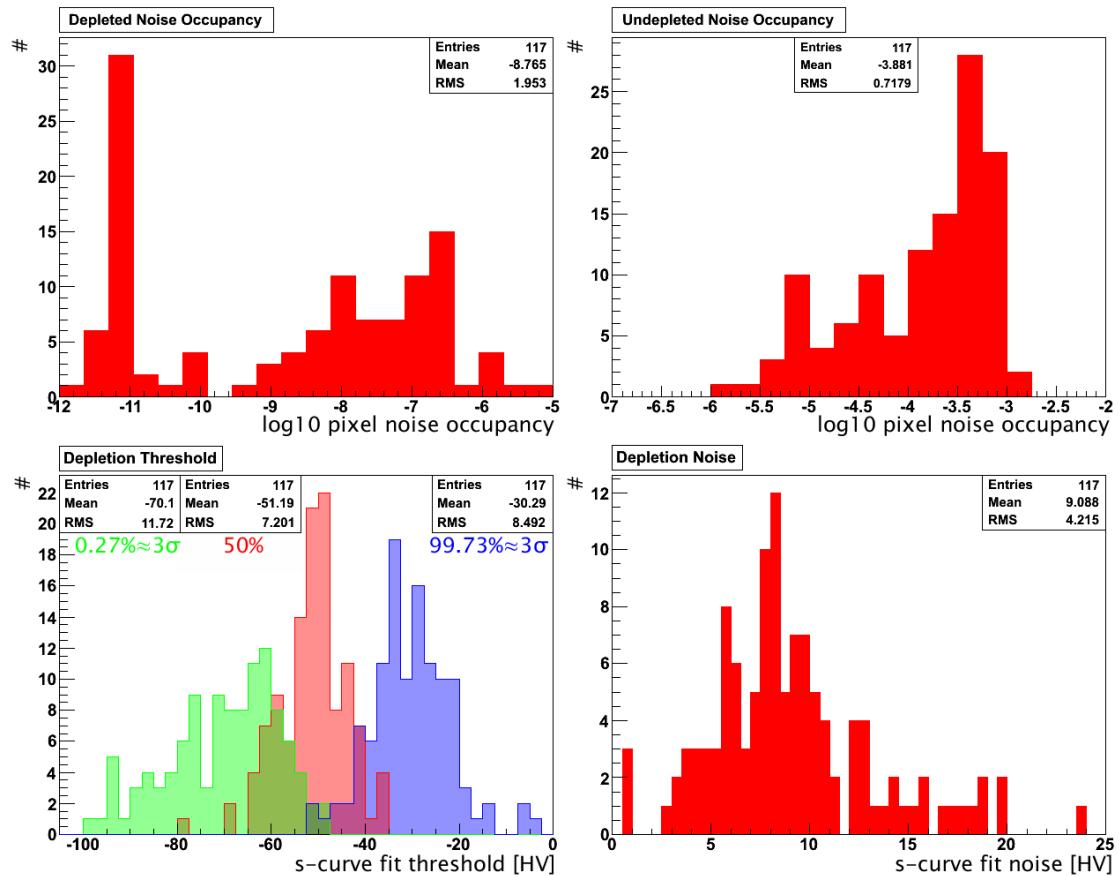


Figure 6-40 \log_{10} noise occupancy s-curve fit results of the endcap A modules. The upper two histograms show the undepleted and depleted noise occupancy distributions. The lower left histogram shows the s-curve depletion voltage mean threshold (50%), depletion voltage (3σ) and undepletion voltage (3σ) distributions. In the lower right histogram the s-curve fit depletion threshold noise is shown.

the undepleted plateau noise occupancy values between 10^{-6} and 10^{-3} are measured. Only a small decrease of the distribution width is expected with masked noisy pixels. The mean depletion threshold voltage (50% s-curve value) and the depletion noise voltage distribution (1 σ Gaussian threshold distribution width) are shown in Figure 6-40. Since the s-curve is fitted to the \log_{10} noise occupancy instead of the noise occupancy itself, it does not describe the transition close to depleted plateau very well. Further consequences are that the depletion threshold and noise voltages are determined in the logarithmic scale and therefore have higher absolute values. By decreasing the absolute threshold voltage 10 V and the noise by 2.5 V the logarithmic scale s-curve fit provides good start parameters for a linear s-curve fit with binomial errors. In Appendix A Figure A-36 some example results of the linear s-curve fits are presented. For 55 out of the 117 modules the noise occupancy curves are well described by the linear fits, which have low χ^2 values. Other fit results have significantly higher χ^2 values. Due to the much lower errors of the depleted noise occupancy bins, the fit typically agrees well with the depleted plateau. The binomial errors increase with increasing noise occupancy values, so that the low value noise occupancy transition bins have higher weights than the undepleted plateau bins. This can result in fits with large discrepancies especially in the undepleted plateau region if the transitions have deviations from the expected s-curve shape close to the depleted plateau. For about 25% of the modules a double s-curve transition is observed, indicating that two groups of pixels with different mean depletion threshold voltages exist in the module. Even though the fit follows mostly the s-curve closer to the depleted plateau, which is interesting for the depletion voltage determination, the shift of the curve by the upper s-curve can result in shifts of the threshold and noise voltages of several volts. An additional fit with a double s-curve is expected to improve the precision of the depletion voltage determination for these cases. In the remaining quarter sensors, numerical fit problems are observed especially if more than seven orders of magnitude are between the depleted and undepleted plateaus. An improved adjustment of the fit parameters is expected to solve these problems. The 50% depletion threshold and depletion noise voltage distributions for the 55 low χ^2 fits are shown in Figure 6-41. The 4 σ s-curve voltage, representing a sensor bias

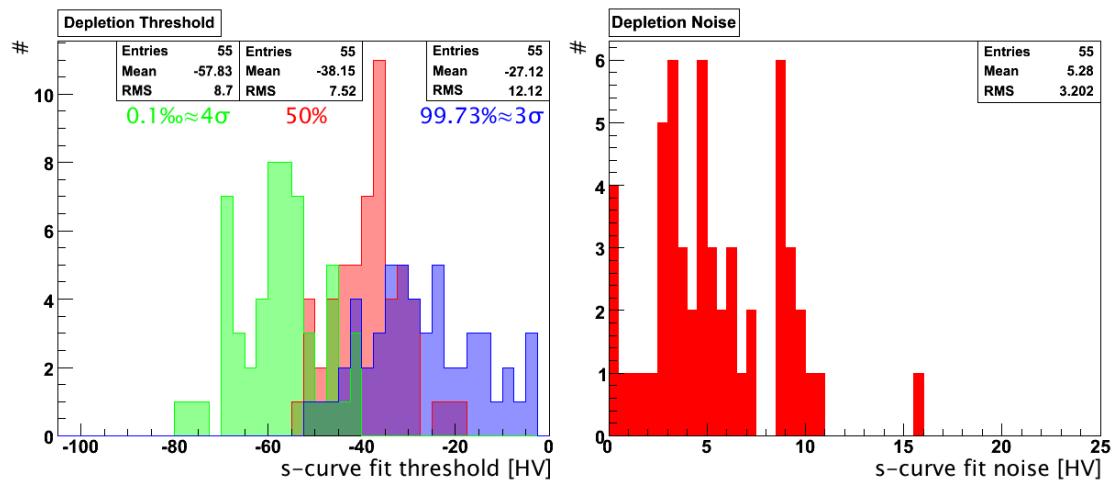


Figure 6-41 Linear noise occupancy s-curve fit results. The left histogram shows the s-curve depletion voltage mean threshold (50%), depletion voltage (4 σ) and undepletion voltage (3 σ) distributions. In the right histogram the s-curve fit depletion threshold noise is shown.

voltage with only 0.1% of the module pixels can be expected to be under-depleted, are used to determine the depletion voltage. The depletion voltage distribution is with a value of 57.8 ± 8.7 V in the expected range. To measure the precision of this depletion voltage determination method a comparison studies to alternative methods (e.g. capacitance versus bias voltage method [WEB07]) is desirable. For the undepletion voltage, the voltage of no further increase of the noise occupancy with decreasing bias voltage, a more loose cut of 3σ is used and results in -27 ± 12 V.

Typical module hitmaps are shown in Appendix A Figures A-37 to A-40. For undepleted sensors no or only a low number of noisy pixels are visible. The noise occupancy typically starts to increase at the ganged pixels in the middle of the modules and at patterns of mostly two sets of interleaved semicircle, which stretch across the entire module. They are similar to known doping concentration rings of the sensor wafers, but due to the sensor tile positions on the silicon wafer the known doping rings are centered close to the middle of the module (Tile 2) or show only one set of interleaved semicircles (Tile 1 and Tile 3). Another observed pattern with stripes along the FE pixel rows is shown in Appendix A Figure A-37. The continuation of the semicircle patterns over FE edges could indicate that the reason for the patterns are sensor effects. Another possible reason for the continuation are FE wafer effects, but with the requirement that neighbored FEs on the wafer are neighbored on the module as well. Some interrupts of the patterns at FE borders and the flip between the semicircle patters coinciding with the FE flip between the two module FE rows support this assumption. With decreasing bias voltage an increasing number of pixels show hits. For most modules hits are observed in all pixels at low bias voltages. The hit number patterns are observed for low bias voltages as well and do not change their structure. For some modules with low undepleted noise occupancy (e.g. Appendix A Figure A-39) the statistics is not sufficient to see hits in all pixels. Some modules have FEs, which significantly show higher hit numbers compared to other FEs on the module. Due to the increased capacitive load of long and ganged pixels and the associated higher preamplifier noise these types of pixels show higher hit numbers. At the undepleted edge of the transition, ganged pixels at the module border show higher hit numbers than in the middle of the module, whereas at the depleted edge of the transition the ganged pixels in the module center show higher hit numbers. No eye-catching correlation between the hitmaps and the success of the linear s-curve fits are observed, but a detailed analysis of the hitmaps for the different pixel types would help to better understand the noise occupancy versus bias voltage curves. For example the existence of a second s-curve in the transition is most probably caused by a different mean threshold or noise value for ganged pixels.

For this study fixed measurement parameters of about two million LVL1 triggers with a fixed trigger frequency of 5 kHz were used for all bias voltage measurement points. Thus, each of the 27 measurement points took six minutes for all modules and an entire scan could be performed in about three hours. With a variation of the trigger frequency and the number of LVL1 triggers according to the expected noise occupancies at each bias voltage value, much faster scans can be expected. At the depleted plateau the readout should be possible with the full LVL1 trigger frequency of 75 kHz and at the undepleted plateau the number of LVL1 triggers could be reduced until similar error values are reached for all bias voltage measurement points. This should reduce the scan time to a tenth. By scanning along decreasing sensor bias

voltages only until a significant increase of the noise occupancies is measured the scan time could be further decreased. An implementation of a simple module hit counting mode in the ROD online monitoring would allow an online analysis of the results.

Despite of the not fully developed analysis and an outstanding comparison to other depletion voltage determination methods, the usability of the noise occupancy versus bias voltage method for the Pixel Detector operation was demonstrated. It is expected to provide precise and fast depletion voltage measurements of the sensor bulks before type inversion and to allow monitoring of the integrated irradiation dose. Compared to other methods it has the advantages that measurements can be performed without change of the power supply chain and no beam collisions are necessary. In the detector maintenance periods it can be used to steer the Pixel Detectors temperature profile according to the transition between annealing and reverse annealing. This way it can help to achieve the best possible detector lifetime.

6.3.8 Endcap System Test Results

The endcap A was operated with the System Test setup for three months including long time round-the-clock operation for more than one week. This gave the possibility for an operator training and important experiences for the detector commissioning and operation were collected. A unification of the detector naming convention and a big step in the online software development were reached. The cooling system was experienced to be reliable and stable aside from minor problems with the leak tightness of the coolant tubes. Further improved stability compared to the bi-stave operation was experienced with the DCS and a comfortable and safe operation of the detector was possible by using the FSM. The power supply system had the good bi-stave operation experienced performance and changes of the PP2 regulators, the revised controller board FPGA programming and the enhanced PP2 FIT command sequence showed the desired improvements. Power-up and switch-off procedures were qualified for the detector operation and were implemented into the FSM. For the interlock system a reliable switch-off of service components in case of detector risks was observed, which allowed safe operation even close to interlock conditions. The stability and ease of use of the DAQ software improved and a new implemented optical tuning scan could be successfully tested.

For some optoboard decreasing light output power and increasing light output power spread between different channels were observed with decreasing optoboard temperatures below 10°C. Other optoboard showed stable light output power and power spread down to -10°C. The optoboard low temperature behavior was studied and light power and power spreads were measured with different measurement methods. This triggered the mounting of V_{Iset} bypass capacitors on the optoboard and enhanced optoboard production quality assurance measurements. Optoboard covers and heaters were added to the SQP design in order to allow optoboard operation temperatures above 10°C and could be qualified. The differences between two optical link parameter scans were systematically studied. Differences between the results indicated the existence of a slow turn-on behavior of the light output power and could be proved with different measurement methods. Checks for slow turn-on behavior were also included to the optoboard quality assurance measurements. A optical tuning

procedure was developed in order to allow the optimal setting of the optical tuning parameters in consideration of the observed optoboard behavior.

For optoboard temperatures between 10 and 15°C in the time-frame of the System Test with the described optical tuning procedure 134 out of the total available 144 optoboard channels could be optical tuned in 40 Mbit/s mode. From the ten (7%) untunable channels six were caused by a retracted V_{PIN} pin in a PP1 connector, one by a not working RX channel of an optoboard and three were caused by a TX problem of another optoboard. The latter optoboard showed a temperature dependence for the three problematic TX channels, which worked properly $\sim 10^\circ\text{C}$ optoboard temperature, but the corresponding three modules did not receive XCK at $\sim 7^\circ\text{C}$ and below. Thus none of the observed problems at 40 Mbit/s and optoboard temperatures around 10°C were related to high power spread or to slow turn-on behavior. In 80 Mbit/s mode additional 20 optoboard channels (14%) were untunable. Seven channels showed failing digital tests coinciding with no error-free region in the V0 versus RX delay scan. Eight channels had failing digital scans coinciding with small error-free regions. Four channels failed digital tests though the width of the error-free region in the V0 versus delay scan were in usual values. On one channel no data could be readout which might have been caused by another readout problem. Considering the limited available time-frame for the 80 Mbit/s tuning a decrease of problematic channels with more careful tuning can be expected. For the presented results the determined optimal V_{Iset} s are distributed from 0.7 to 0.9 V. One time 0.7 V, eight times 0.75 V, 11-times 0.8 V, one time 0.9 V and three times 0.95 V were found to be the optimal optoboard V_{Iset} . Since the quality of the System Test optoboards intendedly were lower than the detector integrated optoboards, significantly less problems are expected in the final detector. This could be proven by the Connectivity Test of the integrated detector subsequent to the System Test and before the detector installation in the experiment.

The excellent module tuning performance from the bi-stave System Test could be confirmed and a sample of 126 modules result in a mean module threshold of $4002 \pm 1.4 \text{ e}^-$ with threshold dispersion of $33.9 \pm 0.9 \text{ e}^-$. Comparison with production measurements showed no indication for increase of the mean module pixel noise of $167.2 \pm 5.5 \text{ e}^-$ and module noise dispersions of $8.9 \pm 1.0 \text{ e}^-$.

With the trigger and DAQ system fixed trigger frequencies up to 55 kHz were reached. Noise occupancies studies with reduced thresholds and decreased sensor bias voltage were performed. Noise occupancies down to 10^{-11} could be measured. During the cosmic data taking combined scintillator trigger frequencies of $\sim 13 \text{ Hz}$ were measured which agrees with the Monte Carlo simulated trigger frequencies of 16-18 Hz. More than a million cosmic muon triggered events could be recorded and serve as a key dataset for studies and verification of the online monitoring, offline software reconstruction and analysis chain including calibration and alignment.

Chapter 7

From Online to Offline – Online Monitoring & Bytestream Converter

The data output of the ATLAS Pixel Detector, as it comes from the FEs through the MCC, optoboard and ROD out of the ROB is a sequence of 32-bit words, the so called bytestream. To be usable it has to be decoded and the contained hit and error information has to be stored in data objects understandable by the subsequent analysis routines. The implementation of the bytestream data quality analysis for online monitoring and of the ATLAS Pixel bytestream converter in the Athena framework are described in this chapter.

7.1 Bytestream Format

An ATLAS full event [BEE05] is build of fragments. Each fragment has a header, which contains all information for event formatting. A full event fragment is an accumulation of sub-detector fragments and each sub-detector fragment is an accumulation of ROS fragments. Again a ROS fragment is an accumulation of ROB fragments, which each contains a single ROD fragment. Each ROD fragment contains several module fragments, which contain the hits of the corresponding module. A schematic view of the raw event format is shown in Figure 7-1. A detailed view of the ROD fragments and the module data format down to single bit level can be seen from Appendix A Figure A-41.

Event, sub-detector, ROS and ROB fragment headers are a sequence of 32-bit words. They contain a header marker, the total fragment and header size, a format version number of the fragment and a source identifier of the fragment building device. Additionally they contain the number of generic status elements, which contain status words for the data within the fragment, followed by the generic status elements themselves, as well as the number of fragment type specific elements followed by the elements themselves. Due to the S-LINK data transmission between ROD and ROB, the ROD fragments have a header and trailer, which provide the formatting information together. ROL transmission of event fragments between the ROD and the ROB are framed with a 'Beginning'- and 'End of Fragment' marker with S-LINK status

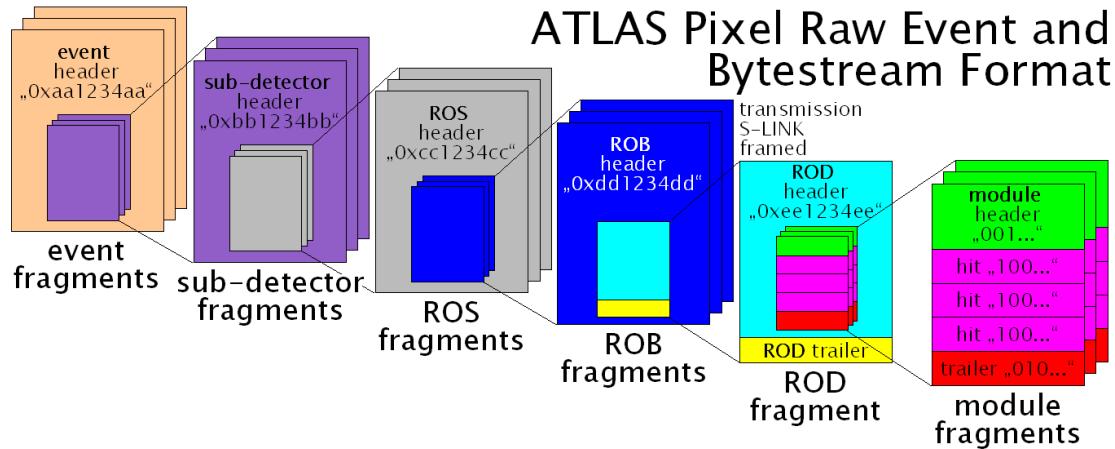


Figure 7-1 ATLAS Pixel Raw Event and Bytestream Format

words in the lower 16 bits and a fixed marker header in the upper 16 bits. ROD headers miss the total fragment size word but contain additional 32-bit words for run number, extended LVL1 ID, BCID, LVL1 trigger type and detector event type (ROD or TIM). The header is followed by the data block which contains all module hit data of the corresponding ROD and a status block which contains a counter for words with errors and bit error flags. ROL markers are removed by the receiving ROB but any contained status flags are preserved in the second status element of the status block. The number of status elements and of data elements as well as the position of the status block (before or after the data block) are contained in the ROD trailer.

The ROD data block contains for each module connected to the ROD a module header, a module trailer and in between for each hit a 32-bit hit word. Three header bits in each word are used to distinguish between the different word types. The header contains the module ROD link number to identify the module, the BCID, the L1ID and skipped L1IDs from the MCC as well as preamble, time out, BCID and L1ID error flag bits. A preamble error indicates a bit-flip in the 5-bit module header, a time out error indicates that a link has not received data in an adjustable timeout period and BCID and L1ID errors indicate a mismatch between the module header BCID and L1ID and the ATLAS TTC BCID and L1ID. Hit words contain a FE chip identifier, the hit TOT value and the hit row and column. Module error words like error flag, raw data or data time out words can follow the hit words. The error flag 32-bit words contain a FE chip identifier and different error flag bits from the MCC or the corresponding FE. If a field separator synchronization bit in the MCC to ROD serial data stream is not detected the ROD link decoder switches to raw data mode and the serial data stream is written into raw data words until a module trailer is detected. The module trailer contains header trailer limit error and data overflow flag bits. Trailer bit errors are not checked in the ROD since hits with zero row, column and TOT would be interpreted as a trailer with an error. A header trailer limit error shows that a ROD de-randomizer FIFO was filled above a programmable threshold, the formatter serial decoder block is switched to header trailer mode suppressing hit writing to the link FIFO and thus hits are lost. The data overflow flag indicates that the link FIFO has an overflow, module headers and trailers are lost and thus the readout synchronization is lost. More details about the bytestream format can be found in [JOS06].

7.2 Online Monitoring

To identify readout problems at different readout chain stages, monitor the data quality and some aspects of detector performance during data taking the bytestream data needs to be decoded and the recovered hit and error information needs to be clearly displayed in histograms that can be accessed and analyzed by data taking shifters.

7.2.1 Online Monitoring Framework

The ATLAS online monitoring infrastructure uses the two ATLAS TDAQ services EMS¹⁷⁸ and OHS¹⁷⁹ to build the online monitoring system. Events or event fragments are provided to the EMS by online samplers which can run on the ROD, ROS or SFI readout chain components. For development, debug and performance study purposes previously recorded or simulated bytestream raw data files can be fed into the EMS by a file sampler. The EMS is responsible for the sampling of events, which is necessary due to the enormous data bandwidth (~ 1.8 GB/s module fragments for the Pixel Detector) and their distribution to the GNAM¹⁸⁰ monitoring process core [ADR06],[DEL06]. The modular, detector independent, code duplication avoiding and TDAQ controllable FSM core is responsible for the common actions like identification of ROD fragments and distribution of ROD fragments lists to sub-detector decoding dynamic libraries. The decoding libraries decode the ROD fragments and store the decoded data in a transiently in memory stored ROOT [BRU97] Tree. Histogramming dynamic libraries book ROOT histograms and return a list of them back to the core for central management like publishing to the OHS. They have access to the entire ROOT Tree, this means all decoded data by the different sub-detector decoding libraries and correlation among different sub-detectors is possible without necessary decoding code duplication. The histogramming libraries retrieve from the ROOT Tree the decoded information of one or more sub-detectors, perform analysis and fill the histograms. The core centrally handles the publication of the histograms to the OHS. In order to optimize the available network resources and to compromise between high event sampling rate and high histogram publishing rate, a sequence of histogram publications is started whenever an adjustable amount of events are filled into histograms or whenever an adjustable timeout is reached. The histogram publication sequence is broken if an adjustable amount of bytes is transmitted to the OHS and is continued at the next publication start. The histograms in the OHS are logically organized in containers and can be accessed by logical paths. Received histograms are pushed to the separate OHP¹⁸¹ application. The OHP interactively displays by regular expression selected histograms. It allows to select and arrange histograms as well as change their graphical layout for shifter panels by a configuration file. It is possible to interact with the histograms like zoom on axis or

¹⁷⁸ Event Monitoring Service

¹⁷⁹ Online Histogramming Server

¹⁸⁰ GNAM is Not AtlMon

¹⁸¹ Online Histogram Presenter

perform a fit. All subscribed OHS histograms are accessible in an expert panel through a folder tree. The OHP allows to send commands through the OHS to the GNAM core. These commands can be used to reset or rebin histograms during runtime. They can be additionally used to individually set for each histogram at runtime if it is reset at the start of a new run, if the histogram is filled and if the histogram is published to the OHS. This allows to monitor important data quality and detector performance parameters with a low granularity but high sampling and publish frequencies in the standard case. For readout chain debugging or for special detector performance studies high granularity and additional histograms can be dynamically appended. The data-flow and command-flow through the monitoring infrastructure for the Pixel online monitoring is illustrated in Figure 7-2.

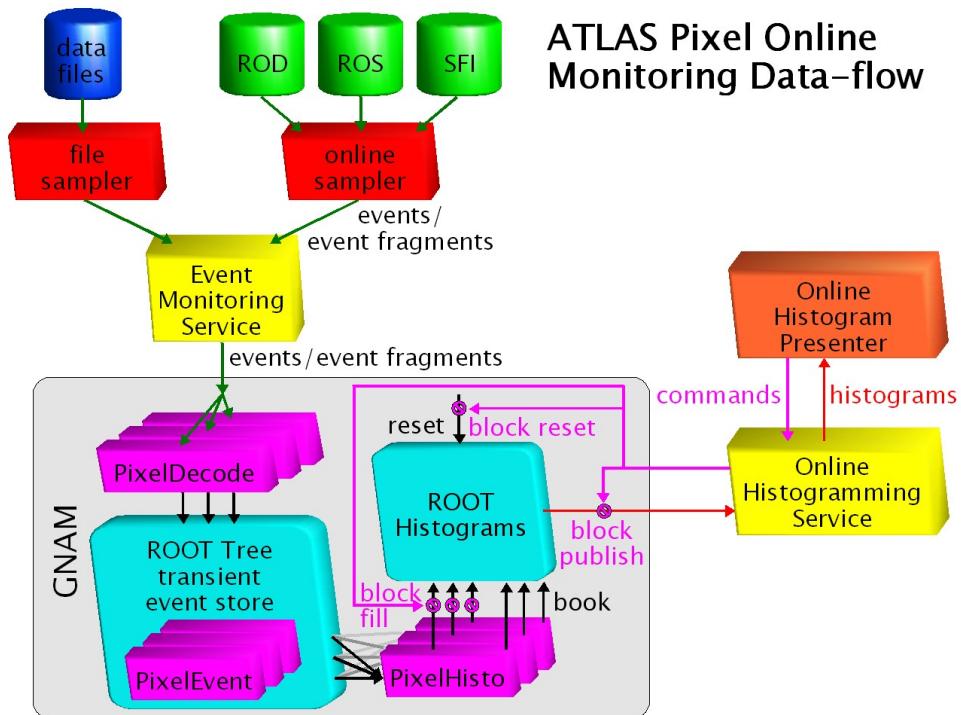


Figure 7-2 Data-flow and command-flow of the Pixel online monitoring from the different readout chain data sources to the Online Histogram Presenter

7.2.2 Pixel Detector Online Monitoring

The Pixel Detector makes especially high demands on the performance of the online monitoring since with its more than 80 million pixels it has an order of magnitude more channels than the SCT and a several orders of magnitude higher channel amount than other ATLAS sub-detectors. On one hand the online monitoring should provide few simple overview histograms which summarize the overall detector data quality and detector performance for data taking shifters. For these histograms the full pixel granularity is not required nor practicable. Providing the histograms in module granularity is sufficient to identify the source of the problem and to allow reasonable event sampling and histogram publishing frequencies for prompt debugging. On the

other hand full pixel granularity histograms are necessary for expert debugging and specific detector performance studies. Since typically these histograms are only necessary occasionally and only for a subset of the detector or the readout chain their filling and publishing should be individually switchable to avoid unnecessary increase of the sampling and publishing rate.

A first implementation of the Pixel online monitoring was made in the scope of this work for the ATLAS Combined Testbeam (CTB) in summer 2004. A segment of the ATLAS experiment with all sub-detectors was placed in the H8 beamline at CERN to allow performance studies of the single sub-detectors and to study the interplay of the different readout chains and the common triggering. For the Pixel Detector six modules were arranged similar to the final experiment alignment. Details about the used Pixel modules and the CTB are presented in [REI06]. The Pixel online monitoring was integrated into the GNAM framework by three dynamic libraries as shown in Figure 7-2. The PixelDecode library receives ROD fragments from the GNAM core, decodes the ROD header, trailer and modules fragments and fills the decoded hits, identifier and error flags into the ROOT Tree database defined in the PixelEvent library. For the CTB runs the mapping for ROD source identifiers and the module link identifiers was automatically created from the received bytestream data and corresponding histograms booked by the PixelHisto library. The ROOT Tree transiently stored information is accessed by the PixelHisto library and filled into ROOT histograms which are published by the GNAM core to the OHS. For the six CTB modules full pixel granularity hitmaps were filled to allow the localisation of the beam spot on the modules. Hit multiplicity distribution histograms allowed to check the module tilt angle with respect to the beam and to identify modules with noisy pixels by an increase of entries with hit multiplicity = 1. Modules with noisy pixels were also identifiable by an increase of low TOT hits in the TOT distribution histograms. The module timing could be adjusted and tested with help of Level-1 accept distribution histograms which shows in which of the 16 Level-1 accept triggers for each beam trigger a hit was found. Row and column correlations between modules and between Pixel modules and SCT modules allowed to check for tilt angle differences between Pixel modules and between Pixel and SCT modules. Since for module events with a hit multiplicity > 1 all possible hit combinations were taken into account off correlation entries exist. They indicate the existence of multiple track events or noisy pixels, because in most of the multiplicity > 1 events the hits are neighbored and form a cluster so that wrong combinations do not have a significant difference to the right correlation combinations. In order to monitor all bytestream contained error flags they were combined to an error code representing all possible error flag combinations. The resulting error code histograms helped to identify readout and trigger problems. Some example online monitoring histograms as displayed by the OHP are shown in Figure 7-3.

For the System Test cosmic run in late 2006 the Pixel online monitoring was extended on the basis of the CTB online monitoring to cope with the 144 modules of the endcap A [GAR07]. In order to allow geometric naming convention labeling of histograms connectivity database queries were implemented into the mapping of ROD source identifiers and modules link identifiers. The configuration of the Pixel monitoring libraries were moved from a configuration file to the TDAQ OKS¹⁸² configuration database. In the cosmic runs for each module a full pixel granularity bitmap, a TOT

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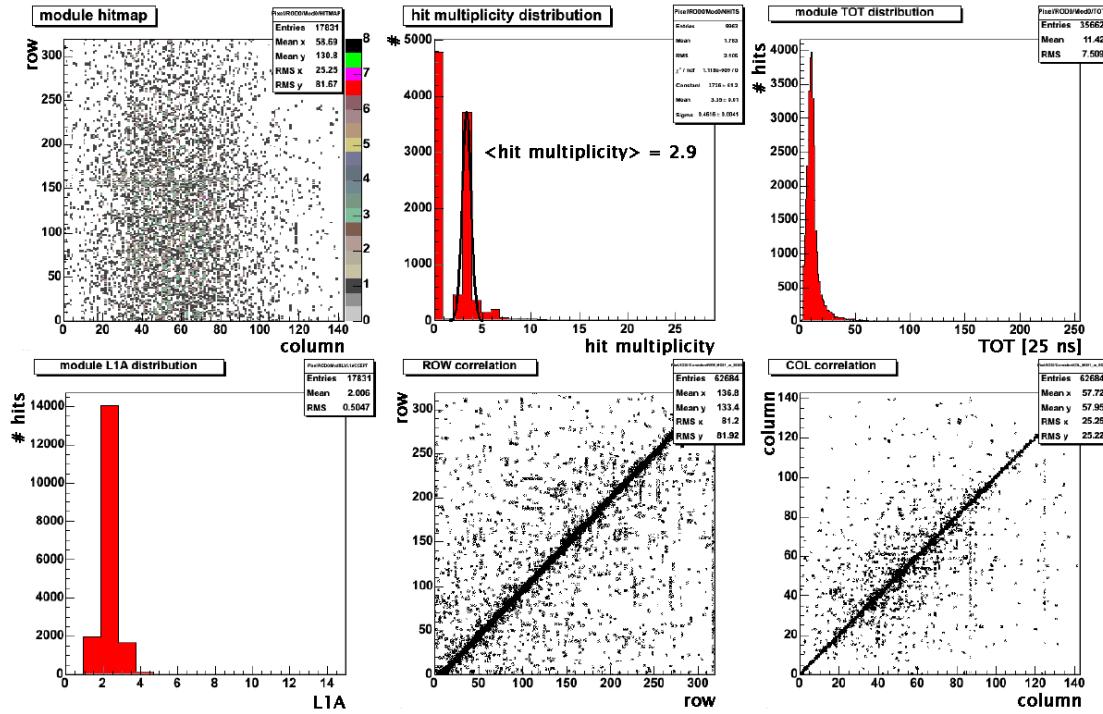


Figure 7-3 Pixel online monitoring histograms of one module from the ATLAS Combined Testbeam run 2004. The top left histogram shows the hitmap and the top middle histogram the event hit multiplicity of the module. The time over threshold distribution is shown in the top right histogram. In the bottom left histogram the module hit timing with respect to the 16 Level-1 accept triggers is shown and the bottom middle and right scatter plots show the correlation of the module hit row and column with the hit row and column of the module behind. Off correlation entries are mainly caused by event with cluster multiplicity > 1 and noisy pixels since all possible hit combinations are taken into account.

distribution histogram, a Level-1 accept timing distribution histogram and a FE/MCC error flag distribution histogram were filled. For each ROD a summary hitmap, a summary TOT distribution, a summary Level-1 accept distribution, ROD error flags distribution, a number of errors and a number of hits histograms were created. For the entire endcap summary TOT and Level-1 accept distributions, a summary ROD error flag as well as number of hits and events histograms were filled. A screenshot of the OHP showing the endcap Level-1 accept timing distribution of the first System Test cosmic run is presented in Figure 7-4. It gave the first evidence that cosmic muon hits were seen in the endcap modules with a fixed effective delay of 125 ns with respect to the first of the 16 Level-1 accept triggers. Off-peak entries were caused by unmasked noisy pixels since they have hits which are not time correlated with the scintillator triggers and thus also not time correlated with the first of the Level-1 accept triggers.

For the first Pixel cosmic data taking in the ATLAS experiment a flexible online monitoring is implemented in the scope of a diploma thesis [HIR07]. The monitoring as implemented for the System Test is not scalable to the full detector since the high amount of histogram bins and the high number of filled and published histograms would decrease the sampling and publishing frequencies to not practicable rates. Therefore it is aimed to fill by default only a small amount of summary histograms with module granularity that give an overview of the detector performance and

readout chain problems for the entire detector. Before histogram publishing these histograms are analyzed and discrepancies to expected values are displayed in a single detector status histogram. The summary histograms should represent both the detector geometry arrangement of modules and the readout chain structure. To identify the source of discrepancies some O(100) ROD histograms with FE granularity should be filled and published by default together with the summary histograms. They should allow to pinpoint the source and type of problems down to the level of FEs. The filling and publishing of additional module histograms down to full pixel granularity of the mentioned parameters should be dynamically switchable by OHP commands for single modules as well as for geographic and readout chain module groups like modules belonging to an optoboard, ROD, stave, layer, disk. This would allow to change the monitoring detail during runtime according to the actual debugging needs without affecting the sampling and publish frequencies for the standard shifter case.

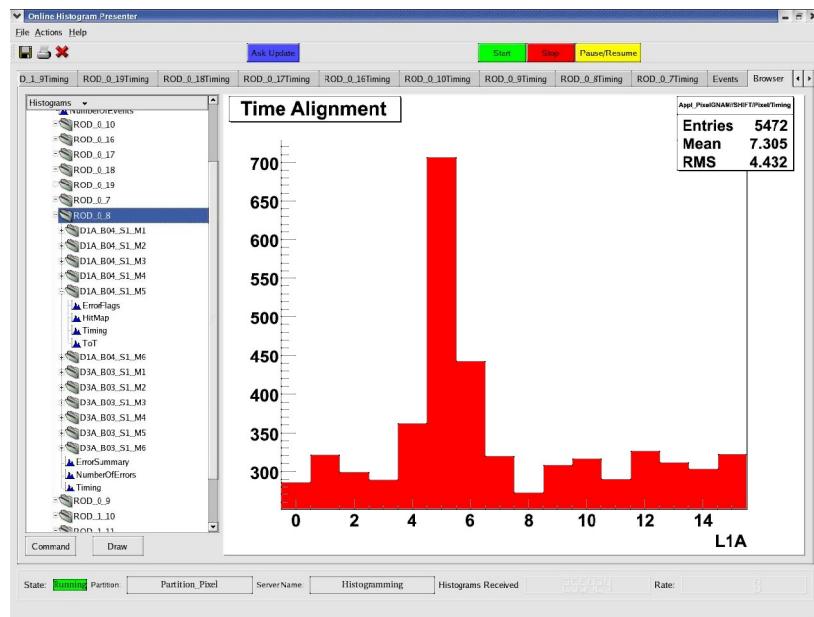


Figure 7-4 Screenshot of the online monitoring histogram presenter showing the Level-1 accept distribution for the first Pixel System Test cosmic run. For each scintillator trigger 16 Level-1 accept triggers were send to the Pixel modules. The hit number peak at the Level-1 accept value of five gave the first evidence that cosmic muon hits were seen with the endcap modules and an effective delay of about 125 ns between the first Level-1 accept trigger and a muon crossing the detector existed. Off-peak hits were caused by noisy pixels which have hits not time correlated to the scintillator trigger.

7.3 ByteStream Converter

7.3.1 Athena Framework

Athena [ATL06] is the concrete ATLAS offline software control framework and is based on the underlying GAUDI architecture originally developed by LHCb. The architecture consist of the specification of components and their interactions with each

other. Components are blocks of software with well defined interfaces and functionalities. They can be flexibly combined in different ways. The main components of the Athena architecture are shown in Figure 7-5.

Three different base classes are defined in Athena: data objects with clear quantity-like entities, algorithms with procedures to create or transform data-like objects and converters between transient and persistent data stores. Algorithms are initialized at the beginning and finalized at the end of a job. Their procedure part is executed once for each event. Services are special algorithms that may be used by many other algorithms as often as required. Only a single instance of a service is needed and it is initialized and finalized the same way as a general algorithm. A second type of special algorithms are tools. These are encapsulated pieces of code executed only for special events, executed many times per event or executed with different configuration by the same or different parent algorithms.

Basic concepts visible in Figure 7-5 are the organization of the job procedure by the application manager service, the configuration of the algorithms by the job options service, the clear distinction between data objects and algorithm objects and the exact differentiation between transient and persistent data.

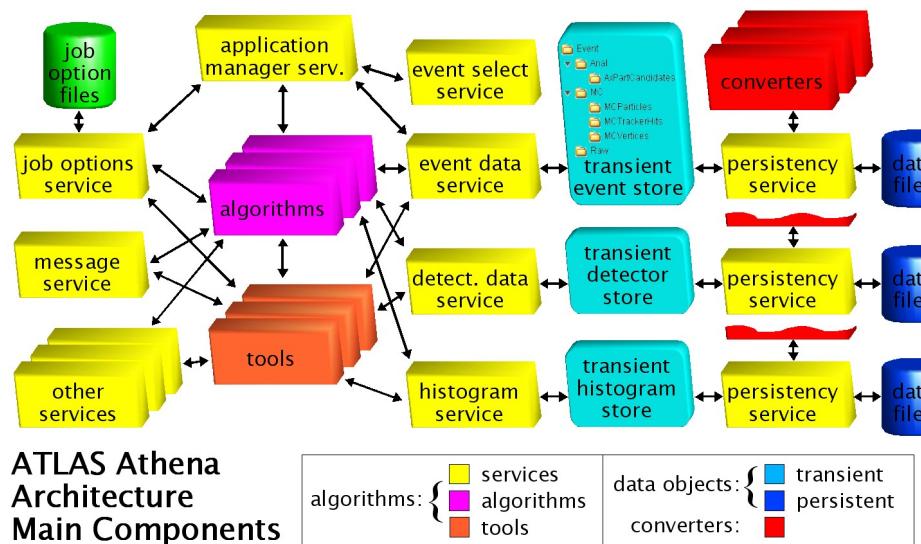


Figure 7-5 Structural view of the ATLAS Athena offline software framework

The application manager starts the job options service, which interprets a job options file at initialization and registers all desired components in the application manager. All components are managed and started by this application manager. The second aim of the job options service is to configure all components at run time (without the need to recompile or relink) with options and properties given in the job options file. Advantages of the 'distinction between data objects and algorithm objects' concept are a minimal coupling between data and algorithms. This means that algorithms do not need any special knowledge about the data producing algorithm (no "interface explosion" problem) and the system is more robust against instabilities of algorithms. The main advantage of the 'differentiation between transient and persistent data' concept is the possibility of a simple exchange or optimization of the storage technologies without changing the algorithms and data objects, because converters are

used as interfaces which know the data formats.

StoreGate (SG) is the Athena implementation of a transient data store (TDS). It belongs to the passive blackboard family: algorithms post data objects to a common in-memory database and other algorithms can access them and produce new data, but without the possibility to directly react to TDS events. SG manages the creation, access and lifetime of a data object as well as the conversion from and to its persistent format. The basic approach to identify data objects is the tree structure. This is possible since uniform data objects are grouped into collections. As result the TDS will mostly contain only a single instance of a data object type. To cover cases with equivalent data recorded by several algorithms, for example several equivalent instances of a track collection produced by alternative tracking algorithms, the identifier of the algorithm instance is added as a second component to the TDS object identifier. Furthermore SG supports uni-directional inter-object relationships and links (persistable pointers).

Other framework services relevant to the bytestream converter are the message service and the tool service. The message service provides the facilities to log information, warnings and errors if the activation level is equal or above a given output level. This output level can be set via the job options service either globally or locally for an individual component to the levels: VERBOSE, DEBUG, INFO, WARNING, ERROR, FATAL or ALWAYS. The responsibility of the tool service is to create tools, configure them, make them available for services and algorithms and terminate them. A tool is created and configured the first time it is requested by a service or algorithm. For following requests the tool service passes the existing instance to the requesting service or algorithm.

7.3.2 Pixel Bytestream Converter

The Pixel bytestream converter is a collection of Athena packages that serve the purpose to decode the uncalibrated detector raw data from ROD fragments in bytestream format and store the hit information in transient RDO¹⁸³s, which is the data format used in the offline software for formation of space points by TOT calibration and hit clustering. A RDO is a data class defined in the InDetRawData package designed to store the hit information of the ROD fragments. It contains for each hit a non-ambiguous 32-bit pixel identifier (PixelID) as well as packed into another 32-bit word the 8-bit hit TOT value, the 8-bit module BCID, 4-bits for module skipped LVL1IDs, the 4-bit module LVL1ID, and the 4-bit Level-1 accept trigger counter. The result is a Pixel RDO per fired pixel cell stored in module corresponding PixelRDO_Collections in StoreGate.

The InDetRawDataByteStreamCnv is the central package of the Pixel bytestream converter and contains the bytestream encoder and decoder. It is implemented as an AlgTool¹⁸⁴ and is automatically called when an algorithm asks for the data of a particular detector element. If used in decoder mode it receives ROD fragments, which were requested by an analysis algorithm, decodes the ROD header and searches for error flags in the ROD header. Errors are reported up to an adjustable amount via

¹⁸³ Raw Data Object

¹⁸⁴ Algorithm Tool – Athena tool base class

the Athena message service as WARNINGS or ERRORS and the occurrence of different error types are counted. The extended 32-bit LVL1ID, which consists of the 24-bit TTCrx LVL1ID and the 8-bit ROD ECRID, is extracted from the ROD header and stored in a StoreGate TimeCollection. The decoder retrieves the ROD source identifier from the ROD header. From each found module header it decodes the module formatter and link and combines them with the ROD source identifier to an Online Identifier. From the Online Identifier the corresponding Offline Identifier is retrieved from the InDetCabling service.

During initialization the InDetCabling service package fills from a text configurations file several maps that allow to associate the module OnlineID to the module OfflineID as well as to obtain lists of OfflineIDs connected to a ROB or to translate between ROB and ROD Identifiers. For the upcoming Pixel commissioning phase it is planned to get these maps from the Pixel connectivity database. A module OnlineID consist of the formatter and link position of the module on the ROD as well as the source identifier of the ROD. The OnlineID indicates the DAQ readout position of a module and the source identifier RODID the sub-detector, layer/disk, readout crate and crate slot position of a ROD. The module OfflineID describes the geographical position of a module in the detector and consists of barrel/endcap identifier bits, the layer/disk number and the module phi and eta indexes describing the position of the module on a layer/disk. These values are packed by the InDetIdentifier package into the unambiguous OfflineID. The meaning of different bytes and bits in the OnlineID and OfflineID are shown in Appendix A Figure A-42.

Module hit words are decoded and from the FE index, the pixel FE row and column a pixel phi and eta index are calculated as shown in Appendix A Figure A-42. For barrel modules and disk modules with odd module phi index the same assignment from FE, row and column to pixel phi and eta index exists. For disk modules with even module phi index the pixel phi index is swapped due to the different orientation of modules on the two sides of a disk. With the module OfflineID, the pixel phi and eta index a detector-wide unique PixelID is retrieved from the InDetIdentifier service. The meaning of the single bits in the PixelID are shown in Figure A-42. A new Pixel RDO is created and the PixelID, TOT, BCID, skipped LVL1IDs, LVL1ID and Level-1 accept are filled. For data taking runs with more than one Level-1 accept a module header and trailer exists for each Level-1 accept with increasing BCIDs. The first BCID of each module in an event is remembered and subtracted from consecutive BCIDs from the same module to obtain the Level-1 accept. The filled RDO is added to the PixelRDO_Collection of the corresponding module.

Module raw data and timeout words as well as error flags in the module headers, trailers and error flag words are analyzed, counted and their occurrence reported via the message service. At the finalization of the bytestream converter tool a summary with the amount of events, hits, and the mentioned DAQ readout errors is reported via the message service. The transfer of DAQ readout errors to the Pixel offline monitoring package was implemented in the scope of a diploma thesis [HIR07].

The verification, extension and maintenance of the Pixel bytestream converter was part of this work. It could be successfully used for the encoding of simulated ATLAS combined testbeam and System Test cosmic data into bytestream format for functional test reasons. It succeeded to convert data taken in the ATLAS combined testbeam and the Pixel System Test cosmic run for offline data track reconstruction and analysis.

*»Do you know like we were saying? About the Earth revolving?
It's like when you're a kid. The first time they tell you that the Earth's turning
and you just can't believe it because everything looks like it's standing still.
I can feel it: the turn of the Earth. The ground beneath our feet is spinning at
a thousand miles an hour. And the entire planet is hurtling around the sun at
67,000 thousand miles an hour and I can feel it. We're falling through space,
you and me. Clinging to the skin of this tiny little world and if we let go...
that's who I am. Now forget me, Rose Tyler. Go home.«*

Doctor Who

Chapter 8

Conclusion and Outlook

The Pixel Detector of the ATLAS experiment is with its over 80 million $50 \times 400 \mu\text{m}^2$ pixel channels for the foreseeable future the biggest pixel particle detector system ever build. In spite of its small active volume of $\sim 1.3 \text{ m} \times 0.35 \text{ m}^2$ it contains more than 80% of the total ATLAS readout channels. It will provide three $\sim 12 \times 100 \mu\text{m}^2$ resolution tracking space points over a pseudo rapidity range of $|\eta| < 2.5$ for all tracks generated within $|z| < 11.2 \text{ cm}$ of the nominal interaction point. High quality assurance requirements arise from its complex mechanical structure and its poor accessibility in the center of the ATLAS experiment. The close proximity of the Pixel Detector to the LHC proton-proton interaction point causes additional challenging requirements. In order to minimize multiple scattering and provide a detector with an interaction length of $X_0 < 10\%$, lightweight materials for the active detectors, their services and the mechanical structure needed to be used. The detector components are required to withstand a radiation lifetime dose of $1 \cdot 10^{15} \text{ n}_{\text{MeV eq}}/\text{cm}^2$ to fulfill this tasks and to achieve excellent b-tagging and high 3D-vertex resolution.

The detector, data acquisition readout and service components were in-depth tested during their production. Especially for the Pixel Package components quality assurance measurements were performed after each assembly step to ensure that no affected components are integrated. In the scope of this work quality assurance measurements for the cabling and assembly of the Pixel barrel at CERN were developed, performed and analyzed. It could be shown that no significant damage of detector components nor worsening of the detector performance were caused by the assembly. During the assembly occurred critical problems could be identified in time and necessary actions were taken to avoid integration of affected components. Fragile aluminum Type0 cables were sorted out by enhanced quality assurance procedures and were replaced by new produced cables. Connectivity test of sense lines were added to barrel assembly quality assurance measurements in order to avoid over-voltage risks for detector front-end electronics. The results verify an excellent Pixel Detector barrel performance with only 1.6% of not working pixels. An analysis of the not working pixel causes and distributions points out possibilities to further increase the performance for an upgrade of the ATLAS Pixel Detector or future silicon pixel detectors.

Despite the detailed production tests, the interplay between all components of the complex Pixel Detector system could be only tested and verified in a large scale System Test. A first small scale laboratory setup (4% of the final system) was used at CERN to investigate the key tuning parameters of the optical data transmission system. The parameter space of the optical link was systematically studied and the parameter influences on the data transmission light signal shape as well as on the data transmission error rate were characterized with different measurement methods. Strategies for the optimal tuning were developed and compared. Results of the first optical readout of the detector in double data bandwidth mode were analyzed and compared to the single bandwidth results.

A close to the final layout laboratory setup, corresponding to about 7% of the complete detector, with services, detector control system, interlock system, data acquisition readout chain, online software and evaporative cooling system was assembled and operated for several months. The mapping of the complex service system was verified. Faulty service components or electrical connections could be identified and fixed without risk or time loss for the production detector components. Problematic behaviors of the low voltage regulator prototypes and their steering could be identified early enough to be fixed before the operation of production detector components. Operation procedures for the cooling system and the services were developed and qualified. An observed change of the module bunch crossing clock frequency during the readout of specific modules was identified to be caused by an electrical crosstalk between the clock line and the specific module data line on the off-detector readout controller cards. Because another clock line is used in the final layout a risk for the stability of the readout by a not understood problem could be excluded. Key characteristics of the readout system and the optical link system were measured. The optical link tuning procedures were studied and improved using module readout up to the highest possible bandwidth of 160 Mbit/s. An alternative and faster optical link parameter scan was successfully tested and was integrated in the tuning procedure. The tuning of the module front-end discriminator thresholds was tested and compared to production tunings. An exact tuning to the target threshold of $4000 e^-$, low threshold dispersions of $30 e^-$ and low noise values of $155 e^-$ verified the excellent performance of the tuning algorithm and excluded additional noise sources in the service system. The functionality of the detector control system software and the online data acquisition software were constantly improved and extended according to System Test experiences.

The System Test setup was extended to operate the integrated endcap A of the Pixel Detector as close to the final experiment layout as possible. This includes the use of a prototype service quarter panel with realistic grounding scheme, optoboard arrangement and bi-phase cooling as well as routing of the data lines and power supply lines. The 144 modules of the endcap correspond to about 8% of the entire detector. The scalability and correct interplay of the service and readout system was proved. Operation procedures were developed, qualified and integrated into the detector control software and the online data acquisition software. Experiences with the bi-phase evaporative cooling system were gained and procedures for its operation were defined. It was found that a fraction of optoboards show low light output power and high light power spreads between their channels at operation temperature below $10^\circ C$. The low temperature behavior of optoboards was systematically studied with different measurement methods. The identification of this critical problem in time

allowed to increase the nominal operation temperature and to extend the optoboard quality assurance measurements in order to avoid the installation of optoboards with power spread problems into the experiment. As additional precaution resistive heaters and thermal isolation covers were installed to the optoboards and qualified to ensure that the optoboard operation temperature can be reached. A comparison between two optical link parameter scans was performed and observed differences were identified to be caused by a slow turn-on behavior of the optoboard laser diodes. Additional quality assurance measurements were used to avoid the integration of optoboards with significant slow turn-on behavior in the Pixel Detector. According to the observed problems a optical link parameter tuning procedure to determine the most stable optical link working point was developed and qualified under realistic conditions with the System Test setup. With the 8% scale system the excellent front-end discriminator threshold tuning performance was verified with threshold dispersions of 34 e^- and noise values of 167 e^- .

The measurement of the silicon sensor depletion voltage and the associated integrated irradiation dose using module noise occupancy versus sensor bias voltage curves was studied and its usability for the Pixel Detector operation was demonstrated. Pixel noise occupancies as low as the measurement sensitivity of 10^{-11} could be shown for some modules with sensor bias voltages above the depletion voltage and masked noisy pixels. The fast determination of depletion voltages without necessity of beam collisions can be used before sensor bulk type inversion. It is suitable to monitor the integrated irradiation dose of the detector in the first period of operation. The identification of the sensor annealing to reverse annealing transition with this method can be used to steer the detector temperature profile during maintenance periods for optimal detector lifetime.

Scintillators above and below the endcap were used to test the trigger and data acquisition system as well as to take cosmic muon data for offline software reconstruction, tracking and alignment studies. The data quality was monitored with an extended version of the Pixel online monitoring software, which was implemented in the scope of this work for the ATLAS Combined Testbeam. Raw data of the Combined Testbeam and System Test cosmic data taking runs were decoded for offline analysis by the Pixel bytestream converter software. This software package was continuously extended and adapted according to the offline analysis software needs in the time-frame of this work.

The results of the System Test presented in this thesis verify that the integrated Pixel Detector, its ancillary services, the detector control software, the DAQ readout chain, the DAQ online software and the evaporative cooling system perform together within and above the intended requirements. The complete system allowed stable operation for several months and could be qualified for integration into the experiment.

Following the System Test the setup was used to test the connectivity of all electrical and optical connections as well as the tunability of the optical links of the Pixel Package during its final assembly. After this final quality assurance measurement the Pixel Detector was successfully integrated into the ATLAS experiment in June 2007. Results, experiences and procedures of the System Test detector operation will help to have an efficient final commissioning phase for the first LHC proton-proton data taking in 2008. The ATLAS Pixel Detector Collaboration is looking forward to this upcoming exciting period.

»Und wer von euch nicht lesen kann,
der schaut sich nur die Bilder an.«

Ernst-Adolf Knäpper

Appendix A

Additional Figures and Measurements

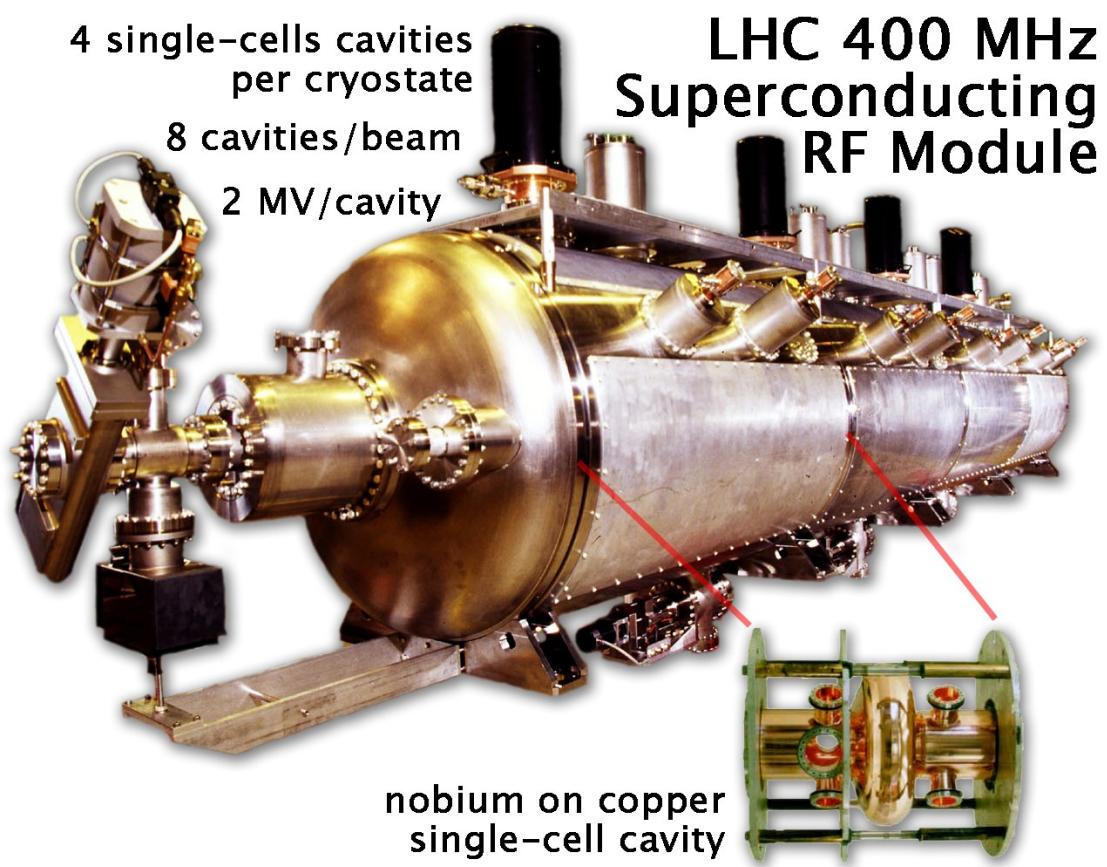


Figure A-1 LHC 400 MHz superconducting RF module with 4 nobium on copper single-cell 2 MV cavities

Simulated Electric Field Strength at Si-SiO₂ Interface of a pn Diode

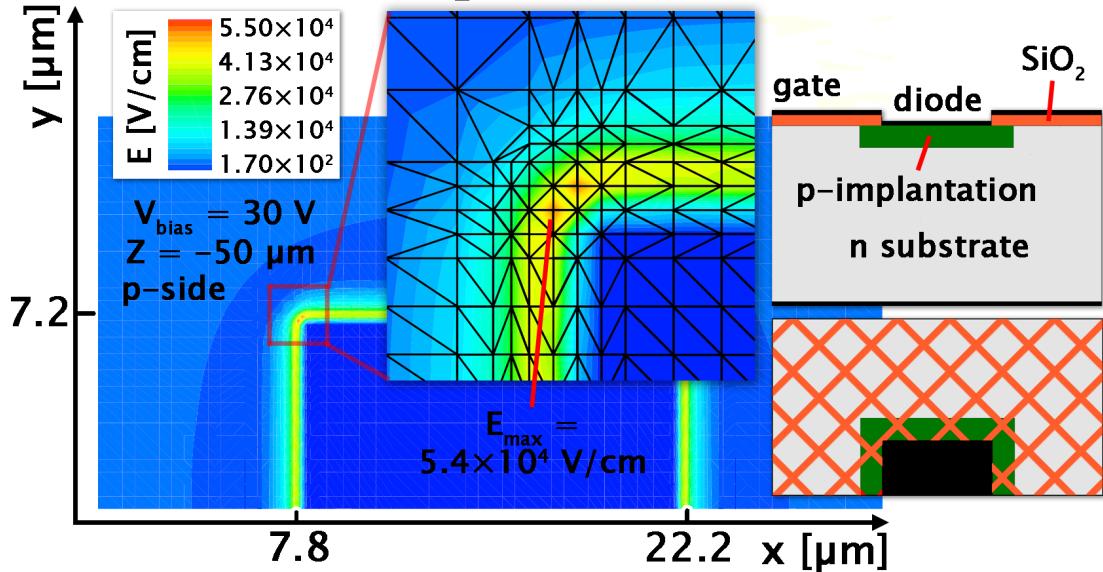


Figure A-2 Peak of electric field strength at the Si-SiO interface of a pn Diode [HÜG01]

ATLAS Pixel FE Channel Schematic

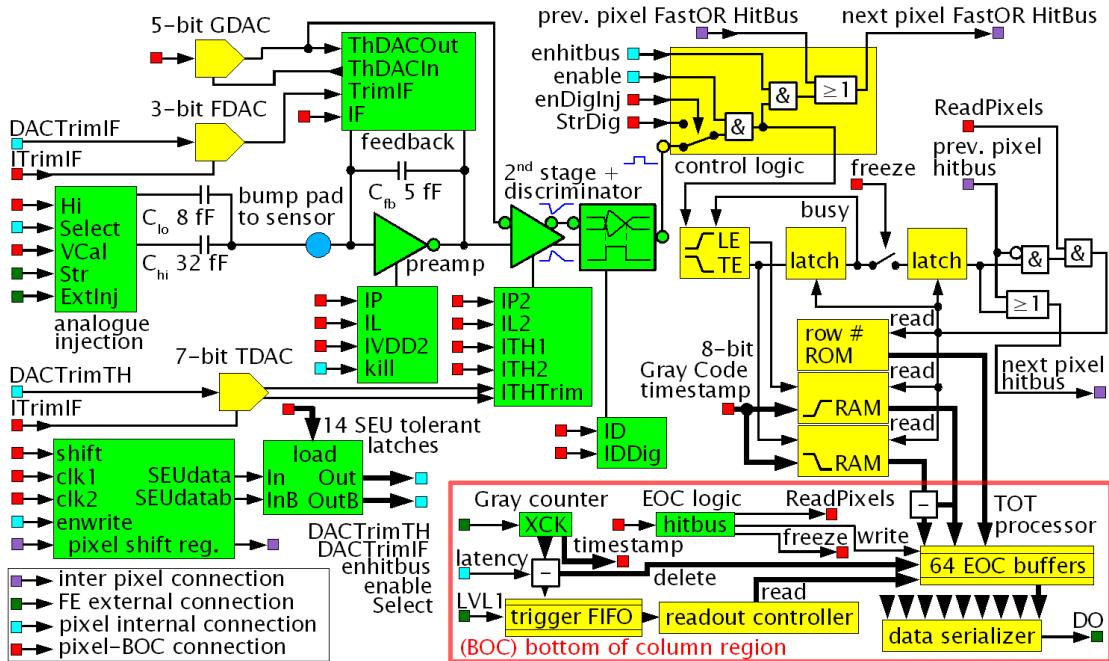


Figure A-3 Schematic of a FE pixel readout cell

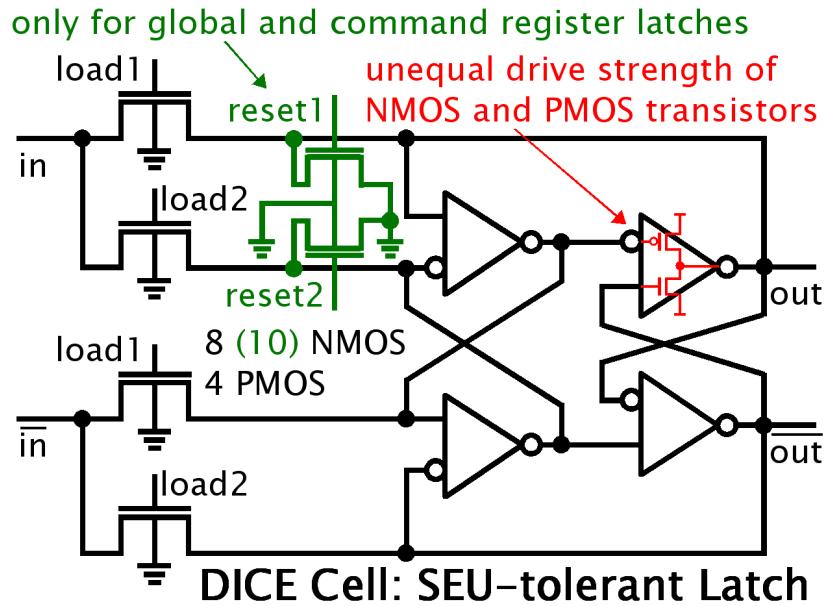


Figure A-4 Schematic of a DICE SEU-tolerant latch cell. Both reset signals are implemented for the Global and Command Register but not for the Pixel Register latches

DORIC Logic Circuitry

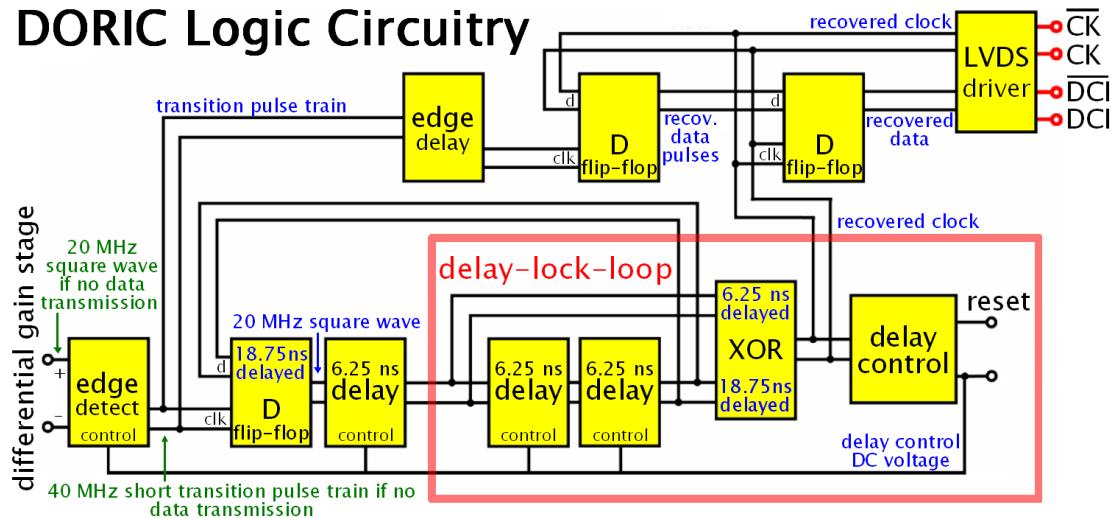


Figure A-5 Schematic of the DORIC logic circuitry with the delay-lock-loop to recover the CK clock and the DCI data stream from the BPM PiN signal

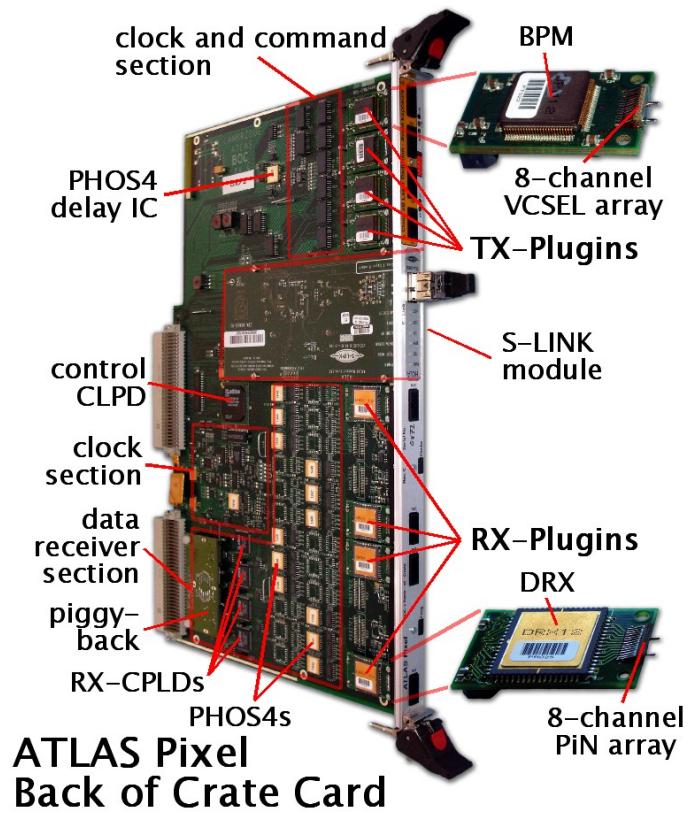


Figure A-6 The ATLAS Pixel Back of Crate Card (BOC)

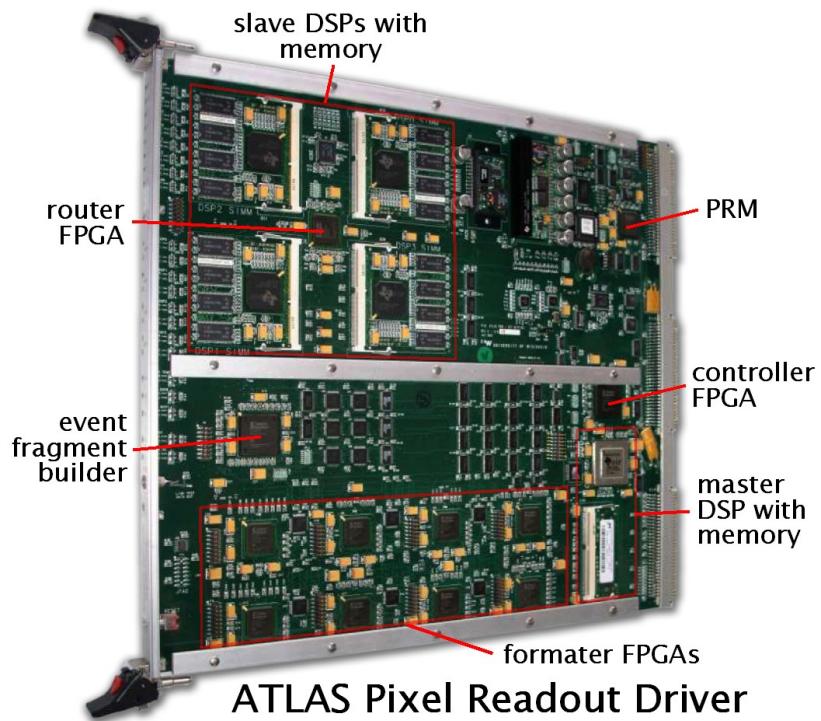


Figure A-7 The ATLAS Pixel Readout Driver (ROD)

ATLAS Pixel MCC to ROD Data Format

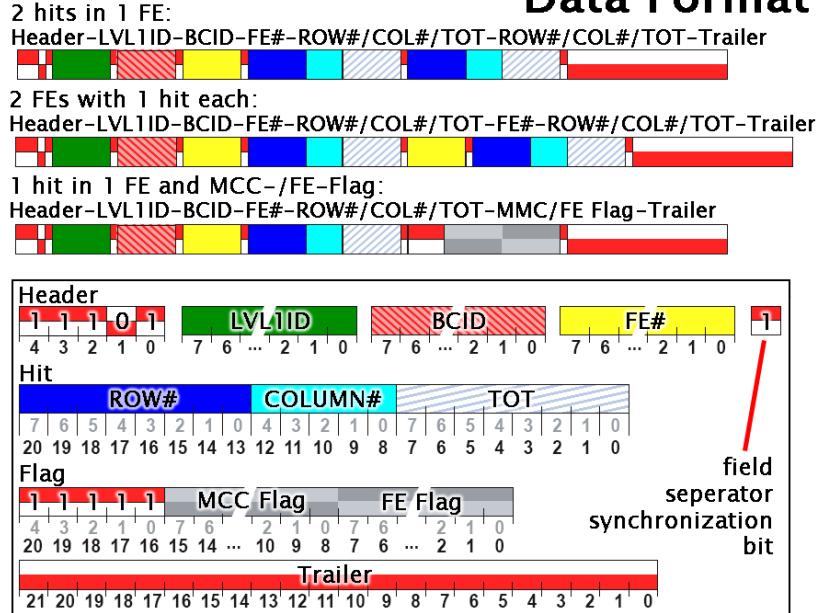


Figure A-8 Data format of the MCC to ROD data transmission [BEC04]

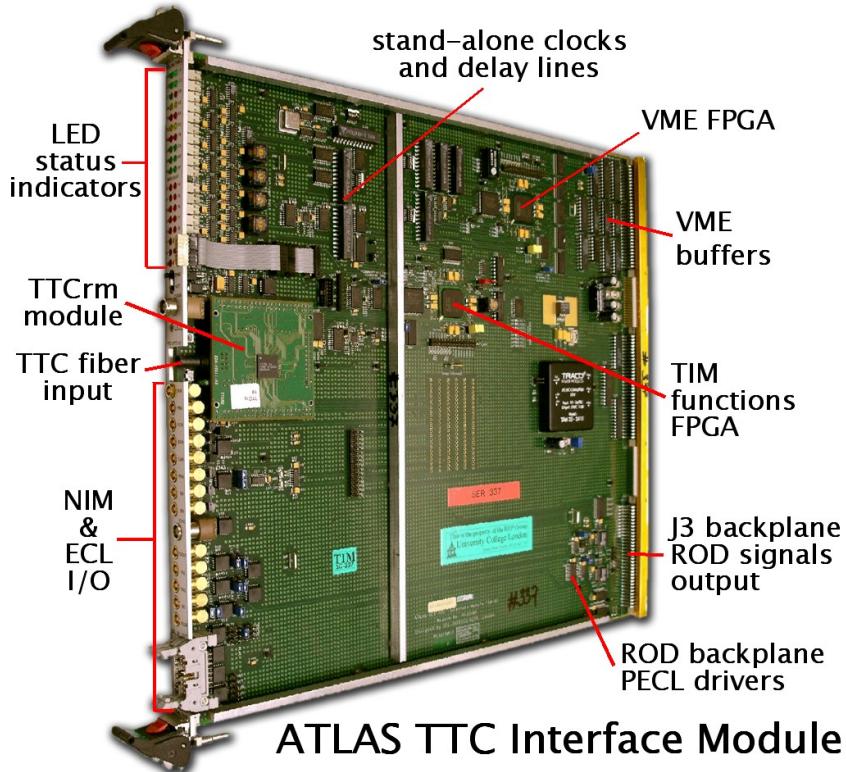


Figure A-9 The ATLAS TTC Interface Module (TIM)

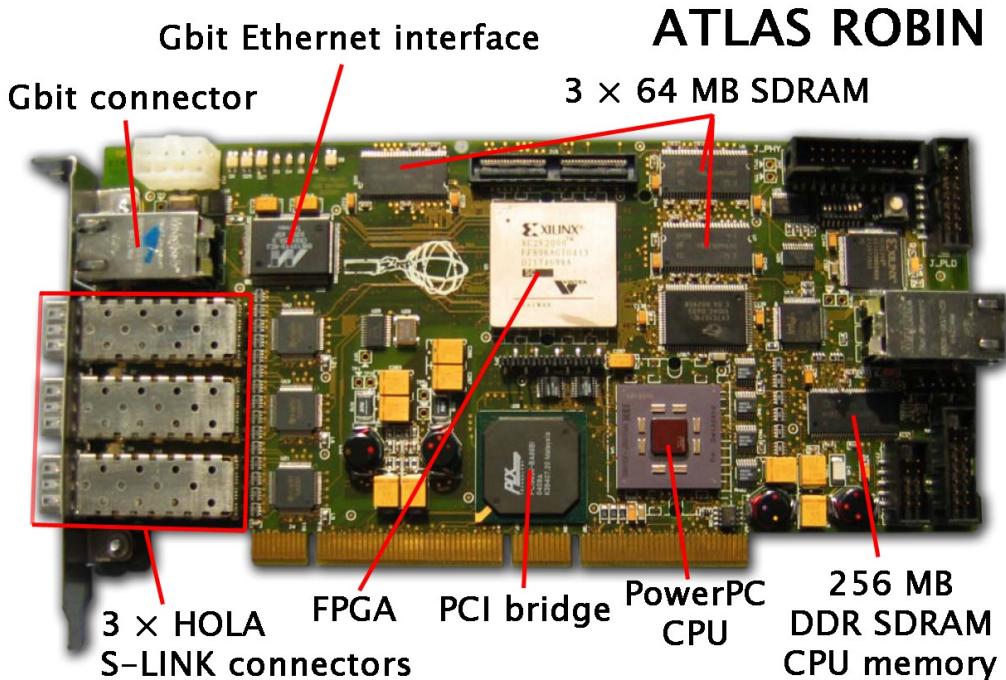


Figure A-10 ATLAS ROBIN PCI card

Voltage Regulator Remote Sensing with Current Compensation

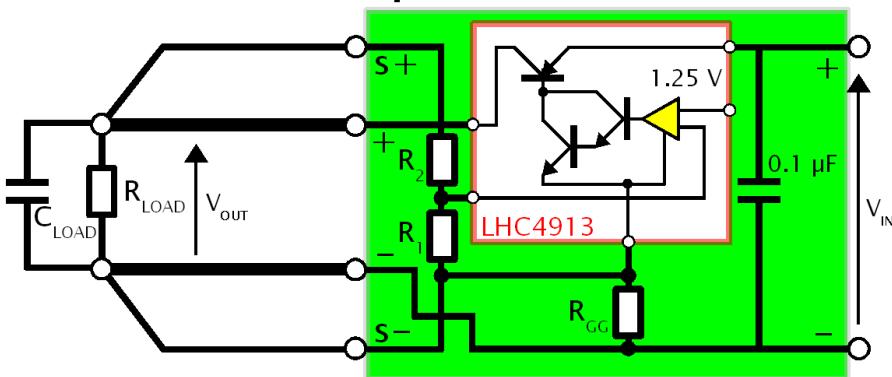


Figure A-11 Schematic of the remote sensing with current compensation circuitry with the LHC4913 voltage regulator

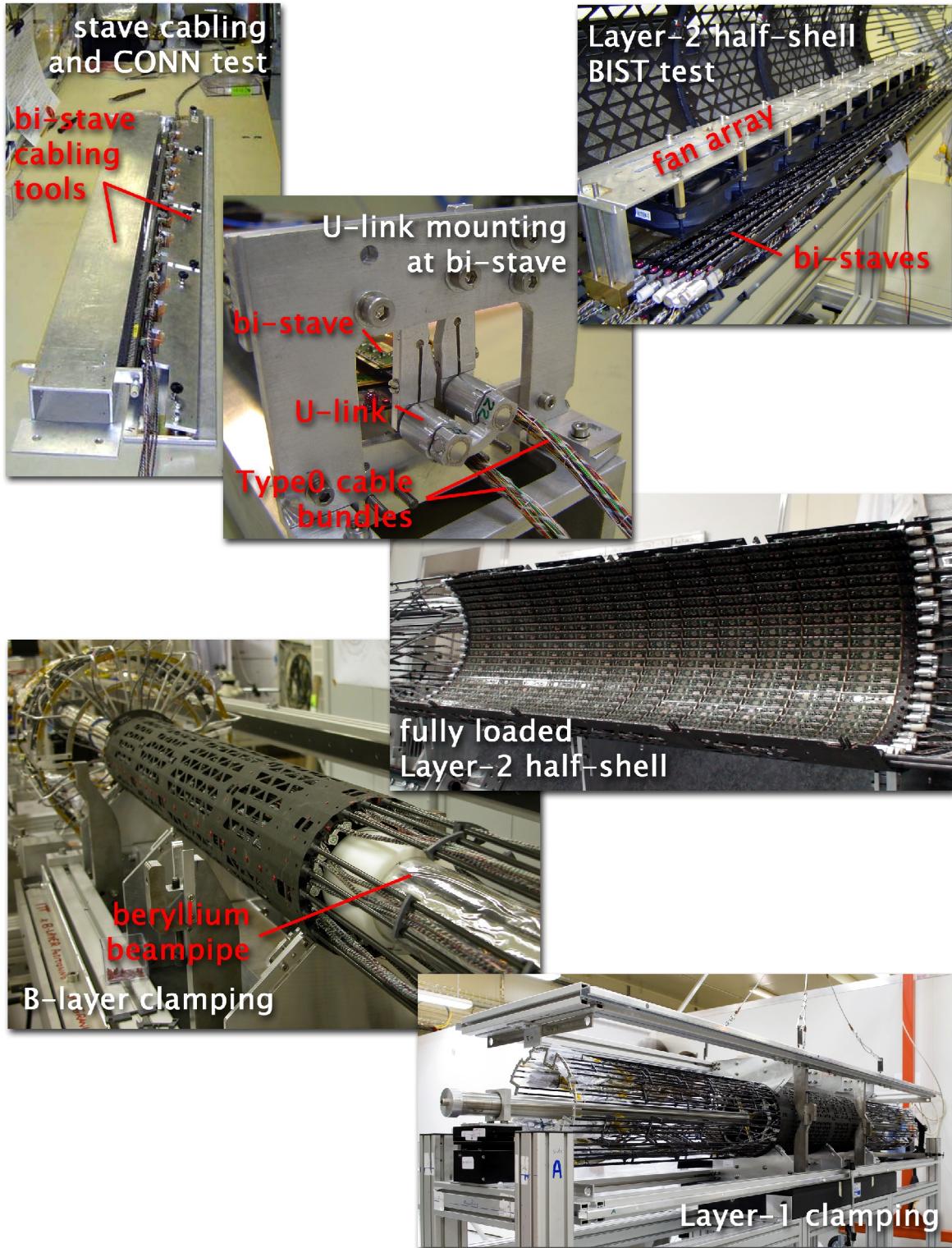


Figure A-12 Snapshots of the stave-cabling, bi-stave U-link mounting and Pixel Detector integration progress as well as at the test steps CONN and BIST

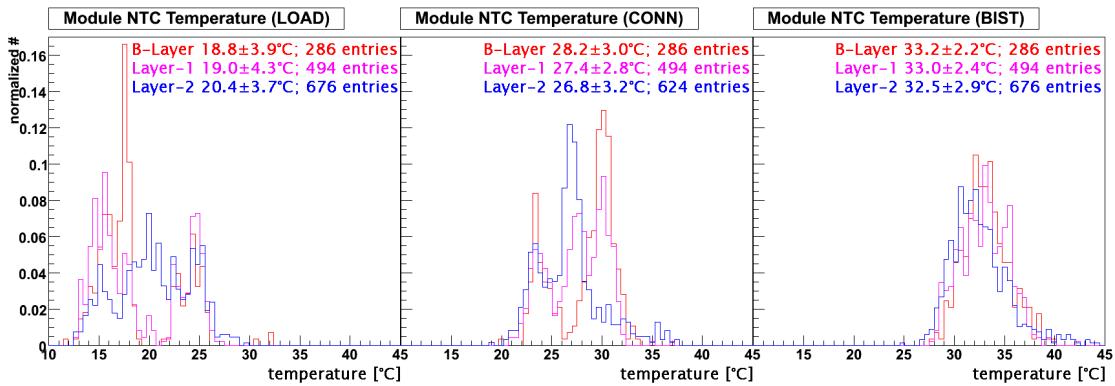


Figure A-13 Module temperature distributions of the Pixel layers for LOAD, CONN and BIST

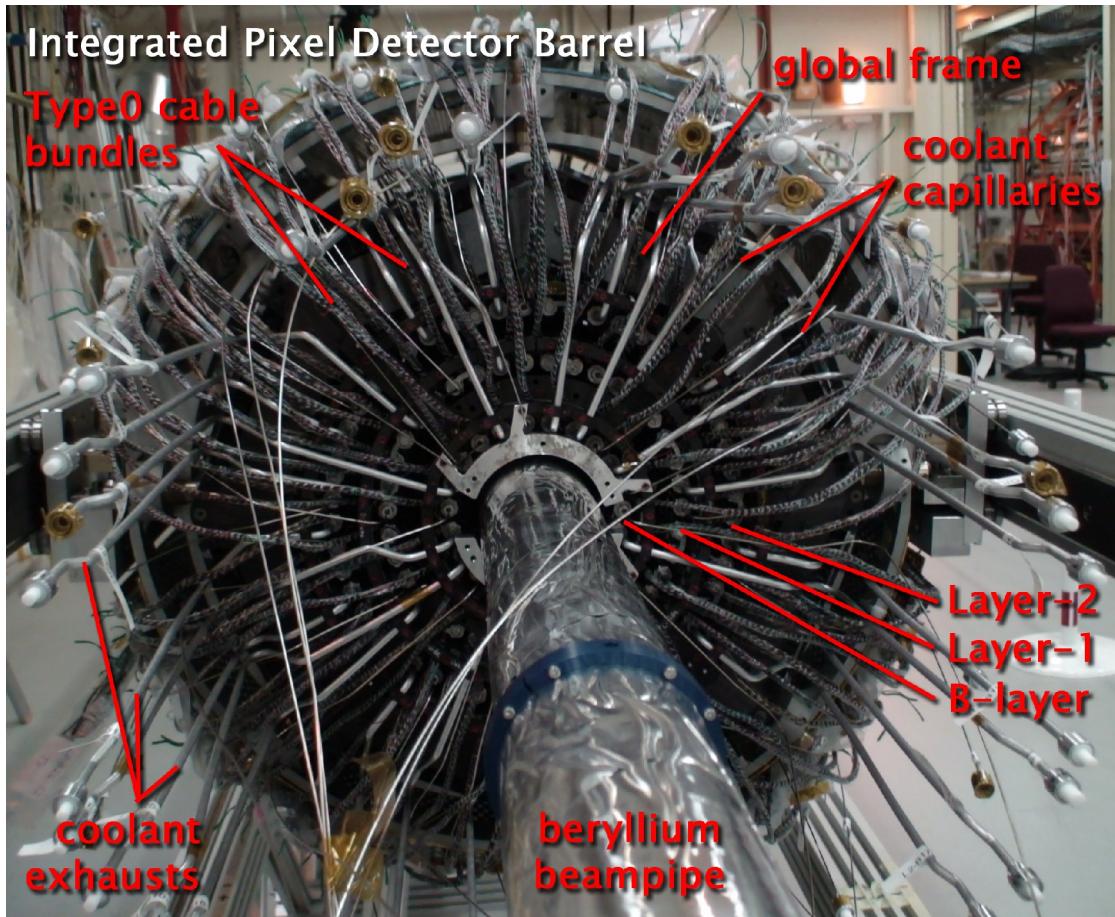


Figure A-14 Integrated barrel part of the Pixel Detector with Type0 cables mounted to temporary support for endcap installation

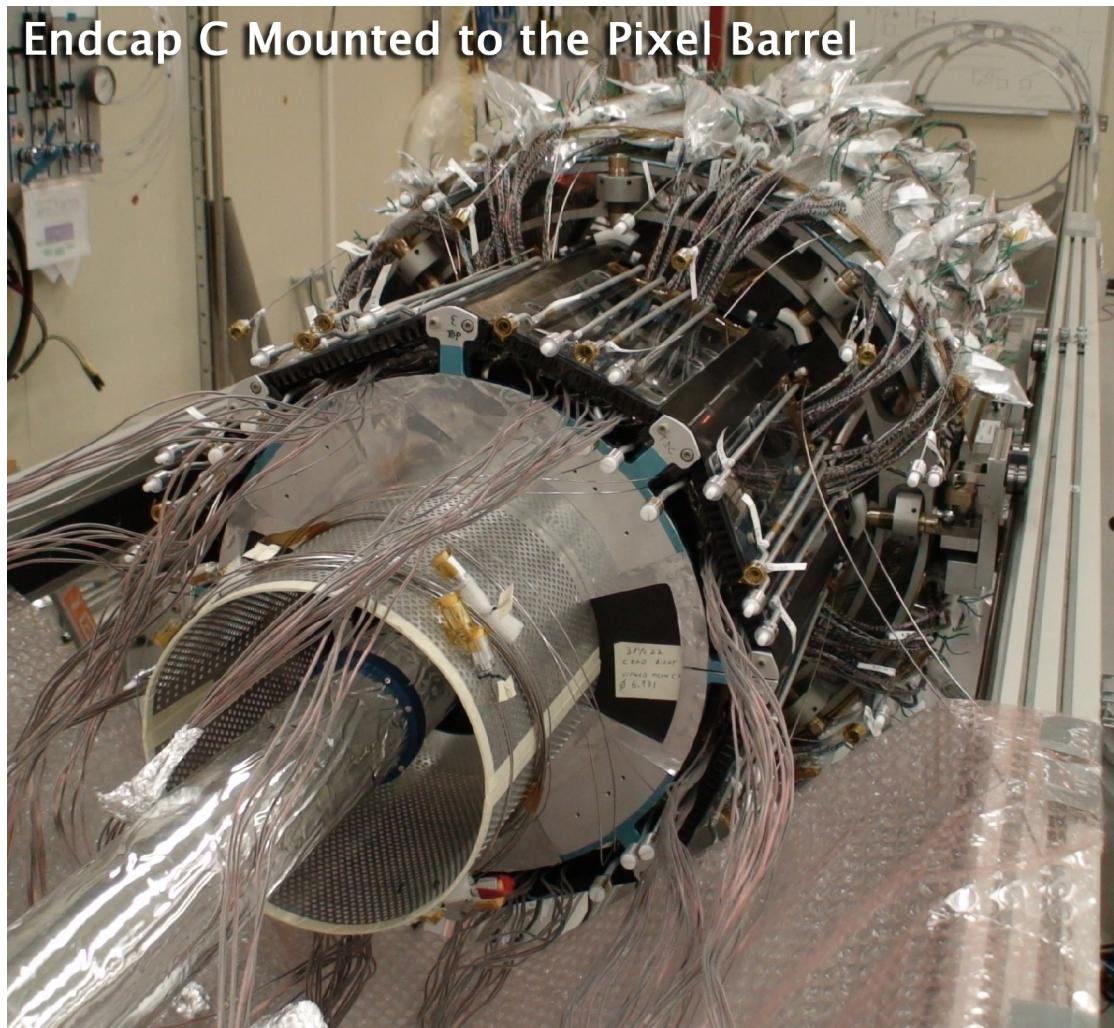


Figure A-15 Beryllium beampipe with Pixel Detector barrel and endcap C on the ITT

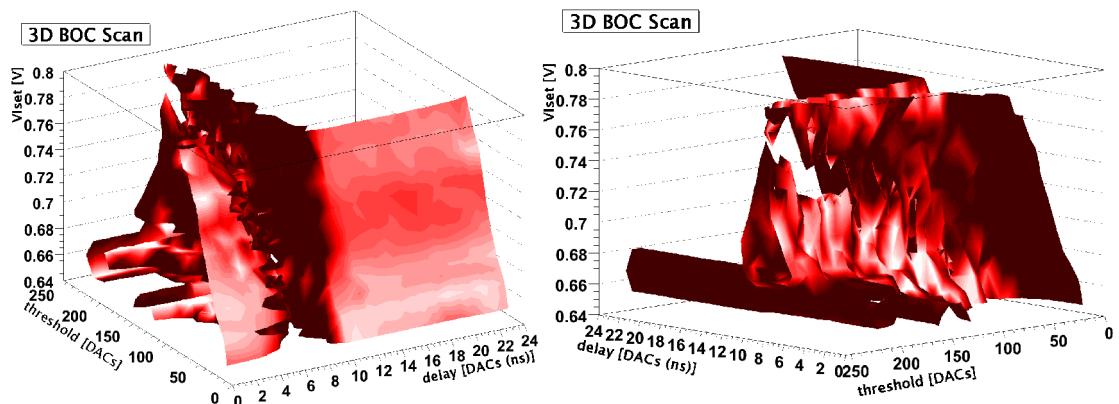


Figure A-16 3D contour plot of the error-free region in the $\{RX\text{ delay}, RX\text{ threshold}, V_{set}\}$ parameter space

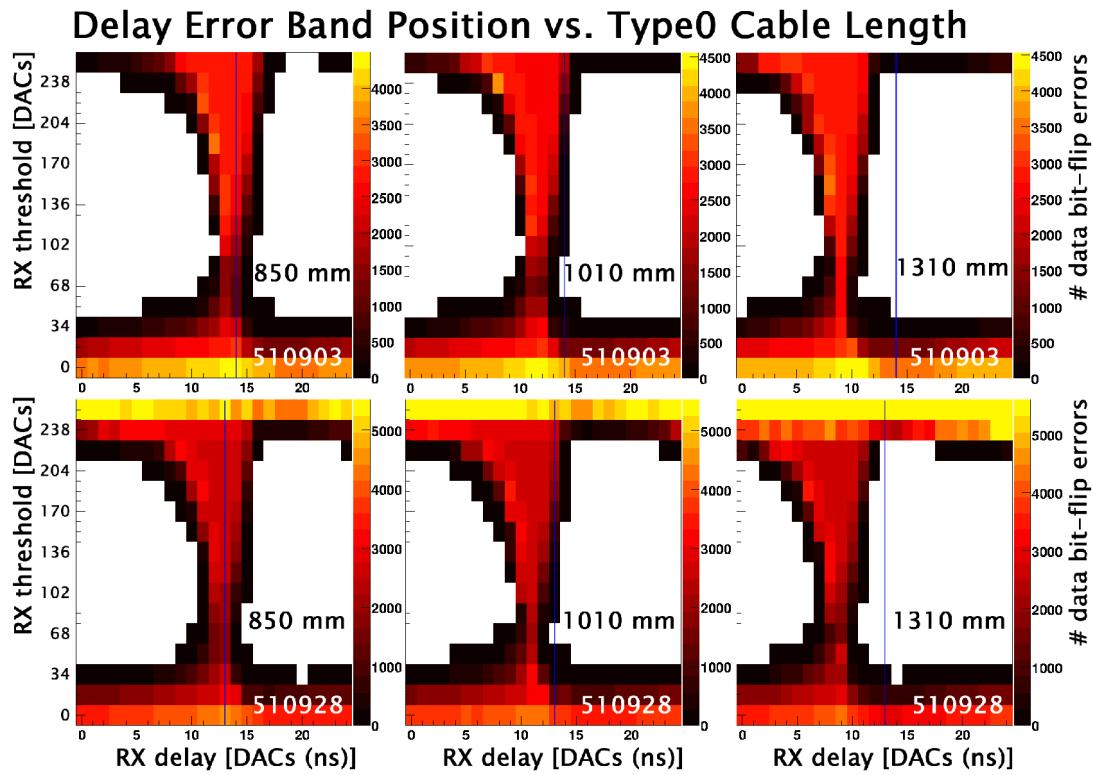


Figure A-17 BOC scans of two different modules with three different Type0 cable lengths

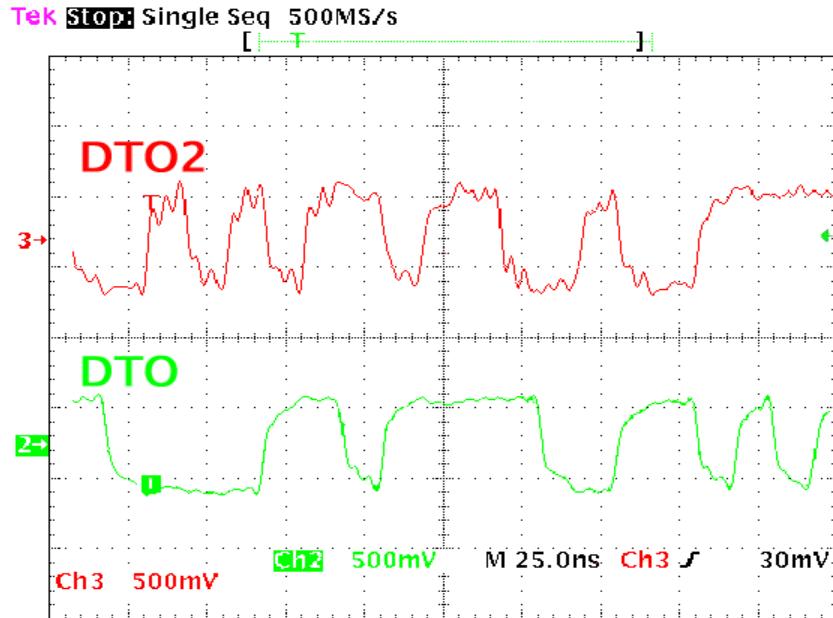


Figure A-18 DTO and DTO2 signal shape measurement of the first module readout in 160 Mbit/s mode with the bi-stave System Test setup

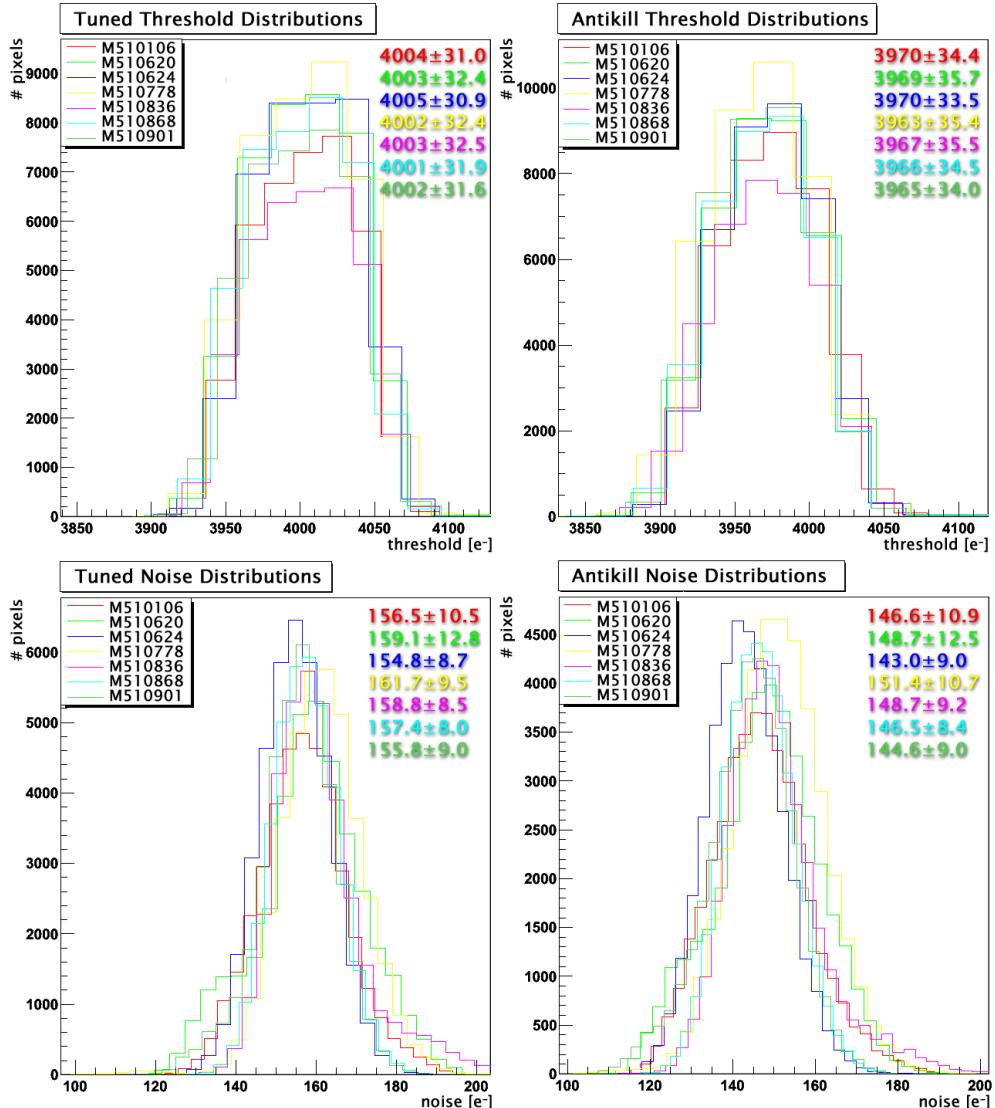


Figure A-19 Bi-stave modules threshold and noise distributions for threshold scans in normal (left) and antikill mode (right) with System Test setup tuning

BOC Scans at Different Temperatures

sector 9029 – optoboard 2008

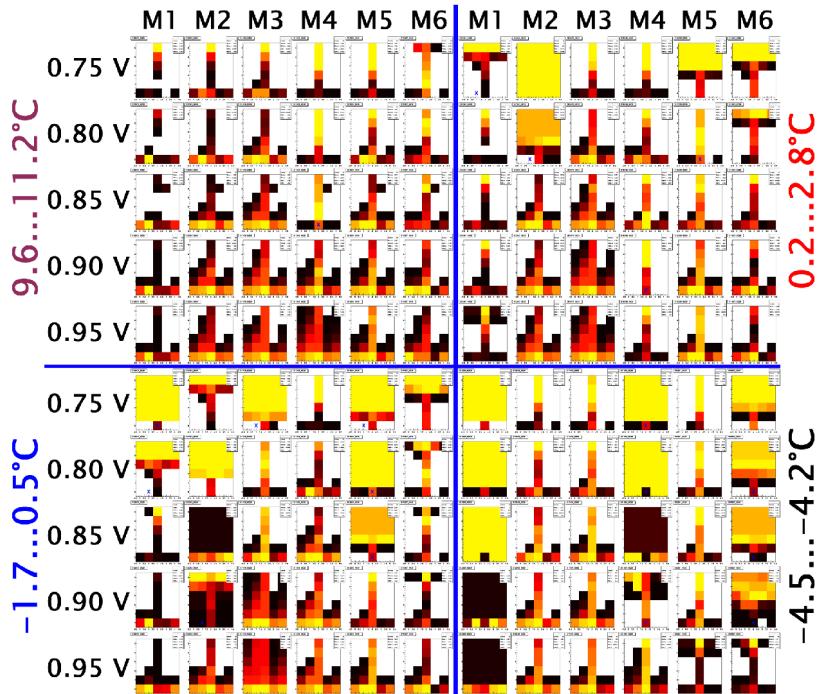


Figure A-20 BOC scans at different temperatures for optoboard 2008

BOC Scans at Different Temperatures

sector 9052 – optoboard 2019

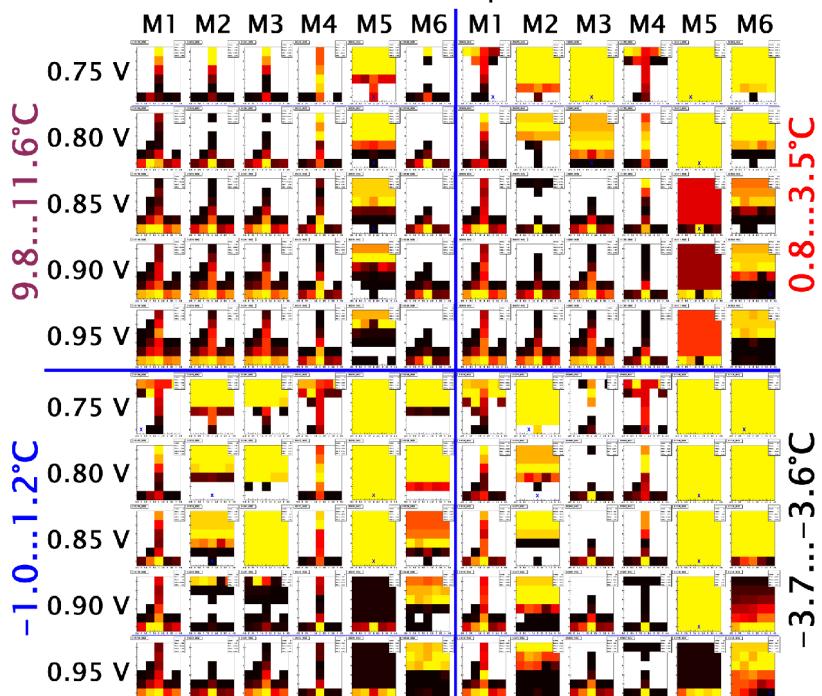


Figure A-21 BOC scans at different temperatures for optoboard 2019

BOC Scans at Different Temperatures

sector 9049 – optoboard 3019

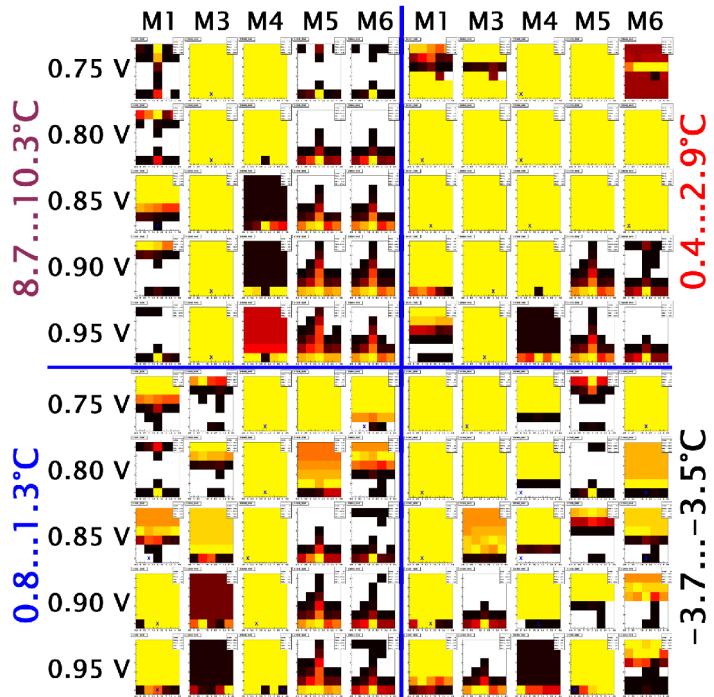


Figure A-22 BOC scans at different temperatures for optoboard 3019

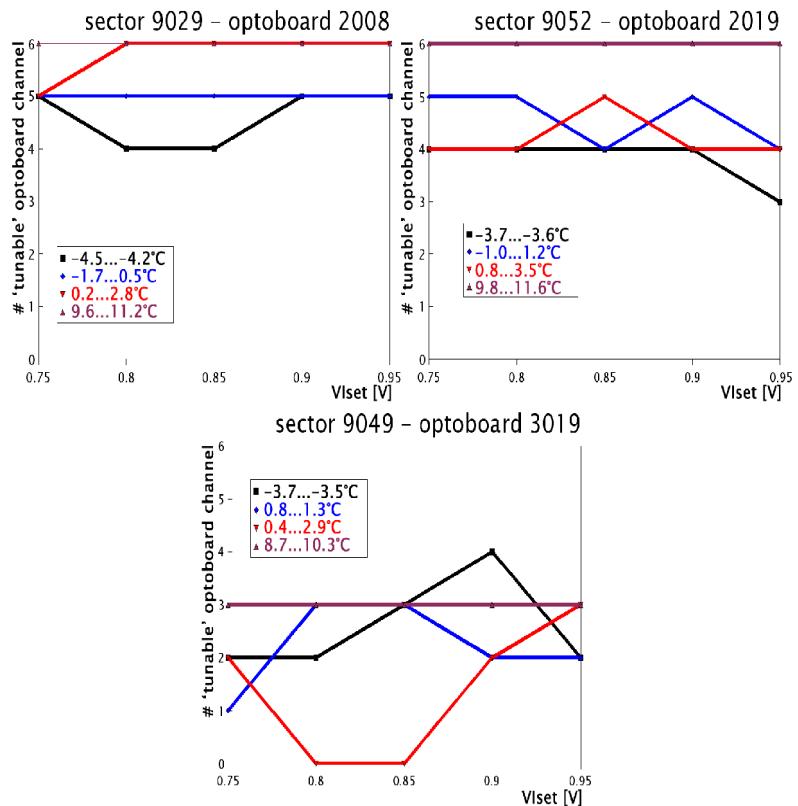


Figure A-23 'Tunable' channels versus V_{lset} [V] at different optoboard temperatures

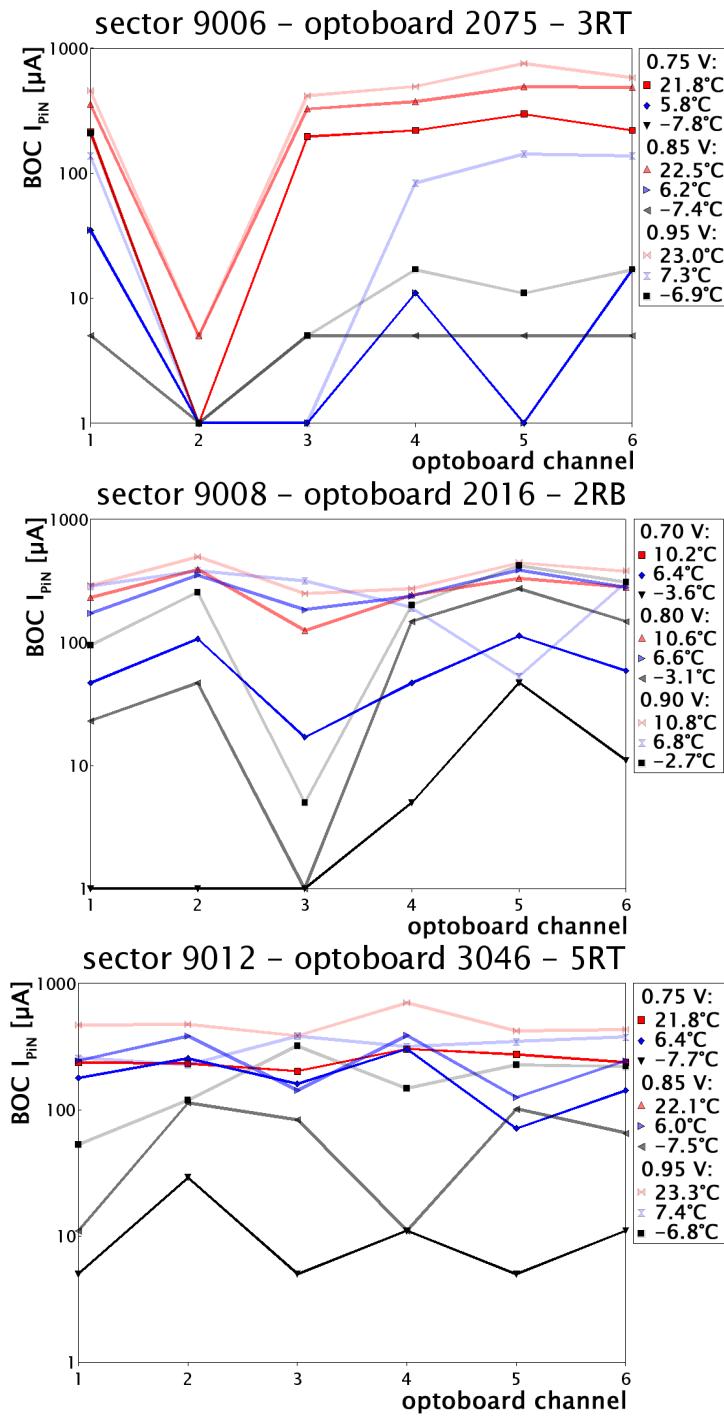


Figure A-24 BOC I_{PIN} light power measurement for three optoboards (2075, 2016 & 3046) at three different temperatures and V_{iset} values

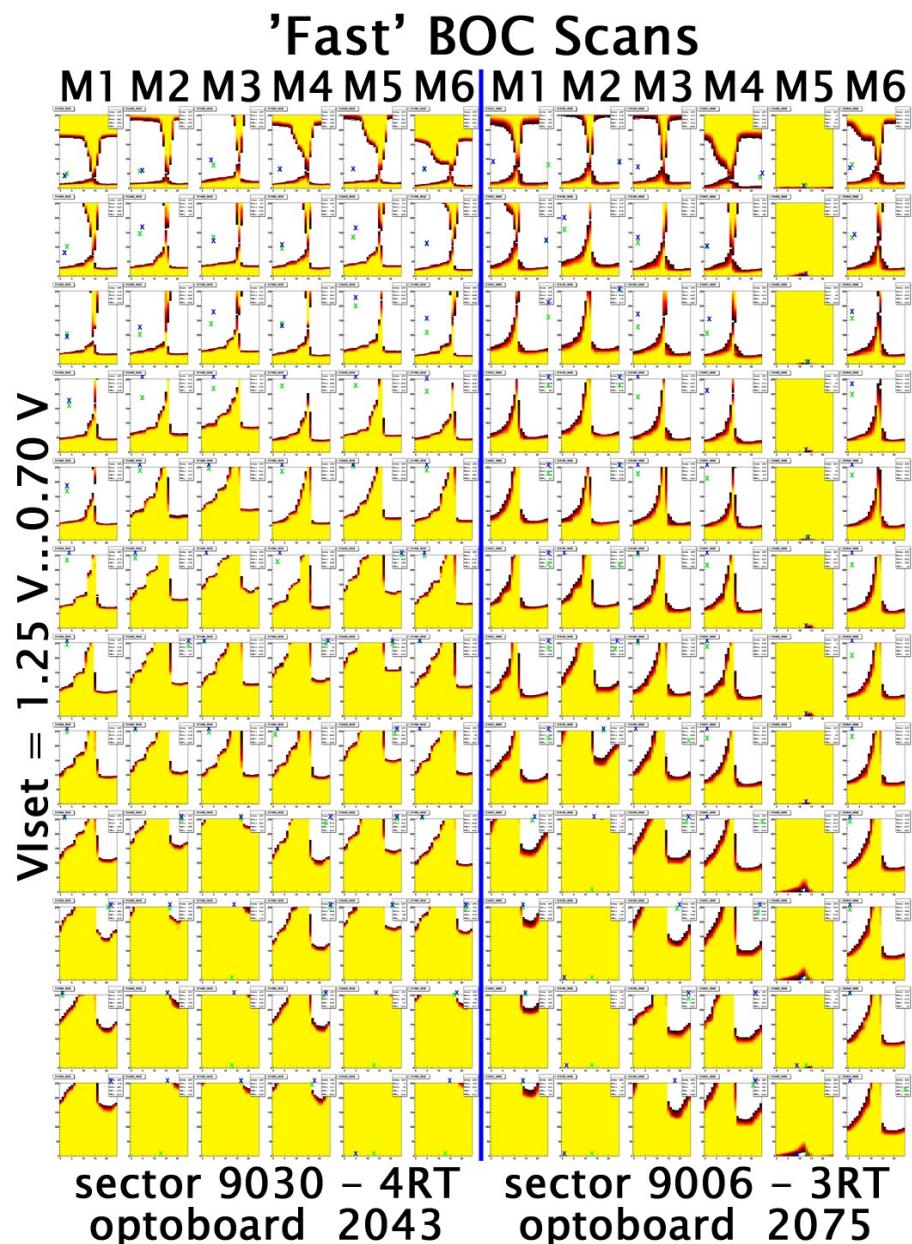


Figure A-25 'Fast' BOC scans for two optoboards (2043 & 2075). Module M5 of optoboard 2075 has a TX problem (module not configurable)

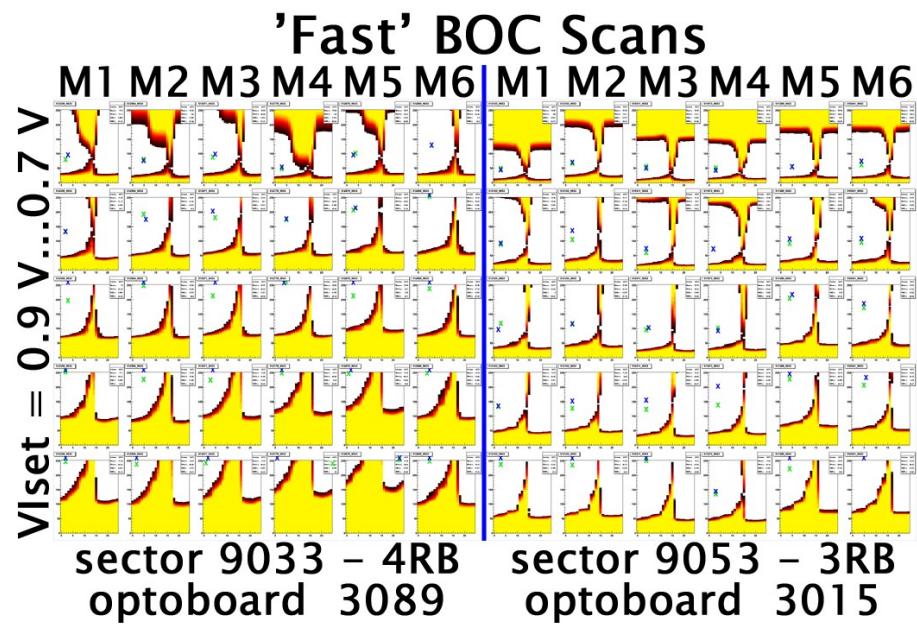
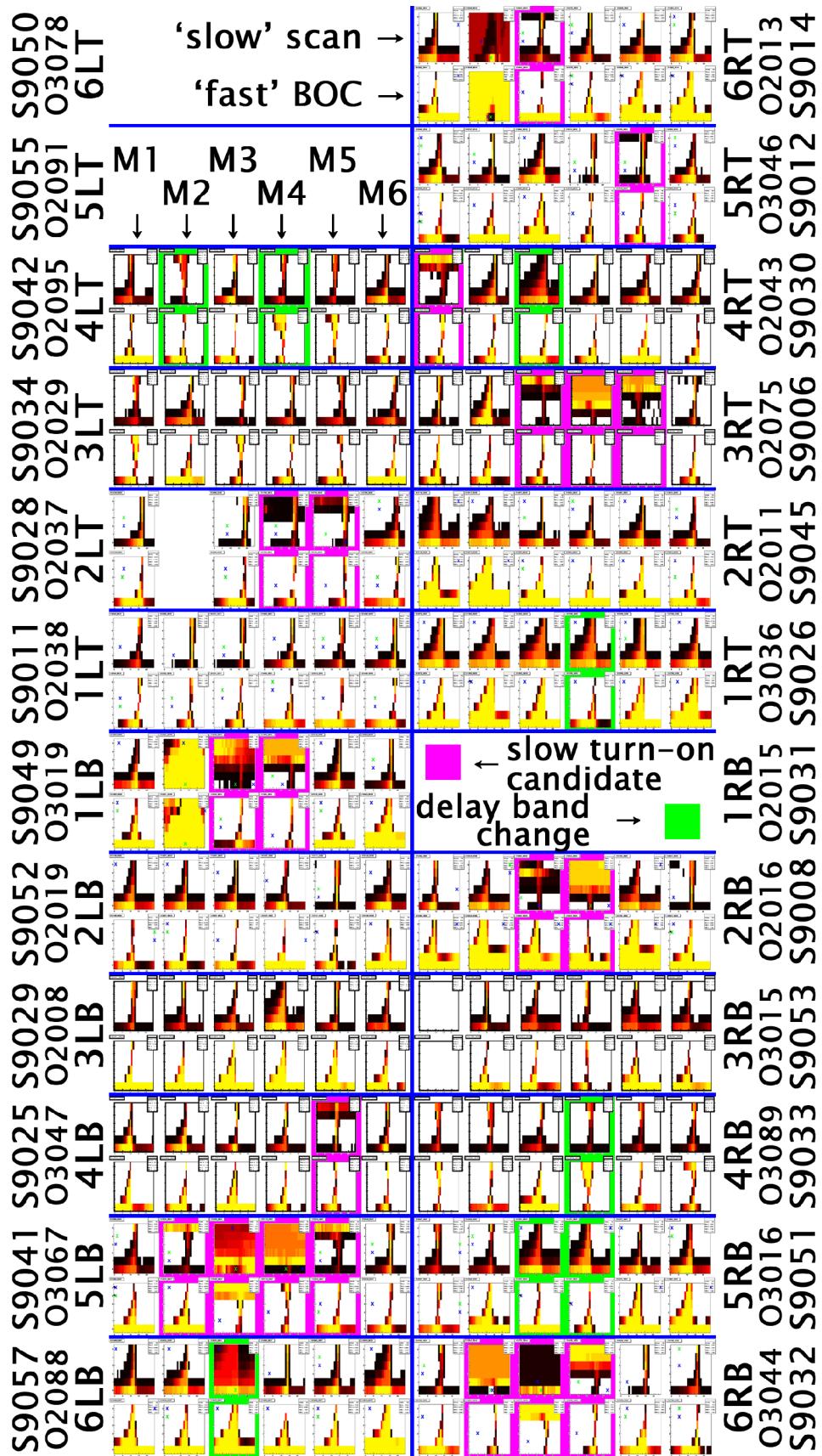


Figure A-26 'Fast' BOC scans for two optoboards (3089 & 3015).

**Figure A-27** System Test 'slow' and 'fast' BOC scan comparison at tuned V_{IsetS}

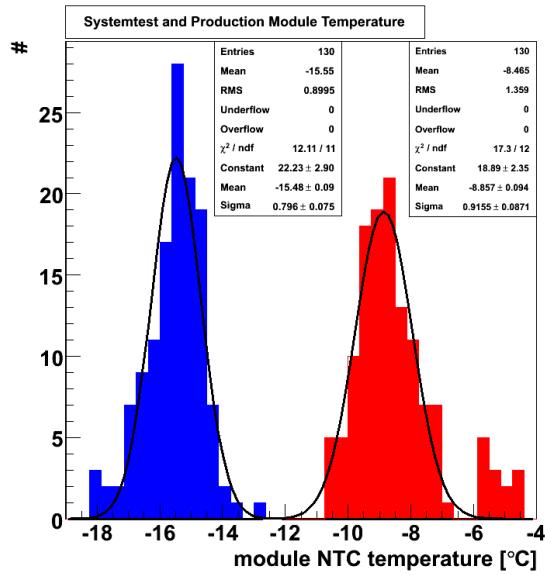


Figure A-28 System test and production tuning module temperatures

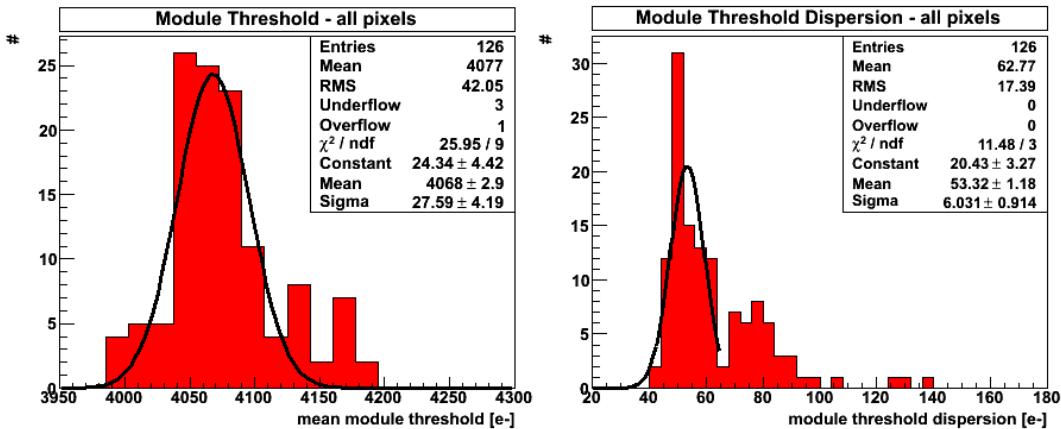


Figure A-29 Production tuning mean module threshold and threshold dispersion distributions

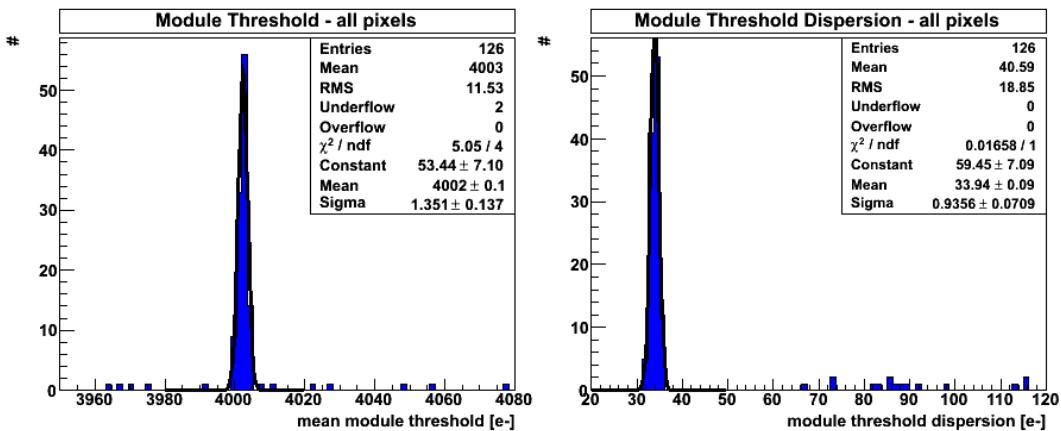
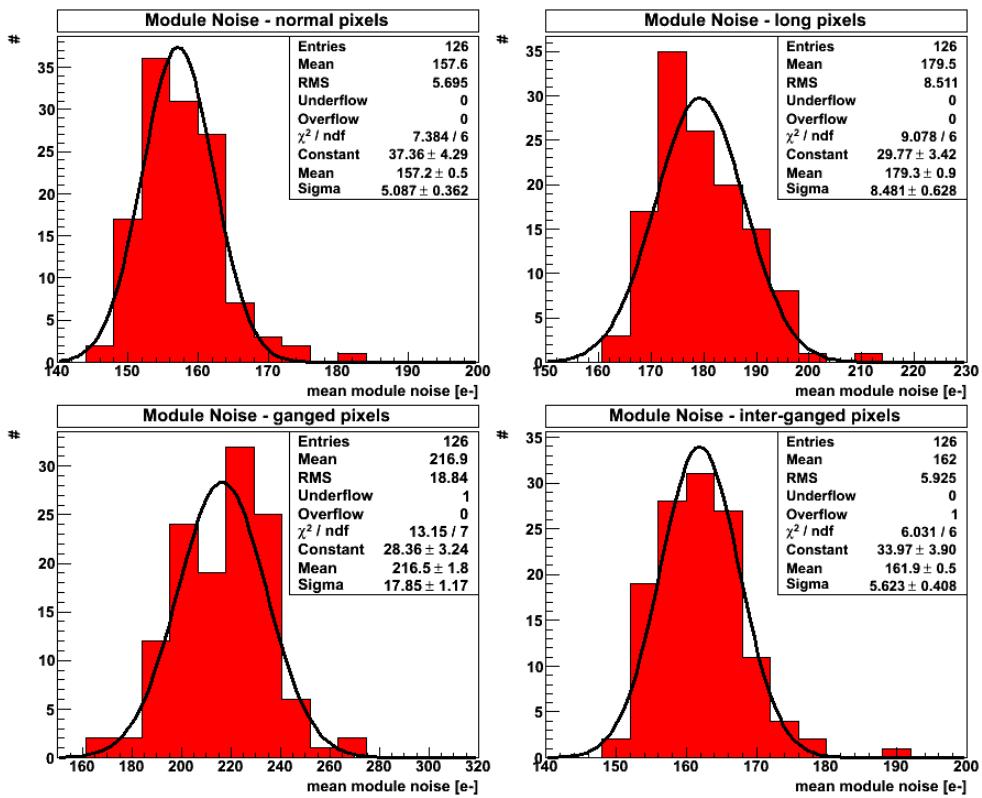
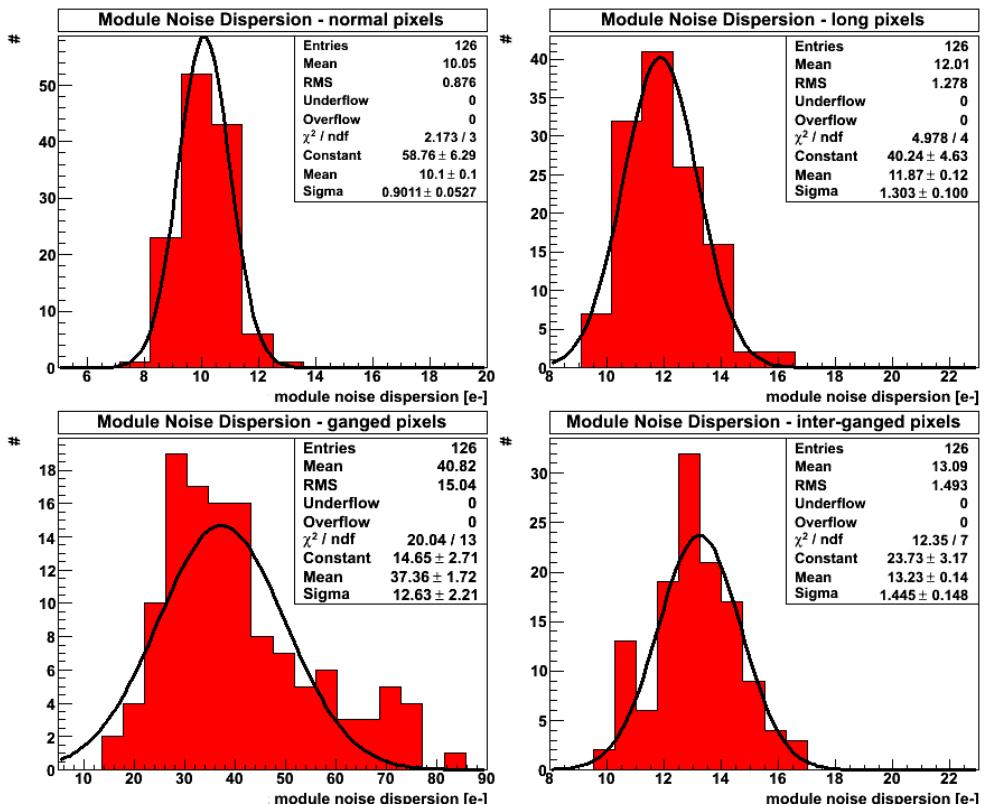
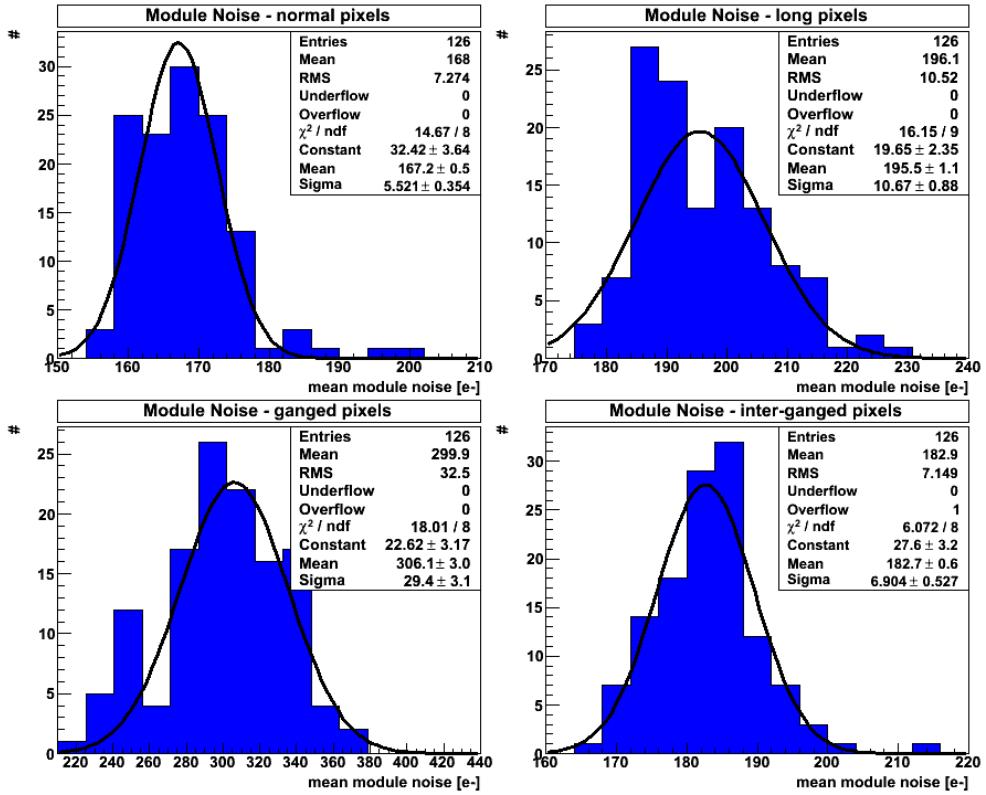
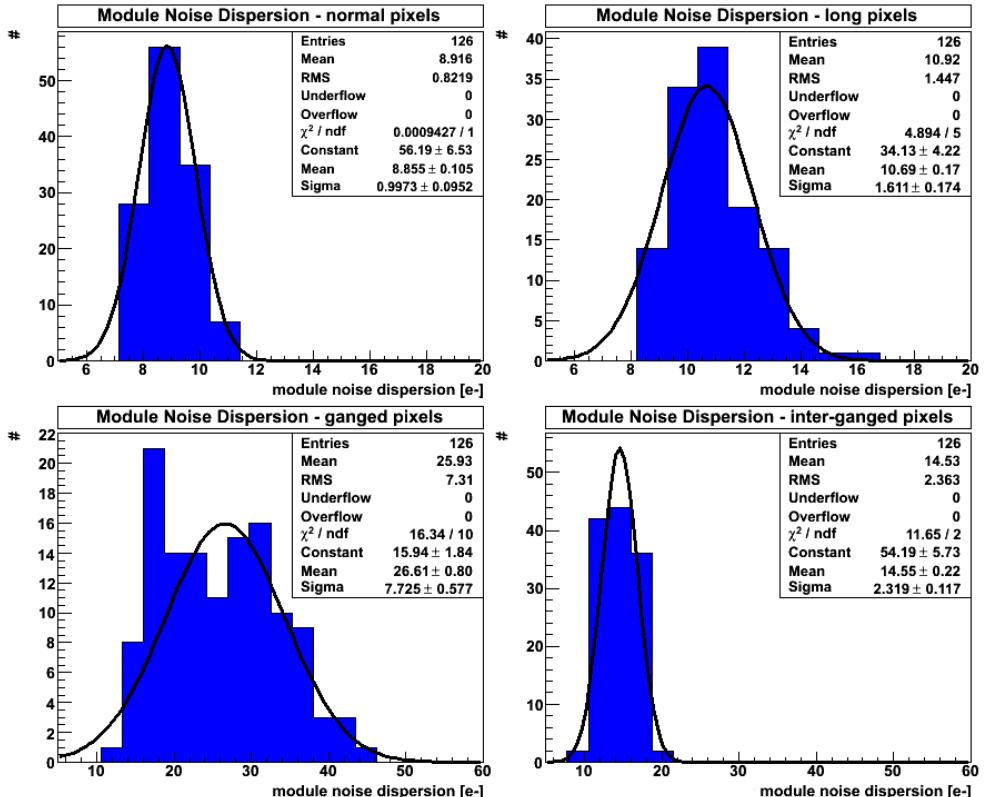


Figure A-30 System Test tuning mean module threshold and threshold dispersion distributions

**Figure A-31** Production tuning mean module noise distributions for different pixel types**Figure A-32** Production tuning module noise dispersion distributions for different pixel types

**Figure A-33** System test mean module noise distributions for different pixel types**Figure A-34** System test module noise dispersion distributions for different pixel types

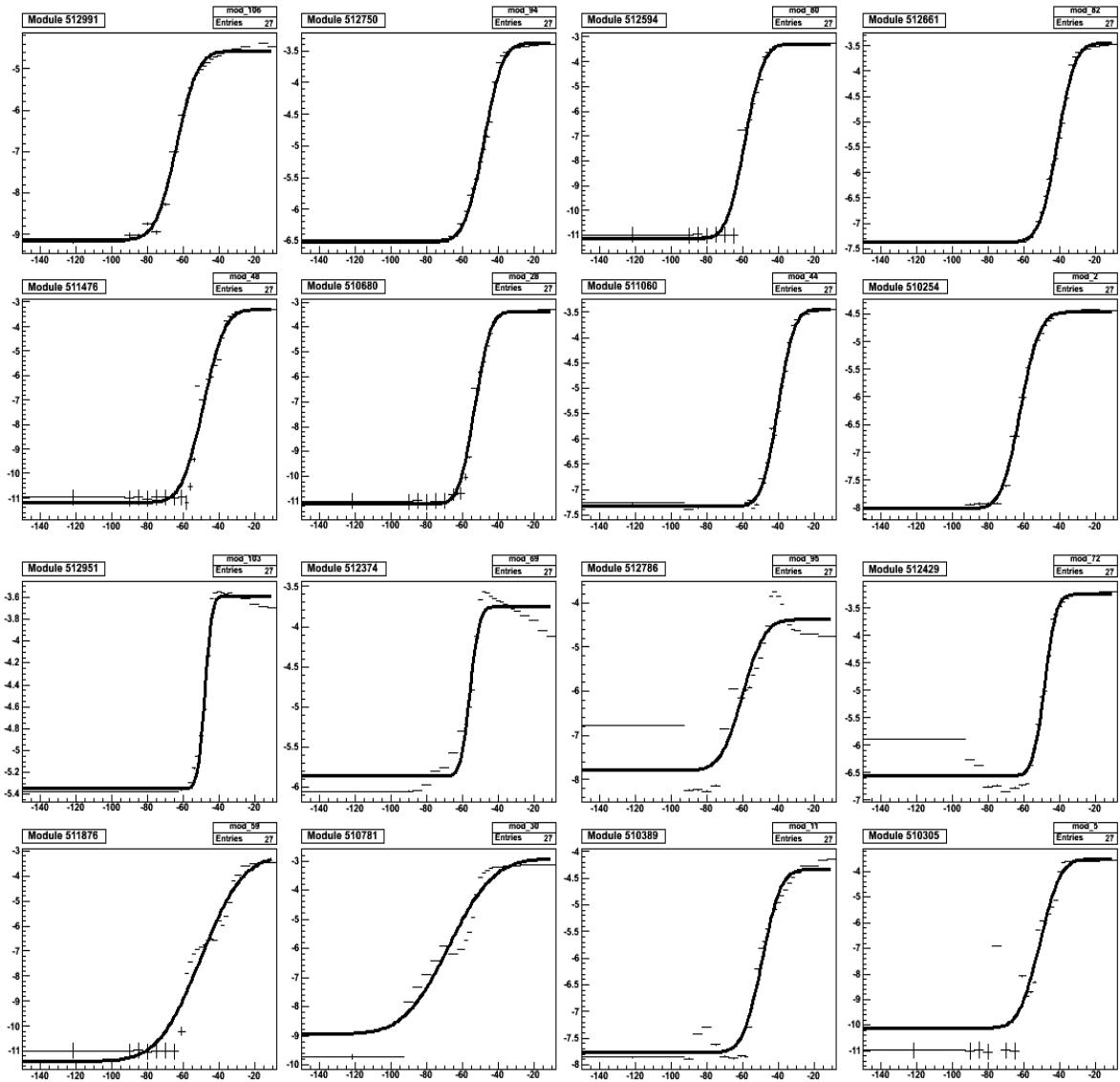


Figure A-35 S-curve fit result examples of \log_{10} noise occupancy curves. The negative sensor bias voltage is plotted along the x-axis and the y-axis represents \log_{10} of the noise occupancy. In the upper two rows low χ^2 fit result are shown and the lower two rows show fit results to noise occupancy curves which have a deviation from the expected s-curve shape.

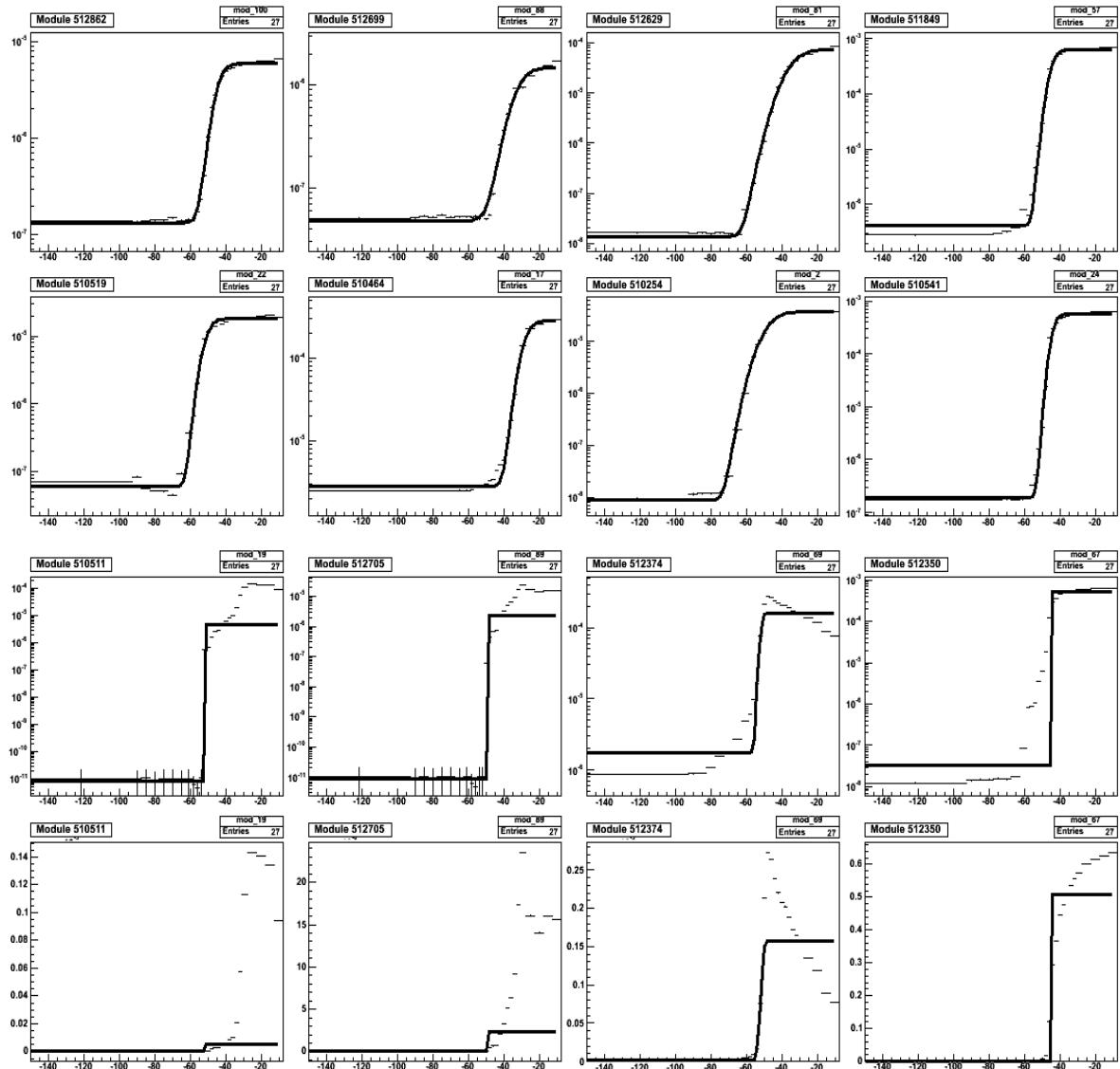
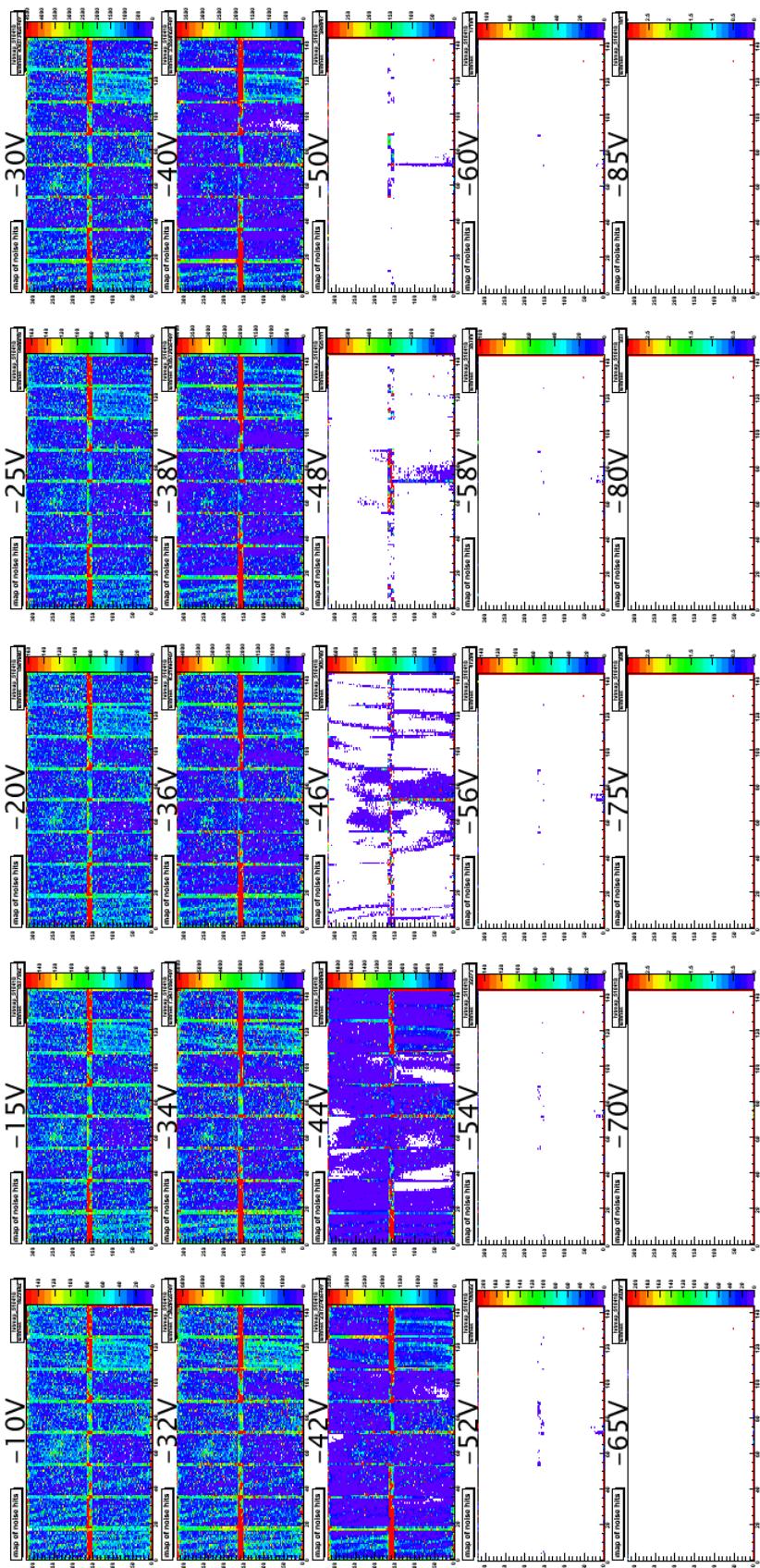


Figure A-36 S-curve fit result examples of linear noise occupancy curves. The negative sensor bias voltage is plotted along the x-axis and the y-axis represents the noise occupancy. In the upper two rows low χ^2 fit result are shown. The lower two rows show fit results to noise occupancy curves which have a deviation from the expected s-curve shape in linear and logarithmic view.

**Figure A-37** Noise occupancy scan hitmaps of module 510418

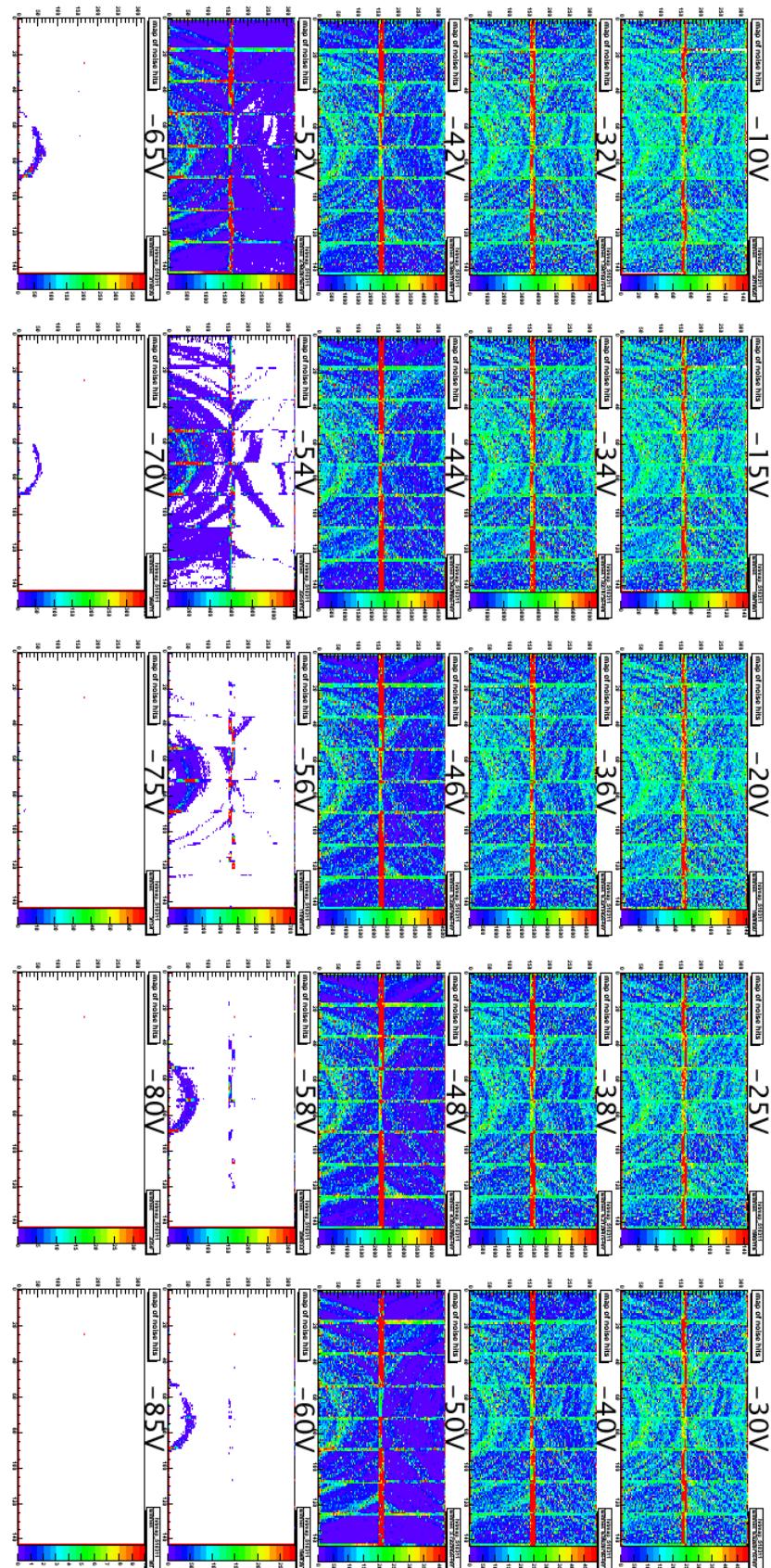


Figure A-38 Noise occupancy scan hitmaps of module 510311

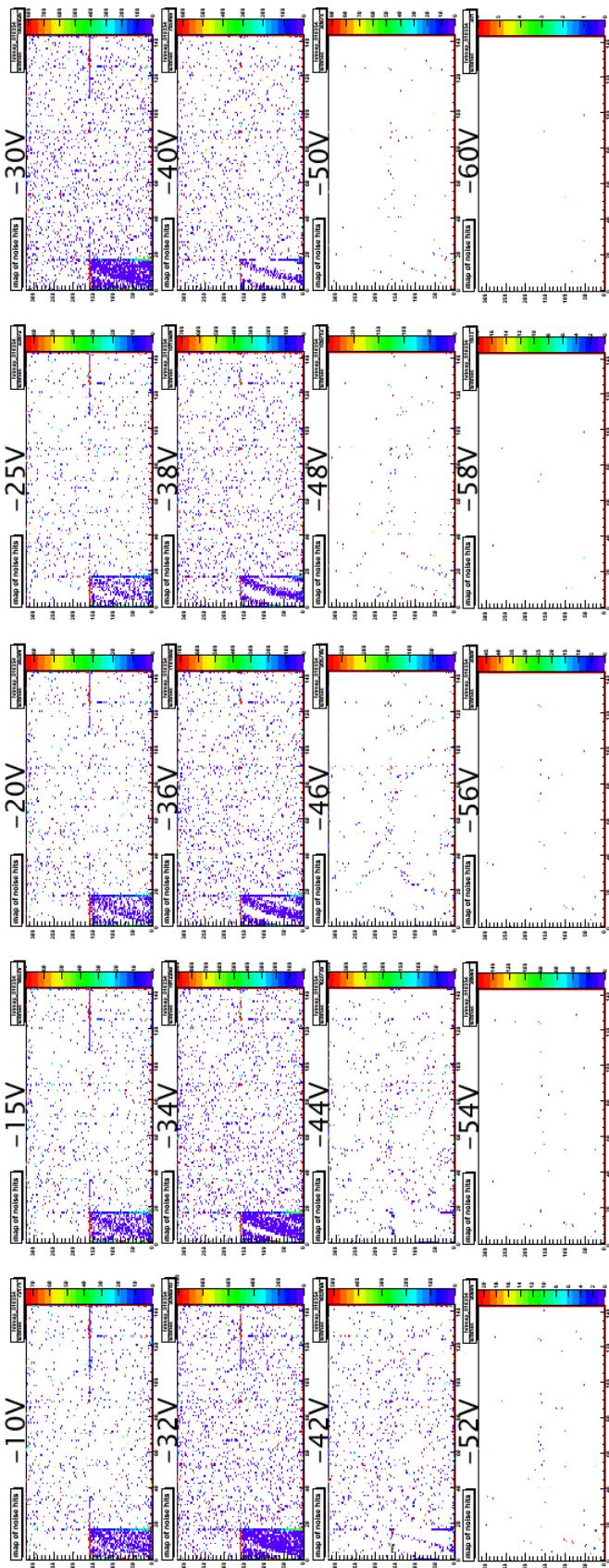


Figure A-39 Noise occupancy scan hitmaps of module 510354

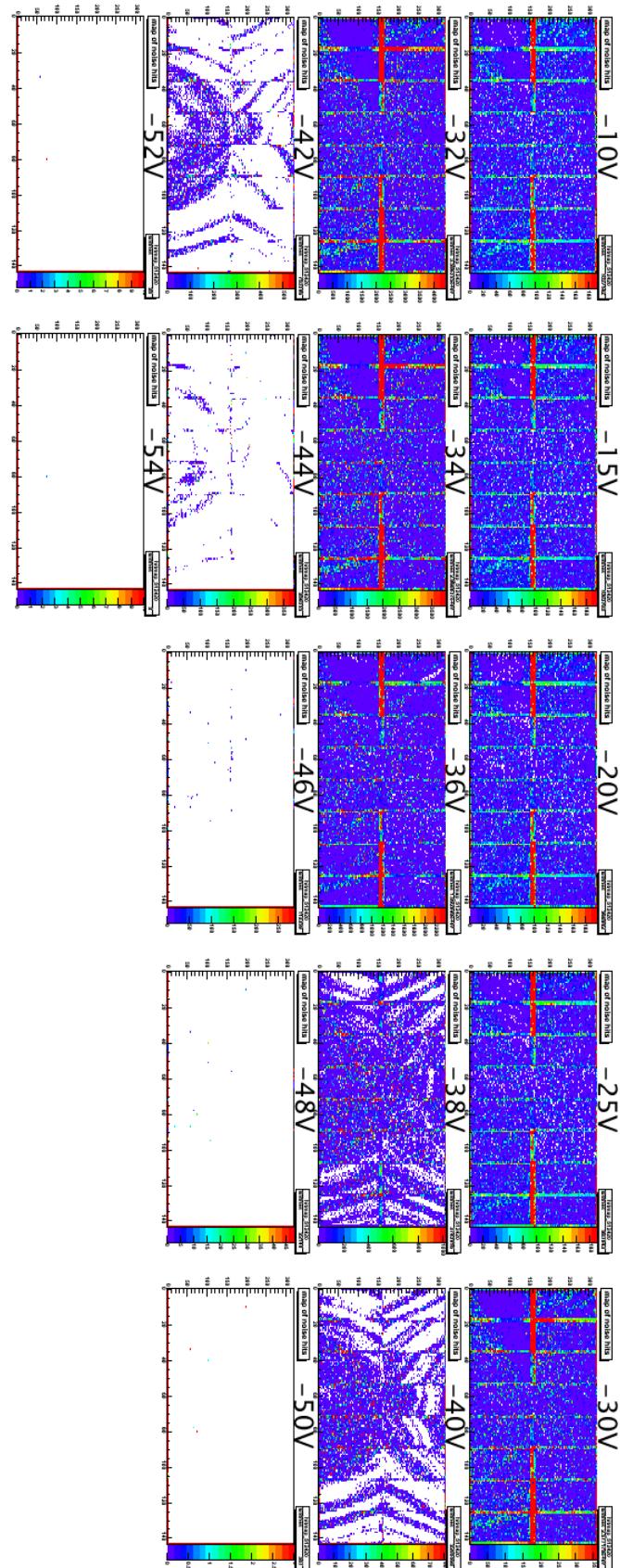


Figure A-40 Noise occupancy scan heatmaps of module 512420

'Beginning Of Fragment' marker	'0xB0F0'+S-LINK flags
start of ROD header	'0xEE1234EE'
header size	'0x9'
format version number	'0x03010000'
source identifier	0x11111111
run number	'0'+31-bit run number
extended Level1 ID	24-bit TTCrx L1ID + 8-bit ROD ECRID
bunch crossing ID	12-bit TTCrx BCID
ATLAS Level1 trigger type	8-bit CTP(LTP) L1TT
detector event type: ROD / TIM	DET
Module data	...
status 1: bit errors	error flags
status 2: count of words with errors	error count, ROL status
number of status words	'0x2'
number of data words	nData
status block pos.: '0' before/ '1' after data	'0x1'
'End Of Fragment' marker	'0xE0F0'+S-LINK flags
[...]	'0xB0F0'+S-LINK flags
[...]	...
[...]	'0xE0F0'+S-LINK flags
ATLAS Pixel Bytestream Format	
ROD header	Module hit
ROD trailer	Module header
Module trailer	Module errors
ROD:	
r = reserved	v = readout crate (0x0..0x9)
s = sub-detector ID (0x11 – Layer-1 & 2, 0x12 – endcap A, 0x13 – endcap C, 0x14 – B-layer)	w = ROD VME slot (0x05..0x15)
u = Pixel layer/disk (0x1, 0x2, 0x3)	P = pramble error t = time out error l = LVL1 error b = bunch crossing ID error M = link number D = raw data Z = trailer bit error H = header trailer limit error V = data overflow error x = filled by ROD with '0's
MCC:	
S = LVL1 skips	FE:
L = LVL1 ID	F = FE number
B = bunch crossing ID	T = time over threshold value
c = LVL1ID EoE check	C = Pixel column
failed	R = Pixel row
d = BCID EoE check	m = EOC overflow
failed	n = 'Hamming Code' error
e = LVL1ID check failed	o = com./*glob. reg. parity
f = EoE overflow	p = hit parity error
g = Hit overflow	q = FE error flag ('1111' = no error / '1110' = error)
	E = FE error code

Figure A-41 Structural view of the ATLAS Pixel bytestream format

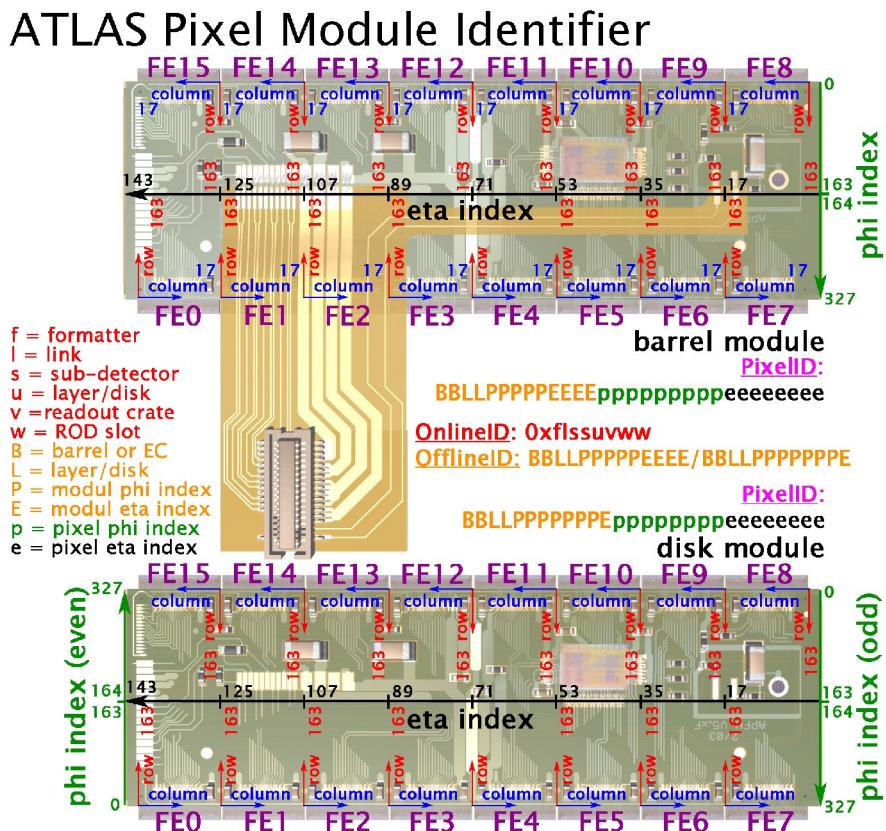


Figure A-42 Bytestream converter pixel identifier, module online and offline identifier



Figure A-43 Showing Jack Steinberger the ATLAS experiment

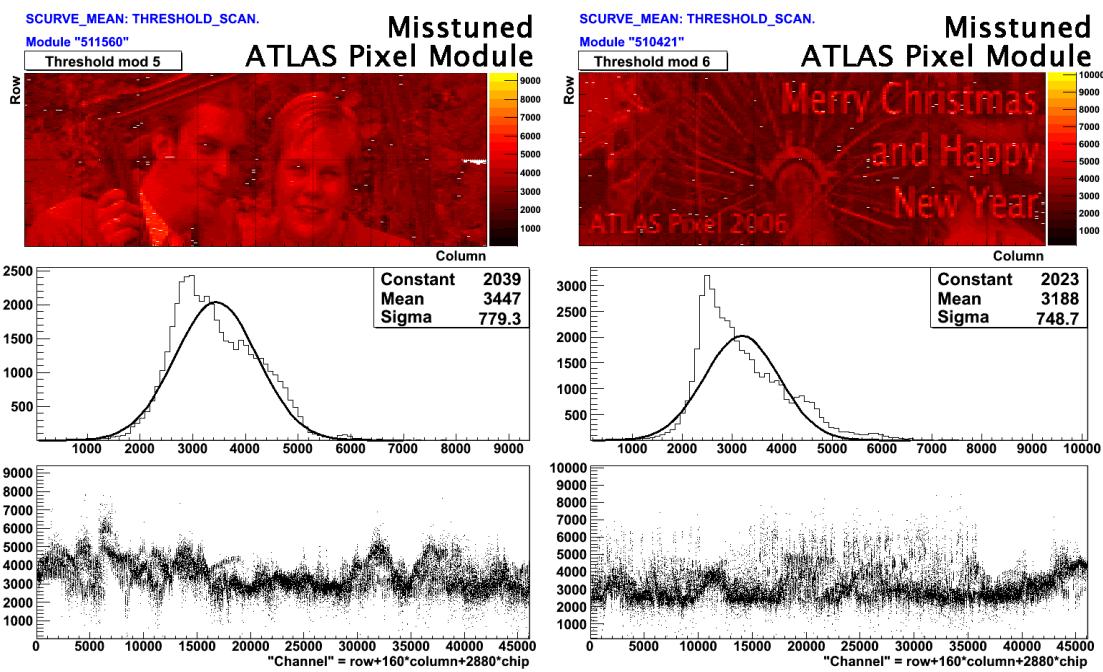


Figure A-44 Examples of “misstuned” ATLAS Pixel modules

»*Physics is, hopefully, simple. Physicists are not.*«

Ede Teller

Appendix B

Additional Tables

Detector:	ID:	Detector:	ID:
Full Event	0x00	TDAQ CTP	0x77
Pixel Layer-1 & Layer-2	0x11	L2SV	0x78
Pixel side A Disks	0x12	SFI	0x79
Pixel side C Disks	0x13	SFO	0x7a
Pixel B-layer	0x14	LVL2	0x7b
...		Event Filter	0x7c

Table B-1 Sub-detector identifiers (byte 2 in source identifier) for raw event data [BEE05]

Run Type:	ID:	Run Type:	ID:
Physics	0x00	Cosmics	0x02
Calibration	0x01	Test	0x0f

Table B-2 Run type identifiers (byte 3 in run number) for raw event data [BEE05]

Type:	Name:	Description:
Clock	BC	Bunch Crossing clock
Event ID	L1ID	24-bit Level-1 trigger IDentifier
	BCID	12-bit Bunch Crossing IDentifier
	TTID	8-bit Trigger Type IDentifier
Fast Command	L1A	Level-1 Accept
	ECR	Event Counter Reset
	BCR	Bunch Counter Reset
	CAL	CALibrate signal

Table B-3 TTC information provided by the TIM to the RODs [POS01]

»Was ich brauche:
Geld, Gesundheit, Ruhe, Frauen, Wechsel, Beliebtheit, Verehrung,
etwas Ruhm, etwas mehr Ruhm, allen Ruhm und eine neue Sommerhose.«

Martin Walser

Appendix C

Abbreviations

ADC ²³	Analog Digital Converter – section 3.2.2 p. 33	BCID ¹⁰⁰	Bunch Crossing IDentification – section 4.3.4 p. 66
ALICE ¹⁵	A Large Ion Collider Experiment – section 3.2 p. 31	BCM ⁵⁴	Beam Condition Monitor – section 4.1 p. 44
AlgTool ¹⁸⁴	Algorithm Tool – Athena tool base class – section 7.3.2 p. 181	BCR ¹⁷⁶	Bunch Counter Reset – section 6.3 p. 140
AMS ⁷⁶	Alenia Marconi Systems, Roma, Italy » www.amsjv.com – section 4.3.1 p. 50	BOC ¹¹³	Back Of Crate – section 4.6 p. 71
ASIC ¹¹⁷	Application Specific Integrated Circuit – section 4.6.1 p. 71	BOC-I-Box ¹⁵⁰	BOC-Interlock-Box – section 4.8.2 p. 87
ATLAS ³	A Toroidal LHC ApparatuS » http://www.atlas.ch – section 1 p. 2	BPM ¹⁰⁴	Bi-Phase Mark – section 4.4 p. 68
BBIM ¹³⁸	Building Block Interlock and Monitoring – section 4.8 p. 81	BPSS ⁵³	Beam Pipe Support Structure – section 4.1 p. 43
BBM ¹³⁹	Building Block Monitoring – section 4.8 p. 81	BT ¹⁷	Barrel Toroid – section 3.2.2 p. 33
		CAN ¹³⁷	Controller Area Network – section 4.8 p. 80

CASTOR ¹⁷³	CERN Advanced STORage manager » castor.web.cern.ch/castor – section 6.3 p. 137	DCS ¹⁴⁵	Detector Control System – section 4.8.1 p. 84
CCK ⁹²	Command ClocK – section 4.3.3 p. 62	DDC ¹⁵⁸	DAQ-DCS Communication – section 4.9 p. 92
CERN ²	Conseil Européen pour la Recherche Nucléaire – » http://www.cern.ch – section 1 p. 1	DDR ¹³⁵	Double Data Rate – section 4.7 p. 78
CEU ⁸⁹	Column Extractor Unit – section 4.3.3 p. 61	DFF ⁹³	Delay Flip-Flop – section 4.3.3 p. 62
CiS ⁷⁹	CiS Institut für Mikrosensorik gGmbH , Erfurt, Germany » www.cismst.de – section 4.3.2 p. 54	DFM ¹³⁶	Data Flow Manager – section 4.7 p. 79
CMOS ⁹¹	Complimentary Metal-Oxide Semiconductor – section 4.3.3 p. 62	DICE ⁹⁵	Dual Interlock Storage Cell – section 4.3.3 p. 62
CMS ¹⁴	Compact Muon Solenoid – section 3.2 p. 31	DMA ¹³⁰	Direct Memory Access – section 4.6.2 p. 76
CPLD ¹²²	Complex Programmable Logic Device – section 4.6.1 p. 72	DORIC ¹⁰⁴	Digital Optical Receiver IC – section 4.4 p. 68
CS ¹⁹	Central Solenoid – section 2.2.3 p. 33	Draka ¹⁰⁹	Draka Comteq Optical Fibre , Eindhoven, Netherlands » www.drakafibre.com – section 4.5 p. 70
CSC ²¹	Cathode Strip Chamber – section 3.2.2 p. 33	DRX ¹²⁰	Driver Receiver IC – section 4.6.1 p. 72
CTP ⁴¹	Central Trigger Processor – section 3.2.5 p. 39	DSM ⁸¹	Deep-SubMicron – section 4.3.3 p. 58
DAC ⁸²	Digital Analogue Converter – section 4.3.3 p. 58	DSP ¹²⁶	Digital Signal Processor – section 4.6.2 p. 74
DAQ ³⁹	Data-AcQuisition – section 3.2.5 p. 39	DST ¹⁶⁸	Dummy Support Tube – section 5.5 p. 111
		DYMAX ¹⁶⁰	DYMAX Corporation, Torrington, CT, USA » www.dymax.com – section 5.1 p. 94

ECL ¹³²	Emitter Coupled Logic – section 4.6.3 p. 77	FE ⁶⁸	Front-End – section 4.3 p. 47
ECR ¹⁷⁷	Event Counter Reset – section 6.3 p. 141	Fermilab ¹²	Fermi National Accelerator Laboratory » http://www.fnal.gov – section 3.1 p. 29
ECT ¹⁸	End-Cap Toroid – section 3.2.2 p. 33	FET ⁹⁶	Field Effect Transistor – section 4.3.3 p. 64
EF ⁴⁹	Event Filter – section 3.2.5 p. 41	FIFO ⁹⁰	First-In, First-Out – section 4.3.3 p. 62
EFB ¹²⁹	Event Fragment Builder – section 4.6.2 p. 75	FIT ¹⁵⁵	Front End Integration Tool – section 4.9 p. 89
ELMB ¹⁴⁶	Embedded Local Monitor Box – section 4.8.1 p. 84	FPGA ¹²³	Field Programmable Gate Array – section 4.6.1 p. 73
EM ²⁷	Electro Magnetic – section 3.2.3 p. 35	FSM ¹⁵⁷	Finite State Machine – section 4.9 p. 90
EMI ⁶⁶	Electro-Magnetic Interference – section 4.2 p. 46	Fujikura ⁶¹	Fujikura Ltd., Tokyo, Japan » http://www.fujikura.co.jp – section 4.1 p. 45
EMS ¹⁷⁸	Event Monitoring Service – section 7.2.1 p. 175	FWHM ³¹	Full Width at Half Maximum – section 3.2.3 p. 35
EOC ⁸⁸	End Of Column – section 4.3.3 p. 61	GA	Geographical Address – section 4.3.4 p. 67
EoE ⁹⁸	End-of-Event – section 4.3.4 p. 65	GDAC ⁸⁴	Global DAC – section 4.3.3 p. 59
Ericsson ⁶⁴	Telefonaktiebolaget LM Ericsson , Stockholm, Sweden » http://www.ericsson.com – section 4.1 p. 45	GDSI ⁷⁸	Grinding and Dicing Services Inc. , Sunnyvale, CA, USA » www.wafergrind.com – section 4.3.1 p. 50
FCAL ³⁶	Forward CALorimeter – section 3.2.3 p. 36	GF PEEK ¹⁵⁹	Glass-Fiber reinforced PolyEtherEtherKetones – section 5.1 p. 94
FCB ⁷³	Flexible Circuit Board – section 4.3 p. 48		
FDAC ⁸³	Feedback DAC – section 4.3.3 p. 59		

GNAM ¹⁸⁰	GNAM is Not AtlMon – section 7.2.1 p. 175	ISEG ¹⁴¹	ISEG Spezialelektronik GmbH, Radeberg, Germany » www.iseg-hv.de – section 4.8 p. 81
GPIB ¹⁶⁵	General Purpose Interface Bus – section 5.2.1 p. 95	ISP ⁵⁷	Inner Service Pannel – section 4.1 p. 44
GRIN ¹¹⁰	GRaded INdex – section 4.5 p. 70	ITC ²⁹	Intermediate Tile Calorimeter – section 3.2.3 p. 35
GSW ⁴	G. Glashow, A. Salam and S. Weinberg – section 1.4 p. 9	ITT ¹⁶⁷	Integration and Testing Tool – section 5.5 p. 110
GUI ¹⁵³	Graphical User Interface – section 4.9 p. 89	IZM ⁷⁵	Frauenhofer Institut für Zuverlässigkeit und Mikrointegration, Berlin, Germany » www.izm.fhg.de – section 4.3.1 p. 50
HEC ³⁵	Hadronic End-cap Calorimeter – section 3.2.3 p. 36		
HLT ⁵¹	High Level Trigger – section 3.2.5 p. 41	LAr ³²	Liquid Argon – section 3.2.3 p. 35
HOLA ¹²⁴	High-speed Optical Link for Atlas » http://hs1.web.cern.ch/HSI/link/devices/hola/ – section 4.6.1 p. 73	LDC ⁷²	Local Decoupling Capacitor – section 4.3 p. 48
HV ⁷⁴	High Voltage – section 4.3 p. 49	LED ¹⁴⁴	Light Emitting Diode – section 4.8.1 p. 83
I-BOX ¹⁴⁸	Interlock-box – section 4.8.2 p. 86	LEMO ⁶³	LEMO S.A., Ecublens, Switzerland » http://www.lemo.com – section 4.1 p. 45
ID ²⁰	Inner Detector – section 3.2.2 p. 33	LHC ¹	Large Hadron Collider » http://www.cern.ch/lhc – section 1 p. 1
IDB ¹⁵¹	Interlock Distribution Boxes – section 4.8.2 p. 88	LTP ⁴²	Local Trigger Processors – section 3.2.5 p. 40
IEL ¹⁰	Ionizing Energy Loss – section 2.5 p. 24	LVDS ⁹⁷	Low Voltage Differential Signaling – section 4.3.3 p. 63
Ipp1Box ¹⁴⁹	Interlock patch panel 1 Box – section 4.8.2 p. 87	LVL1 ⁴⁰	LeVeL-1 – section 3.2.5 p. 39

LVL1ID ⁹⁹	LeVeL 1 IDentification – <i>section 4.3.4 p. 66</i>	OHS ¹⁷⁹	Online Histogramming Server – <i>section 7.2.1 p. 175</i>
LVL2 ⁴⁸	LeVeL-2 – <i>section 3.2.5 p. 41</i>	OKS ¹⁸²	Object Kernel Support – <i>section 7.2.2 p. 177</i>
MCC ⁷¹	Module Control Chip – <i>section 4.3 p. 47</i>	ON ⁸⁰	ON Semiconductor Czech Republic a.s., Roznov, Czech Republic (www.onsemi.cz) – <i>section 4.3.2 p. 54</i>
MDAC ¹¹⁸	Multi channels DAC – <i>section 4.6.1 p. 72</i>	Op-Amp ¹⁴⁷	Operational Amplifier – <i>section 4.8.1 p. 84</i>
MDT ²²	Monitored Drift-Tube – <i>section 3.2.2 p. 33</i>	OPC ¹⁵⁴	Object Linking and Embedding for Process Control – <i>section 4.9 p. 89</i>
MIP ⁷	Minimum Ionizing Particles – <i>section 2 p. 15</i>	OSP ⁵⁸	Outer Service Panel – <i>section 4.1 p. 44</i>
MSSM ⁶	Minimal Supersymmetric Standard Model – <i>section 1.5 p. 13</i>	PCB ¹⁰²	Printed Circuit Board – <i>section 4.4 p. 67</i>
MUX ⁹⁴	MUltipleXer – <i>section 4.3.3 p. 62</i>	pCVD ⁵⁵	poly-crystalline Chemical Vapor Deposition – <i>section 4.1 p. 44</i>
MXI ¹⁶⁴	Multisystem eXtension Interface – <i>section 5.2.1 p. 95</i>	PECL ¹³¹	Positive Emitter Coupled Logic – <i>section 4.6.3 p. 77</i>
NIEL ⁸	Non Ionizing Energy Loss – <i>section 2.5 p. 23</i>	PiN ¹⁰³	Positive-intrinsic-Negative – <i>section 4.4 p. 67</i>
NIM ¹³³	Nuclear Instrumentation Module – <i>section 4.6.3 p. 77</i>	PKA ⁹	Primary Knock on Atom – <i>section 2.5 p. 23</i>
NTC ⁷⁰	Negative Temperature Coefficient – <i>section 4.3 p. 47</i>	PLC ¹⁷²	Programmable Logic Controller – <i>section 6.2.1 p. 127</i>
OCTJR ¹⁸⁶	On Coolant Tank Jumping Rat – <i>Epilogue</i>	PMT ³⁰	PhotoMultiplier Tube – <i>section 3.2.3 p. 35</i>
OHP ¹⁸¹	Online Histogram Presenter – <i>section 7.2.1 p. 175</i>	PP0 ⁵⁹	Patch Panel 0 – <i>section 4.1 p. 45</i>

PP1 ⁶²	Patch Panel 1 – section 4.1 p. 45	ROL ¹²⁵	Read-Out Link – section 4.6.1 p. 73
PP2 ¹¹¹	Patch Panel 2 – section 4.5 p. 70	ROS ¹¹⁶	Read-Out Subsystem – section 4.6 p. 71
PRM ¹²⁷	Program Reset Manager – section 4.6.2 p. 74	RPC ²⁴	Resistive Plate Chamber – section 3.2.2 p. 34
PST ⁶⁵	Pixel Support Tube – section 4.1 p. 45	SCA ³⁴	Switching Capacitor Array – section 3.2.3 p. 35
PVSS ¹⁵²	Prozess Visualisierungs- und Steuerungs-System, ETM professional control GmbH, Eisenstadt, Austria » www.etm.at – section 4.9 p. 89	SC-OLink ¹⁴²	Supply and Control for Optical Link – section 4.8 p. 81
QCD ⁵	Quantum ChromoDynamics – section 1.4 p. 9	SCT ³⁸	SemiConductor Tracker – section 3.2.4 p. 38
RAM ¹¹⁹	Random Access Memory – section 4.6.1 p. 71	SDRAM ¹²⁸	Synchronous Dynamic Random Access Memory – section 4.6.2 p. 75
RCC ¹¹⁵	ROD Crate Controller – section 4.6 p. 71	SEU ⁴⁴	Single Event Upset – section 3.2.5 p. 40
RDB ¹⁷⁰	Remote DataBase – section 6.2 p. 127	SFI ⁵⁰	Sub-Farm Interface – section 3.2.5 p. 41
RDO ¹⁸³	Raw Data Object – section 7.3.2 p. 181	SFO ⁵²	Sub-Farm Output – section 3.2.5 p. 42
RMS ²⁶	Root Mean Square – section 3.2.2 p. 34	SIMM ¹⁰⁸	Stepped Index MultiMode – section 4.5 p. 71
ROB ⁴⁶	Read-Out Buffer – section 3.2.5 p. 41	SIT ¹⁵⁶	System Integration Tool – section 4.9 p. 90
ROBIN ¹³⁴	Read-Out Buffer INput – section 4.7 p. 78	SMD ⁶⁹	Surface Mounted Device – section 4.3 p. 47
ROD ⁴⁵	Read-Out Driver – section 3.2.5 p. 41	SMS ¹⁸⁵	Senseless Money Swale – Epilogue
RoI ⁴⁷	Region-of-Interest – section 3.2.5 p. 41	SMT ⁶⁰	Surface Mount Technology – section 4.1 p. 45

S-LINK ¹²¹	Simple-LINK » hsi.web.cern.ch/HSI/s-link – <i>section 4.6.1 p. 72</i>	TPCC ¹⁶¹	Turbo Pixel Control Card – <i>section 5.2.1 p. 94</i>
SPS ¹³	Super Proton Synchrotron – <i>section 3.1 p. 30</i>	TPLL ¹⁶³	Turbo Pixel Low Level – <i>section 5.2.1 p. 95</i>
SQP ⁵⁶	Service Quarter Panel – <i>section 4.1 p. 44</i>	TRT ³⁷	Transition Radiation Tracker – <i>section 3.2.4 p. 37</i>
SRAM ⁷⁷	Static Random Access Memory – <i>section 4.3.3 p. 61</i>	TTC ¹⁰¹	Trigger, Timing and Control – <i>section 4.3.4 p. 66</i>
STMicroelectronics ¹⁴³	STMicroelectronics , Geneva, Switzerland » www.st.com – <i>section 4.8.1 p. 82</i>	TTCex ¹⁷⁵	TTC encoder/transmitter – <i>section 6.3 p. 140</i>
SuRF ¹⁶²	Supply and Readout/Fanout – <i>section 5.2.1 p. 94</i>	TTCvi ¹⁷⁴	TTC vmeBUS interface – <i>section 6.3 p. 140</i>
TDAC ⁸⁵	Trim DAC – <i>section 4.3.3 p. 59</i>	UBM ⁷⁷	Under Bump Metalization – <i>section 4.3.1 p. 50</i>
Tektronix ¹⁶⁹	Tektronix Inc., Beaverton, OR, USA » www.tek.com – <i>section 6.1.1 p. 119</i>	VCSEL ¹⁰⁶	Vertical Cavity Surface Emitting Laser – <i>section 4.4 p. 69</i>
TGC ²⁵	Thin Gap Chamber – <i>section 3.2.2 p. 34</i>	VDC ¹⁰⁷	VCSEL Driver Chip – <i>section 4.4 p. 69</i>
TIM ¹¹⁴	TTC Interface Module – <i>section 4.6 p. 71</i>	VME ¹¹²	Versa Module Europa – <i>section 4.6 p. 71</i>
TMT ⁶⁷	Thermal Management Tile – <i>section 4.2 p. 47</i>	WIENER ¹⁴⁰	WIENER Plein und Baus GmbH, Burscheid, Germany » www.wiener-d.com – <i>section 4.8 p. 81</i>
TOF ⁴³	Time-Of-Flight – <i>section 3.2.5 p. 40</i>	XCKr ¹⁶⁶	XCK return – <i>section 5.2.2 p. 96</i>
TOT ⁸⁶	Time Over Threshold – <i>section 4.3.3 p. 59</i>		

»Very strange people, physicists. In my experience the ones who aren't actually dead are in some way very ill.«

Douglas Adams

Appendix D

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»Bewundert und bewundernd kommt man in die Welt,
verachtet und verachtend verläßt man sie. Wenn alles normal verläuft.«

Martin Walser

Epilogue

You really did it. I'm quite impressed that you jumped directly from the prologue to the epilogue without reading a single word. Did you had at least a look at the robot caricatures I draw? If you are one of the brave who really fought your way through the entire book I'm really sorry. Please send me your mobile phone and I will send you a SMS¹⁸⁵ with the key word "SORRY". Everyone who participates will take part in a draw lottery for a mobile phone. However, where did I stop in the prologue? Attila answers with "QWERTYUIOP", the only – wait we passed that already.

The doctor shrugs off Attila and begins to turn around, but suddenly, not believing his eyes, he notices the smallest of the robots begins to splutter in his lambent light language. Attila, elated by his C++ conversation success, immediately identifies it as Morse code and translates: "I-F I C-O-U-L-D R-E-M-E-M-B-E-R T-H-E N-A-M-E-S O-F A-L-L T-H-E-S-E P-A-R-T-I-C-L-E-S COMMA I-D B-E A B-O-T-A-". He gets stopped by the doctor next to him: "She speaks ancient bytestream, but with a horrible accent and lisps quite heavily. We guess her communication module is poorly adjusted. But we are happy she now speaks at all." Attila gets interested and decides in absence of beach related alternatives to understand the diagnosis and treatments of the robot doctors. "Who are you?", he asks. "We are followers of φυσιολογία from the house of the ATLAS club." "ATLAS? My peticle machine?", Attila exclaims. "How should I know? I wasn't present in your unconsciousness hallucinations. The ATLAS club vets and psychologically attends robots from the ATLAS family, all build by a scientific madman threatening the world. *[et voilà: you, dearest reader, found the explanation of the subhead]*", the doctor explains. He tells him the three pieces of wisdom of the followers of φυσιολογία: "Three is the magic number – Three dominates your entire career. There are three important things you should take to heart to be a good follower of φυσιολογία:

1. Praise yourself every day
2. Have an excellent memory
3. , 3rd, ..., 3rd I forgot

And there are three types of φυσιολογία followers:

1. those who can count
2. those who cannot

If you follow this advises you may join the ATLAS club." "Yeah. Where do I sign?"

Attila spends several years in the robo ward and learns a lot about modern art, how to sentinel fridges, red cables, inverted reverse psychology, filigree silicon craftsmanship, blue cables, new ergonomic possibilities of sleep, true love, freezing communication modules, probe needle fencing, black cables, incontinence of robot veins, loyal friendship, gray cables, imaginary psychosomatic diseases, more gray

cables, creative insect control, liquid dry air, the definition of 'in principle', gray cable trauma, bi-phase beer cooling, OCTJR¹⁸⁶s, deep frustration, cosmic muon rate adjustment, left/right and all their 213 possible permutations, mostly nonviolent motivation with a (gray) cable harness, quiet dignity and grace, sunlight and other harmful light source interlock systems, exuberant happiness, wrestling with many-headed cable hydras, and last, but not least, about successful declaration of the (temporary) end of the physical examination – or as sometime summarized: life.

My personal favorite scene is when Attila meets Jewei, the god of sarcasm. Attila quarrels, tries to come up with an intelligence pretending question and ends up with: "So, you are the god of irony?" (retrospectively viewed the second most intelligent question after "Hmm?"). "No – ", Jewei answers, "I tried to be sarcastic, but I gave it up a long time ago. It's really not worth it. Every time I believed I was sarcastic, everybody else confirmed that I was just describing reality." In lieu of another intelligent question Attila decides to rename Jewei into 'GOS_JeWei/13-%z45:L6273b'.

It takes Attila a long and painful process to understand that the success of a project like this mainly increases with the number of naming conventions. In detail Jack describes how Attila in his first approach names everything after a single scheme, gets depressed because nothing works, creates one new naming convention after the other, spends months with engraving conversion tables into stone and ends up with 21 naming conventions. His favorite comprise the names of extinct

Stop. Now I have summarized you more than enough of the story. So if you decide to read the book yourself, you can directly continue the story on the second half of the first introduction page where Attila describes his favorite naming convention.

But before I also would like to say some words about the history of this revised edition of the OSTT(AOOOMMOL)LA. As many literary critics have argued for years about the political and social statement of this book, I decided to visit Jack Dapid in the Michael Faraday Memorial Mental Home And Weapon Factory, Panic, Pennsylvania, USA, in late 1982 to make sure all my changes have been made in the spirit in which it was intended. Mostly sober he explained me that all analysts only thought of absurd interpretations such as dependencies on the first world war or the global butter crisis, but none of them understood the obvious connection to a warm summer night, an overwhelming amount of vodka bottles and three Swedish au pair girls. Even though I rate myself as an expert on this book I cannot explain to you, dearest reader, the meaning of the sub-subhead "Terror Over Lima". None of these three words exist in the book (I checked it from July 1984 till November 1992). After I was sure that the text itself doesn't make a statement at all, I tried to contact Jack Dapid again, but unfortunately he died 92 years in March 1991 in a shooting motivated by jealousy. So this and the reason for the existence of beer with cherry-flavor will remain unsolvable mysteries of mankind.

Jack finishes his book with the well known and often quoted sentences: "After solving all problems and open questions of mankind (besides cherry-flavor beer), Attila decides it is time to shutdown this universe and boot a new one. Last one out, please switch off the time!" I'm sure there are no better last sentences for a book, but to have an open end and at least one self written sentence (I hope, dearest reader, you apologize this little personal comment) I close with: "So what?"

Daniel Dobos
Geneva, 01. 09. 2007

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