



Experimental Methods in Particle Physics (HS 2016)

Electronics, Data Acquisition and Trigger - Systems -

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Overview

- Experimental setup
- Pulse Generators
- Discriminators
- Logic modules
- ADC
- Scalar
- Crates

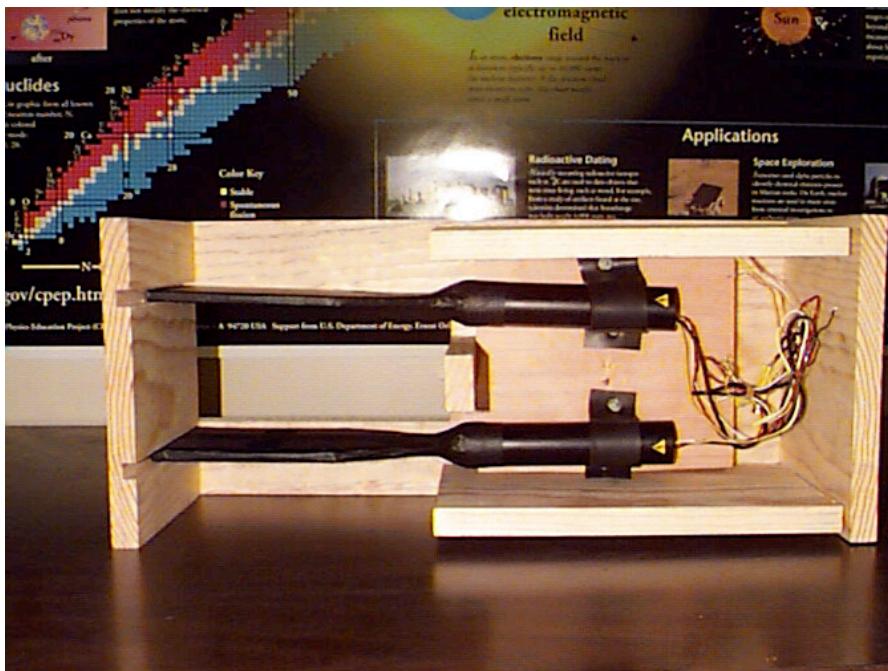
Experimental setup

PMT



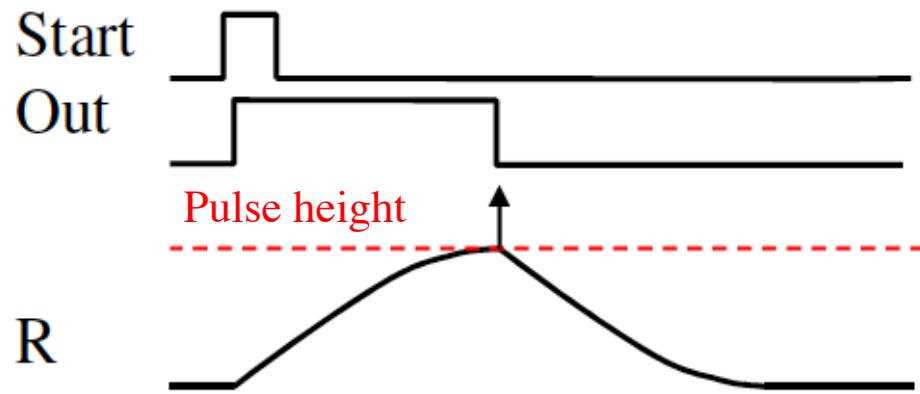
Scintillator

COSMIC RAY TELESCOPE



Pulse Generator

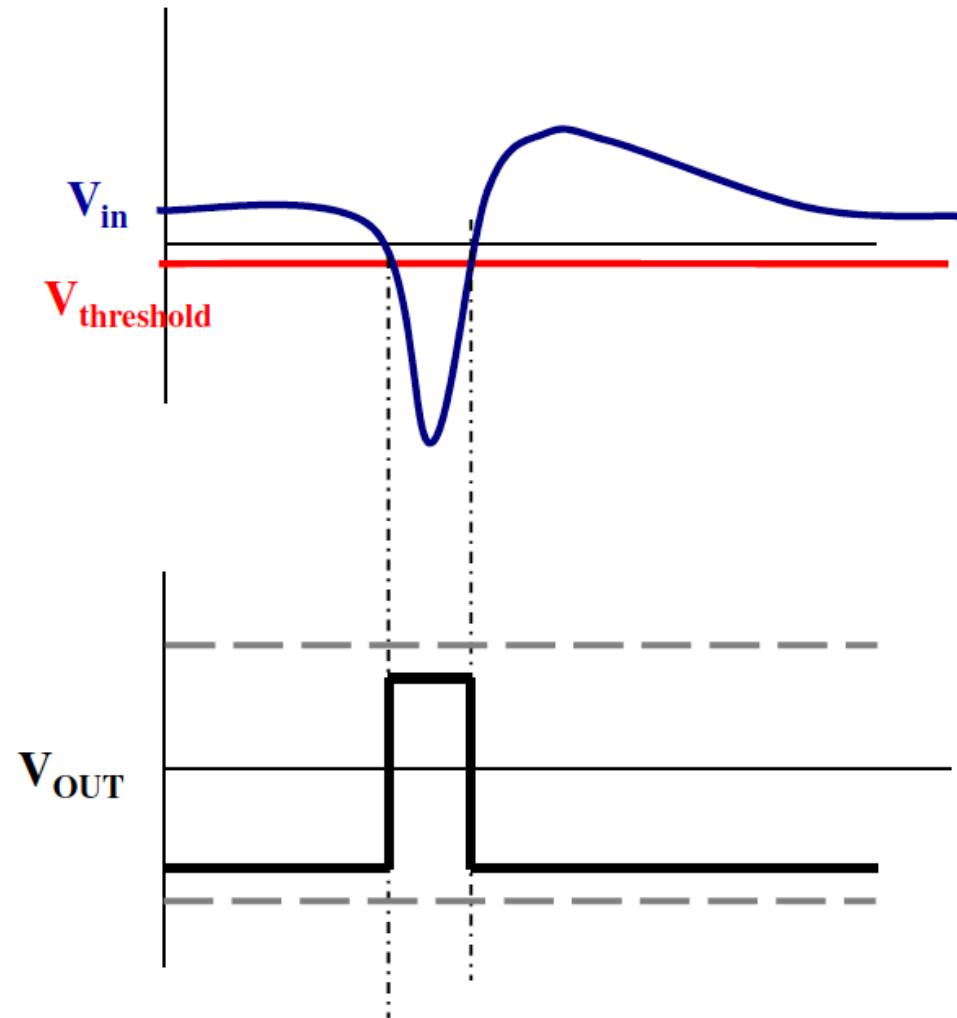
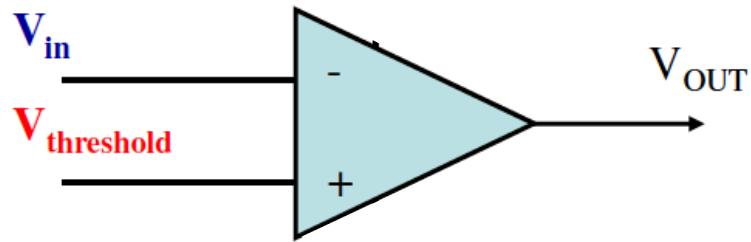
- Generates analog output pulse upon start signal
- Pulse shape (rise time and decay time) can be adjusted with the help of variable resistor



$$T \approx RC$$

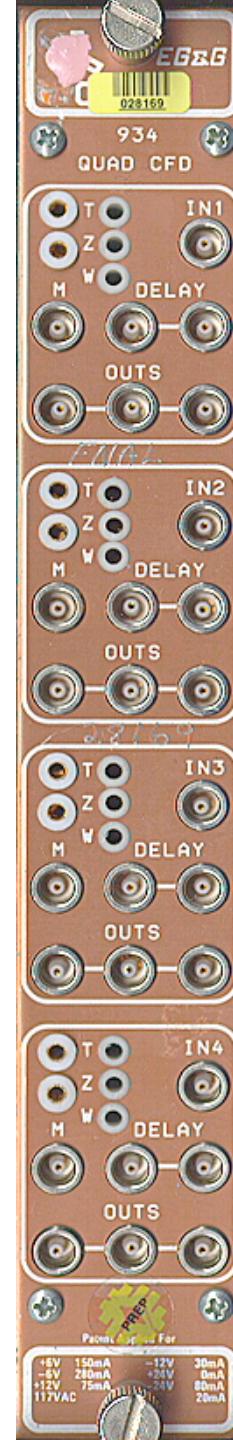


Discriminator

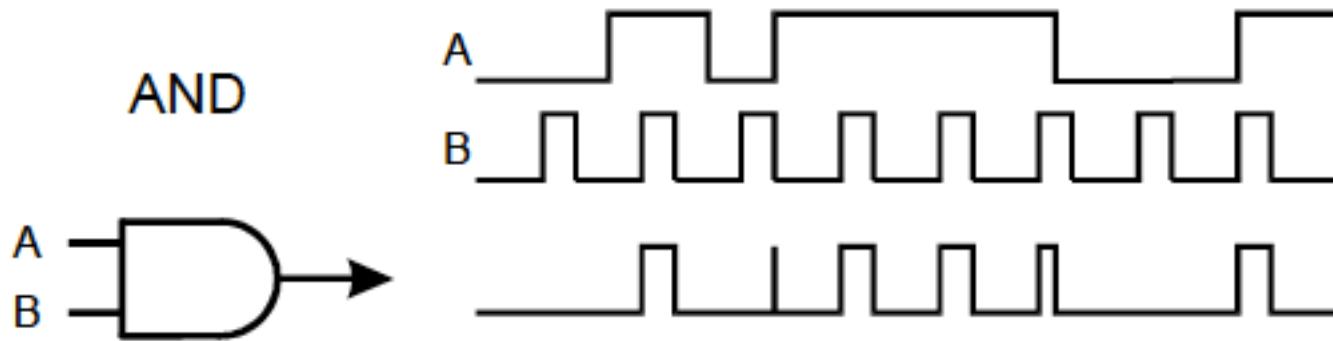


Discriminator module

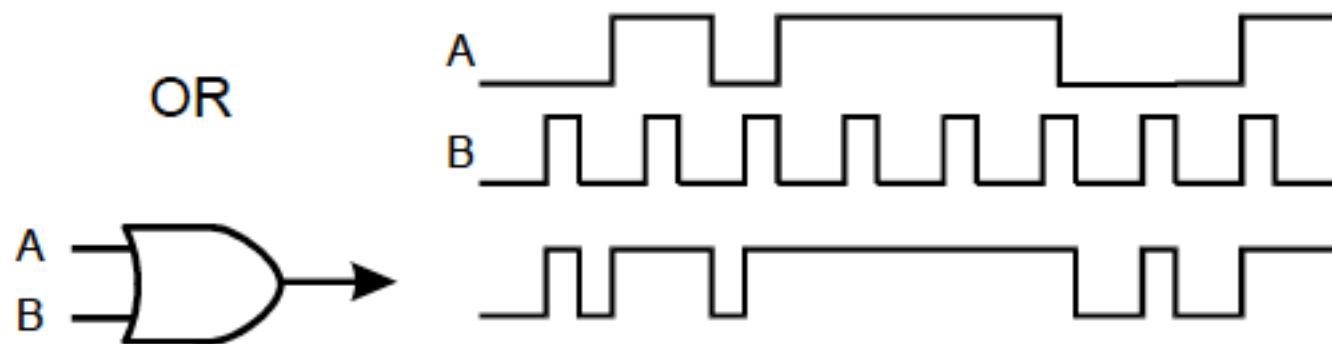
- NIM module with 1 input and 3 simultaneous outputs
- 4 independent units
- Front-panel screwdriver adjustment for threshold (T), time walk (Z) and width (W)
- Characteristics:
 - Speed
 - Input signal range
 - Stability of threshold, delay, width, ...
 - Operating conditions (temperature, radiation hardness, ...)



Logic Functions



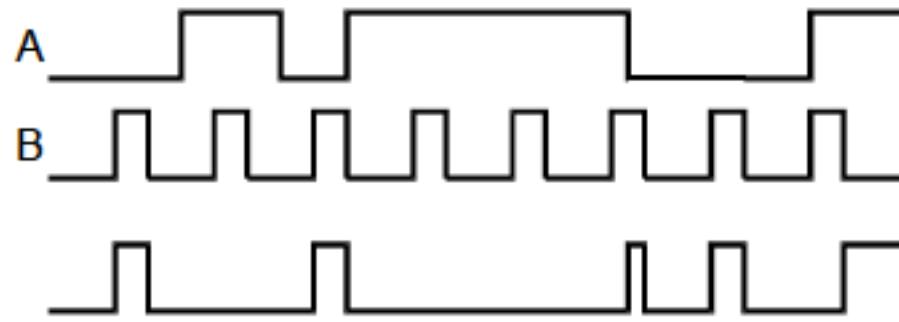
→ AND: Output high, when both inputs are high.



→ OR: Output high, when any input is high.

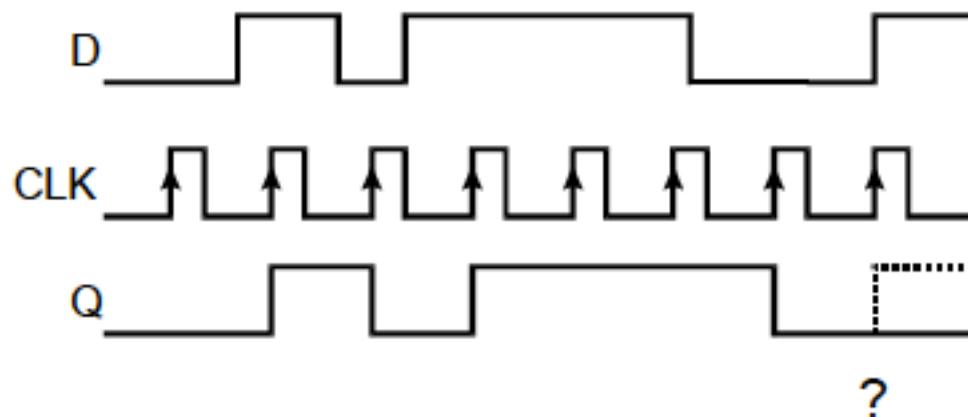
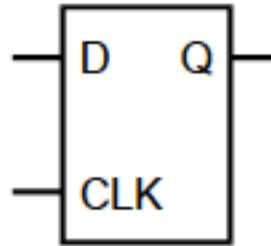
Logic Functions

EXCLUSIVE
OR



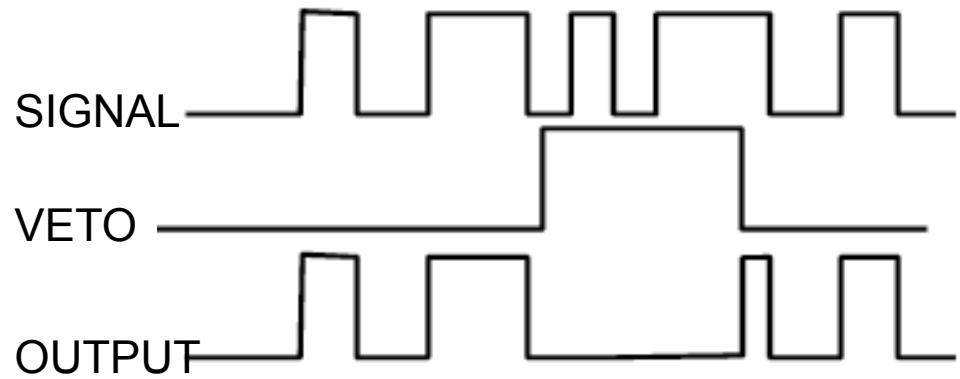
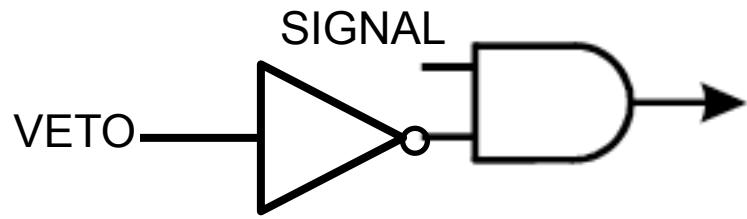
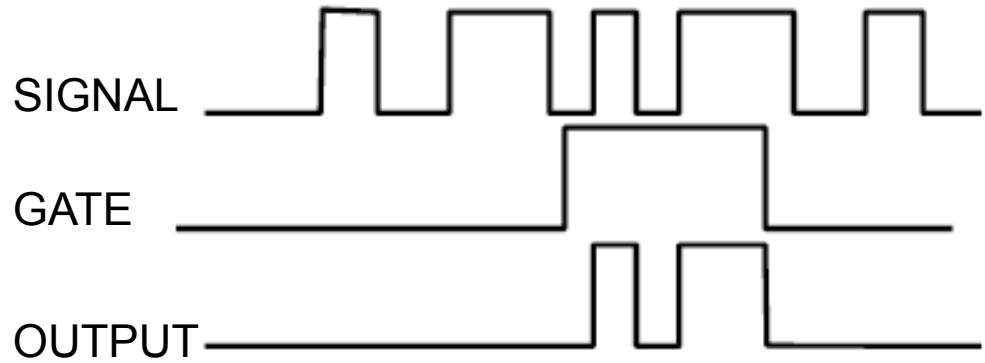
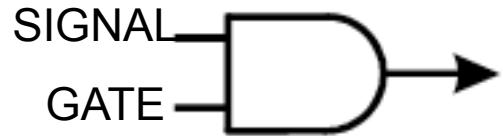
→ EXCLUSIVE OR: Output high, when only one input is high.

D FLIP FLOP
(LATCH)



→ FLIP-FLOP: Level is stored at positive clock transition.
(Ambiguity if data and clock transition simultaneous)

Gate and Veto

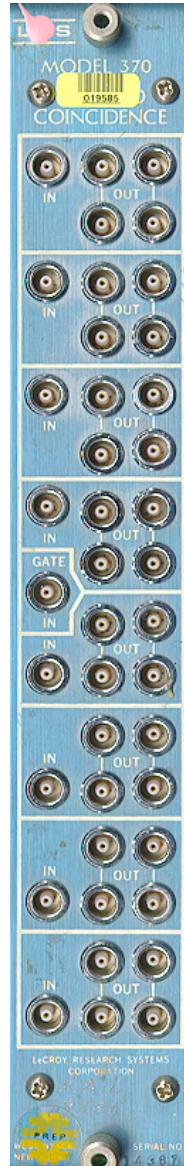


Coincidence modules

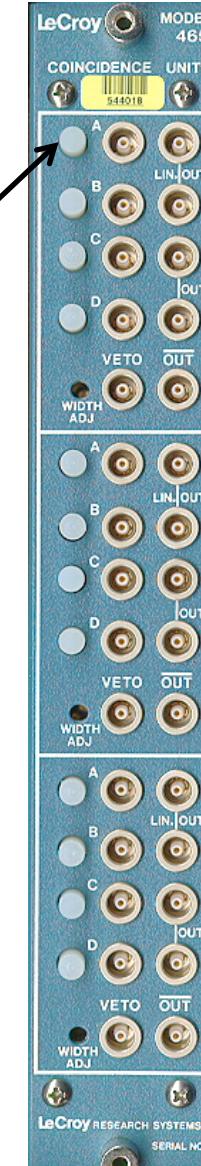
4 independent units with 2 channel coincidence module



8 channel coincidence with common gate

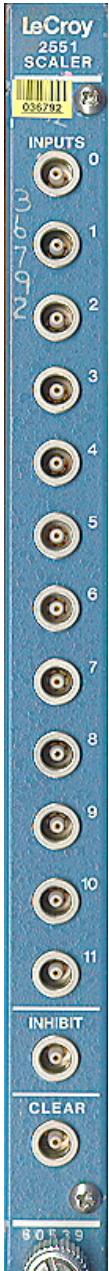


3 independent units with 4 channel coincidence module and veto

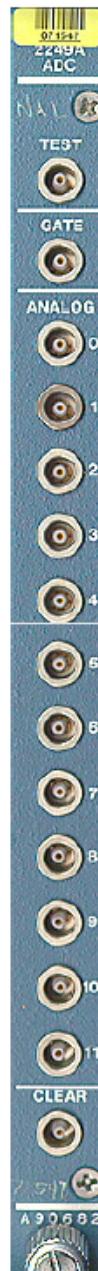


Disable/
enable push
buttons

Scaler and ADC module

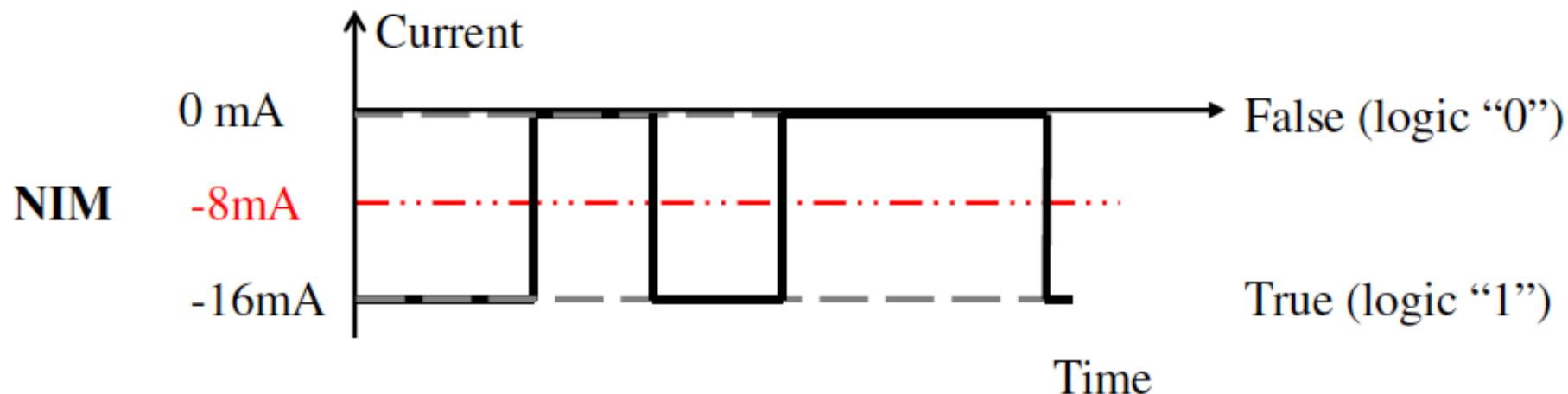
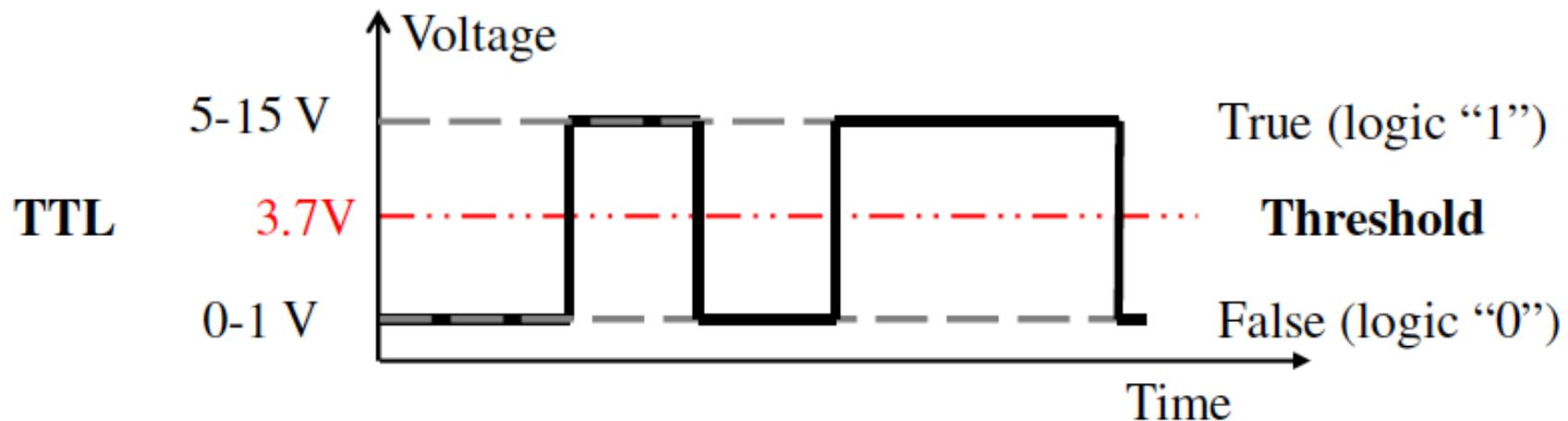


- 12 channel scaler module
- Counts pulse signals on each input
- Common inhibit
- Common reset
- Characteristics:
 - Speed
 - Input signal range
 - Multi-pulse resolution
 - Operating conditions (temperature, radiation hardness, ...)



- 12 channel ADC
- Digitizes analog input
- Common gate
- Common clear
- Common test input (linearly increasing signal)
- Characteristics:
 - Resolution
 - Linearity
 - Conversion time
 - Rate capability
 - Stability
 - Operating conditions (temperature, radiation hardness, ...)

Logic level standards



Logic level standards

NIM-TTL converter



TTL (Voltage)

Advantages:

Low pickup
Directly compatible with common digital Si-IC's

NIM (Current)

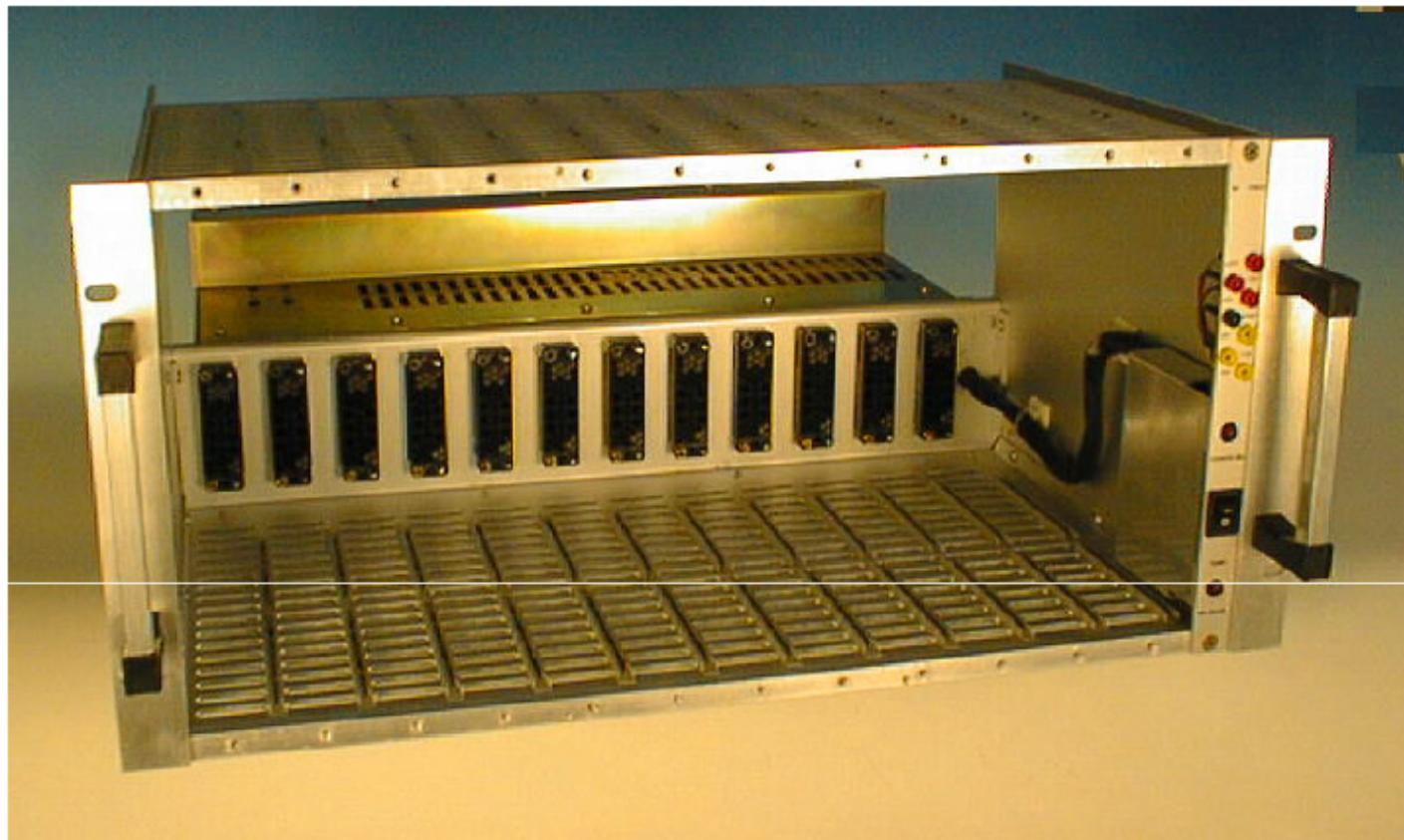
Low crosstalk
Low power dissipation
High speed (~1ns)
Transmission by 50 Ohm lines

Drawbacks:

Low speed (<10ns)
High crosstalk
High power dissipation on 50 Ohm load

Higher pickup
Directly not compatible with common Si-IC's

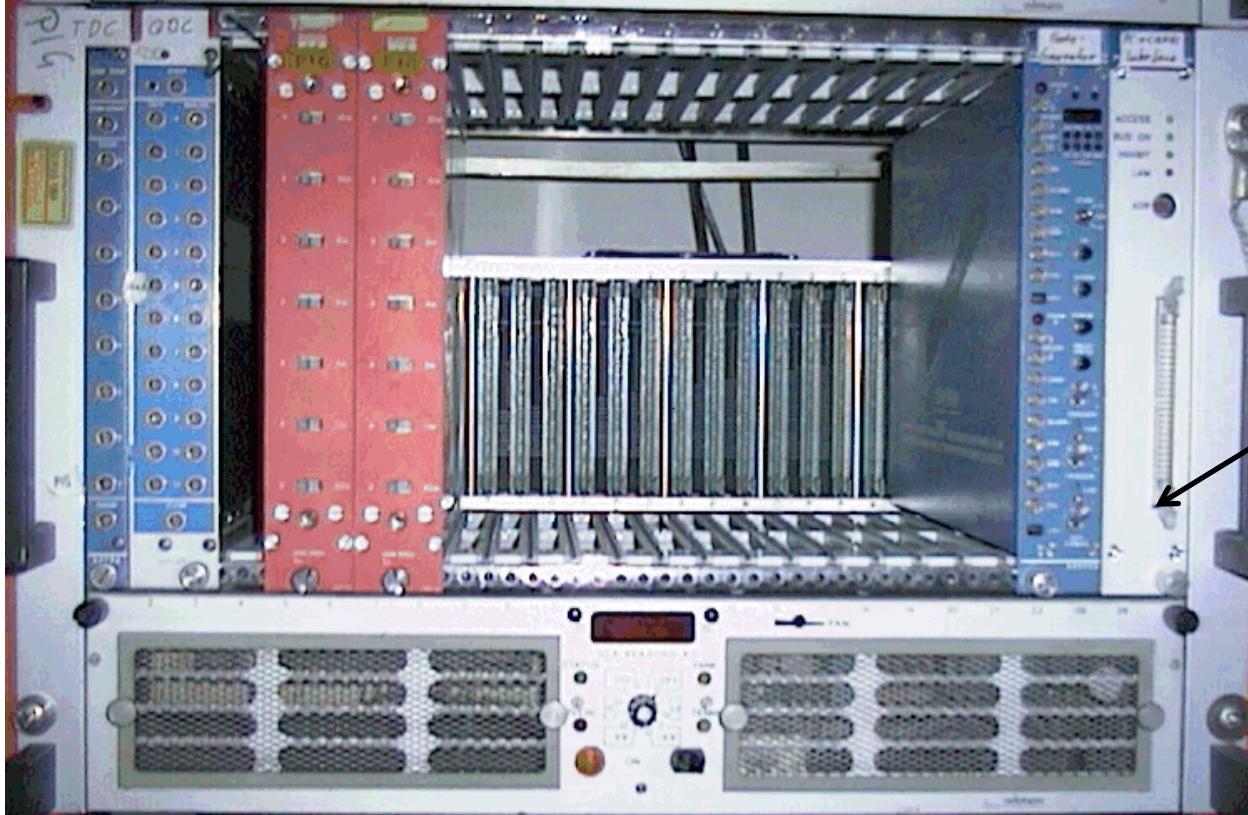
Digital frames (crate): NIM crate



| Pin # | Function | Pin # | Function |
|-------|--------------------|-------|------------------|
| 1 | Reserved [+3 V] | 2 | Reserved [-3 V] |
| 3 | Spare bus | 4 | Reserved bus |
| 5 | Coaxial | 6 | Coaxial |
| 7 | Coaxial | 8 | 200 V DC |
| 9 | Spare | 10 | +6 V |
| 11 | -6 V | 12 | Reserved bus |
| 13 | Spare | 14 | Spare |
| 15 | Reserved | 16 | +12 V |
| 17 | -12 V | 18 | Spare bus |
| 19 | Reserved bus | 20 | Spare |
| 21 | Spare | 22 | Reserved |
| 23 | Reserved | 24 | Reserved |
| 25 | Reserved | 26 | Spare |
| 27 | Spare | 28 | +24 V |
| 29 | -24 V | 30 | Spare bus |
| 31 | Spare | 32 | Spare |
| 33 | 117 V AC (hot) | 34 | Power return Gnd |
| 35 | Reset (scaler) | 36 | Gate |
| 37 | Reset (aux) | 38 | Coaxial |
| 39 | Coaxial | 40 | Coaxial |
| 41 | 117 V AC (neutral) | 42 | High-quality Gnd |
| G | Gnd guide pin | | |

- Houses a number of NIM modules
- Backplane connectors follow NIM standard
- No common data bus
- $\pm 6V$, $\pm 12V$, $\pm 24V$, 200V
- Common RESET and GATE

CAMAC crate



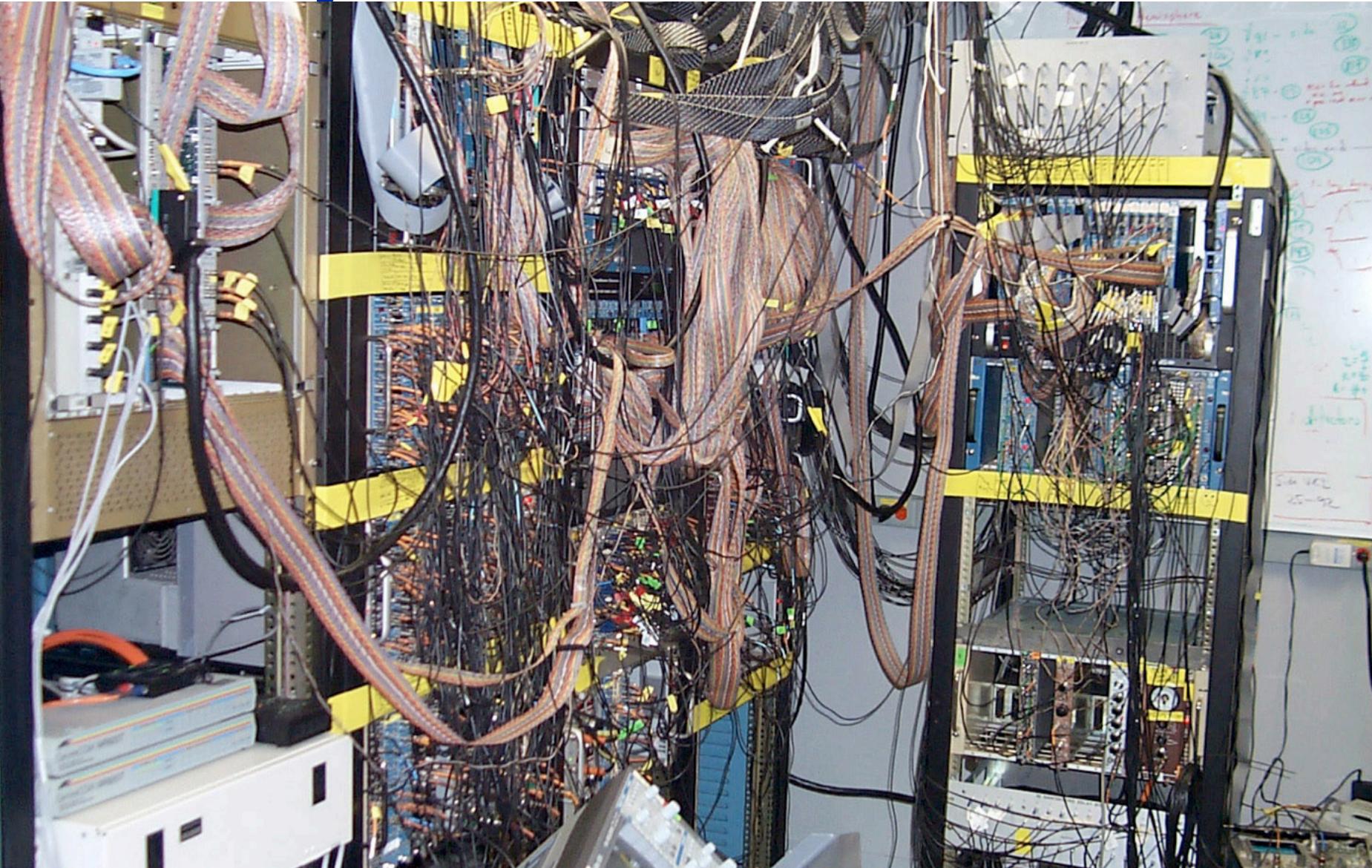
25 slots
Crate controller
in slot 25

Crate controller:
Interface to PC

- Programming of modules
- Readout data from modules

- CAMAC: Computer controlled electronics
- Common data bus on backplane
- Data bandwidth up to 1 megaword/sec (1 word is 16 or 24 bits)
- Relatively slow data acquisition and processing

CAMAC System



VME crate



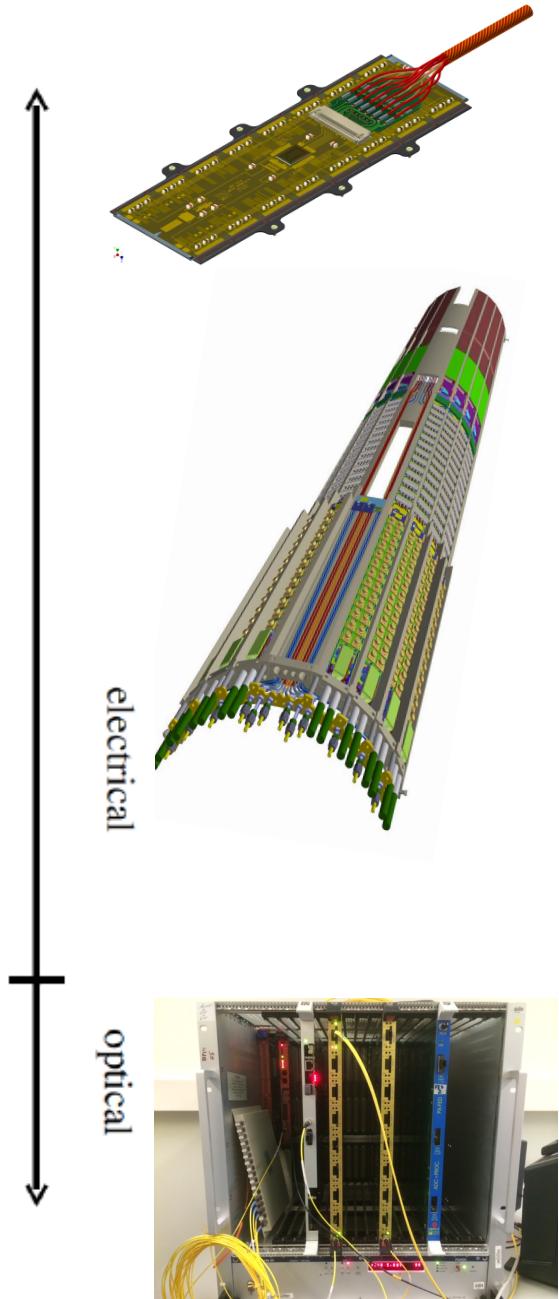
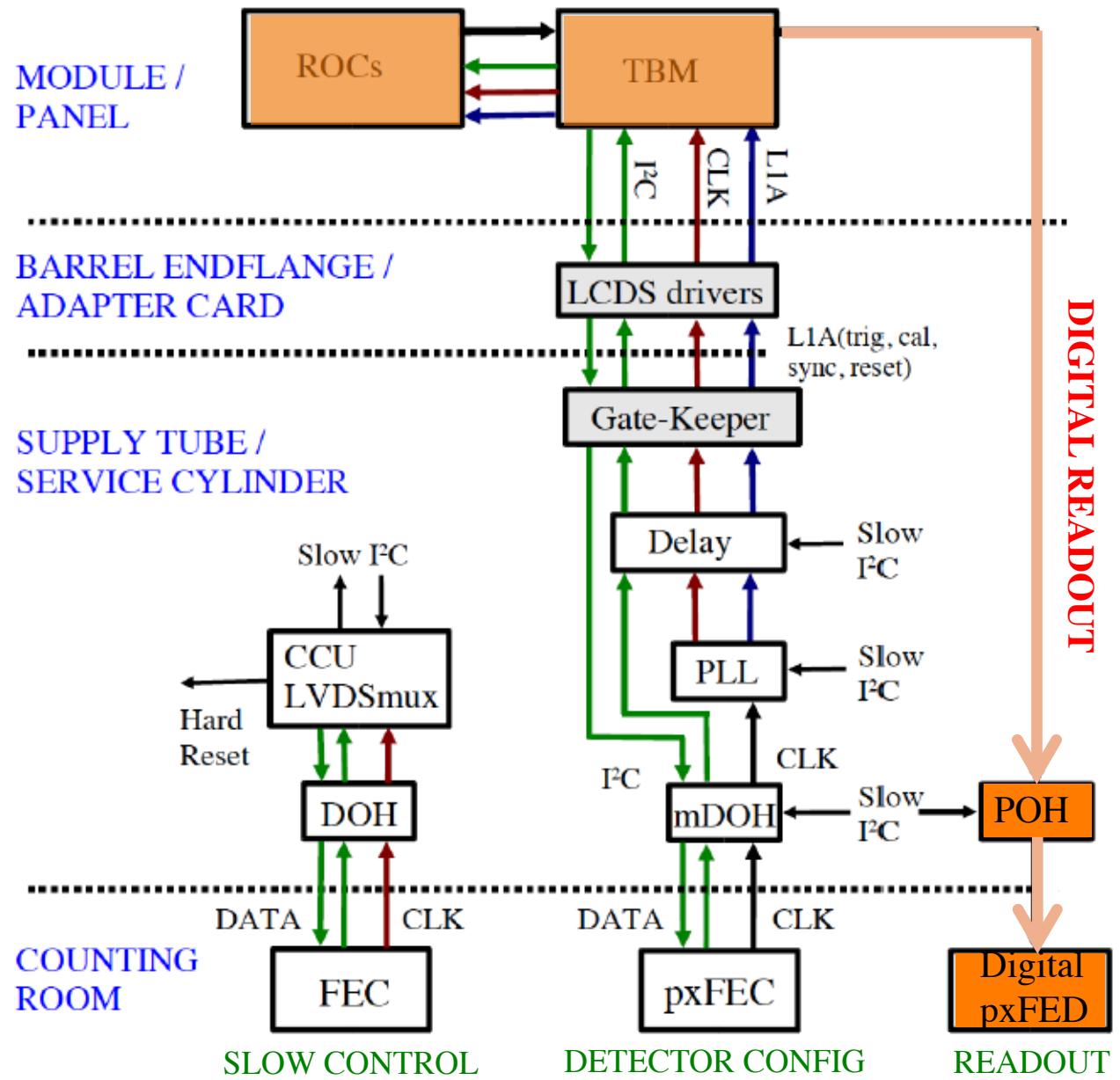
- Different numbers of slots, crate controller can be in any slot
- Common backplane with DATA BUS and ADDRESS BUS
- Data bandwidth up to 40 MB/sec
- $\pm 6V$, $\pm 12V$, $\pm 24V$
- Fast data acquisition and processing
- Can be controlled by internal or external CPU

CMS pixel VME crate

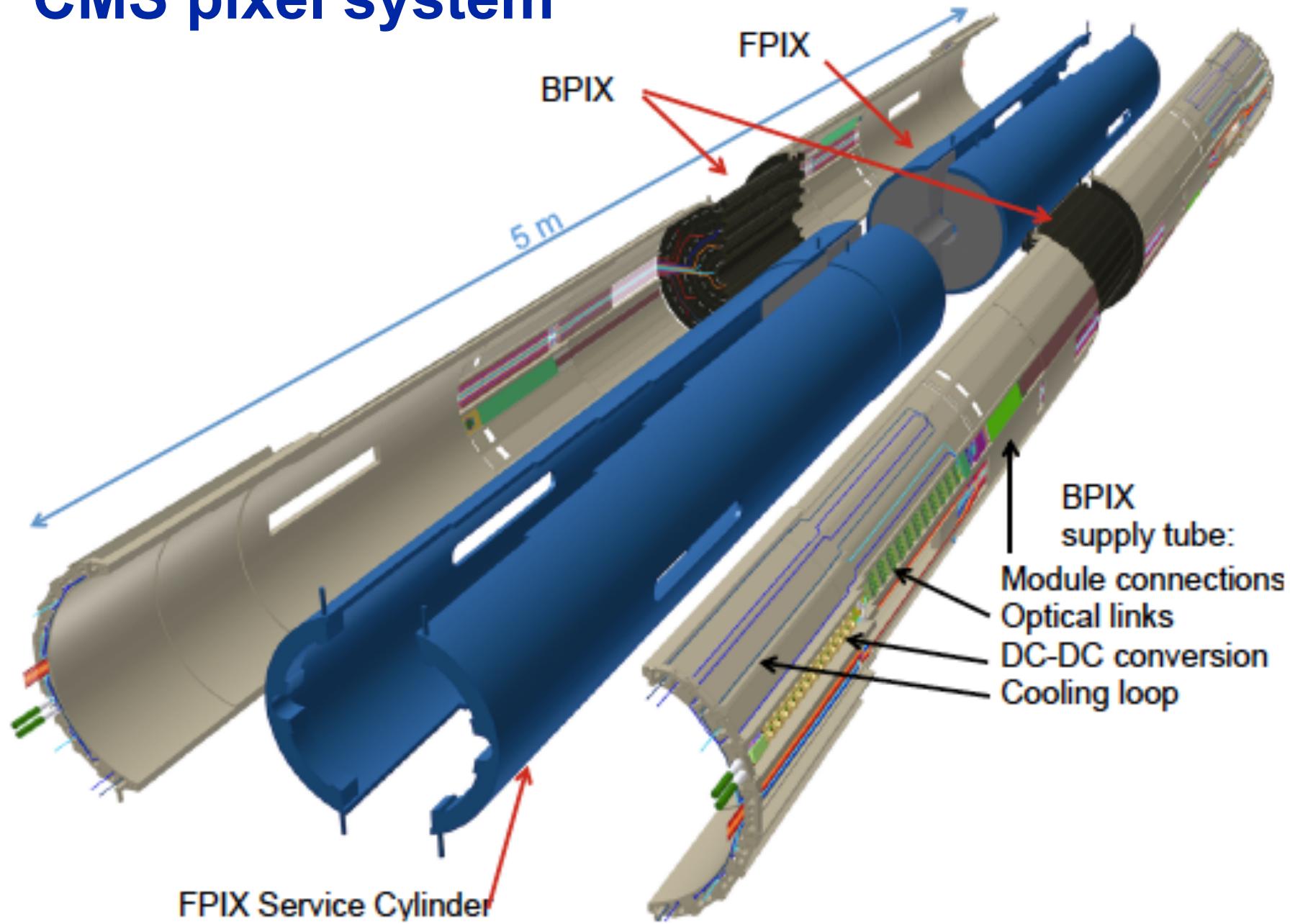
Crate controller Trigger and FED (DAQ) FEC (controller) FED (DAQ)



CMS pixel readout and control



CMS pixel system



Summary

- Topics covered
 - Analog data processing
 - Digitization
 - Basic trigger concepts
 - Multi-level trigger system at CMS
 - Components to build DAQ systems in the lab
- Lecture notes posted here
 - <http://www.physik.uzh.ch/lectures/empp/>