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Timing adjustment of the IBL and Pixel Detectors for the LHC Run 2

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Abstract

Timing commissioning of the Pixel and IBL detectors are summarized in this report. The contents include the latency change of the Pixel L1A from Run1 to Run2 reflecting the replacement of the Pixel services to nSQP and optical ribbons, initial commissioning of timing adjustment using cosmic rays, relative timing adjustment of FE-I4 chips sharing the same Tx link, and final timing adjustment using collision beams and performances.

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42 1. Introduction

43 The clock phase and the Level-1 Accept (L1A) signal have to arrive at each individual module of the Pixel
 44 [1–3] and IBL [4] detector with optimal delay size determined by the latency configuration of the front-
 45 end module, so that the in-time efficiency of hits originating from charged particles from proton-proton
 46 collisions is maximized within a limited readout timing window. For the Pixel and IBL detector the size of
 47 readout window is restricted to a 25 ns bunch crossing (1 BC), i.e., the minimal possible window size. The
 48 propagation time of the clock and the L1A signal from the ATLAS Central Trigger Processor (CTP) [5] is
 49 different by modules reflecting the different latencies of signal path lengths (cables), module-by-module
 50 dispersion of latency, etc. Adjustment of timing is made with inserting appropriate size of delays in the
 51 middle of the latency chain.

52 Ultimately the calibration source of the timing is particles flying from proton-proton collision themselves.
 53 Optimizing the hit efficiency *in-situ* gives the most reliable way of timing adjustment including the tiny
 54 timing difference of each module due to the time-of-flight (ToF) of particles. Determination of the optimal
 55 timing for each module is made by sweeping the delay of the entire detector coherently during a special
 56 proton-proton collision run which has isolated bunches, denoted as the *timing scan*. Such a change
 57 of data-taking configuration is not allowed to do in the nominal physics runs, hence the opportunities to
 58 perform timing scans are limited typically at the beginning of the physics run period or commissioning runs
 59 where other detectors would also have other commissioning menus. The timing scan and its consequent
 60 adjustment is the last step of the timing commissioning.

61 In order to minimize the range to be scanned in the timing scan, it is required to set a pre-adjustment of
 62 the latency so that the timing dispersion is squeezed within approximately 1 BC. The adjustment is made
 63 with using cosmic-ray data. Since cosmic rays randomly arrive at the detector with respect to the phase of
 64 the clock, the intrinsic timing dispersion of cosmic rays as a timing calibration source is about 10 ns. The
 65 adjustment of the latency with cosmic rays is meaningful only to align the timing dispersion of modules
 66 to a level of 1 BC.

67 For Run 2, the full-scale timing adjustment of both the Pixel and IBL detectors had to be made; for the
 68 Pixel the refurbishment of the optical ribbons as well as the Pixel service panels (nSQPs) [6] changed the
 69 latency. Needless to say, the IBL is a new detector from Run 2.

70 The timing commissioning of the IBL was not very straightforward as was originally planned. In particular,
 71 it was found that the timing adjustment was necessary to be made inside the module, i.e. relative adjustment
 72 of the latency between the two FE-I4 chips sharing the same Tx optical link. The latency of the FE-I4 chip
 73 can be adjusted with changing a front-end configuration parameter called *DisVbn* [7]. Since changing
 74 *DisVbn* affects to the calibration of the front-end (threshold and ToT tunings), the *DisVbn* adjustment has
 75 to be made before the full calibration of the IBL.

76 This note provides an overall description of the timing adjustment of Pixel and IBL in the Long Shutdown-1
 77 and at the beginning of the Run 2, as a sequel of the Run 1 study summarised in Ref. [8, 9]. Section 2 reports
 78 the preparatory studies of cable latency estimation. Section 3 reports about the timing commissioning
 79 using cosmic-ray data. Section 4 describes about the timing scan using collision beams, the *DisVbn*
 80 tuning, and the timing performance for 25 ns bunch space collisions. Section 5 summarizes the current
 81 status, open issues, and the future outlook.

82 2. Latency estimation

83 2.1. Optical ribbon length measurement

84 The optical ribbon connecting the BOC and the optoboard is the largest change of the latency of the Pixel
 85 detector from Run1. In order to confirm the data sheet of the optical ribbons is consistent, a sampling
 86 optical fiber length test was performed using an OTDR¹. Table 1 shows the result. For Pixel the measured
 87 length of the sampled cables is about 1 m longer than the quoted length. For IBL the measured length
 88 is about 5 m longer than the quoted length. In the following commissioning the measured values were
 89 referred.

Category	Fiber ID	Design Length [m]	Measured Length [m]	Diff (design – measured) [m]	Diff Average [m]
Pixel	2100007.2	70	71.08 ± 0.30	1.08 ± 0.30	0.93
	2100007.8	70	70.76 ± 0.30	0.76 ± 0.30	
	2100006.2	70	70.92 ± 0.30	0.92 ± 0.30	
	2100006.8	70	70.85 ± 0.30	0.85 ± 0.30	
	2100032.4	91	92.03 ± 0.30	1.03 ± 0.30	
IBL	2149208.1	80	85.04 ± 0.30	5.04 ± 0.30	5.32
	2149213.7	80	86.59 ± 0.30	5.59 ± 0.30	

Table 1: Result of the optical link length measurement with the OTDR.

90 2.2. Estimation of the total cable latency

91 There are additional latencies coming from cabling between the BOC and modules, and the inclusive sum
 92 of each module's latency of signal propagation was estimated. For Pixel, the following contributions were
 93 considered:

- 94 • Optical ribbon
- 95 • ER bundle
- 96 • Cable from the end of the ER bundle to the PP0
- 97 • Type0 cable

98 For IBL, the following contributions were considered:

- 99 • Optical ribbon
- 100 • Type1 bundle
- 101 • I-flex cable
- 102 • Type0 cable and Stave-Flex

103 Figure 1 shows the distribution of the estimated cable latency for Pixel (Run1), Pixel (Run2), and for IBL.
 104 The Pixel modules are grouped into two reflecting the optical ribbon length of 71 m and 92 m. The 71 m
 105 group has shorter latency than the Run1 case, and the 92 m group is more than 4 BC (100 ns) delayed than
 106 the 71 m group. The IBL modules, which has 85 m of the optical ribbons, are sitting at the middle of the
 107 two groups. The dispersion of the IBL timing is expected to have much simpler than the Pixel reflecting
 108 the simplified service structure compared to the Pixel.

¹ Optical Time Domain Reflectometer

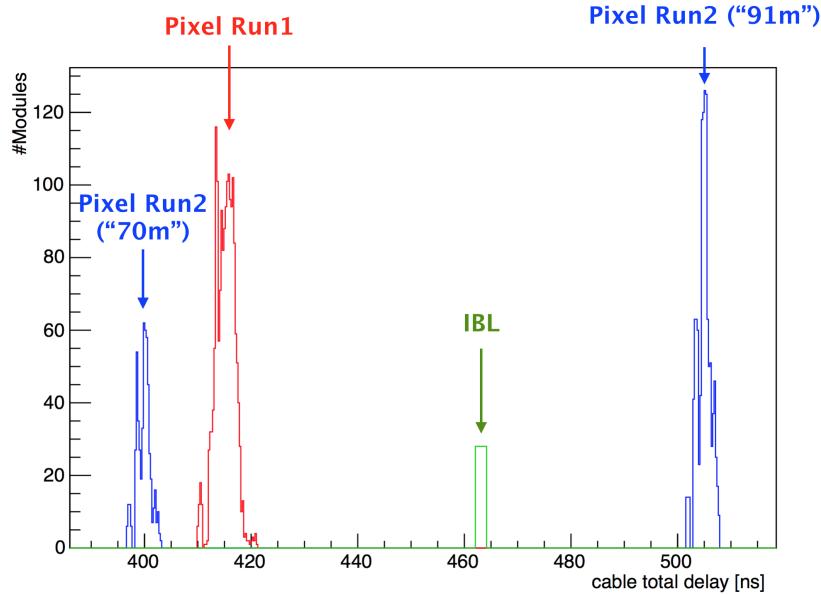


Figure 1: Distribution of the estimated latency of physical cables between BOC and the front-end.

¹⁰⁹ 3. Timing with cosmics rays

¹¹⁰ 3.1. Milestone runs

¹¹¹ The cosmic commissioning campaigns during LS-1 are called milestone runs/weeks (M-weeks). The
¹¹² Pixel and IBL started to join M-weeks from M5. Table 2 summarizes the activities from M5 and M9.

¹¹³ 3.2. Pixel: Initial comic ray hits finding

¹¹⁴ Cosmic ray data were collected during the initial phase of the Run2 commissioning in so-called milestone
¹¹⁵ weeks (M-Weeks). The first cosmic hit candidates were found in M6 runs firstly in Pixel and later in IBL
¹¹⁶ as well. In run 242147 and 242148 (zero B-field runs), the timing configuration of the Run1 was used so
¹¹⁷ that it is possible to confirm the split of the cable length group between 71 m and 92 m. The data was
¹¹⁸ reconstructed into tracking validation xAODs.

¹¹⁹ Since the detector alignment was not properly made after re-installation of the Pixel, the cosmic hit
¹²⁰ candidates were selected among the list of the Pixel clusters with requiring the distance to the cosmic
¹²¹ ray track to be less than 2 mm. For IBL, the Geant4 geometry was incorrect in terms of the global
¹²² rotation of the staves around the beam axis, therefore the identification of the IBL cosmic ray hits was
¹²³ not straightforward². Existence of on-track hit candidates was confirmed by drawing hand-made event

² In the M6 runs only 9 staves out of 14 joined the ATLAS data taking. It was firstly realized the reconstructed hit *xy*-map was incorrect by corresponding the staves which were included in the run to the geometry. The incorrectness of the geometry (not the incorrectness of the connectivity) was finally confirmed with finding out that the global IBL package was rotated around the beam axis by 19.6 degrees by hand, the distance of the hits to the reconstructed tracks creates a narrow peak which proves the consistency of having the cosmic tracks.

Milestone	Duration	Commissioning achievements	Data amount [hours]	Readout Window [BC]
M5	Sep 8 - Sep 12, 2014	Pixel (full package) and IBL (1 stave) joined ATLAS data taking.	-	15
M6	Oct 13 - Oct 18, 2014	Pixel (full package) and IBL (9 staves) joined ATLAS data taking. / First observation of cosmic ray hits on tracks both for Pixel and IBL (IBL hits were observed after finding geometry mistake of the stave positions). /Confirmation of the Pixel cable groups of 71 m and 92 m.	~ 8	15
pre-M7	Nov 17 - Nov 19	ID-combined runs. Application of rough adjustment to Pixel to compensate cable length.	~ 16	8
M7	Nov 24 - Dec 8, 2014	Illumination of all Pixel and IBL modules with $O(100)$ cosmic rays. Observation of average L1A for each module granularity.	~ 110	5
M8	Feb 9 - Feb 15, 2015	First data taking of DBM.	$O(100)$	5
M9	Mar 8 - Mar 25, 2015	Largest statistics.	$O(200)$	5

Table 2: Summary of M-week activities, achievements, cosmic-ray data amount, and the width of the readout window during the data taking.

¹²⁴ displays as shown in Figure 2.

¹²⁵ Figure 3(a) shows the distribution of Pixel clusters as a function of the distance to the track. The blue
¹²⁶ histogram indicates all clusters around the reconstructed tracks, and the red histogram represents the
¹²⁷ on-track clusters reconstructed by the tracking algorithm. With manually calculating the distance to the
¹²⁸ track of clusters regardless they are on-track or not, it is possible to collect candidate clusters with better
¹²⁹ efficiency.

¹³⁰ Figure 3(b) shows the cluster timing distribution with using the above analysis. A couple of peaks which
¹³¹ are distant about 4 BC is clearly seen. This confirms that the Pixel detector has two groups of cable lengths
¹³² of 71 m and 92 m as described in the previous section: the peak at (`TriggerDelay + L1A`) \sim 137 BC
¹³³ corresponds to the 92 m group, and the other peak at (`TriggerDelay + L1A`) \sim 141 BC corresponds to the
¹³⁴ 71 m group.

¹³⁵ With using this data, a validation of the cable length map was made.

¹³⁶ 3.3. Timing adjustment at TTCrx's

¹³⁷ The latency alignment was two folded: one is the adjustment at TTCrx's, and the other is the alignment at
¹³⁸ the front-ends. In November 2014, the delays at the TTCrx was modified so that the latency is all aligned
¹³⁹ at the TTCrx for the Pixel crates. Table 3 shows the TTCrx default configuration after this adjustment.
¹⁴⁰ It was confirmed with a scope on February 2015 that with these setting the latency is perfectly aligned
¹⁴¹ between TIMs.

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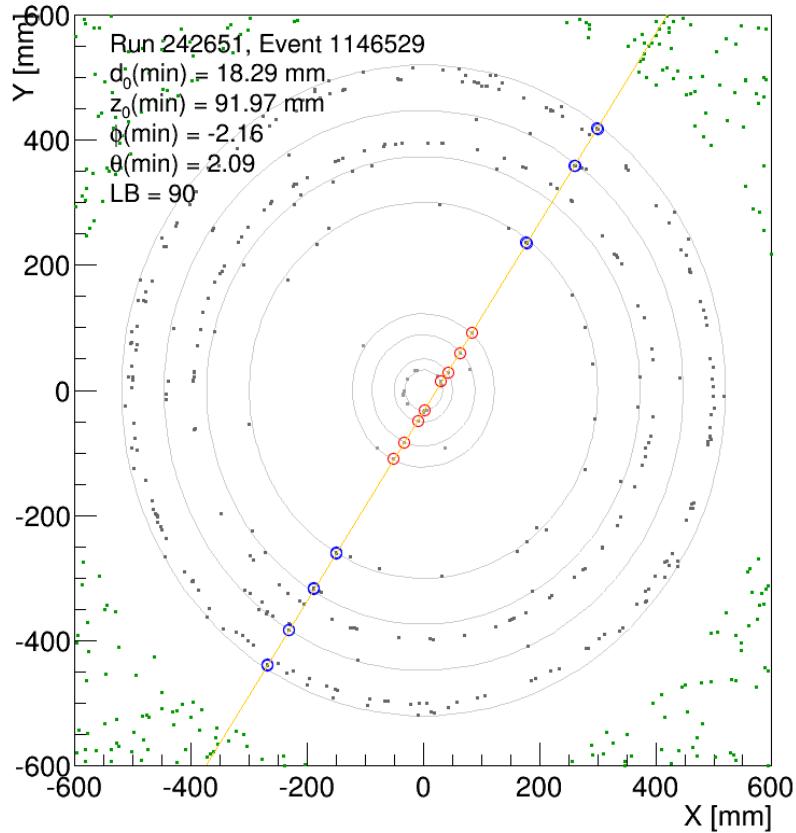


Figure 2: An event display of one of firstly found cosmic hit candidates on the Pixel layers and on the IBL. The IBL hits are manually rotated around the beam axis by 19.6 degrees.

TIM	TTCrxCoarse	TTCrxFine [ns]	Total [ns]
TIM_B1	2	23.2	73.2
TIM_B2	2	21.4	71.4
TIM_B3	2	17.0	67.0
TIM_D1	2	10.6	60.6
TIM_D2	2	8.8	58.8
TIM_L1	1	24.0	49.0
TIM_L2	1	23.0	48.0
TIM_L3	2	3.2	53.2
TIM_L4	2	0.8	50.8
(TIM_I1)	2	0.4	50.4

Table 3: Delays applied to each TTCrx in November 2014.

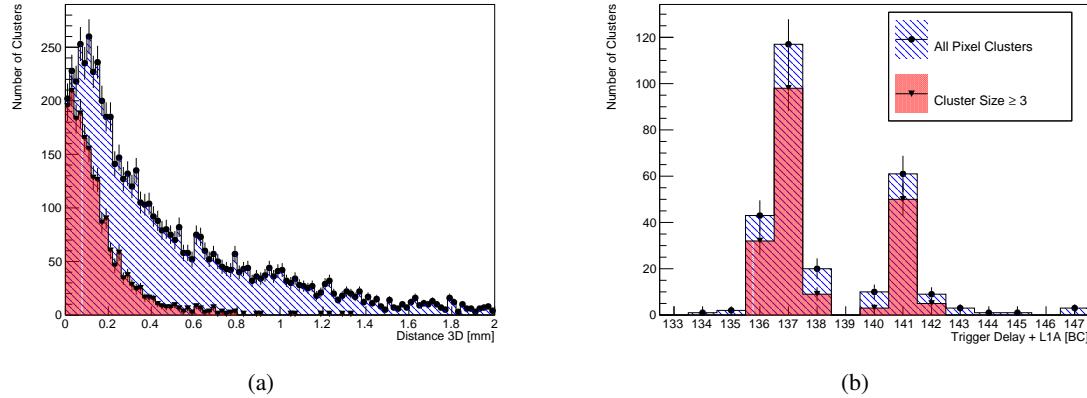


Figure 3: (a) Distribution of distance of Pixel hits to tracks in M6 runs. The blue histogram shows all Pixel hits, while the red histogram shows the hits associated on tracks by the reconstruction. (b) The timing distribution of the Pixel modules in M6 runs. The split two peaks correspond to the two different cable length groups of 71 m (the right peak) and 92 m (the left peak), respectively.

3.4. Pixel: Pre-adjustment of BOC delays

The first BOC delay adjustment made to the Pixel was the alignment of the 71 m cable group and 92 m cable group modules. With referring the cable latency map shown in Figure 1, the rough adjustment, denoted as *pre-adjustment* in this note, was applied. The target latency of the sum of the cable delay plus the BOC delay tunes was targeted at 515 ns.

The initial attempt of the pre-adjustment which was applied during M6 had problems in listing-up all modules, and had modules which were not applied the expected adjustment values. Later before pre-M7, the debugged pre-adjustment was applied. As shown in Figure 4 and 5, with this pre-adjustment the timing dispersion by modules was sufficiently controlled within ~ 1 BC, and this configuration for the Pixel was used until the timing scan.

3.5. IBL: commissioning of BOC

The M7 data taking was long enough to illuminate all modules with $O(100)$ cosmic ray hits. Therefore by-module granularity timing was studied.

For the IBL, the intrinsic latency dispersion originating from cable path length difference is considered to be much smaller than the Pixel (see Figure 1). However, as shown in Figure 4 and 5, the observed dispersion size was sizable. At this moment the feature of the front-end dependent latency related to the discriminator bias current (DisVbn) was not aware of, and the origin of having such large dispersion was unknown.

Towards M8, the coarse timing adjustment of the IBL was prepared and applied expecting that this dispersion would be compensated. The result of M8 runs exhibited the dispersion of the IBL by-module latency with the same order.

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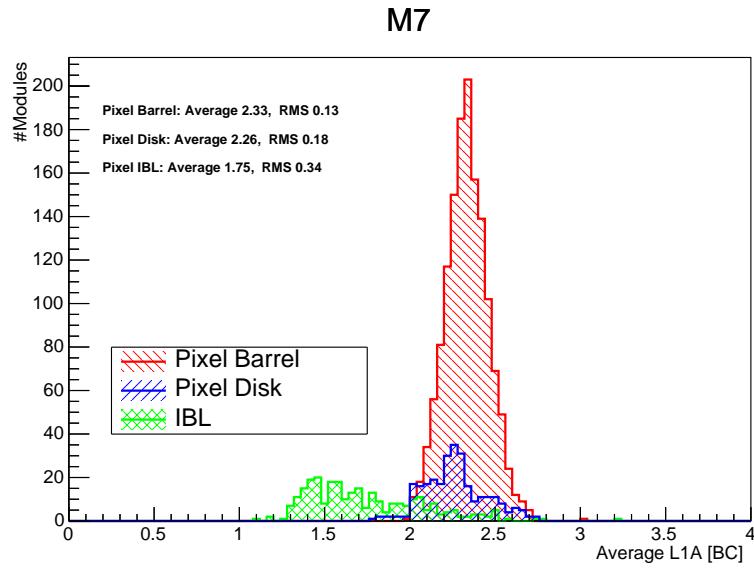


Figure 4: Distribution of the average timing for each module for clusters on tracks of cosmic-rays during commissioning runs in December 2015 (M7 runs). Modules are classified into Pixel Barrel, Pixel Disk, and the IBL. For the Pixel the pre-adjustment was applied, while for the IBL no by-module correction delays were applied.

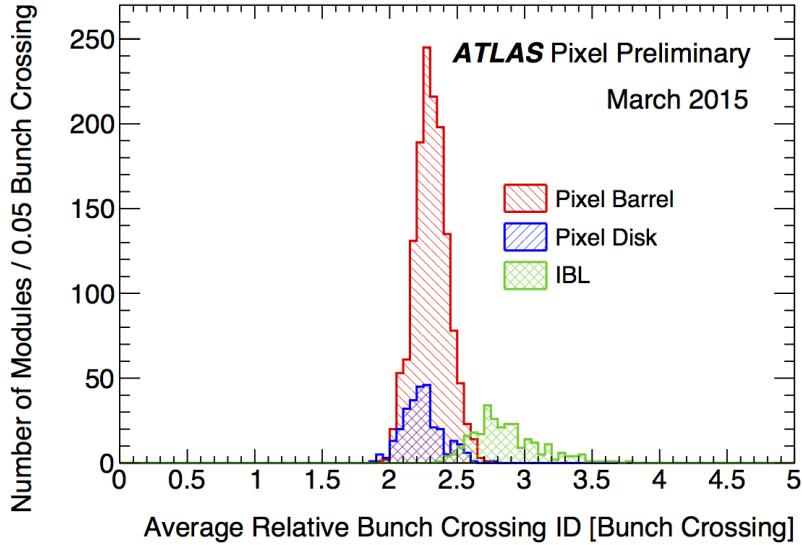


Figure 5: Distribution of the average timing for each module for clusters on tracks of cosmic-rays during commissioning runs in March 2015 (M9 runs). Modules are classified into Pixel Barrel, Pixel Disk, and the IBL. The target of the adjustment in this phase was to squeeze the module-by-module dispersion in 1 BC (25 ns) towards the upcoming timing scan with collision beams. The relatively-shifted peak position of the IBL distribution compared to Figure 4 is because of artificially decreasing the trigger delay by 1 BC with respect to the M7 data taking. The public plot is available in Ref. [10].

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163 Further investigations clarified another feature; there was a significant timing gap between the C-side and
 164 the A-side half staves. This problem was sourced to the function to divide the global 25 ns clock into 6.25
 165 ns internally in the BOC, and that the phase of this clock division had random ambiguity, and each half
 166 stave corresponding to one independent logic block of the BOC could have a phase gap of multiple of 0.25
 167 BC. Such a feature is seen in Figure 6, that each half-stave has a discrete phase of multiple of 0.25 BC that
 168 the average L1A data prefers to fit. This problem was sorted out before M9 by updating the firmware.

169 After this fix, the latency has become fully deterministic. Still the timing dispersion of the IBL in M9
 170 runs was sizable. The cause of this was not clarified until performing the timing scan described in the
 171 next section.

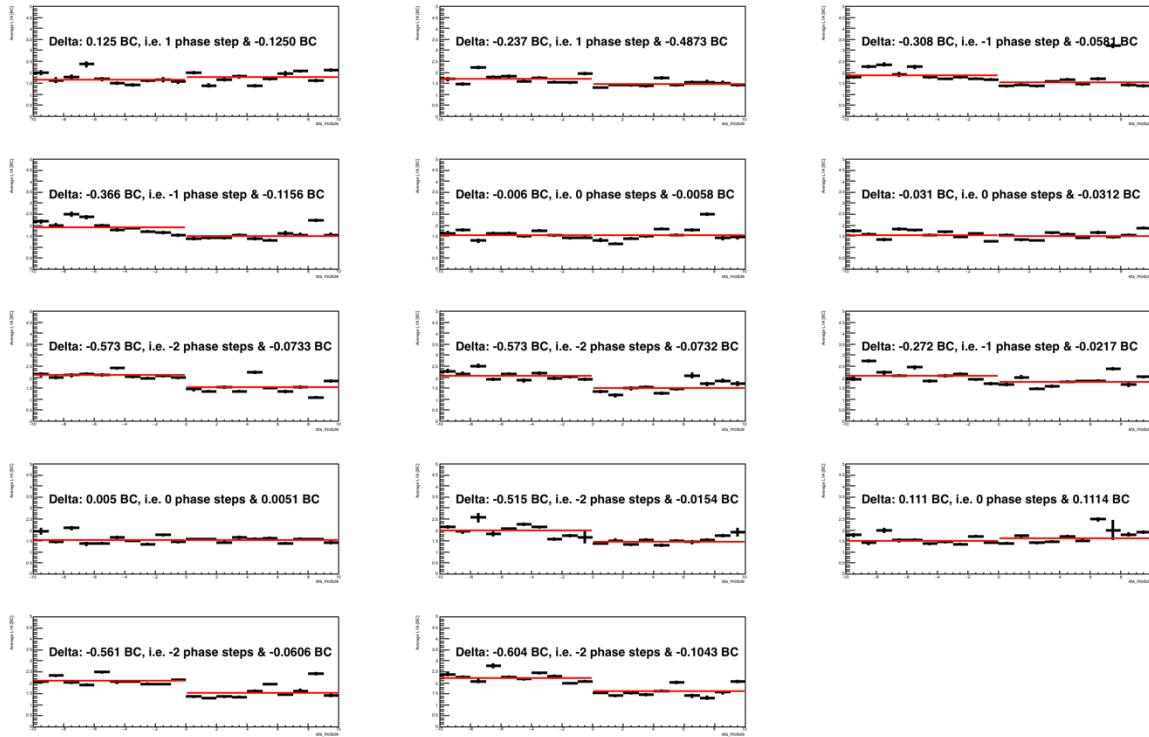


Figure 6: Module-by-module average L1A for each stave of the IBL.

172 4. Timing Scan with collision data

173 4.1. Timing Scan in May with the commissioning collision

174 The timing scan is performed by changing the TTCrx coarse and fine delays during collision data taking.
 175 The in-time efficiency is measured as a function of scan delay step, and the optimal delay size is determined
 176 for each module. For Run-2, three timing scans took place by October 2015. The first scan (run 264034,
 177 May 6) was performed only for the Pixel. The Pixel Detector's final timing adjustment was obtained using
 178 this run. The second scan (run 265573, May 21) was performed mainly for IBL, and by the analysis of this
 179 scan, it was clarified that the problem for the IBL of the timing gap between the paired front-ends sharing
 180 the same Tx line. After sorting-out this issue, the third timing scan (run 270441, July 5) was performed
 181 to establish the timing adjustment for IBL. Table 4 summarizes the list of scans and its configurations.

Run	Date	\sqrt{s}	Scan Range [ns]	Scan step [ns]	Duration/point [LB]	Comment
264034	May 6, 2015	900 GeV	25	1	2	for Pixel only
265573	May 21, 2015	13 TeV	45	1	2	mainly for IBL
270441	Jul 5, 2015	13 TeV	40	2	2	after DisVbn tuning

Table 4: List of the timing scan runs at the beginning of Run2 (including commissioning runs).

182 In order to perform timing scan, it is required to open the readout window to at least 3 BC. Having the
 183 fourth L1A bin is even better to monitor the background level. For collision beams, the contribution of
 184 noise hits is considered insignificant. The colliding bunch has to be well isolated so that the migration of
 185 hits from neighbor colliding bunches is not present. There is no strong requirement on the selection of
 186 the trigger stream as long as sufficient statistics is available. For the Run2 analysis typical trigger streams
 187 used are `physics_ZeroBias`, `physics_MinBias`, and `express_express`.

188 For each scan point for each module or front-end, the fraction of hits above a certain ToT (Pixel: ToT ≥ 10 ,
 189 IBL: ToT ≥ 5) at each L1A bin is calculated. Figure 7 shows a typical scan result. The efficiency at the
 190 L1A=1 bin is maximized at around relative delay size of 10 ns to the default timing. If the delay is larger
 191 than this point, the efficiency rapidly drop. If the delay is smaller than this point, for high ToT hits the
 192 efficiency can still keep high, but it is lost for low ToT hits due to time-walk effect. The optimal delay
 193 for high-ToT hits was obtained by fitting the efficiency curve of the target bin (L1A=1) with the following
 194 empirical function:

$$\varepsilon(t) = 1 - A - B \exp(-Ct) - \Theta(t - t_0) \cdot D \cdot (t - t_0)^2 \quad (1)$$

195 where A , B , C , D , and t_0 are the free parameters to fit. $\Theta(t - t_0)$ is the step function. The parameter t_0
 196 gives the optimal delay size. The term A is the contribution of the constant background (e.g. noise hits).
 197 The term $B \exp(-Ct)$ empirically describes the efficiency for L1A=2. The term $\Theta(t - t_0) \cdot D \cdot (t - t_0)^2$
 198 empirically describes the efficiency for L1A=0. This methodology was used for both Pixel and IBL to
 199 determine the optimal delay. An additional safety offset margin can be applied arbitrarily after obtaining
 200 the optimal delay. For the Pixel this size was chosen to 5 ns and this is the same convention as the Run1
 201 choice. For IBL the safety margin is not taken to expect maximized efficiency; it is considered for the IBL
 202 that the delay precision is high enough.

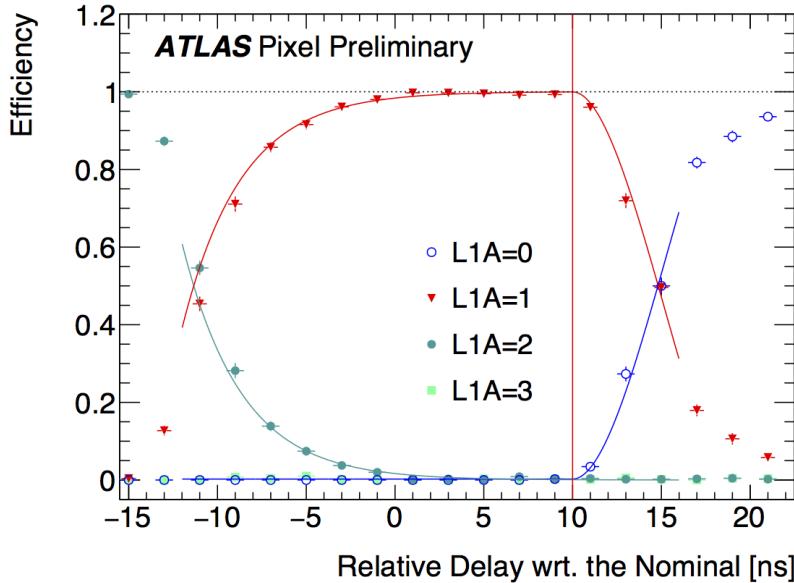


Figure 7: An example of the timing scan for a particular front-end chip of the IBL (Run 270441). The markers show the efficiency at the given delay for time-over-threshold ($\text{ToT} \geq 5$ bunch crossing (BC)), and the lines show the fitting result of the scan for each Level1 accept (L1A) timing window of 25 ns. The vertical line in the figure represents the optimal delay for the timing window labelled as "L1A=1" as the result of the timing scan. The optimal timing has to be determined as the rightmost edge of the plateau in the figure in order to expect the maximum efficiency for low-ToT hits, which has non-negligible time-walk effect, and low-ToT hits are delayed than high-ToT hits. The public plot is available in Ref. [10].

Using run 265573 data, the difference of the optimal delay between the two FEs was calculated. The result is shown in Figure 8. As shown in the plot, it turned out the timing gap size is substantial and not small fractions of the modules have the gap greater than 5 ns. The large dispersion seen in the cosmic ray data in Figure 5 was turned out to be originated by front-end internal latency dispersion. This is problematic for timing adjustment that the two front-ends share the same Tx line, and only one common delay for each channel is there.

4.2. DisVbn tuning of the IBL

After having observed the large latency gap between the two front-ends sharing the same Tx line, it was clarified that the behavior is explained due to the characteristic of discriminator delay for each front-end, and adjustment of the discriminator bias current, DisVbn, was urgently required to ensure the in-time efficiency for 25 ns bunch crossing space collisions. This campaign was performed during the technical shutdown-1 (TS1) in June 2015. The detail of the latency delay mechanism by the discriminator is given in Appendix B.

The adjustment was carried based on the so-called T_0 scan calibration. With the T_0 scan, the parameter PlsrDelay, which is the control of the delay of the strobe of the calibration charge injection, is swept, and the hit efficiency of the target L1A latency is measured. Then one can identify the size of the PlsrDelay that gives the in-time hit efficiency of 50 %.

Delay Gap between 2 Rx's

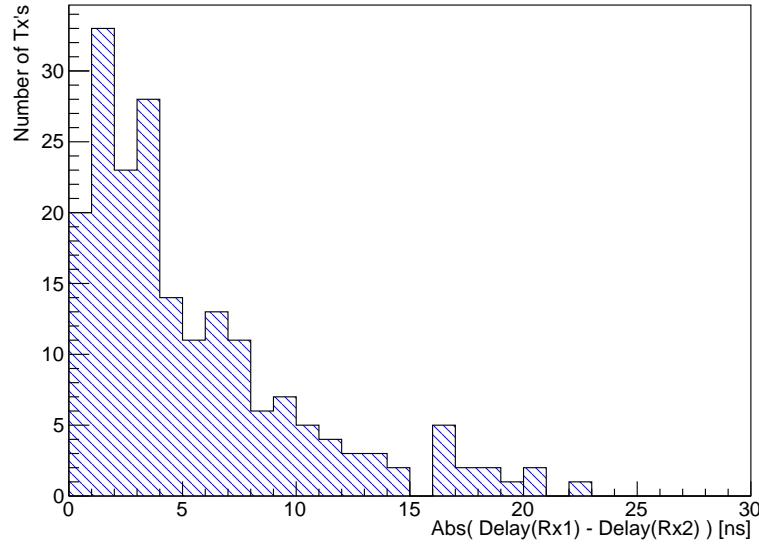


Figure 8: The difference of the latency between the two FE-I4s sharing the same module sharing the same Tx signal line calculated using the timing scan data in the run 265573.

220 The one tick of the PlsrDelay is considered as about 1.2 ns/tick in average, but this is front-end dependent,
 221 and its dispersion is considered of $O(10\%)$. Therefore this method has intrinsic uncertainty to convert the
 222 PlsrDelay to the real time dimension of that order. In addition, in the present T_0 determination method,
 223 as described above, it is defined at the threshold of 50 % efficiency. However the timing dispersion by
 224 pixels in the front-end is also front-end dependent, and adjustment of the delay with targeting at 50 %
 225 efficiency is giving inaccuracy to the timing at 100 % efficiency. This is another source of imperfectionness
 226 of the DisVbn tuning at the moment.

227 The adjustment procedure is as follows. The two front-ends of the same Tx channel is labelled as FE-1
 228 (one at the relatively C-side) and FE-2 (the other one at the relatively A-side). The basic strategy is to
 229 fix the DisVbn of FE-1, and to adjust the T_0 of the FE-2 by seeking the appropriate DisVbn value. The
 230 baseline of the DisVbn value of FE-1 is chosen by looking at the T_0 distribution at a fixed DisVbn value,
 231 and it is determined at so that FE-2's T_0 can be adjusted to the FE-1's for as much FE pairs as possible.
 232 The baseline DisVbn of the FE-1s was chosen as 55. The adjustment of the FE-2's DisVbn is automatized
 233 in the calibration console, and for about 90 % of the pairs it gave valid adjustment. For the rest pairs,
 234 the automatic adjustment failed because the algorithm does not find a solution in the scanned DisVbn
 235 parameter range due to having large latency gap between the FEs. In this case, the DisVbn- T_0 map as
 236 shown in Figure 9 is consulted for each pair, and the DisVbn values of both FE-1 and FE-2 are chosen
 237 manually so that the T_0 of the two FEs matches. Figure 10 gives the DisVbn map after the automatic and
 238 custom adjustments.

239 Finally the T_0 scan is performed, and the timing difference between the two FEs is measured. Figure 11
 240 compares the T_0 gap between FE-1 and FE-2 before and after the DisVbn adjustment.

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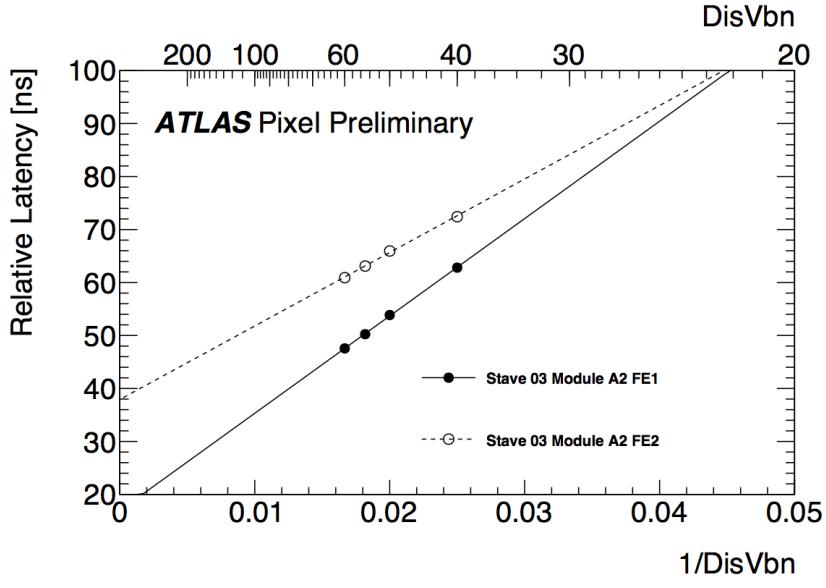


Figure 9: Variation of the latency of front-end chips of a particular module of the IBL as a function of FE-I4 configuration parameter DisVbn to change the discriminator bias. The public plot is available in Ref. [10].

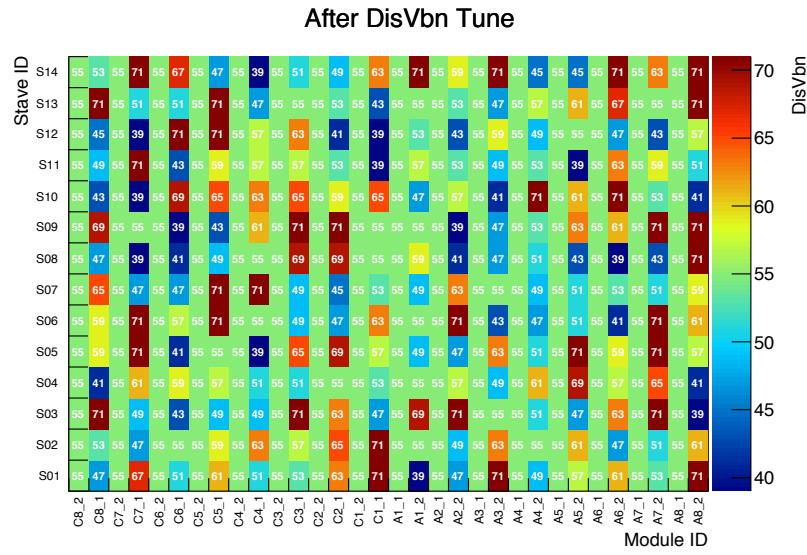


Figure 10: Map of the DisVbn for each front-end after the DisVbn adjustment.

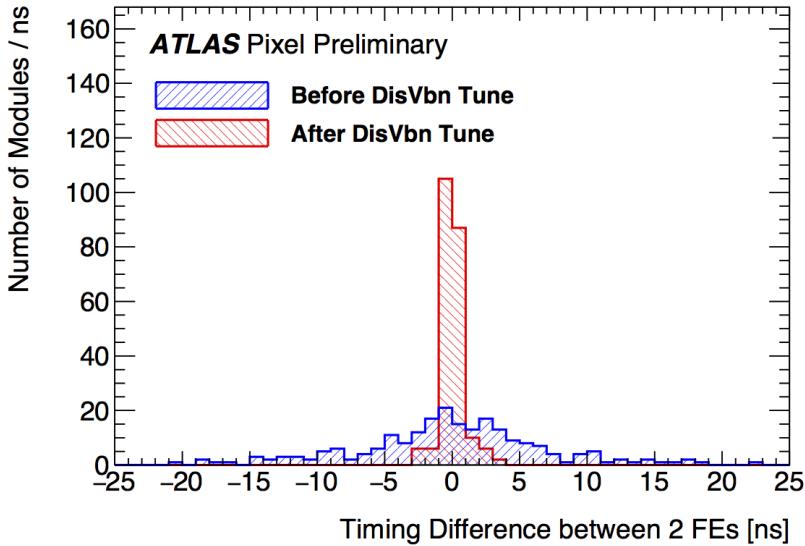


Figure 11: Timing difference between the 2 FEs in the common module of the IBL for the status before and after the discriminator bias (DisVbn) adjustment. The public plot is available in Ref. [10].

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241 4.3. Timing Scan after the DisVbn tuning

242 With the DisVbn tuning during the TS-1, the latency gap of the front-end pairs was mostly compensated.
243 After TS-1, another timing scan (run 270441, July 5) was performed in order to determine the BOC delay
244 size for each pair (Figure 7). The BOC delay map was created using both the coarse and the fine delay
245 mechanisms. The result of the BOC delay adjustment was in general satisfactory as will be presented in
246 Figure 13.

247 For small number of front-end pairs, this timing scan identified >3 ns gap between the front-ends. This
248 is considered to be the tail dispersion of the T_0 scan accuracy discussed in the previous section. It was
249 decided for these FE pairs, an additional manual DisVbn adjustment is made during TS-2 in August 2015.
250 The adjustment size is determined by consulting the DisVbn- T_0 relation in Figure 9. The in-time efficiency
251 measurement after this showed some improvements in the average efficiency, in particular at ToT=3 a few
252 percent improvement was achieved.

253 4.4. In-time efficiency measurement

254 In-time efficiency was measured to validate the timing adjustment using runs with ≥ 3 BC readout window,
255 and the target timing window is set at the second L1A bin. For collision beams, the contribution of noise
256 hits is considered insignificant. The colliding bunch has to be well isolated so that the migration of hits
257 from neighbor colliding bunches is not present. In this measurement, the efficiency is simply calculated
258 for each ToT as the fraction of hits at the second L1A bin over the total number of hits in the 3 BC window.
259 In order to obtain the pure in-time efficiency, both of the hit doubling of the Pixel and HitDiscCnfg of the
260 IBL are required to be turned off.

261 Figure 12 shows Pixel Detector’s average in-time efficiency as a function of ToT. The in-efficiency turns-on
 262 at around $\text{ToT} \approx 5$ and saturates around $\text{ToT} \approx 20\text{-}30$. This turn-on structure reflects the time-walk effect.
 263 Figure 13 shows the same plot for the IBL. For comparison, the status before the adjustment using the
 264 timing scan result, and the expected in-time efficiency using the timing scan result are also shown in
 265 the plot. The result overall agrees with the expectation, and is slightly better than the expectation. The
 266 adjustment status is considered to be sufficiently good.

267 In this plot, the hits with $\text{ToT}=1$ have significantly higher efficiency than $\text{ToT}=2$, and this is not explained
 268 by the simple time-walk mechanism. This fundamental cause of having such a feature is not understood
 269 very well, but it is observed, at least for the IBL, that these “fast $\text{ToT}=1$ ” hits are indeed associated to
 270 physical hits (not noises), in particular the cluster’s size and total charge is large. Some examples of such
 271 clusters are shown in Appendix D.

272 4.5. Performance with time-walk compensation : Hit Doubling (Pixel) and HitDiscCnfg 273 (IBL)

274 The time-walk effect delays low-charge hits, and this could be a source of inefficiency for 1 BC readout.
 275 For the Pixel, the hit doubling function enables to copy the hits with ToT less than a specified value to with
 276 tagging as the hits of the previous bunch crossing. The copied hits occupy the buffer in addition to the
 277 original ones, therefore the hit occupancy increases. The hits with $\text{ToT} \leq 7$ were doubled when limiting
 278 the Pixel’s readout window to 1 BC.

279 For the IBL, a similar function is implemented with a switch called HitDiscCnfg. The implementation
 280 detail is given in Appendix C. For 25 ns bunch space collisions, it was decided to operate the IBL with
 281 configuring HitDiscCnfg=2. The in-time efficiency with enabling HitDiscCnfg is shown in Figure 14.
 282 Compared to Figure 13, the recovery of the efficiency for low-ToT hits ($\text{ToT}=1,2$) is substantial.

283 5. Outlook

284 The timing of DBM is not commissioned yet since the DBM was not operational in the 2015 runs, and
 285 this is the subject to be done once the DBM takes part in ATLAS. For the Layer-2 upgrade which will
 286 take place from the end of 2015, it is necessary to re-adjust the timing. Monitoring of the stability of the
 287 timing is needed. Studies in 2015 showed that the IBL T_0 scan showed drifting by ~ 1 ns, as shown in
 288 Figure 15. It is not clear if this drift is correlated to the total ionization doze effect which makes drift other
 289 calibration parameters. The last timing scan which took place in November 2015 however didn’t exhibit
 290 correlated delay of the latency, which suggests that for monitoring of the timing adjustment stability the
 291 T_0 scan might not be useful and the actual timing scan would be necessary. Further studies are necessary
 292 to understand the behavior the timing of the IBL under irradiation.

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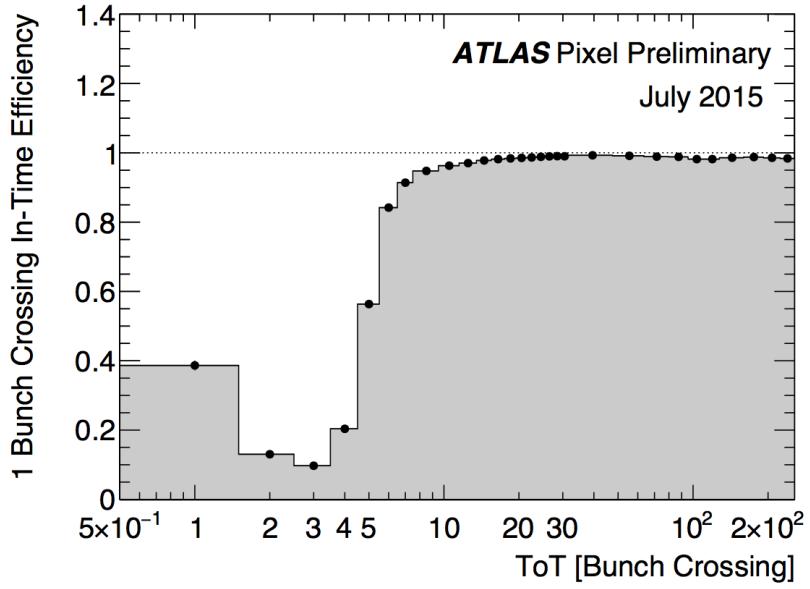


Figure 12: One bunch-crossing in-time efficiency of the Pixel as a function of time-over-threshold (ToT) after the timing adjustment reflecting the result of the timing scan. The data was taken during a 50 ns bunch space collision run. The public plot is available in Ref. [10].

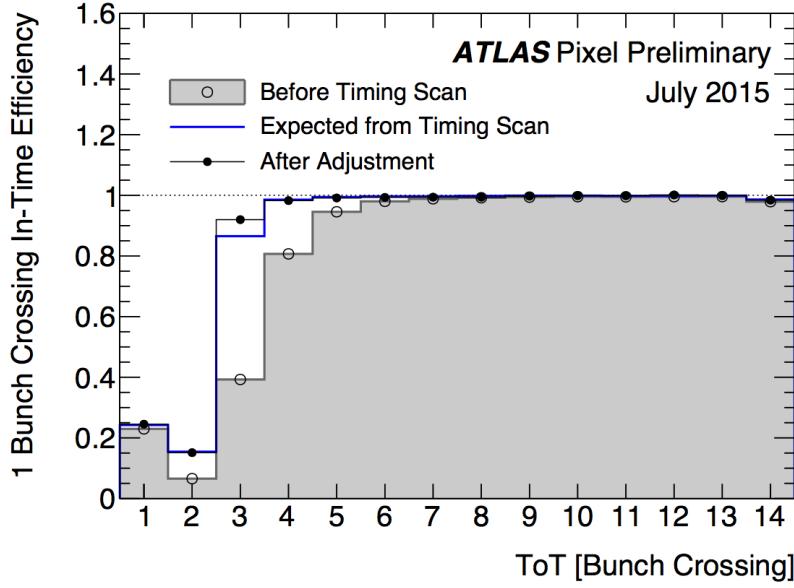


Figure 13: One bunch-crossing in-time efficiency of the IBL as a function of time-over-threshold (ToT) before and after the adjustment reflecting the timing scan result in July 2015. The blue histogram is the estimation of the expected efficiency from the result of the timing scan. Note that the function to recover small ToT hits is not enabled in these data. The public plot is available in Ref. [10].

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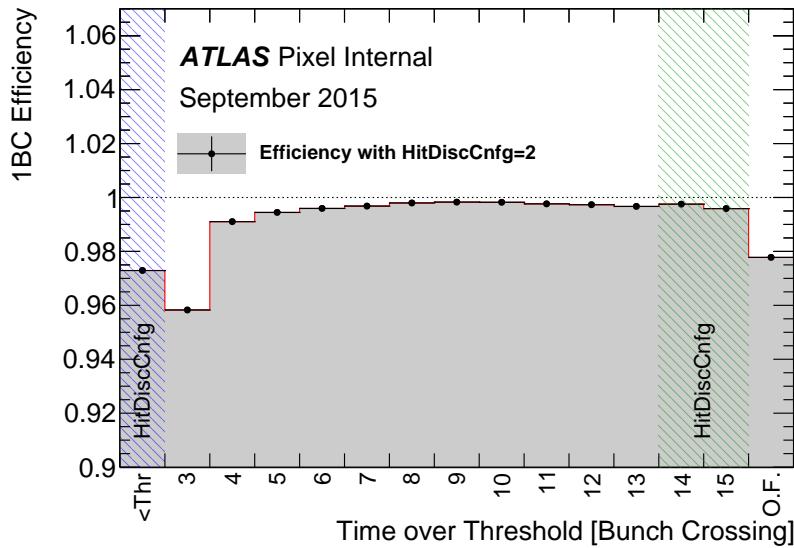
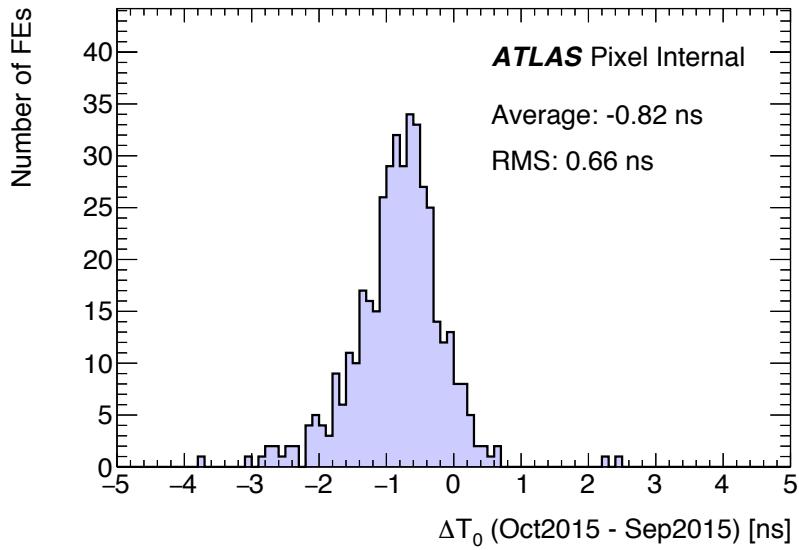
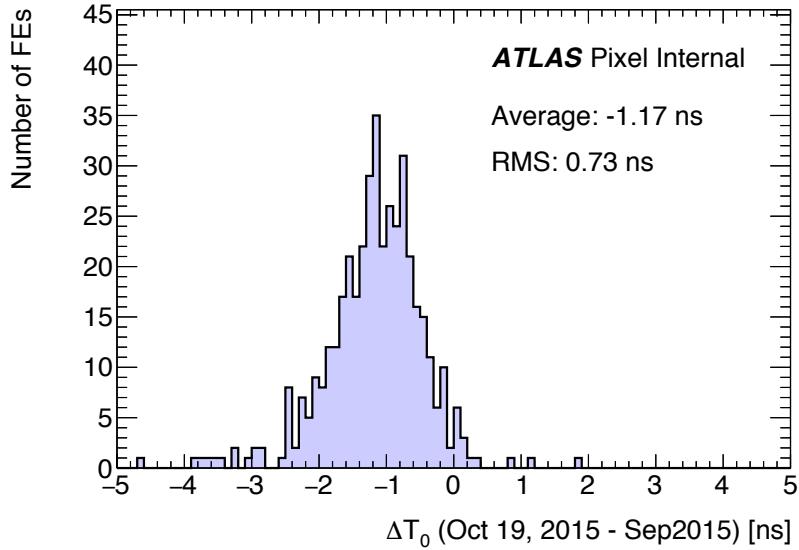


Figure 14: In-time hit efficiency of the IBL for 1 bunch crossing (BC) readout window with setting HitDiscCnfg configuration to mode “2” (the default configuration for 25 ns bunch space collisions). This switch was activated with the change of the LHC bunch filling scheme from 50 ns bunch space to 25 ns bunch space in August 2015. The measurement of the in-time hit efficiency shown in this plot was performed using a special condition run with expanding the readout window from 1 BC to 3 BCs in September 2015. In this HitDiscCnfg mode, low time-over-threshold (ToT) hits of ToT=1,2 is combined in “< Thr” bin (blue band) with also copying the hits in the next bunch crossing to the triggered bunch crossing. This contributes to achieve about 97 % hit efficiency for ToT=1,2 hits with recovering delayed hits due to time walk at the cost of being ToT=1 and ToT=2 hits degenerated. As a by-product of HitDiscCnfg switch, the ToT dynamic range is expanded from 13 to 15 (green band). “O.F.” bin represents the overflowed hits with ToT greater than 15. The public plot is available in Ref. [10].

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(a) Measurement on October 8, 2015



(b) Measurement on October 19, 2015

Figure 15: Difference of the average T_0 of each front-end obtained by the T_0 scan with respect to the measurement performed on September 1, 2015 (integrated luminosity: $\sim 0.2 \text{ fb}^{-1}$) for (a) the scan on October 8 (integrated luminosity: $\sim 2.2 \text{ fb}^{-1}$), and (b) on October 19 (integrated luminosity: $\sim 2.6 \text{ fb}^{-1}$)

293 **Appendix**

294 **A. Distribution of timing and trigger signals to the front-end electronics**

295 In this section the components of the DAQ chain relevant to propagation of timing signals, the commu-
296 nication of the timing signals, and the delay tuning parameters are described.

297 **A.1. DAQ electronics**

298 The timing signal propagation from the central ATLAS to each module of the Pixel and IBL is a large
299 tree structure and bifurcation in several steps. It is convenient to classify the chain into sub-categories as
300 follows:

- 301 • CTP and TTC crate,
- 302 • DAQ crate,
- 303 • On-detector components.

304 The overview of the chain is illustrated in the diagram in Figure 16. In the following, brief description on
305 each element is given.

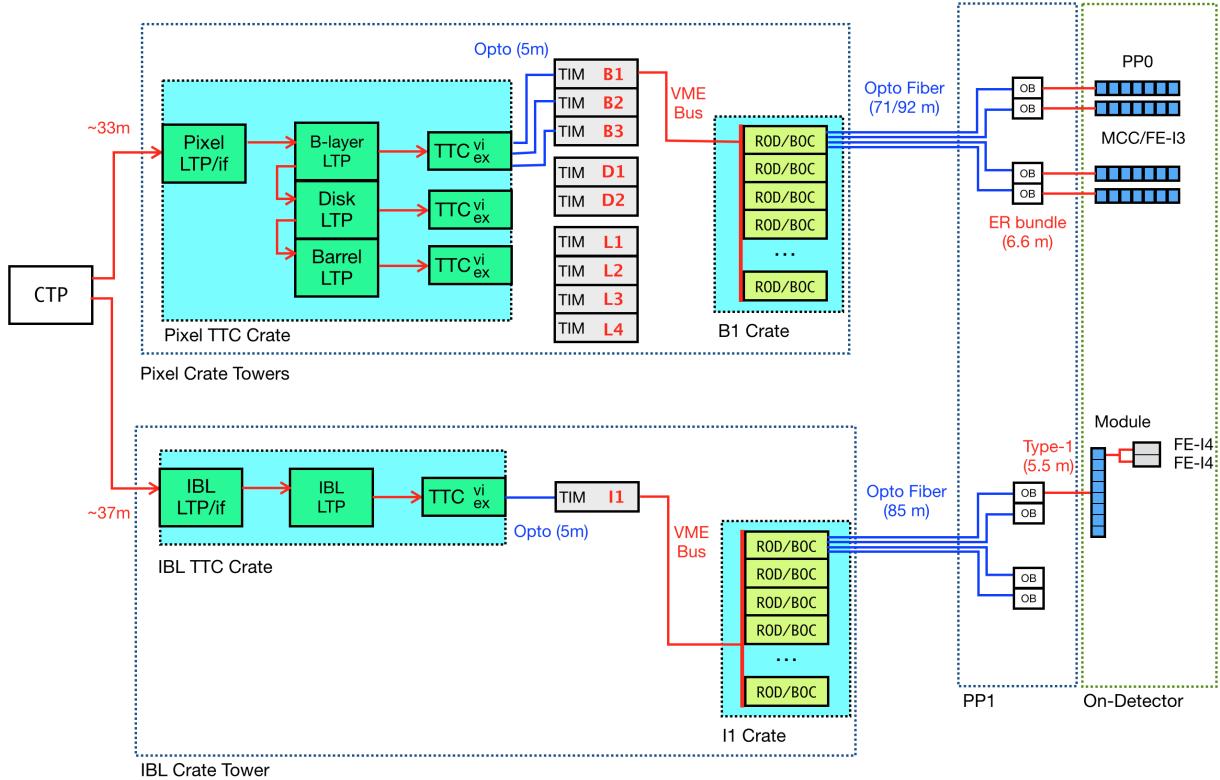


Figure 16: Schematic diagram of the TTC signal chain in the Pixel and IBL partitions in Run2.

306 **A.1.1. CTP and TTC crate**

307 **CTP** Central Trigger Processor (CTP) [5] is the core of the Level-1 trigger which gathers all Level-1
 308 requests from sub-detectors (L1Calo, MuCTPi,...), and it distributes the L1A signal to all sub-
 309 detectors via the CTP link.

310 **CTP Link** The CTP link is a bundle of electronic signal lines connecting the CTP and the TTC interface
 311 board of each detector. There is one CTP link for the entire Pixel detector, and there is another one
 312 for the IBL and DBM. The Pixel CTP link is about 33 m, while the IBL CTP link is about 37 m.

313 **LTP interface** LTP interface is the interface board between the CTP and the LTP. The latency is estimated
 314 to be about 12.5 ns.

315 **LTP** A Local Trigger Processor (LTP) [11] is controling a DAQ partition. For Pixel there are three LTPs
 316 of B-Layer, Disk, and Barrel. For IBL/DBM there is one LTP. A LTP has one CTP link input and
 317 one CTP link output. The CTP link output can be connected to another LTP to compose a daisy
 318 chain of the LTPs. For Pixel, the B-Layer LTP (LTP_B) is connected to the Pixel LTP interface, and
 319 it is daisy-chained to the Disk's (LTP_D) and Barrel's (LTP_L) LTP in this order. LTP is the root
 320 node of the DAQ chain in case of running standalone data taking.

321 **TTCvi (Mark-II)** The TTCvi module [12] delivers the A-Channel and B-Channel signals to the TTC
 322 transmitters (TTCex) for multiplexing, encoding, optical conversion and distribution to the TTCrx
 323 ASICs. It accepts L1A signals from the parent LTP or other sources, or it can also generate random
 324 triggers or calibration triggers for testing. The phase between the clock and the phase of the A- and
 325 B-Channel output can be adjusted with the front-panel BC DELAY switch from 0 to 30 ns with 2
 326 ns tick.

327 **TTCex** The TTCex encodes the clock, A/B-Channel in bi-phase mark (BPM) encoding, and does transmit
 328 laser signals to multiple TTCrx modules.

329 **A.1.2. DAQ crate**

330 **TTCrx** The TTCrx module [13] is the receiver of the TTC signals transmitted from the TTCrx which
 331 is mounted on each TIM. It is possible to add coarse and fine delays (TTCrxCourseDelay and
 332 TTCrxFineDelay) for adjusting the timing phase of the entire crate.

333 **TIM** A TIM (TTC Interface Module) [14] is inserted in the middle of the crate (the slot 13). The TIM
 334 receives the TTC signals from the TTC crate via the TTCrx module, and distributes them to RODs
 335 and BOCs in the crate using the VME backplane bus lines. The number of TIMs, i.e. the number
 336 of crates depends on the partition in table . The so-called trigger delay (TIM Trigger Delay) is
 337 used to adjust the latency of the L1A signal to match with the front-end chip's latency.

Partition	Number of Crates	List of Crates
Pixel B-Layer	3	B1, B2, B3
Pixel Disk	2	D1, D2
Pixel Barrel	4	L1, L2, L3, L4
IBL and DBM	1	I1

Table 5: Mapping between partitions and crates.

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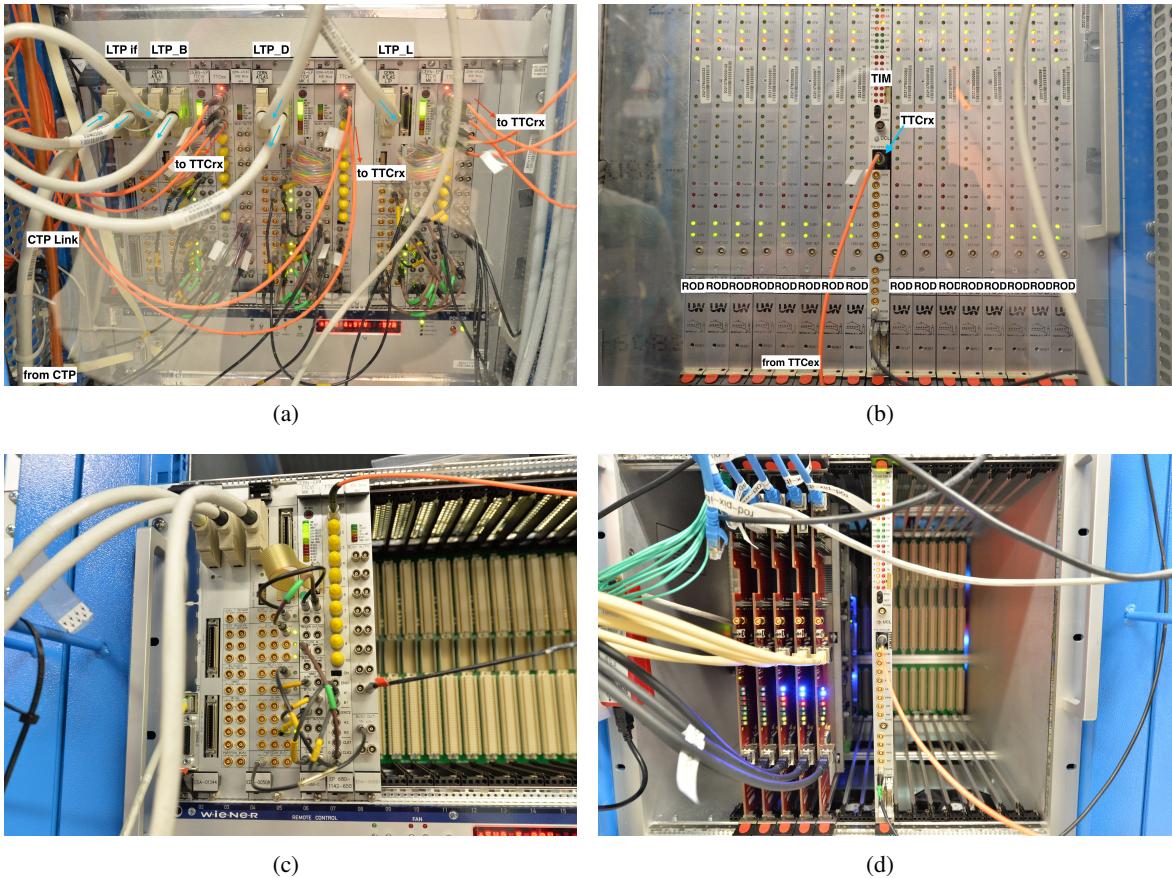


Figure 17: (a) Picture of the Pixel TTC crate. (b) Picture of a Pixel DAQ Crate (B1?). (c) Picture of the IBL TTC Crate. (d) Picture of the IBL DAQ Crate (I1).

338 **ROD and BOC** There are up to 15 RODs (Read-Out Drivers) [15] allocated for each crate. Slot 6-21 of
 339 the crate (except Slot 13 used for the TIM) are the place to hold RODs. The RodBcidOffset is set
 340 in the RunConfig to adjust the BCID offset between the LHC and the module.

341 One BOC (Back-of-Crate) module [16] is paired for each ROD. A BOC has 4 sockets of the Tx and
 342 Rx optical ribbons, respectively. The Tx line is used to transfer the timing signals from the BOC
 343 to modules, and the Rx line is used to receive the module's hit data. A BOC also has a couple of
 344 S-Links to transfer the data processed by the ROD to ROS (Read-Out Storage) and to the FTK.

345 **Optical ribbons** An optical ribbon connects the BOC Tx or Rx socket to the Optoboard socket. Each
 346 ribbon contains either 8 or 12 fiber lines. For Tx ribbons, a fiber line in the ribbon corresponds to
 347 one module. The optical ribbons were replaced for the Pixel during LS-1. The length of the optical
 348 ribbon is about 71 m or 92 m for Pixel, and is 85 m for IBL and DBM.

349 Signals transmitted from the Tx line to the module are Clock, L1A, BCR, ECR, and various module
 350 configuration commands.

351 Note that, for the timing commissioning, only the Tx side ribbons are considered for adjustment of
 352 the L1A latency. The Rx side is irrelevant to the timing commissioning. For Pixel, however, it is

353 necessary to tune the timing phase of the Rx receiver (so-called BOC Tuning) but this is outside
 354 the scope of this note.

355 **A.1.3. On-detector components**

356 **Optoboard** The optoboard (OB) [17] converts the received optical signal to electric signal (Tx), the
 357 received electrical signal to optical signal (Rx). It is attached at the Patch-Panel-1 (PP1) around the
 358 Inner Detector End Plate (IDEP).

359 **ER-bundle / Type1 bundle** The so-called ER-bundle (for Pixel) and Type1 bundle (for IBL) connects
 360 between the PP1 optobards and the PP0 (Patch-Panel-0). The PP0 for Pixel is mounted on the
 361 detector side of the nSQP which is a few tens centimeter distant from the module.

362 **Pixel: MCC and FE-I3** Please refer Ref. [18] for MCC and Ref. [19] for FE-I3.

363 **IBL / FE-I4** Please refer Ref. [7] for FE-I4.

364 **A.2. Clock and signal propagation from ATLAS to modules**

365 **CLOCK** The LHC clock frequency is 40 MHz (25 ns tick). For physics collision beams, The ATLAS
 366 central clock is synchronized with the LHC clock (for cosmic-ray data taking the ATLAS employs
 367 its own clock and distributes to all subsystems.). Many downstream DAQ components have their
 368 own clock so that they can work stanalone. For instance, the LTP has its internal clock, and for the
 369 Pixel standalone data taking the system works with synchronization to the LTP clock. In case of the
 370 ATLAS central data taking, all these clocks phases are synchronized to the central clock.

371 **L1A** The L1A (Level-1 Accept, LVL1A) signal is issued whenever the CTP decides to trigger the event.
 372 The L1A signal up to TTCrx is a single bit, and it is sent from TTCvi to TIM via A-signal
 373 (asynchronous signal line) to minimize the latency. The L1A signal emitted from BOC is 5 bit long
 374 (**11010**).

375 **ORBIT/BCR and BCID** The ORBIT signal is transmitted per orbit revolution frequency of 11 kHz from
 376 the LHC to the CTP, and it is distributed to all subsystem partition's TTCvi. An ORBIT signal is
 377 converted to a BCR (Bunch Counter Reset) and emitted downstream from the TTCvi. The phase of
 378 the BCR can be adjusted using the TTCvi BCR Delay parameter. The BCID (Bunch Crossing ID)
 379 is incremented every clock cycle at the local counter in the chain, e.g. at the ROD or at the module.
 380 The BCID is reset to the initial value at the ROD and the module respectively once the BCR signal
 381 is received.

382 The ORBIT signal is sent via a dedicated line in the CTP link to the LTP interface, and via B-signal
 383 (synchronous signal line) from the TTCvi to the TIMs. From BOCs to modules the BCR signal is
 384 sent via the same line as the L1A signal, the L1A signal cannot be sent during the BCR signal is
 385 sent ³. The BCR signal emitted from BOC is 9 bit long (**101100001**), and the L1A signal is 5 bit
 386 long. The 14 BC duration where the BCR and the L1A signal are colliding has problem in issuing
 387 either BCR or L1A.

³ Such feature is only specific to Inner Detector

388 This is an undesirable situation and it is indeed desired to be able to issue L1A for all possible
 389 colliding bunches, especially at BCID=1⁴. In order to solve this problem, the BCR signal is moved
 390 into the abort gap for Pixel [20], and the BCR signal arrives at each front-end module by 13 BC
 391 earlier than the other subsystems. This is achieved by subtracting the TTCvi.BCR.Delay by 13 BC.
 392 The counterpart delay of 13 BC has to be inserted as the TIM.BCR.Delay so that the ROD.BCID is
 393 kept synchronized with the ATLAS BCID.

394 Inevitably the module.BCID and the ROD.BCID has a finite offset which should not be counted as
 395 the BCID mismatch. This offset is specified as RodBcidOffset and its size is 11 BC for both Pixel
 396 and IBL. The composition of this 11 BC is not simple, but formally it should be written as

$$\begin{aligned} 11 \text{ BC} &= [(\text{TIM.BCR.Delay}) - \text{size(BCR signal)}] + \text{ROD.Latency} + \text{size(L1A signal)} \\ &= \text{RodBcidOffset} \end{aligned}$$

397 where TIM.BCR.Delay = 13 BC, size(BCR) = 9 BC, ROD.Latency = 2 BC, and size(L1A) =
 398 5 BC, respectively.

399 The BCID difference between the ROD and the module is calculated as

$$\text{BCID diff} = ((\text{module.BCID}) - (\text{ROD.BCID}) - \text{RodBcidOffset}) \& 0xff$$

400 and the l.h.s. of the above equation is kept zero when no *unexpected* BCID mismatch is there,
 401 otherwise the BCID Error is issued in the ROD trailer of the bytestream.

402 **ECR** The ECR (Event Counter Reset) signal is issued once per a few second. If an ECR is received, the
 403 lower 24 bits of the L1ID (event counter) is reset to zero for both the TIM and the modules, and
 404 the higher 8 bits of the L1ID (ECR counter) is incremented. The propagation of ECR is similar to
 405 BCR. The ECR signal emitted from BOC also is 9 bit long (101100010).

406 **L1ID** Similar to the BCID, the L1ID information is also transmitted from the TTC to the TIM. With the
 407 similar manner to the BCID, there are ROD L1ID (which is transmitted from the TIM) and module
 408 L1ID. The ROD L1ID information is not propagated to the module, and at each module the L1ID is
 409 incremented locally every time the L1A signal arrived. Therefore the ROD L1ID and the module
 410 L1ID are compared at the ROD, and if mismatches are detected the ROD issues L1ID Error in the
 411 ROD trailer of the bytestream.

412 A.3. Tuning parameters

413 The list of tuning parameters for timing commissioning is listed as follows:

414 **TTC Segment Configurations (Common)** TTCvi.BCR.Delay

415 **TTCrx coarse/fine delay (Common)** TTCrx coarse and fine delay inserts a finite size delay to all signals
 416 transmitted from the TTC. Not only the L1A signal, but also other signals including CLOCK is
 417 delayed. The TTCrxCoarseDelay has a unit of 1 BC (25 ns), and the TTCrxFineDelay has a unit
 418 of 0.1 ns.

⁴ For example, if the LHC has only 1 bunch filled, that bunch is labelled as BCID=1.

419 **TIM Trigger Delay (Common)** The TIM Trigger Delay is the delay to the L1A signal. It has a unit of
 420 1 BC (25 ns), and is used to compensate the shortage of the L1A latency compared to the latency
 421 configuration of the front-end module. The Pixel front-end latency has been set to 255 BC, and for
 422 the Run2 the trigger delay is set at 118 BC by default. The remaining residual of 137 BC matches
 423 with the ATLAS central latency and the latency of the Pixel/IBL DAQ system.

424 **BOC coarse and fine delay (Pixel)** The BOC delays are used to compensate the latency dispersion de-
 425 pending on modules reflecting the difference of e.g. cabling lengths. The Pixel BOC coarse delay
 426 has a unit of 1 BC, can be set in [0-31]. The Pixel BOC fine delay has a unit of 0.3 ns, can be set in
 427 [0-127]. The technology of implementing the fine delay is based on the BPM phase control. There
 428 is an intrinsic inaccuracy of the fine delay tick size. See Ref. [[timon_boc](#)] for details of the BOC
 429 fine delay studies.

430 **BOC coarse and fine delay (IBL)** The coarse delay is implemented using a variable-tap shift register
 431 clocked with 160 MHz with using both the rising and falling edges. The IBL BOC coarse delay has
 432 a unit of 0.125 BC (3.125 ns) which is implemented by subdivision of the given clock into 8 within
 433 the BOC internal logic. The fine delay is adjusted using IODELAY2 elements in the Spartan6 I/O
 434 blocks. These IODELAY2 elements are described in and provide a step of around 28 ps per tap. A
 435 set of ACE files corresponding to 350 ps unit delay is deployed.

436 **FE-I4 DisVbn (IBL)** The DisVbn is a parameter to change the FE-I4's discriminator bias current which
 437 changes the delay of the discriminated pulse's output from the actual threshold crossing time. The
 438 relation between the FE-I4 internal latency and DisVbn is given in Appendix B. The standard value
 439 of DisVbn was chosen at 40 for Stage qualification assurance (QA) during construction, and it was
 440 chosen at 55 for Run2.

441 B. DisVbn parameter of FE-I4

442 There are two major factors which determine the time delay of the FE-I4 - the amount of charge injected
 443 and the current supplied to the discriminator (DisVbn). DisVbn is a parameter that is common to all
 444 pixels on a module and can be internally adjusted. During detector operation the amount of signal charge
 445 varies from hit to hit and this variation cannot be controlled. This presents a problem when attempting
 446 to associate a hit with a particular beam crossing. The time delay for a large hit may be 50 ns, while the
 447 time delay for a small hit could be as much as 100 ns. Since the beam crosses at the center of ATLAS
 448 every 25 ns, the firing time of a pixel alone is not sufficient information to associate a hit with a particular
 449 crossing. This time walk - difference in time delays between large and small hits - is a challenge that
 450 detector operation must contend with.

451 To understand the behavior of the discriminator, one can consider the behavior of a simple model as shown
 452 in Figure 18. The resistance is the output impedance of the ideal amplifier and the capacitance is the load
 453 capacitance of the ideal inverter. The output of the ideal amplifier is $V_{IAO} = \alpha(V_{thr} - V_{AO})$ where α is the
 454 gain of the amplifier. V_{IAO} must stay between the negative and positive power supply voltages, namely
 455 ground and V_{dd} . When V_{AO} goes below V_{thr} , V_{IAO} will rise from the ground to V_{dd} . Current will run
 456 through the resistor and the capacitor will begin to charge. Once the voltage across the capacitor is high
 457 enough, say V_S , the output of the ideal inverter will immediately switch from ground to V_{dd} . To find the

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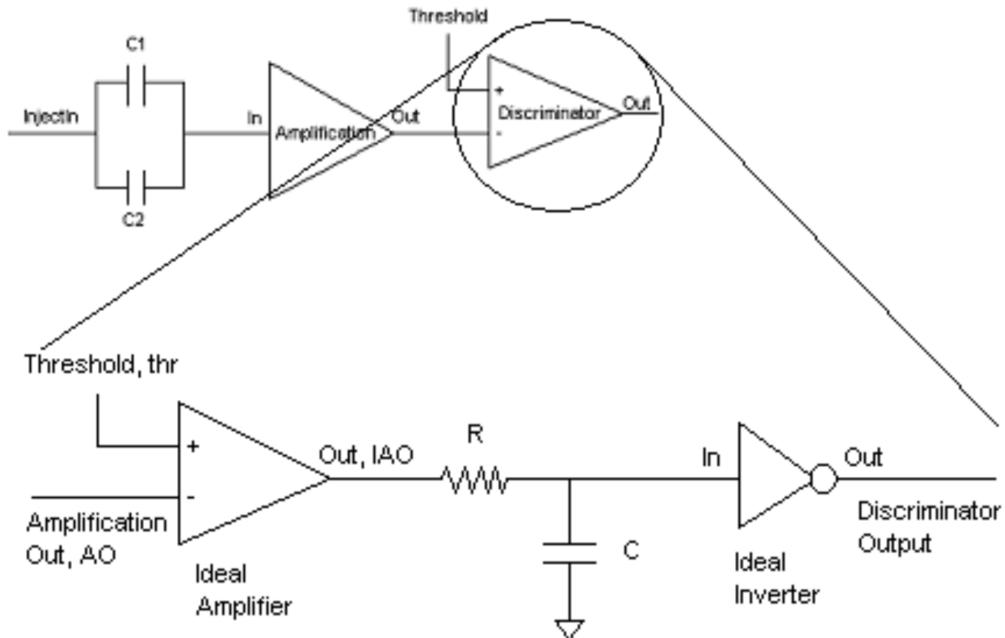


Figure 18: A model of a pixel’s discriminator. The resistance is the output impedance of the ideal amplifier and the capacitance is the load capacitance of the ideal inverter. Once the voltage across the capacitor is high enough, the ideal inverter will output a positive going digital pulse, and the discriminator will fire.

458 amount of time that takes the capacitor to charge up to V_S , observe that $V_C + V_R = V_{IAO}$. This equation
459 becomes a first-order differential equation about q with substituting $V_C = q/C$ and $V_R = R\dot{q}$:

$$R\dot{q} + q/C = V_{IAO}. \quad (2)$$

460 V_{IAO} quickly reaches V_{ddd} because of the high gain of the ideal amplifier and can be treated as a constant. The
461 solution to this equation is $q(t) = V_{IAO} \cdot C(1 - e^{-t/RC})$ which can be used to find $V_C(t) = V_{IAO}(1 - e^{-t/RC})$.
462 The amount of time it takes the capacitor to charge to V_S can be found by substituting V_S for V_C and solving
463 for t : $t = RC \cdot \ln(V_{IAO}/(V_{IAO} - V_S))$. Once the capacitor has charged to V_S , the discriminator fires in
464 response to the hit. In this simple model, the output impedance, R , is given by V_{ddd}/DisVbn . This is
465 because the discriminator cannot supply more current than its input operating current, DisVbn . Therefore
466 the discriminator time delay becomes

$$t_{\text{discr}} = C \cdot \ln \left(\frac{V_{IAO}}{V_{IAO} - V_S} \right) \cdot \frac{V_{ddd}}{\text{DisVbn}}. \quad (3)$$

467 The main consequence of the above discussion is that the discrimination delay is scaling to $1/\text{DisVbn}$.
468 However, the coefficient is quite front-end dependent, as illustrated in Figure 9. In addition, in the IBL
469 DAQ system the Tx signal line is common for the two front-ends, and the latency difference between the
470 two front-ends is, by default, mismatched. This feature of FE-I4 requires to tune DisVbn to adjust the
471 latency between the two front-ends, so that the rest of the latency between the IBL modules becomes
472 adjustable only with the delay for the Tx signal at the BOC.

473 C. HitDiscCnfg of FE-I4

474 The output data of the FE-I4 about the ToT information of hits has a unique feature of encoding called
 475 “ToT code”, and its encoding manner is dependent on the configuration of digital threshold switch called
 476 HitDiscCnfg. These FE-I4 “ToT code” ToTs are mapped to another ToT values at the ROD which are as
 477 close to the “real” ToT as possible, but that is also dependent on the HitDiscCnfg configuration reflecting
 478 the FE-I4’s behavior. Table 6 summarizes the relation between the “real” ToT, FE-I4 ToT (“ToT code”),
 479 and the ROD output (bytestream).

480 The following items summarize the features of the ToT mapping in Table 6:

- 481 • Pulses below the analog threshold is always recorded as 15 (**0xF**) at the FE-I4, and decoded as 0 at
 482 the ROD output.
- 483 • *Small hits* (above the analog threshold and below the digital threshold) are recorded as 14 (**0xE**) at
 484 the FE-I4, and decoded as 1 at the ROD output.
- 485 • *Big hits* (above the digital threshold) are counted from 0 at the FE-I4, and its counting starts above
 486 the digital ToT threshold. The ROD converts the FE-I4 output so that the real ToT is reproduced.
 487 The exception is the overflow hits for HitDiscCnfg=2, where the hits of the real ToT greater than
 488 15 are recorded as 2 at the ROD.
- 489 • Overflow threshold changes with HitDiscCnfg. It is 14, 15, and 16 for HitDiscCnfg=0, 1, and 2,
 490 respectively.

491 The reason of having such complex encoding of the “ToT code” at the FE-I4 is related to the ToT counting
 492 mechanism. The following description of the detail of the ToT “encoding” (or implementation) in the
 493 FE-I4 and its relation to the HitDiscCnfg (digital threshold) configuration is cited from the FE-I4B
 494 Integrated Circuit Guide Section 4.4 [7]:

- 495 • The digital threshold is applied to the discriminator output of each pixel prior to starting a dedicated
 496 4-bit binary counter for ToT. This is done with a shift register adjustable between 1 and 3 cells (1
 497 cell for digital threshold 0 to 3 for digital threshold 2).
- 498 • If the input and output of the shift register are both high, then the hit has passed the digital threshold
 499 and is considered a “big hit”.
- 500 • The reset value of the ToT counter is **1111**, and for pixels whose analog discriminator did not fire,
 501 this is the value that will remain as the ToT code meaning “no hit”.
- 502 • Whenever the analog discriminator does fire, the counter is decremented to **1110**, which means
 503 “small hit”, but does not automatically continue to count until the digital threshold shift register has
 504 finished shifting. If the digital threshold is passed (big hit), the counter is cleared to **0000** and starts
 505 to count. Otherwise it remains at the **1110** code for small hit.

506 With HitDiscCnfg, it is possible to recover small hits delayed to be discriminated due to the time-walk
 507 effect:

508 While the “big hit status” of each pixel is allowed to persist for only one clock cycle, a
 509 “small hit status” persists for 2 clock cycles. *Thus the ToT code for small hit will be recorded*
 510 *if it was present either at the same time as a big hit or in the clock after.* Each pixel has one
 511 neighbor: above (below) in the same column for the pixels at the top (bottom) of the PDR. If

512 the neighbor's status shows a small hit during at the time a big hit occurs or in the clock after,
 513 the neighbor bit is latched, if it shows a big hit or no hit then it is not latched.

Real ToT	Output					
	HitDiscCnfg=0		HitDiscCnfg=1		HitDiscCnfg=2	
	FE-I4	ROD	FE-I4	ROD	FE-I4	ROD
Below analog thr.	15	0	15	0	15	0
1	0	1	14	1	14	1
2	1	2	0	2	14	1
3	2	3	1	3	0	3
4	3	4	2	4	1	4
5	4	5	3	5	2	5
6	5	6	4	6	3	6
7	6	7	5	7	4	7
8	7	8	6	8	5	8
9	8	9	7	9	6	9
10	9	10	8	10	7	10
11	10	11	9	11	8	11
12	11	12	10	12	9	12
13	12	13	11	13	10	13
14	13	14	12	14	11	14
15	13	14	13	15	12	15
>15	13	14	13	15	13	2

Table 6: Map of the real ToT, the FE-I4 output (“ToT Code”), and the ROD output for different configurations for HitDiscCnfg={0,1,2}.

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514 D. Investigation on low-ToT hits

515 “Fast ToT=1” hits are (mostly) part of clusters. (Not isolated.) “Fast ToT=1” hits are (mostly) part of
 516 physics, not noises. Should be included in the in-time efficiency calculation. “Fast ToT=1” hits are often
 517 seen in the peripheral part of large-size and large-charge clusters which contain multiple overflow hits
 518 (heavy-particle-like).

519 The reason why we have “Fast ToT=1” hits is not clear so far, but it seems to be correlated with large
 520 charge deposit. Further investigations will be needed to better understand this.

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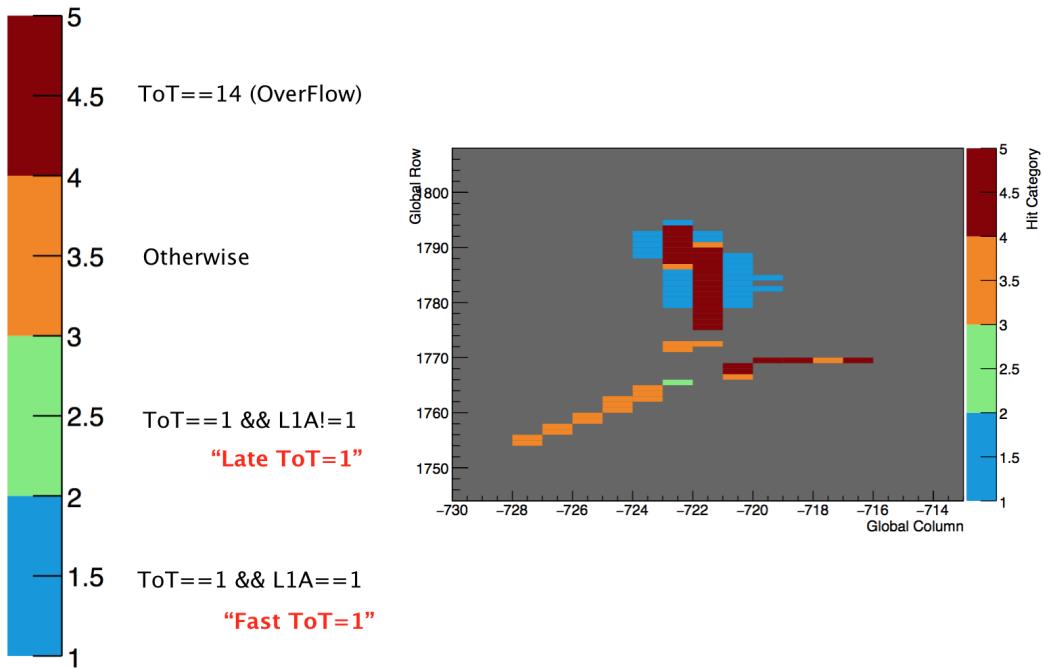


Figure 19: Legends explaining the hit map of the IBL for Figure 20.

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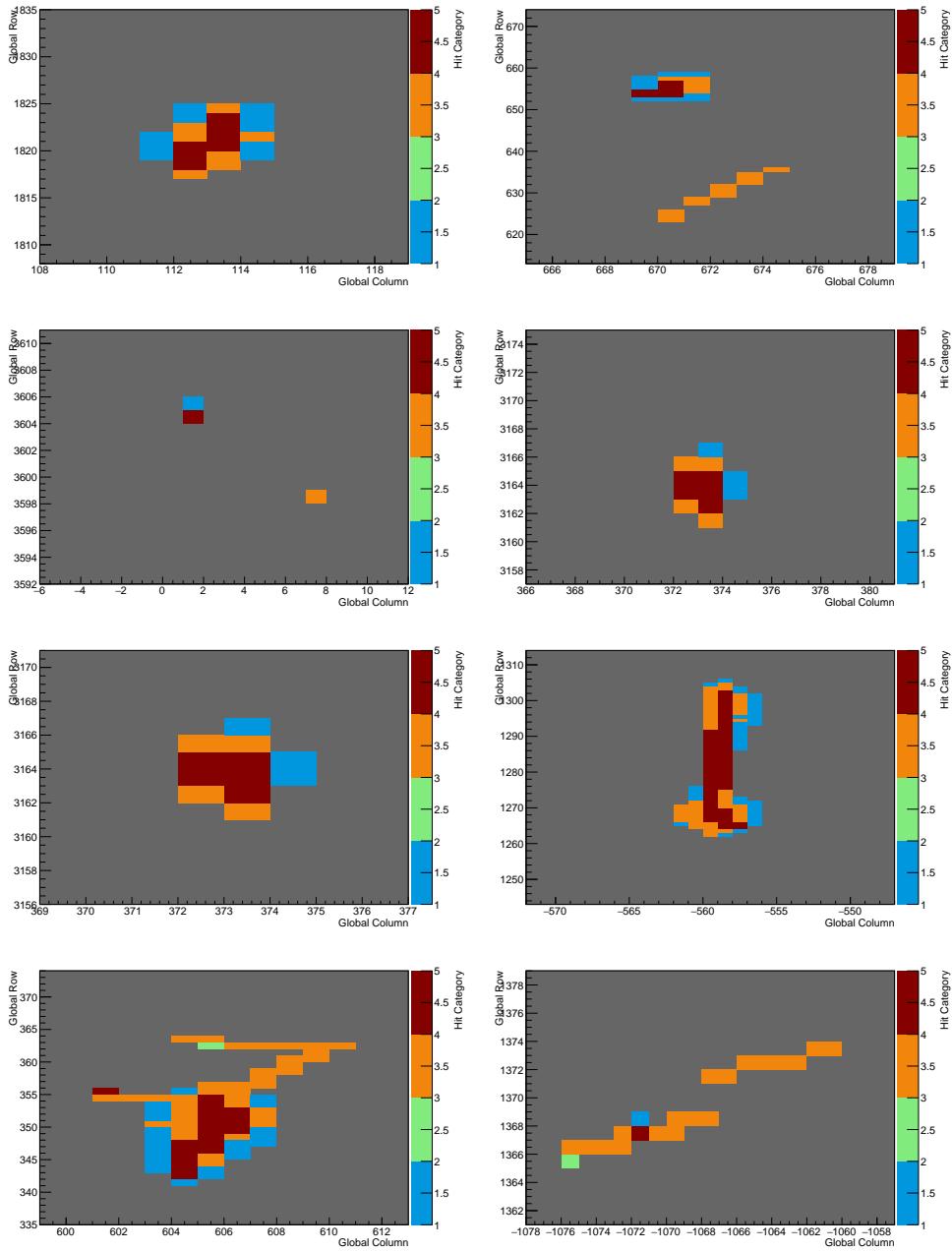


Figure 20: Examples of the IBL hit map with having fast ToT=1 hits in the data.

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553 Joern Grosse-Knetter	DisVbn adjustment development.
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