



γ tty2l dr1 all syst SR2 Truth bin 4 SR2 bin 0003
 γ tty2l dr1 all syst SR2 Truth bin 3 SR2 bin 0002
 γ tty2l dr1 all syst SR1 Truth bin 3 SR1 bin 0002
 γ tty2l dr1 all syst SR1 Truth bin 2 SR1 bin 0001
 γ tty2l dr1 all syst SR1 Truth bin 1 SR1 bin 0000
 γ SR2 bin 0006
 γ SR2 bin 0005
 γ SR2 bin 0004
 γ SR2 bin 0003
 γ SR2 bin 0002
 γ SR2 bin 0001
 γ SR2 bin 0000
 γ SR1 bin 0006
 γ SR1 bin 0005
 γ SR1 bin 0004
 γ SR1 bin 0003
 γ SR1 bin 0002
 γ SR1 bin 0001
 γ SR1 bin 0000