

Global: Do not use hyphen for "minus" sign.

Global: Do not use apostrophe for prime sign.

Figure 1-1

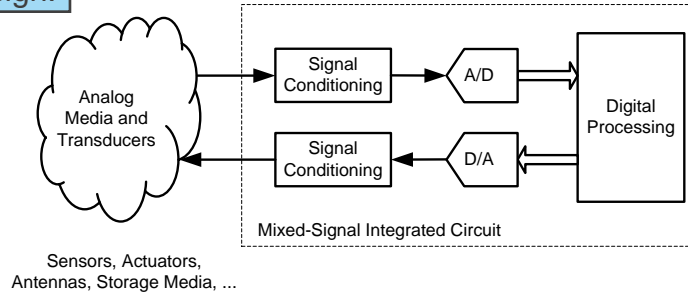
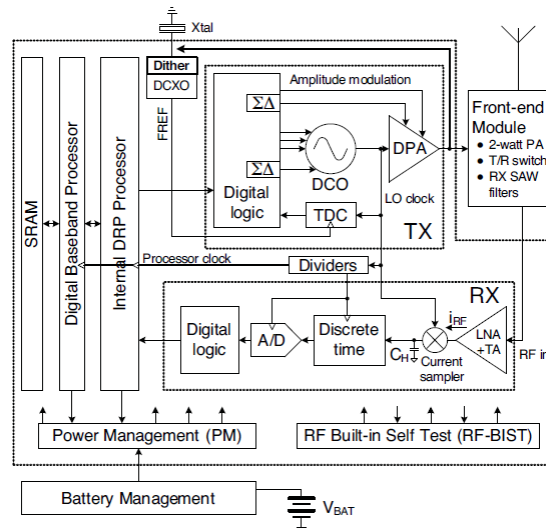


Figure 1-2



Use title case for component labels.

This figure is taken from an IEEE publication and should not be modified.

Figure 1-3

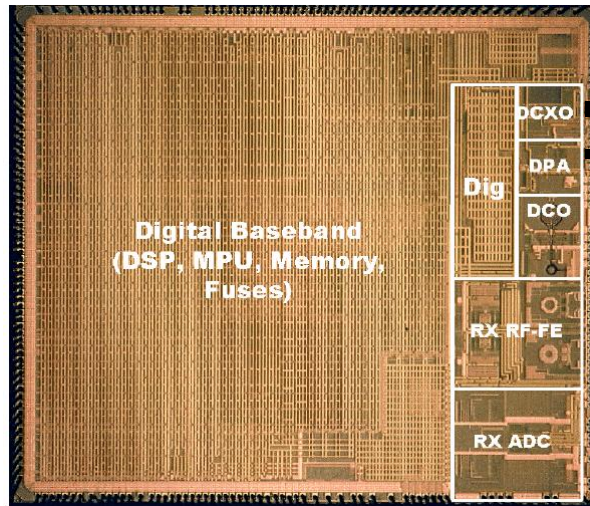
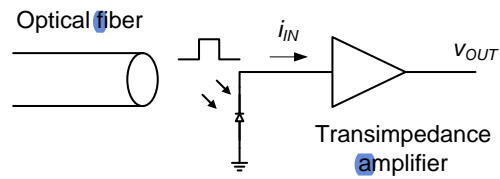


Figure 1-4



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Figure 1-5

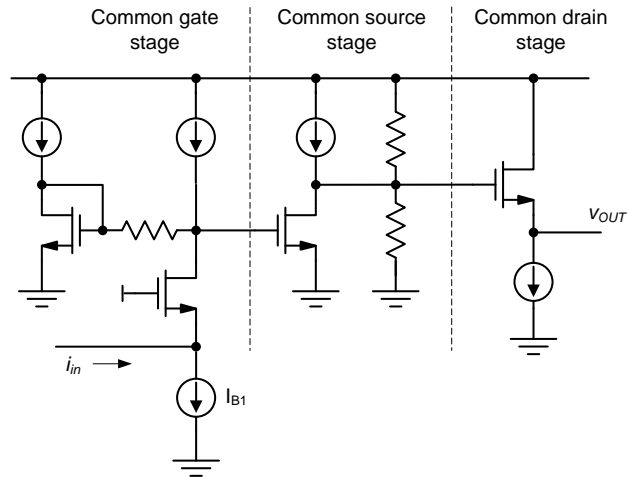


Figure 1-6

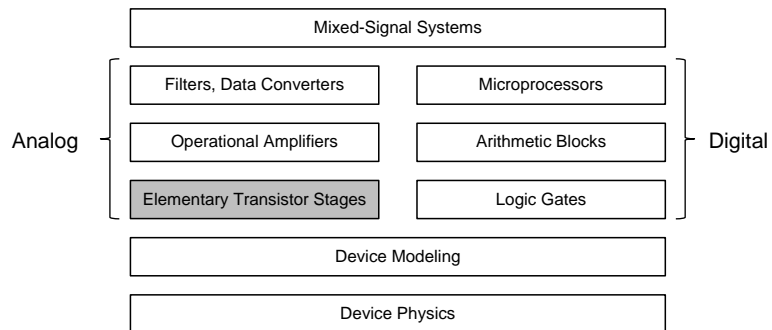


Figure 1-7

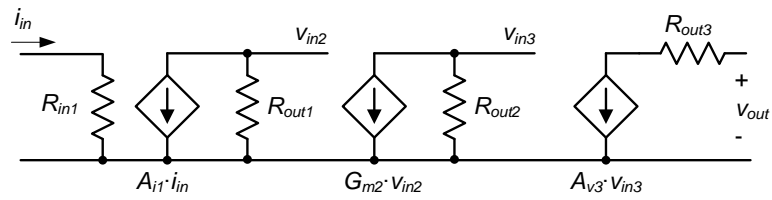


Figure 1-8

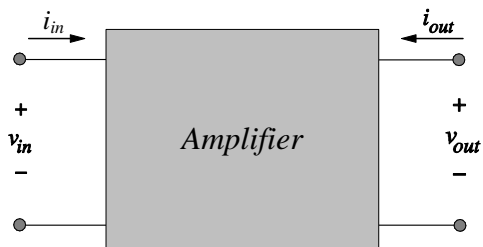
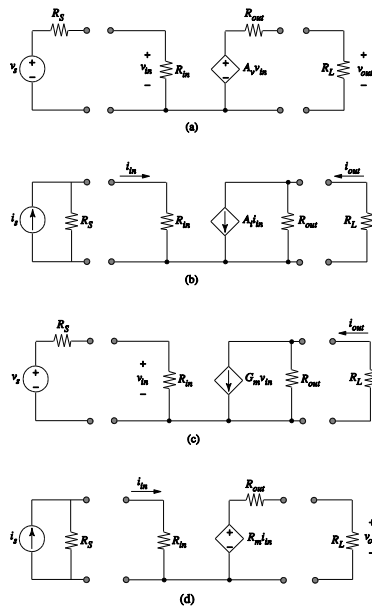


Figure 1-9



(Howe & Sodini, Figure 8.2)

Figure 1-10

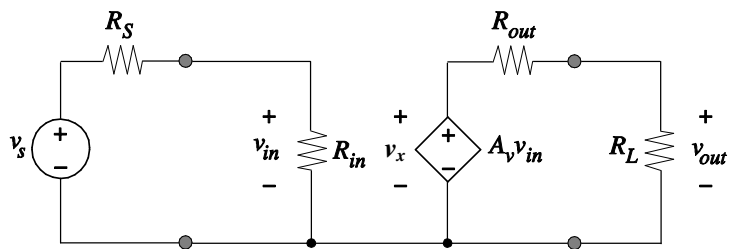
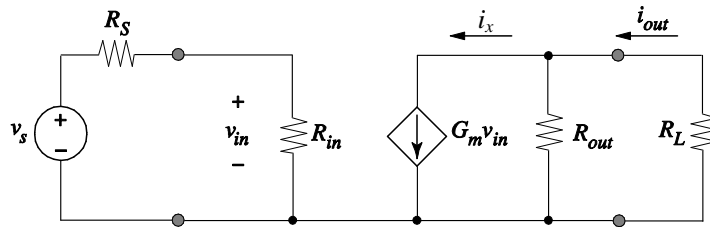


Figure Ex1-1



(Howe & Sodini, Figure 8.5)

Figure 1-11

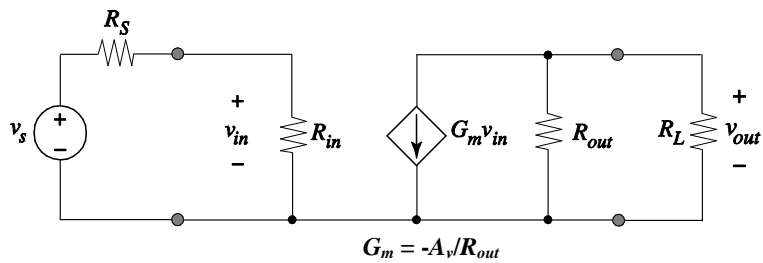


Figure 1-12

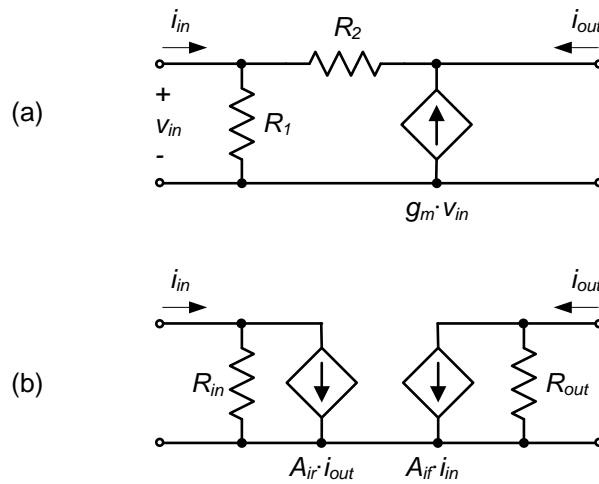
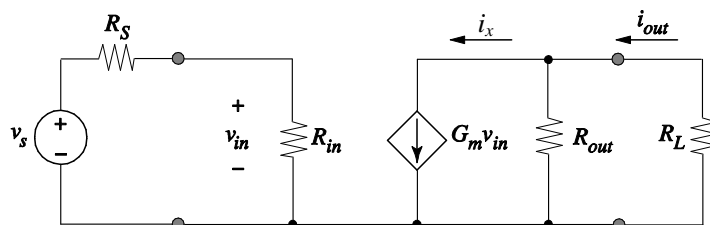


Figure Ex1-1



(Howe & Sodini, Figure 8.5)

Figure 1-13

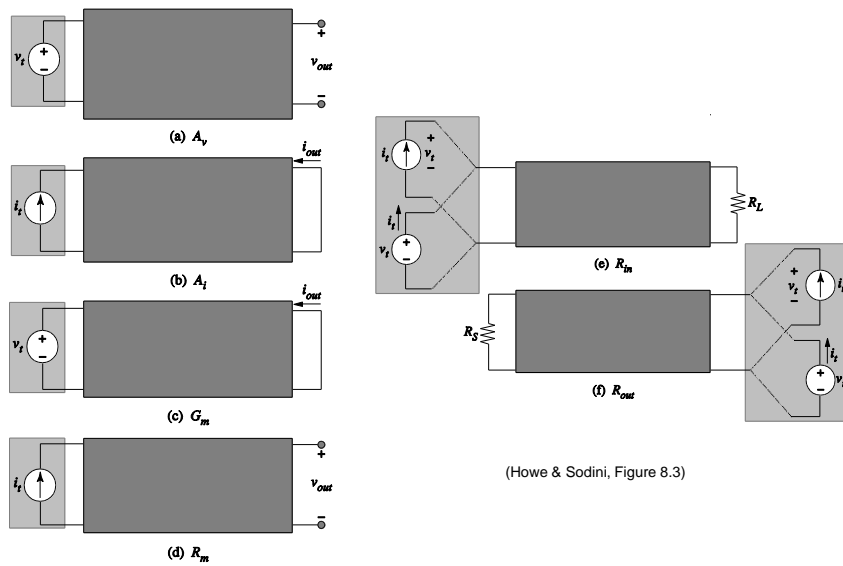
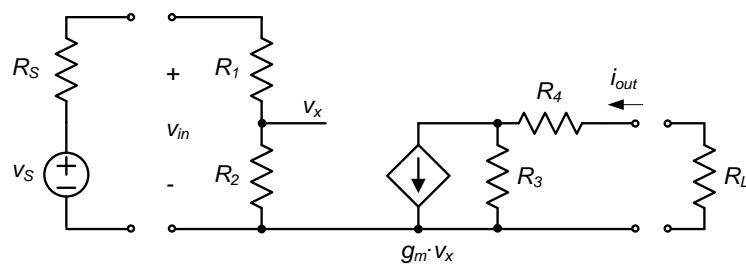
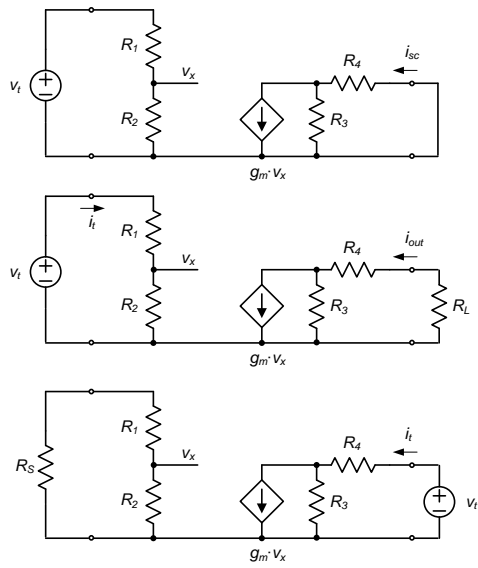


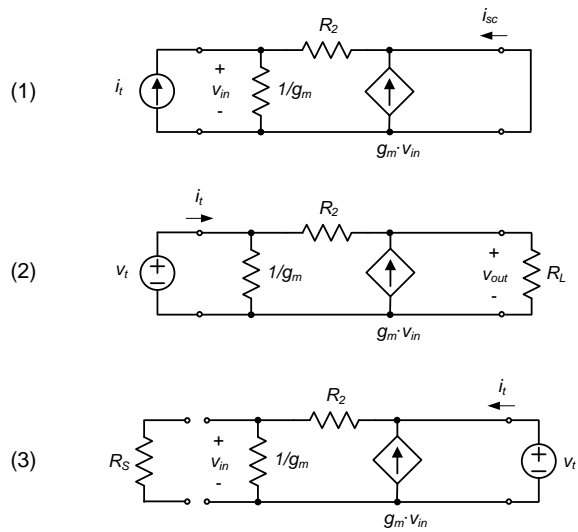
Figure Ex1-2



Ex1-2 (Solution)



Ex1-3 (Solution)



Ex1-3 (Solution)

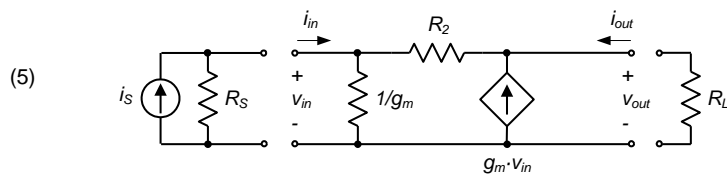
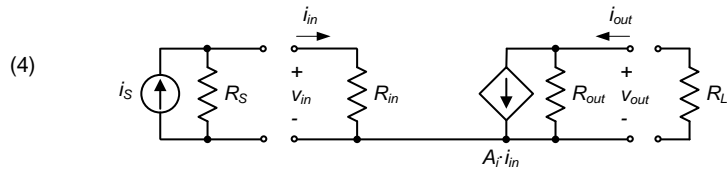


Figure 1-14

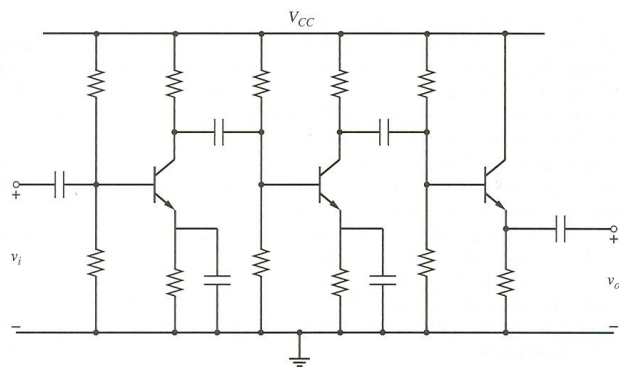


Figure P1-1

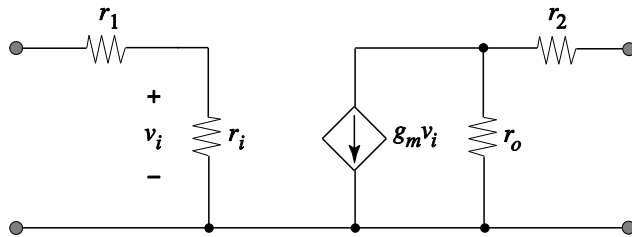


Figure P1-5

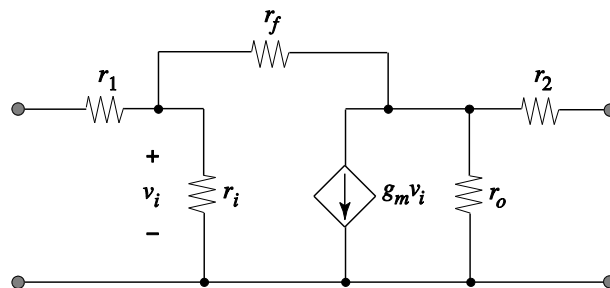


Figure 2-1

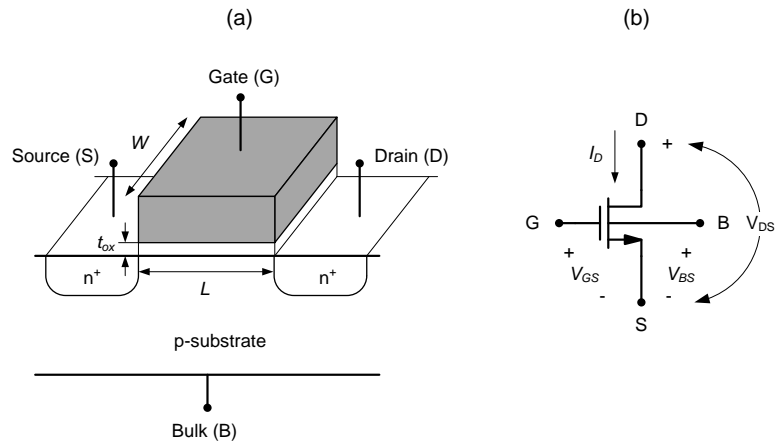


Figure 2-2

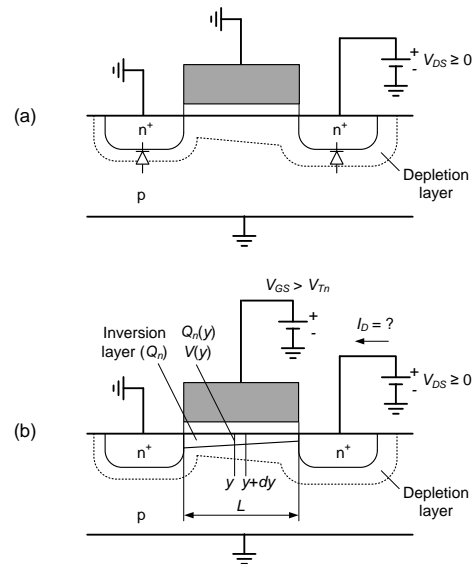


Figure 2-3

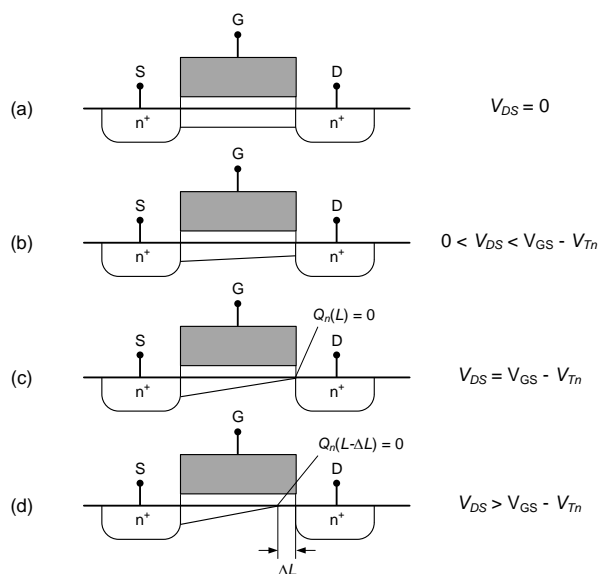


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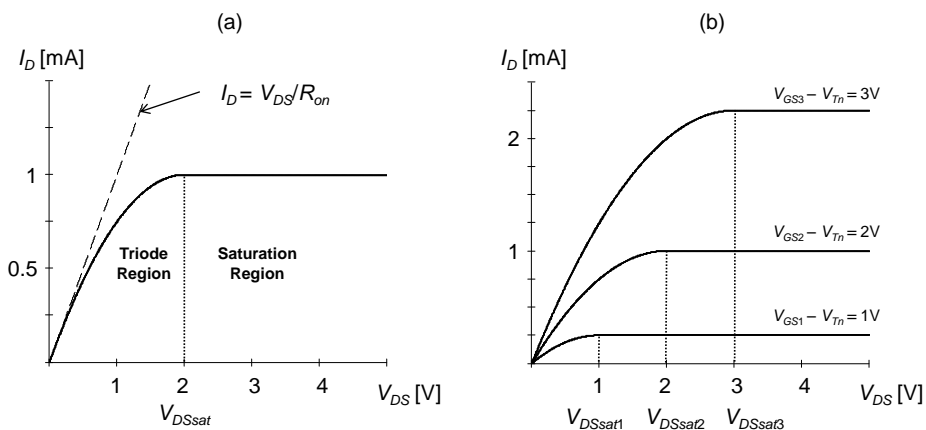


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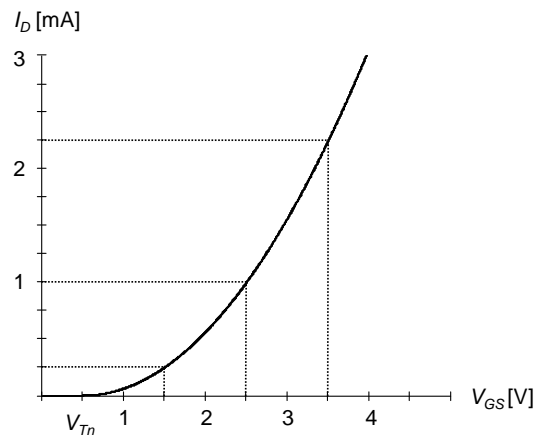


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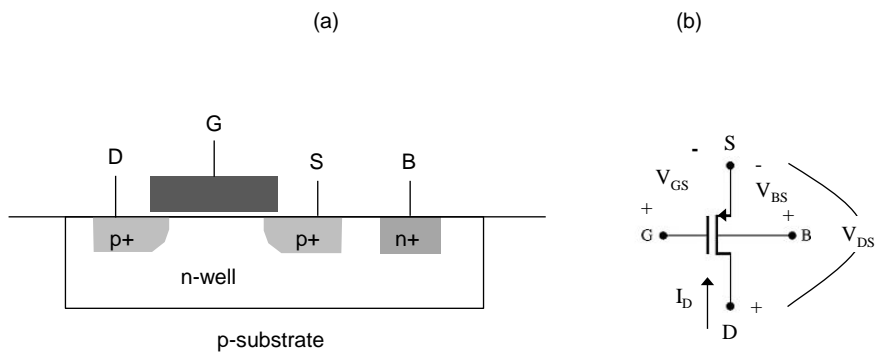


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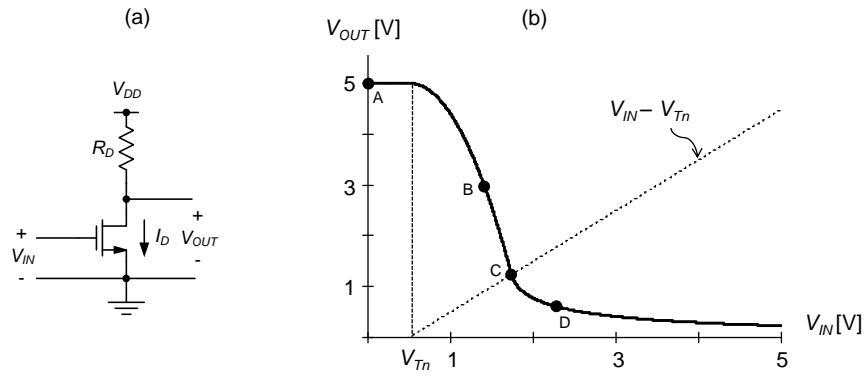
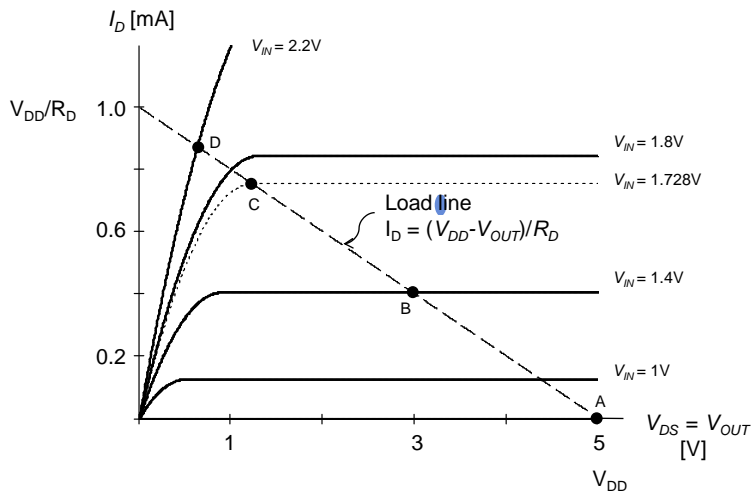


Figure 2-8



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Figure Ex2-3

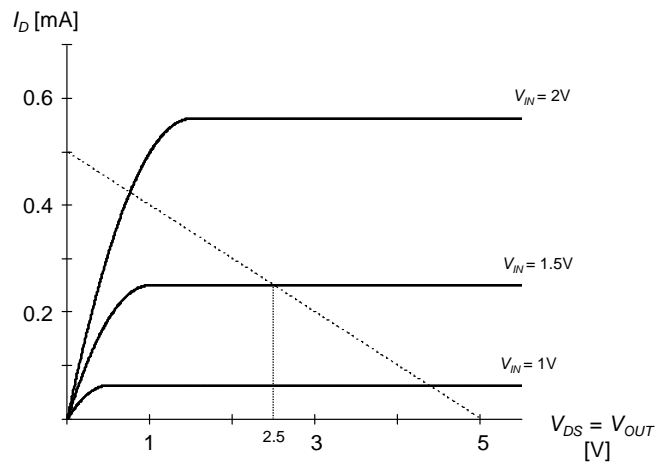


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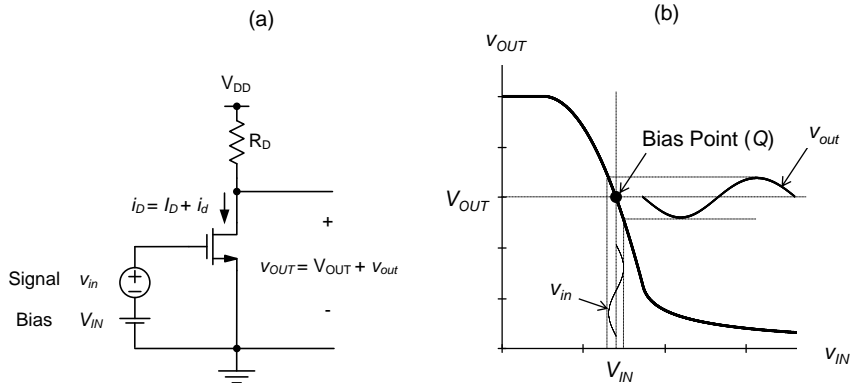


Figure 2-10

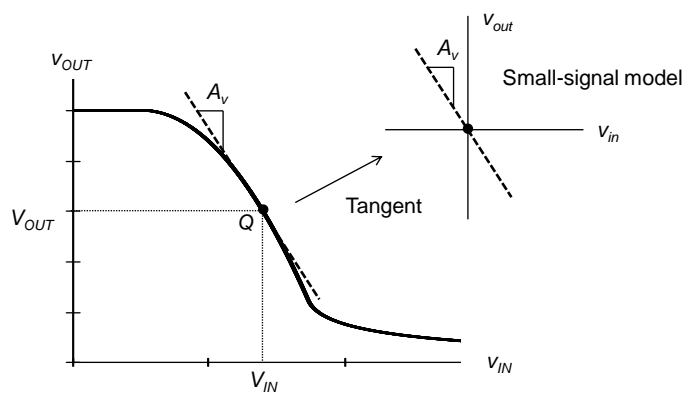


Figure 2-11

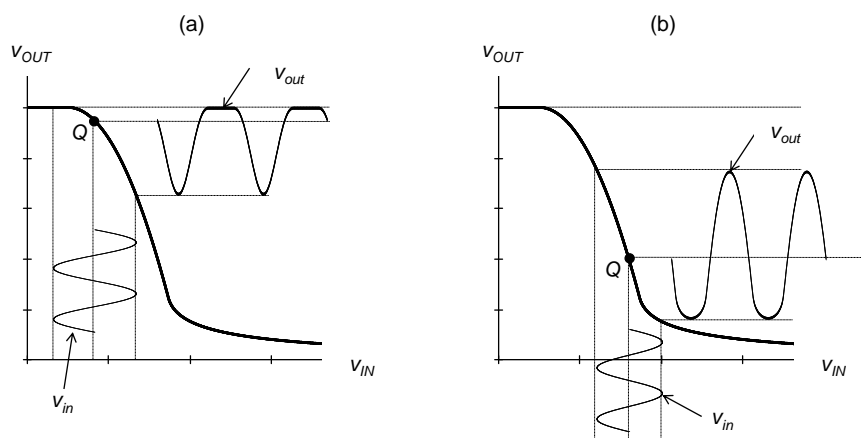


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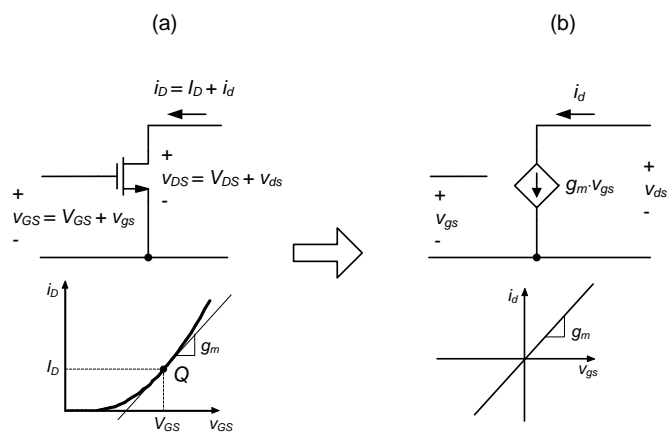


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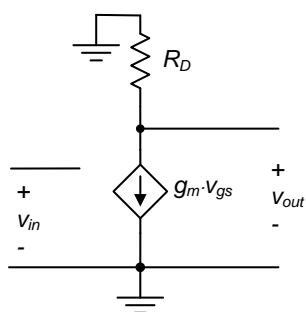


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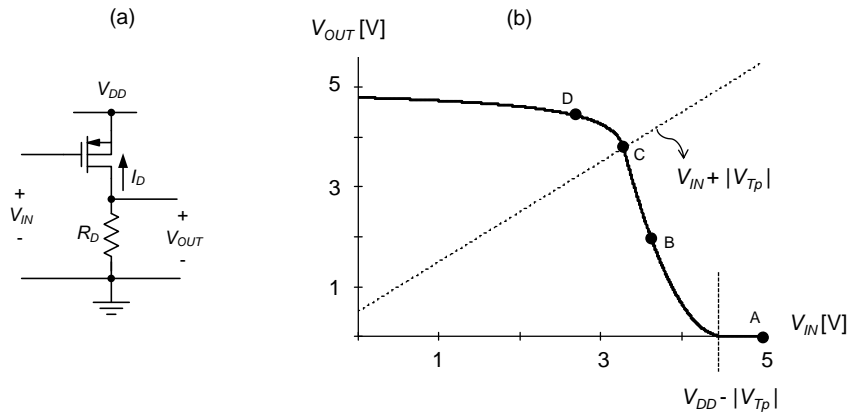


Figure 2-15

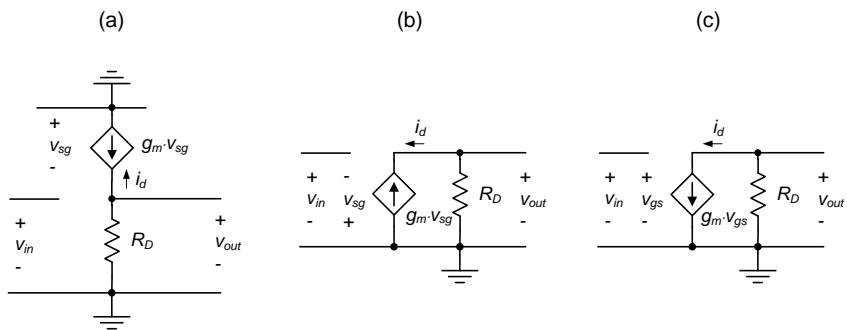


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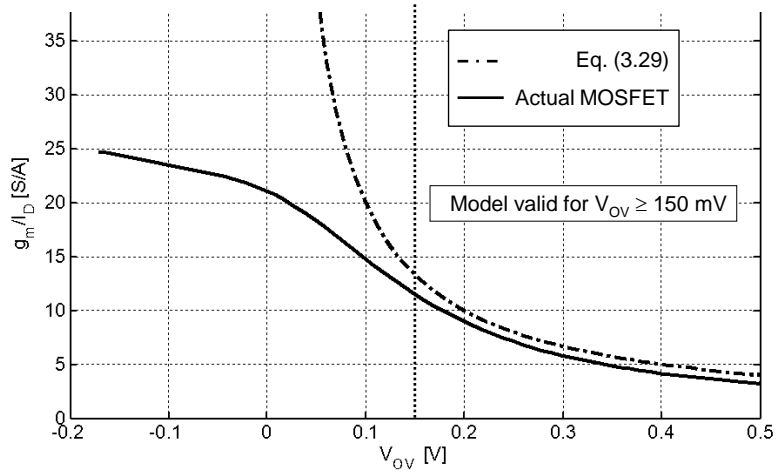


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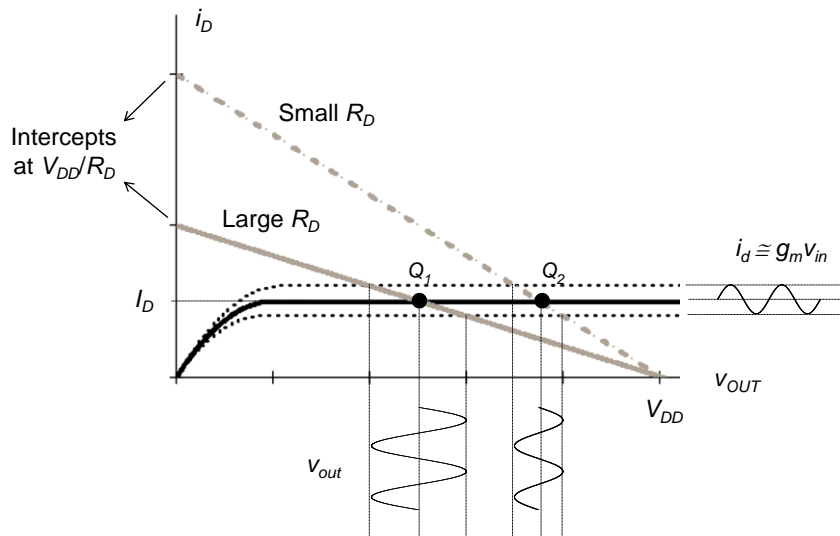


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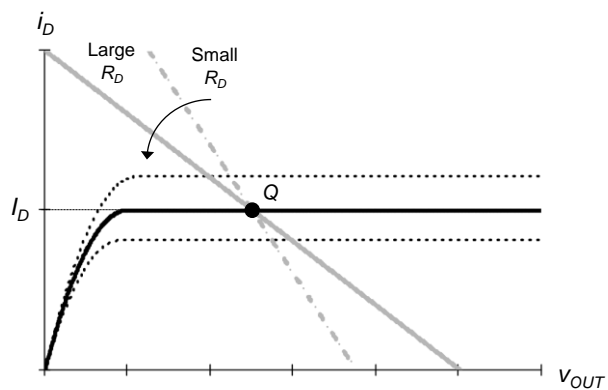


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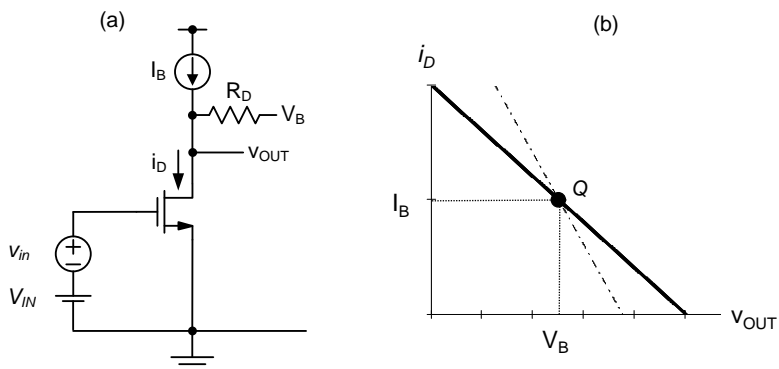


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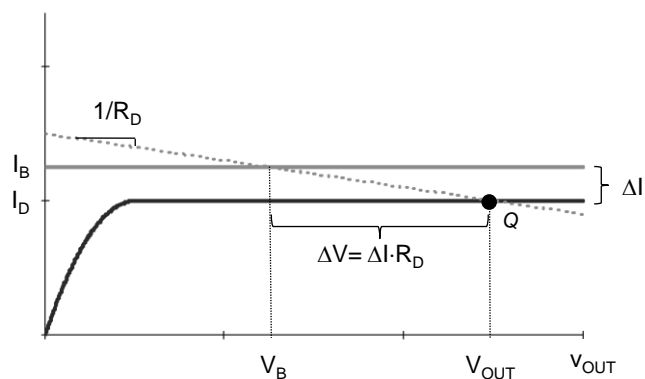


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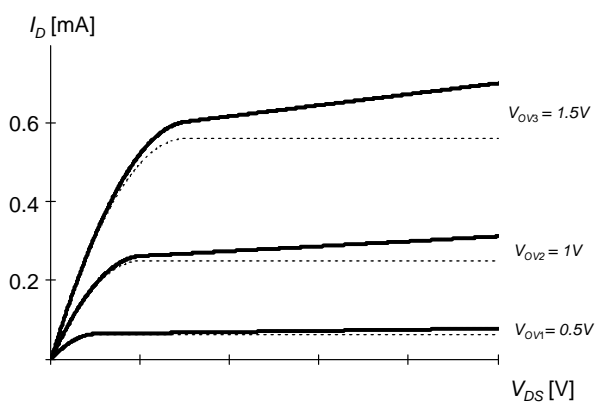


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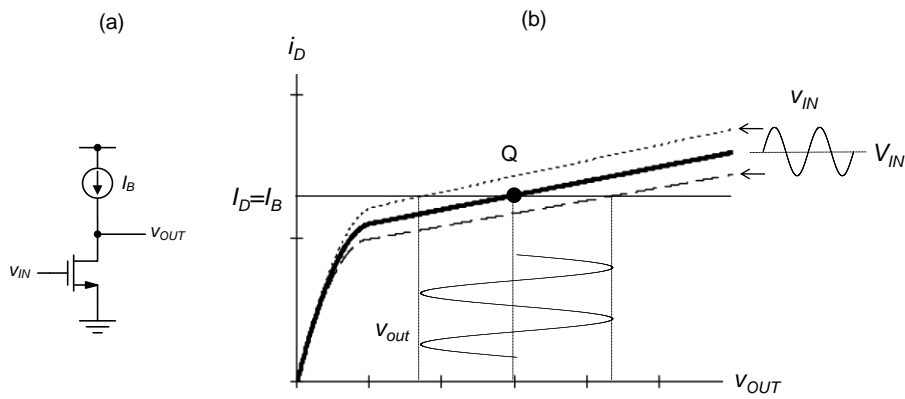


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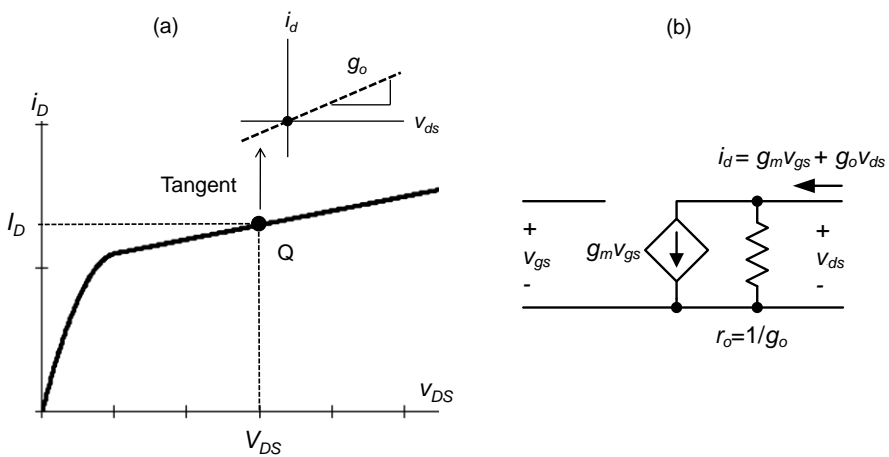


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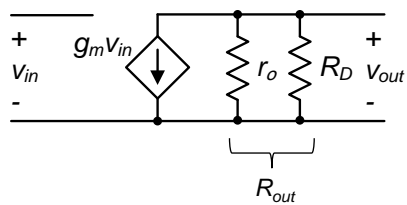


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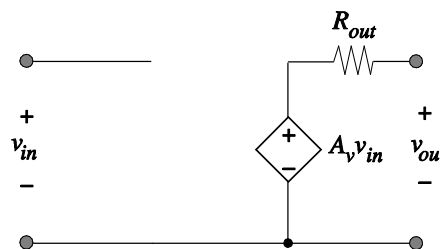


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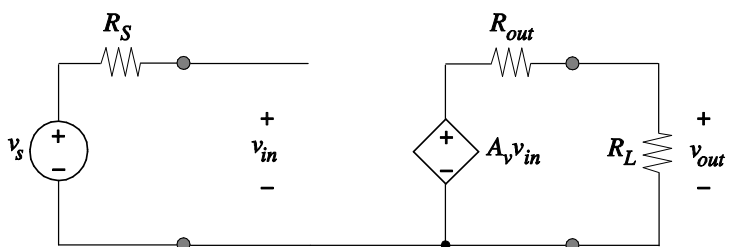
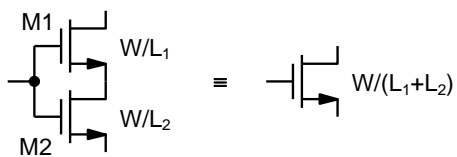
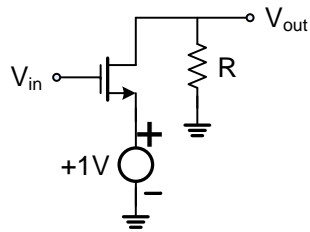


Figure P2-2



Italicize variables.

Figure P2-5



Italicize variables.

Figure P2-12

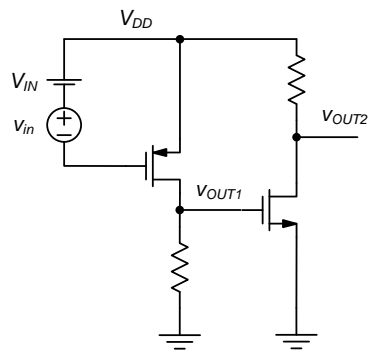
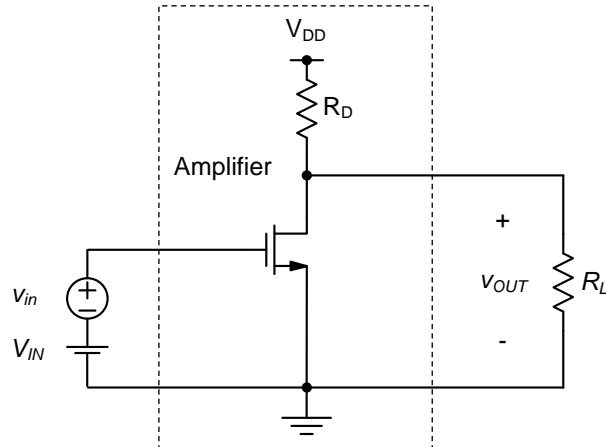


Figure P2-17



Italicize variables.

Figure 3-1

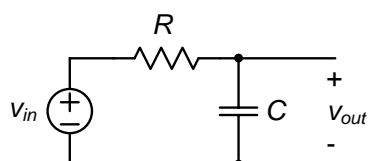
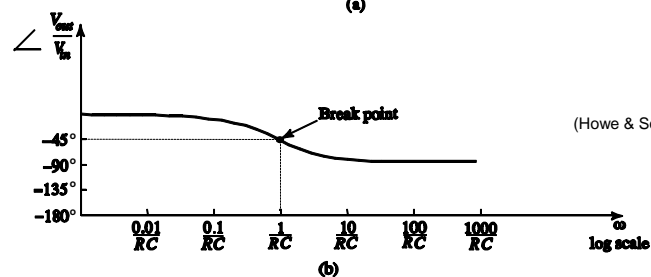
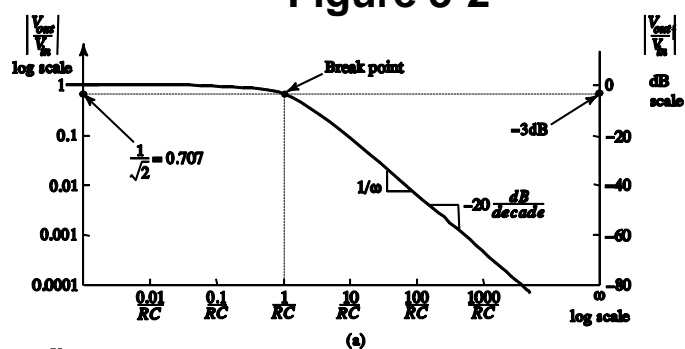


Figure 3-2



(Howe & Sodini, Figure 10.2)

Figure 3-3

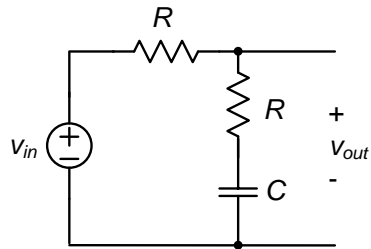


Figure Ex3-2

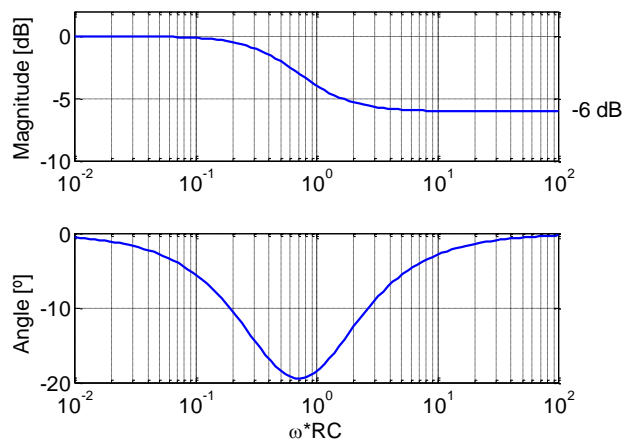


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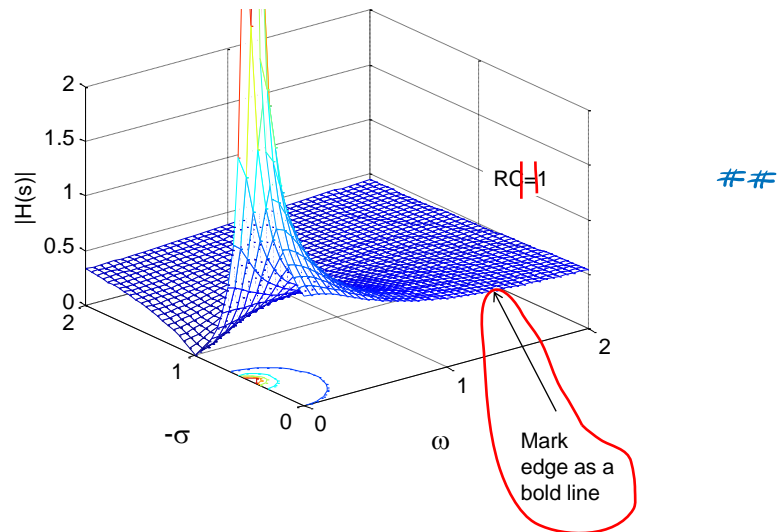


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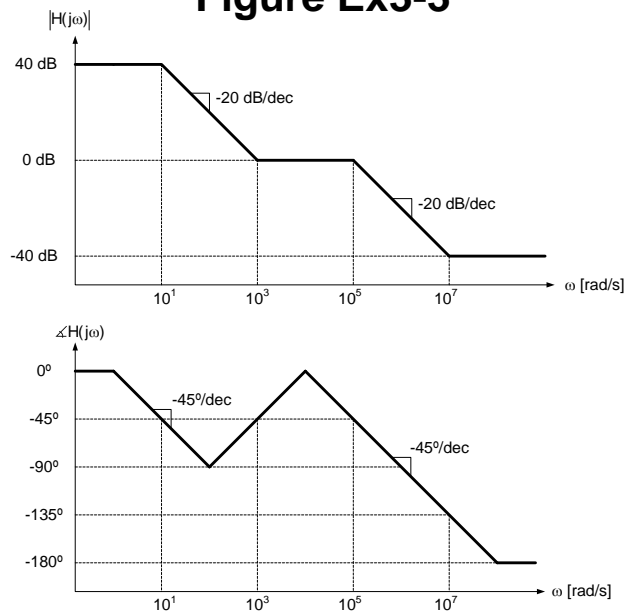


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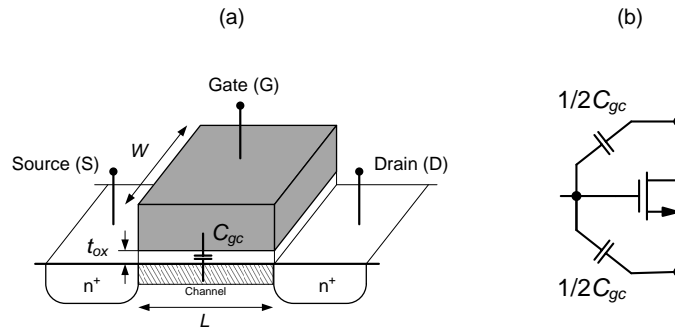
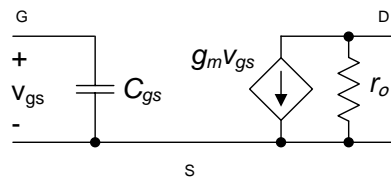


Figure 3-6



Italicize variables.

Figure 3-7

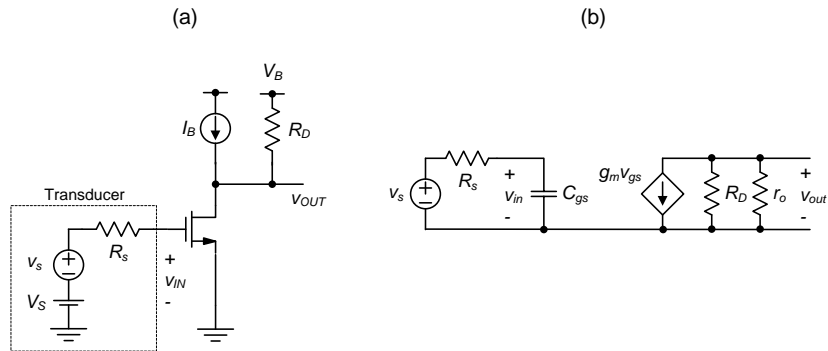


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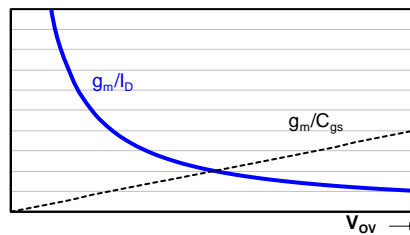


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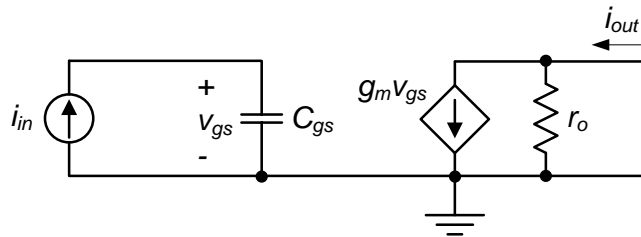
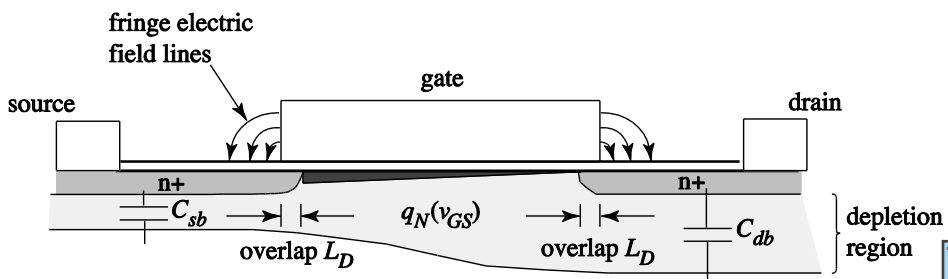


Figure 3-10



(Howe & Sodini, Figure 4.23)

Title-case labels

Figure 3-11

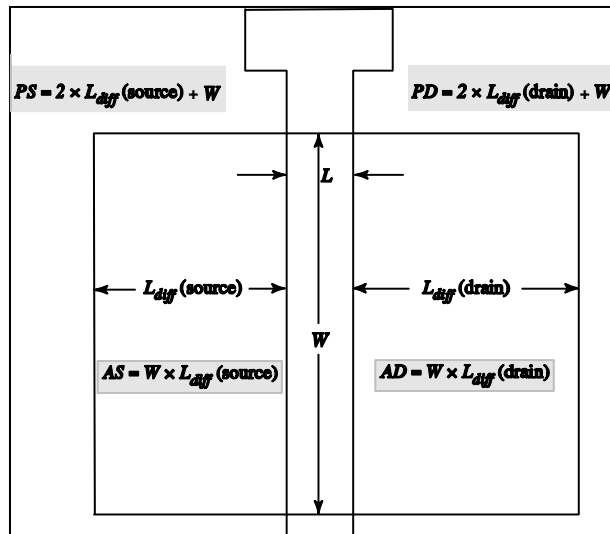


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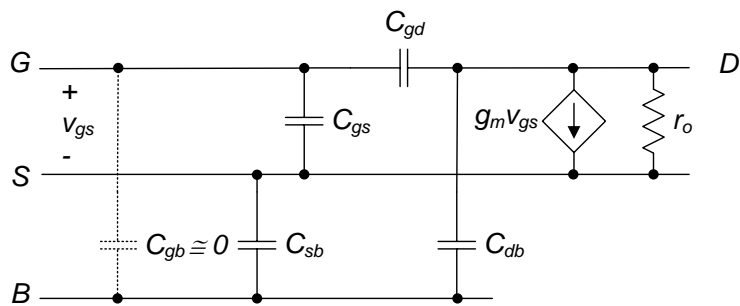


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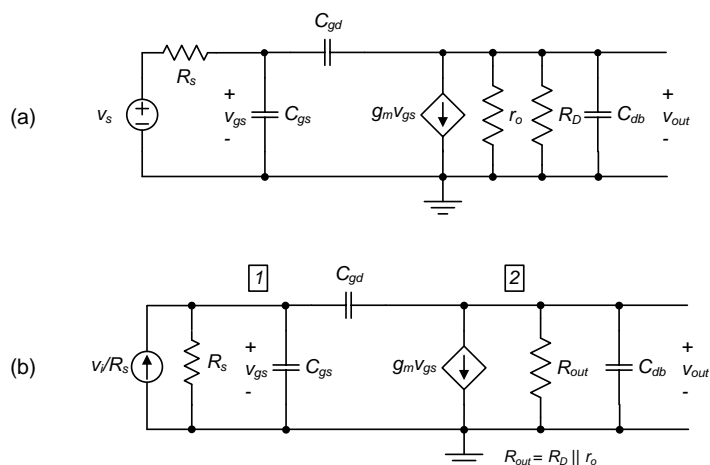


Figure Ex3-6

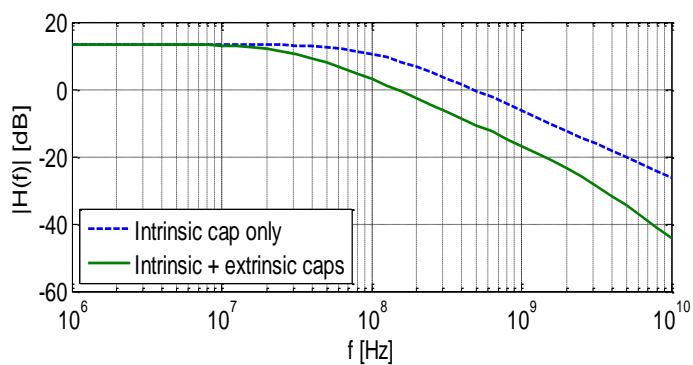


Figure 3-14

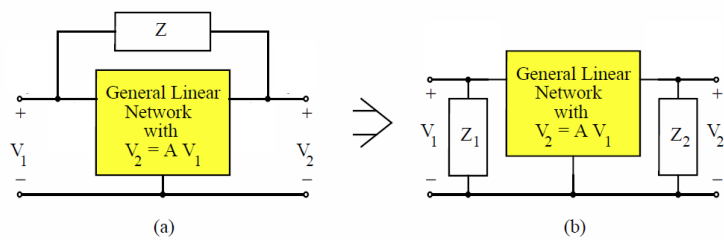


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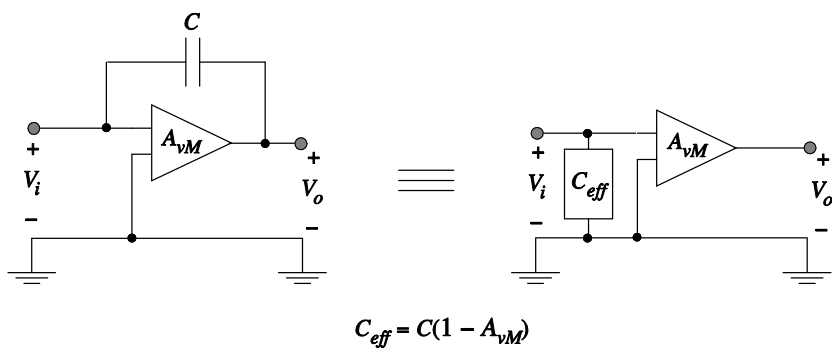


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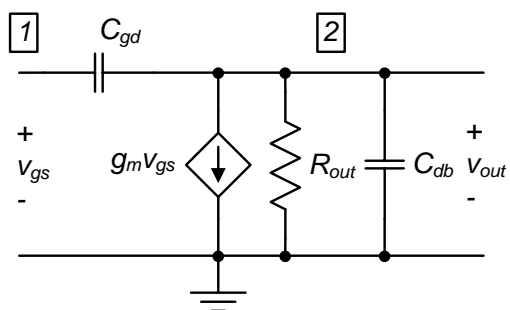


Figure 3-17

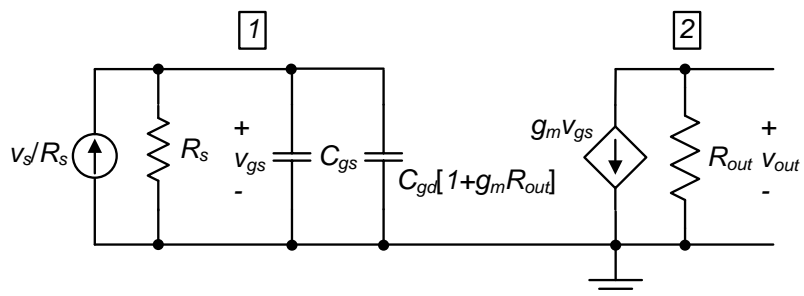


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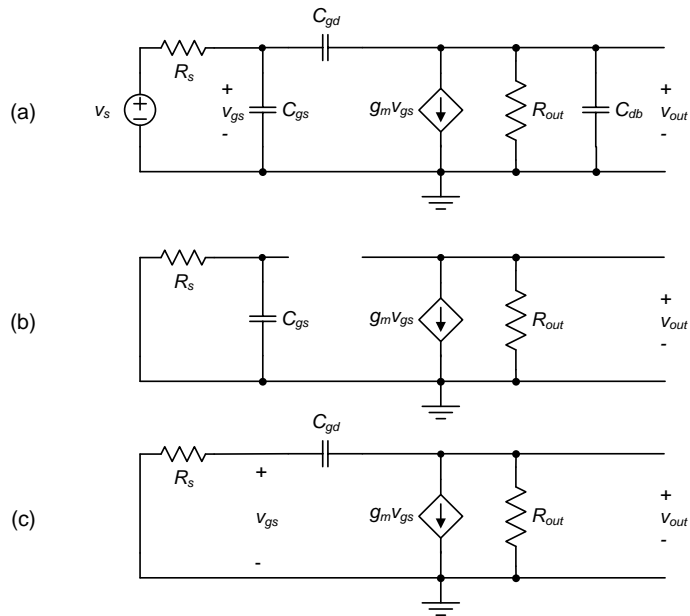


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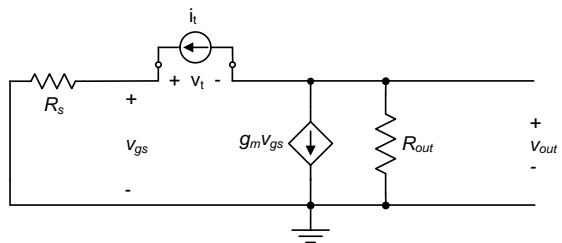


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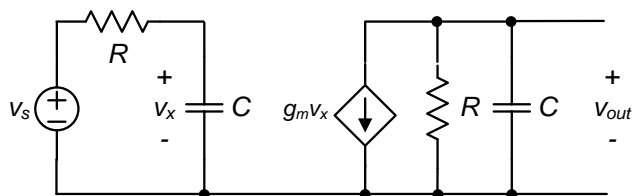


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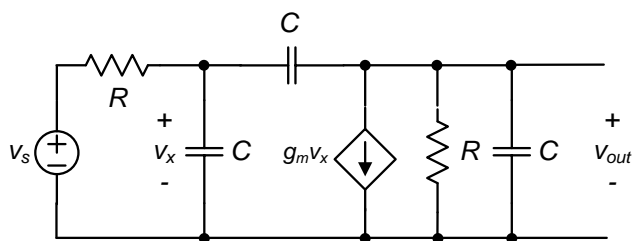


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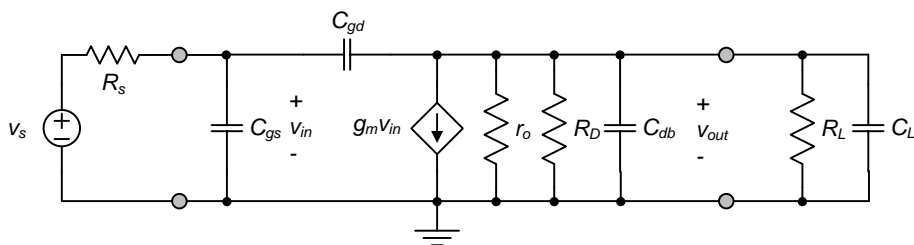


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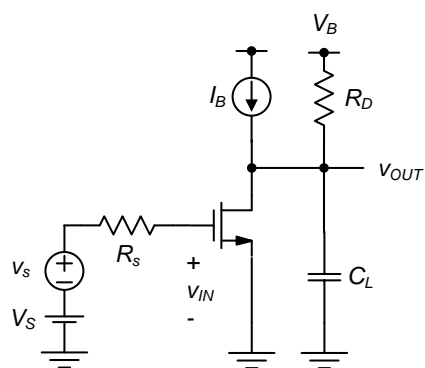


Figure P3.3

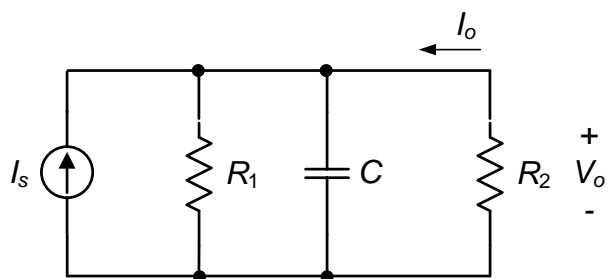
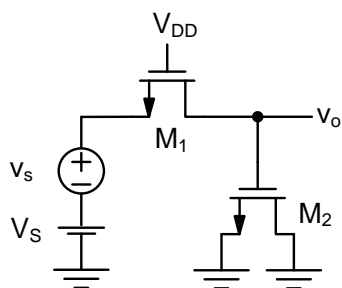


Figure P3.7



Italicize variables.

Figure P3-13

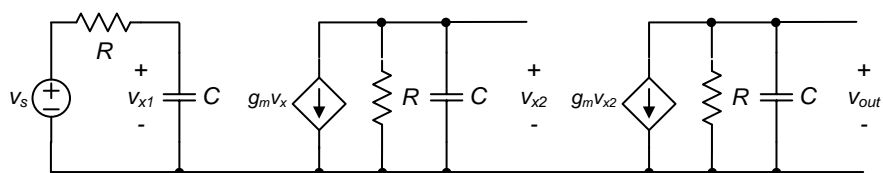


Figure P3-16

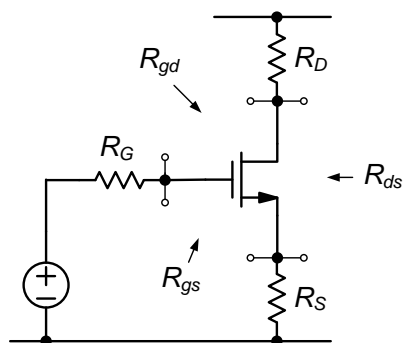


Figure P3-17

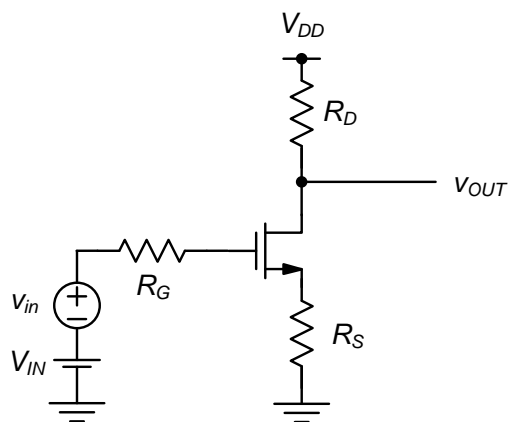


Figure 4-1

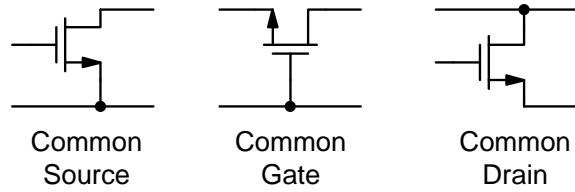
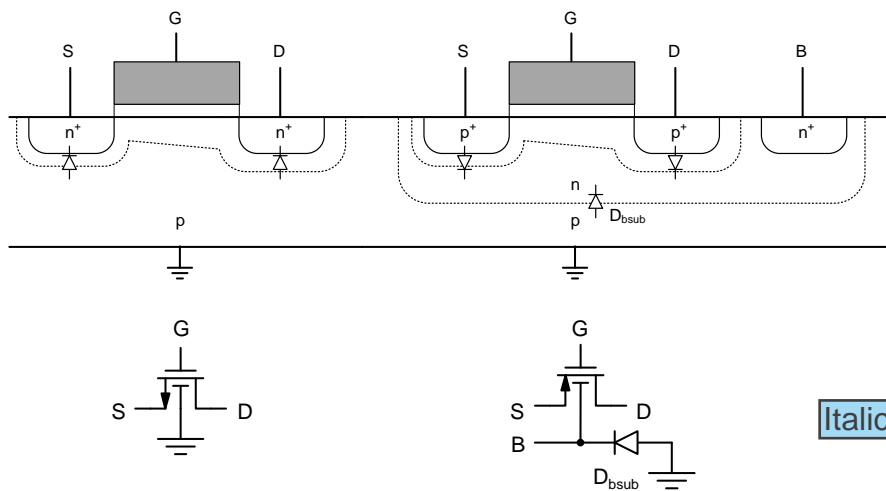
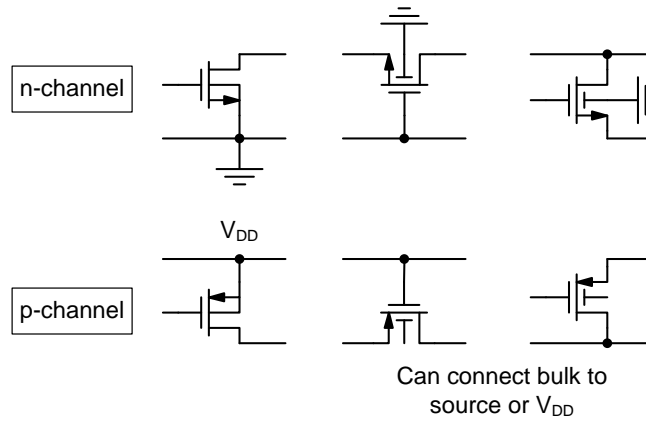


Figure 4-2



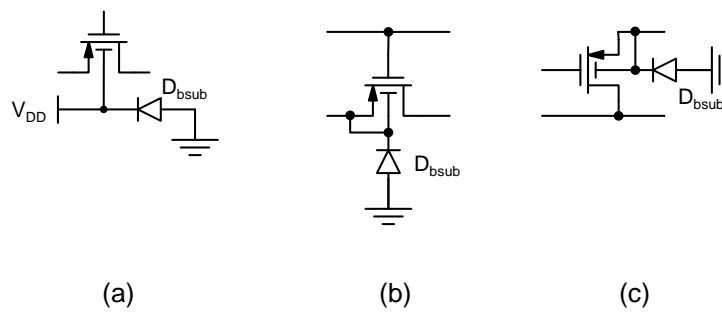
Italicize variables.

Figure 4-3



Italicize variables.

Figure 4-4



Italicize variables.

Figure Ex4-1

The diagram illustrates a well system within a rectangular boundary. On the left, a well is shown with a central gravel pack (G) of length L and two side filter zones (S and D) each of length L_{diff} . The total width of this well assembly is W . The distance from the left boundary to the start of the filter zone is $X1$, and the distance between the two filter zones is $X2$. To the right, a well contact is shown as a vertical rectangle of width $X1$ and height $X1$. The distance from the right boundary to the well contact is also $X1$.

Figure 4-5

The diagram illustrates the effect of source-bias voltage V_{SB} on the depletion layer of a MOSFET. The device is shown with a gate voltage V_{GS} , a drain-source voltage V_{DS} , and a drain current I_D . The source terminal is connected to a voltage source V_{SB} relative to the body. Two depletion layer profiles are shown: a solid line for $V_{SB} = 0$ and a dashed line for $V_{SB} > 0$. The dashed line shows a wider depletion layer, indicating that the depletion layer width increases with V_{SB} .

cap cap

Figure 4-6

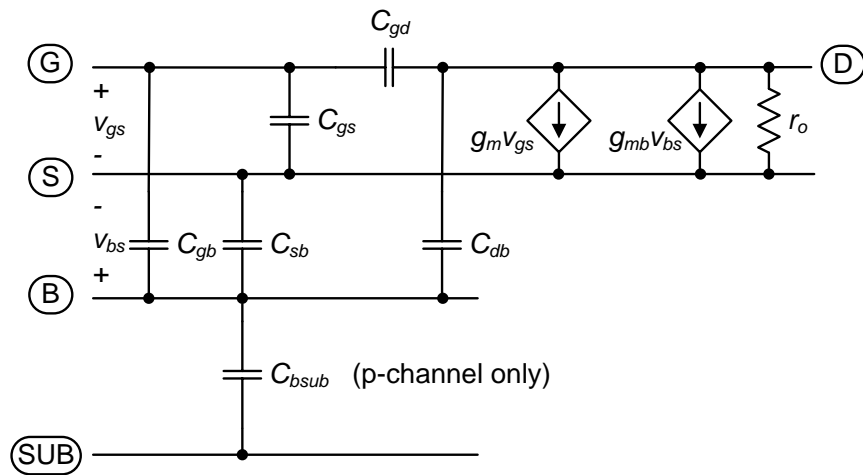


Figure 4-7

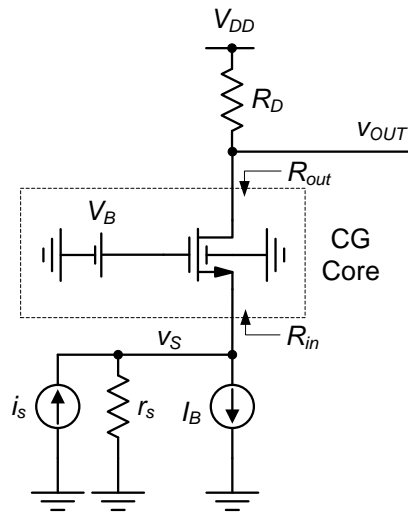


Figure 4-8

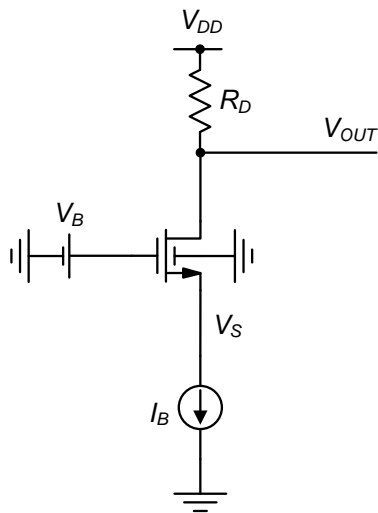


Figure 4-9

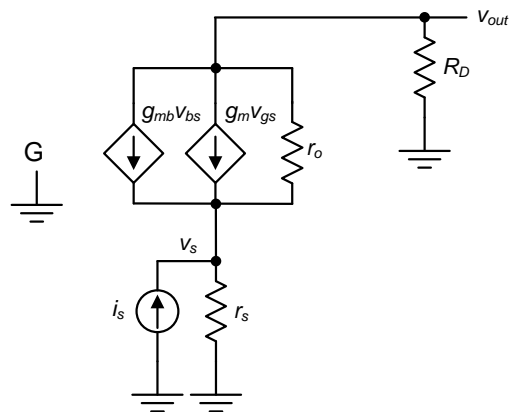


Figure 4-10

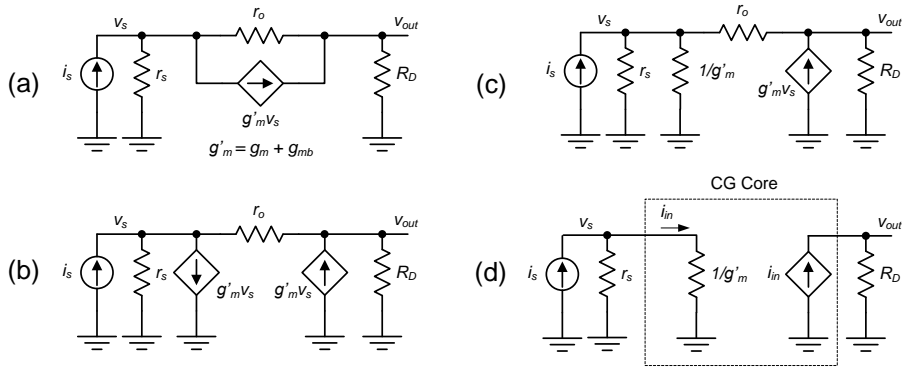


Figure 4-11

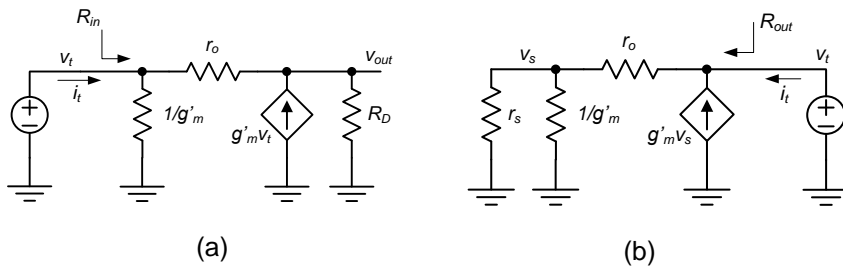


Figure 4-12

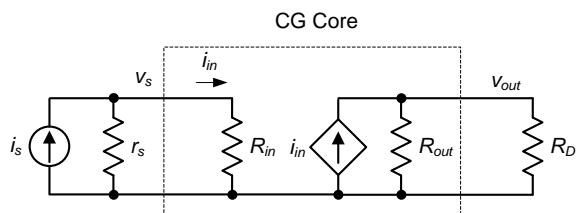


Figure 4-13

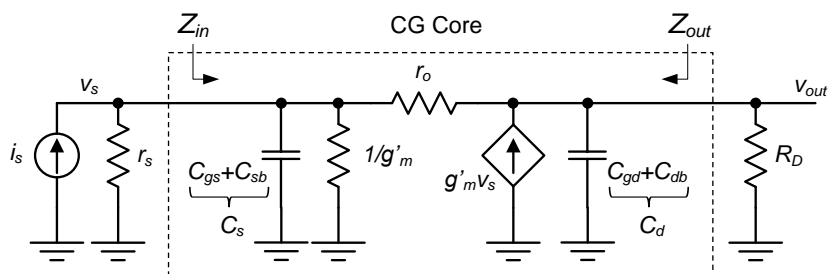


Figure 4-14

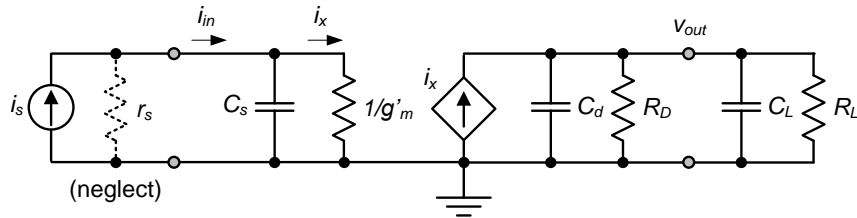
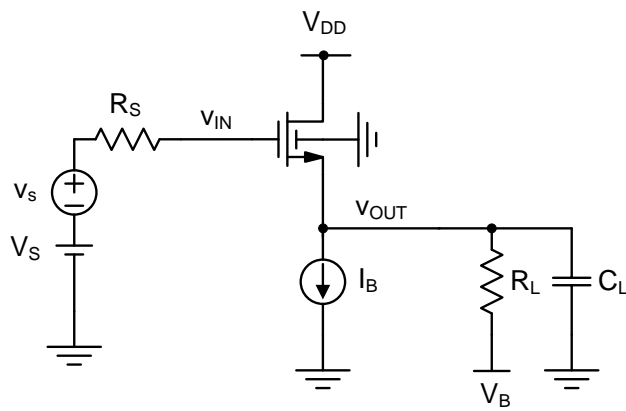


Figure 4-15



Italicize variables.

Figure 4-16

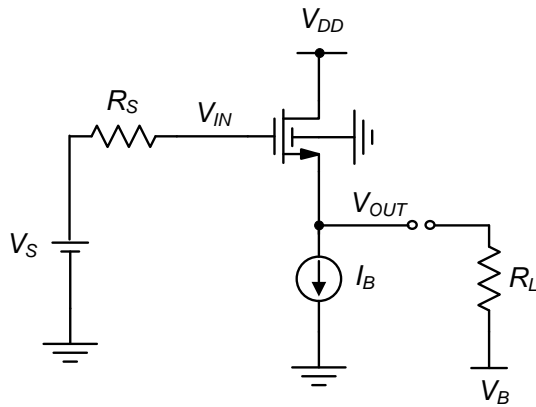
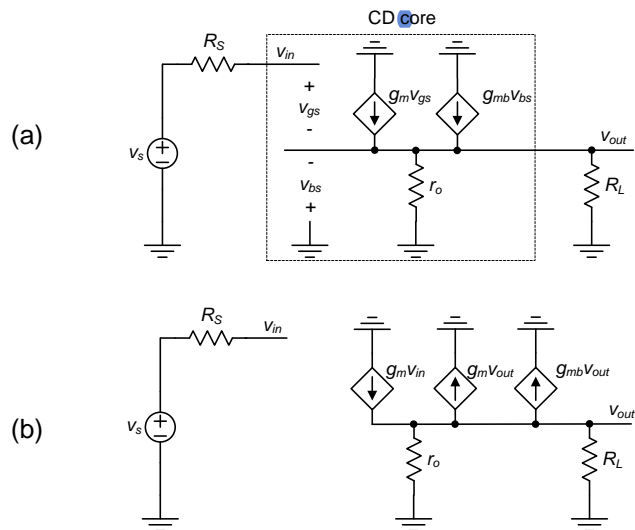


Figure 4-17



cap

Figure 4-17 (continued)

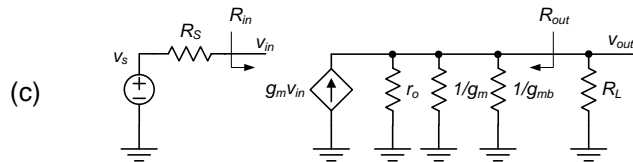


Figure 4-18

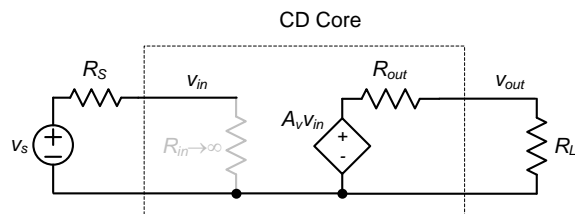


Figure 4-19

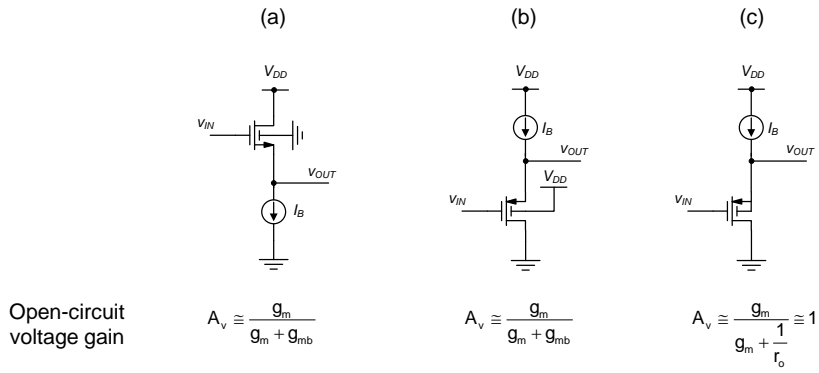


Figure Ex4-5

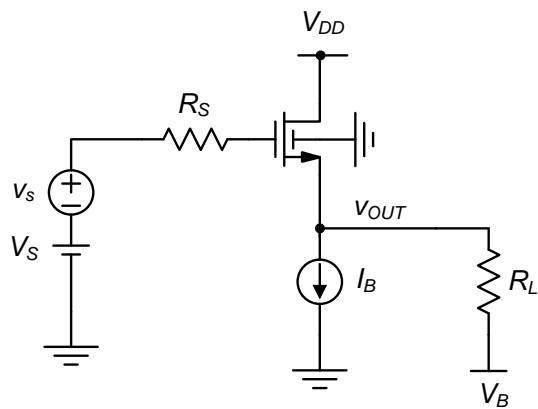


Figure 4-20

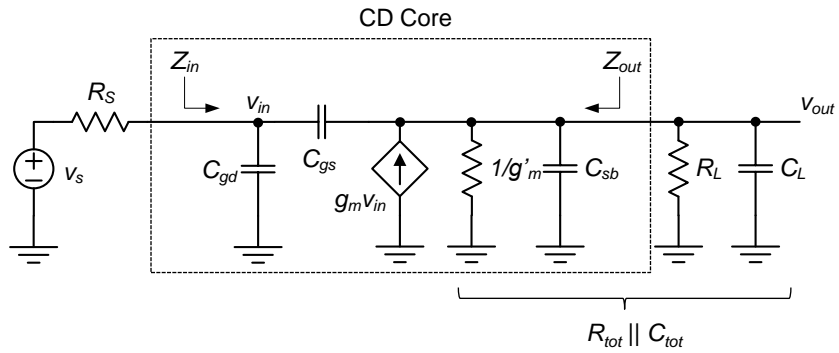


Figure 4-21

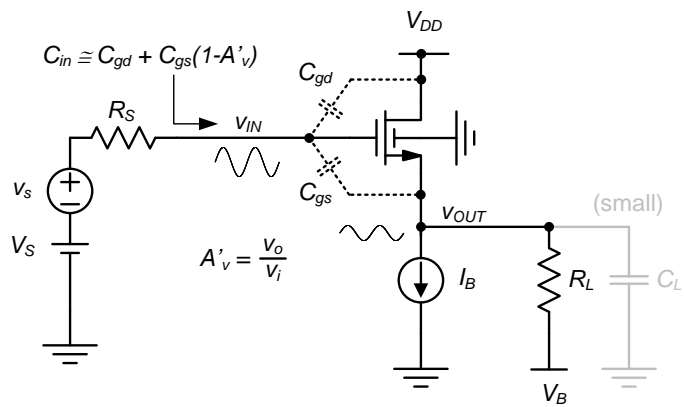


Figure 4-22

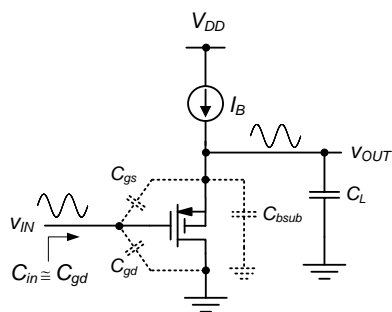


Figure 4-23

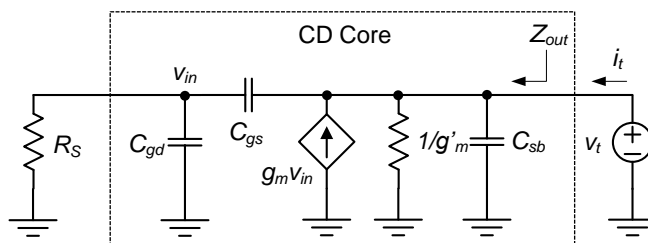


Figure 4-24

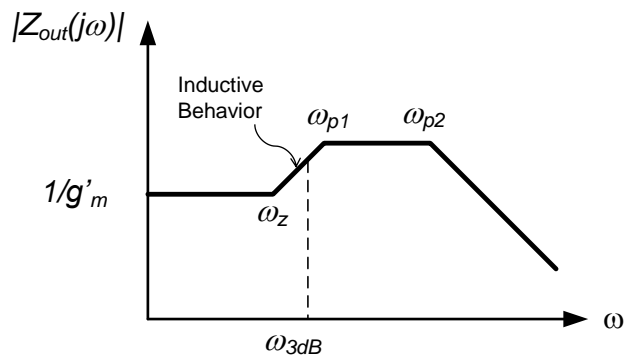


Figure 4-25

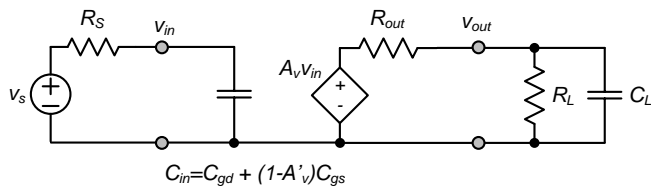
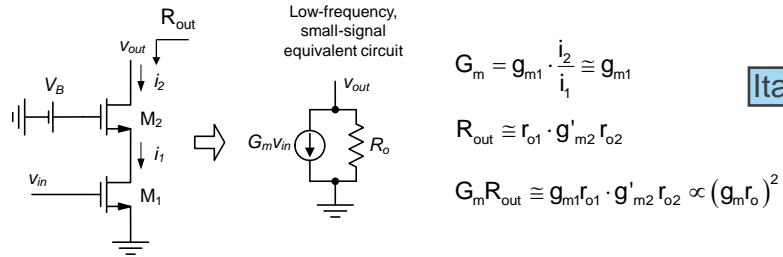
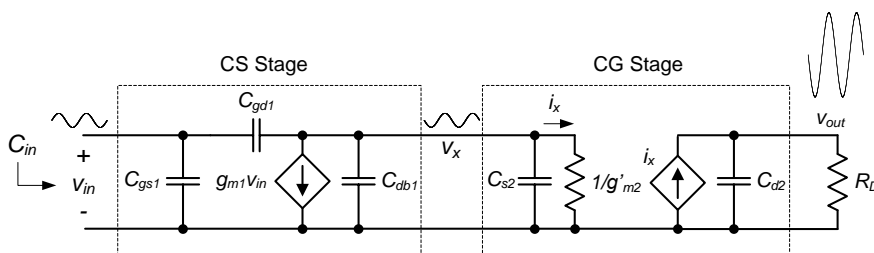


Figure 4-26



Italicize variables.

Figure 4-27



$$C_{in} \cong C_{gs1} + C_{gd1} (1 - A_{vM}) \quad A_{vM} \cong -\frac{g_{m1}}{g'_{m2}} \cong -1$$

$$\therefore C_{in} \cong C_{gs} + 2C_{gd}$$

Italicize variables.

Figure 4-28

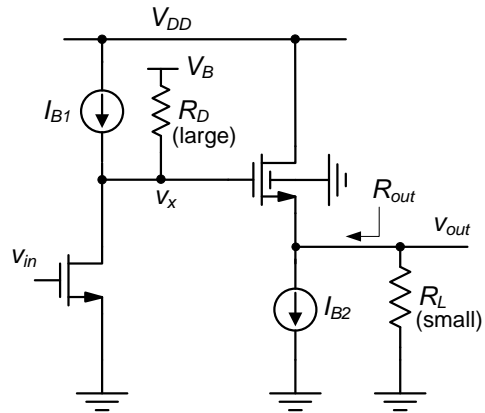
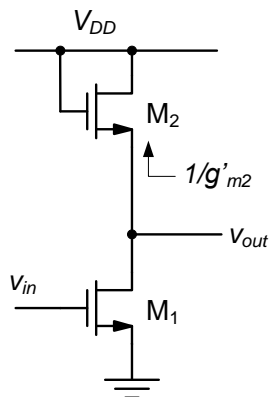


Figure 4-29



Italicize variables.

Figure 4-30

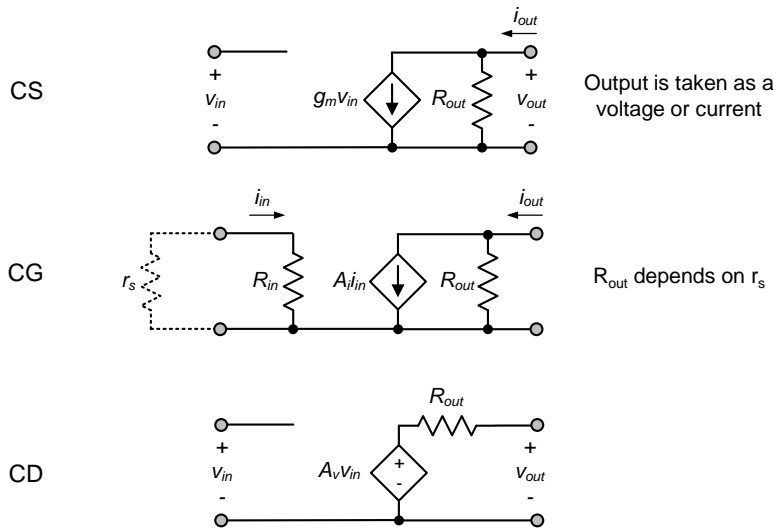


Figure P4.1

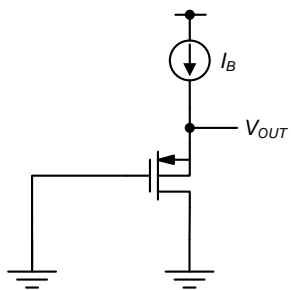


Figure P4.3

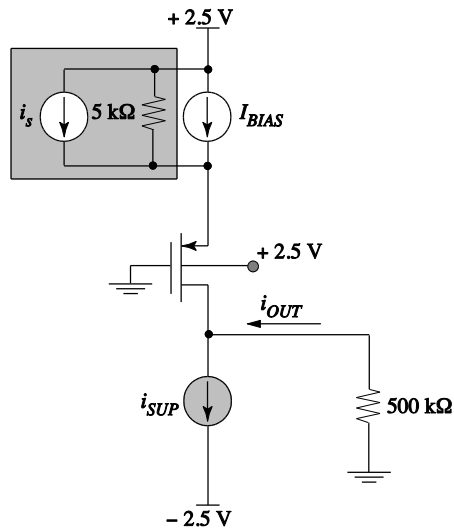
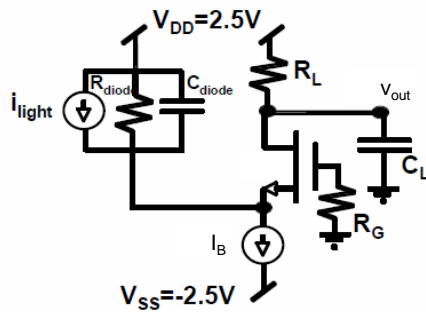
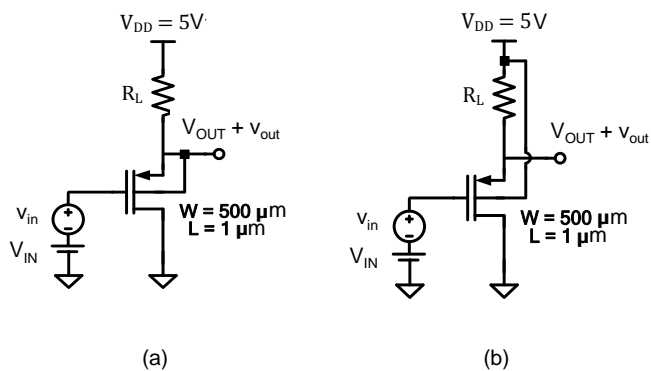


Figure P4.5



Italicize variables.

Figure P4.7



Italicize variables.

Figure P4.8

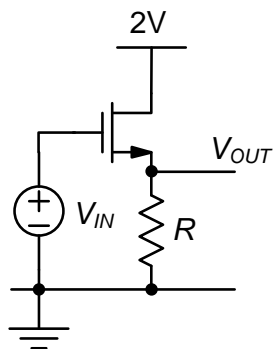


Figure P4.12

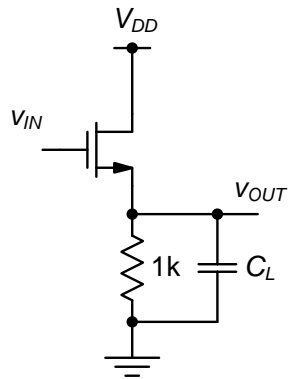


Figure P4.16

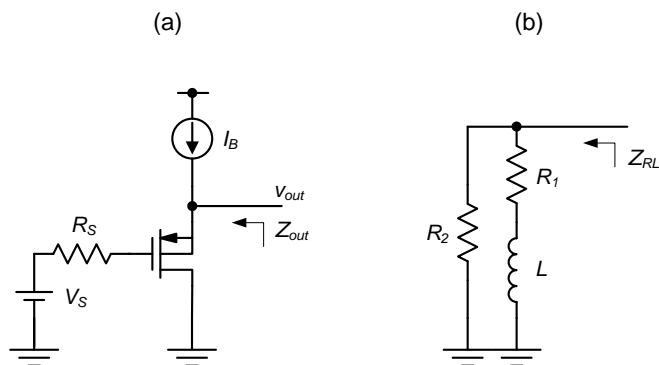


Figure 5-1

Process Variation and Device Mismatch
Section 5.2

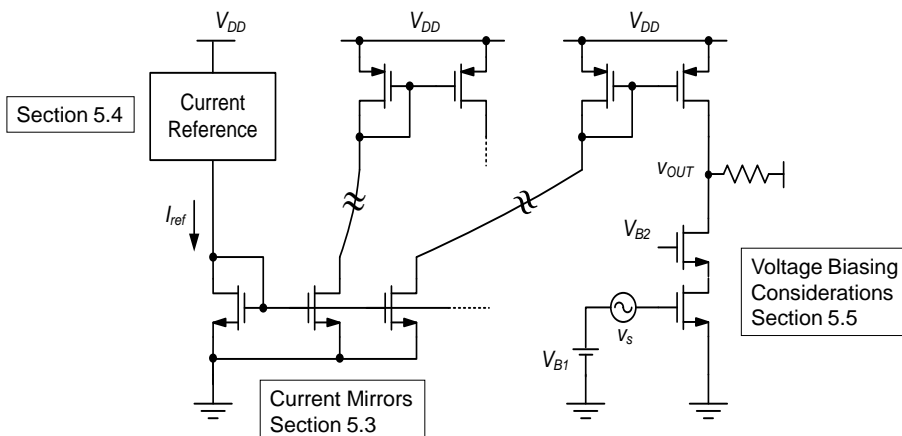


Figure Ex5-1

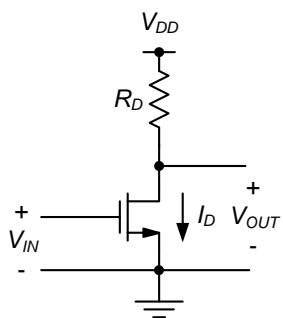


Figure 5-2

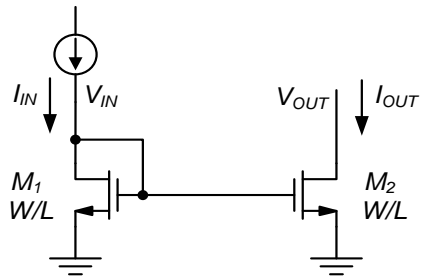
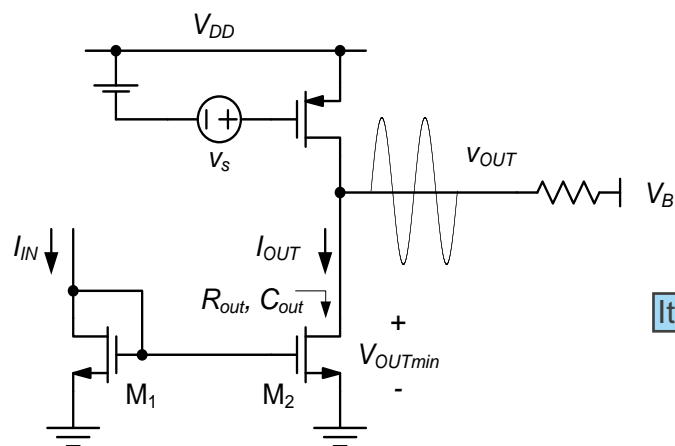
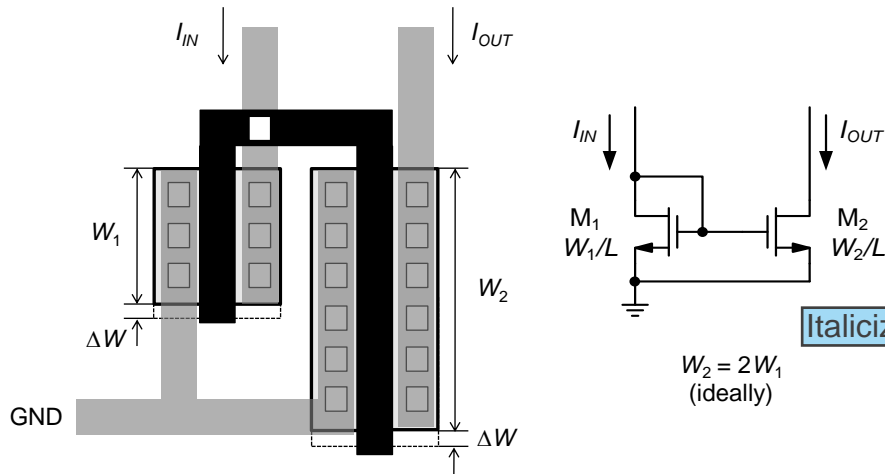


Figure 5-3



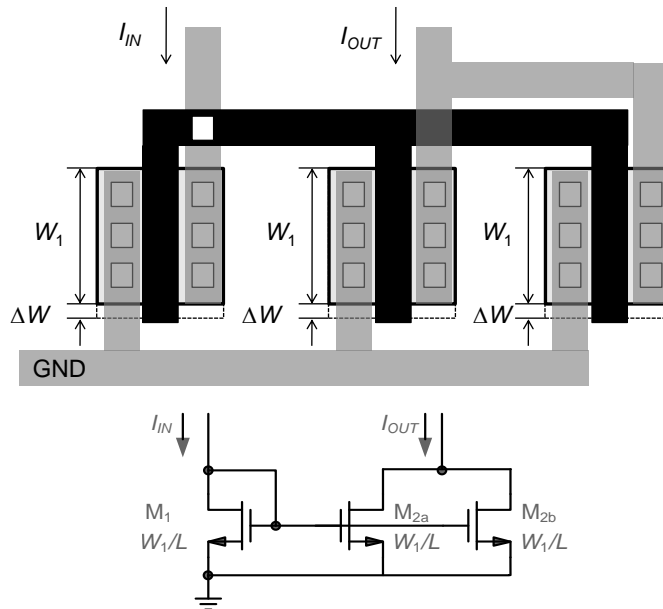
Italicize variables.

Figure 5-4



Italicize variables.

Figure 5-5



Italicize variables.

Figure 5-6

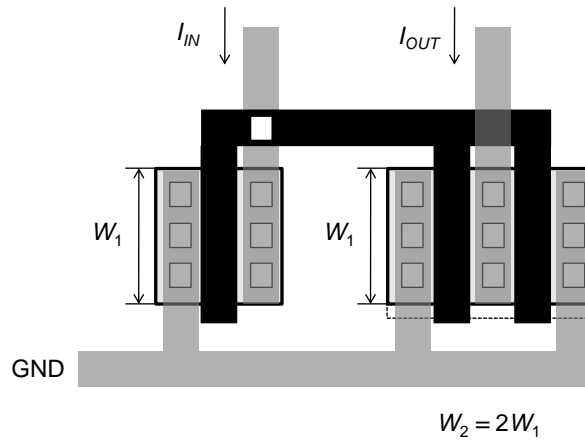
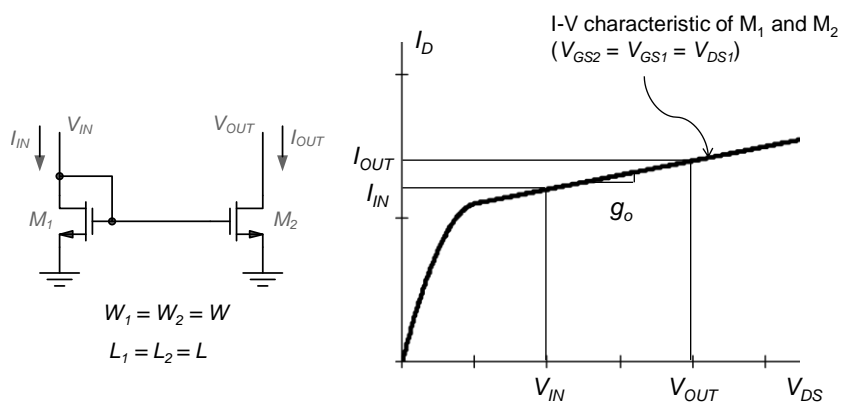
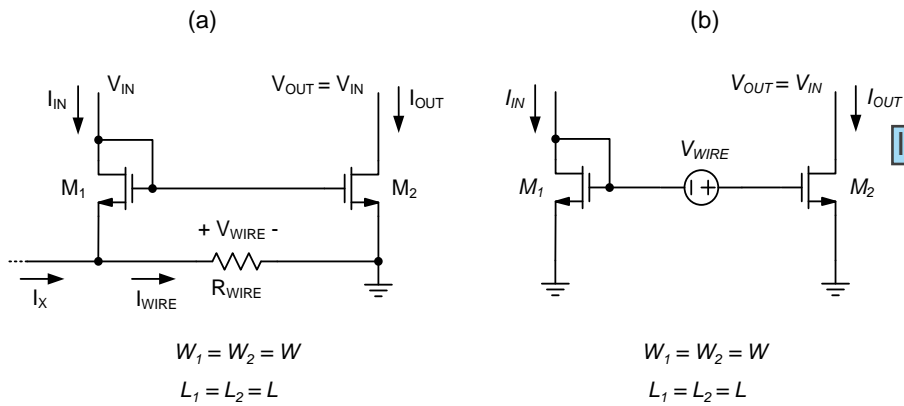


Figure 5-7



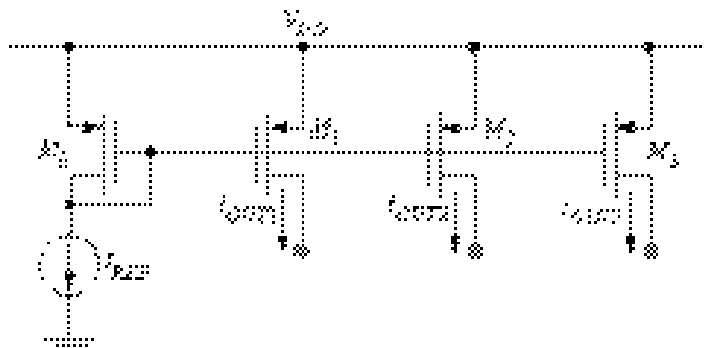
Italicize variables.

Figure 5-8



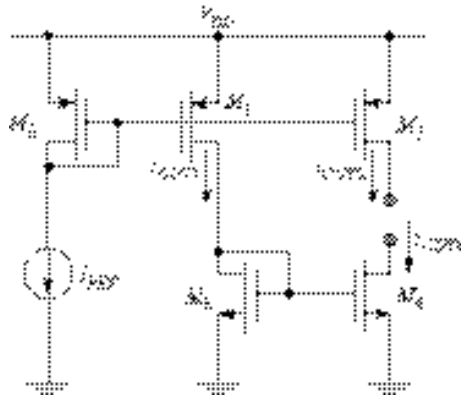
Italicize variables.

Figure 5-9



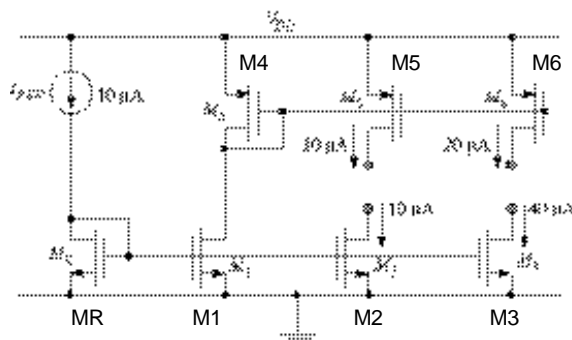
(Howe & Sodini, Figure 9-31)

Figure 5-10



(Howe & Sodini, Figure 9-32)

Figure Ex5-3



Device Data
 $V_{DD} = 1.5$
 $V_{TH} = 0.5$
 $\mu_{n0} C_{ox} = 200 \mu A/V^2$
 $\mu_{p0} C_{ox} = 100 \mu A/V^2$
 $\lambda_n = \lambda_p = 0.1 V^{-1}$ @ $L = 1 \mu m$

Delete

(Howe & Sodini, Figure Ex 9-8)

Italicize variables.

Figure 5-11

(a)

(b)

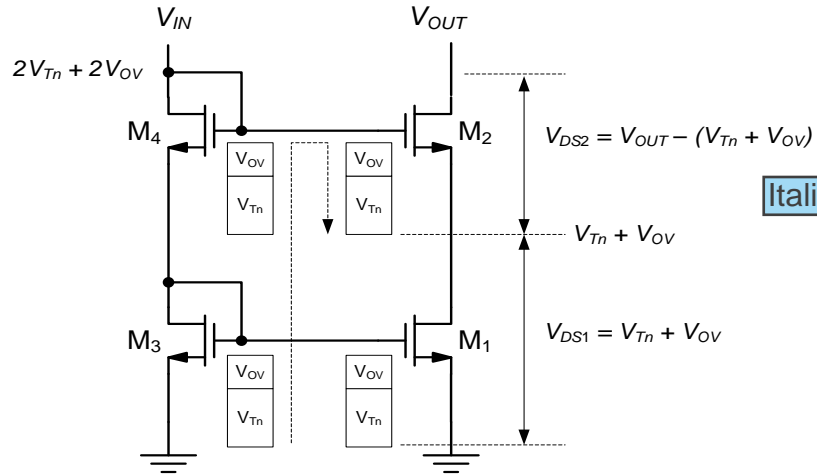


Figure 5-12

The figure consists of two parts. The left part is a circuit diagram of a source follower (common-drain) amplifier. It features an NMOS transistor M_1 with its gate connected to a bias voltage V_{D1} and its source connected to a load resistor r_{o2} . The output voltage V_{out} is taken from the source of M_1 . The transconductance of M_1 is denoted as g'_{m2} . The right part is a graph of the drain current I_{OUT} versus the drain-source voltage V_{DS} for the transistor M_1 . The curve shows the I-V characteristic of M_1 . A horizontal line at I_{OUT} intersects the curve, and a vertical line drops from this point to the x-axis at V_{D1} . The slope of the curve at this point is labeled g_{o1} . A small signal i_{out} is indicated on the I_{OUT} axis. A voltage divider is shown between r_{o2} and g'_{m2} , with the output voltage V_{d1} indicated across g'_{m2} .

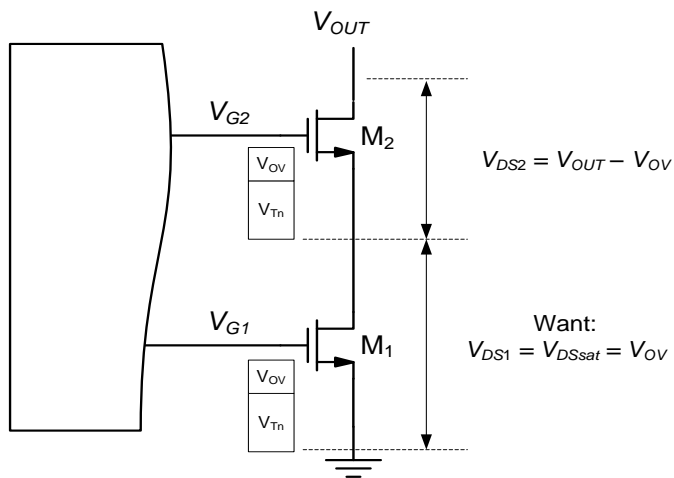


Figure 5-13



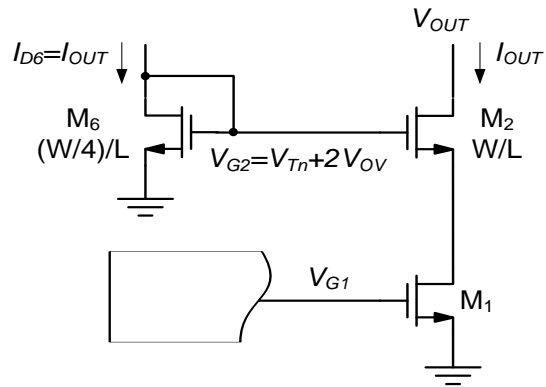
Italicize variables.

Figure 5-14



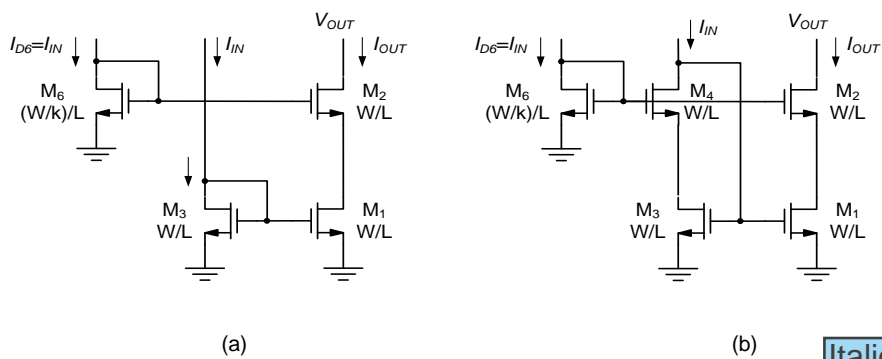
Italicize variables.

Figure 5-15



Italicize variables.

Figure 5-16



Italicize variables.

Figure 5-17

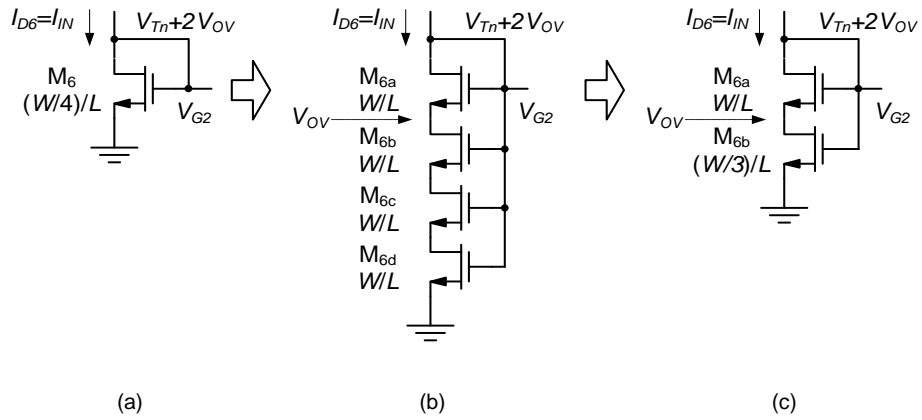
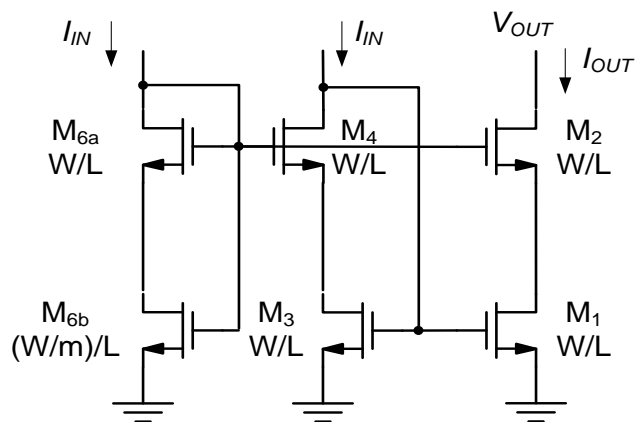
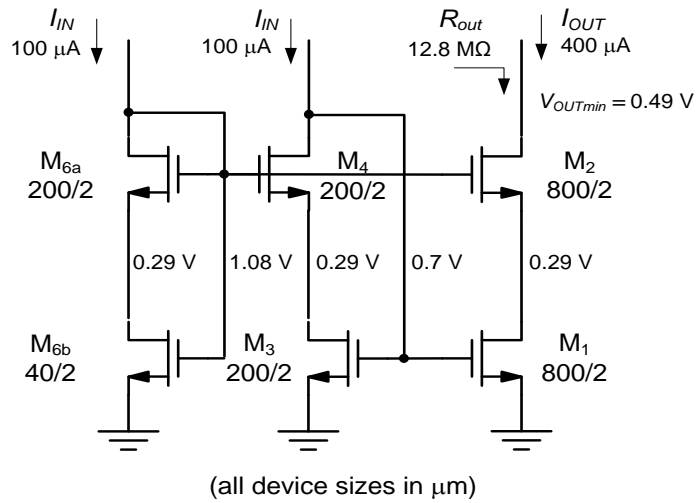


Figure 5-18



Italicize variables.

Solution to Ex 5-3



Italicize variables.

Figure 5-19

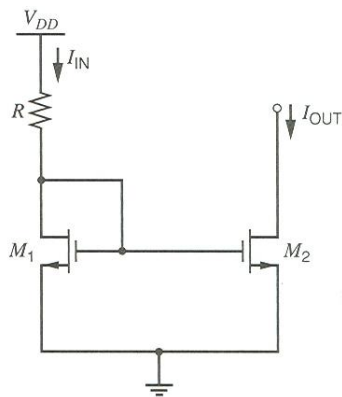


Figure 5-20

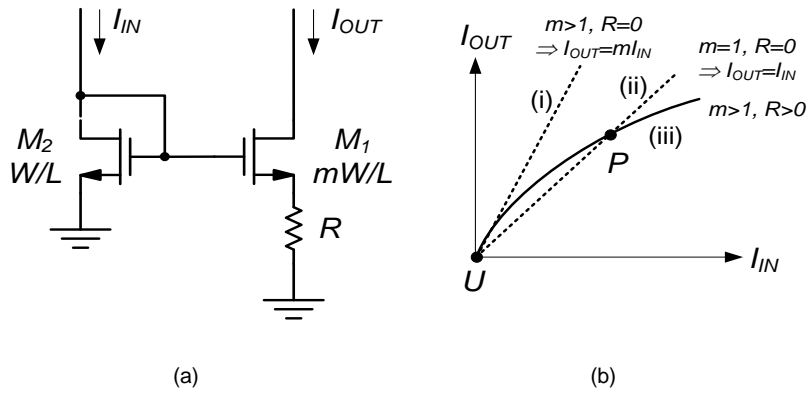


Figure 5-21

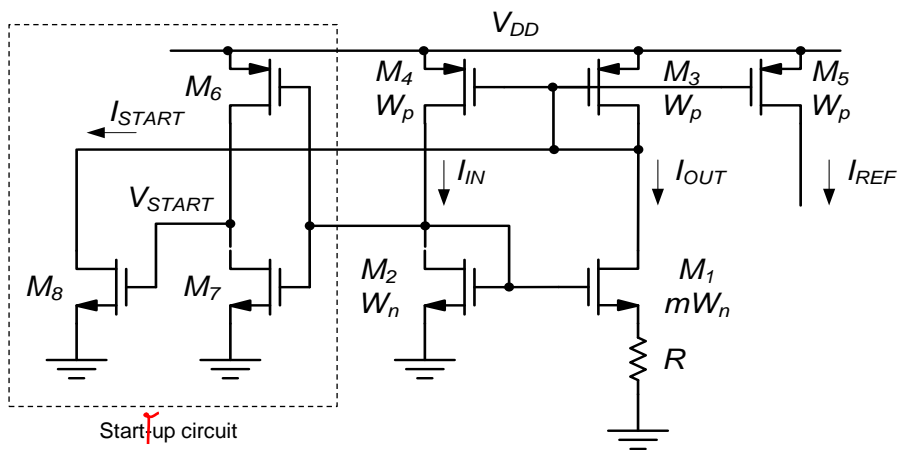


Figure 5-22

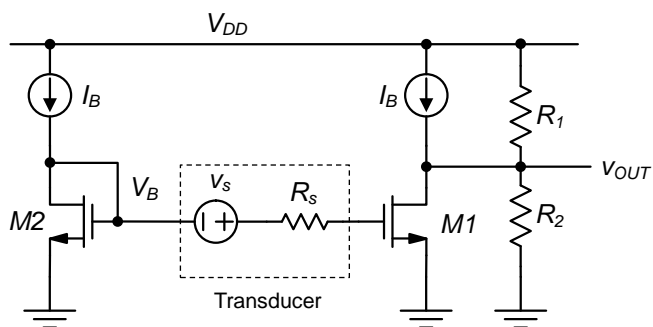


Figure 5-23

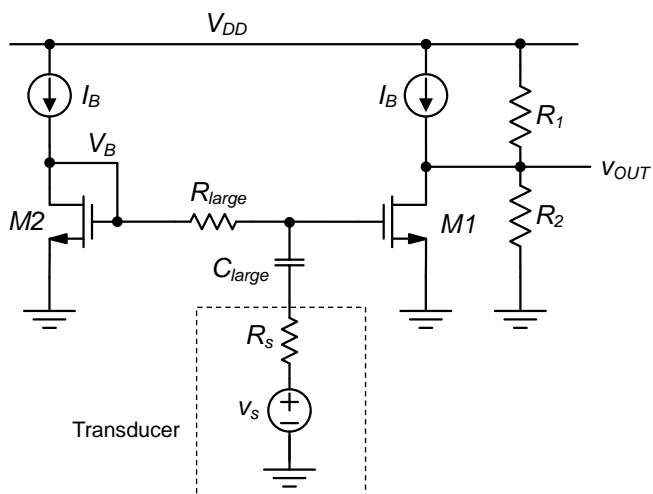
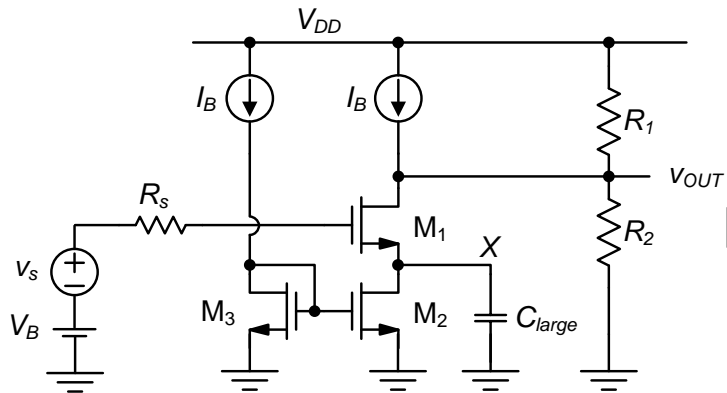
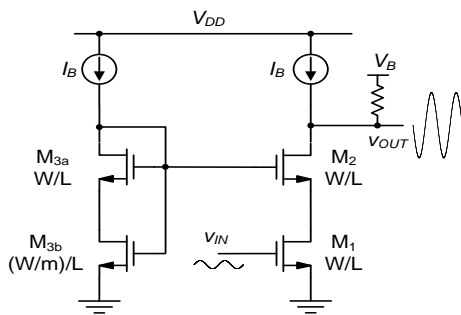


Figure 5-24

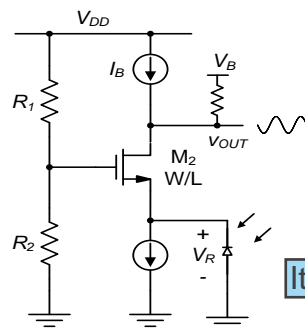


Italicize variables.

Figure 5-25



(a)



(b)

Italicize variables.

Figure 5-26

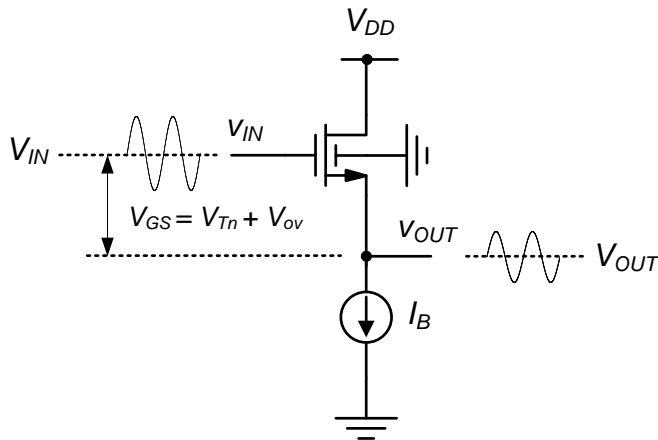
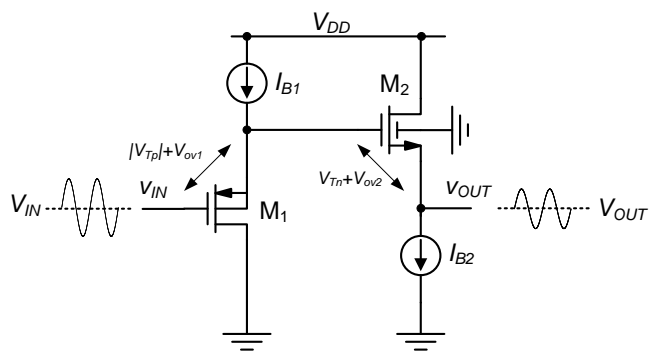


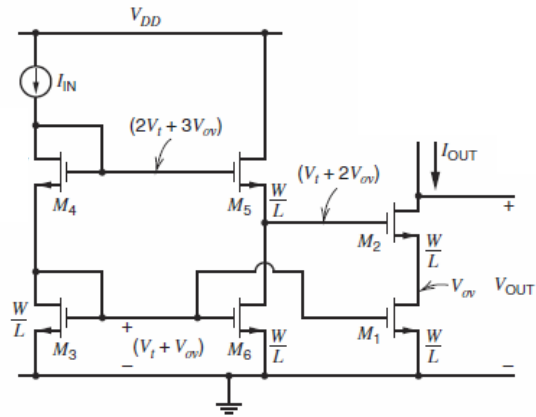
Figure 5-27



Italicize variables.

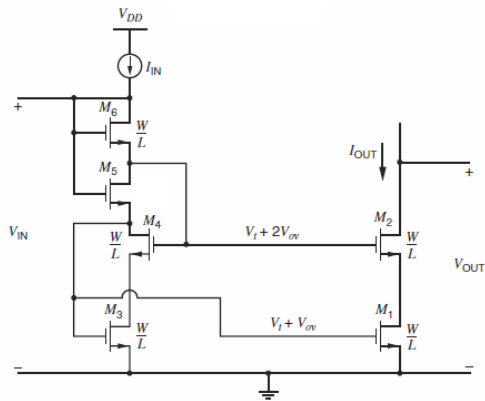
Problem P5.5

The circuit diagram shows a multi-stage CMOS amplifier. The input current I_{IN} is applied to the gate of transistor M_4 . The gates of M_4 and M_5 are connected to V_{DD} through a resistor labeled $(2V_t + 3V_{ov})$. The gates of M_3 and M_6 are connected to ground through a resistor labeled $(V_t + V_{ov})$. The gates of M_2 and M_1 are connected to the output node V_{OUT} through a resistor labeled $(V_t + 2V_{ov})$. The output current I_{OUT} is drawn from the output node V_{OUT} . The transistors are labeled M_1 through M_5 . The width-to-length ratio $\frac{W}{L}$ is indicated for each transistor: $\frac{W}{L}$ for M_1 , M_2 , M_3 , M_4 , and M_5 ; and $\frac{W}{L}$ for M_6 . The overdrive voltage V_{ov} is indicated for the output stage transistors M_1 and M_2 .

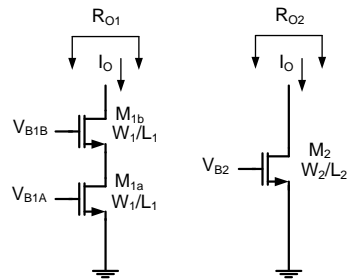


Problem P5.6

The diagram shows a CMOS differential amplifier circuit. The input signal V_{IN} is applied to the gates of two NMOS transistors, M_3 and M_4 . The gates of two PMOS transistors, M_5 and M_6 , are connected to V_{DD} . The source of M_3 is connected to ground, and the source of M_4 is connected to the source of M_1 . The source of M_1 is connected to ground. The source of M_2 is connected to the source of M_4 . The source of M_5 is connected to the source of M_4 , and the source of M_6 is connected to V_{DD} . A tail current source I_{IN} is connected between V_{DD} and the source of M_4 . The output voltage V_{OUT} is taken from the drain of M_2 . The drain of M_1 is connected to ground. The drain of M_2 is connected to V_{DD} . The drain of M_3 is connected to the drain of M_1 . The drain of M_4 is connected to the drain of M_2 . The drain of M_5 is connected to the drain of M_4 . The drain of M_6 is connected to V_{DD} . The output current I_{OUT} is shown flowing out of the output node.

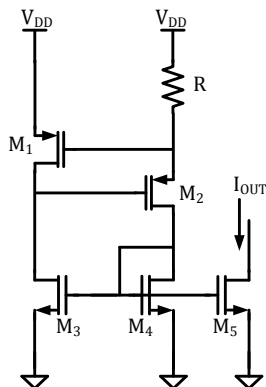


Problem P5.9



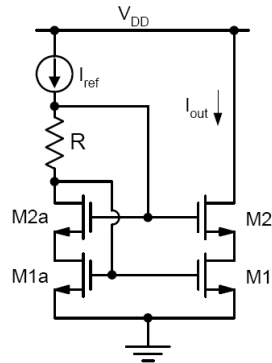
Italicize variables.

Problem P5.10



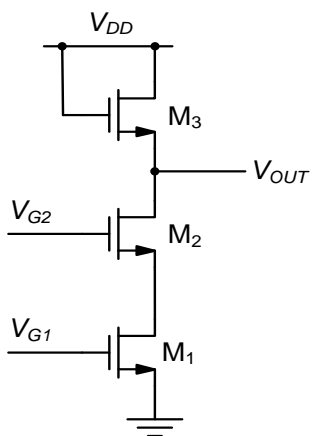
Italicize variables.

Problem P5.11



Italicize variables.

Problem P5.12



Italicize variables.

Problem P5.13

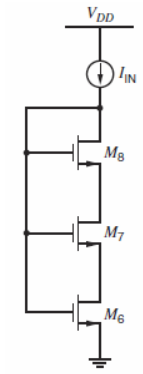


Figure 6-1

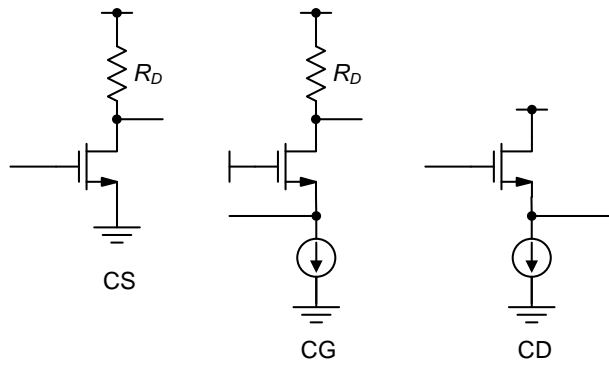


Figure 6-2

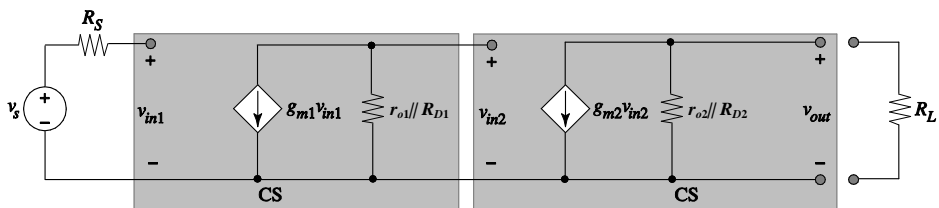


Figure 6-3

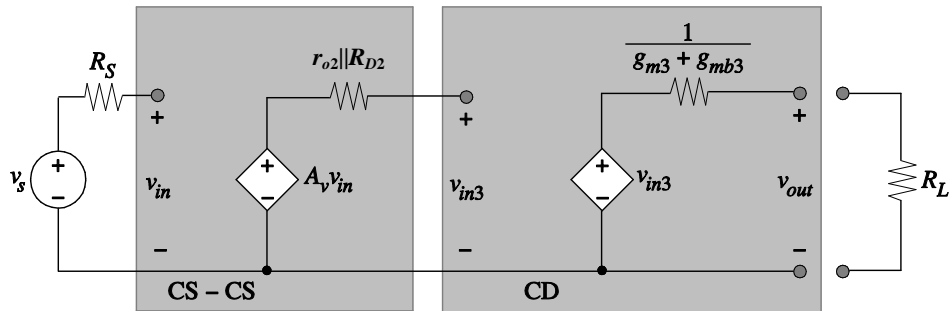


Figure 6-4

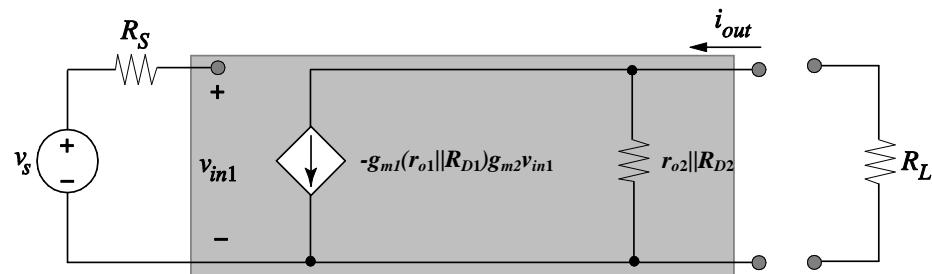


Figure 6-5

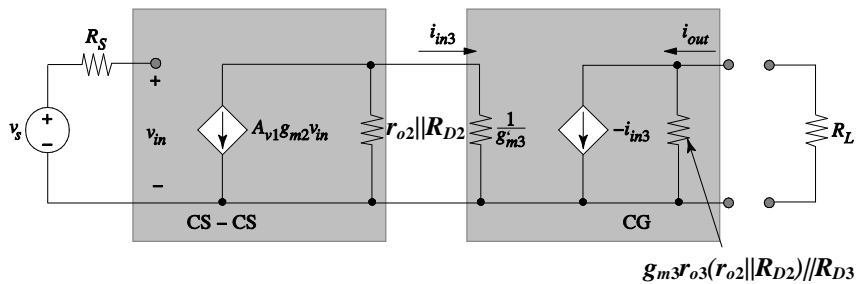


Figure Ex6-1A

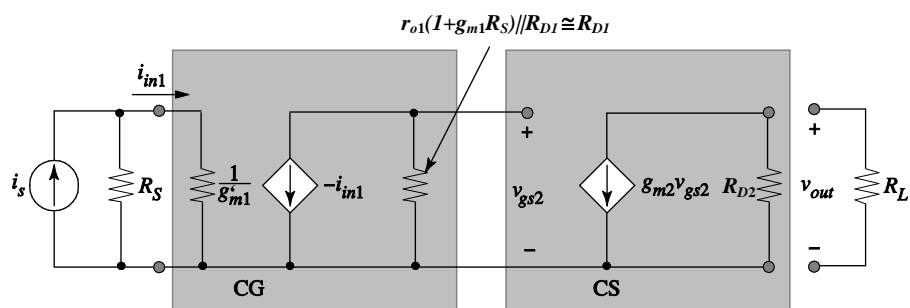


Figure Ex6-1B

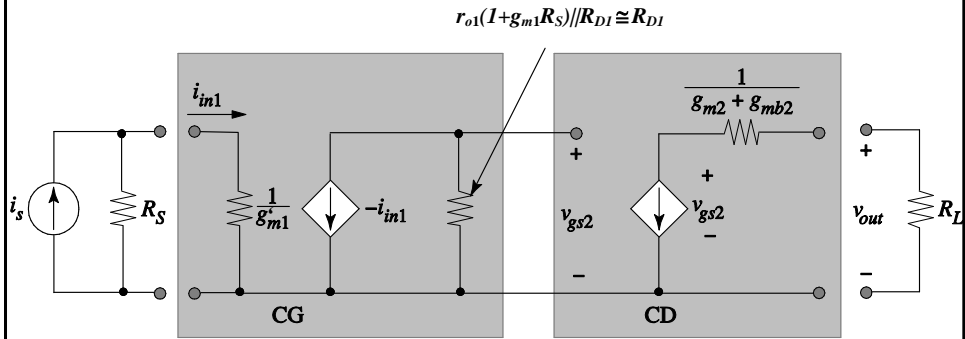


Figure 6-6

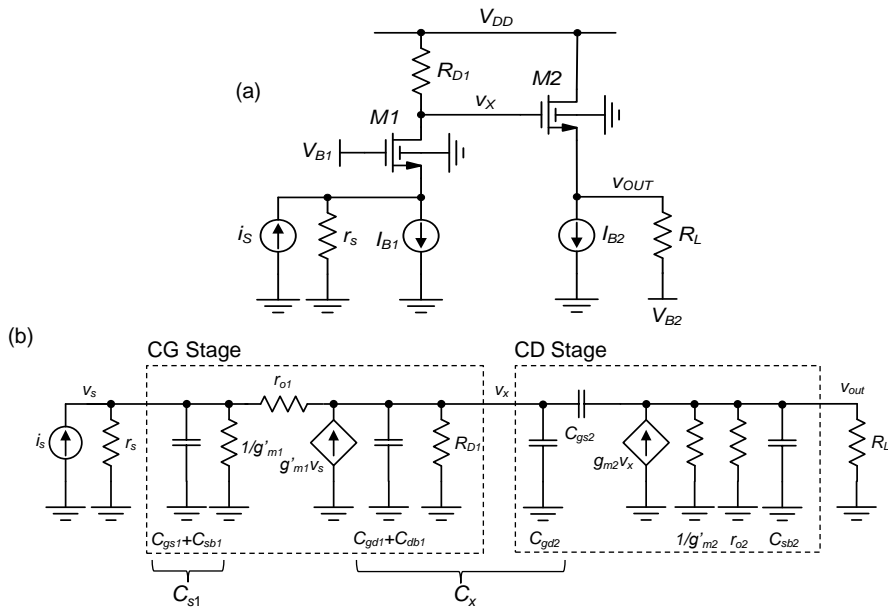
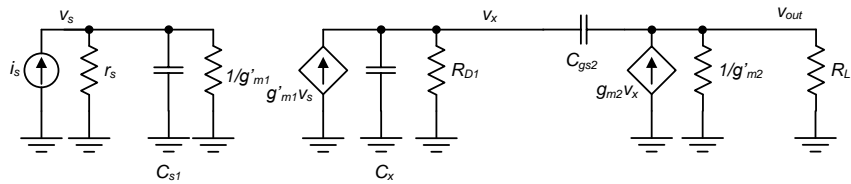
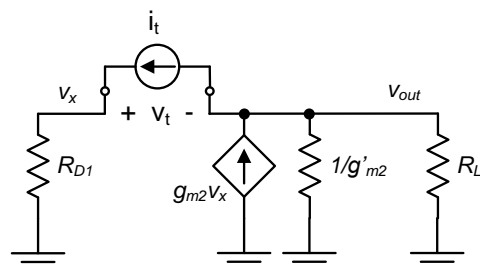


Figure 6-7



Example 6-2 Solution



Italicize variables.

Example 6-3 Solution

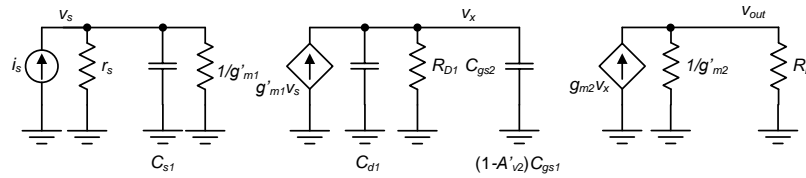


Figure 6-8

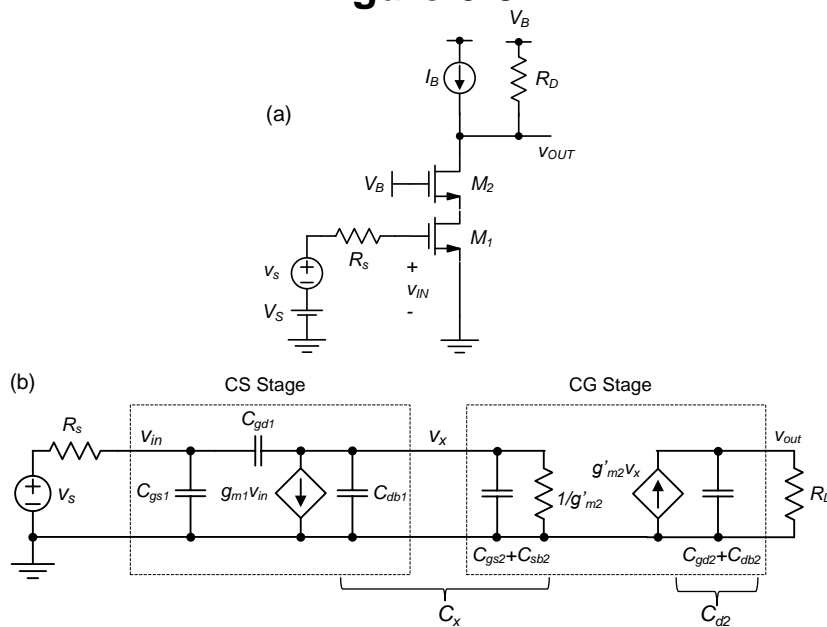


Figure Ex6-3

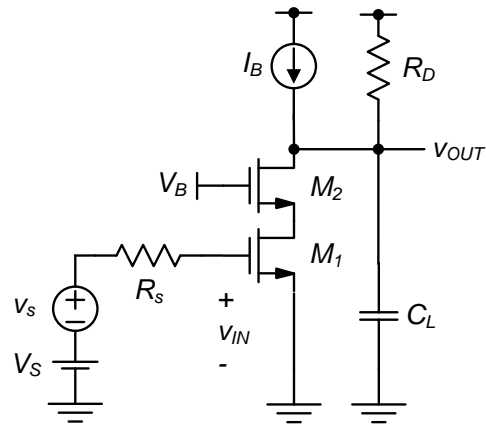


Figure 6-9

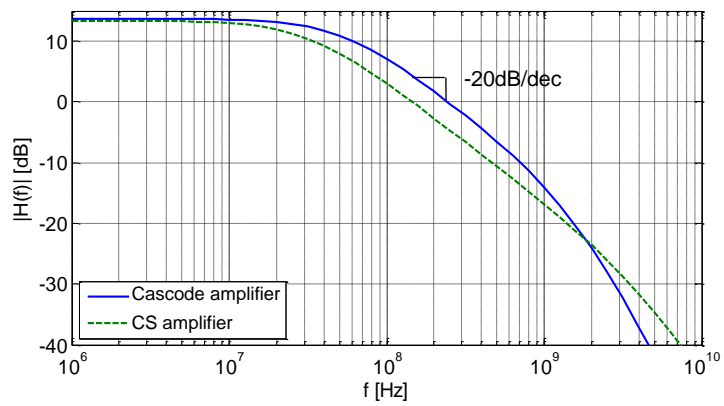


Figure 6-10

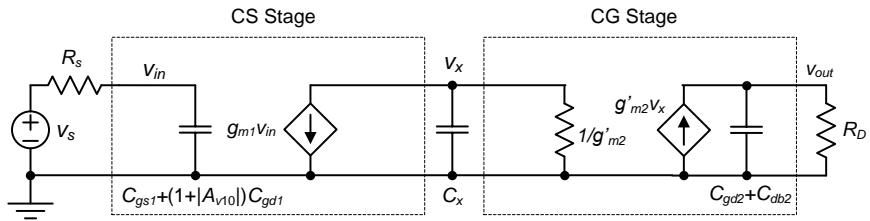


Figure 6-11

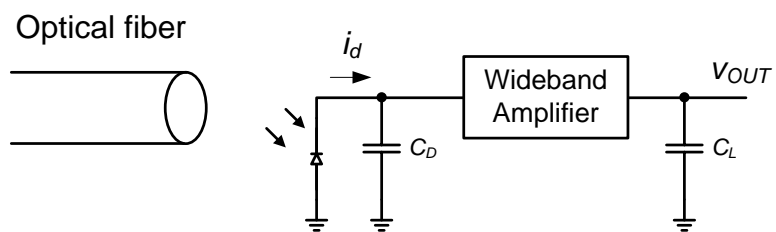
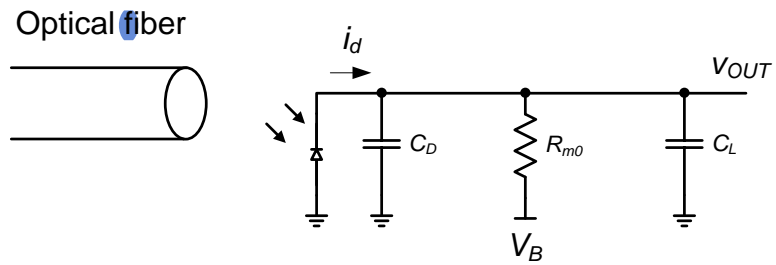


Figure 6-12



cap

Figure 6-13

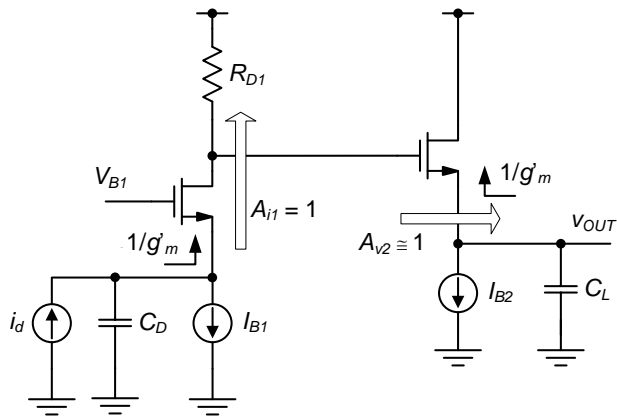


Figure 6-14

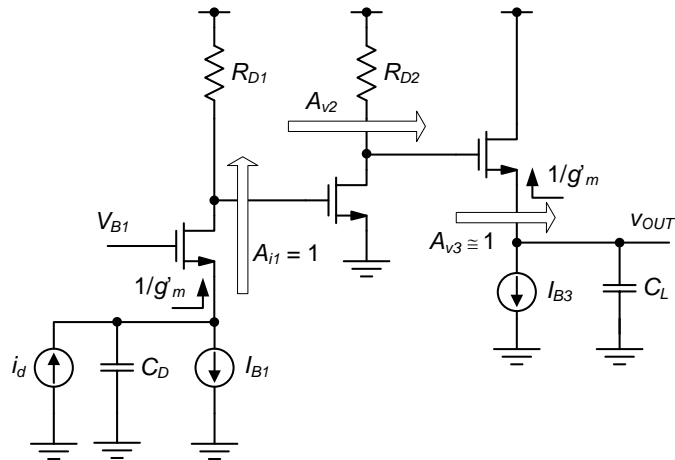
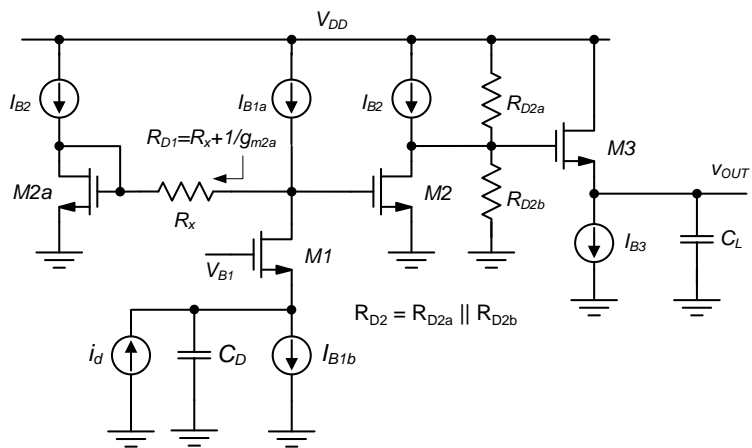
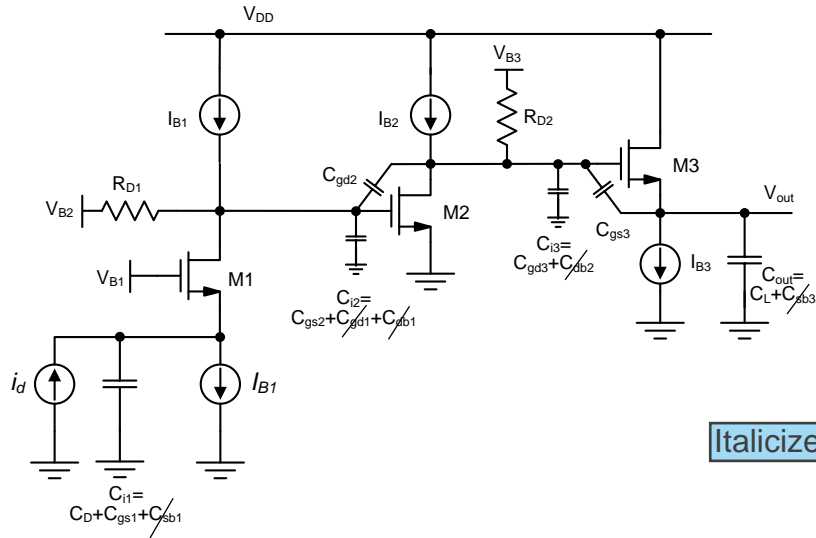


Figure 6-15



Italicize variables.

Figure 6-16



Italicize variables.

Figure 6-17

```
% Design script for three-stage transresistance amplifier

% Process technology parameters
kp_n = 50e-6;
Cox = 2.3e-3;
mu_n = kp_n/Cox;
Cov = 0.5e-9;
gmb_gm = 0.2;

% Design specifications
Rm = 2e3;
CD = 5e-12;
CL = 10e-12;
IDtot = 3e-3;

% Design choices
VOV1 = 0.3;
VOV2 = 0.3;
VOV3 = 0.3;
L1 = 1e-6;
L2 = 1e-6;
L3 = 1e-6;

% optimization parameters
ID1_IDtot = 0.25;
ID3_IDtot = 0.25;
Av20 = 10;

% Compute drain currents
ID1 = IDtot*ID1_IDtot;
ID3 = IDtot*ID3_IDtot;
ID2 = IDtot - ID1 - ID3;

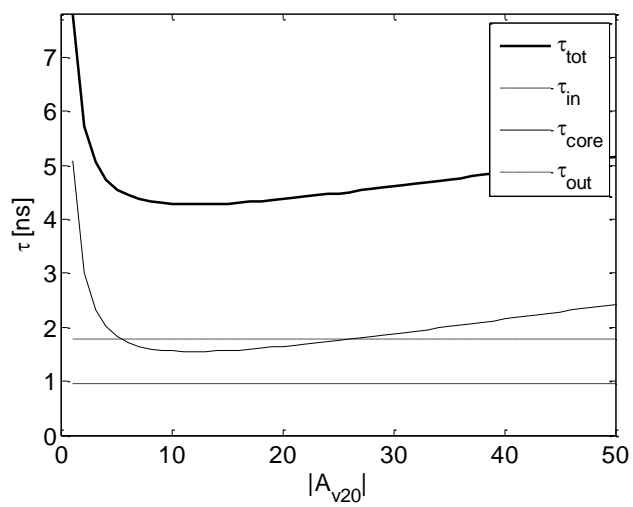
% Calculations for M1
gm1 = 2*ID1/VOV1;
W1 = 2*ID1/(kp_n/L1*VOV1^2);
Cgs1 = 2/3*W1*L1*Cox + W1*Cov;
tau_in = (Cgs1+CD)/(gm1*(1+gmb_gm));

% Calculations for M3
gm3 = 2*ID3/VOV3;
W3 = 2*ID3/(kp_n/L3*VOV3^2);
Cgs3 = 2/3*W3*L3*Cox + W3*Cov;
Cgd3 = W3*Cov;
Av30 = 1-gmb_gm;
tau_out = (CL+Cgs3)/(gm3*(1+gmb_gm));

% Calculations for M2
gm2 = 2*ID2/VOV2;
W2 = 2*ID2/(kp_n/L2*VOV2^2);
Cgs2 = 2/3*W2*L2*Cox + W2*Cov;
Cgd2 = W2*Cov;
RD1 = Rm/Av20/Av30;
RD2 = Av20/gm2;
tau_core = RD1*(Cgs2 + (1+Av20)*Cgd2) + RD2*(Cgd3+(1-Av30)*Cgs3);

% Total time constant and bandwidth estimate
tau_tot = tau_in + tau_core + tau_out;
f3dB = 1/(2*pi*tau_tot);
```

Figure 6-18



Italicize variables.

Figure P6-3

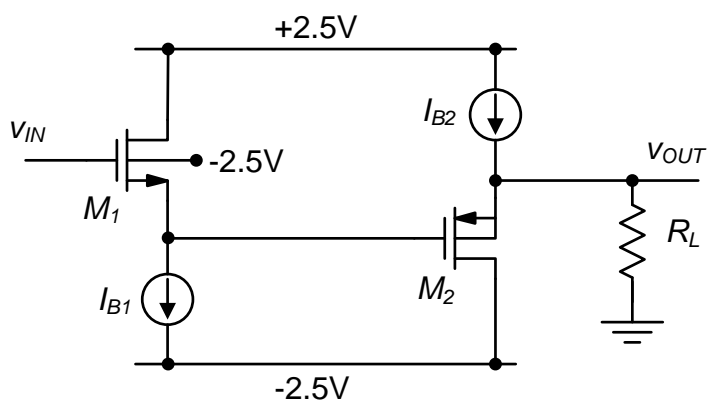
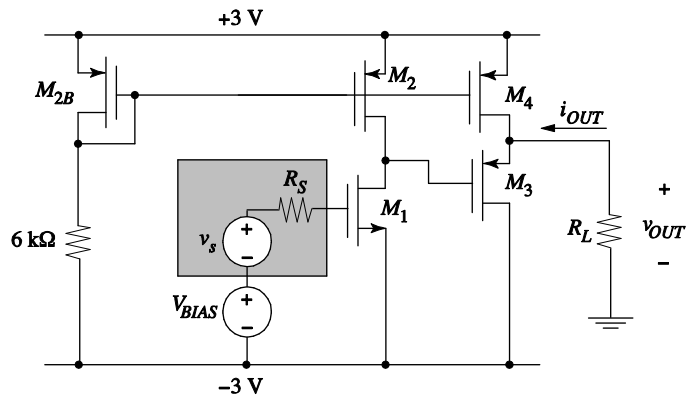
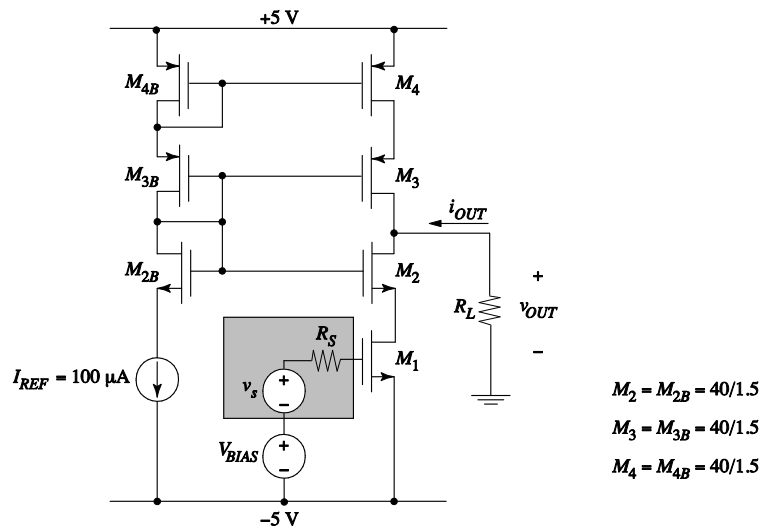


Figure P6-5



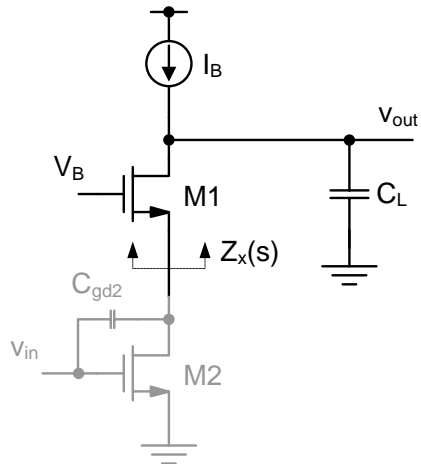
Howe & Sodini, Fig. P9-17

Figure P6-6



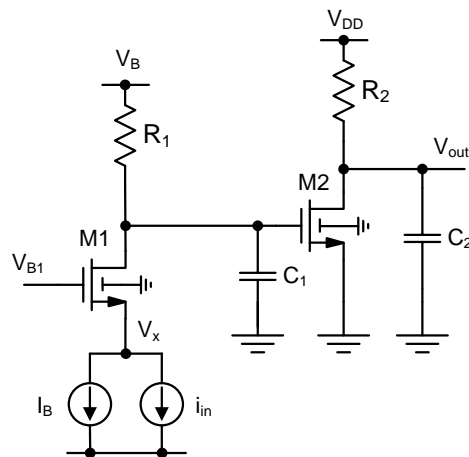
Howe & Sodini, Fig. P9-20

Figure P6-7



Italicize variables.

Figure P6-8



Italicize variables.

Figure P6-9

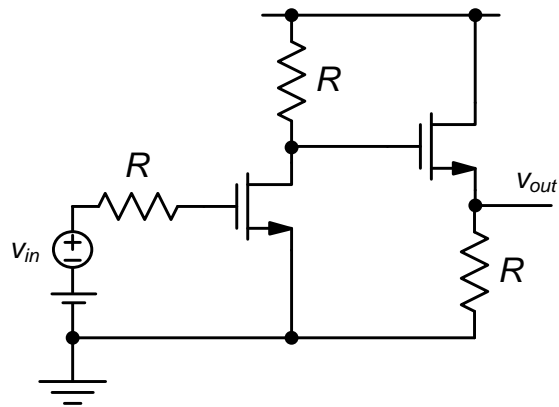
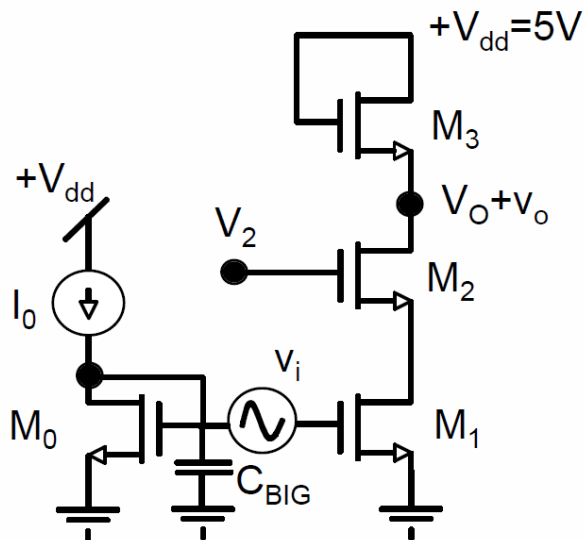
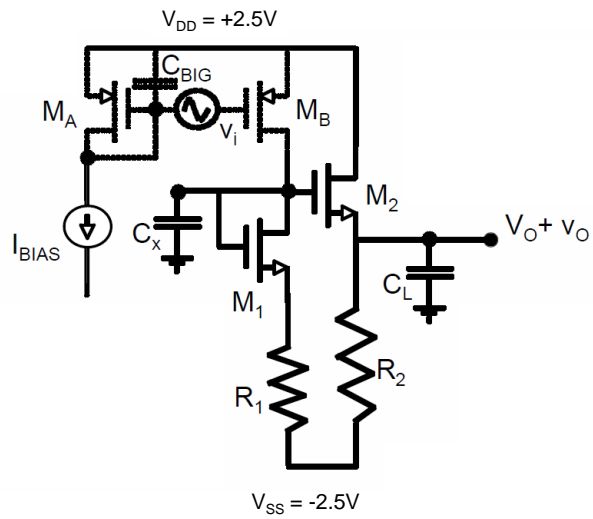


Figure P6-12



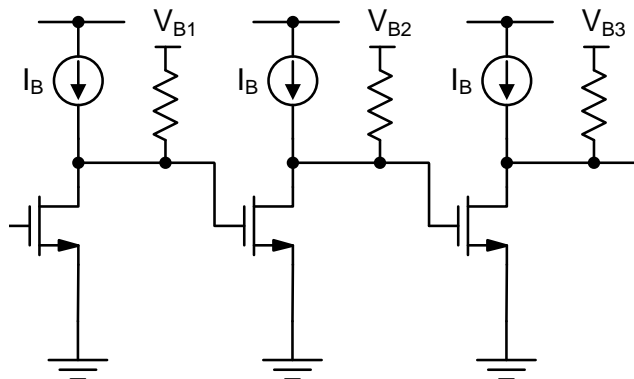
Italicize variables.

Figure P6-13



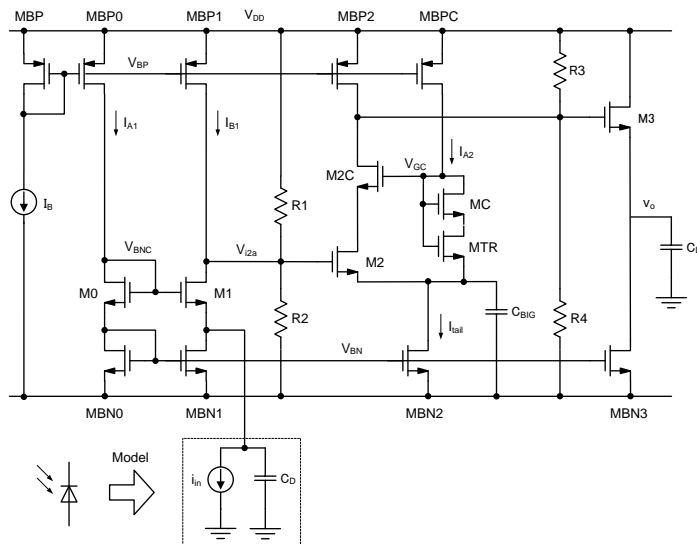
Italicize variables.

Figure P6-14



Italicize variables.

Figure P6-15



Italicize variables.