

Figure 5-1

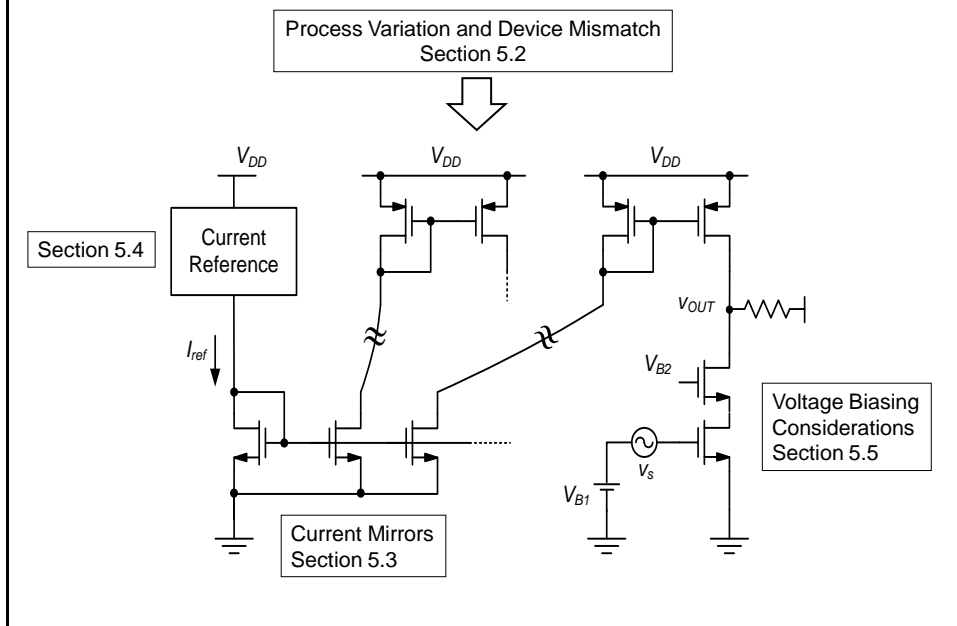


Figure Ex5-1

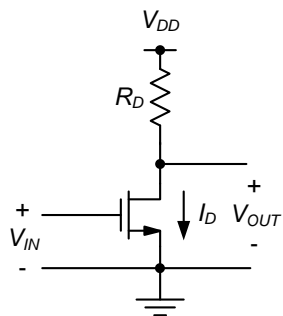


Figure 5-2

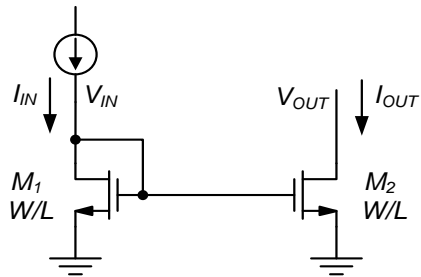


Figure 5-3

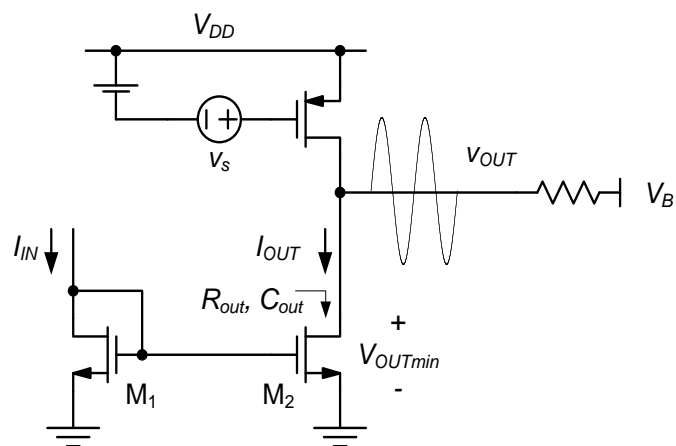


Figure 5-4

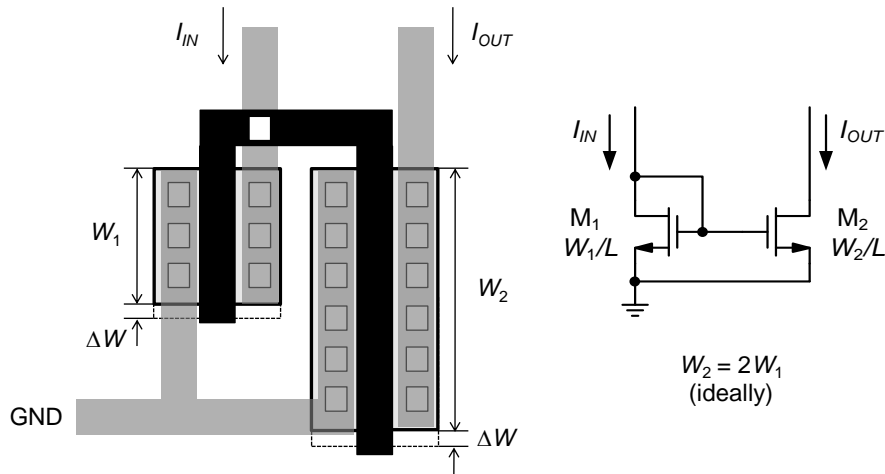


Figure 5-5

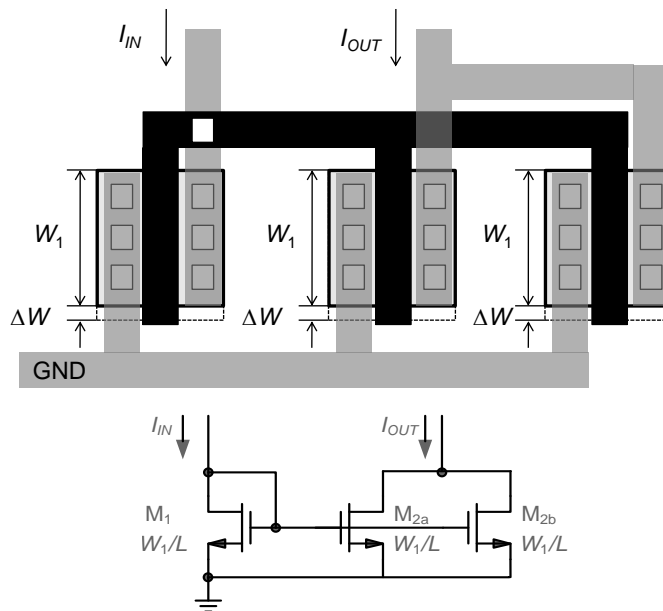


Figure 5-6

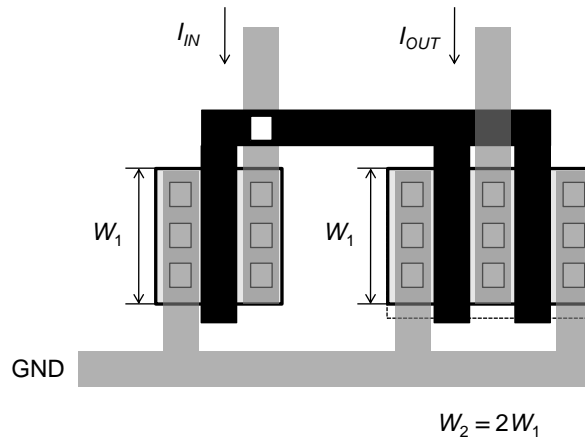


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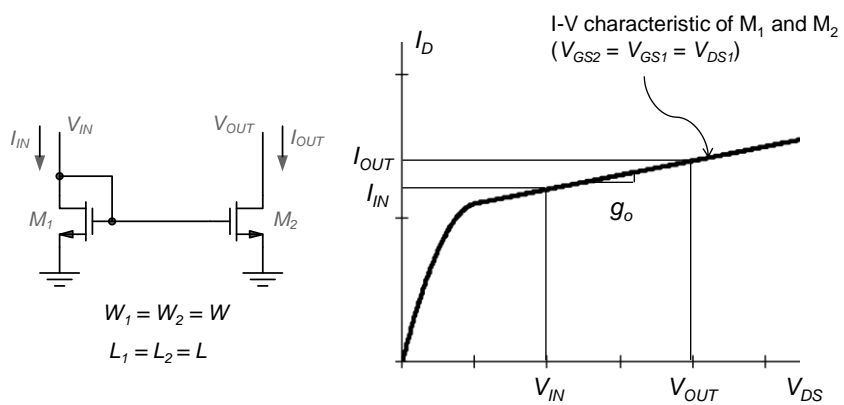


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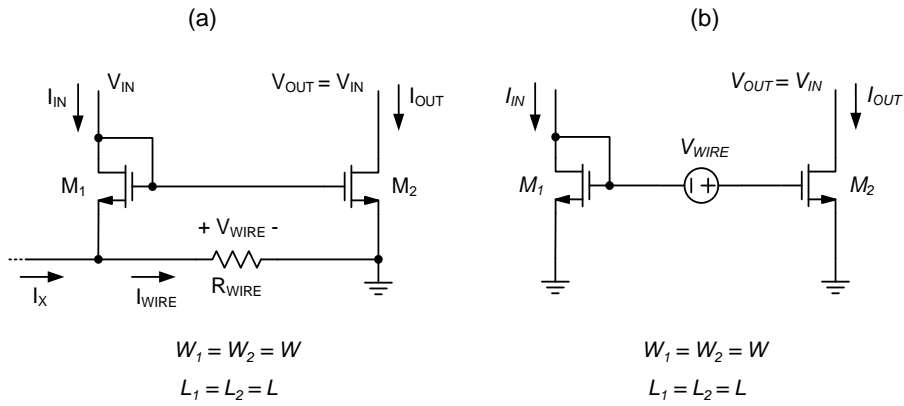
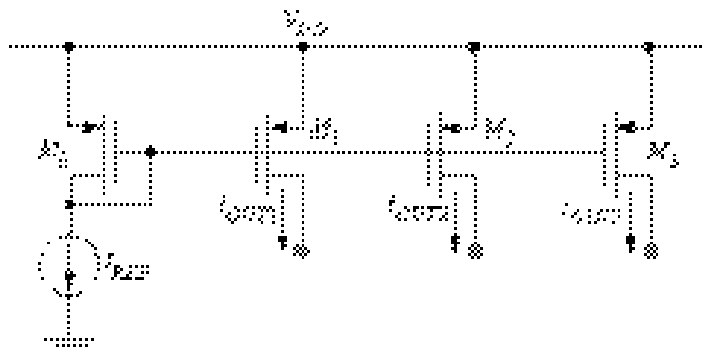
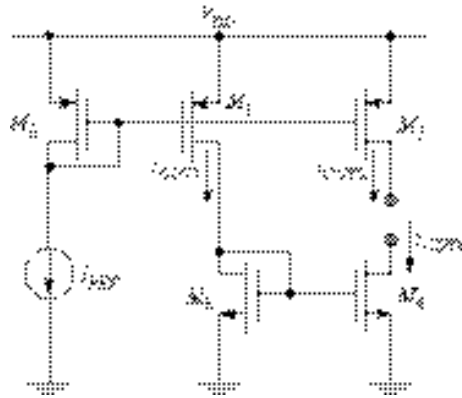


Figure 5-9



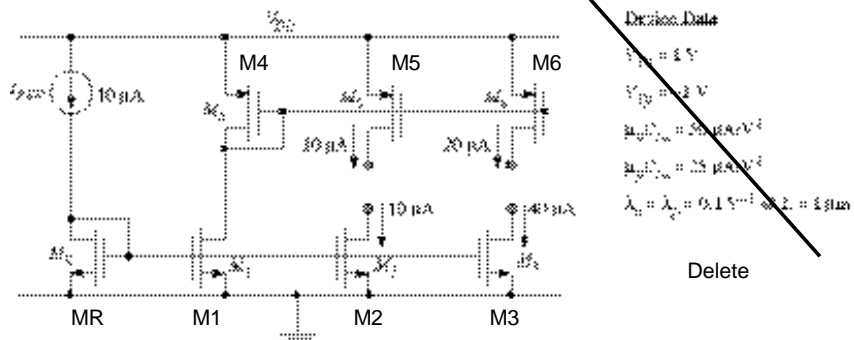
(Howe & Sodini, Figure 9-31)

Figure 5-10



(Howe & Sodini, Figure 9-32)

Figure Ex5-3



(Howe & Sodini, Figure Ex 9-8)

Figure 5-11

(a) Schematic of a cascode stage. It consists of two PMOS transistors, M_4 and M_2 , and two NMOS transistors, M_3 and M_1 . The input signal V_{IN} is applied to the gate of M_4 , and the output V_{OUT} is taken from the drain of M_2 . The gates of M_2 and M_3 are connected to a common bias voltage V_{G2} . The gates of M_1 and M_4 are connected to a common bias voltage V_{D1} . The sources of M_3 and M_1 are connected to ground. The sources of M_4 and M_2 are connected to the gates of M_3 and M_1 respectively. The input current I_{IN} flows into the drain of M_4 , and the output current I_{OUT} flows into the drain of M_2 . The bias voltages are labeled $V_{D3}=V_{G3}=V_{G1}$ and V_{D1} .

(b) Small-signal equivalent circuit of the cascode stage. The output resistance R_{out} is shown at the top. The circuit includes two dependent current sources, $g_{mb2}v_{bs2}$ and $g_{m2}v_{gs2}$, in parallel with the output resistance r_{o2} of the PMOS transistor M_2 . The source of M_2 is connected to ground through the output resistance r_{o1} of the NMOS transistor M_1 . The gate of M_1 is connected to ground through a bias voltage source $G1$.

Figure 5-12

Figure 5-12 illustrates the small-signal model and the I-V characteristic of a common-source amplifier.

The left diagram shows the small-signal model of the amplifier. The input signal v_{d1} is applied to the gate of the NMOS transistor M_1 . The output signal v_{out} is taken from the drain of M_1 , which is connected to a load resistor r_{o2} . The transconductance of M_1 is denoted by g'_{m2} .

The right diagram shows the I-V characteristic of the NMOS transistor M_1 . The horizontal axis represents the drain-source voltage V_{DS} , and the vertical axis represents the drain current I_{OUT} . The curve shows the relationship between I_{OUT} and V_{DS} for a given gate-source voltage V_{D1} . The slope of the curve at a specific operating point is labeled g_{o1} . The output voltage v_{out} is shown as a small signal v_{d1} superimposed on the DC bias V_{D1} . The output current I_{OUT} is shown as a small signal i_{out} superimposed on the DC bias I_{OUT} . The text "I-V characteristic of M_1 " points to the curve. The text "Voltage divider between r_{o2} and g'_{m2} " points to the output voltage v_{out} .

Figure 5-13

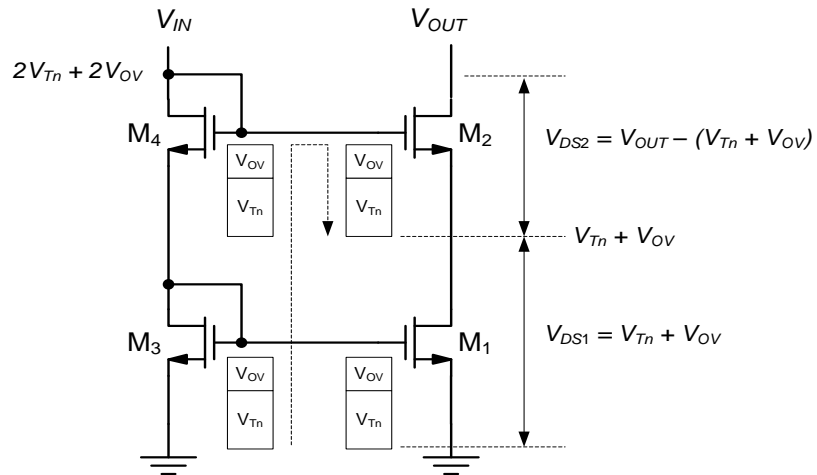


Figure 5-14

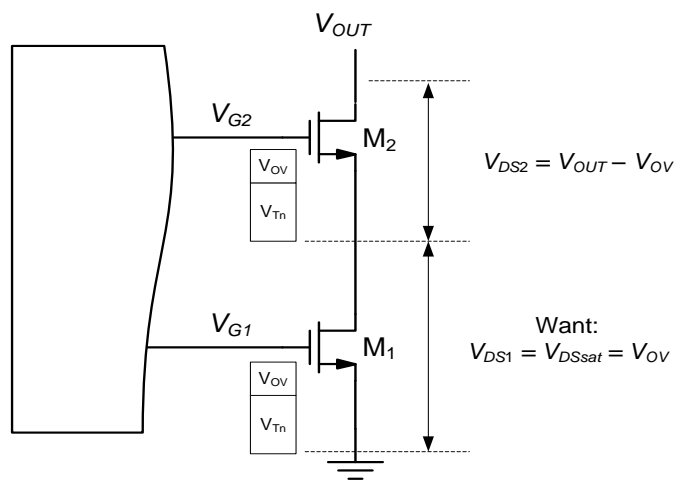


Figure 5-15

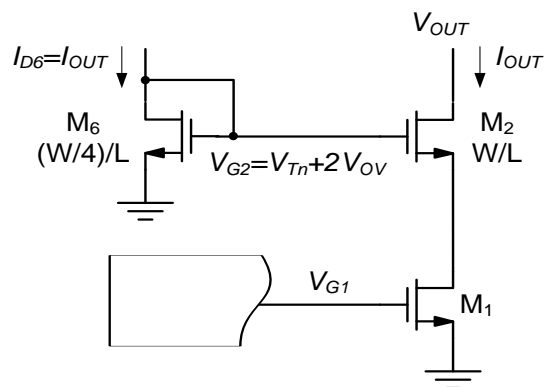


Figure 5-16

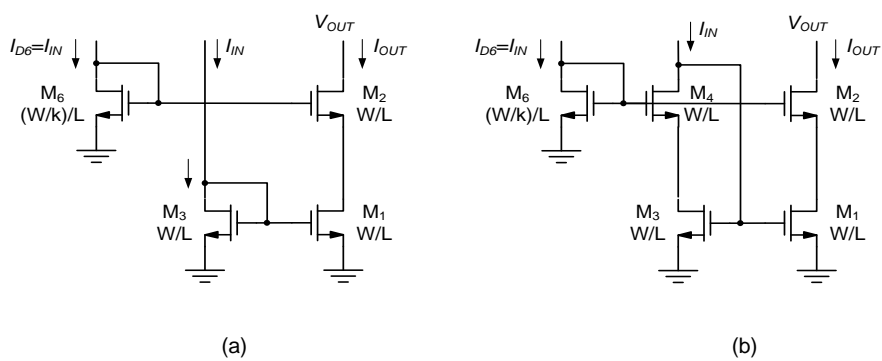


Figure 5-17

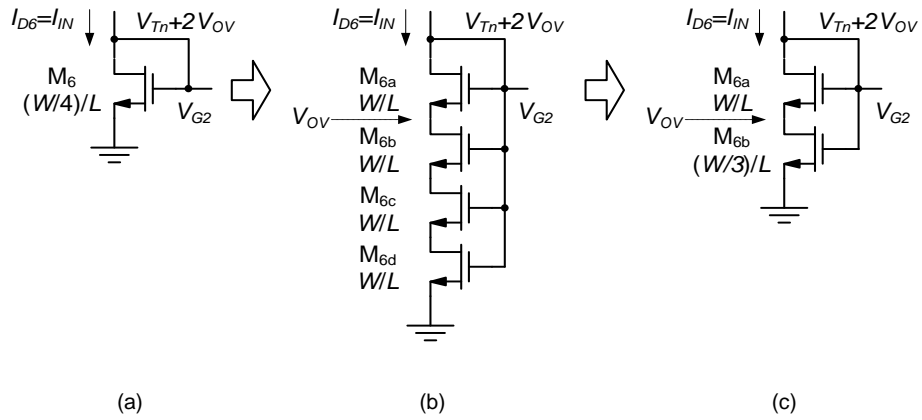
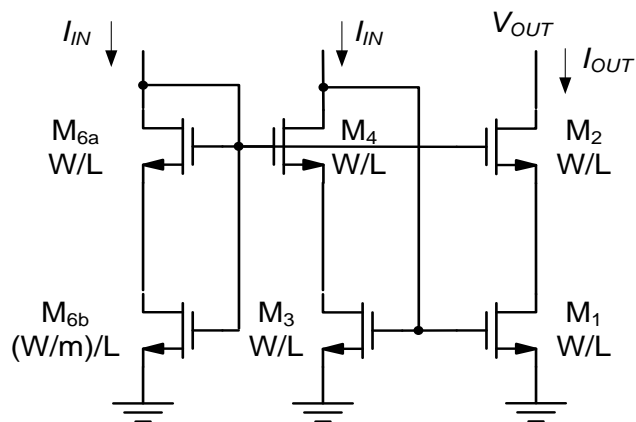


Figure 5-18



Solution to Ex 5-3

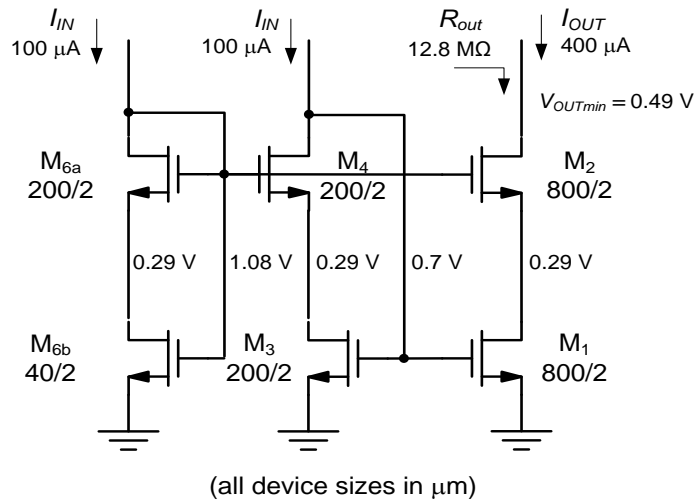


Figure 5-19

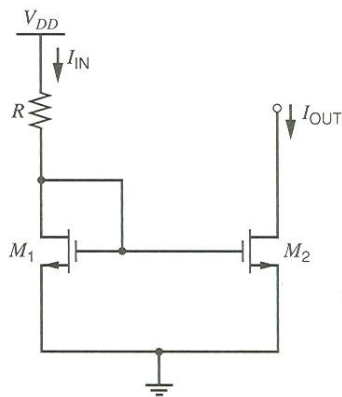


Figure 5-20

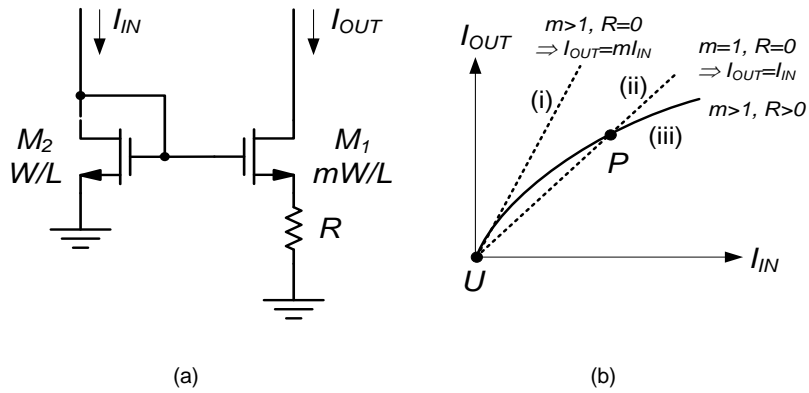


Figure 5-21

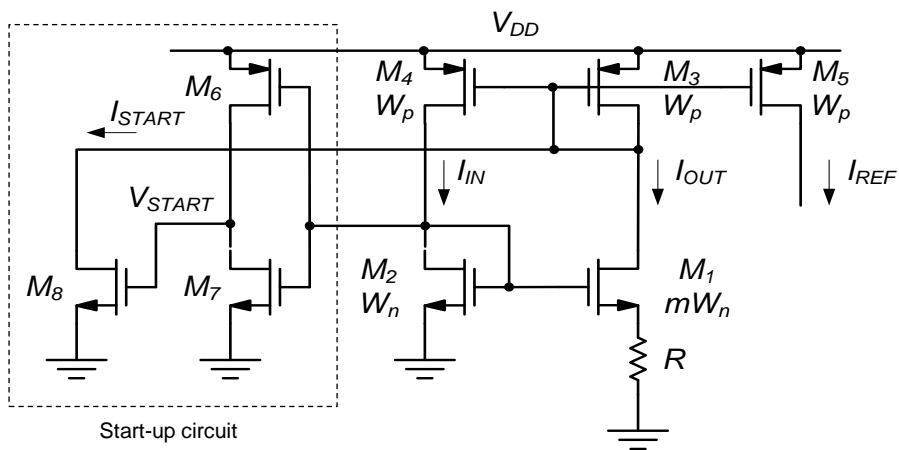


Figure 5-22

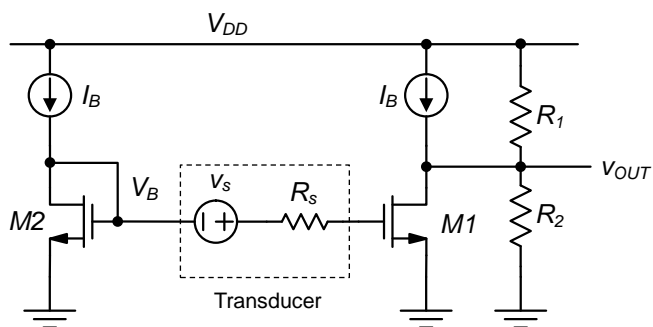


Figure 5-23

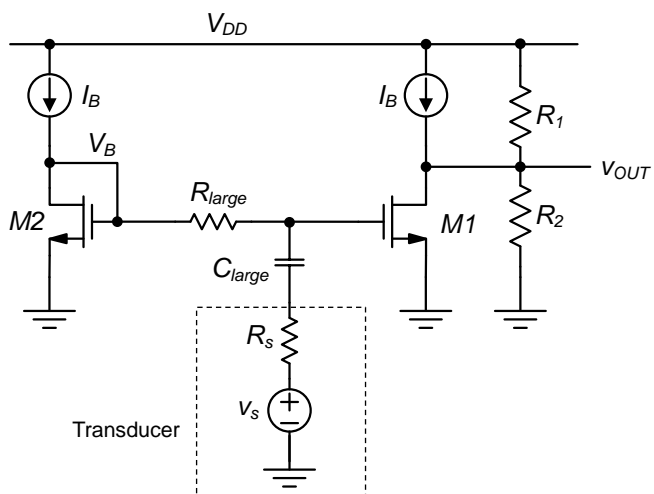


Figure 5-24

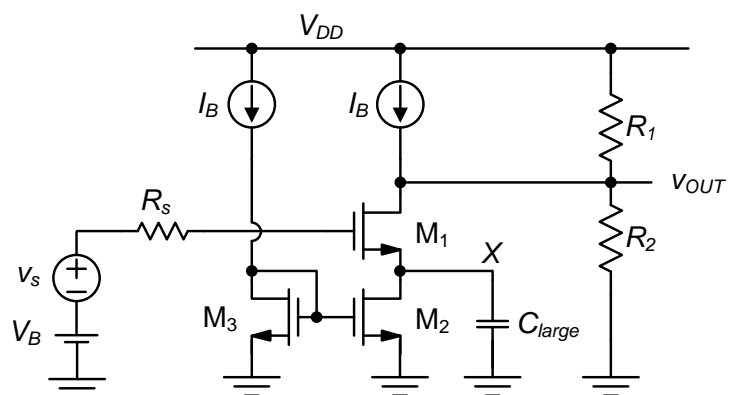


Figure 5-25

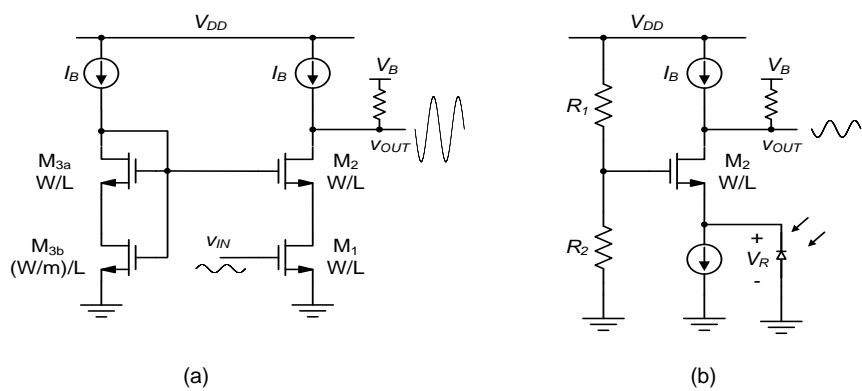


Figure 5-26

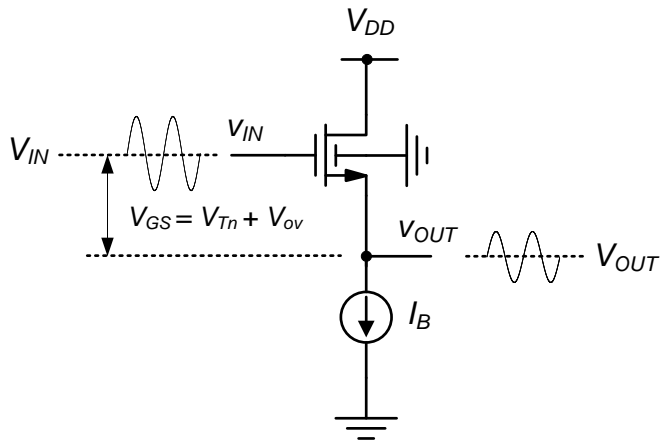
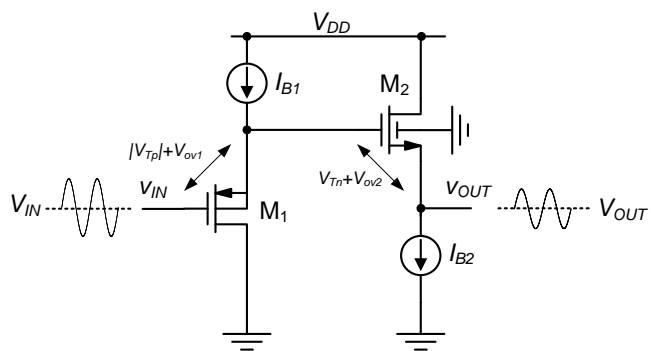
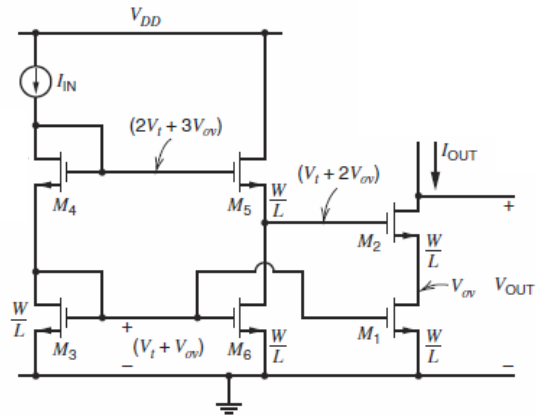


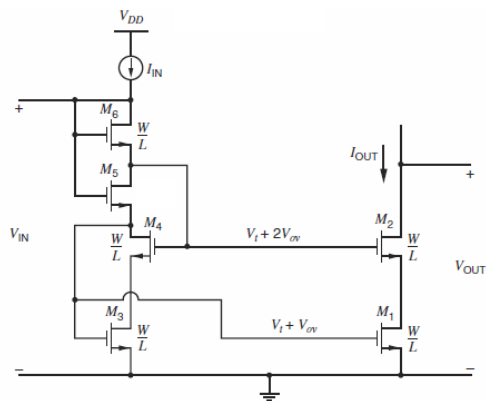
Figure 5-27



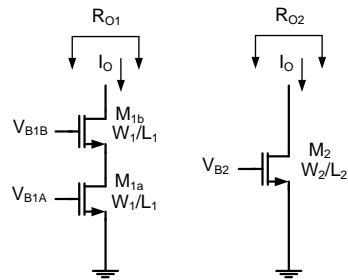
Problem P5.5



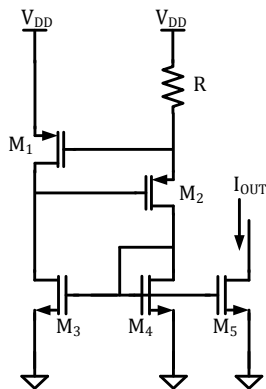
Problem P5.6



Problem P5.9

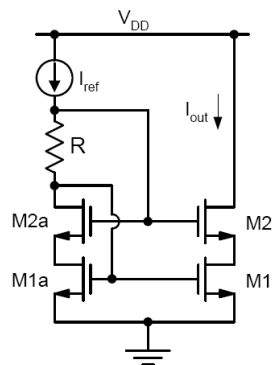


Problem P5.10



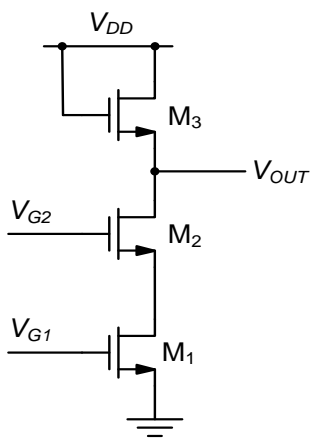
Problem P5.11

The circuit diagram shows a current mirror configuration. A reference current source I_{ref} is connected to the V_{DD} supply and a resistor R . The other end of the resistor R is connected to the gates of two NMOS transistors, M2a and M1a. The source of M2a is connected to the V_{DD} supply, and its drain is connected to the gates of two more NMOS transistors, M2 and M1. The source of M2 is connected to the V_{DD} supply, and its drain is connected to the output current I_{out} . The source of M1 is connected to the V_{DD} supply, and its drain is connected to ground. The gates of M2 and M1 are connected to the gates of M2a and M1a, respectively. The sources of M2 and M1 are connected to ground.



Problem P5.12

The diagram shows a vertical stack of three CMOS inverters. The top inverter, labeled M_3 , has its gate connected to V_{DD} and its drain connected to V_{DD} . Its source is connected to the output node V_{OUT} . The middle inverter, labeled M_2 , has its gate connected to V_{G2} and its drain connected to V_{OUT} . Its source is connected to the input of the bottom inverter. The bottom inverter, labeled M_1 , has its gate connected to V_{G1} and its drain connected to the input of the middle inverter. Its source is connected to ground. The gates of M_2 and M_1 are connected to V_{G2} and V_{G1} respectively, which are shown as input signals.



Problem P5.13

