

Figure 1-1

The diagram illustrates the architecture of a Mixed-Signal Integrated Circuit. On the left, a cloud-shaped block labeled "Analog Media and Transducers" is connected to a dashed rectangular box representing the "Mixed-Signal Integrated Circuit". Inside this box, the signal path is as follows: an arrow points from the cloud to a "Signal Conditioning" block, then to an "A/D" (Analog-to-Digital) converter, then to a "Digital Processing" block. From the "Digital Processing" block, an arrow points to a "D/A" (Digital-to-Analog) converter, then to another "Signal Conditioning" block, and finally back to the cloud. Below the cloud, the text "Sensors, Actuators, Antennas, Storage Media, ..." is listed.

```
graph LR;
    Cloud((Analog Media and Transducers)) --> SC1[Signal Conditioning];
    subgraph MSIC [Mixed-Signal Integrated Circuit];
        SC1 --> AD[A/D];
        AD <--> DP[Digital Processing];
        DP <--> DA[D/A];
        DA --> SC2[Signal Conditioning];
    end;
    SC2 --> Cloud;
```

Sensors, Actuators,
Antennas, Storage Media, ...

Figure 1-2

The diagram illustrates the internal architecture of the RFIC, organized into several functional blocks and their interconnections:

- Power and Clock Management:**
 - Battery Management:** Provides the main power source V_{BAT} to the **Power Management (PM)** block.
 - Power Management (PM):** Distributes power to the **Digital Baseband Processor**, **Internal DRP Processor**, **Power Management (PM)** block itself, and the **RF Built-in Self Test (RF-BIST)**.
 - Crystal:** An external crystal X_{tal} provides a reference frequency F_{REF} to the **Dither DCXO** and the **Digital logic**.
- Digital Baseband Processor:** A central digital block that interfaces with **SRAM** and the **Internal DRP Processor**.
- Internal DRP Processor:** Manages internal digital resources and provides a **Processor clock** to the **Dividers** and **Digital logic**.
- Transmit Path (TX):**
 - Dither DCXO:** Generates a clock signal F_{REF} for the **Digital logic**.
 - Digital logic:** Receives F_{REF} and provides control signals to the **Amplitude modulation** block and the **DCO**.
 - Amplitude modulation:** A $\Sigma\Delta$ modulator that shapes the digital baseband signal.
 - DCO (Digital Controlled Oscillator):** Generates the **LO clock** based on digital inputs.
 - TDC (Time-to-Digital Converter):** Provides feedback to the **Digital logic** based on the **LO clock**.
 - DPA (Digital Power Amplifier):** Converts the digital baseband signal into an analog signal.
 - TX:** The output of the **DPA** is sent to the **Front-end Module**.
- Receive Path (RX):**
 - RF In:** The received signal enters the **Front-end Module**.
 - Front-end Module:** Contains a **2-watt PA**, a **T/R switch**, and **RX SAW filters**.
 - LNA + TA (Low Noise Amplifier + Tuning Amplifier):** Amplifies the received signal.
 - Current sampler:** Samples the current of the **LNA + TA** output.
 - Discrete time:** A $\Sigma\Delta$ modulator that converts the sampled current into a digital signal.
 - A/D (Analog-to-Digital Converter):** Converts the discrete-time signal into a digital baseband signal.
 - Digital logic:** Receives the digital baseband signal and provides control to the **Discrete time** block.
- Test and Control:**
 - Dividers:** Generate various clock signals from the **Processor clock**.
 - RF Built-in Self Test (RF-BIST):** Performs self-testing on the RF path.

Figure 1-3

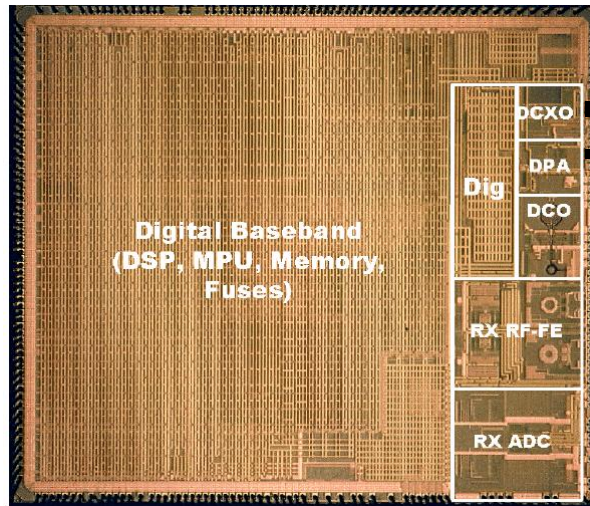


Figure 1-4

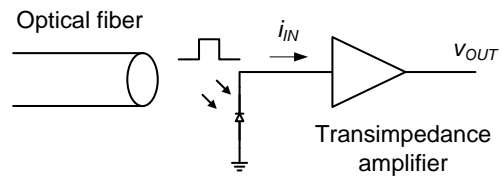


Figure 1-5

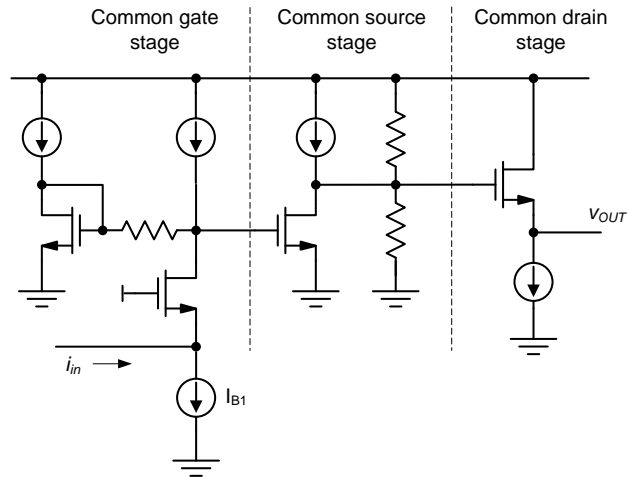


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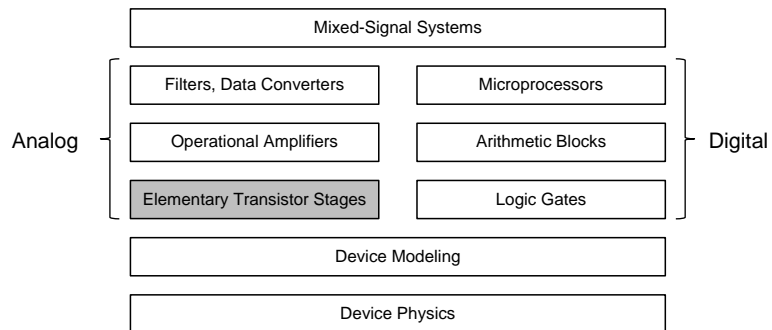


Figure 1-7

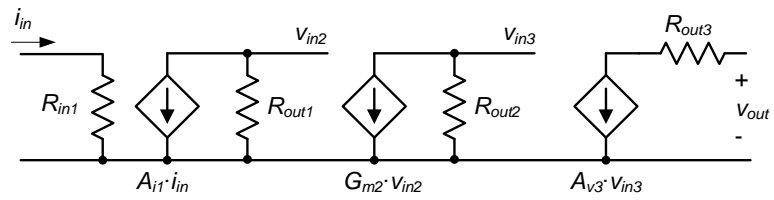


Figure 1-8

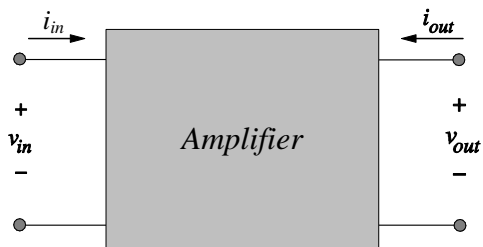
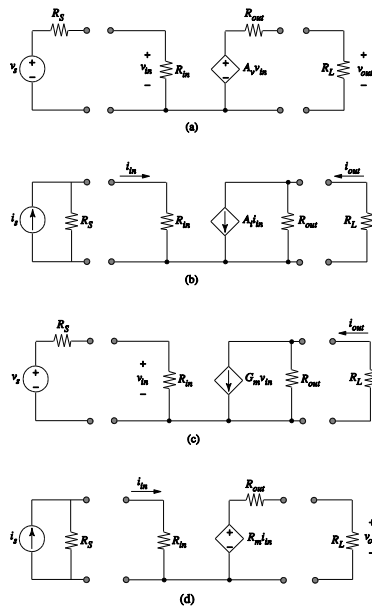


Figure 1-9



(Howe & Sodini, Figure 8.2)

Figure 1-10

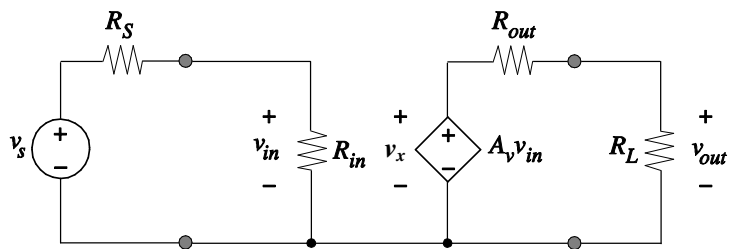
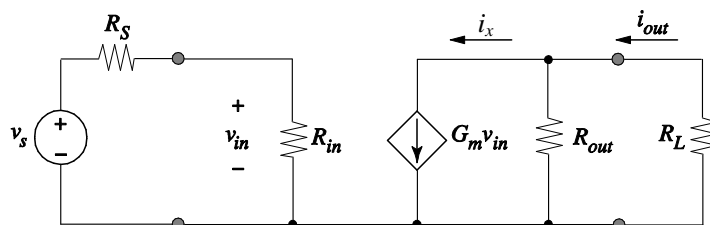


Figure Ex1-1



(Howe & Sodini, Figure 8.5)

Figure 1-11

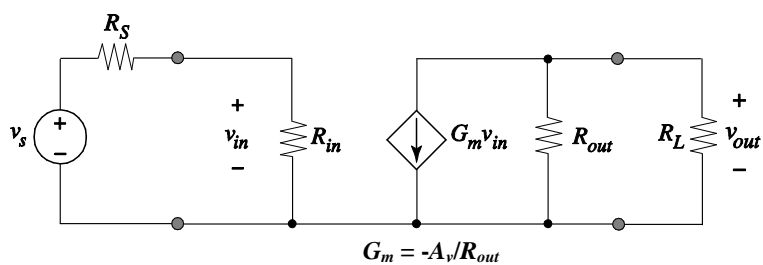


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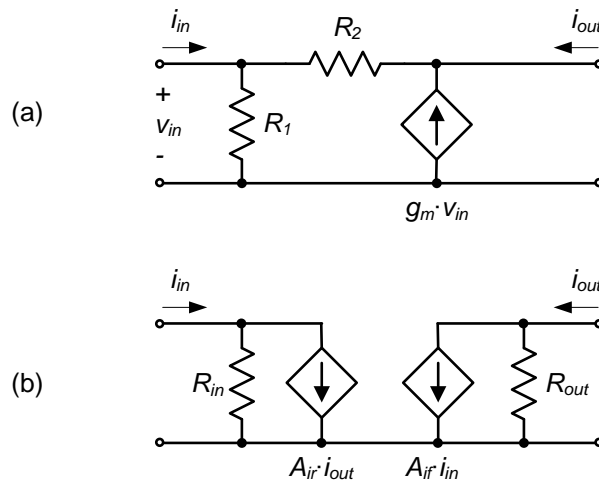
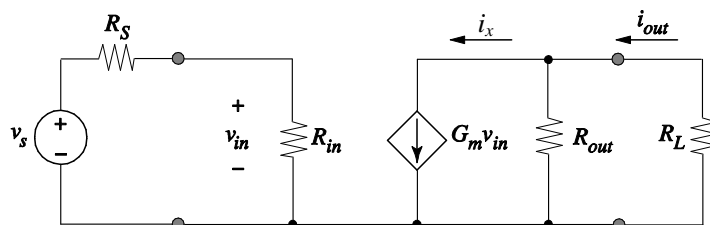


Figure Ex1-1



(Howe & Sodini, Figure 8.5)

Figure 1-13

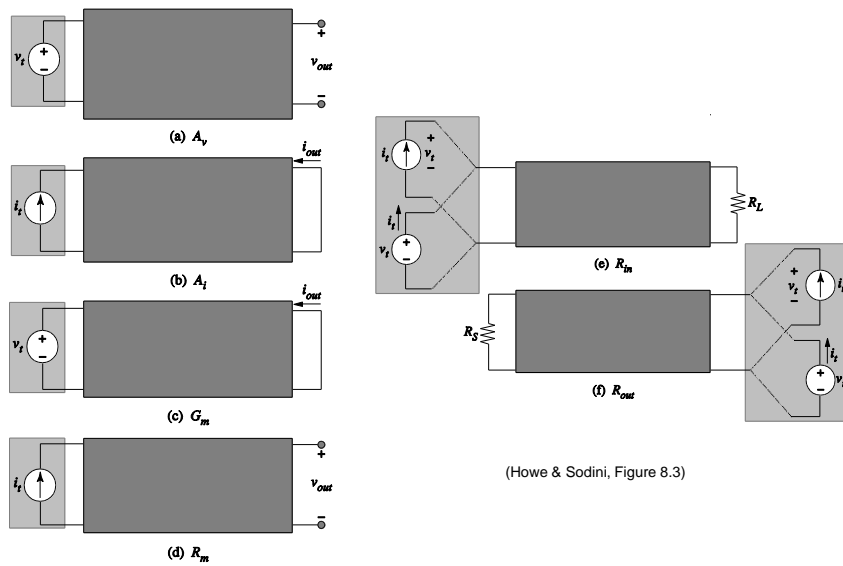
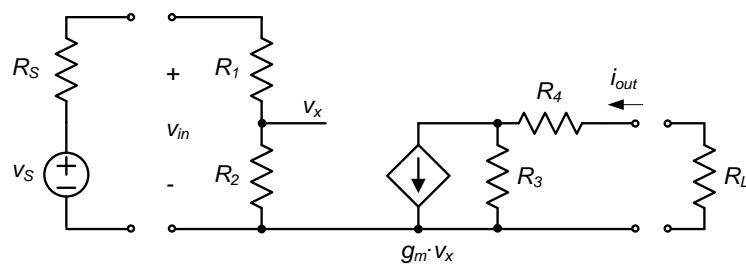
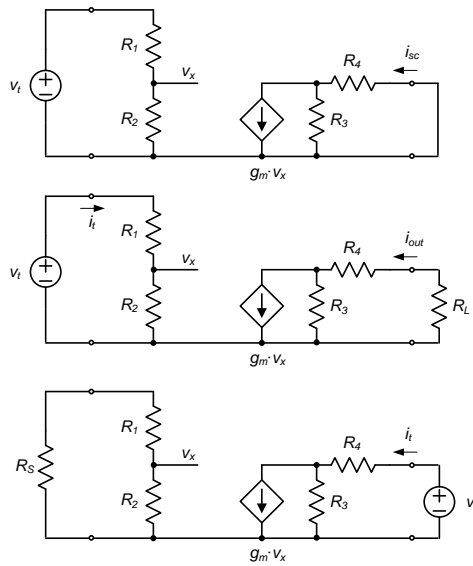


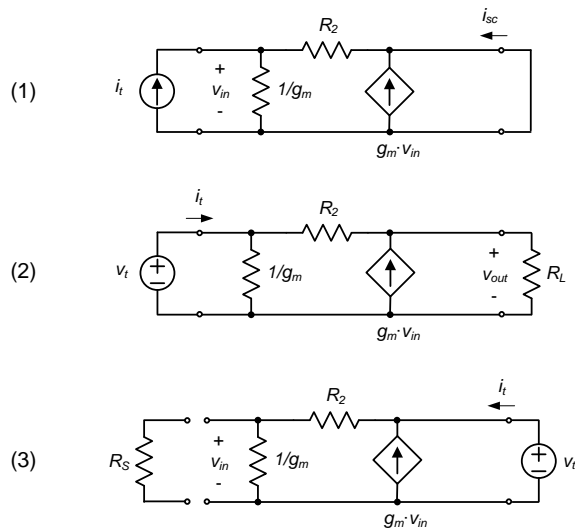
Figure Ex1-2



Ex1-2 (Solution)



Ex1-3 (Solution)



Ex1-3 (Solution)

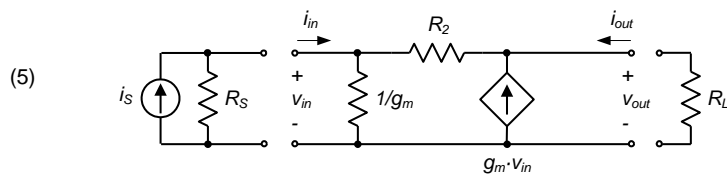
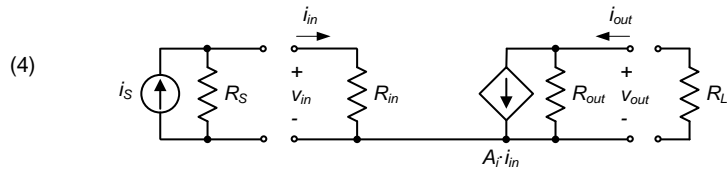


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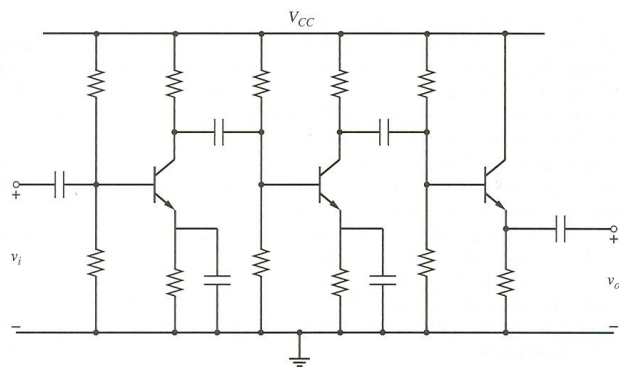


Figure P1-1

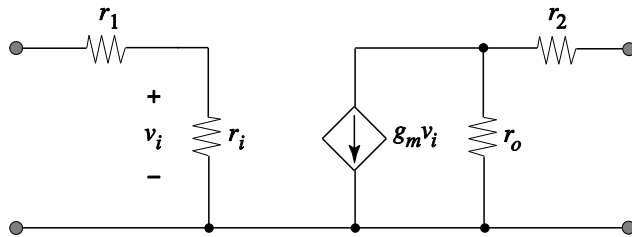


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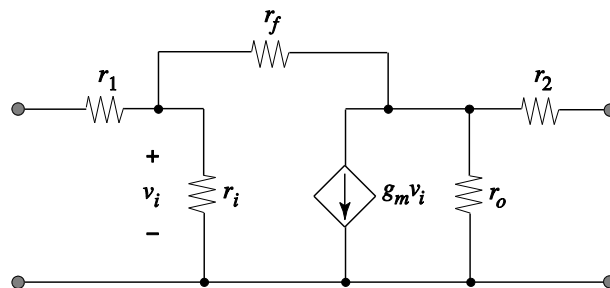


Figure 2-1

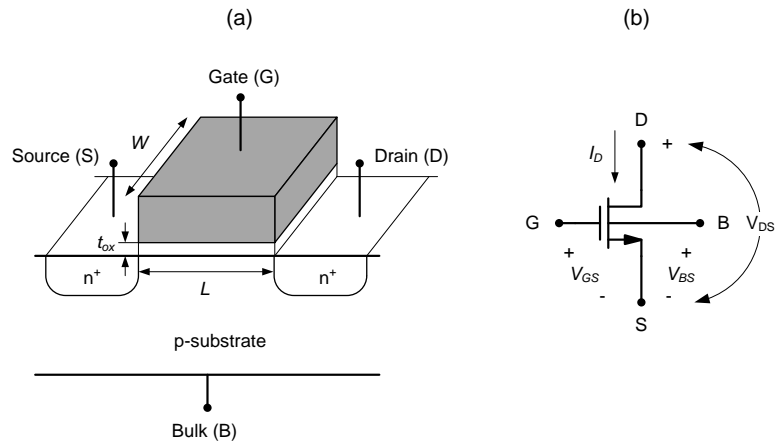


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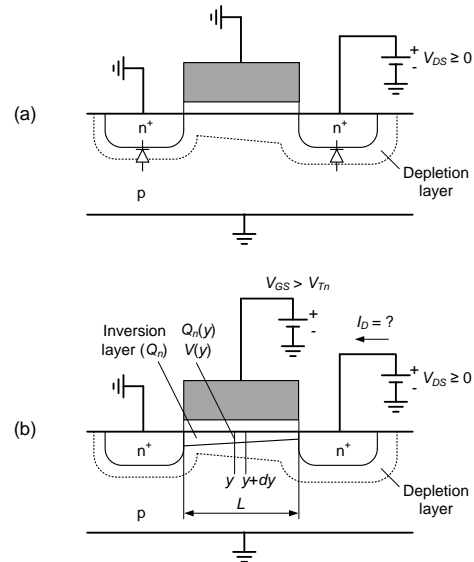


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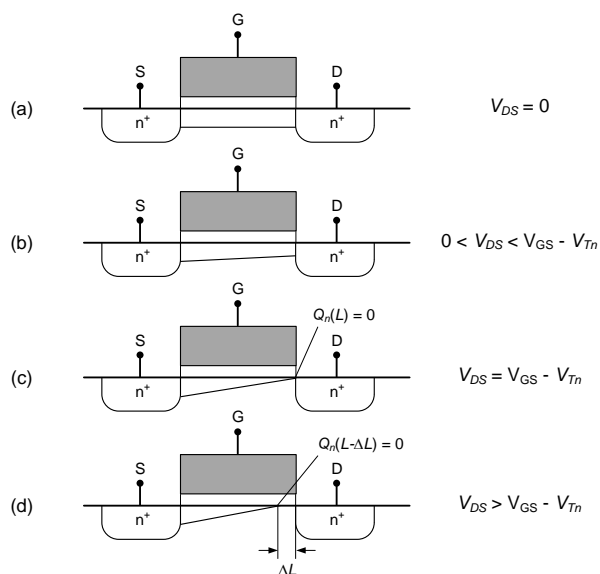


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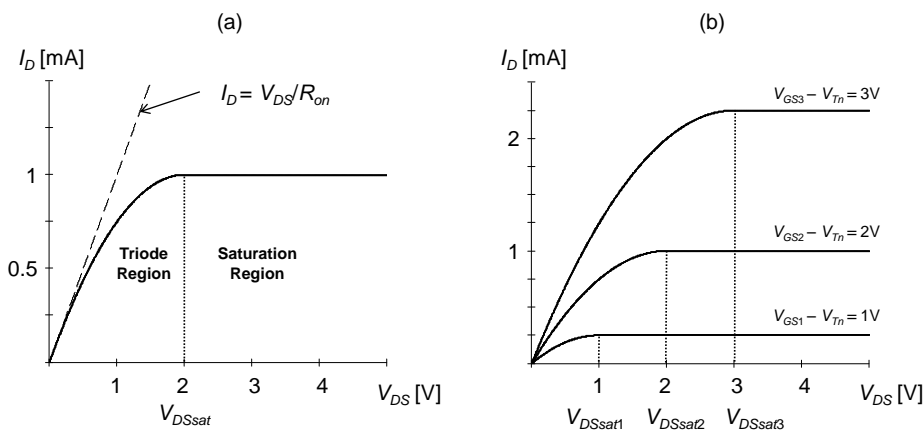


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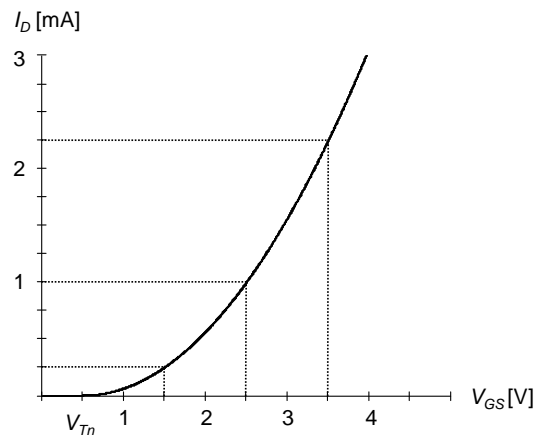


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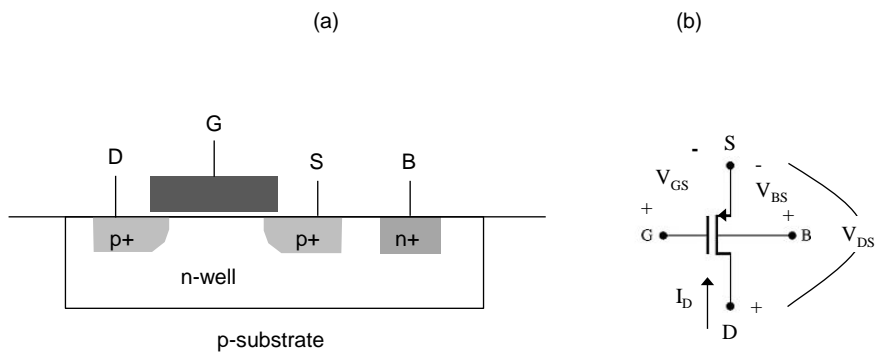


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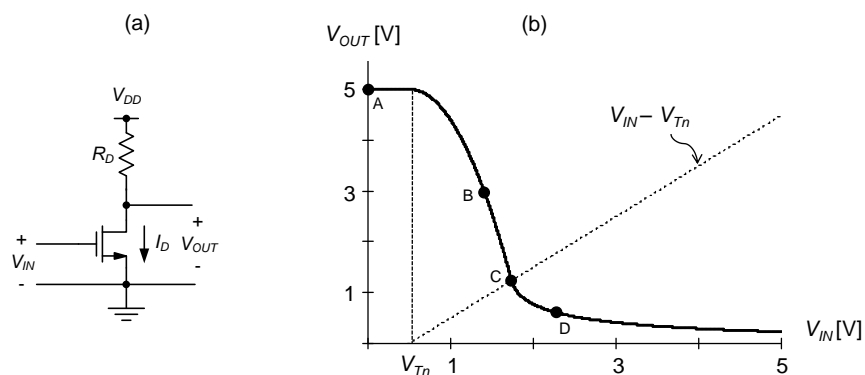


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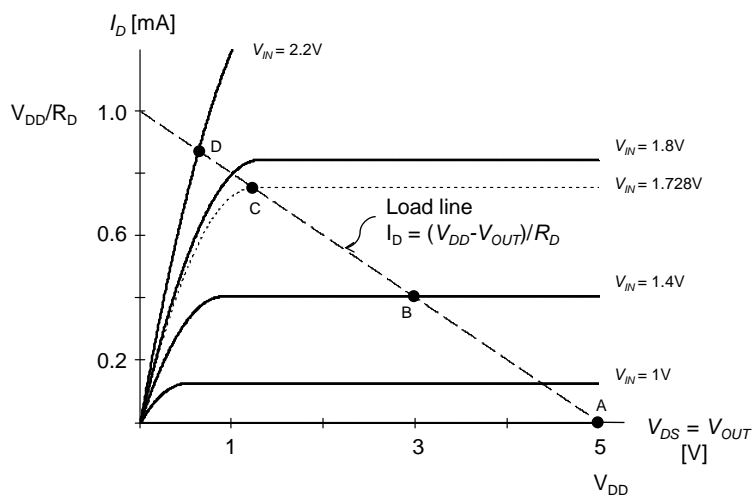


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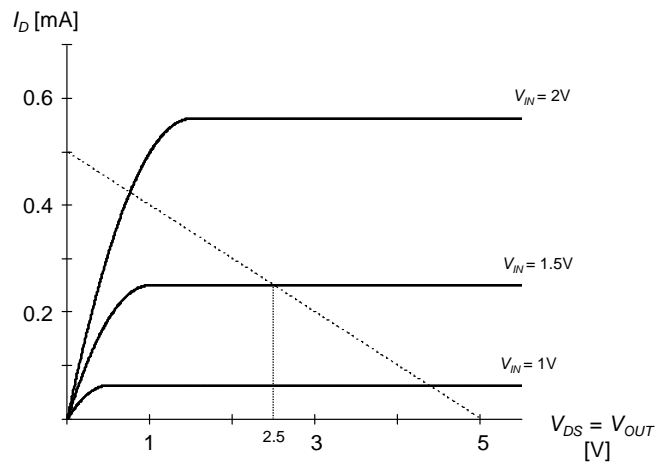


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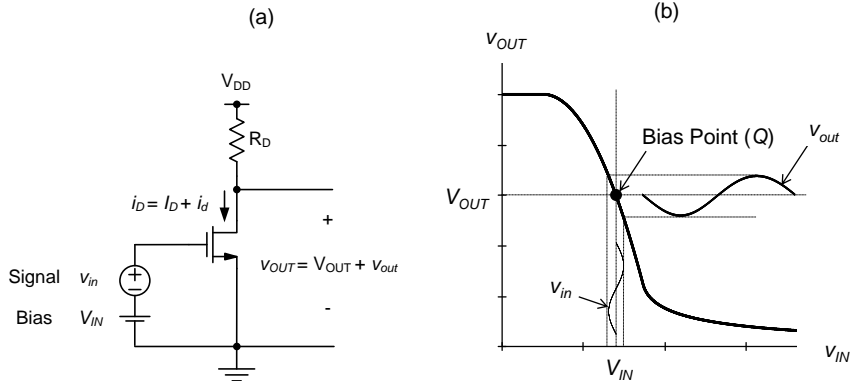


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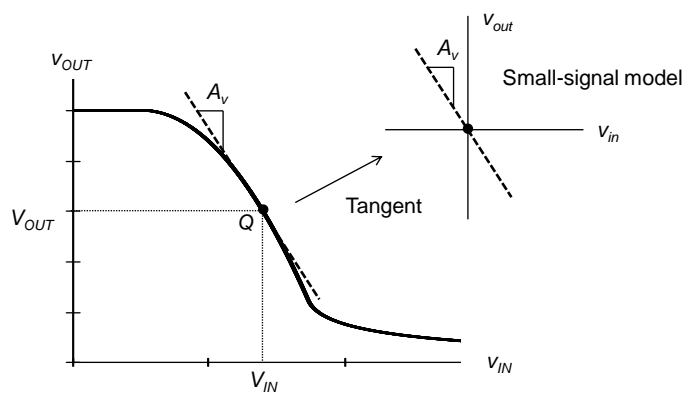


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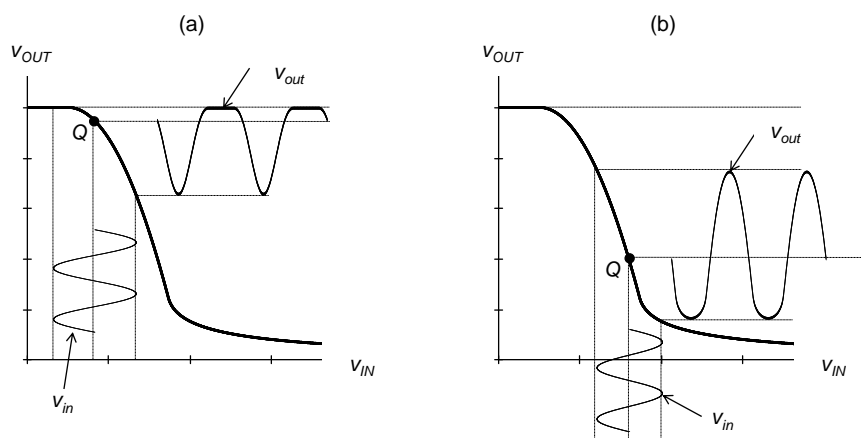


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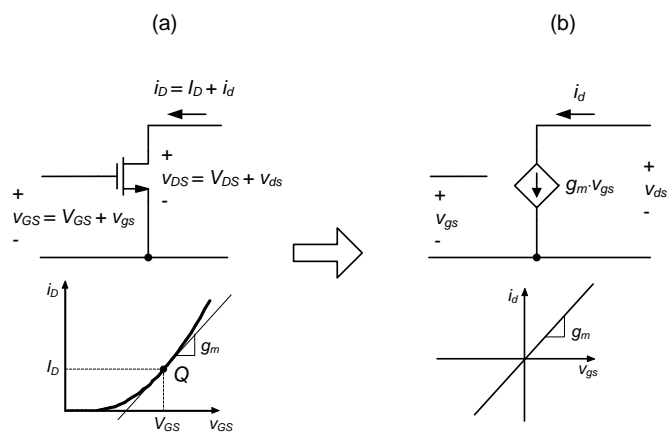


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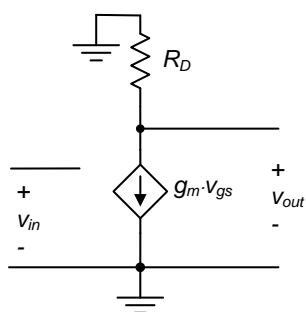


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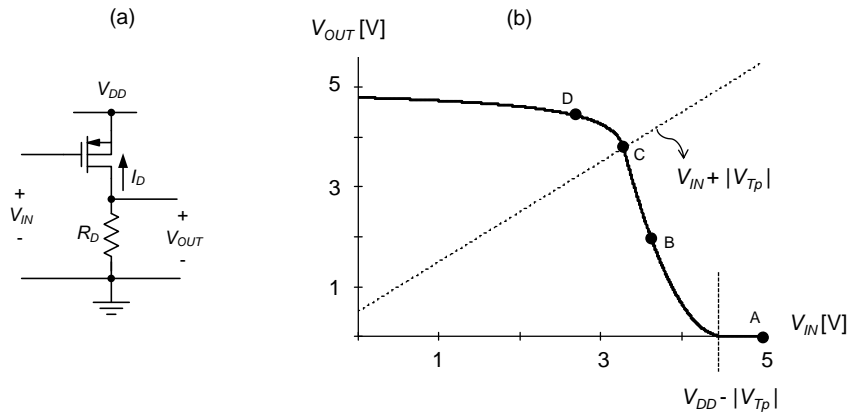


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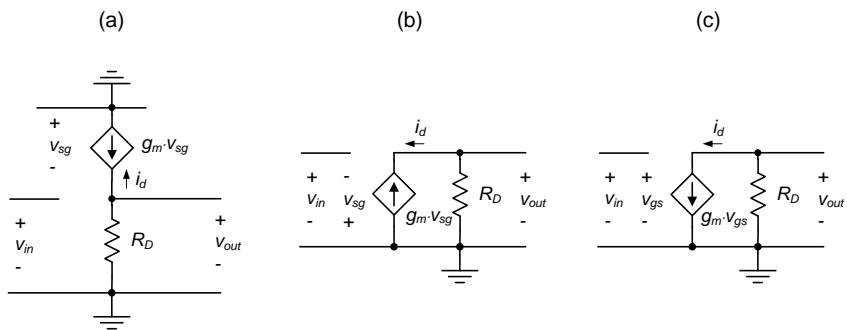


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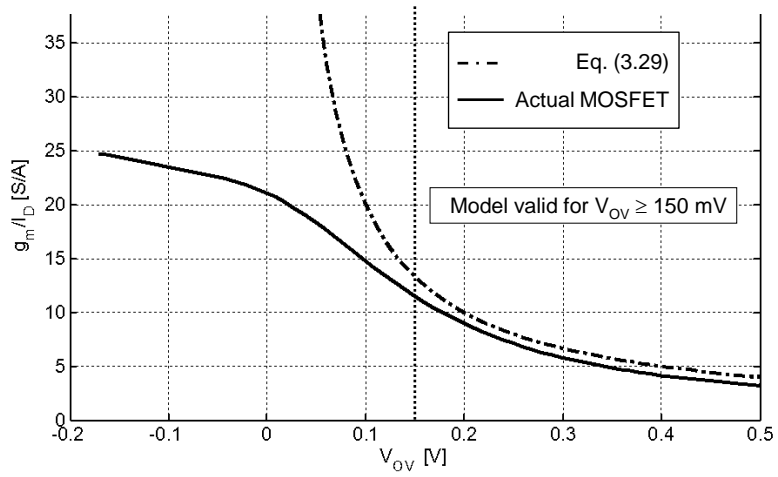


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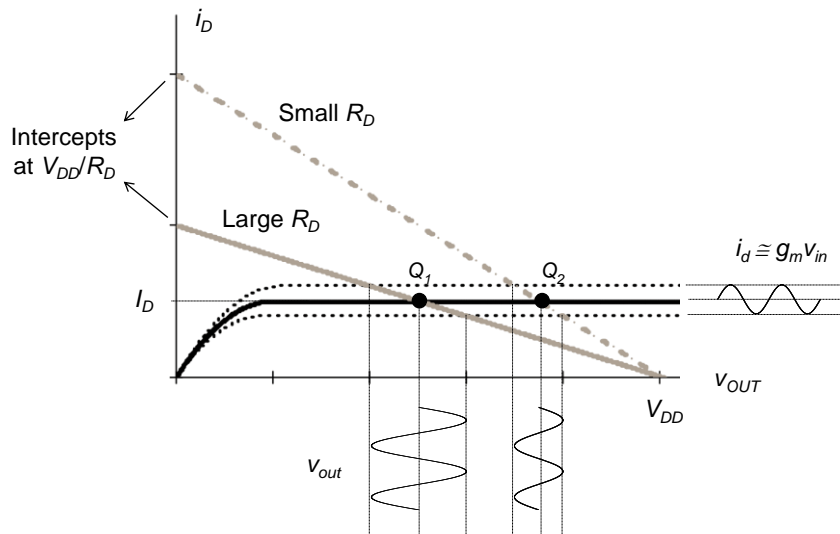


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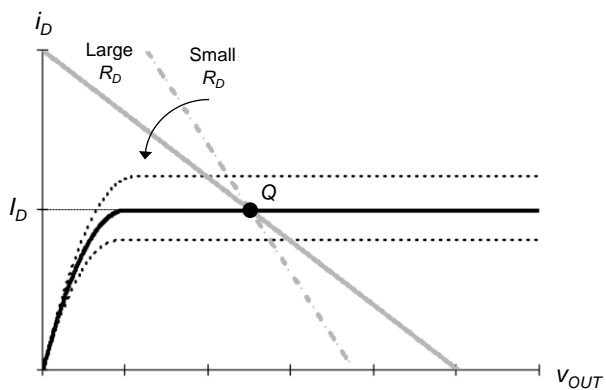


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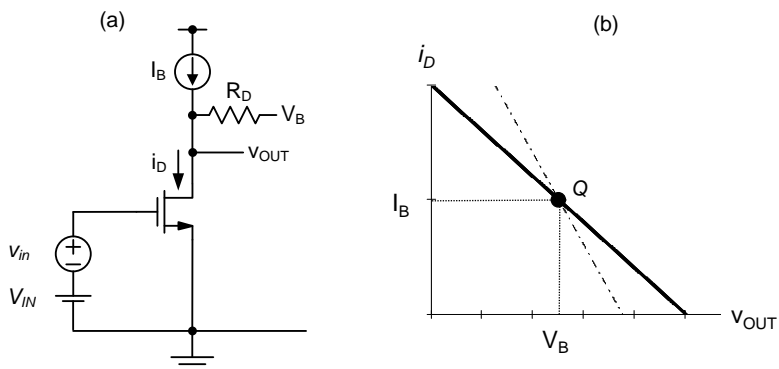


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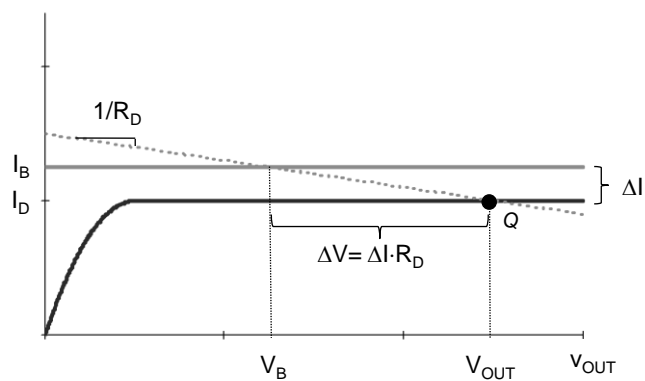


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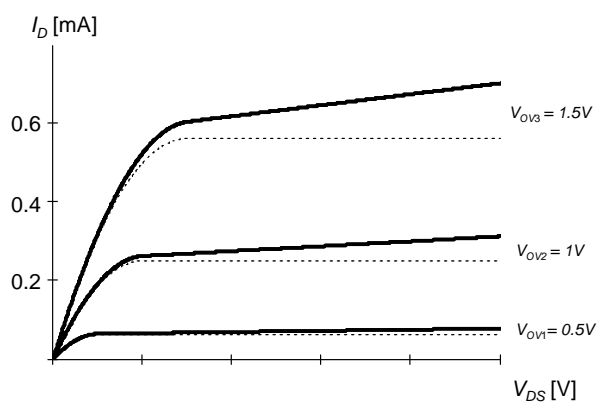


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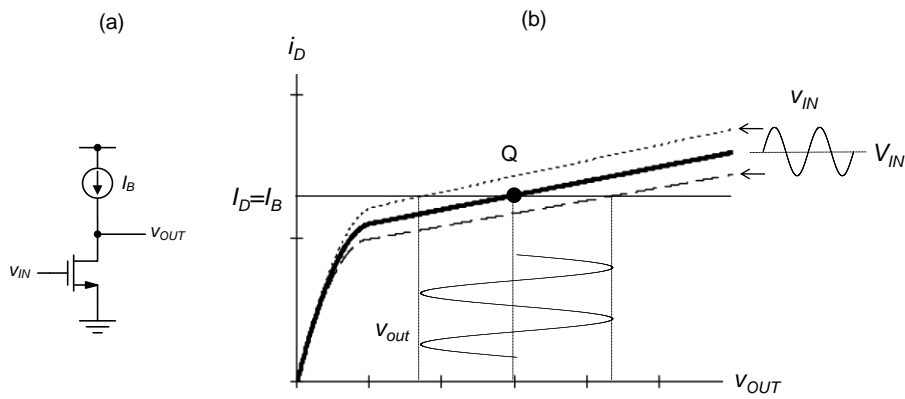


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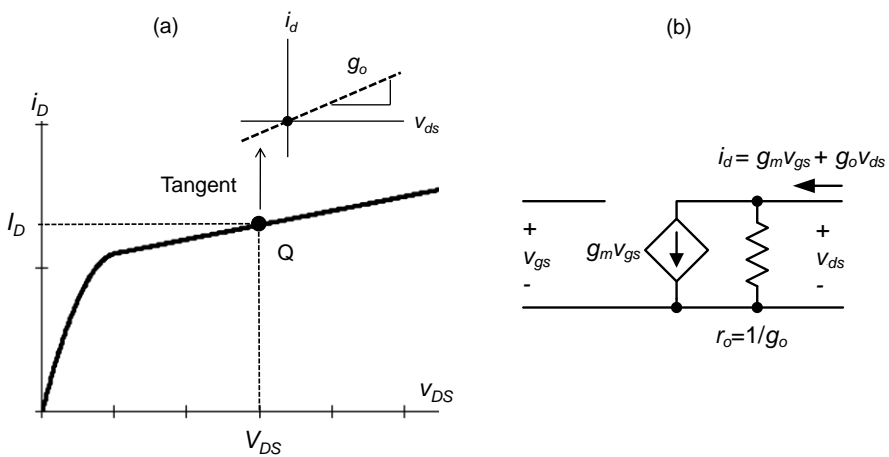


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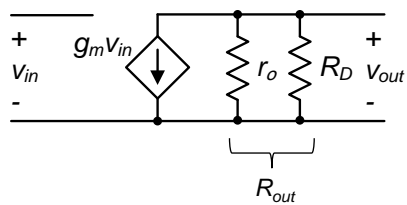


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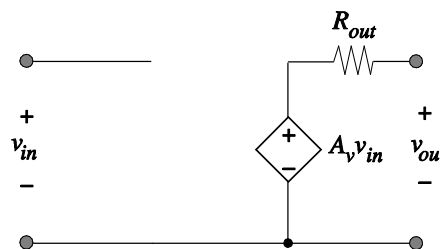


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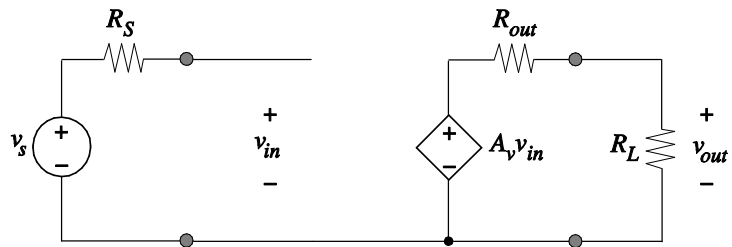


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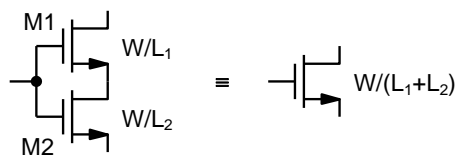


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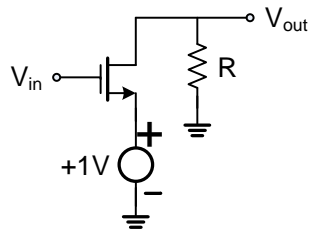


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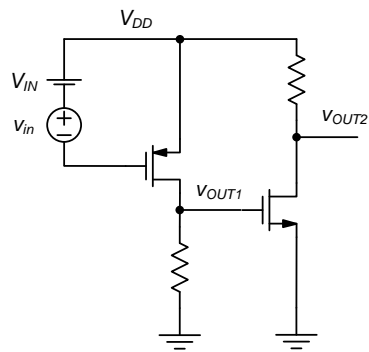


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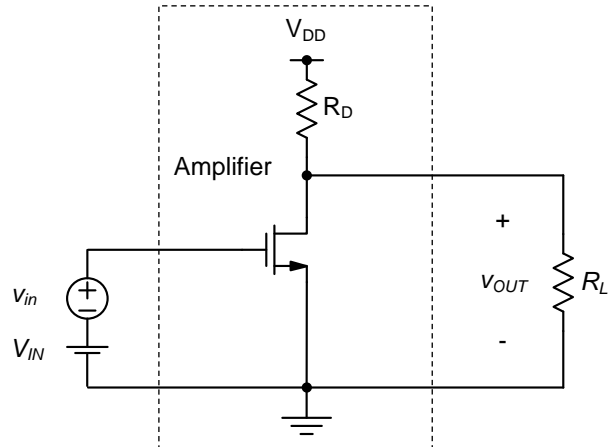


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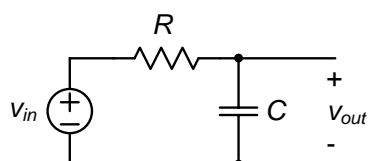
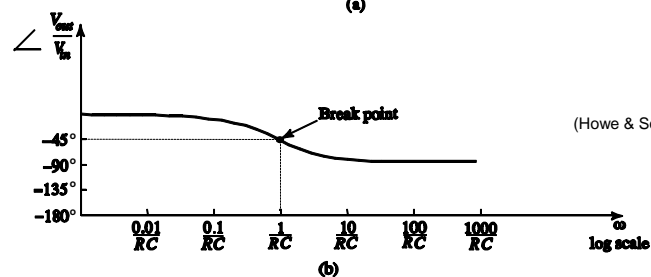
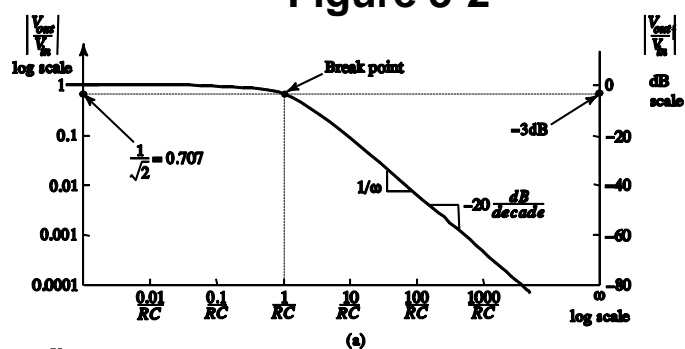


Figure 3-2



(Howe & Sodini, Figure 10.2)

Figure 3-3

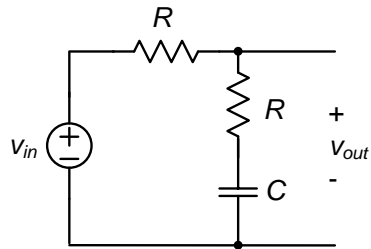


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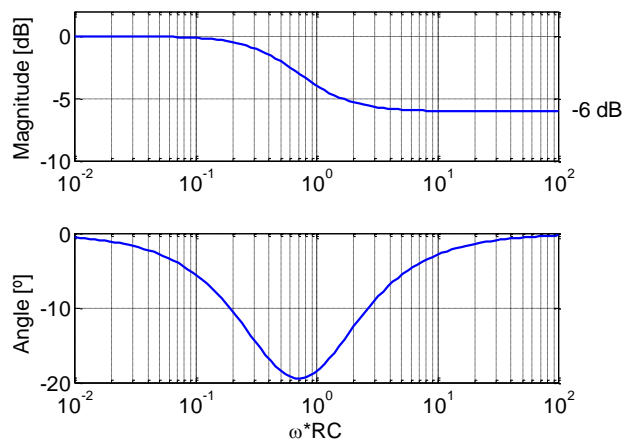


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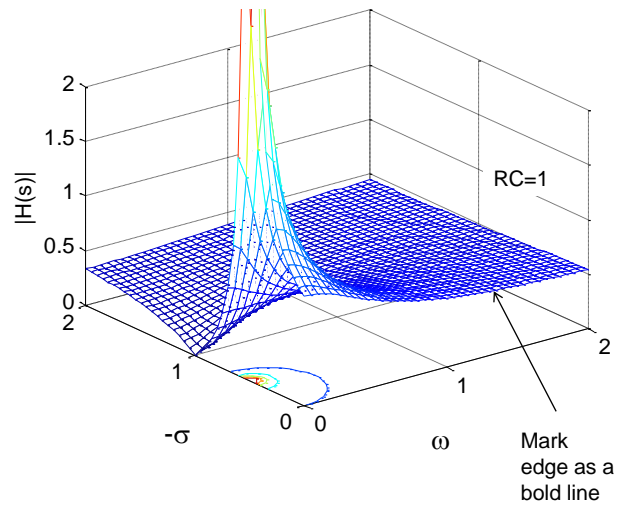


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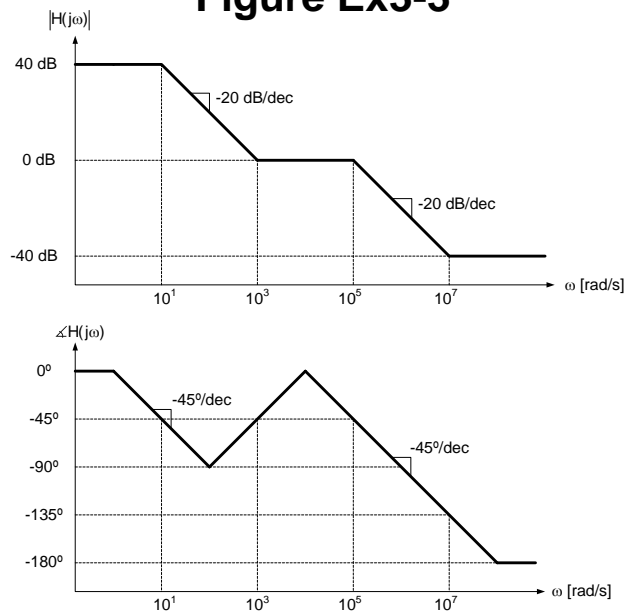


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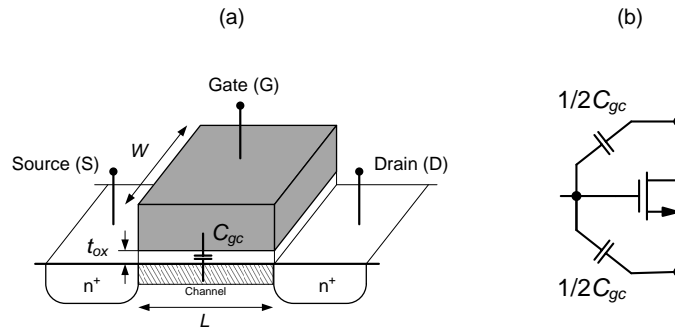


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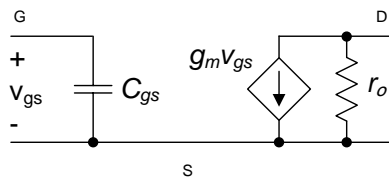


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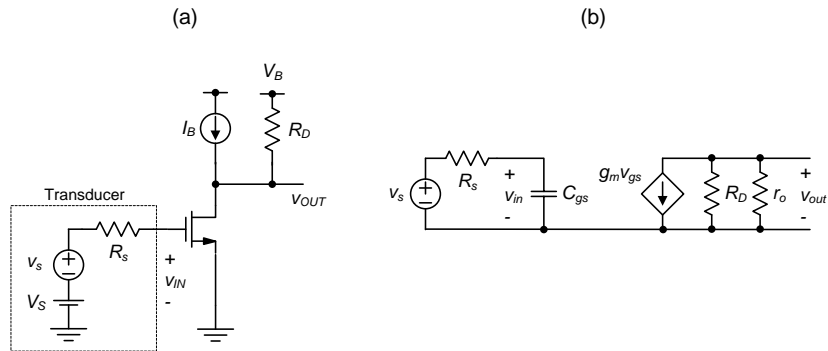


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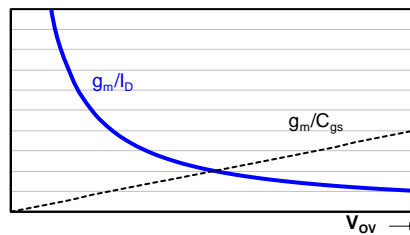


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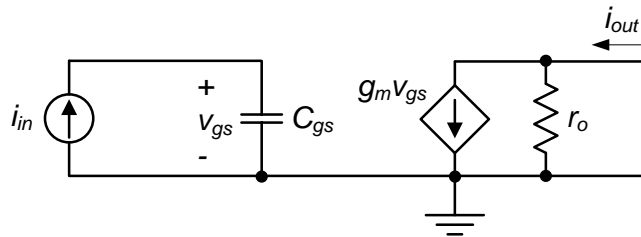
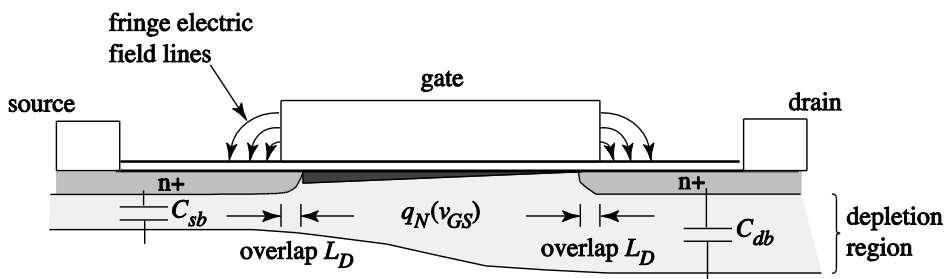


Figure 3-10



(Howe & Sodini, Figure 4.23)

Figure 3-11

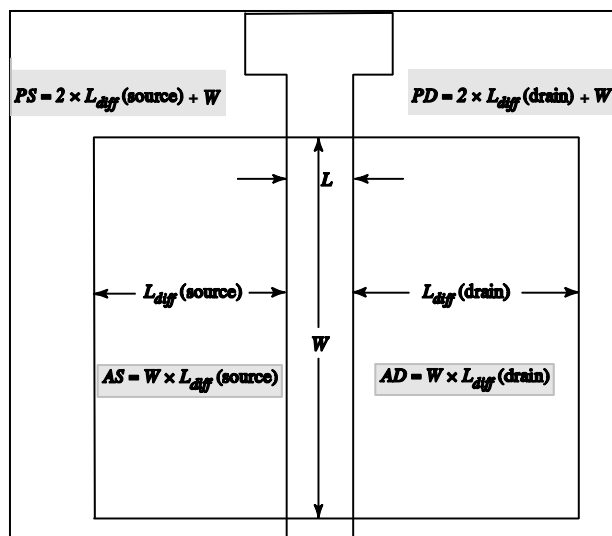


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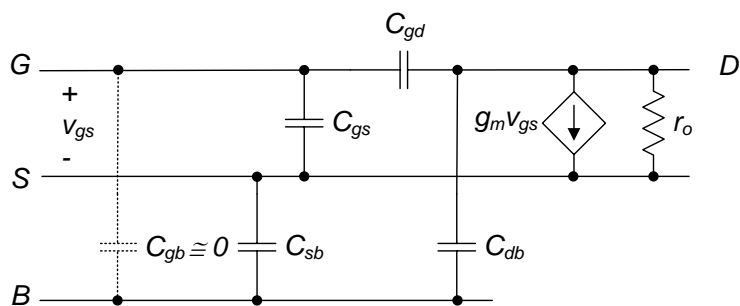


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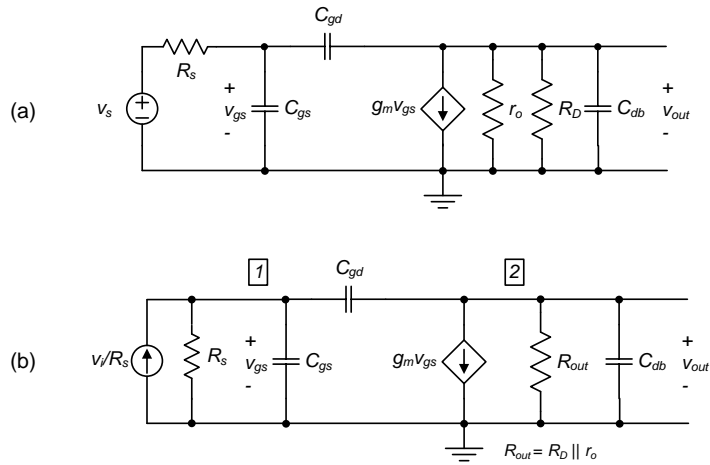


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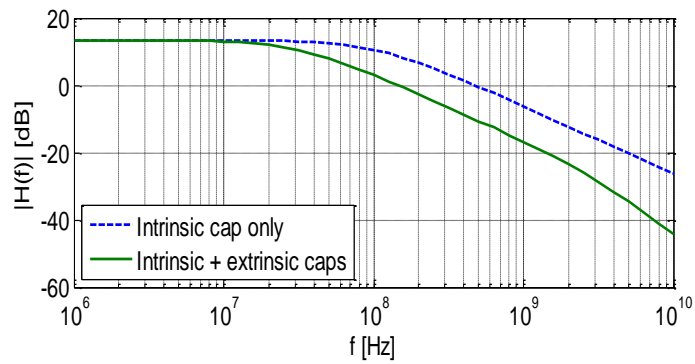


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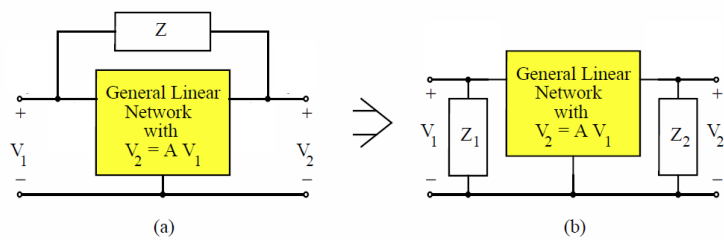


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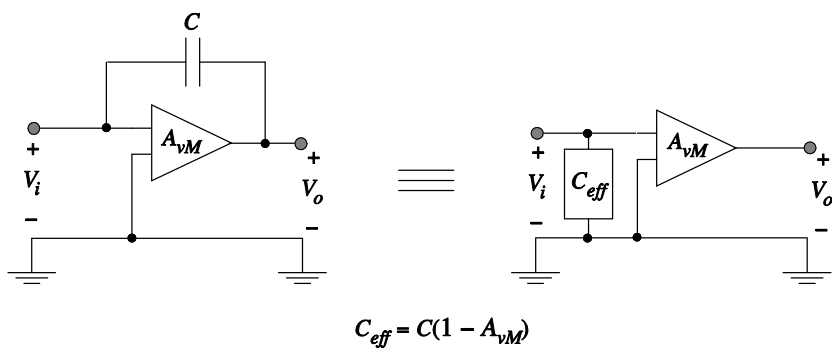


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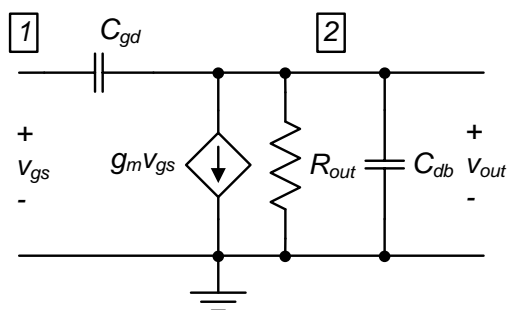


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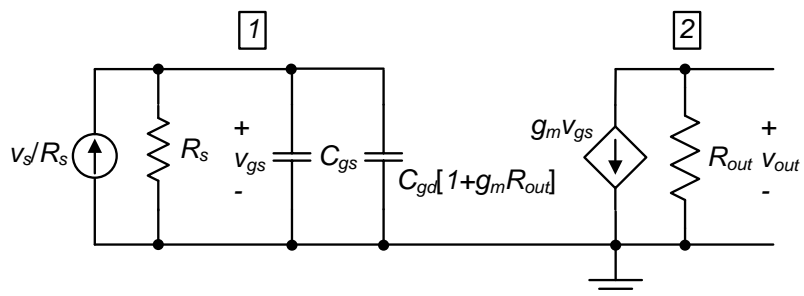


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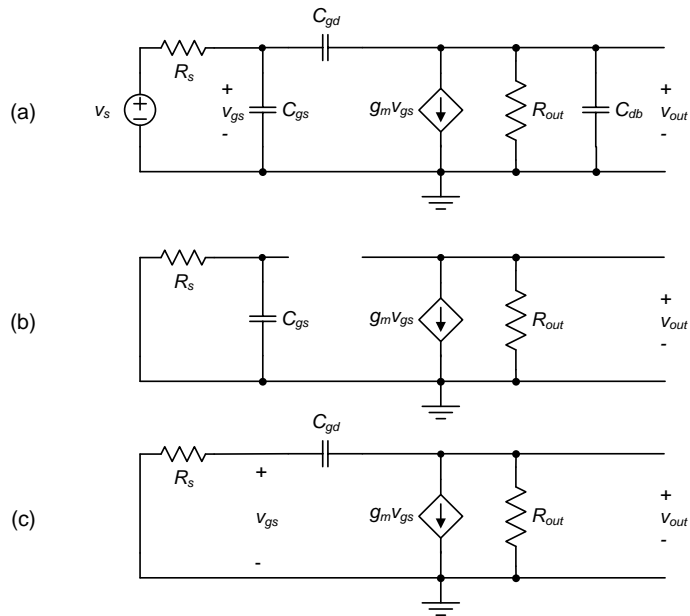


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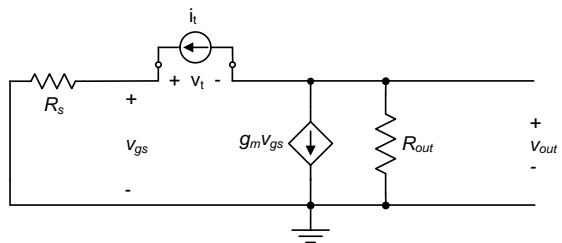


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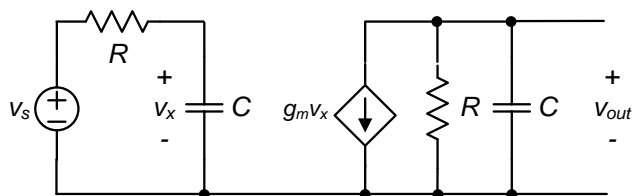


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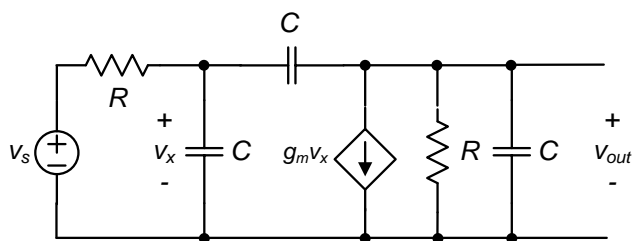


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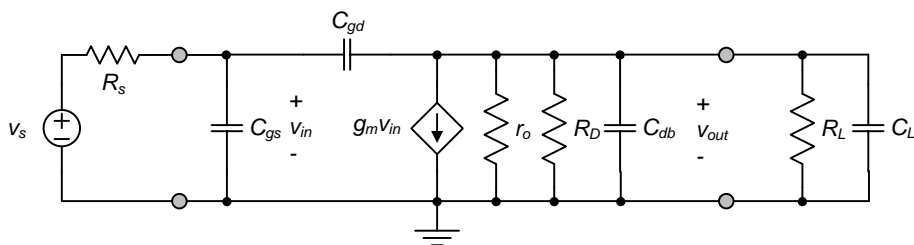


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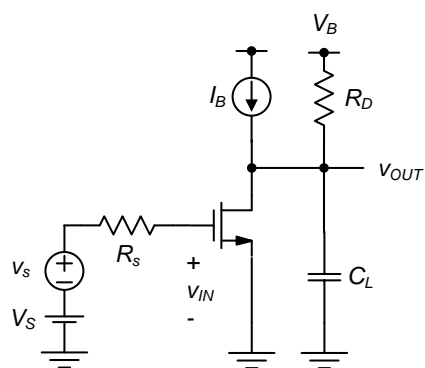


Figure P3.3

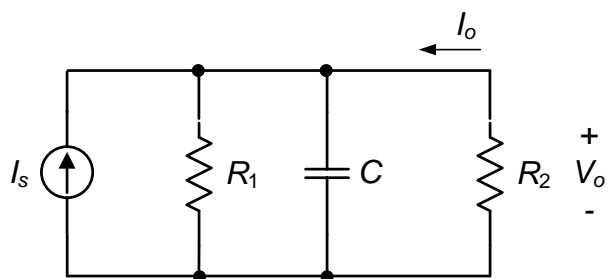


Figure P3.7

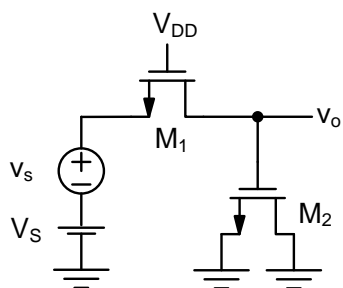


Figure P3-13

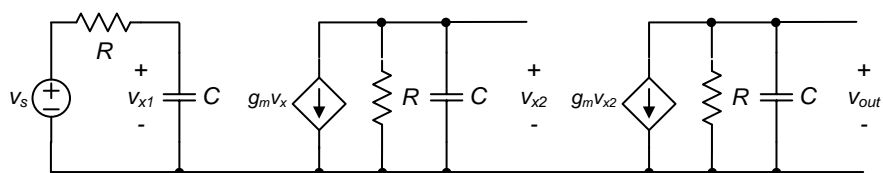


Figure P3-16

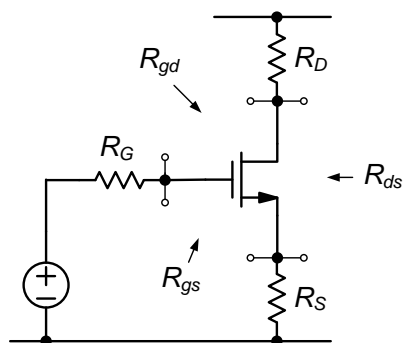


Figure P3-17

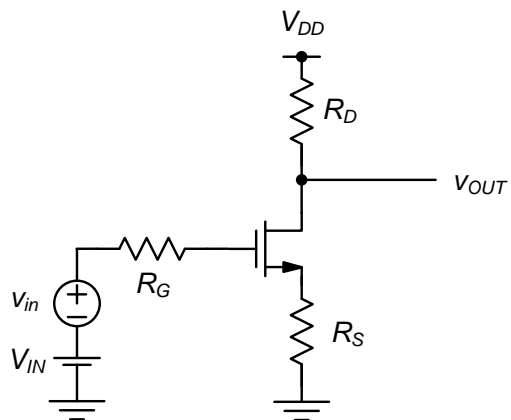


Figure 4-1

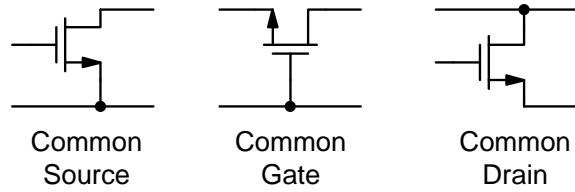


Figure 4-2

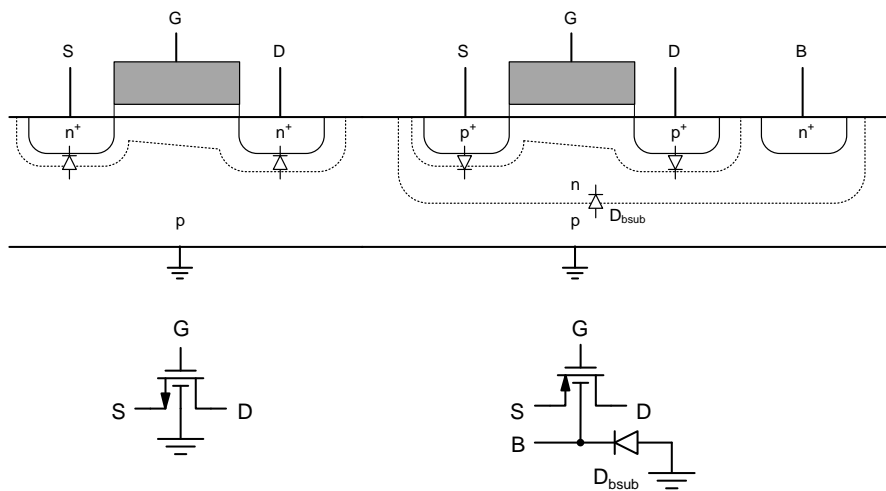


Figure 4-3

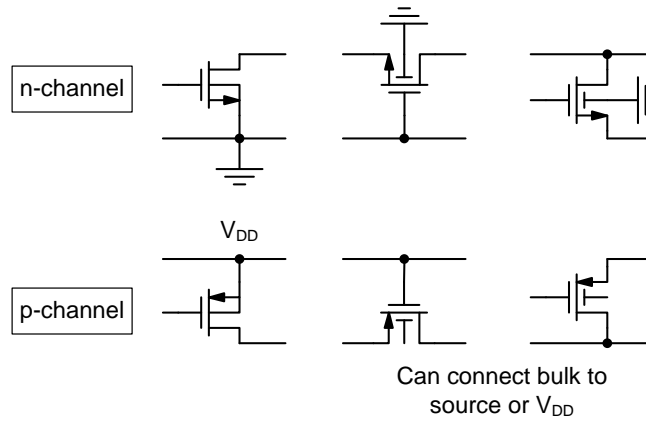


Figure 4-4

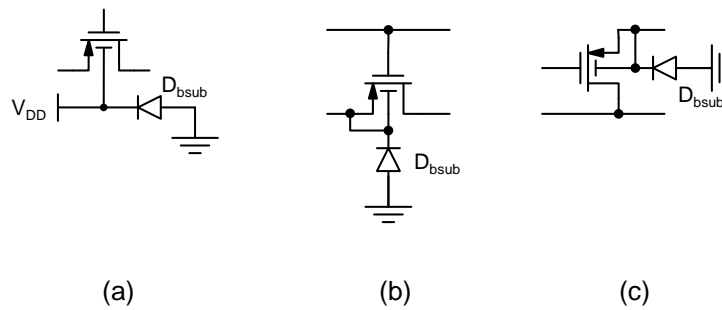


Figure Ex4-1

The diagram illustrates a well system within a rectangular boundary. On the left, a well is shown with a central gravel pack (G) of length L and two filter zones (S and D) of length L_{diff} each. The total width of the well is W . The distance from the well to the gravel pack is $X1$, and the distance from the gravel pack to the well contact is $X2$. The well contact is a vertical line on the right. The distance from the well contact to the right boundary is $X1$. The well contact is labeled "Well Contact".

Figure 4-5

The diagram illustrates a MOSFET structure with a gate, source, and drain. The source is connected to a negative bias V_{SB} relative to the substrate (ground). The gate is connected to a positive bias V_{GS} . The drain is connected to a positive bias V_{DS} relative to the source. A drain current I_D is shown flowing from the drain to the source. Two depletion regions are highlighted: a solid line represents the depletion layer for $V_{SB} = 0$, and a dashed line represents the depletion layer for $V_{SB} > 0$. The dashed line shows an increased depletion width in the channel region due to the reverse bias V_{SB} .

Figure 4-6

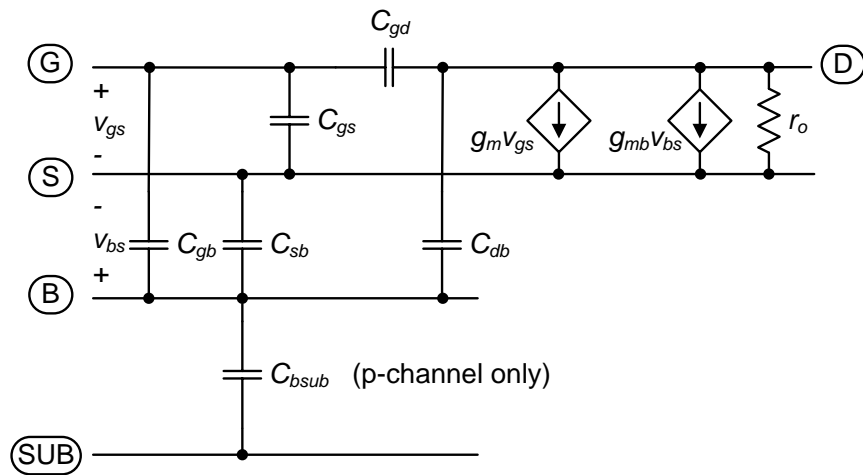


Figure 4-7

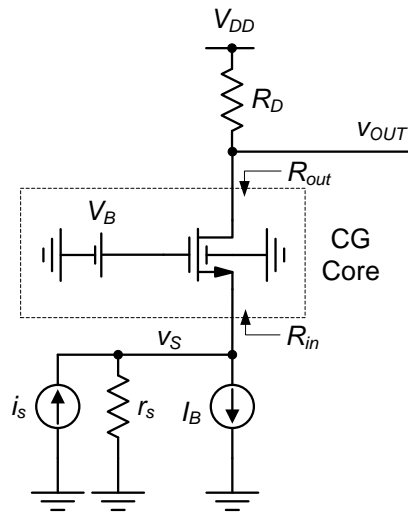


Figure 4-8

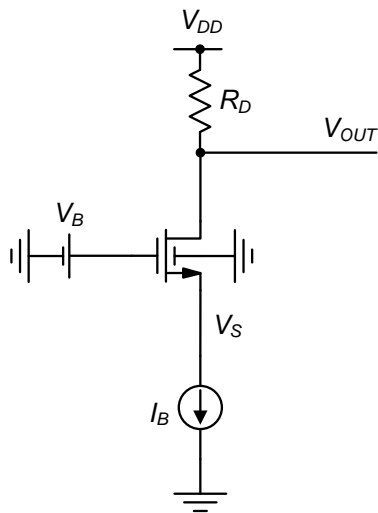


Figure 4-9

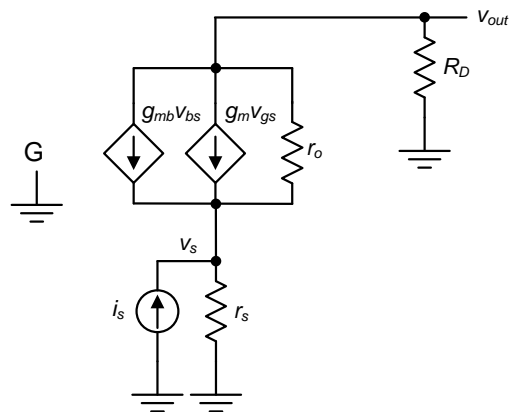


Figure 4-10

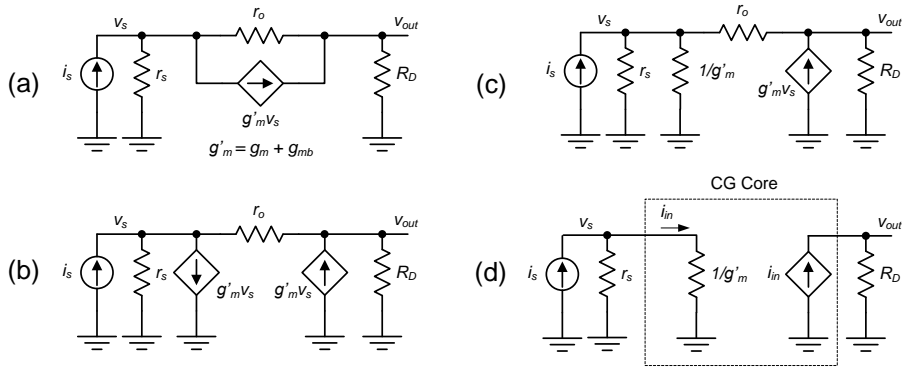


Figure 4-11

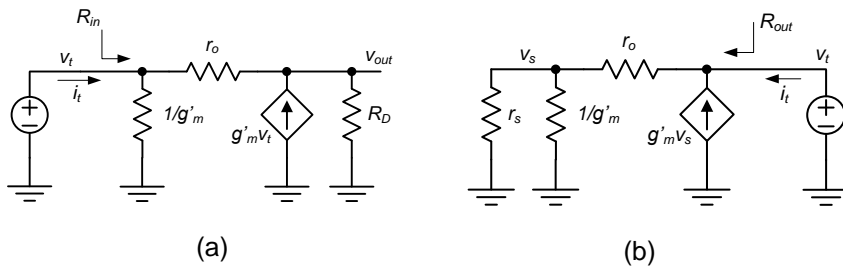


Figure 4-12

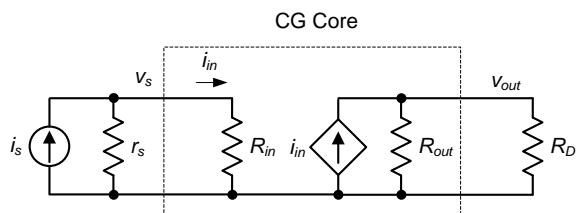


Figure 4-13

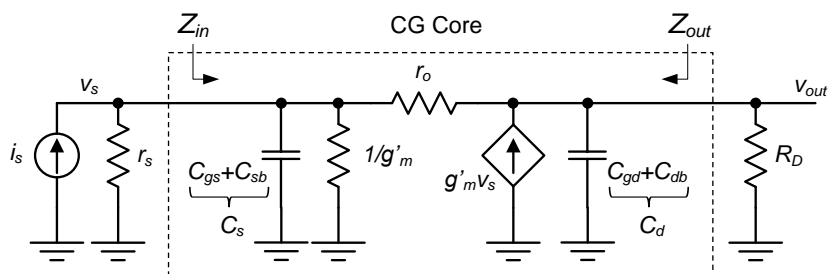


Figure 4-14

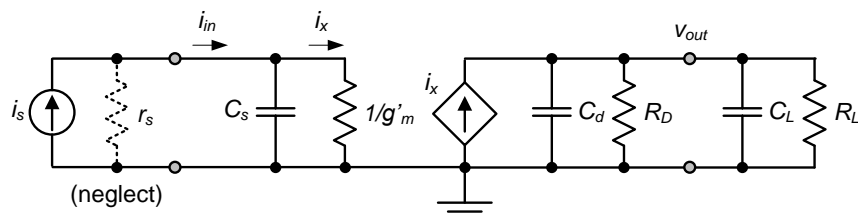


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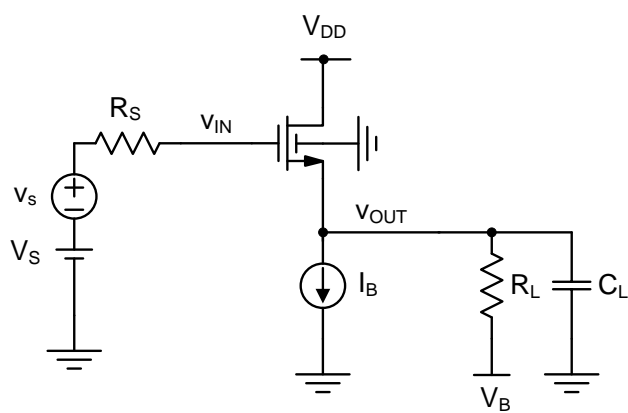


Figure 4-16

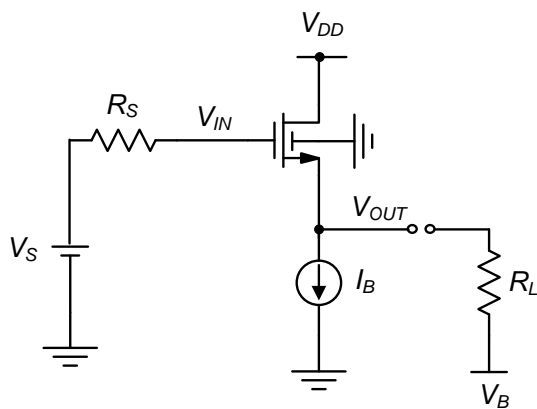


Figure 4-17

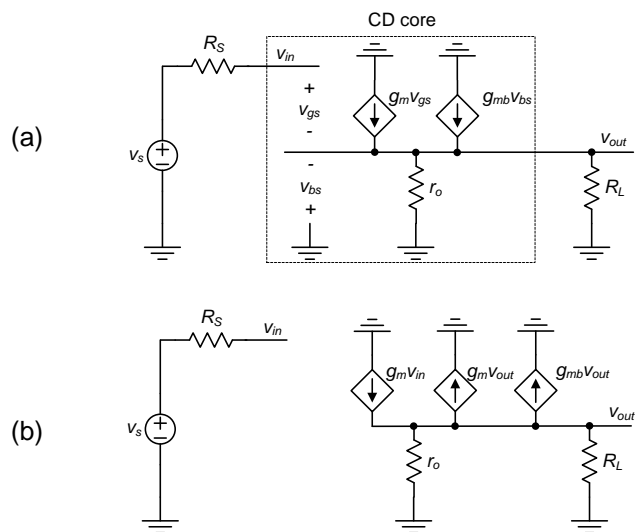


Figure 4-17 (continued)

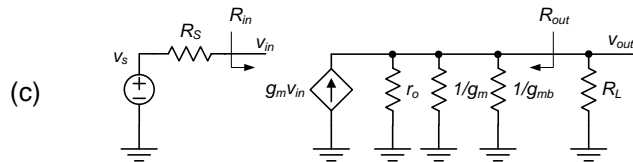


Figure 4-18

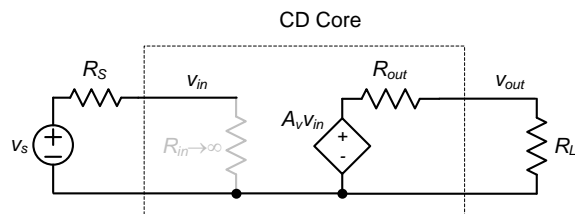


Figure 4-19

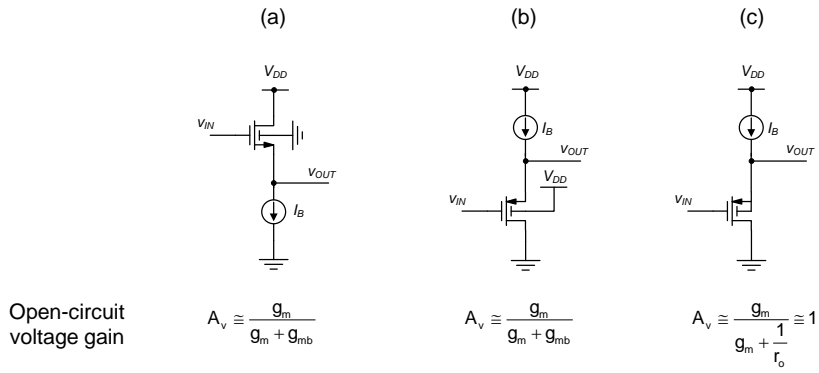


Figure Ex4-5

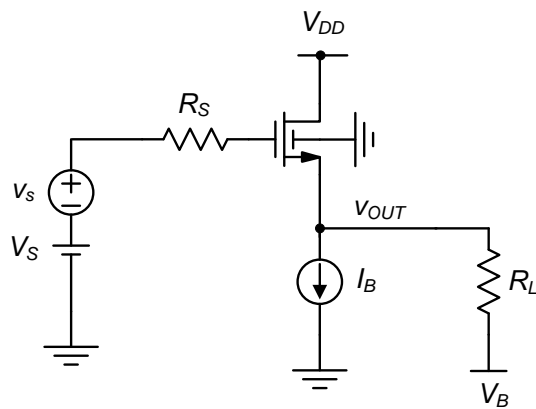


Figure 4-20

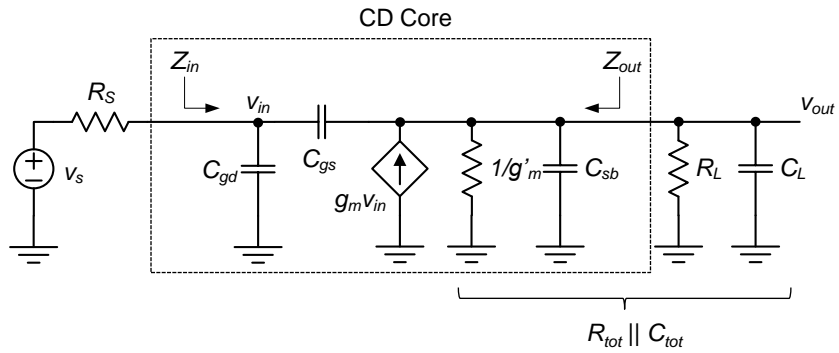


Figure 4-21

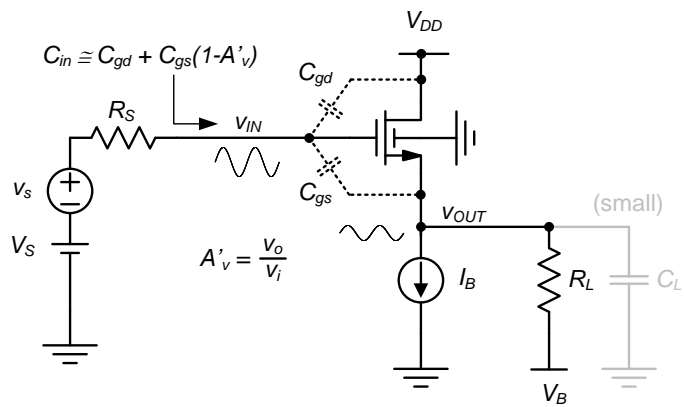


Figure 4-22

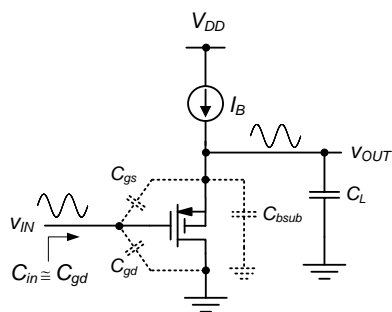


Figure 4-23

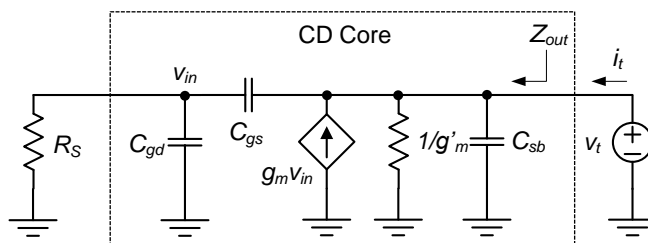


Figure 4-24

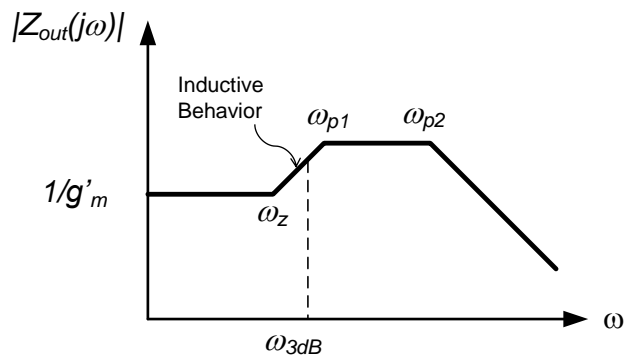


Figure 4-25

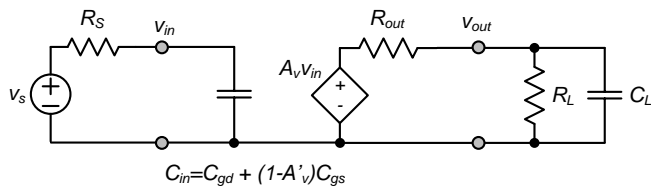


Figure 4-26

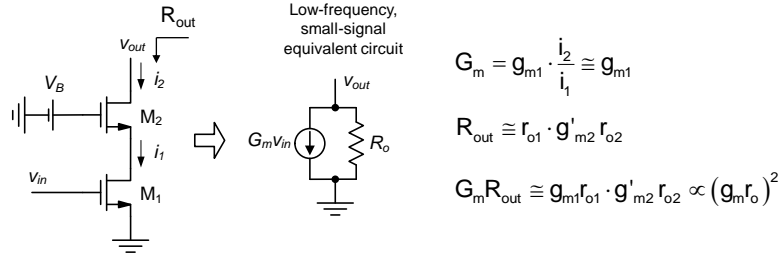


Figure 4-27

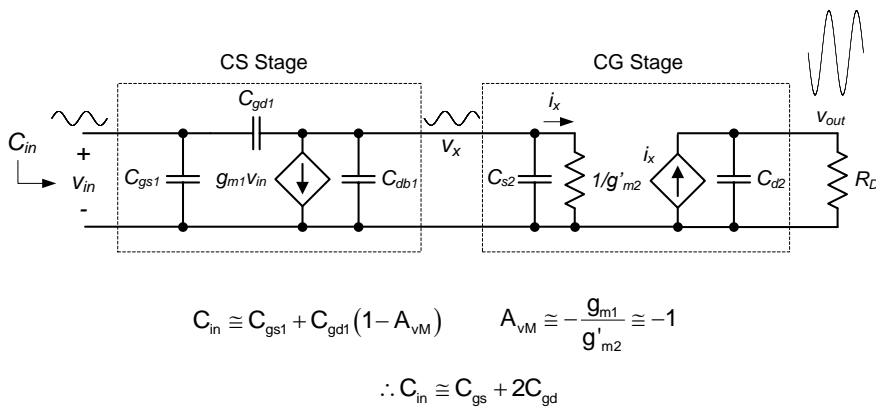


Figure 4-28

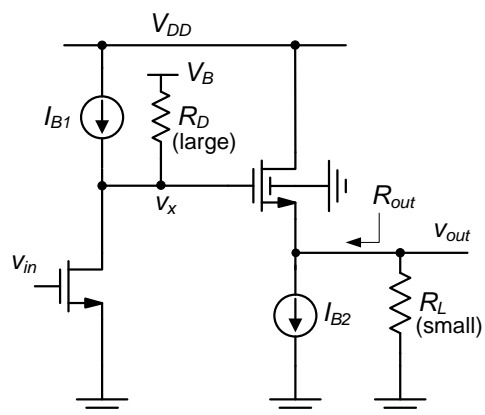


Figure 4-29

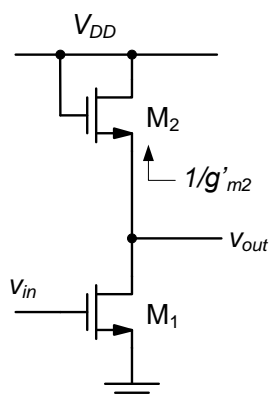


Figure 4-30

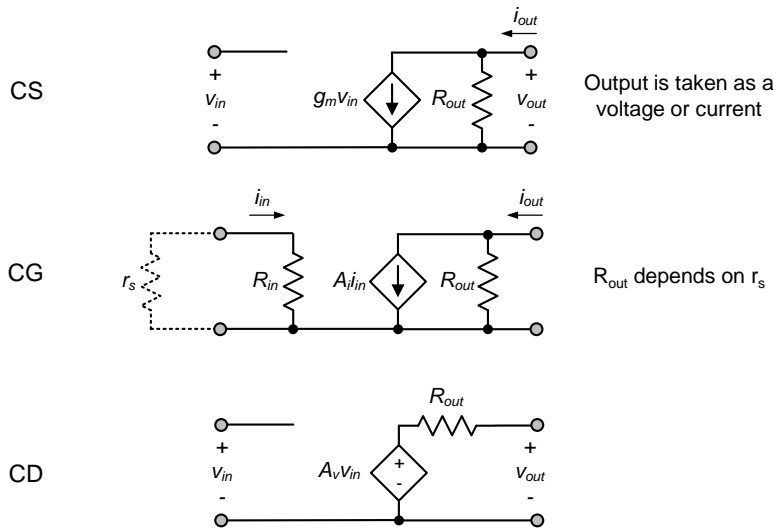


Figure P4.1

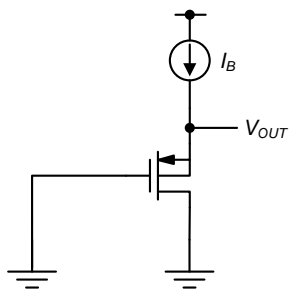


Figure P4.3

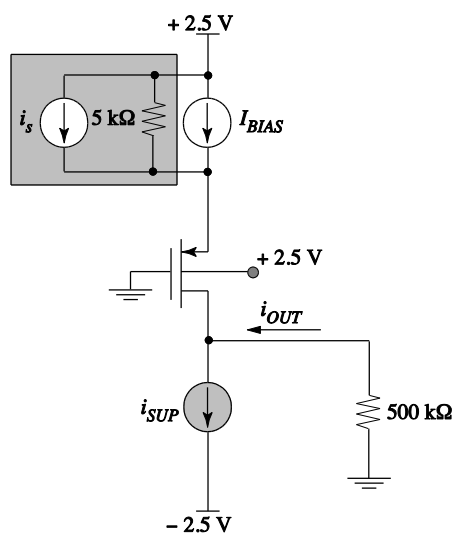


Figure P4.5

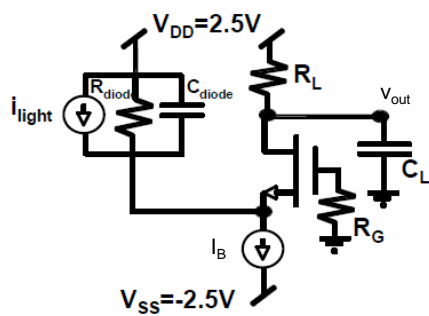


Figure P4.7

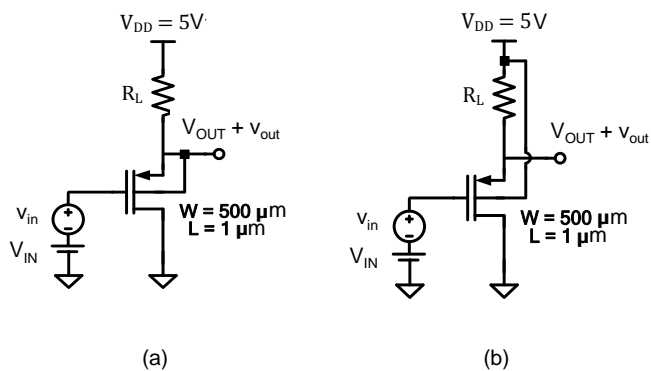


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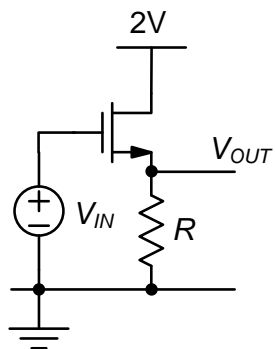


Figure P4.12

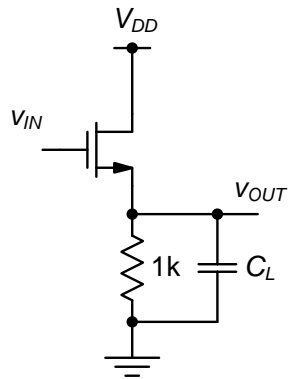


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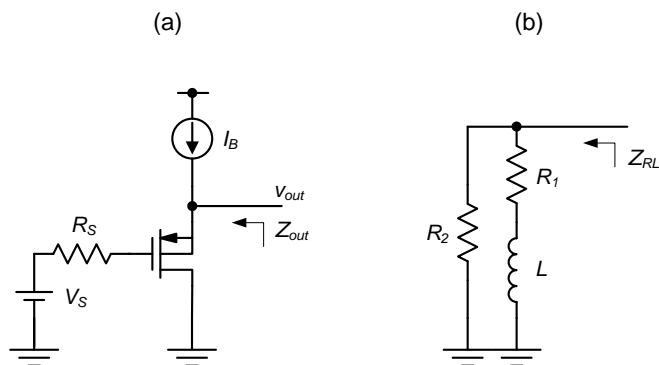


Figure 5-1

Process Variation and Device Mismatch
Section 5.2

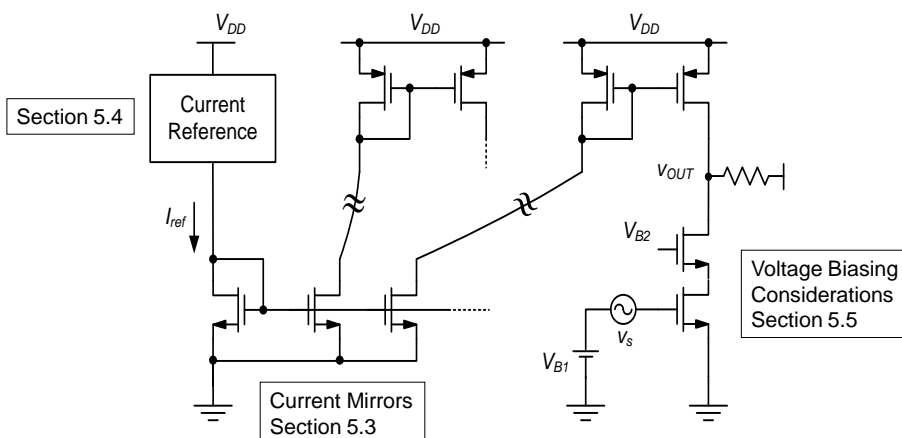


Figure Ex5-1

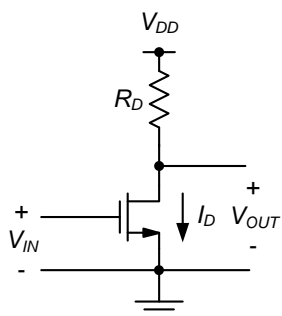


Figure 5-2

The diagram shows a current mirror circuit with two NMOS transistors, M_1 and M_2 , both with width/length ratio W/L . The gates of both transistors are connected to a common bias voltage V_{IN} . The drain of M_1 is connected to its gate and to an input current source I_{IN} . The drain of M_2 is connected to an output voltage V_{OUT} and an output current source I_{OUT} . The gates of both transistors are connected to a common bias voltage V_{IN} .

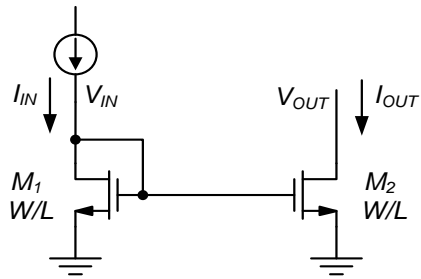


Figure 5-3

The circuit diagram shows a Wilson current mirror configuration. The top node is connected to V_{DD} . A current source I_s is connected between V_{DD} and the gate of a PMOS transistor. The PMOS transistor's source is connected to V_{DD} and its drain is connected to the output node. The output node is also connected to a load resistor and a load capacitor C_{out} . The output voltage is V_{OUT} , and the output current is I_{OUT} . The output node is also connected to the gate of a PMOS transistor M_2 . The source of M_2 is connected to ground. The drain of M_2 is connected to the gate of a PMOS transistor M_1 . The source of M_1 is connected to ground. The drain of M_1 is connected to the output node. The input current I_{IN} is injected into the output node. The output voltage is V_{OUT} , and the output current is I_{OUT} . The output node is also connected to a load resistor and a load capacitor C_{out} . The output voltage is V_{OUT} , and the output current is I_{OUT} . The output node is also connected to the gate of a PMOS transistor M_2 . The source of M_2 is connected to ground. The drain of M_2 is connected to the gate of a PMOS transistor M_1 . The source of M_1 is connected to ground. The drain of M_1 is connected to the output node. The input current I_{IN} is injected into the output node. The output voltage is V_{OUT} , and the output current is I_{OUT} . The output node is also connected to a load resistor and a load capacitor C_{out} . The output voltage is V_{OUT} , and the output current is I_{OUT} .

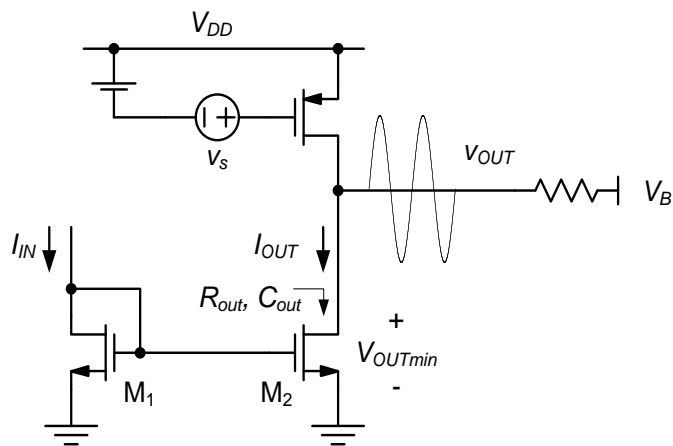


Figure 5-4

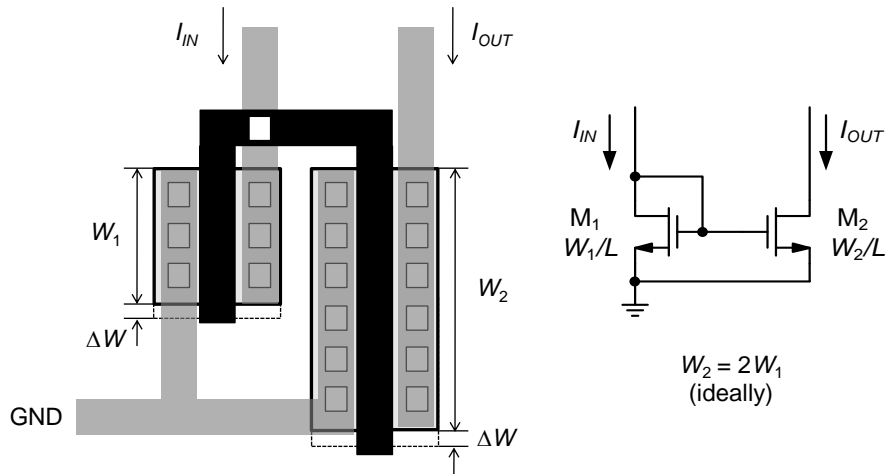


Figure 5-5

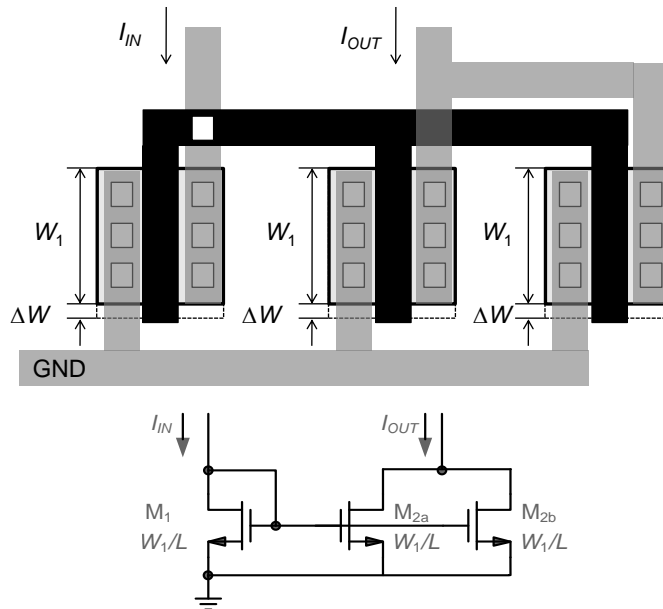


Figure 5-6

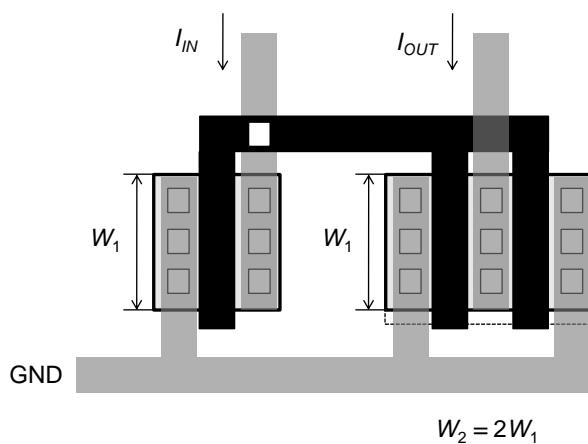


Figure 5-7

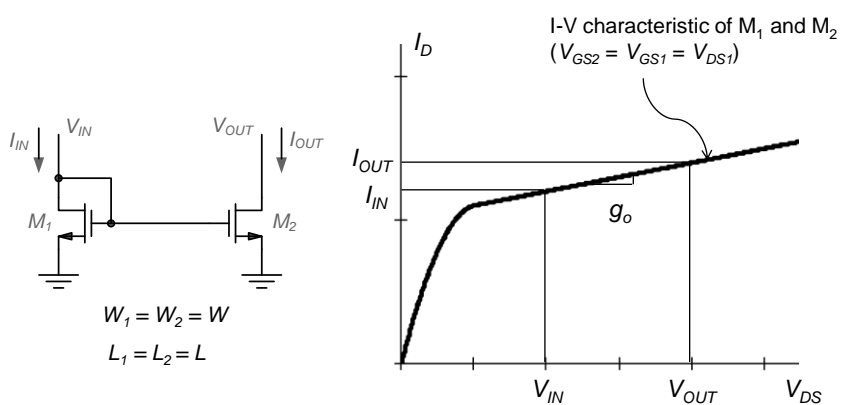


Figure 5-8

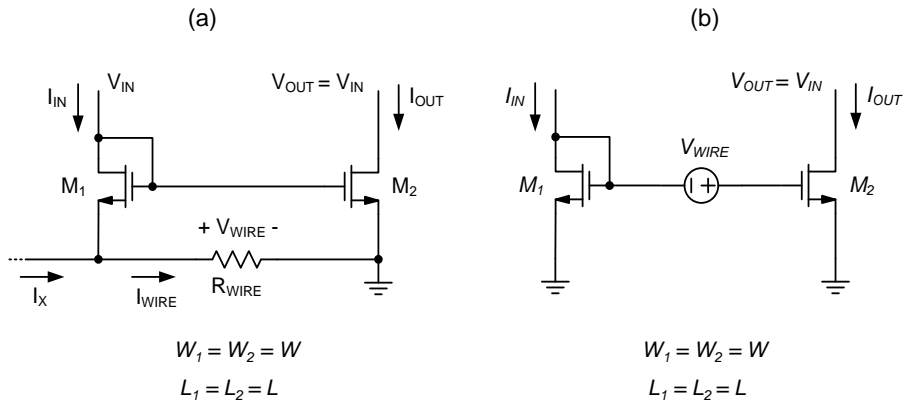
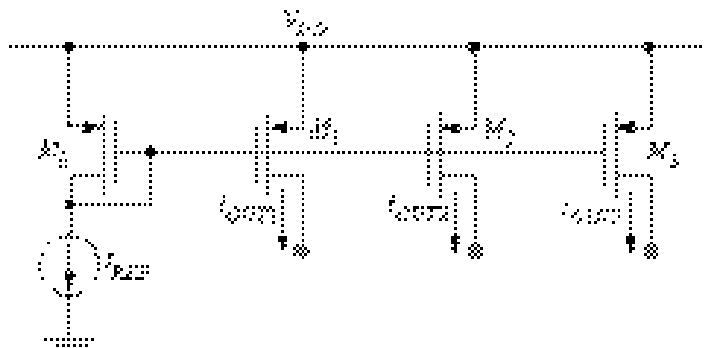
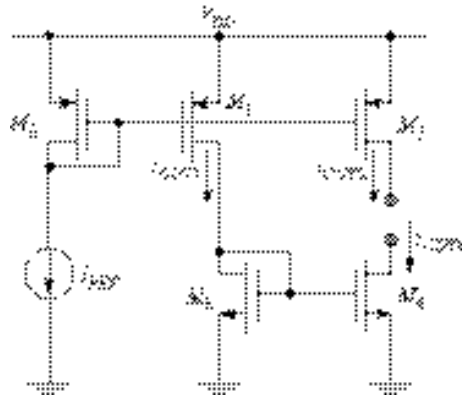


Figure 5-9



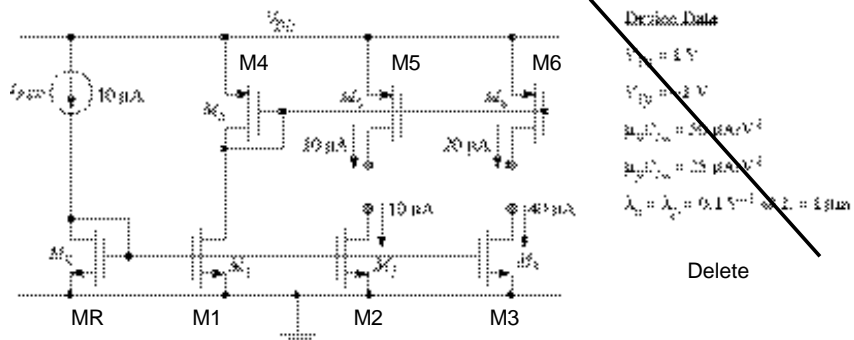
(Howe & Sodini, Figure 9-31)

Figure 5-10



(Howe & Sodini, Figure 9-32)

Figure Ex5-3



(Howe & Sodini, Figure Ex 9-8)

Figure 5-11

(a)

(b)

Figure 5-12

Figure 5-12 illustrates the small-signal model and the I-V characteristic of a common-source amplifier.

The left diagram shows the small-signal model. The input signal v_{d1} is applied to the gate of the NMOS transistor M_1 . The output signal v_{out} is taken from the drain of M_1 , which is connected to a load resistor r_{o2} . The transconductance of M_1 is denoted by g'_{m2} .

The right diagram shows the I-V characteristic of M_1 . The horizontal axis represents the drain-source voltage V_{DS} , and the vertical axis represents the drain current I_{OUT} . The curve shows the relationship between I_{OUT} and V_{DS} . The operating point is determined by the intersection of the load line (a straight line from the y-axis to the x-axis at V_{D1}) and the I-V characteristic curve. The small-signal output current i_{out} is shown as a small variation around the operating point. The transconductance g_{o1} is indicated as the slope of the I-V characteristic at the operating point. The voltage v_{d1} is shown as a small variation around the operating point, and the voltage divider between r_{o2} and g'_{m2} is indicated.

Figure 5-13

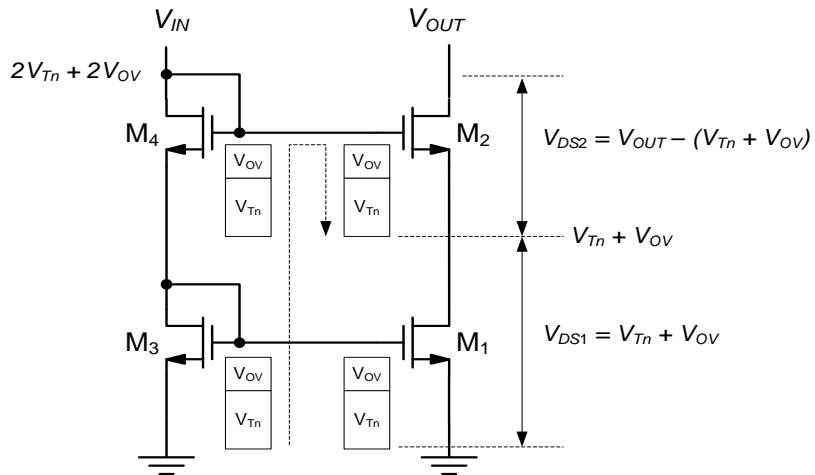


Figure 5-14

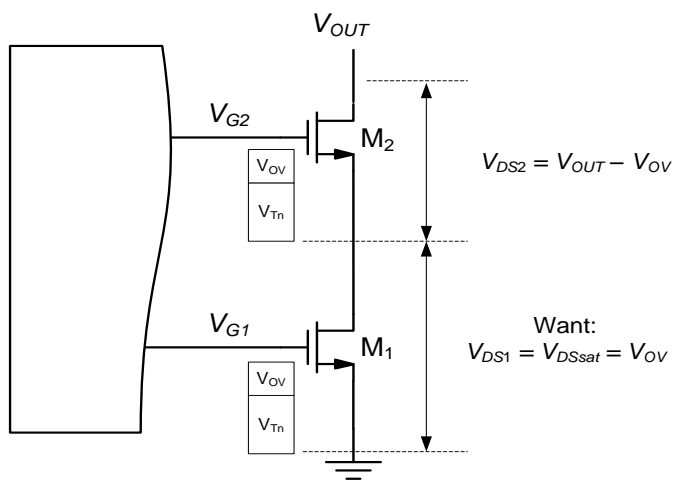


Figure 5-15

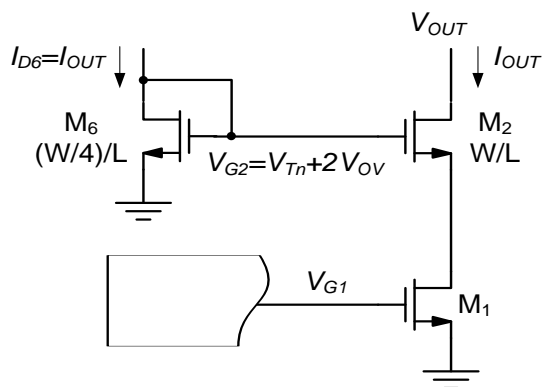


Figure 5-16

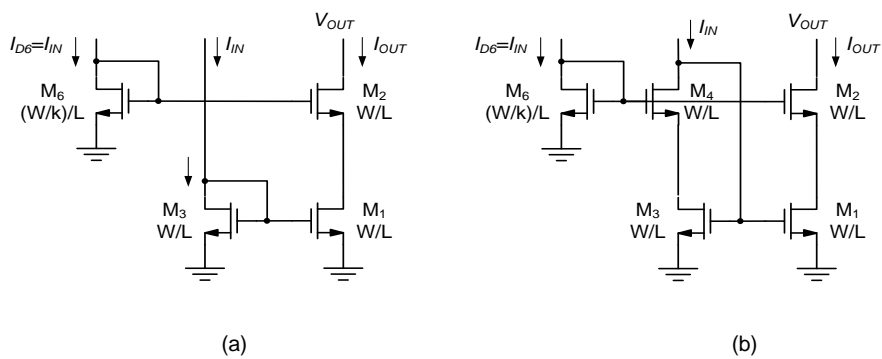


Figure 5-17

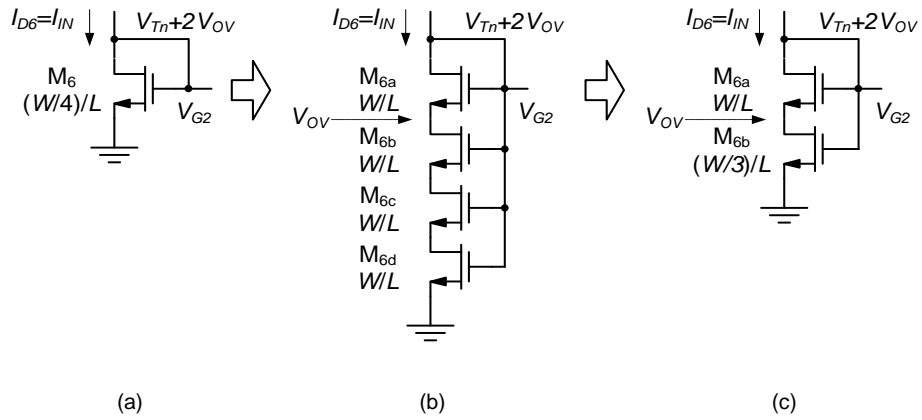
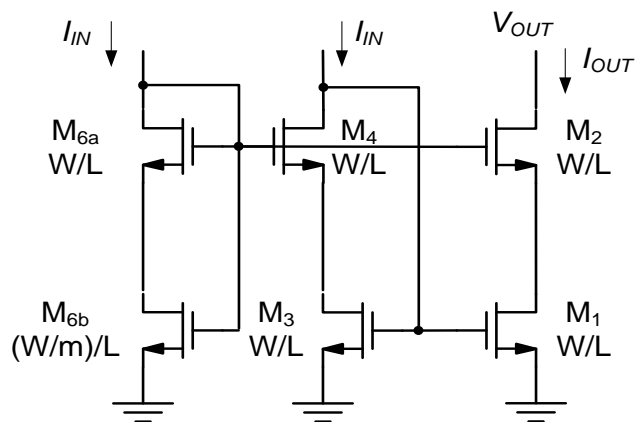


Figure 5-18



Solution to Ex 5-3

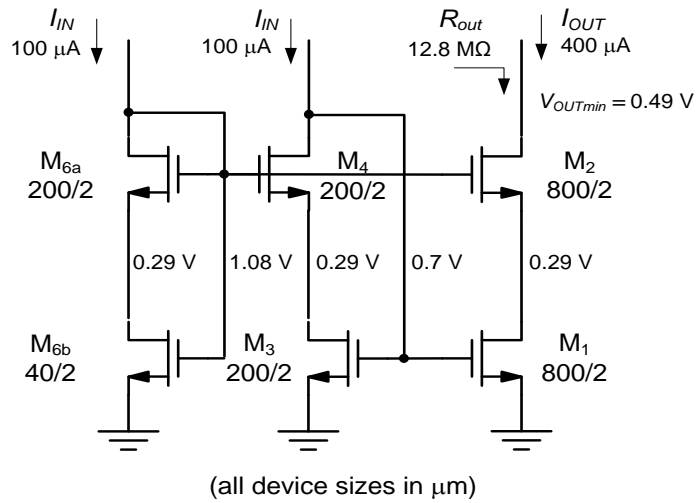


Figure 5-19

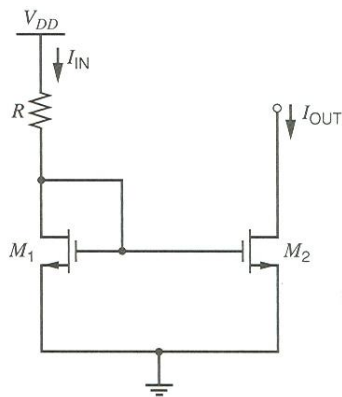


Figure 5-20

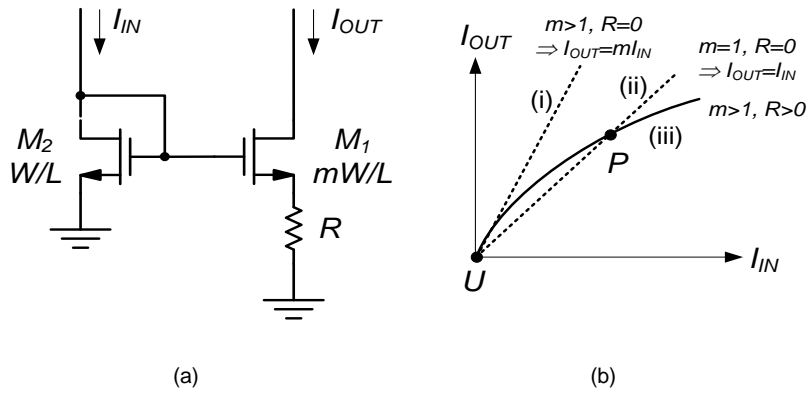


Figure 5-21

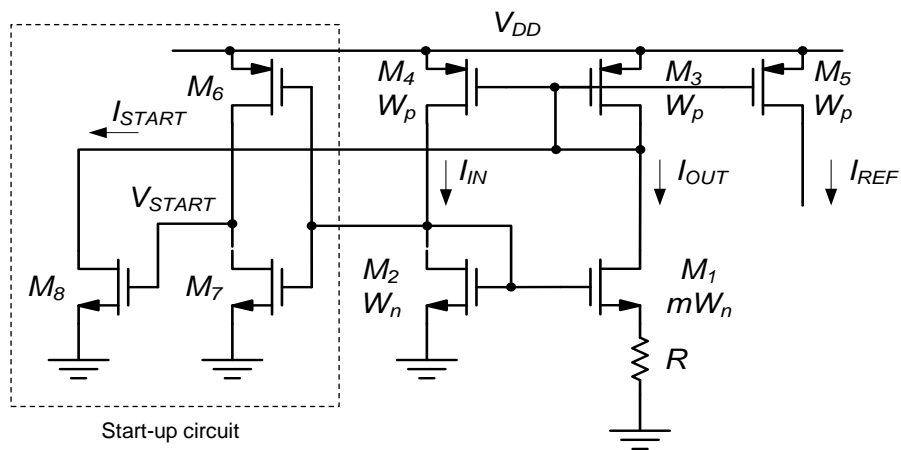


Figure 5-22

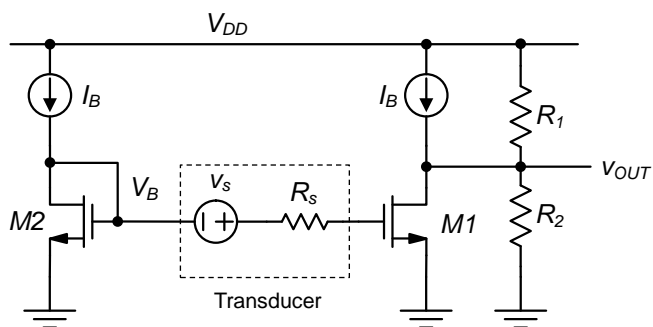


Figure 5-23

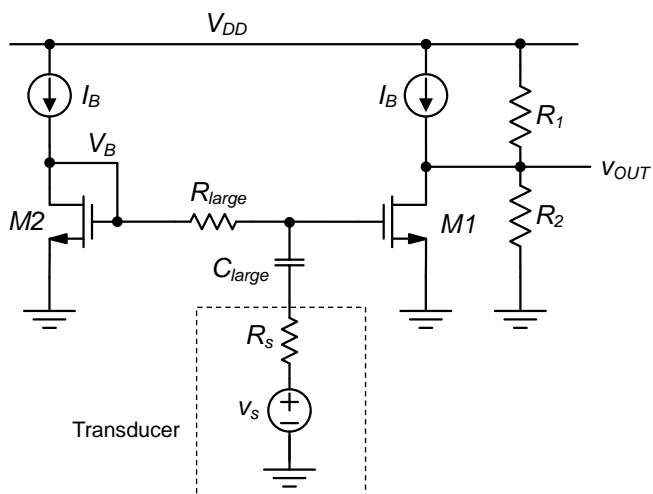


Figure 5-24

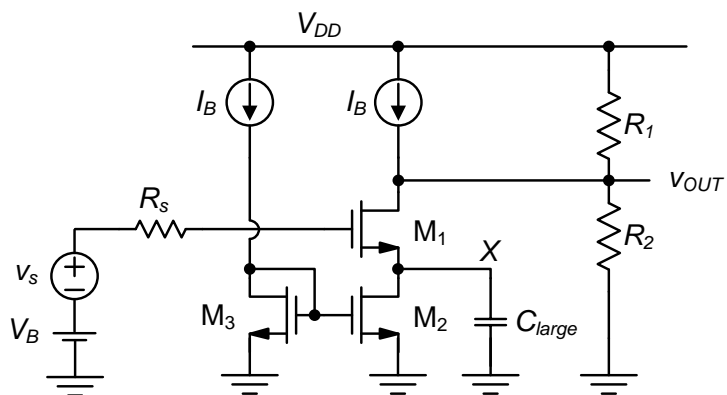


Figure 5-25

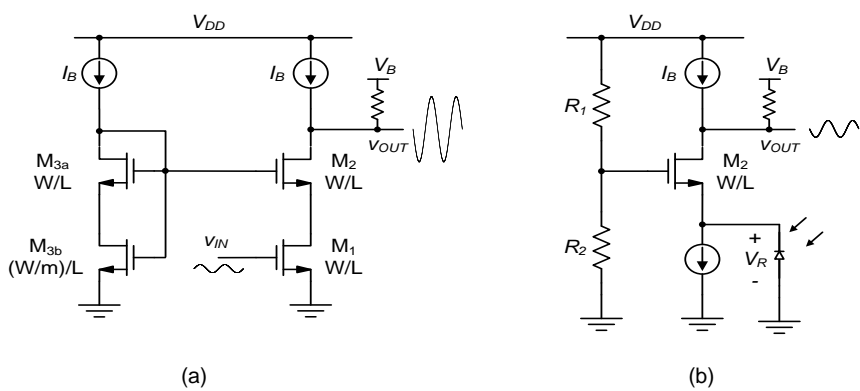


Figure 5-26

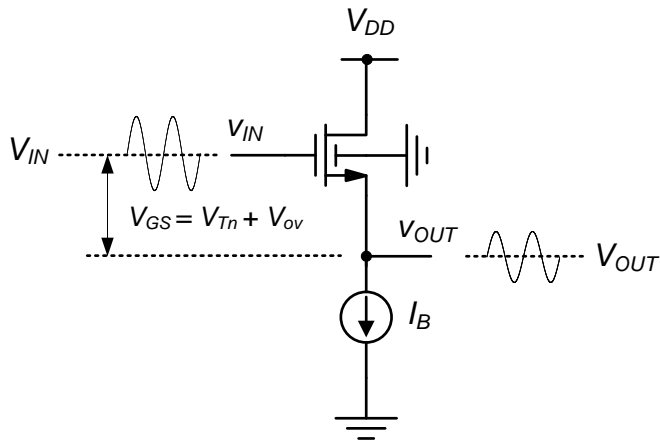
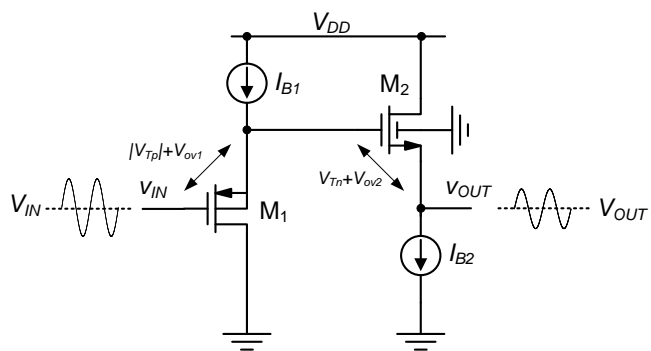
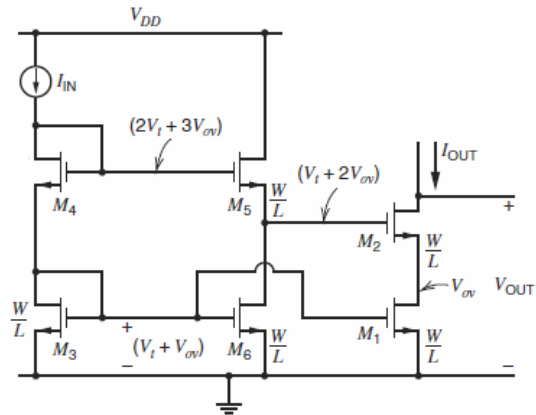


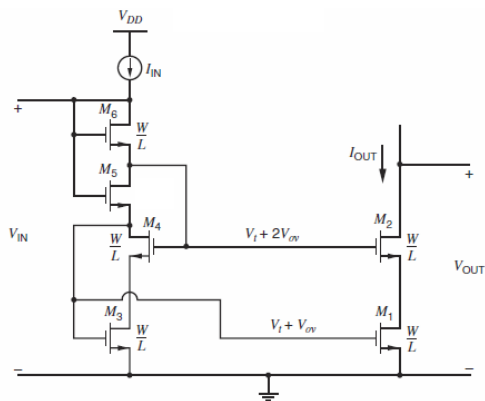
Figure 5-27



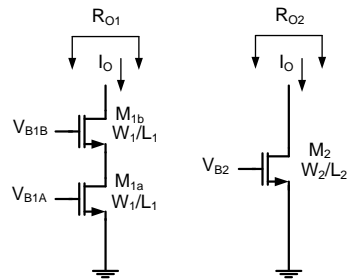
Problem P5.5



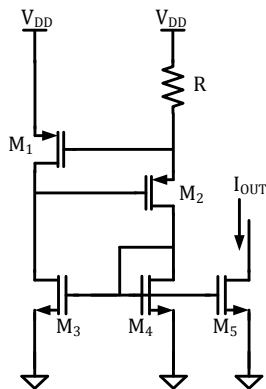
Problem P5.6



Problem P5.9

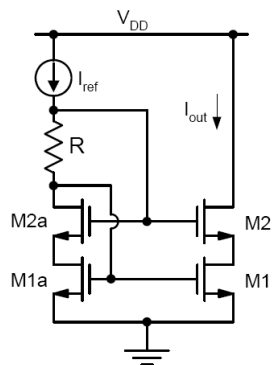


Problem P5.10



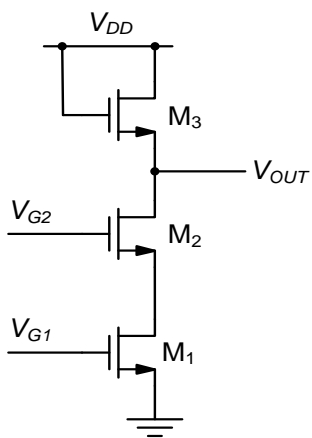
Problem P5.11

The circuit diagram shows a current mirror configuration. A reference current source I_{ref} is connected to the V_{DD} supply. The current I_{ref} flows through a resistor R and then through the gate of transistor $M2a$. The source of $M2a$ is connected to ground. The drain of $M2a$ is connected to the gates of both $M1$ and $M2$. The source of $M1$ is connected to ground. The source of $M2$ is connected to the output node, which is also connected to the V_{DD} supply. The output current I_{out} is the current flowing out of the output node. The gates of $M1$ and $M2$ are connected to the gates of $M2a$ and $M1a$, which are also connected to the gates of $M1$ and $M2$ respectively. The sources of $M1a$ and $M2a$ are connected to ground.



Problem P5.12

The diagram shows a vertical stack of three CMOS inverters. The top inverter, labeled M_3 , has its gate connected to V_{DD} and its drain connected to V_{DD} . Its source is connected to the output node V_{OUT} . The middle inverter, labeled M_2 , has its gate connected to V_{G2} and its drain connected to V_{OUT} . Its source is connected to the input of the bottom inverter. The bottom inverter, labeled M_1 , has its gate connected to V_{G1} and its drain connected to the input of the middle inverter. Its source is connected to ground. The gates of M_2 and M_1 are connected to V_{G2} and V_{G1} respectively, which are shown as input signals.



Problem P5.13

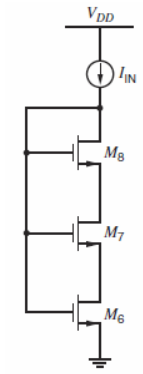


Figure 6-1

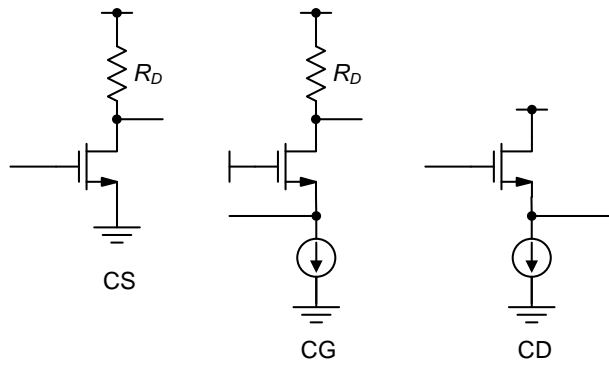


Figure 6-2

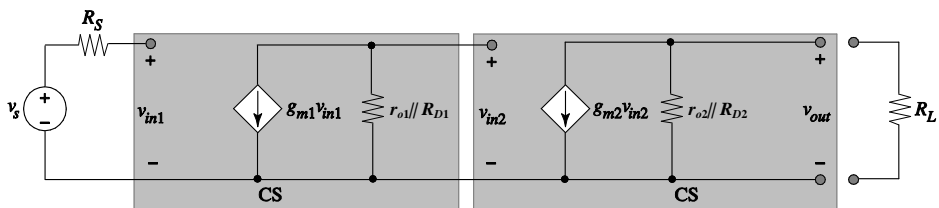


Figure 6-3

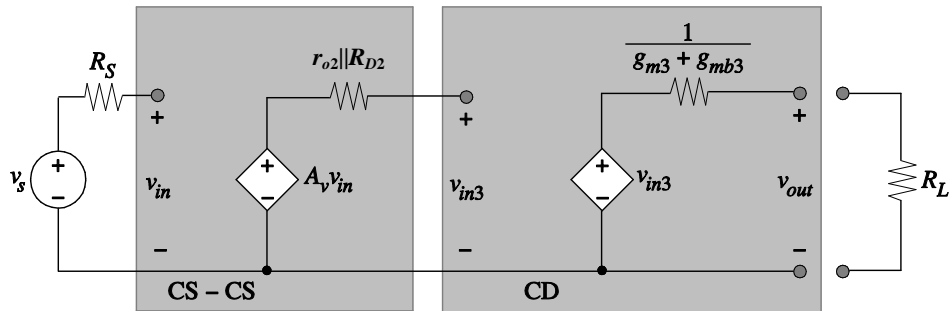


Figure 6-4

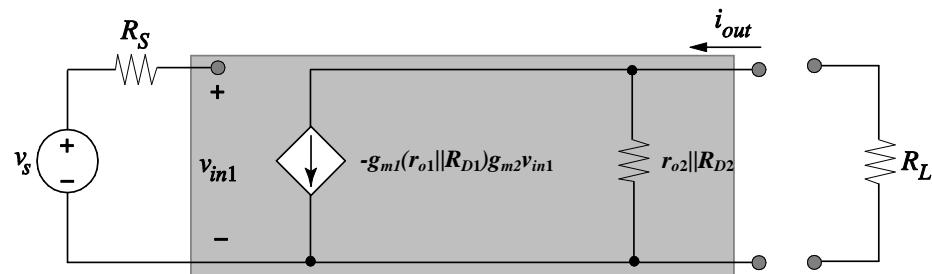


Figure 6-5

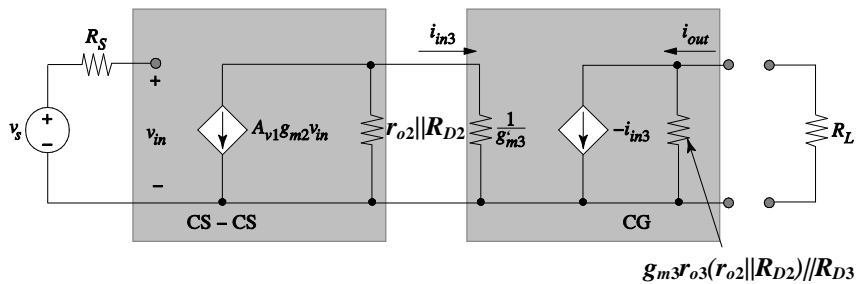


Figure Ex6-1A

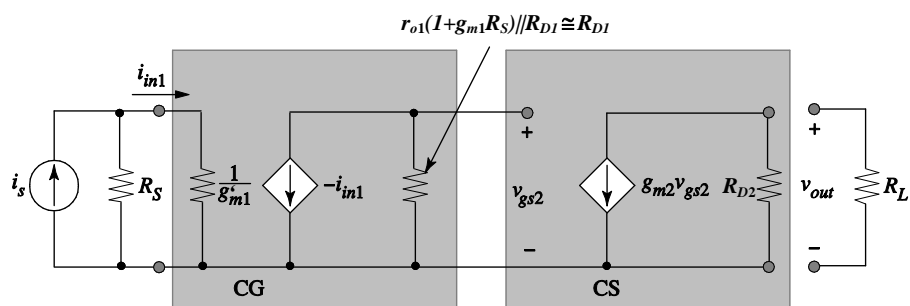


Figure Ex6-1B

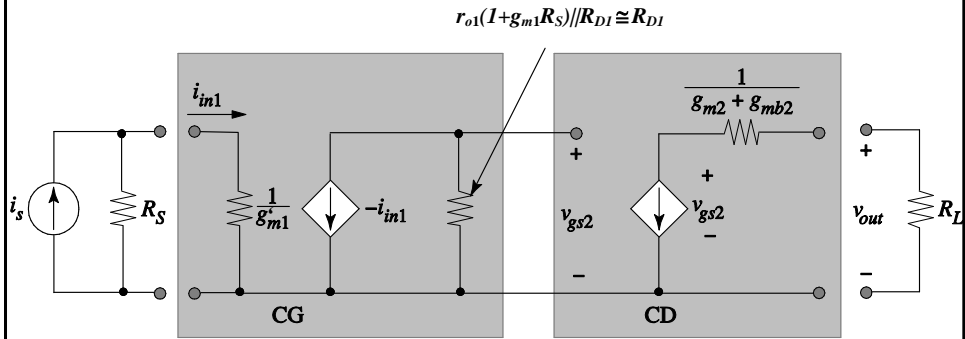


Figure 6-6

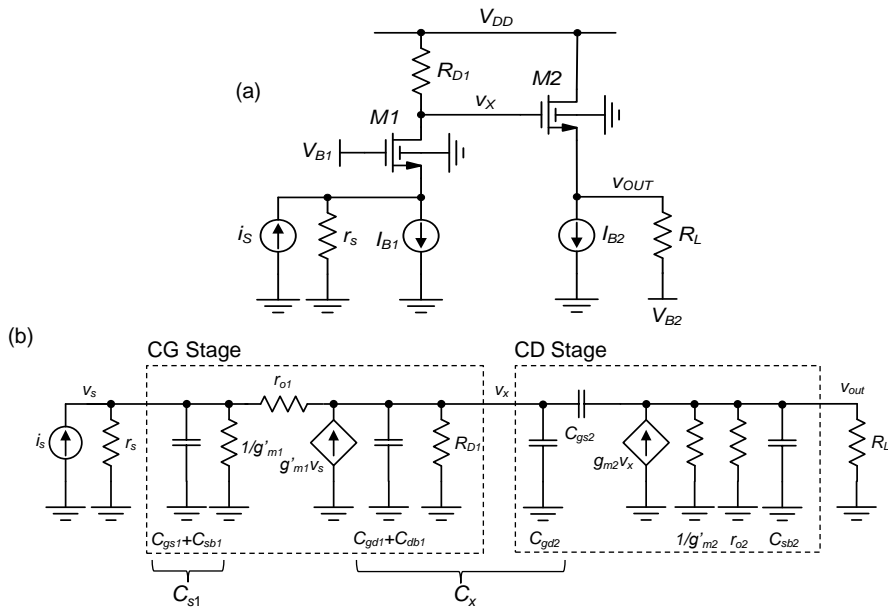
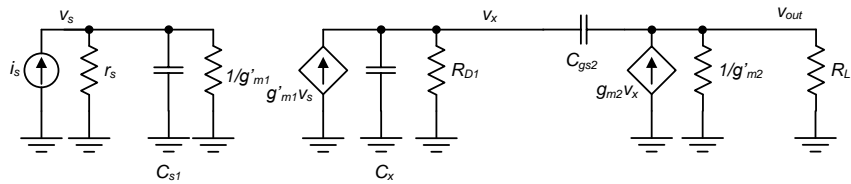
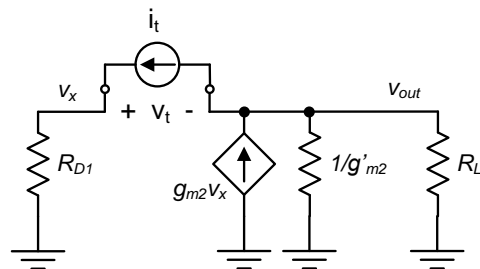


Figure 6-7



Example 6-2 Solution



Example 6-3 Solution

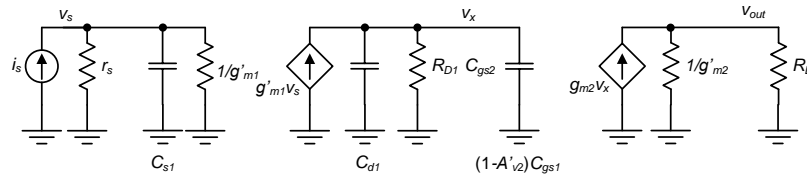


Figure 6-8

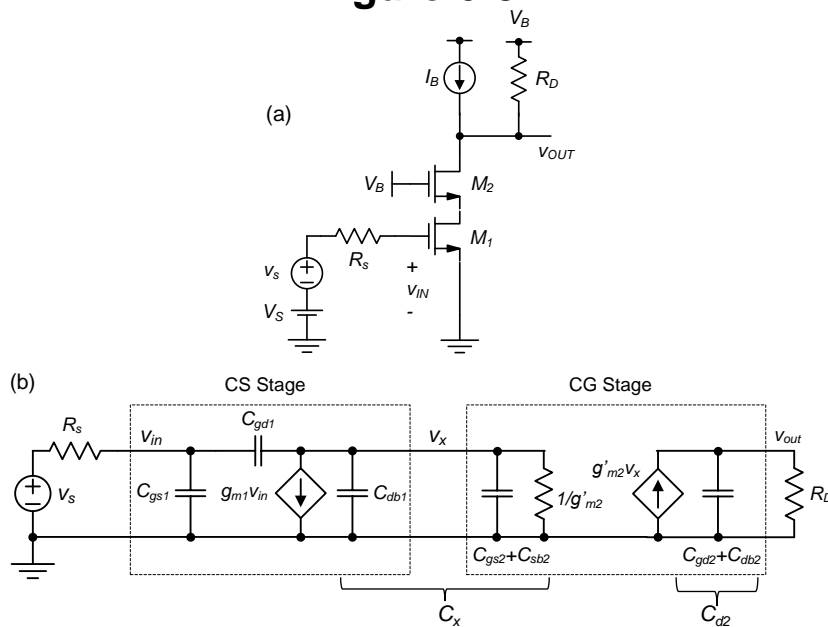


Figure Ex6-3

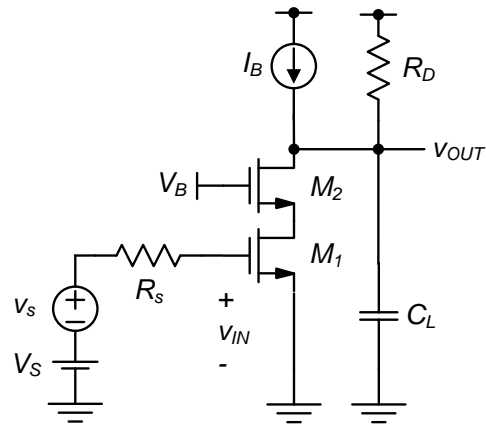


Figure 6-9

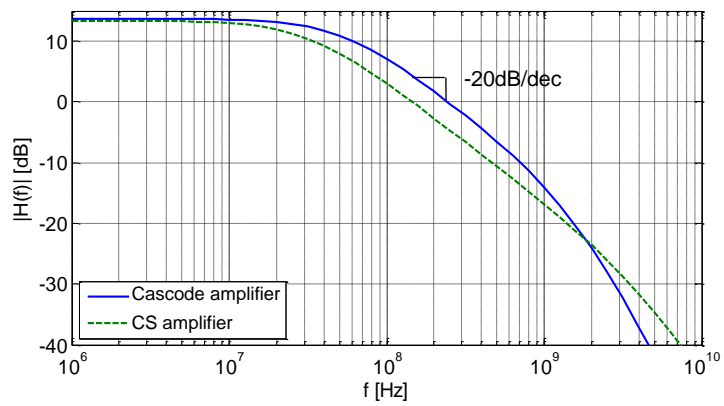


Figure 6-10

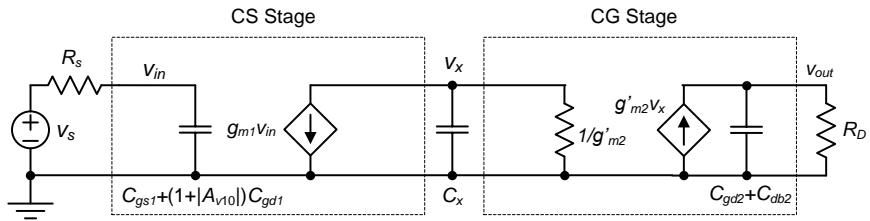


Figure 6-11

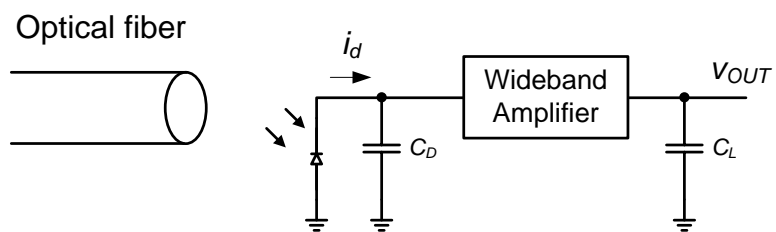


Figure 6-12

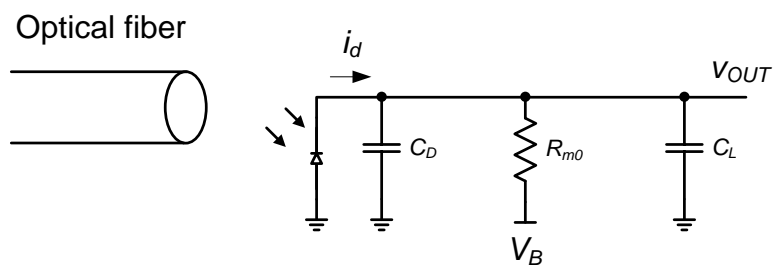


Figure 6-13

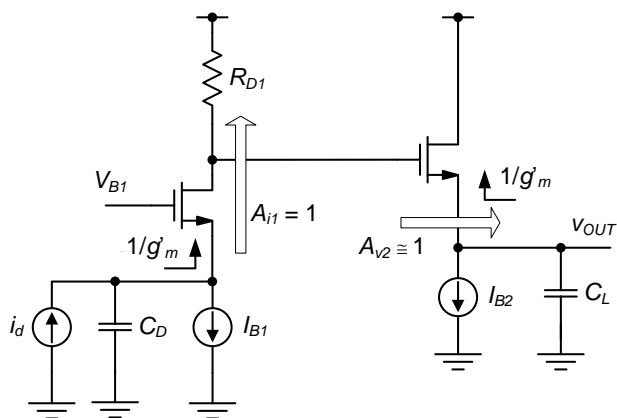


Figure 6-14

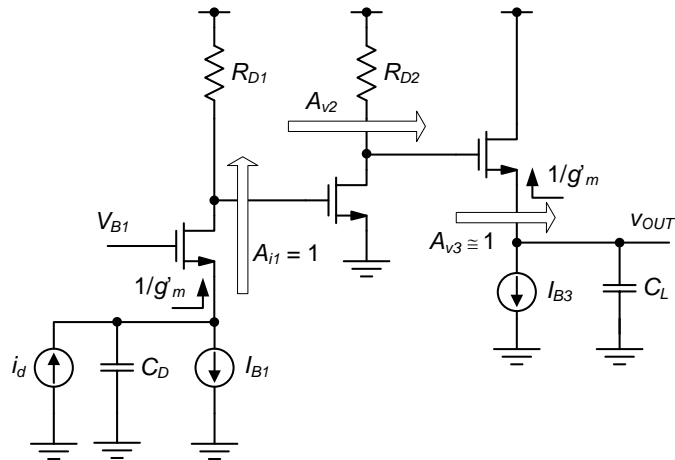


Figure 6-15

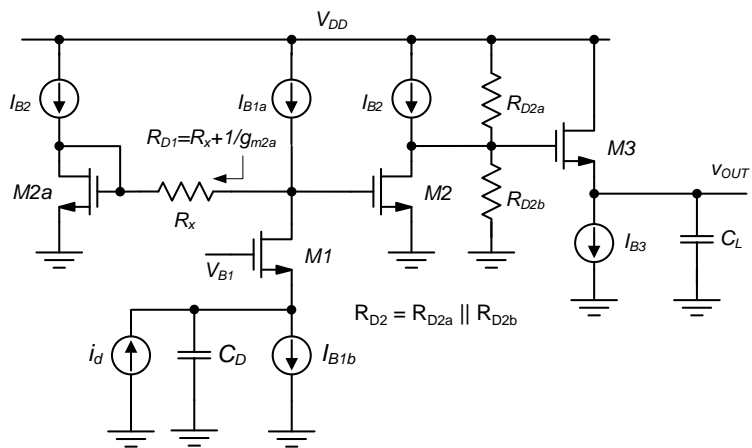


Figure 6-16

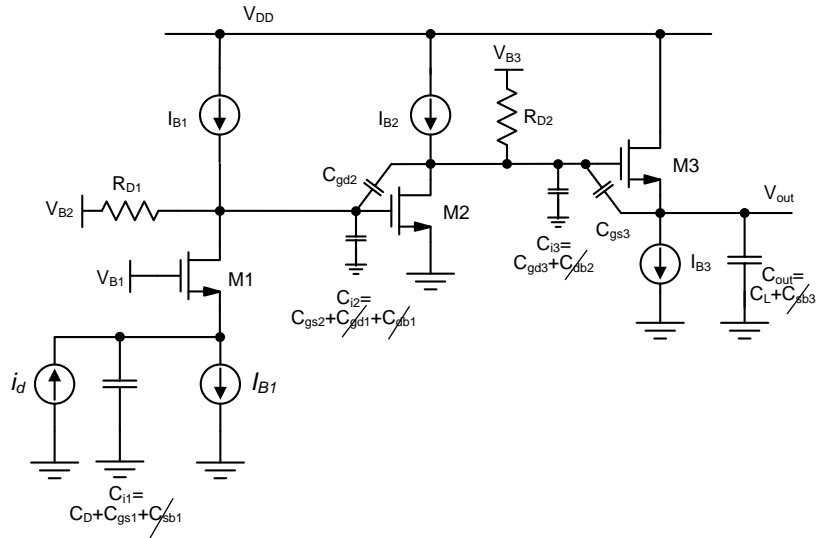


Figure 6-17

```
% Design script for three-stage transresistance amplifier

% Process technology parameters
kp_n = 50e-6;
Cox = 2.3e-3;
mu_n = kp_n/Cox;
Cov = 0.5e-9;
gmb_gm = 0.2;

% Design specifications
Rm = 2e3;
CD = 5e-12;
CL = 10e-12;
IDtot = 3e-3;

% Design choices
VOV1 = 0.3;
VOV2 = 0.3;
VOV3 = 0.3;
L1 = 1e-6;
L2 = 1e-6;
L3 = 1e-6;

% optimization parameters
ID1_IDtot = 0.25;
ID3_IDtot = 0.25;
Av20 = 10;

% Compute drain currents
ID1 = IDtot*ID1_IDtot;
ID3 = IDtot*ID3_IDtot;
ID2 = IDtot - ID1 - ID3;

% Calculations for M1
gm1 = 2*ID1/VOV1;
W1 = 2*ID1/(kp_n/L1*VOV1^2);
Cgs1 = 2/3*W1*L1*Cox + W1*Cov;
tau_in = (Cgs1+CD)/(gm1*(1+gmb_gm));

% Calculations for M3
gm3 = 2*ID3/VOV3;
W3 = 2*ID3/(kp_n/L3*VOV3^2);
Cgs3 = 2/3*W3*L3*Cox + W3*Cov;
Cgd3 = W3*Cov;
Av30 = 1-gmb_gm;
tau_out = (CL+Cgs3)/(gm3*(1+gmb_gm));

% Calculations for M2
gm2 = 2*ID2/VOV2;
W2 = 2*ID2/(kp_n/L2*VOV2^2);
Cgs2 = 2/3*W2*L2*Cox + W2*Cov;
Cgd2 = W2*Cov;
RD1 = Rm/Av20/Av30;
RD2 = Av20/gm2;
tau_core = RD1*(Cgs2 + (1+Av20)*Cgd2) + RD2*(Cgd3+(1-Av30)*Cgs3);

% Total time constant and bandwidth estimate
tau_tot = tau_in + tau_core + tau_out;
f3dB = 1/(2*pi*tau_tot);
```

Figure 6-18

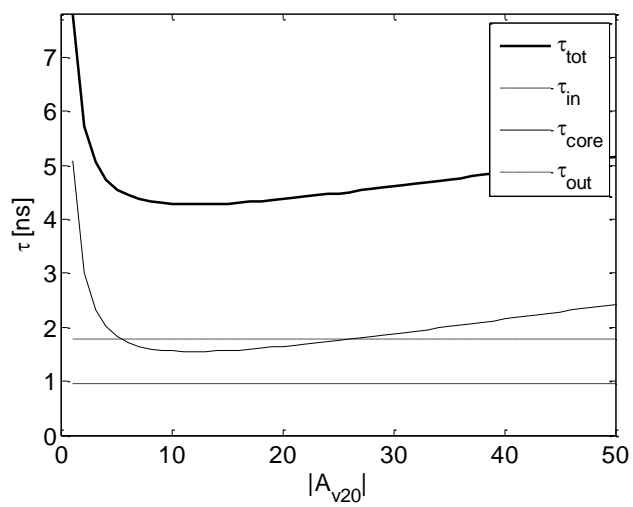


Figure P6-3

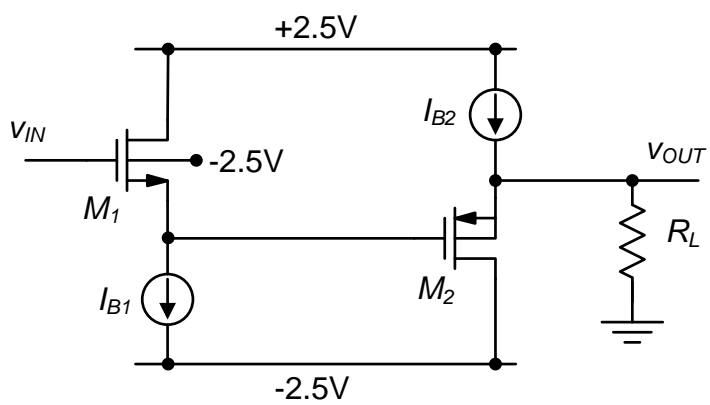


Figure P6-7

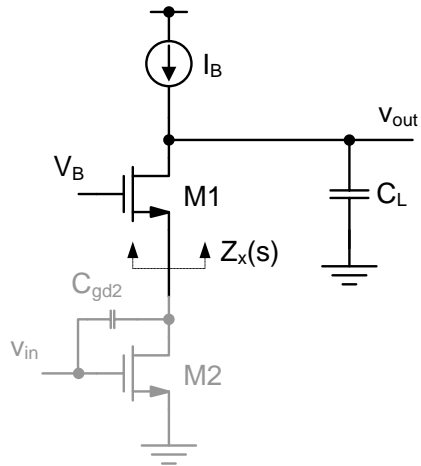


Figure P6-8

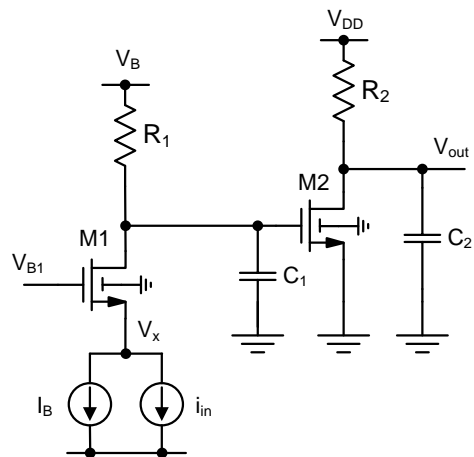


Figure P6-9

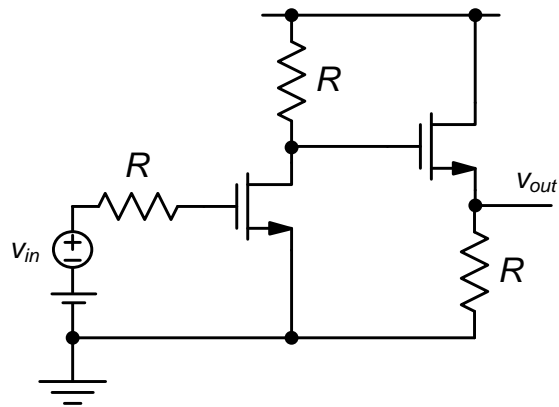


Figure P6-12

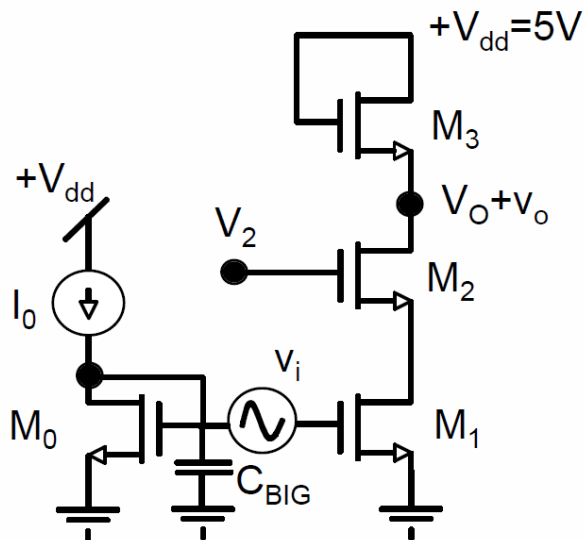


Figure P6-13

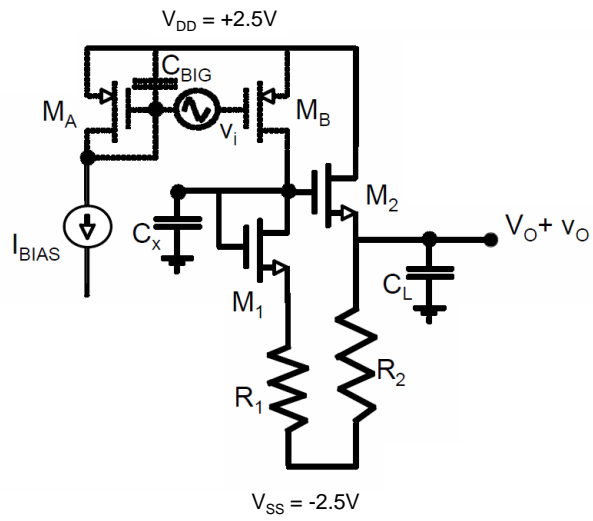


Figure P6-14

