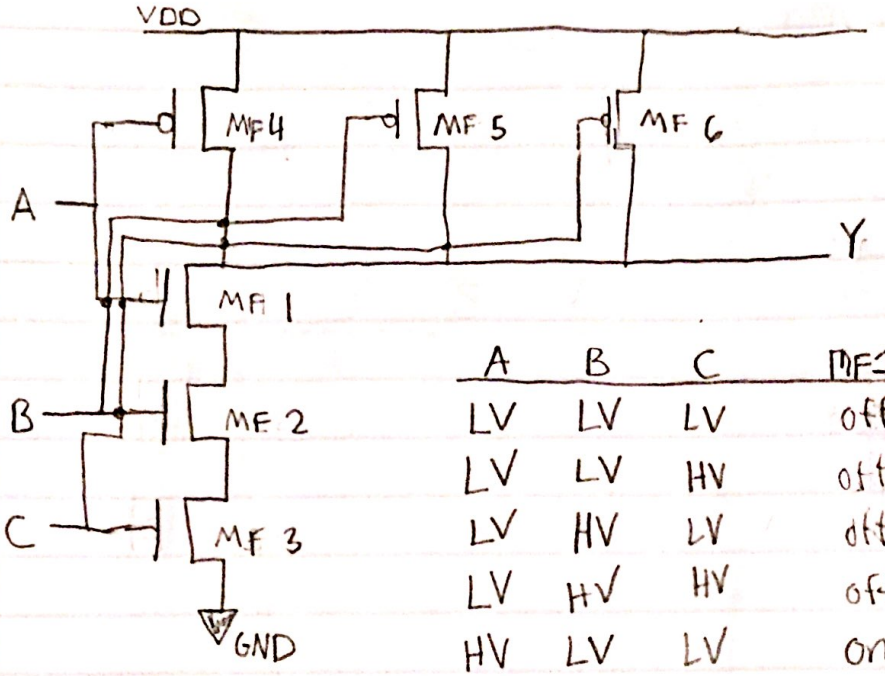
Brandon Wynne
Bmwynne
9/17/2015
B441

1.1: CMOS 3-Input NAND circuit



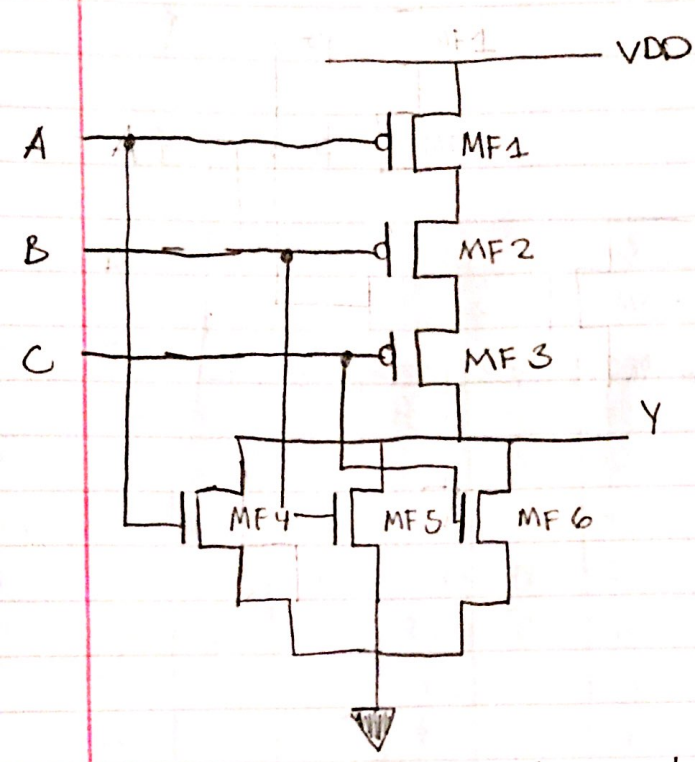

| A | B | C | MF1 | MF2 | MF3 | MF4 | MF5 | MF6 | I | Y |
|---|---|---|---|---|---|---|---|---|---|---|
| LV | LV | LV | off | off | off | on | on | on | 0 | H |
| LV | LV | HV | off | off | on | on | on | off | 0 | H |
| LV | HV | LV | off | on | off | on | off | on | 0 | H |
| LV | HV | HV | off | on | on | on | off | off | 0 | H |
| HV | LV | LV | on | off | off | off | on | on | 0 | H |
| HV | LV | HV | on | off | on | off | on | off | 0 | H |
| HV | HV | LV | on | on | off | off | off | on | 0 | H |
| HV | HV | HV | on | on | on | off | off | off | 0 | L |

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

The current is zero amps because the connection to VDD is blocked through the n/p-channel transistors at any time.

Brnlwynne

## 1.2: CMOS 3-INPUT NOR CIRCUIT



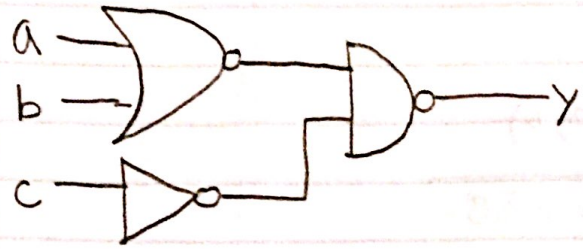

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

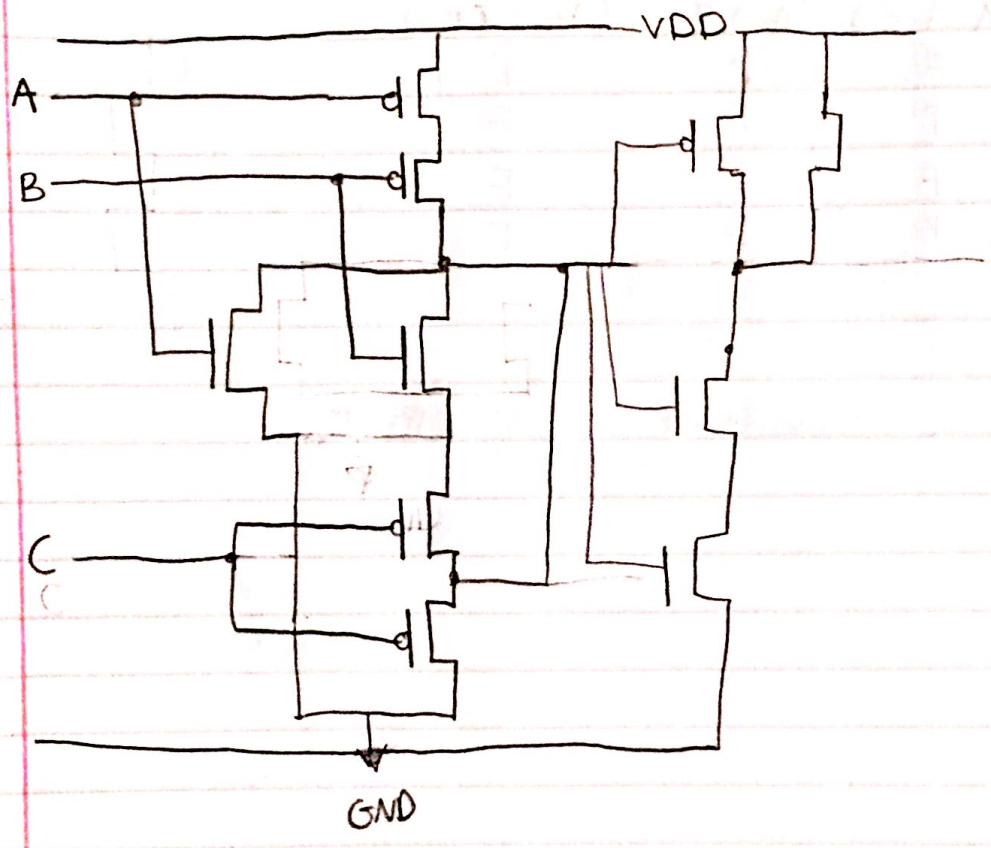
| A | B | C | MF1 | MF2 | MF3 | MF4 | MF5 | MF6 | I | Y |
|---|---|---|---|---|---|---|---|---|---|---|
| LV | LV | LV | ON | ON | ON | OFF | OFF | OFF | 0 | 1 |
| LV | LV | HV | ON | ON | OFF | OFF | OFF | ON | 0 | 0 |
| LV | HV | LV | ON | OFF | ON | OFF | ON | OFF | 0 | 0 |
| LV | HV | HV | ON | OFF | OFF | OFF | ON | ON | 0 | 0 |
| HV | LV | LV | OFF | ON | ON | ON | OFF | OFF | 0 | 0 |
| HV | LV | HV | OFF | ON | OFF | ON | OFF | ON | 0 | 0 |
| HV | HV | LV | OFF | OFF | ON | ON | ON | OFF | 0 | 0 |
| HV | HV | HV | OFF | OF | OFF | ON | ON | ON | 0 | 0 |

The current is zero amps for the same reason as the NAND circuit.

Bmwynnc

Part 1.3 : CMOS Logic circuit

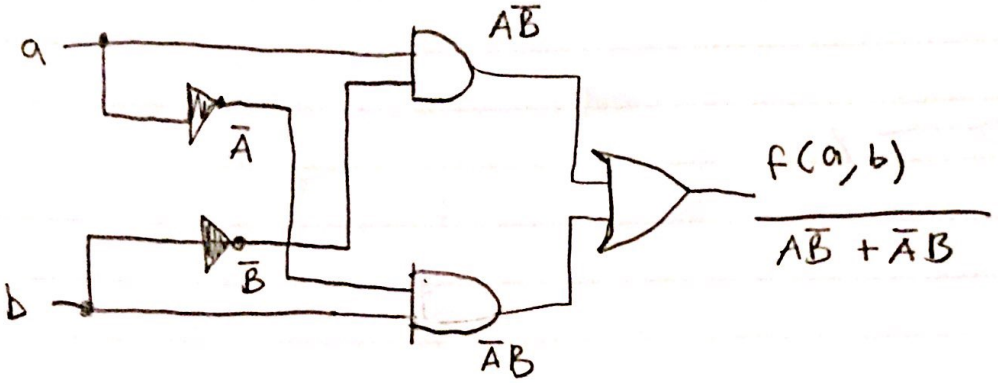



Pretty sure I'm doing this way wrong

Brwyne

Part 2.1 : Analysis of a Combinational Logic Circuit




| A | B | $\bar{A}$ | $\bar{B}$ | $(A \wedge \bar{B})$ | $(\bar{A} \wedge B)$ | $\overline{(A\bar{B} + \bar{A}B)}$ |
|---|---|---|---|---|---|---|
| T | T | F | F | F | F | T |
| T | F | F | T | T | F | F |
| F | T | T | F | F | T | F |
| F | F | T | T | F | F | T |

Part 2.2 : Analysis of a combinational logic circuit