Brandon Wynne
bmwynne
October 23, 2015

Homework 08

Part 1:

Serial Peripheral Interface, commonly referred to as SPI, is a synchronous communication interface in embedded systems. The SPI protocol is a full-duplex serial bus, developed by Motorola, and operates with the master-slave design concept. The master-slave paradigm is a parallel programming concept which breaks up the hosts computations into subroutines which are then sent to the slave for computation. In embedded systems this is often executed through the processor and a peripheral device. The two communicate in full-duplex, which allows them to send data back independently and simultaneously.

There are four logic signals that compose a SPI interface: Serial Clock (SCLK), Master Output (MOSI), Master Input (MISO), and Slave Select (SS). Serial Clock is generated through the host and is used to synchronize communication with the peripheral. In order to instantiate communicate the two devices must share the same baud rate-- or clock rate. The clock rate is the frequency as to which the processor is computing. The MOSI and MISO are data lines and the direction as to which data flows is hinted through their names. Data can be sent in either full or half duplex – however bytes must be sent even if they are to be ignored (If I remember correctly from 442 – elsewise the queue will be full). SS is used as a chip select and the signal for a corresponding peripheral is drawn low when chosen for communication (see figure 1 for diagram of all signals)

Part 2:

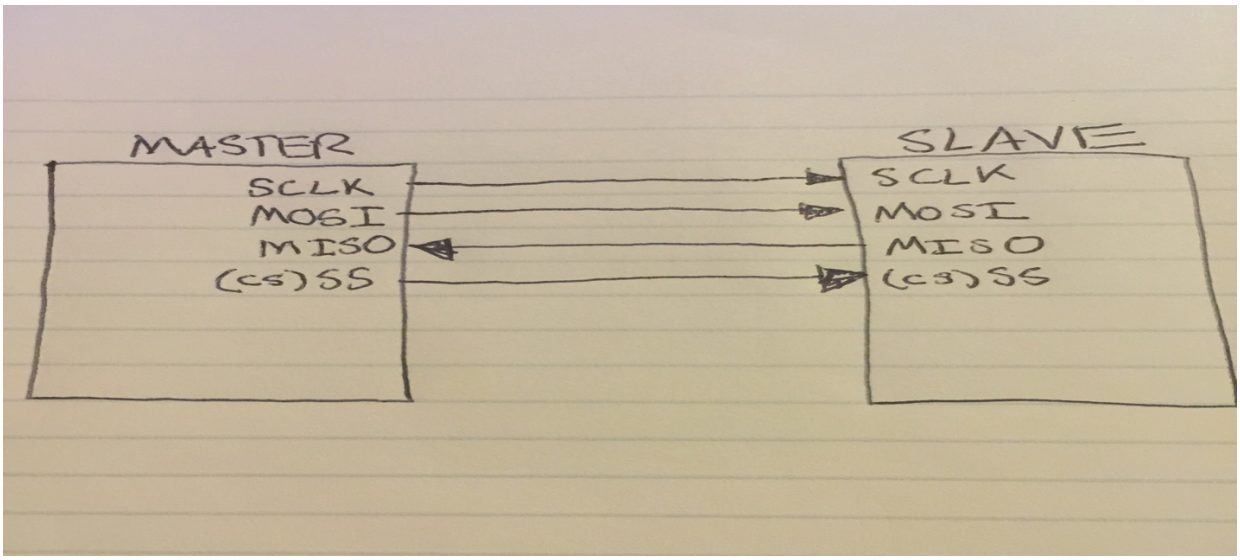

Figure 1

Part 3:

The timing in the frame of data is determined by the polarity of the signal – which can either be high or low. Communication is instantiated by the master by configuring the SCLK. In figure 2, the master drives the signal and when it selects the peripheral it drops the chip select, or SS, to low. The two devices now are synchronous and share the same baud rate. The master sends data to the slave and the slave sends data to the master.

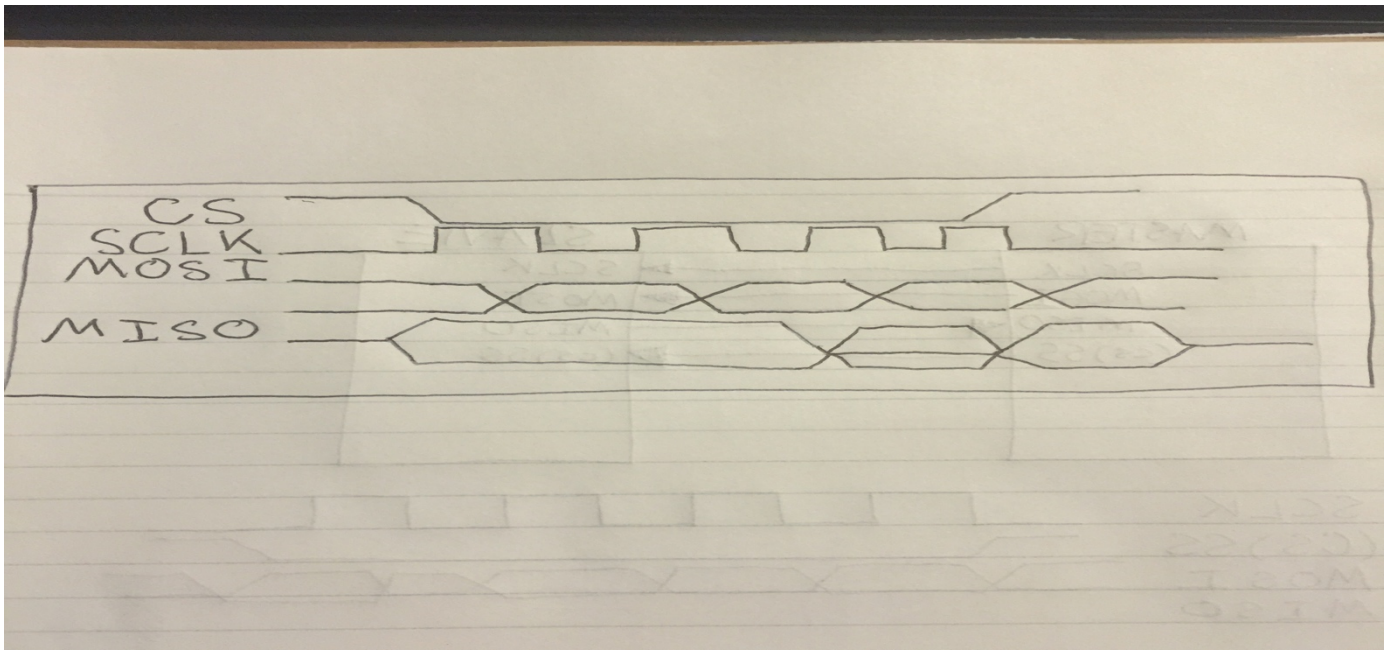

Figure 2