Mask Set Errata for Mask 1N97F

Introduction

This report applies to mask 1N97F for these products:

- KINETIS_L

Errata ID	Errata Title
3863	ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage
5746	PIT: When using the PIT to trigger DMA transfers using cycle steal mode, two data transfers per request are generated
5667	PMC: When used as an input to ADC or CMP modules, the PMC bandgap 1-V voltage reference is not available in VLPx, LLS, or VLLSx modes
5472	SMC: Mode transition VLPR->VLLS0(POR disabled)->RUN, will cause POR & LVD.
5745	SPI1: Back to back DMA data transfers are not possible if the core:bus frequency ratio is greater than 4:1
5490	SPI1: DMA data transfers at the maximum baud rate can result in corrupted data
5515	TSI: The end of scan flag is not automatically cleared when continuously scanning
5744	UART0: Receiver wakeup control bit cannot be set immediately after a wakeup event
5563	UART0: When the Receiver Wake Up control bit is set, an IDLE condition is not detected correctly
5753	UART1 / UART2: When the Receiver Wake Up control bit is set, an IDLE condition is not detected correctly

e3863: ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage

Errata type: Errata

Description: In 16-bit differential mode, the ADC may result in a conversion error when the input voltage on the plus-side of the differential pair (DPx) exceeds approximately (VREFH*31/32). Other modes are unaffected.

Workaround: To avoid a conversion error near positive full-scale in this mode, do not allow the input voltage on the plus-side of the differential pair (DPx) to exceed (VREFH*31/32).

e5746: PIT: When using the PIT to trigger DMA transfers using cycle steal mode, two data transfers per request are generated

Errata type: Errata

Description: If the PIT is used to trigger DMA transfers using cycle steal mode, DMA_DCRn[CS] = 1, each transfer request will cause the source data to be written twice. The data will be written first to the desired destination address and then a second time to the destination address + 1. The destination address pointer increments by 2 for each transfer request.

Workaround: It is recommended that the PIT not be used for triggering DMA transfers and the low power timer (LPTMR) be used instead.

If it is required to use the PIT to trigger DMA transfers, the destination address must be in RAM and the buffer size must be twice the amount of data being transferred. Software must then skip every second entry in the destination buffer.

e5667: PMC: When used as an input to ADC or CMP modules, the PMC bandgap 1-V voltage reference is not available in VLPx, LLS, or VLLSx modes

Errata type: Errata

Description: The Power Management Controller (PMC) bandgap 1-V reference is not available as an input to the Analog-to-Digital Converter (ADC) module (using ADC input channel AD27) or the Comparator (CMP) module (using CMP input IN6) in Very Low Power Run (VLPR), Very Low Power Wait (VLPW), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), Very Low Leakage Stop3 (VLLS3), Very Low Leakage Stop2 (VLLS2), Very Low Leakage Stop1 (VLLS1), or Very Low Leakage Stop0 (VLLS0) modes.

This erratum does not apply to the VREF module 1.2 V reference voltage.

Workaround: Use of the PMC bandgap 1-V reference voltage as an input to the ADC and CMP modules requires the MCU to be in Run, Wait, or Stop modes.

e5472: SMC: Mode transition VLPR->VLLS0(POR disabled)->RUN, will cause POR & LVD.

Errata type: Errata

Description: The Mode transition of VLPR into VLLS0 (POR disabled) then Exit, with LLWU event, back to to RUN mode will cause a POR and LVD reset instead of the expected WAKEUP exit.

Workaround: The recommendation is to transition from VLPR to RUN before entering VLLS0 with POR disabled mode.

e5745: SPI1: Back to back DMA data transfers are not possible if the core:bus frequency ratio is greater than 4:1

Errata type: Errata

Description: When using DMA with SPI1, if the core:bus frequency ratio is greater than 4:1 (SIM_CLKDIV1[OUTDIV4] greater than 3), the first data transfer in a sequence will be transmitted twice.

This only applies to SPI1.

Workaround: When using DMA with SPI1, the core:bus frequency ratio must be 4:1 or less, SIM_CLKDIV1[OUTDIV4] must be less than 4.

If it is required to use SPI1 with core:bus frequency ratios greater than 4:1, an interrupt or polling mechanism in software must be used.

e5490: SPI1: DMA data transfers at the maximum baud rate can result in corrupted data

Errata type: Errata

Description: DMA transfers of SPI1 data can result in corrupted data when the maximum baud rate is selected for SPI1, SPI1_BR[SPPR] = 0 and SPI1_BR[SPR] = 0.

This only applies to SPI1.

Workaround: When using DMA to transfer Rx or Tx data for SPI1, the SPI1_BR[SPPR] and SPI1_BR[SPR] fields must not both be written to 0.

If it is required to use SPI1 at the maximum baud rate, with SPI1_BR[SPPR] = 0 and SPI1_BR[SPR] = 0, an interrupt or polling mechanism in software must be used.

e5515: TSI: The end of scan flag is not automatically cleared when continuously scanning

Errata type: Errata

Description: The TSI requires the end of scan flag (TSIx_GENCS[EOSF]) to be cleared after each scan. This prevents the out of range interrupt from being available in continuous scanning as each scan needs the TSIx_GENCS[EOSF] bit to be cleared by software. This limits the TSI from providing an optimal low power wake-up capability.

Workaround: There are 3 workarounds that can be used depending on the application:

1. When the TSI is used in normal RUN mode without DMA, at the end of each scan, the TSIx_GENCS[EOSF] bit must be cleared by software. The end of scan can be detected either by polling the TSIx_GENCS[EOSF] bit or by enabling the end of scan interrupt.

2. When DMA is used, it can automatically clear the TSIx_GENCS[EOSF] bit after each scan. This can be used for run mode but not for low power mode.

3. Low power mode applications will have to wake-up on each end of scan, clear the TSIx_GENCS[EOSF] bit and check the out of range flag to determine if touch has happened.

e5744: UART0: Receiver wakeup control bit cannot be set immediately after a wakeup event

Errata type: Errata

Description: The receiver wakeup control bit, UART0_C2[RWU], is cleared by hardware after a wakeup event has occurred. After the UART0_C2[RWU] bit is cleared due to a wake up event, software cannot set this bit for 3 asynchronous UART0 clock cycles.

Workaround: After a wakeup event, with UART0_C2[RWU] previously being set, software must wait 4 clock cycles of the UART0 clock (selected by the SIM_SOPT2[UART0SRC] field) before setting UART0_C2[RWU].

e5563: UART0: When the Receiver Wake Up control bit is set, an IDLE condition is not detected correctly

Errata type: Errata

Description: An IDLE condition requires the receive line to become idle for a full character time, following a period of activity (e.g. a character was received). The IDLE flag cannot become set again until after a new character has been received.

The problem occurs when the Receiver Wake Up control bit is set, UART0_C2[RWU] = 1. In this case, an idle condition is detected whenever the receive line becomes idle for a full character time, regardless of whether a previous character is received or not. This can cause the UART0_C2[RWU] bit to clear (if UART0_C1[WAKE] = 0) and the UART0_S1[IDLE] flag to set (if UART0_S2[RWUID] = 1) incorrectly.

This only applies to UART0.

Workaround: The UART0_C2[RWU] bit must only be set after a character has received and before the UART0_S1[IDLE] flag is set. The UART0_C2[RWU] bit must not be set when the receive line is already idle.

e5753: UART1 / UART2: When the Receiver Wake Up control bit is set, an IDLE condition is not detected correctly

Errata type: Errata

Description: An IDLE condition requires the receive line to become idle for a full character time, following a period of activity (e.g. a character was received). The IDLE flag cannot become set again until after a new character has been received.

The problem occurs when the Receiver Wake Up control bit is set, UARTx_C2[RWU] = 1. In this case, an idle condition is detected whenever the receive line becomes idle for a full character time, regardless of whether a previous character is received or not. This can cause the UARTx_C2[RWU] bit to clear (if UARTx_C1[WAKE] = 0) and the UARTx_S1[IDLE] flag to set (if UARTx_S2[RWUID] = 1) incorrectly.

This only applies to UART1 and UART2. The “x” in the register names refers to either UART1 or UART2.

Workaround: The UARTx_C2[RWU] bit must only be set after a character has received and before the UARTx_S1[IDLE] flag is set. The UARTx_C2[RWU] bit must not be set when the receive line is already idle.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Document Number: KINETIS_L_1N97F
Rev. 05 OCT 2012

freescale