

LICA- Module-1

Syllabus ⇒

Operational amplifier fundamentals ⇒

- ✓ → Basic op-amp ckt.
- ✓ → OP-amp parameters
 - ✓ → i/p & o/p voltage
 - ✓ → CMRR
 - ✓ → PSRR
 - ✓ → offset vfgs and currents
 - ✓ → i/p & o/p impedances
 - ✓ → slew rate
 - ✓ → Frequency limitations

Scd.
Dr. T. C. Manjunath
Prof. & HOD, ECE, DSCE

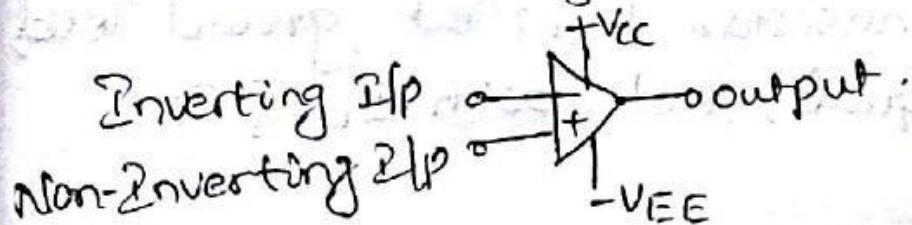
Op-amp as DC amplifiers ⇒

- ✓ → Biasing OP-amps
- ✓ → Direct coupled
 - ✓ → Voltage follower
 - ✓ → Non-INV amp^r
 - ✓ → INV amp^r
 - ✓ → Summing amp^r
 - ✓ → Difference amp^r

Operational Amplifier Fundamentals:

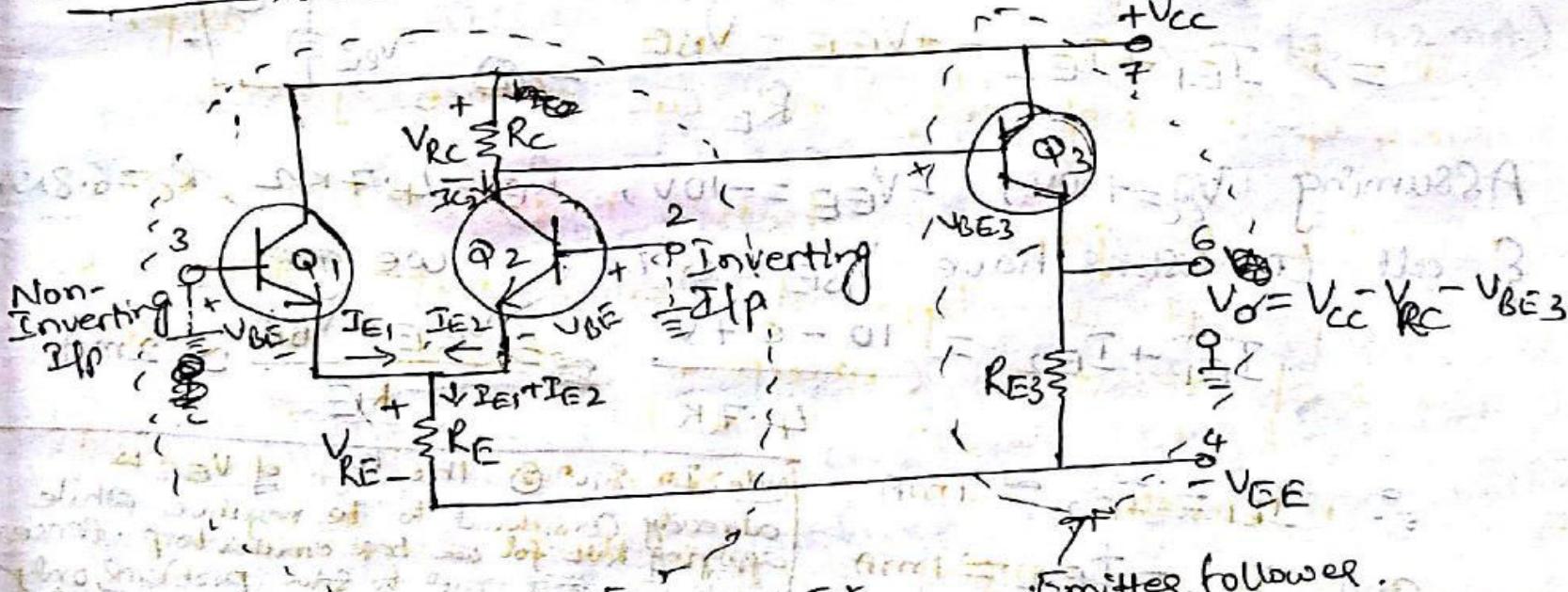
Operational amplifiers are very high gain integrated circuit amplifiers with two high input impedance input terminals [i.e Inverting & Non-inverting inputs] and one low impedance output.

The Circuit Symbol is as shown below.



A signal applied to the inverting input results in a signal of opposite phase at the output.
A signal applied to the non-inverting input produces a signal of identical phase at the output.

Basic operational amplifier circuit:



Differential amplifier (in a op-amp can accept two ip signals & amplify the difference b/w these two input signals)

The basic circuit of an op-amp is as shown above. Supply voltages $+V_{cc}$ & $-V_{EE}$ are provided & the input terminals are grounded. Transistors Q_1 and Q_2 constitute a differential amplifier, which produces a voltage change at the collector of Q_2 when a difference input voltage is applied to the bases of Q_1 and Q_2 .

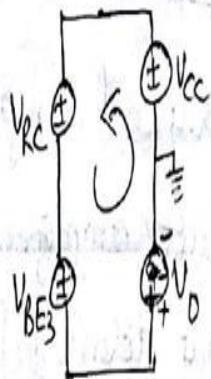
Transistor Q_3 operates as an emitter-follower to provide a low output impedance.

The dc output voltage V_o at terminal 6 is given

$$\text{by } V_o = V_{cc} - V_{RC} - V_{BE3}$$

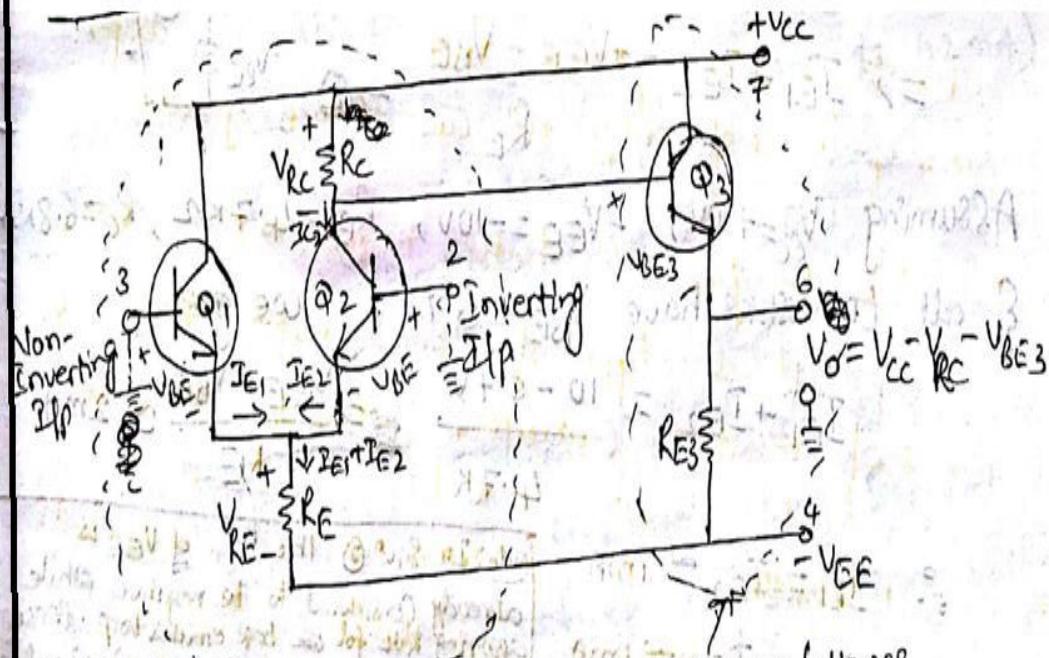
$$\Rightarrow V_o = V_{cc} - V_{RC} - V_{BE3}$$

$$\Rightarrow V_o = V_{cc} - (I_{C2} R_C) - V_{BE} \Rightarrow 0$$



Assuming that Q_1 and Q_2 are matched transistors, i.e. they have equal V_{BE} levels and equal current gains. Then both the transistors bases at ground level, the emitter currents are equal, and both I_{E1} & I_{E2} flow through R_E .

$$\therefore I_{E1} + I_{E2} = \frac{V_{RE}}{R_E}$$



Differential amplifier (that can accept two ip signals & amplify the difference b/w these two input signals)

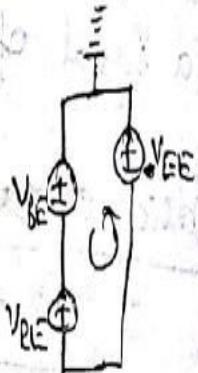
Emitter follower.

With Q_1 and Q_2 bases grounded,

$$+V_{EE} - V_{BE} - V_{RE} = 0$$

$$\Rightarrow V_{RE} = V_{EE} - V_{BE}$$

$$\Rightarrow I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E} \rightarrow 0$$



Assuming $V_{CC} = +10V$, $-V_{EE} = -10V$, $R_E = 4.7k\Omega$, $R_C = 6.8k\Omega$

{ all transistors have $V_{BE} = 0.7V$; we get

$$I_{E1} + I_{E2} = \frac{10 - 0.7V}{4.7k} = \frac{V_{EE} - V_{BE}}{R_E} \approx 2mA$$

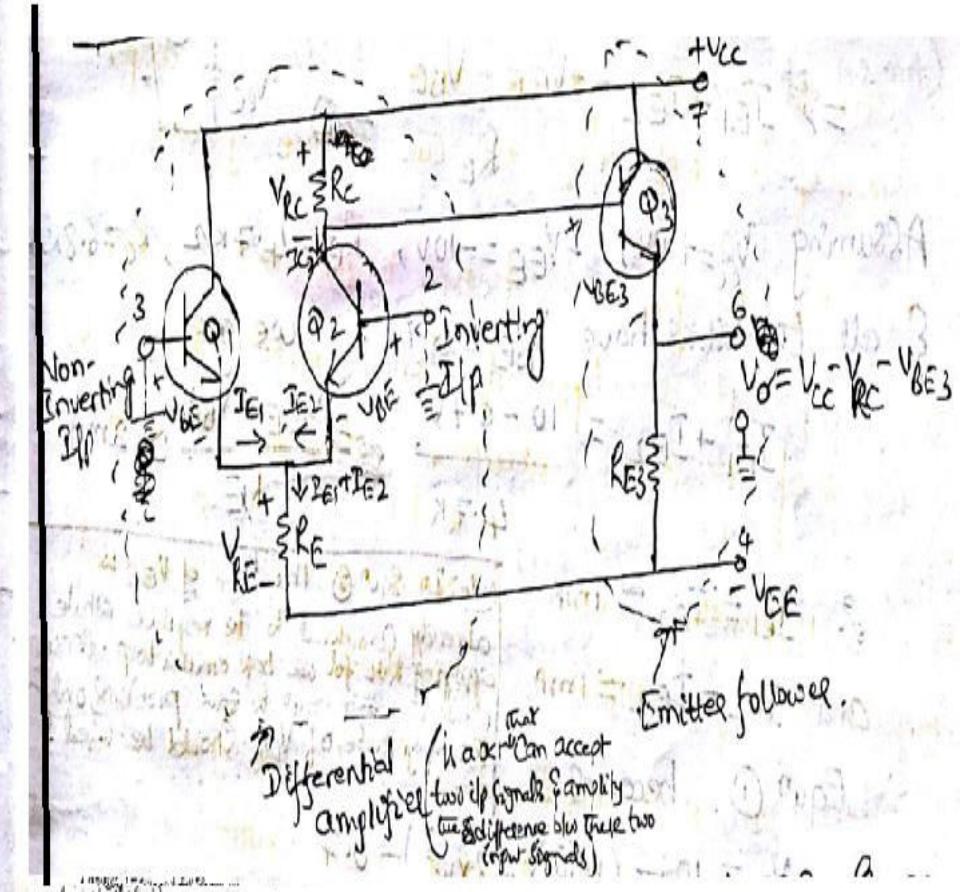
$$\therefore I_{E1} = I_{E2} \approx 1mA$$

$$\text{and } I_{C2} = I_{E2} \approx 1mA$$

\therefore Equn ① becomes

$$V_o = 10 - (1 \times 10^3 \times 6.8 \times 10^{-3}) - 0.7$$

$$V_o \approx 2.5V$$



If a +ve going voltage is applied to the non-inverting input terminal (base of Q_1), the emitter terminal of Q_1 follows the input signal. Since Q_1 & Q_2 emitters are connected together, the emitter of Q_2 is also pulled up by the +ve going signal at the non-inverting input terminal. The base of Q_2 is fixed at ground level so the +ve going signal at its emitter causes a reduction in its base-emitter voltage (V_{BE2}). This results in reduction in I_{C2} & also $\beta_{Q2} I_{C2}$.

If we assume that the going input signal at the base of Q_1 reduces I_{C2} by 0.2mA (i.e. from 1mA to 0.8mA) this gives $V_o = V_{CC} - I_{C2} R_C - V_{BE}$

$$\begin{aligned} \text{This gives } V_o &= V_{CC} - I_{C2} R_C - V_{BE} \\ &= 10 - (0.8 \times 6.8 \times 10^3) - 0.7 \\ &\approx 3.9V. \end{aligned}$$

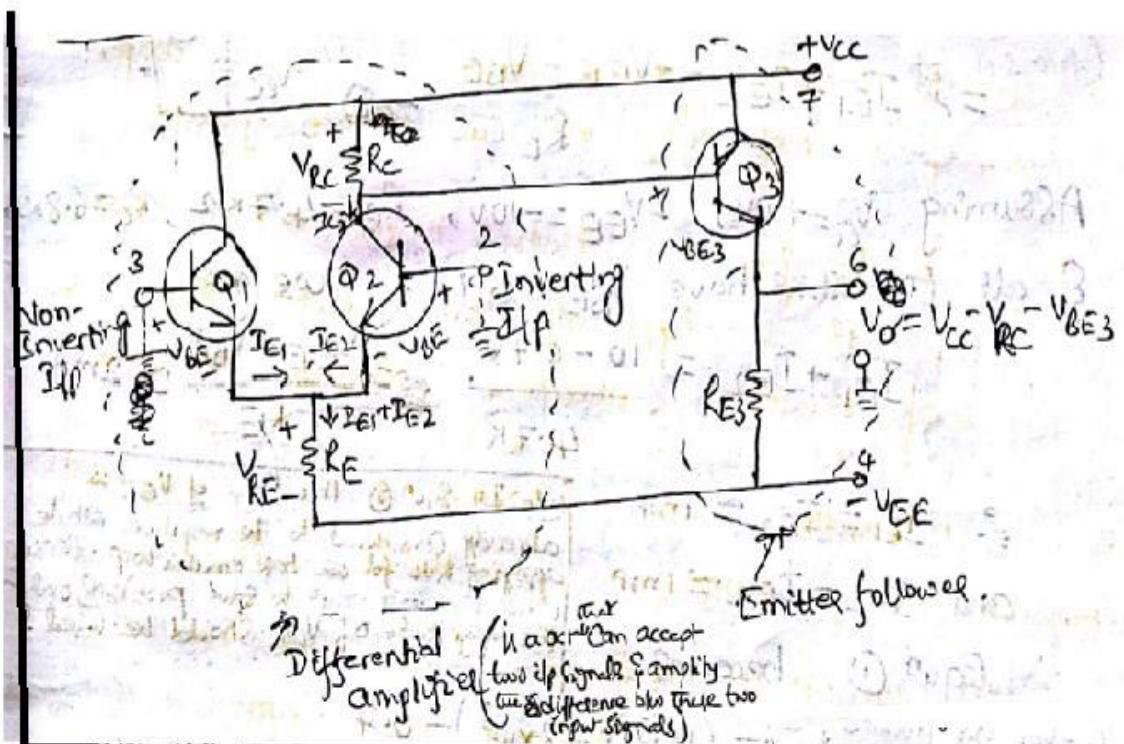
i.e o/p voltage increases from 2.5V to 3.9V, a change of 1.4V for a reduction in 0.2mA in I_{C2} .

If a +ve going voltage is applied to Inverting terminal (base of Q_2), grounding the non-inverting terminal (base of Q_1), Q_1 is reduced by a (i.e. β_{Q1}) similar amount and hence there is an increase in I_{E2} & also in I_{C2} .

If we assume that the going input at Q_2 increases I_{C2} by 0.2mA (i.e. from 1mA to 1.2mA) then $V_o = V_{CC} - I_{C2} R_C - V_{BE}$

$$\begin{aligned} \text{Then } V_o &= V_{CC} - I_{C2} R_C - V_{BE} \\ &= 10 - (1.2 \times 10^{-3} \times 6.8 \times 10^3) - 0.7 \end{aligned}$$

$$V_o \approx 1.1V$$

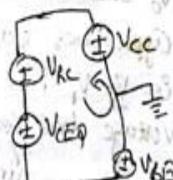


i.e o/p voltage reduced from 2.5V to 1.1V, a change of -1.4V. ∵ the +ve going signal at the inverting input produces negative going voltage at the output.

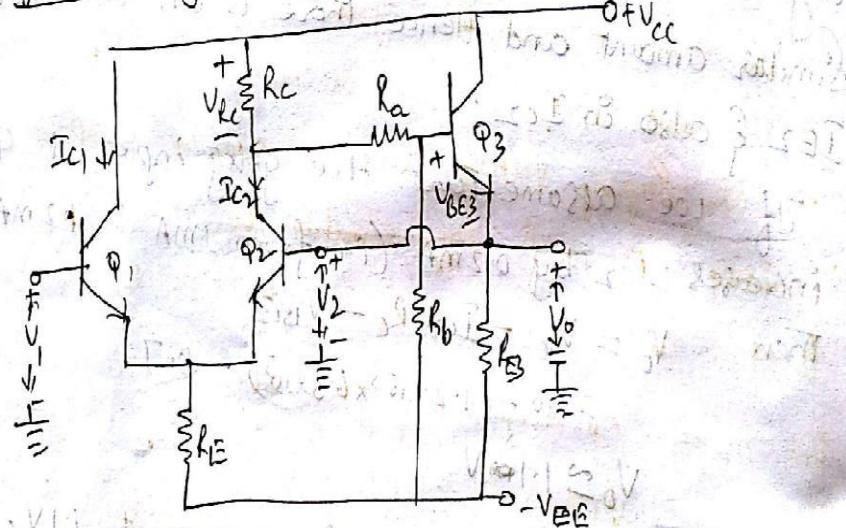
As the transistors are matched $V_{CE1} = V_{CE2} = V_{CEQ}$ which gives the Q point voltage for each transistor i.e.

$$V_{CC} - V_{RC} - V_{CEQ} + V_{BE} = 0$$

$$\therefore V_{CEQ} = V_{CC} - V_{RC} + V_{BE} \rightarrow (3)$$



Input voltage range



The basic op-amp circuit is connected to function as a voltage follower as shown above. Consideration of the circuit shows that as the input voltage is increased positively the output follows it and I_{C2} must decrease in order to raise the Q_3 base voltage. Thus I_{C2} decreases as V_i increases, and at some point I_{C2} is so small that Q_2 approaches cut-off. When this occurs, any further increase in V_i has no effect on the output and so the input voltage has reached its positive going limit.

Similarly, when the output is increased in a -ve direction, I_{C2} increases to increase V_{RC} in order to drive V_{B2} down to keep the output following the input.

Collector Current I_{C1} must decrease in order to increase I_{C2} and so the limit of the increase in I_{C2} occurs when Q_1 approaches cut-off. Hence again, an increase in -ve going input voltage has no further effect and the input voltage has arrived at its negative going limit.

The maximum effective positive going and negative going voltage that may be applied to the input of an op-amp is termed as its input voltage range. The 741 Op-Amp data sheet specifies the typical input voltage range is $\pm 13V$ for a $\pm 15V$ supply.

Output Voltage Range

When the Op-amp is connected to function as either an inverting or non-inverting amplifier, the output voltage can swing in a direction much larger than the input. Just how far the output voltage can swing in a +ve or -ve direction depends upon the supply voltage and on the op-amp internal circuitry. A rough approximation for most op-amps is that the maximum output voltage swing is $(\pm V_{cc} - 1V)$. For a 741 Op-amp with $\pm 15V$ supply, the op voltage swing is $\pm 14V$ when $R_L \geq 10k\Omega$. With lower resistance loads, the op voltage range is reduced. Some op-amps have an output swing that extends from $-V_{EE}$ to $+V_{cc}$. This is referred to as rail to rail operation.

Common Mode Rejection

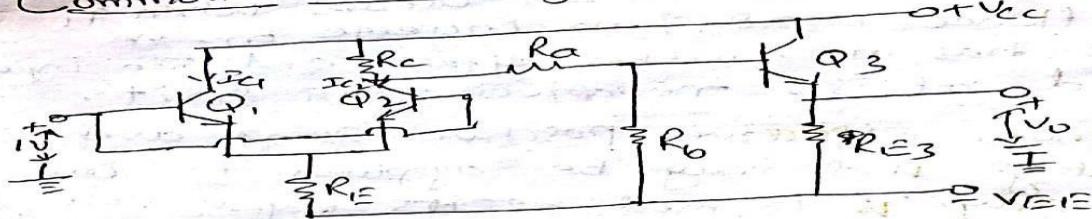


Fig shows a basic ckt of an operational amplifier with common mode rejection. Two inputs short circuited and a common input voltage of IV is applied to it.

Since base voltages of Q_1 & Q_2 are raised to IV , the voltage drop across R_E also increases by IV . This increases I_{C1} and I_{C2} . Thus voltage drop across R_E also increases, which results in a change in the op-amp output V_O . Similarly, if a $-IV$ common mode input is applied, I_{C2} falls and again a change is produced at the circuit output.

Thus Common mode voltage gain A_{cm} is defined as the ratio of change in op-amp voltage to the change in common mode input voltage (V_{icm}).

$$\text{i.e. } A_{cm} = \frac{V_o(cm)}{V_i(cm)}$$

The ability of the op-amp in rejecting common mode inputs is defined as common mode rejection ratio (CMRR).

CMRR is defined as the ratio of the open loop gain 'm' to the common mode gain A_{cm} . i.e.

$$\text{CMRR} = \frac{m}{A_{cm}}$$

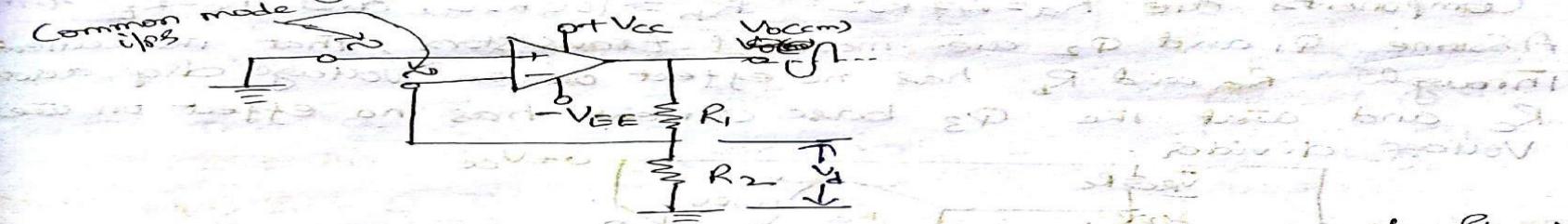
Differential gain/open loop gain ('m') is defined as the ratio of op-amp voltage to input voltage for two inputs. i.e. $m = \frac{V_o}{V_A} = \frac{V_o}{V_{in}}$

The CMRR is usually expressed in decibels.

$$\text{i.e. } (\text{CMRR})_{dB} = 20 \log_{10} \left(\frac{m}{A_{cm}} \right) dB$$

Typical value of CMRR for 741 IC is $90dB$.

The effect of Common mode gain can be modified with feedback to give a closed loop gain. Consider one non-inverting amplifier circuit shown below:



With one input terminal grounded, the circuit of P should also be at ground level. Now suppose a sine wave signal is picked up at both i/p's, as illustrated. This is a common mode mod input.

$$\text{with } \text{op-amp circuit } A_{cm} = \frac{V_{ocm}}{V_{icm}}$$

$$\therefore \text{Op-amp voltage } V_{ocm} = A_{cm} \cdot V_{icm} \quad \text{--- (1)}$$

However, any output voltage will produce a feedback voltage across resistor R_2 , which results in a differential voltage at the op-amp input terminals. The differential voltage at the op-amp input terminals is equal to the output voltage required to cancel V_{ocm} .

$$V_d = \frac{A_{cm} \cdot V_{icm}}{M} \quad \text{--- (2)}$$

Putting (1) in (2), we get

$$V_d = \frac{A_{cm} \cdot V_{icm}}{M} \quad \text{--- (3)}$$

From fig., the feedback voltage V_d across R_2 is

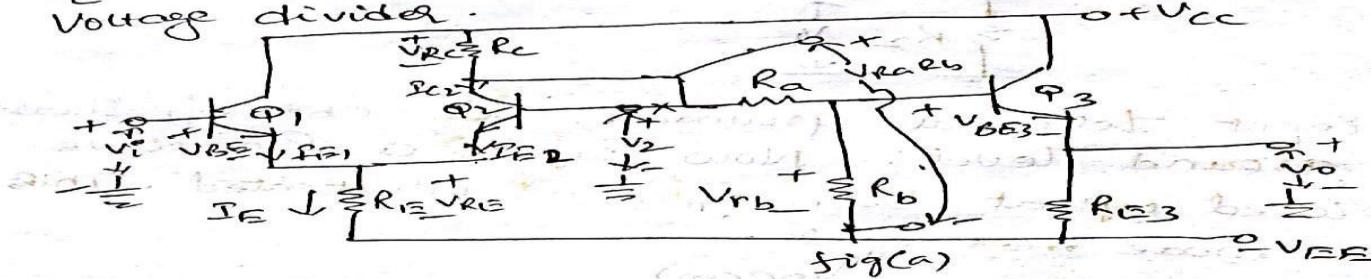
$$V_d = \frac{V_{ocm}}{R_1 + R_2} \cdot R_2 \quad \text{--- (4)} \quad (\text{using voltage division rule})$$

From (3) & (4)

$$V_{ocm} = \frac{A_{cm} \cdot V_{icm}}{M} \cdot \frac{R_1 + R_2}{R_2}$$

$$V_{ocm} = \frac{A_{cm} \cdot V_{icm}}{M} \cdot A_v \quad \text{whole } A_v = \frac{R_1 + R_2}{R_2}$$

① Calculate the voltage and current levels for the circuit shown if $V_{cc} = \pm 10V$, $V_i = V_2 = 0$ and the components are $R_a = 4.7k\Omega$, $R_b = 100k\Omega$, and $R_c = R_E = 4.7k\Omega$. Assume Q_1 and Q_2 are matched transistors, that the current through R_a and R_b has no effect on the voltage drop across R_c and that the Q_3 base current has no effect on the voltage divider.



Soln: Applying KVL for one from the base of Q_1 to $-V_{EE}$ supply we get

$$V_i - V_{BE} - V_{RE} + V_{EE} = 0$$

$$\therefore V_{RE} = V_i + V_{BE} - V_{EE}$$

$$= 0 - 0.7 + 10$$

$$V_{RE} = 9.3V$$

$$\text{WKT } I_E = \frac{V_{RE}}{R_E} = \frac{9.3}{4.7 \times 10^3} = 1.98 \text{ mA}$$

$$\text{WKT } I_{E1} + I_{E2} = I_E$$

$$\therefore I_{E2} = I_E - I_{E1} = I_{C1} = I_{C2} = \frac{I_E}{2} = 0.99 \text{ mA}$$

$$\therefore V_{RC} = I_{C2} \times R_C = 0.99 \times 10^{-3} \times 4.7 \times 10^3 = 4.65V$$

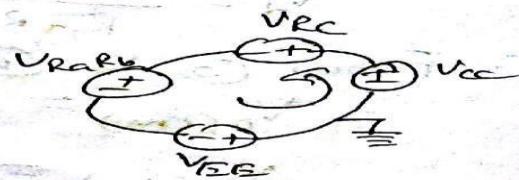
$\frac{V_{RE}}{R_{RE}} \Rightarrow$ Applying KVL for the loop considering $+V_{cc}$, V_{RC} , V_{RARB} & $-V_{EE}$ we get

$$V_{cc} - V_{RC} - V_{RARB} + V_{EE} = 0$$

$$\therefore V_{RARB} = V_{cc} - V_{RC} + V_{EE}$$

$$= 10 - 4.65 + 10$$

$$= 15.35V$$



$$\therefore V_{RB} = \frac{V_{RA} R_B \times R_B}{R_A + R_B} = \frac{15.53 \times 100 \times 10^3}{100 \times 10^3 + 4.7 \times 10^3} = 10.4 \text{ V}$$

$\therefore V_{RA} = V_{RA} R_B - V_{RB} = 15.35 - 10.4 = 4.95 \text{ V}$

Now applying KVL for the loop Considering $+V_{CC}$, V_{RC} , V_{RA} , V_{BES} and V_O we get

$$V_{CC} - V_{RC} - V_{RA} - V_{BE} - V_O = 0$$

$$\therefore V_O = V_{CC} - V_{RC} - V_{RA} - V_{BE}$$

$$= 10 - 4.65 - 4.95 - 0.7 =$$

$$V_O = -0.3 \text{ V}$$



- (2) Calculate V_O for the circuit of fig(a). (i.e previous problem) when $V_{CC} = \pm 15 \text{ V}$ & R_C & R_{B2} are changed to $5.6 \text{ k}\Omega$.

- (3) A 741 Op-amp is used in a non-inverting amplifier with a voltage gain of 50. Calculate the typical CMRR with a voltage that would result from a common-mode input voltage that would result from a common-mode input with a peak level of -100 mV .

$$\text{WKT } (\text{CMRR})_{dB} = 20 \log_{10} (\text{CMRR})$$

$$\text{CMRR} = \text{antilog} \frac{(\text{CMRR})_{dB}}{20}$$

$$= \text{antilog} \frac{90 \text{ dB}}{20} \quad (\text{i.e. } \frac{90}{20} = 4.5)$$

(info from the 741 datasheet; typical CMRR = 90dB)

$$\therefore \text{CMRR} = 31623$$

$$\text{WKT } V_{O(\text{cm})} = \frac{V_{O(\text{cm})}}{\text{CMRR}} \times A_V = \frac{100 \times 10^3 \times 50}{31623} = 158 \mu\text{V}$$

- (4) An LM308 Op-amp circuit with a closed loop gain of 33 has a common mode input of 1.5 V . Calculate the maximum off voltage this might produce. The minimum CMRR for LM308 is 80dB.

Soln: Given $(CMRR)_{dB} = 80dB$, $A_V = 33$, $V_{o(Ccm)} = 1.5V$

$$WKT \quad (CMRR)_{dB} = 20\log_{10}(CMRR)$$

$$80 = 20\log_{10}(CMRR)$$

$$\therefore CMRR = \text{antilog}_{10}\left(\frac{80}{20}\right) = 10000$$

$$WKT \quad V_{o(Ccm)} = \frac{V_{o(Ccm)}}{CMRR} \cdot A_V = \frac{1.5}{10000} \times 33 = 5mV.$$

Q5) When a 741 op-amp having a typical CMRR of 90dB is used in a non-inverting amplifier with a voltage gain of 100, the op. voltage was measured to be 15.8mV with some common-mode ZLP. Determine the common mode ZLP voltage.

Soln: Given $A_V = 100$, $V_{o(Ccm)} = 15.8mV$, $V_{o(Ccm)} = ?$
 $(CMRR)_{dB} = 90dB$.

$$WKT \quad CMRR = \text{antilog}_{10}\left(\frac{(CMRR)_{dB}}{20}\right) = 31622.78$$

$$WKT \quad V_{o(Ccm)} = \frac{V_{o(Ccm)} \cdot CMRR}{A_V} = \frac{15.8 \times 10^{-3} \times 31622.78}{100}$$

$$V_{o(Ccm)} = 5V$$

Power Supply Rejection Ratio (PSRR):

In basic op-amp circuit, a variation in $-V_{EE}$ have the same effect as an ZLP or voltage change. Thus variations in V_{CC} and V_{EE} do produce some changes at op. op.

The PSRR is a measure of how effective the operational amplifier is in dealing with variations in supply voltage.

The PSRR is the ability of the op-amp to reject variations in the power supply voltages.

$$\text{ie } PSRR = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}$$

If a variation of IV in V_{CC} & V_{EE} caused the output change by IV , then the PSRR is $IV \text{ per volt}$ (mV/V)

If the output changes by 10mV when one of the supply lines changes by 1V , then the supply rejection ratio is 10mV/V .

For a 741 op-amp, the PSRR is typically $30\mu\text{V/V}$.

For LM108, the supply PSRR is expressed in decibels.

- ① A 741 operational amplifier uses a $\pm 15\text{V}$ supply with a $2\text{mV}, 120\text{Hz}$ ripple voltage superimposed. Calculate the amplitude of the output voltage produced by the power supply ripple.

$$\text{Ans: WKT for } 741 \Rightarrow \text{PSRR} = 30 \mu\text{V/V}$$

$$\text{WKT } \text{PSRR} = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}$$

$$V_o(\text{ripple}) = \text{PSRR} \times V_s(\text{ripple})$$

$$= 30\mu\text{V/V} \times 2\text{mV}$$

$$V_o(\text{ripple}) = 60\text{nV}$$

- ② An LM108 op-amp has a typical PSRR of -80dB , working with $\pm 15\text{V}$ supply having 3mV ac ripple. Calculate the max level of op voltage ripple.

$$\text{Ans: Given } (\text{PSRR})_{AB} = -80\text{dB}, V_s(\text{ripple}) = 3\text{mV}, V_o(\text{ripple}) ?$$

$$(\text{PSRR})_{AB} = 20 \log_{10} (\text{PSRR})$$

$$-80 = 20 \log_{10} (\text{PSRR})$$

$$\therefore \text{PSRR} = 10^4$$

$$\text{WKT } \text{PSRR} = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}$$

$$\therefore V_o(\text{ripple}) = \text{PSRR} \times V_s(\text{ripple}) = 10^4 \times 3\text{mV} = 0.3\mu\text{V}$$

- ③ A 741 op-amp having a PSRR of $30\mu\text{V/V}$, has a minimum offset signal level of 100mV . Op-amp ripple voltage produced by the ripple on the supply voltages is not to exceed 0.1% of the minimum op-amp signal level. Determine the maximum permissible supply voltage ripple.

$$\text{Given PSRR} = 30\mu\text{V/V}$$

$$\text{Minimum op-amp Signal} = 100\text{mV}$$

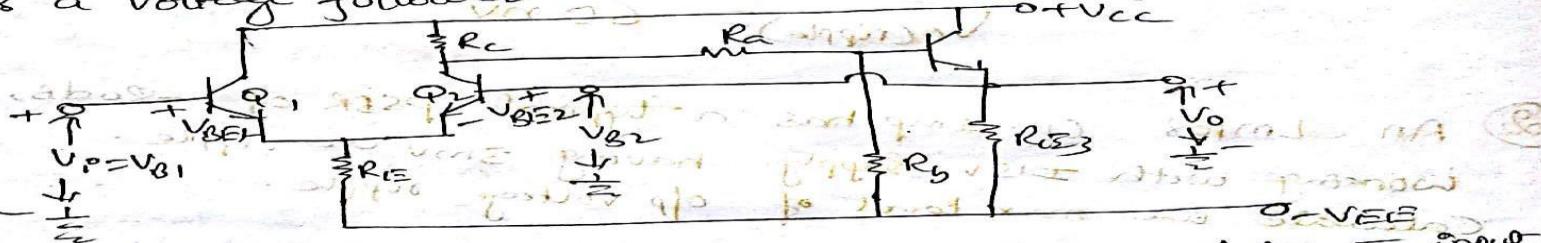
$$\therefore V_o(\text{ripple}) = 0.1\% \text{ of minimum op-amp Signal} \\ = \frac{0.1}{100} \times 100\text{mV} = 0.1\text{mV}$$

$$V_s(\text{ripple}) = \frac{V_o(\text{ripple})}{\text{PSRR}} = \underline{\underline{3.33\text{mV}}}$$

Offset Voltages and Currents

Input offset voltage and output offset voltage

The basic operational amplifier circuit connected to function as a voltage follower is shown in fig.

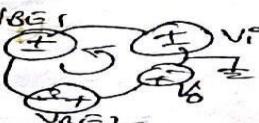


For the output voltage to be exactly equal to the input, the transistors Q₁ and Q₂ must be perfectly matched. The output gain voltage can be calculated as,

$$V_o = V_{BE1} + V_{BE2} - V_0 = 0.1 \text{ mV}$$

$$\text{i.e. } V_o = V_i - V_{BE1} + V_{BE2} \rightarrow ①$$

With $V_{BE1} = V_{BE2}$ and $V_i = 0$ $V_o = V_i = 0\text{V}$



Now suppose that the transistors are not perfectly matched and that $V_{BE1} = 0.7V$ while $V_{BE2} = 0.6V$. with the input at ground level,

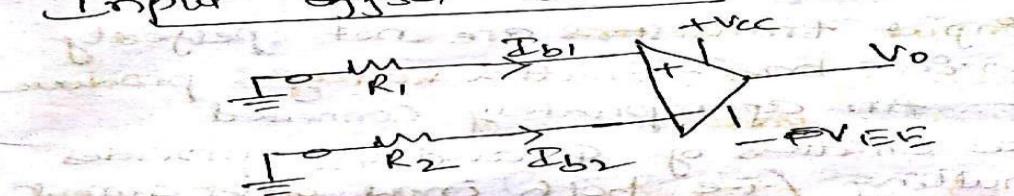
$$V_o = 0 - 0.7V + 0.6V = -0.1V.$$

This $-0.1V$ unwanted output is known as an "offset voltage".

To set $V_o = 0V$, the input would have to be raised to $+0.1V$. This is termed as "input offset voltage" (V_{os}).

The typical input offset voltage for a JFET op-amp is $1mV$.

Input bias current

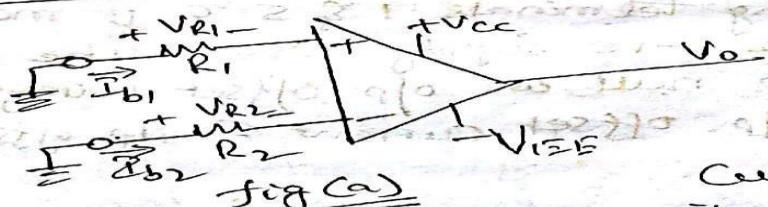


The average value of the two currents flowing into the op-amp EIP terminals is called EIP bias current.

$$\text{i.e. } I_b = \frac{I_{b1} + I_{b2}}{2}$$

For a JFET, maximum value of I_b is $500nA$.

Input offset current



The input bias currents produce voltage drops across resistors R_1 & R_2 .

i.e. $I_{pos} = |I_{b1} - I_{b2}|$. The difference in bias currents produces unequal

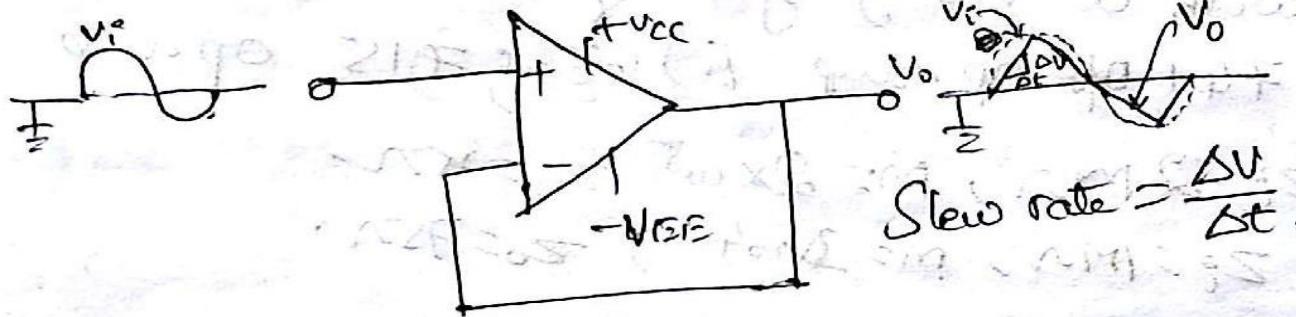
resistor voltage drops which result in an unwanted output offset voltage. Typical input offset current for a JFET op-amp is $20nA$ (min) $200nA$ (max)

Slew rate:

The Slew rate (S) is defined as the maximum rate of change of output voltage with time.

When the input voltage changes too quickly, output waveform distortion results in ~~an~~ output. This is shown in fig below, which shows a sine wave i/p to a

Voltage follower producing a triangular output waveform. The triangular o/p results because the output simply cannot move fast enough to follow the sine wave input.



$$\text{Slew rate} = \frac{\Delta V}{\Delta t}$$

Typical slew rate of the 2741 opamp is $0.5V/\mu s$. This means that $1\mu s$ is required for the output to change by $0.5V$.

The equation relating time, voltage change & slew rate is

$$t = \frac{\Delta V_o}{S}$$

Input Impedance

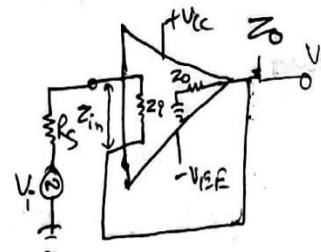
It is the equivalent impedance (or resistance) measured at either the inverting or noninverting input terminal with the other input terminal grounded.

In most op amp applications some form of -ve feedback is normally provided by externally connected components.

From the feedback, the i/p impedance of opamp at the i/p terminal is given by

$$Z_{in} = (1 + M\beta) Z_o$$

where Z_o = Opamp i/p impedance without feedback
(or an impedance the hardware had in the absence of -ve feedback)



M = Opamp open loop gain

β = feedback factor = 1 for a voltage follower

Z_o = Thevenin's source (output) impedance of the open

The impedance of signal sources connected at the input terminals should be very much smaller than the amplifier i/p impedance to avoid a loss of signal across R_s .

Ideally input impedance of an opamp is infinite but for a 741 it is of the order of $2M\Omega$. Min value is $0.3M\Omega$.

Output Impedance

It is the equivalent impedance measured b/w the output terminal of an Opamp & the ground. The typical o/p impedance for 741 is 25Ω .

The o/p impedance of an opamp with -ve feedback is $Z_{out} = \frac{Z_o}{1 + M\beta}$

Load impedance (resistance) connected at the o/p of an opamp should be very much larger than the o/p impedance to avoid loss of o/p as a voltage drop across Z_L .

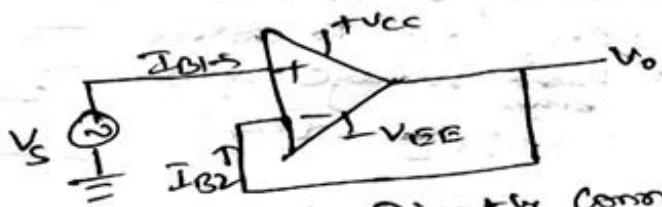
Op amps as DC amplifiers

Biasing of Op-Amps

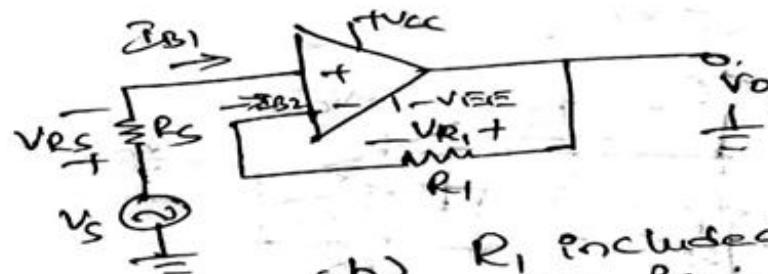
Bias current paths:

The op-amps must be correctly biased if they are to function properly. Base currents must flow into the terminals for the transistors to be operational.

In most of the op-amp applications, the dc bias voltage V_B is applied and V_B is approximately halfway ($\frac{V_{CC}}{2}$ or $\frac{-V_{EE}}{2}$) between the +ve & -ve supply voltages.



(a) Directly Connected
voltage follower



(b) R_1 included to
match R_S .

One of the two E/P terminals is usually connected to the op-amp o/p to facilitate -ve feedback. The other E/P is biased directly to ground via Source voltage (V_S) as shown in fig (a).

Fig (b) shows a resistor R_1 included in series with the inverting terminal to match signal source resistance R_S .

R_S & R_1 should be selected in such a way that their drops are equal. Any difference in these drops will have the same effect as an E/P offset voltage.

Maximun bias resistor values

If very small resistance values are selected for R_S & r_e , the voltage drops across them will be small. If R_S & r_e are large, the voltage drops might be several volts. Hence for good bias stability, the maximum voltage drop across the resistors should be much smaller than the typical forward biased V_{BE} level. Usually the voltage drop is made at least ten times smaller than V_{BE} .

$$\text{inc } I_{B(\max)} R_{(max)} = \frac{V_{BE}}{10} = \frac{0.7}{10} = 0.07 \text{ V}$$

WKT $I_{B(\max)} = 500 \text{ nA}$ for 741 op amp.

$$\therefore R_{(max)} = \frac{0.07}{500 \text{ nA}} \approx 140 \text{ k}\Omega$$

This is the max value for the bias resistors for a 741 op amp.

For other op-amps, $R_{(max)}$ is calculated using the eqn

$$R_{(max)} = \frac{0.1 V_{BE}}{I_{B(\max)}}$$

Potential divider bias

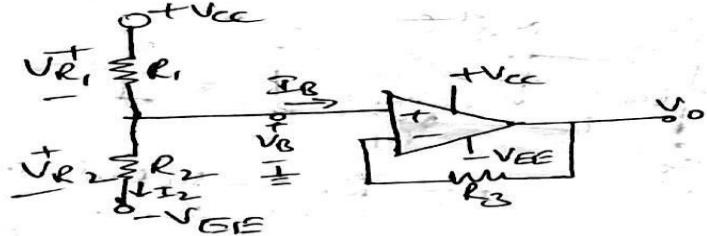


Fig 8 shows a potential divider (R_1 & R_2) employed to derive a input bias voltage from the power supply voltage.

The potential divider current (I_2) should be much larger than the op-amp maximum input bias current ($I_{B(max)}$). This is to ensure that I_B , and any bias current variation, has a negligible effect upon the bias voltage level V_B . usually I_2 is made 100 or more times I_B . Then

$$R_1 = \frac{V_R1}{I_2} \quad \& \quad R_2 = \frac{V_R2}{I_2} \quad (\text{means } I_B \text{ is very very small & negligible compared to } I_2)$$

Typically, $I_{B(max)} = 500 \text{ nA}$ for 741 op amp.

$$\therefore R_2 = 500 \text{ nA} \times 100 = 50 \mu\text{A}$$

This is the minimum level for R_2 when using 741 & 2D it would be quite satisfactory to use a current of 1mA.

V_{R1} & V_{R2} would usually be selected to give V_B close to ground level, or half way b/w $+V_{CC}$ & $-V_{EE}$. But V_B can be above or below ground level so long as it is within the specified input voltage range (i.e. minimum of $\pm 12V$ for a 741 with a $\pm 15V$ supply).

The resistance seen when looking out of the non-inverting terminal is $R_1 \parallel R_2$.

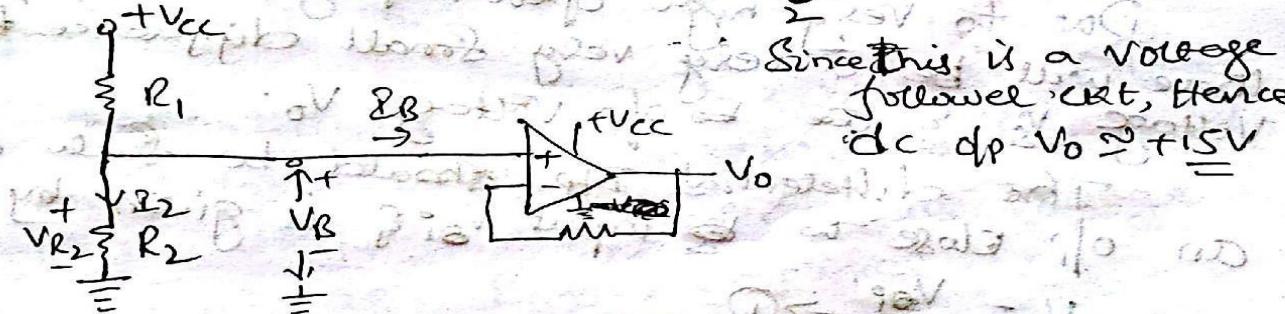
To equalize voltage drops at the input terminals, we must have

$$I_{B2} R_3 = I_{B1} (R_1 \parallel R_2)$$

$$\Rightarrow \text{or } R_3 = R_1 \parallel R_2$$

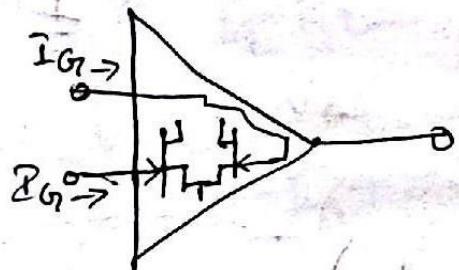
A single polarity supply voltage can be employed with an op-amp as shown in fig below. The input terminals should usually be biased at approximately half the supply voltage ($\frac{+V_{CC}}{2}$).

Ex: If $V_{CC} = 30V$, then $V_B = V_{R2} \approx \frac{V_{CC}}{2} = 15V$



Since this is a voltage follower circuit, hence DC op $V_o \approx +15V$

Biasing BIFET Op-Amps



→ BIFET op-Amps are operational amplifiers with FET i/p stages.

→ They draw very low levels of input bias current (in the order of 50pA)

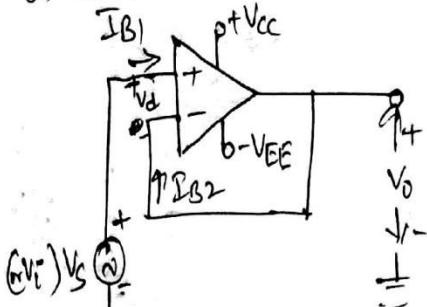
→ In this case the usual design approach of selecting resistor currents 100 times $I_{B\max}$ would result in very high resistor values which are undesirable because of the following reasons

- i) A charge can accumulate at the gate & this might take a relatively long time to discharge. This results in unstable gate voltage & bias conditions would be uncertain.
- ii) Stray capacitance becomes more effective as resistance value increases, possibly resulting in unwanted circuit oscillations.

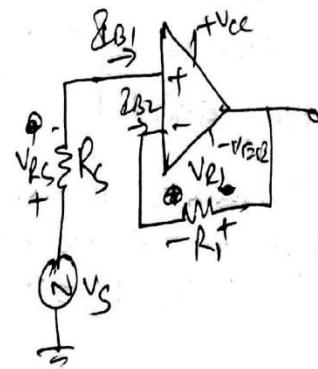
— Hence for BIFET opamps, the resistance seen when looking out of either i/p terminal should not exceed $1\text{M}\Omega$.

Direct Coupled Voltage follower

a) Design:



(a) Directly Coupled Connected voltage follower



(b) R_1 is included to match R_s .

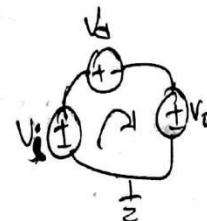
Without using any external components it is possible to use op-amp as a direct coupled voltage follower as shown in fig(a).

Due to very high open loop gain (m) of the op-amp there will be a very very small difference b/w the o/p voltage V_s & the o/p voltage V_o .

The differential Z_{IP} should be such as to produce an o/p close to the input V_s if is given by

$$V_d = \frac{V_o}{m} \rightarrow ①$$

Applying KVL from i/p to o/p we get



$$V_i - V_d - V_o = 0$$

$$\Rightarrow V_o = V_i - V_d \rightarrow ②$$

Put ① in ②

$$V_o = V_i - \frac{V_o}{m} = V_i \left(1 - \frac{1}{m}\right)$$

However as shown in fig(b), R_1 is used b/w o/p & inverting terminal to match the source resistance R_s .

Let the maximum values of I_{B1} & I_{B2} are $I_{B1(\max)}$ & $I_{B2(\max)}$, Then the maximum voltage drop across each resistor is

$$I_{B1(\max)} R_s = I_{B2(\max)} R_1$$

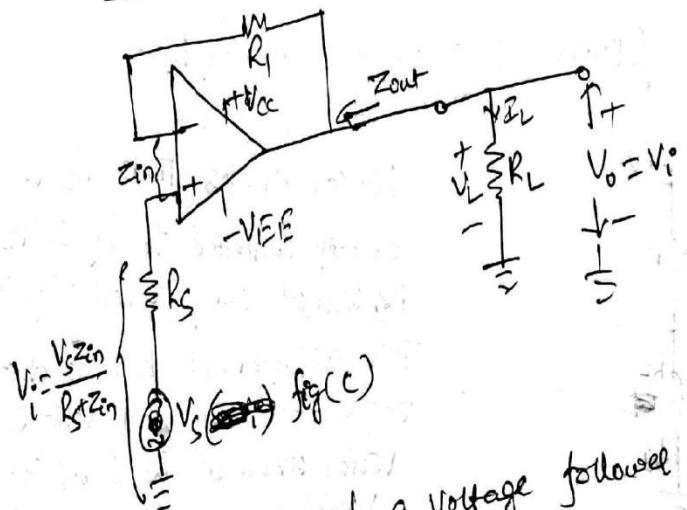
The input offset voltage produced is given by
 $V_{i\text{off}} = I_{i\text{off}} \times (R_s + R_1)$

The Z_{IP} impedance of voltage follower is given by

$$Z_{in} = (1+m) Z_o$$

The o/p impedance is given by $Z_{out} = \frac{Z_o}{(1+m)}$

b) Performance:
Reducing loading effect using voltage follower.



W.R.T The Input Impedance of a voltage follower is

Very ~~high~~ is given by

$$Z_{in} = (1 + M) Z_i \quad (\text{Eqn})$$

& o/p impedance is given by $Z_{out} = \frac{Z_o}{1 + M}$

Because of high Z_{in} & low Z_{out} , voltage follower is used to convert high impedance source to low o/p impedance thus acting as a buffer. Thus voltage follower is also called as Buffer amplifier.

The load voltage is given by

$$V_o = I_L R_L$$

$$V_L = \frac{V_o}{R_s + Z_{out}} \cdot R_L$$

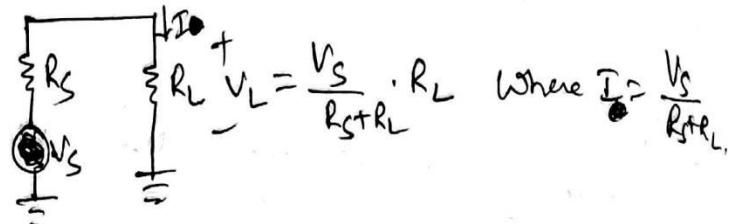
Z_{out} is normally much smaller than R_L i.e $R_L \gg Z_{out}$. Thus neglecting Z_{out} we get

$$V_L = \frac{V_o \cdot R_L}{R_L}$$

appear as o/p

\downarrow Thus there is effectively no signal loss & all of o/p voltage V_o appears across load resistance.

~~Conclude~~ If R_L is directly connected to the source as shown below, part of o/p signal is lost.



$$\text{Where } I_o = \frac{V_s}{R_s + R_L}$$

c) Voltage follower using potential divider bias.

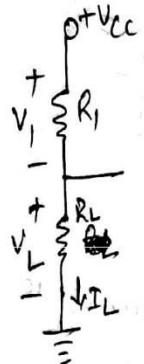


Fig (a) Shows that R_L is directly connected to Supply through R_1 without using a voltage follower.

This arrangement has a disadvantage that the load voltage varies when the load resistance varies.

(a) V_L derived directly from V_C varies when R_L varies

$$\text{Design: } 1) I_L = \frac{V_L}{R_L}$$

2) Applying KVL to the cut we get

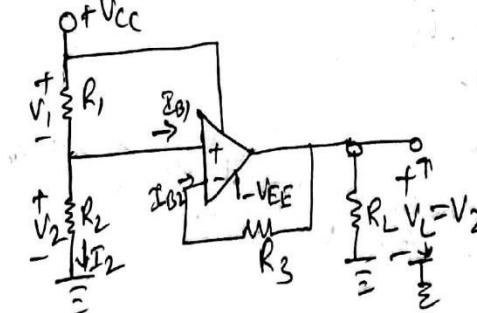
$$V_C - V_1 - V_L = 0 \\ \therefore V_1 = V_C - V_L$$

$$3) R_1 = \frac{V_1}{I_L}$$

$$4) V_L = I_L R_L = \frac{V_C}{R_1 + R_L} \cdot R_L$$

5) when R_L changes (say -10%)

$$V_L = \frac{V_C (R_L - 10\% \text{ of } R_L)}{R_1 + (R_L - 10\% \text{ of } R_L)}$$



(b) A potential divider & a voltage follower produces a constant V_L

Design:

$$1) V_2 = V_L$$

$$2) V_1 = V_{CC} - V_L$$

$$3) I_2 = 100 I_B (\text{max})$$

$$4) R_2 = \frac{V_2}{I_2}$$

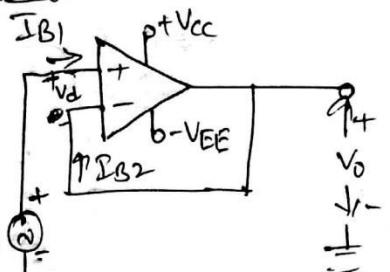
$$5) R_1 = \frac{V_1}{I_2}$$

6) When R_L changes (say -10%), $\underline{V_L = V_2}$, i.e. no change occurs in V_L .

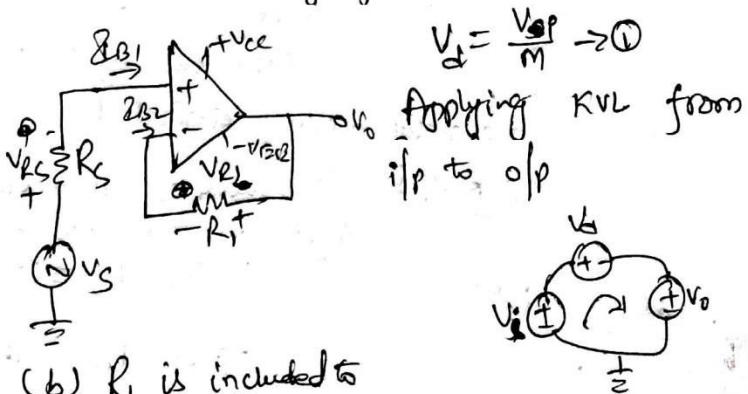
$$7) R_3 = R_1 || R_2$$

Direct Coupled Voltage follower

a) Design:



(a) Directly coupled connected voltage follower



(b) R_1 is included to match R_s .

$$V_d - V_d = V_o \Rightarrow V_o = V_d - V_d \rightarrow (2)$$

put (1) in (2)

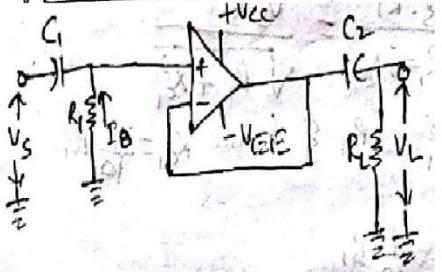
$$V_o = V_d - \frac{V_o}{m} = V_o \left(1 - \frac{1}{m}\right) \parallel$$

$$Z_{B1(\max)} R_s = Z_{B2(\max)} R_1$$

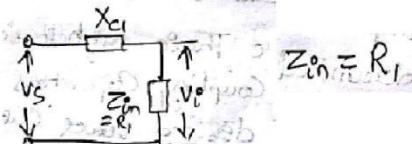
$$Z_{in} = (1+m) Z_o \quad Z_{out} = \frac{Z_o}{(1+m)}$$

$$Z_{in} = (1+m) Z_o \quad Z_{out} = \frac{Z_o}{(1+m)}$$

Capacitor Coupled Voltage follower



$$\text{Design: } f_{1(\max)} = \frac{(1+m)V_{BE}}{2(B(\max))}$$

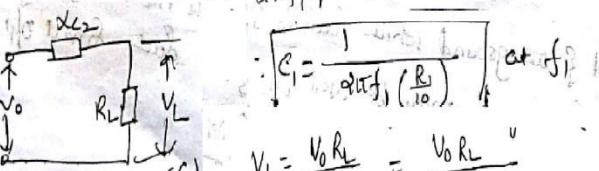


(b) Signal voltage is divided across $X_{C1} \parallel Z_{in}$

$$V_d = \frac{V_i \cdot R_1}{R_1 + jX_{C1}} = \frac{V_i \cdot R_1}{R_1 - jX_{C1}} = \frac{V_i \cdot R_1}{\sqrt{R_1^2 + X_{C1}^2}}$$

To have $V_d = V_i \cdot \sqrt{R_1^2 + X_{C1}^2} \approx R_1 \parallel X_{C1}$ at lower cutoff freq f_1 .

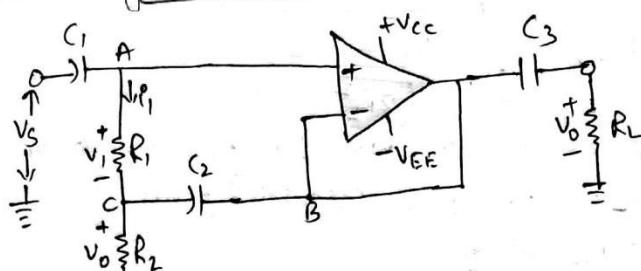
$$\text{i.e. } \frac{1}{j2\pi f_1} = \frac{1}{10} R_1$$



$$V_L = \frac{V_o R_L}{R_L - jX_{C2}} = \frac{V_o R_L}{\sqrt{R_L^2 + X_{C2}^2}} = 0.707 V_o = V_o - 3dB$$

$$X_{C2} = R_L \text{ at } f_1 \quad \text{which gives } C_2 = \frac{1}{2\pi f_1 R_L}$$

High Z_{in} Capacitor Coupled Voltage follower



Design: Step 3.

Let $R_1 + R_2 = R_{max}$. Then R_{max} is calculated by using

$$R_{max} = \frac{0.1 V_{BE}}{f_1 (B_{max})}$$

If $R_1 = R_2$, then $R_1 = R_2 = \frac{R_{max}}{2}$

If $R_1 = R_2$, then maintain feedback voltage same as V_o at lowest operating frequency, $X_{C2} = \frac{R_2}{10}$ at f_1

$$\therefore C_2 = \frac{1}{2\pi f_1 (\frac{R_2}{10})}$$

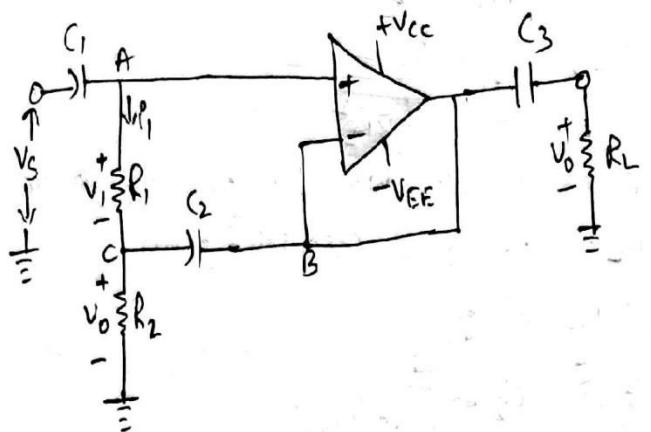
C_3 can be obtained similar to basic capacitor coupled voltage follower. i.e. $C_3 = \frac{1}{2\pi f_1 R_L}$

The impedance of G should be determined theoretically by using $X_{C1} = \frac{Z_{in}}{10}$ at f_1 . But due to the effect of stray capacitance, practically C_1 is calculated by using $X_{C1} = \frac{R_1}{10}$ at f_1

$$\therefore C_1 = \frac{1}{2\pi f_1 (\frac{R_1}{10})} \text{ at } f_1$$

If $R_1 = R_2 = R_{max}$, then $C_1 = C_2$

High Z_{in} Capacitor Coupled Voltage follower



WKT the input impedance of the Capacitor Coupled Voltage follower is R_1 . This gives a much smaller input impedance than that of a direct-coupled voltage follower. The above fig shows a method by which the input impedance of the Capacitor Coupled Voltage follower can be increased.

The Capacitor C_2 is connected b/w the nodes B & C. Since the input is AC signal, C_2 acts as a short circuit. Hence $V_B = V_0 = V_C$. Thus V_0 is developed across R_2 .

$$\text{From the ext, } V_i = V_s - V_0 \rightarrow ①$$

But V_i is the voltage across two o/p terminals of Op-Amp which acts as differential voltage V_d . i.e $V_d = \frac{V_o}{A_{OL}}$

$$\therefore V_o = A_{OL} V_d \rightarrow ② \quad \text{where } A_{OL} = \text{open loop}$$

$$= A_{OL} \left(\frac{V_s - V_0}{R_1} \right)$$

Put ② in ①

$$V_i = V_s - A_{OL} V_d$$

$$V_i (1 + A_{OL}) = V_s$$

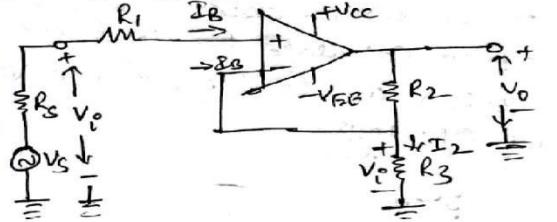
$$V_i = \frac{V_s}{1 + A_{OL}} \rightarrow ③$$

$$\therefore i_1 = \frac{V_i}{R_1} = \frac{V_s}{R_1(1 + A_{OL})} \rightarrow ④$$

The input impedance at the non inverting terminal is

$$Z_{in} = \frac{V_s}{i_1} = R_1(1 + A_{OL}) \rightarrow ⑤$$

Direct Coupled Non-Inverting amplifier



Design:

$$\rightarrow \text{Voltage gain} \\ A_V = \frac{R_2 + R_3}{R_3}$$

$$\rightarrow I_2 = 100 \beta B_{\max}$$

$$\rightarrow R_1 = (R_2 + R_3)$$

If R_1 is not much larger than $R_2 + R_3$, then determine R_1 using

$$(R_1 + R_S) \approx (R_2 + R_3)$$

For BJT, select $R_1 = 1M\Omega$

$\rightarrow R_2 \& R_3$ determined using V_o, V_i & I_2

From fig

$$V_o = (R_2 + R_3) I_2$$

$$R_3 = \frac{V_i}{I_2}$$

\rightarrow For non-2nv amplifier feedbae factor is given by

$$\beta = \frac{1}{A_V} = \frac{R_3}{R_2 + R_3}$$

\rightarrow z_{in} impedance, $z_{in} = (1 + m\beta) z_e$

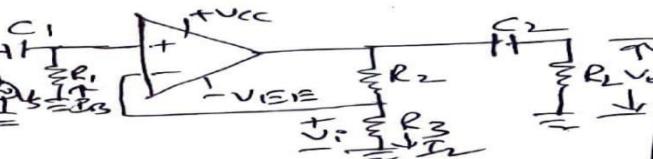
z_{in} seen from Clp source is

$$z_{in} = R_1 + z_{in}$$

\rightarrow z_{out} impedance

$$z_{out} = \frac{z_o}{(1 + m\beta)} = \frac{z_o}{(1 + M)} \quad (1 + M = \frac{1}{A_V})$$

Coupled Non-Inverting amplifier



Design:

$$\rightarrow R_1 = R_{\max} = \frac{0.1 V_{BIE}}{\beta B_{\max}}$$

$$\rightarrow X_{C1} = \frac{1}{10} R_1 \text{ at } f_1$$

$$\therefore C_1 = \frac{1}{2\pi f_1 (R_1/10)}$$

$$\rightarrow X_{C2} = R_L$$

$$\therefore C_2 = \frac{1}{2\pi f_1 R_L} \text{ at } f_1$$

$$\rightarrow I_2 = 100 \beta B_{\max}$$

$$\rightarrow R_3 = \frac{V_i}{I_2}$$

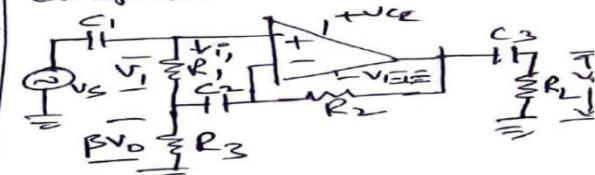
$$\rightarrow A_V = \frac{V_o}{V_i} \text{ where}$$

$$A_V = \frac{R_2 + R_3}{R_3}$$

$$\rightarrow V_o = (R_2 + R_3) I_2$$

$$\rightarrow z_{in} = R_1$$

High Zin Capacitor Coupled Non-Inverting amplifier



Design:

\rightarrow z_{in} impedance can be increased by using C_2

\rightarrow In this case the voltage feedback from V_2 via R_2, C_2 & R_3 is not 100%. Instead V_2 is attenuated by a factor β , where

$$\beta = \frac{1}{A_V} = \frac{R_3}{R_2 + R_3}$$

$$\rightarrow \text{From fig} \quad V_i = V_S - \beta V_o \rightarrow ①$$

$$\text{WKT } \cancel{V_i = V_S} \quad V_i = \frac{V_o}{m}$$

$$\Rightarrow V_o = m V_i \rightarrow ②$$

$$V_i = V_S - \beta m V_i$$

$$\Rightarrow (1 + m\beta) V_i = V_S$$

$$\Rightarrow V_i = \frac{V_S}{1 + m\beta}$$

$$\text{From fig } i_1 = \frac{V_i}{R_1} = \frac{V_S}{(1 + m\beta) R_1},$$

$$\text{WKT } z_{in} = \frac{V_S}{i_1} = \frac{V_S}{(1 + m\beta) R_1 z_{in}}$$

$$\rightarrow R_1 + R_3 = R_{\max} = \frac{0.1 V_{BIE}}{\beta B_{\max}}$$

$$\rightarrow R_1 + R_3 = R_2$$

$$\rightarrow R_1 \ll R_2$$

\rightarrow Choose $C_1 = 1000 \text{ pF}$
(To be much larger than
stage capacitance 3pF)

$$\rightarrow X_{C2} = R_3 \text{ at } f_1$$

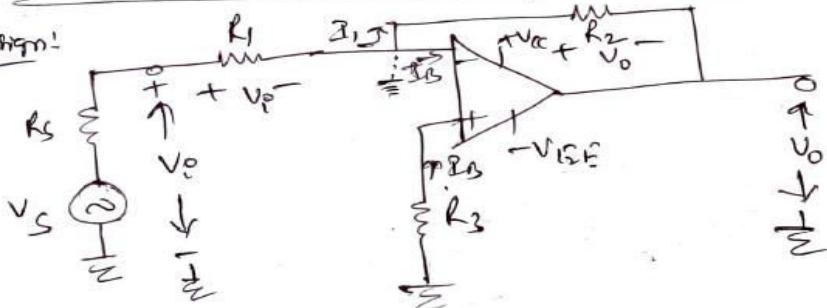
$$\therefore C_2 = \frac{1}{2\pi f_1 R_3}$$

$$\rightarrow X_{C3} = \frac{1}{10} R_2 \text{ at } f_1$$

$$\therefore C_3 = \frac{1}{2\pi f_1} \left(\frac{R_2}{10} \right)$$

Direct Coupled Inverting amplifiers

Design:



→ R_3 used to equalize the dc voltage drops due to $\text{I}_{\text{P}}/\text{I}_{\text{N}}$ bias currents.

$$\rightarrow R_3 \approx R_1 \| R_2$$

If R_1 is not very much larger than the source resistance, then $R_3 \approx (R_1 + R_S) \| R_2$

→ Start selecting potential divider current I_1 , to be much greater than the maximum level of $\text{I}_{\text{P}}/\text{I}_{\text{N}}$ bias current I_{B} . Then $R_1 = V_o / I_1$, $R_2 = V_{o0} / I_1$

→ For BJT opamp select target value resistors as 1MΩ. Then $R_1 = \frac{V_o}{I_1}$ & $R_2 = \frac{V_{o0}}{I_1}$

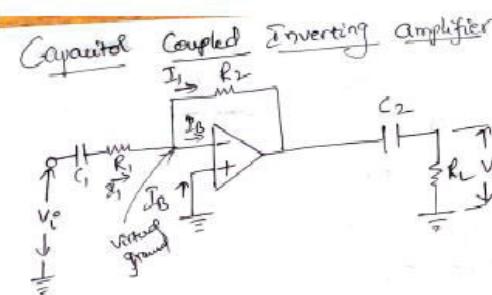
$$Z_{\text{in}} = R_1$$

Bjt inverting amplifier

$$Z_{\text{out}} = \frac{Z_0}{(1 + M\beta)} \quad \beta = \frac{R_1}{R_1 + R_2}$$

$$\therefore Z_{\text{out}} = \frac{Z_0}{1 + M R_1 / (R_1 + R_2)}$$

when $R_2 \gg R_1$,



→ This circuit does not need extra resistor to provide bias out path since current to the inverting terminal Since the non-inverting terminal is grounded. So the feedback provides the bias current to the inverting terminal.

→ To equalize the voltage drops at inverting & non-inverting terminals, a resistor can be connected between non-inverting terminal & ground. But it is not necessary since C_2 blocks the dc offset voltages.

Design:

$$1) I_1 = 100 \text{ } \mu\text{A}(\text{max})$$

$$2) R_1 = \frac{V_o}{I_1}$$

$$3) R_2 = \frac{V_{o0}}{I_1}$$

$$4) X_{C1} = \frac{R_1}{10} \text{ at } f_1 \quad \therefore C_1 = \frac{1}{2\pi f_1 (R_1)}$$

$$5) X_{C2} = R_L \text{ at } f_1 \quad \therefore C_2 = \frac{1}{2\pi f_1 R_L}$$

$$Z_{\text{out}} = \frac{Z_0}{1 + M/A_V}$$

① Design a J41 opamp, design a non inverting amplifier to have a voltage gain of 66. The signal amplitude is 15mV.

Soln: WKT $I_{B\max} = 500\text{nA}$
 Let $I_2 = 100I_{B\max} = 50\mu\text{A}$.
 $R_3 = \frac{V_i}{I_2} = \frac{15\text{mV}}{50\mu\text{A}} = 300\Omega$ (use a std 270Ω resistor).

$$V_o = A_v \times V_i = 66 \times 15\text{mV} = 990\text{mV}.$$

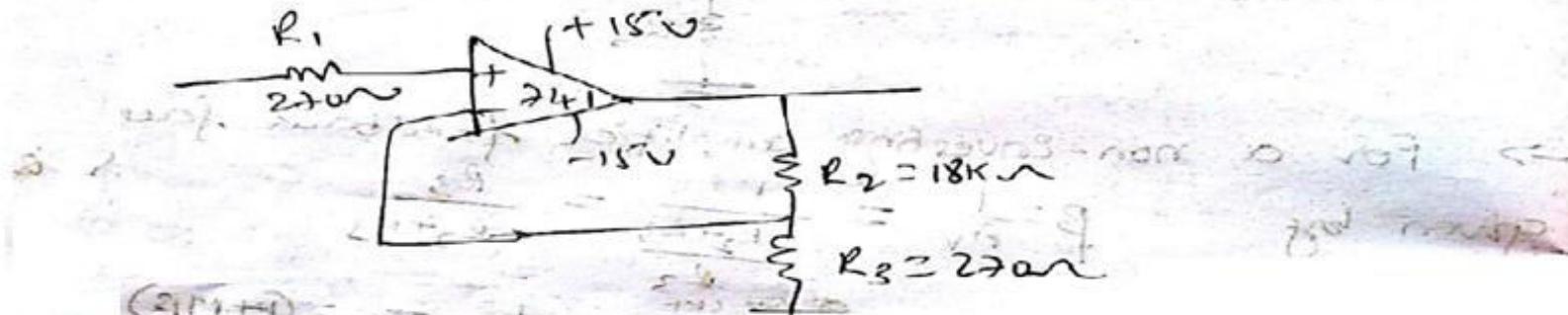
$$R_2 + R_3 = \frac{V_o}{I_2} = \frac{990\text{mV}}{55.6\mu\text{A}} = 17.8\text{k}\Omega$$

$$R_2 = (R_2 + R_3) - R_3 = 17.8\text{k} - 270\Omega = 17.53\text{k}\Omega$$

(use 18kΩ
18kΩ std
resistor)

$$\therefore R_1 \approx R_2 \| R_3 = 270\Omega \| 18\text{k}\Omega \approx 270\Omega$$

Supply voltage should be in range specified on the data sheet (ordinarily $\pm 9\text{V}$ to $\pm 18\text{V}$).



① Design an inverting amplifier using 741. The voltage gain is to be 50 & the output voltage amplitude is 2.5V

Given: $I_B = 50 \mu A$

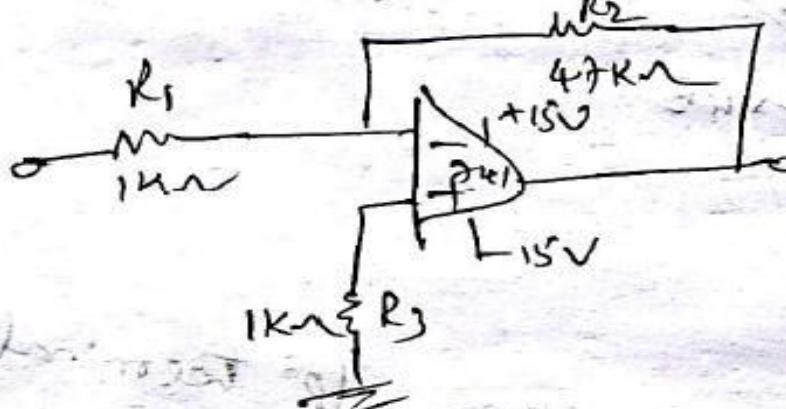
$$I_I = 100 \times I_B = 50 mA$$

$$V_I = \frac{V_o}{A_v} = \frac{2.5V}{50} = 50 mV$$

$$R_1 = \frac{V_I}{I_I} = \frac{50 mV}{50 mA} = 1 k\Omega \text{ (Set value)}$$

$$R_2 = \frac{V_o}{I_{B, \phi}} = \frac{2.5V}{50 \mu A} = 50 k\Omega \text{ (Set } 47 k\Omega \text{ due to negative feedback)}$$

$$R_3 = R_1 \parallel R_2 = 1k \parallel 50k = 1k\Omega$$



- Q) Design a Capacitor coupled voltage follower using
 i) a 741 op-amp &
 ii) a LF353 BiFET op-amp.
 for the lower cutoff freq 50Hz & $R_L = 3.9k\Omega$

Soln:- i) For 741 op-amp

$$a) R_1 = \frac{0.1 V_{B1\Sigma}}{I_B(\max)} = \frac{0.1 \times 0.7}{500\text{nA}} \approx 140k\Omega \quad (\text{use } 120k\Omega \text{ std value})$$

$$b) C_1 = \frac{1}{2\pi f_1 (R_1/10)} = \frac{1}{2\pi \times 50 \times (120k/10)} = 0.27\mu\text{F}$$

$$c) C_2 = \frac{1}{2\pi f_1 R_L} = 0.82\mu\text{F}$$

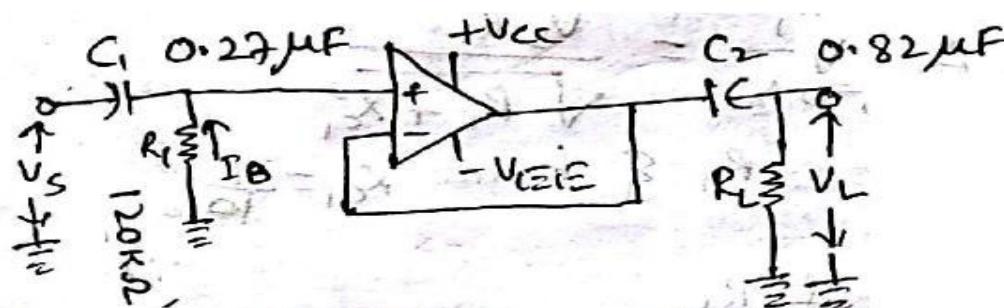
Choose supply voltages below $\pm 9\text{V}$ to $\pm 18\text{V}$.

ii) For LF353 BiFET

$$a) R_1(\max) = 1M\Omega$$

$$b) C_2 = \frac{1}{2\pi f_1 R_L} = 0.82\mu\text{F}$$

$$c) C_1 = \frac{1}{2\pi f_1 (R_1/10)} = 0.032\mu\text{F} \quad (\text{use } 0.033\mu\text{F} \text{ std value})$$



① Design a high Z_{in} Capacitor Coupled Voltage follower using an op-amp having lower cut-off freq of 50Hz & maximum i_{IP} bias current of 500nA. The load resistance is 3.3k Ω . If open loop gain is 10^5 , find ideal value of input impedance of the circuit.

Given: Given $f_L = 50\text{Hz}$, $R_{Bmax} = 500\text{nA}$, $R_L = 3.3\text{k}\Omega$, $A_{OL} = 10^5$, $Z_{in} = ?$

$$\textcircled{1} R_{max} = \frac{0.1VB_1}{I_{Bmax}} = \frac{0.1 \times 0.7}{500 \times 10^{-9}} = 140\text{k}\Omega$$

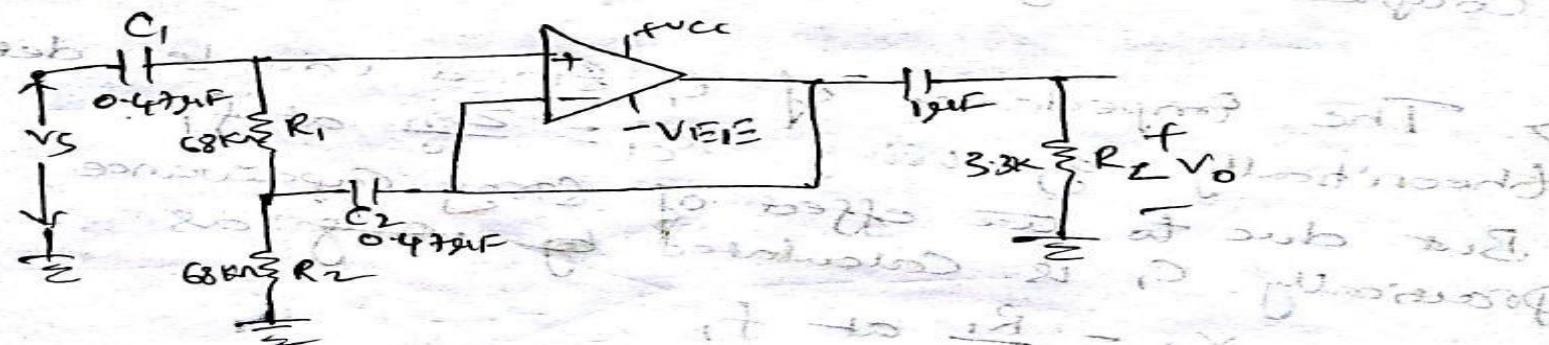
$$\textcircled{2} R_1 = R_2 = \frac{R_{max}}{2} = \frac{140}{2} = 70\text{k}\Omega \quad (\text{use } 68\text{k}\Omega)$$

$$\textcircled{3} C_2 = \frac{1}{2\pi f_L (R_2)} = \frac{1}{2\pi \times 50 \times \left(\frac{68}{10}\right)} = 0.468\mu\text{F} \quad (\text{use } 0.47\mu\text{F})$$

$$\textcircled{4} C_3 = \frac{1}{2\pi f_L R_L} = 0.964\mu\text{F} \quad (\text{use } 1\mu\text{F} \text{ std value})$$

$$\textcircled{5} C_1 = C_2 = 0.47\mu\text{F}$$

$$Z_{in} = R_1 (1 + A_{OL}) = 68 \times 10^3 \times 10^5 = 6800\text{M}\Omega$$



① A Capacitor Coupled non-inverting amplifier using opamp is to have $A_V = 100$ & $V_o = 5V$. The load resistance is $10k\Omega$ & lower cutoff freq is 100Hz. Design a suitable ckt.

Soln: Given $A_V = 100$, $V_o = 5V$, $R_L = 10k\Omega$, $\omega_{c1} = 100\text{Hz}$

$$\rightarrow R_{\text{max}} = \frac{0.1 V_B \bar{I}_2}{g_{\text{max}}} = \frac{0.1 \times 0.7}{500 \times 10^{-9}} = 140k\Omega$$

Choose $R_1 = 120k\Omega$

$$\rightarrow C_1 = \frac{1}{2\pi f_1 (R_1)} = 0.132\mu\text{F} \quad \text{choose } C_1 = 0.15\mu\text{F}$$

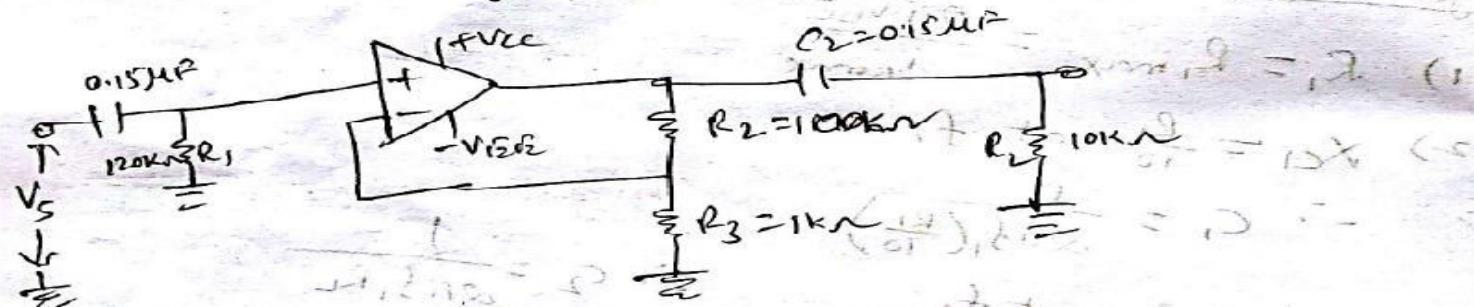
$$\rightarrow C_2 = \frac{1}{2\pi f_1 R_L} = 0.159\mu\text{F} \quad \text{choose } C_2 = 0.15\mu\text{F}$$

$$\rightarrow I_2 = 100 g_{\text{max}} = 100 \times 500 \times 10^{-9} = 50\mu\text{A}$$

$$\rightarrow R_3 = \frac{V_o}{I_2} = \frac{5V}{50 \times 10^{-6}} = 100k\Omega$$

$$R_3 = \frac{V_o}{I_2} = \frac{50 \times 10^3}{50 \times 10^{-6}} = 1k\Omega$$

$$\rightarrow R_2 = \left(\frac{V_o}{I_2} - R_3 \right) = 99k\Omega \quad \text{choose } R_2 = 100k\Omega$$



Q) A Capacitor Coupled Enveloping amplifier with input signal of 30mV & $R_L = 2.2k\Omega$ is to have $A_v = 150 \}$

$f_1 = 80Hz$. Design a suitable circuit for a) T-tube

b) BIFET

Ans: $V_i = 30mV \quad A_v = 150 \quad R_L = 2.2k \quad f_1 = 80Hz$

$$a) I_1 = 100 \text{ mA} = 100 \times 10^{-3} A$$

$$R_1 = \frac{V_i}{I_1} = 600\Omega \approx 560\Omega$$

$$A_v = \frac{R_2}{R_1}$$

$$R_2 = R_1 \times A_v = 560 \times 150 = 84k\Omega \approx 82k\Omega$$

$$X_{C1} = \frac{1}{f_1} R_L = 560$$

$$\therefore C_1 = 35.5 \mu F \approx 39 \mu F$$

$$X_{C2} = R_L = 2.2k\Omega$$

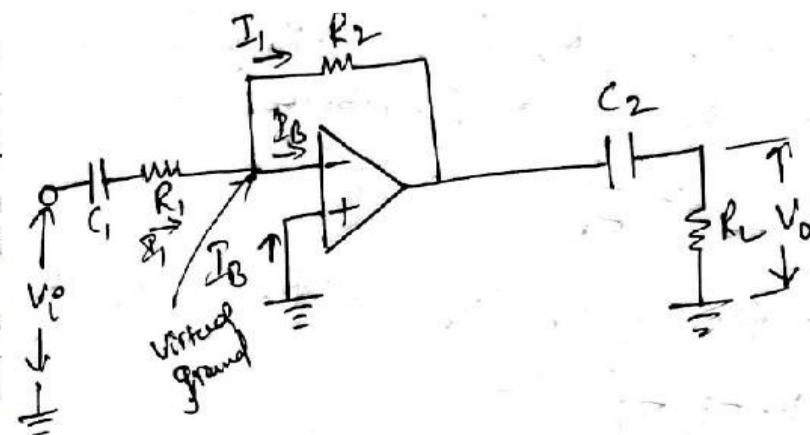
$$\therefore C_2 = 0.9 \mu F \approx 1 \mu F$$

b) choose $R_2 = 1M\Omega$

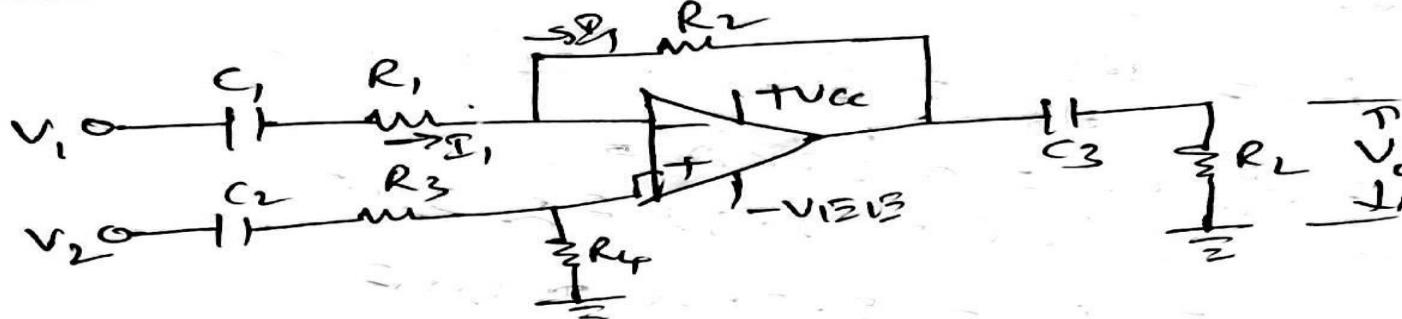
$$\therefore R_1 = \frac{R_2}{A_v} = 6.66k\Omega \approx 6.8k\Omega$$

$$X_{C1} = \frac{1}{f_1} R_1 = 0.68k\Omega \Rightarrow \\ \therefore C_1 = 2.9 \mu F \approx 3 \mu F$$

$$X_{C2} = R_L = 2.2k\Omega \approx 1 \mu F$$



Capacitor Coupled difference amplifier



This ckt amplifies the difference between two input voltages at one of the two input terminals of the op amp.

The opv voltage is given by $V_o = V_2 - V_1$

Design steps:

$$1) R_L = 100 \text{ k}\Omega$$

$$2) R_1 = \frac{V_o}{A_v}$$

$$3) R_3 = R_1$$

$$4) R_2 = R_4$$

$$5) R_2 = \frac{V_o}{A_v}$$

$$6) X_{C1} = \frac{R_1}{10} \text{ at } f, \quad \therefore C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$

$$7) X_{C2} = \frac{(R_3 + R_4)}{10} \text{ at } f,$$

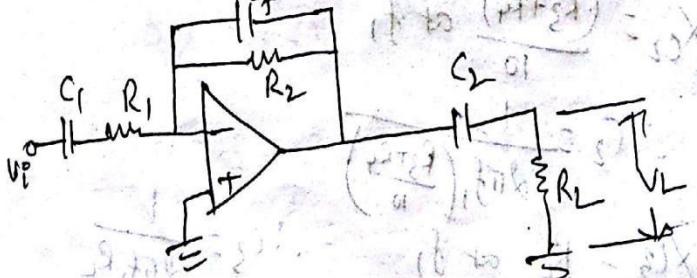
$$\therefore C_2 = \frac{1}{2\pi f_1 \left(\frac{(R_3 + R_4)}{10} \right)}$$

$$8) X_{C3} = R_L \text{ at } f, \quad \therefore C_3 = \frac{1}{2\pi f_1 R_L}$$

$$9) V_o = A_v (V_2 - V_1) \quad \text{where } A_v = \frac{R_2}{R_1}$$

Setting up the upper cut-off freq

The highest signal freq that can be processed by an opamp cut depends upon the op-amp selected. If very low freq signals are to be amplified & unwanted higher freq signals are to be excluded then the voltage gain of the cut must be made to fall off just above the highest desired signal freq. The usual method of doing this is to connect a FB capacitor from the opamp o/p to its i/p terminal as shown in fig.



For inverting amplifier, the voltage gain is

$$A_V = \frac{R_2 || C_f}{R_1} = \frac{R_2 C_f}{R_1 [R_2 + jX_{C_f}]} = \frac{R_2 C_f}{R_1 [\sqrt{R_2^2 + X_{C_f}^2}]}$$

when $R_2 = X_{C_f}$

$$A_V = \frac{R_2}{R_1} \times \frac{1}{\sqrt{2}} = 0.707 A_{Vmax}$$

Thus the upper cutoff freq for the cut can be set to the desired freq f_2 by making $X_{C_f} = 2\pi f_2$.

