

Module - 03

Op Amp as Non-Linear Circuit

Operational amplifiers are widely used in circuits in which the output is switched between the +ve and -ve saturation levels. Positive feed back is employed in these circuits.

$$\text{Generally, } +V_{\text{sat}} \approx (V_{cc} - 1V)$$

$$-V_{\text{sat}} \approx (-V_{EE} + 1V)$$

The 1V difference may change from op-amp to op-amp. For very small change in input voltage, the op-amp output switches from $+V_{\text{sat}}$ to $-V_{\text{sat}}$.

Input Voltage Range:

In linear applications, -ve feedback keeps the op-amp input terminal voltages closely equal. In switching applications, the dc voltage level at one input terminal is different from that at the other input terminal. The switching application normally employ +ve feedback to provide a substantial voltage difference between the two input terminals. This ensures that o/p is saturated at either a +ve or -ve voltage level. So, in switching applications, there is normally a differential voltage at the op-amp input terminal.

\therefore The minimum differential voltage required to produce output saturation is given by:-

$$V_{i(\text{diff})} \approx \frac{V_{cc}}{M_{\min}}, \text{ where } M_{\min} = \text{minimum open loop voltage gain of op amp.}$$

For 741 Op-amp, $M_{\min} \approx 50,000$

$$\text{If a } \pm 15V \text{ supply is used, } V_{i(\text{diff})} = \frac{\pm 15V}{50,000} = \pm 300 \mu V$$

Most op-amp can accept a differential input voltage equal to twice the supply voltage. The op-amp input stage may be damaged if this maximum is exceeded.

For eg: with a $\pm 15V$ supply, the maximum differential input should not exceed $30V$.

Op-amp as Comparator

A comparator is a circuit which compares a signal voltage applied at one i/p of an op-amp with a known reference voltage at the other end, and produces either a high or a low output voltage, depending on which i/p is higher.

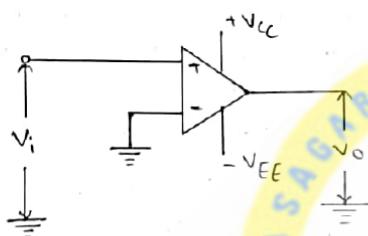
Zero Crossing Detector (ZCD)

The important application of comparator is zero crossing detector.

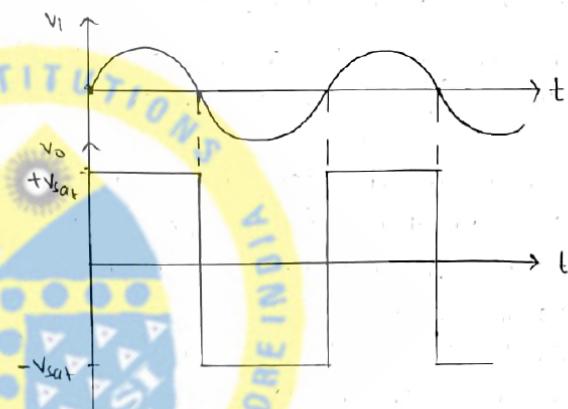
The types of ZCD are-

- * Non-inverting ZCD
- * Inverting ZCD
- * Capacitor coupled ZCD.

Non-Inverting ZCD:



- If $V_i > 0 \Rightarrow V_o = +V_{sat}$
- If $V_i < 0 \Rightarrow V_o = -V_{sat}$



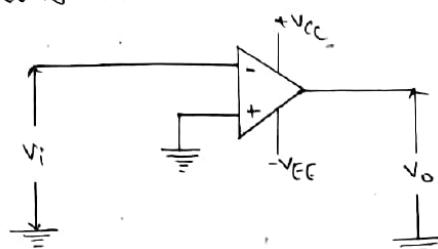
In a non-inverting zero crossing detector, the op-amp is used in open loop mode.

Inverting terminal is grounded and input is applied to the non-inverting terminal.

When the i/p is below ground level, the o/p is saturated at its -ve extreme. When the i/p goes above ground level by 300 mV, the o/p immediately switches to +ve saturation level.

Each time the i/p voltage crosses zero level, the o/p switches from one saturation level to the other.

Since, the o/p moves in a +ve direction when the i/p crosses zero from -ve to +ve, circuit is said to be non-inverting ZCD. Regardless of the i/p waveshape, the o/p is always a rectangular wave form.

Inverting ZCD

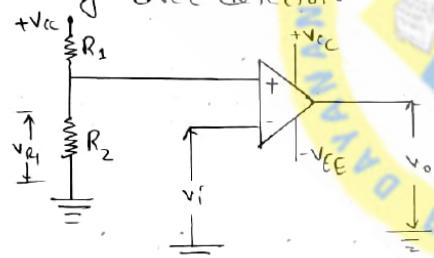
- If $V_i > 0 \Rightarrow V_o = -V_{sat}$
- If $V_i < 0 \Rightarrow V_o = +V_{sat}$

In inverting ZCD, the i/p. is applied to the inverting s/p terminal while the non-inverting terminal is grounded.

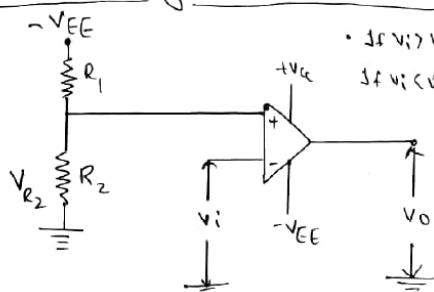
When the i/p voltage crosses zero line going in +ve direction, the o/p goes -ve and vice-versa.
This circuit is called as inverter.

Voltage level detector:

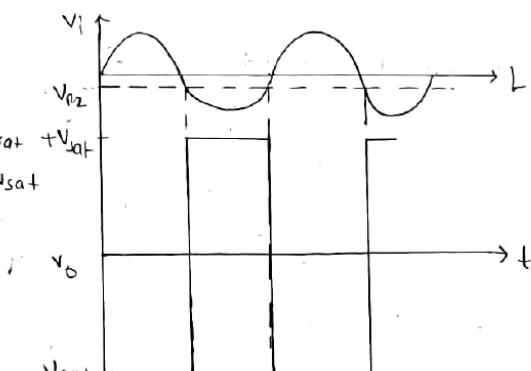
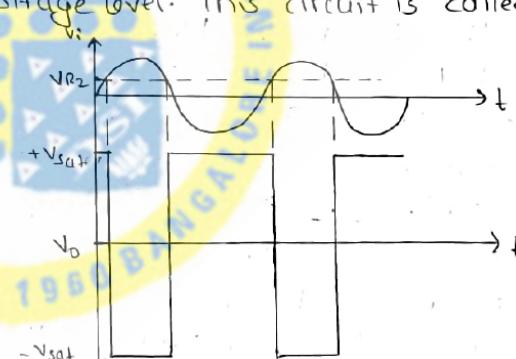
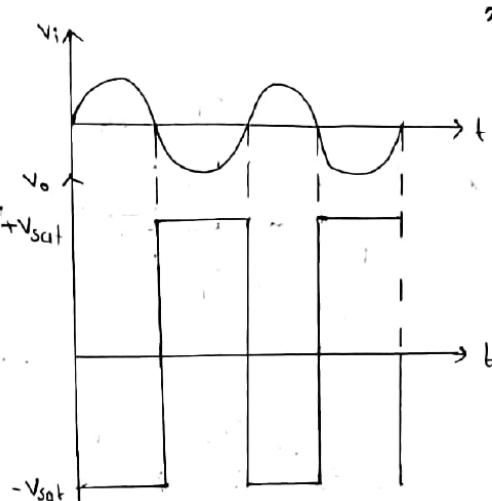
Instead of being biased to ground level, the non-inverting i/p terminal of the op-amp could be biased to a +ve or -ve dc level as shown in fig. The circuit o/p changes when the i/p arrives at the bias voltage level. This circuit is called a voltage level detector.

+ve voltage level detector

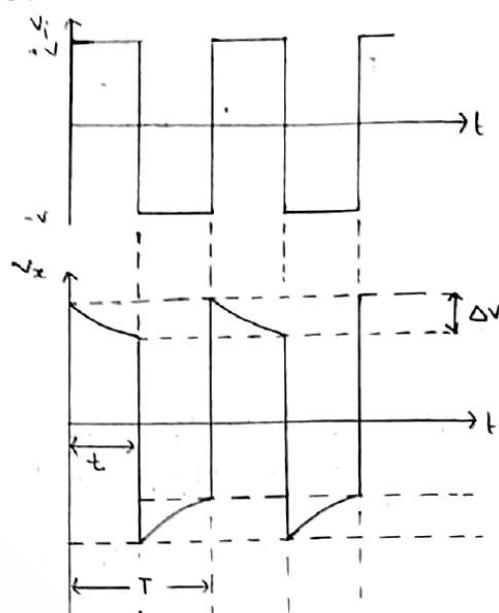
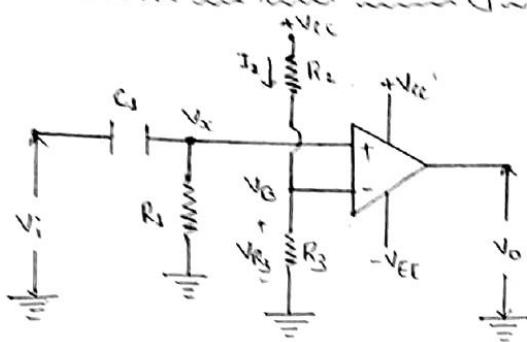
- If $V_i < V_{R2} \Rightarrow V_o = +V_{sat}$
- $V_i > V_{R2} \Rightarrow V_o = -V_{sat}$

-ve voltage level detector

- If $V_i > V_{R1} \Rightarrow V_o = -V_{sat}$
- If $V_i < V_{R1} \Rightarrow V_o = +V_{sat}$



Capacitor coupled crossing detector:



The capacitor coupled crossing detector has the op-amp non-inv. input terminal connected to ground via resistor R_1 , to provide a dc bias current path to op-amp. Also, the inverting terminal is biased to a dc voltage level $-V_{sat}$ slightly above ground. This is required to ensure that the output is saturated in a -ve direction when no i/p is present.

The output switches to $+V_{sat}$ when the capacitor coupled signal drives the non inverting terminal above V_B and falls back to $-V_{sat}$ when the i/p drops below V_B .

Design:

* To design R_2 and R_3 ,

$$I_2 = 100 I_{B\max}$$

$$V_B = 0.1V \quad [200]$$

$$V_{R2} = V_{CC} - V_B \quad \text{and} \quad V_{R3} = V_B$$

$$R_2 = V_{R2} / I_2$$

$$R_3 = V_{R3} / I_2$$

$$* R_1 = \frac{0.1 V_{BE}}{I_{B\max}}$$

* To find C_1 :

- For sinusoidal input, to eliminate phase shift error which may make the circuit unstable, X_{C1} must be smaller than R_1 at min. signal frequency f_1 .

$$\therefore X_{C1} = \frac{1}{2\pi f_1 R_1} \Rightarrow C_1 = \frac{1}{2\pi f_1 (R_1/2\pi)}$$

- When a square wave is applied as an i/p to the capacitor coupled crossing detector, the waveform can develop tilt at op-amp input terminal as shown.

As long as the o/p is constant at saturation levels, tilt is insignificant.

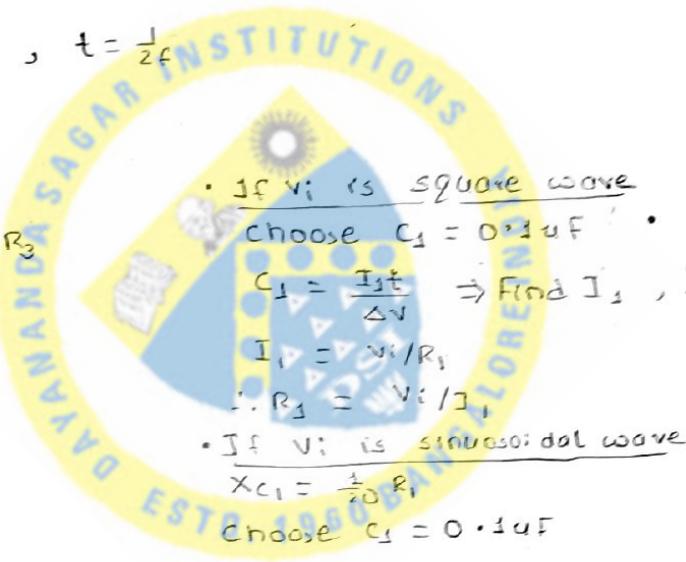
In such case, to determine C_1 , first time 't' is measured for acceptable tilt in V_x :

$$I_1 = \frac{V_i}{R_1}$$

$$C_1 = \frac{I_1 t}{\Delta V}, \quad t = \frac{1}{2f}$$

For BIFET:

- Let, $R_2 = 1\text{ M}\Omega$
 - Find I_2 & calculate R_3
- $$R_2 = \frac{V_{C2} - V_B}{I_2} = \frac{V_C - V_B}{I_2}$$
- $$\therefore I_2 = \frac{V_C - V_B}{R_2}$$
- Find R_3 , $R_3 = \frac{V_B}{I_2}$



- Q. A capacitor coupled zero crossing detector is to handle 1 KHz square wave i/p with a peak to peak amplitude of 6V. Design a suitable circuit using a 741 OP amp with a $\pm 12\text{V}$ supply.

Sol: Draw circuit diagram and waveform

$$\begin{aligned} \text{Let, } I_2 &= 100 I_{B\max} \\ &= 100 \times 500\text{nA} \\ &= 50\text{ uA}. \end{aligned}$$

$$\text{Let, } V_B = 0.1V$$

$$V_{R2} = V_{CC} - V_B = 12V - 0.1V = 11.9V$$

$$\bullet R_2 = \frac{V_{R2}}{I_2} = \frac{11.9}{50 \times 10^{-6}} = 238 k\Omega \approx 220 k\Omega$$

$$V_{R3} = V_B = 0.1V$$

$$\bullet R_3 = \frac{V_{R3}}{I_2} = \frac{0.1}{50 \times 10^{-6}} = 2k\Omega \approx 1.8k\Omega$$

$$\bullet R_1 = \frac{0.1V_{BE}}{I_{B\max}} = \frac{0.1 \times 0.7}{500 \times 10^{-9}} = 140 k\Omega \approx 120 k\Omega$$

$$V_{i(\text{peak})} = \frac{6V}{2} = 3V$$

Square wave:

$$I_1 = \frac{V_i}{R_1} = \frac{3}{120 \times 10^3} = 25 \mu A$$

$$t = \frac{1}{2f} = \frac{1}{2 \times 1 \times 10^3} = 500 \mu s$$

$$C_1 = \frac{I_1 t}{\Delta V} = \frac{25 \times 10^{-6} \times 500 \times 10^{-6}}{1} \approx 0.0125 \mu F \approx 0.015 \mu F$$

Q) A capacitor coupled ZCD is to provide an o/p voltage approx. $\pm 17V$ when a 3kHz , with $\pm 2V$ square wave i/p is applied. Design a suitable detector using bipolar op amp.

Soln: $+V_{sat} = +17V, f = 3\text{kHz}$

$$t = \frac{1}{2f} = \frac{1}{2 \times 3 \times 10^3} = 0.167 \text{ ms}$$

$$R_1 = \frac{0.1V_{BE}}{I_{B\max}} = \frac{0.1 \times 0.7}{500 \times 10^{-9}} = 140 k\Omega \approx 120 k\Omega$$

$$I_2 = 100 I_{B\max} = 50 \mu A$$

$$R_2 = \frac{V_{CC} - V_B}{I_2} = \frac{18 - 0.1}{50 \times 10^{-6}} = 358 k\Omega \approx 330 k\Omega$$

$$R_3 = \frac{V_{R3}}{I_2} = \frac{V_B}{I_2} = \frac{0.1}{50 \times 10^{-6}} = 2k\Omega \approx 1.8k\Omega$$

sg. wave:

$$C_1 = \frac{I_1 \Delta t}{\Delta V}, I_1 = \frac{V_i}{R_1} = \frac{2}{120 \times 10^3} = 16.67 \mu A$$

$$= 2734.77 \mu F \approx 3000 \mu F$$

BIFET: $R_2 = 1M\Omega$

$$I_2 = \frac{V_{R2}}{R_2} = \frac{(V_{CC} - V_B)/R_2}{10^6} = (18 - 0.1)/10^6 = 1.79 \times 10^{-6} A$$

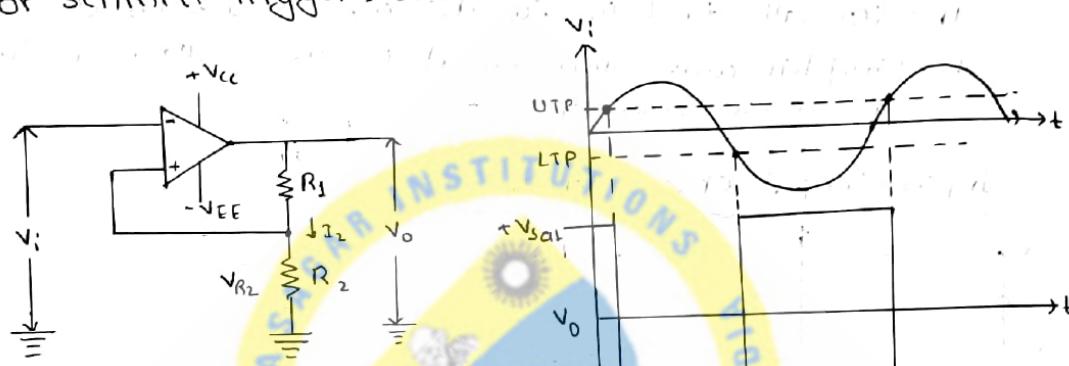
$$R_3 = \frac{V_{R3}}{I_2} = \frac{V_B}{I_2} = 5.5 k\Omega \approx 5.6 k\Omega$$

$$\text{choose, } C_1 = 0.1 \mu F, K_C = K_B, R_1 = 3.3 k\Omega$$

Inverting schmitt Trigger circuit

4.

In a basic comparator, a feedback is not used and the Op-Amp is used in the open loop mode. As open loop gain of opamp is large, very small noise voltages can cause triggering of the comparator, to change its state. This may cause lot of problems in the applications of comparators as ZCD. Such unwanted noises cause the output to jump between high and low states. The comparator circuit used to avoid such unwanted triggering is called Regenerative comparator or schmitt trigger, which basically uses +ve feedback.



$$\bullet V_{R2} = \frac{V_o}{(R_1 + R_2)} \times R_2$$

$$\bullet \text{If } V_i < V_{R2} \Rightarrow V_o = +Vs_{at}$$

$$V_{R2} = \frac{+Vs_{at}}{R_1 + R_2} \times R_2 \rightarrow \text{UTP (Upper triggering point)}$$

$$\bullet \text{If } V_i < V_{R2} \Rightarrow V_o = -Vs_{at}$$

$$V_{R2} = \frac{-Vs_{at}}{R_1 + R_2} \times R_2 \rightarrow \text{LTP (Lower triggering point)}$$

The basic circuit of inverting schmitt trigger is shown above. The i/p is applied to the inverting terminal and +ve feedback is provided.

The voltage at non inverting i/p is $V_{R2} = \frac{V_o}{R_1 + R_2} \times R_2$

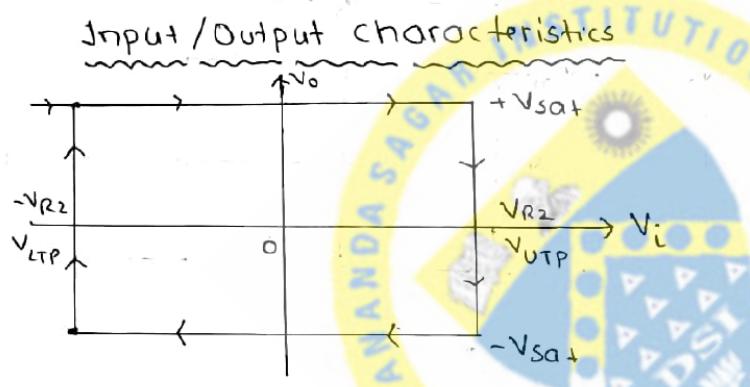
when the o/p voltage is saturated in +ve direction at $+Vs_{at}$, V_{R2} is a positive quantity. When the o/p is at $-Vs_{at}$, V_{R2} is negative.

The o/p switch from the +ve saturation level to the -ve saturation level only when the inverting i/p terminal is raised above the voltage at non-inverting input terminal (V_{R2}).

$+V_{R2}$ is for +ve saturation when $V_o = +V_{sat}$ and is called UTP (Upper Threshold point)

$-V_{R2}$ is for -ve saturation when $V_o = -V_{sat}$ and is called LTP (Lower Threshold point)

The o/p switches from +ve to -ve when the i/p voltage reaches UTP and from -ve to +ve when the i/p falls to LTP. So, the o/p is always a rectangular waveform. So, it is also called sine to square wave converter.



Typical I/O characteristics of an op-amp inverting schmitt trigger is shown above.

Initially with o/p at $+V_{sat}$ and i/p at zero, when V_i is raised to UTP, the o/p switches from $+V_{sat}$ to $-V_{sat}$.

Any further increase in V_i above UTP maintains the o/p at $-V_{sat}$. When the i/p is being reduced from UTP to the LTP, the o/p remains at $-V_{sat}$.

When V_i equals the LTP, the o/p rapidly switches from $-V_{sat}$ to $+V_{sat}$. Now any further decrease in V_i below the LTP, maintains the o/p voltage at $+V_{sat}$.

The voltage difference between the upper and lower trigger points is referred to as hysteresis. 5.

$$V_H = UTP - LTP$$

$$= \frac{+V_{sat}}{R_1 + R_2} \times R_2 - \left[\frac{-V_{sat}}{R_1 + R_2} \times R_2 \right]$$

$$\text{When } V_i < LTP, V_o = +V_{sat}$$

$$\text{When } V_i > UTP, V_o = -V_{sat}$$

$$\left. \begin{array}{l} V_i < UTP \Rightarrow V_o = +V_{sat} \\ V_i > UTP \Rightarrow V_o = -V_{sat} \\ V_i < LTP \Rightarrow V_o = -V_{sat} \\ V_i > LTP \Rightarrow V_o = +V_{sat} \end{array} \right\}$$

$LTP < V_i < UTP \Rightarrow V_o = \text{Previous state.}$

Design steps:

Let, the current through R_1 and R_2 is I_2 .

- $I_2 = 100 I_{B\max}$

- $R_2 = \frac{\text{Triggering voltage}}{I_2}$

- $R_1 = \frac{V_o - \text{Triggering voltage}}{I_2}$

BIFET:

- choose $R_1 = 1 M\Omega$

- Find I_2

$$I_2 = \frac{V_o - \text{Triggering voltage}}{R_1}$$

- ⇒ Find R_2

$$R_2 = \frac{\text{Triggering voltage}}{I_2}$$

- Q. Using a 741 op amp with a supply of $\pm 12V$, design an inverting schmitt trigger circuit to have a trigger point of $\pm 2V$

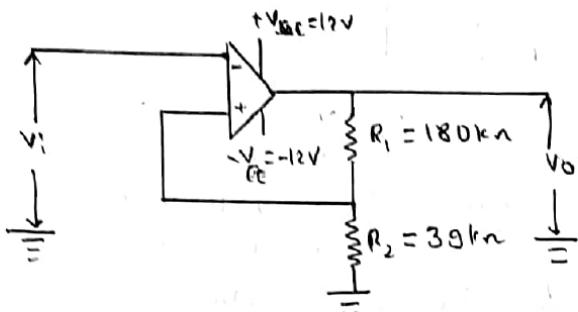
Soln: Let, $I_2 = 100 I_{B\max}$
 $\approx 50 \mu A$

$$+V_{R2} = UTP = 2V$$

$$R_2 = \frac{V_{R2}}{I_2} = \frac{2V}{50 \mu A} = 40 k\Omega \approx 39 k\Omega$$

$$V_{R1} = V_{O_{SA1}} - V_{R2} = (12 - 1) - 2 = 9V$$

$$R_1 = \frac{V_{R1}}{I_2} = 180 \text{ k}\Omega \approx 180 \text{ k}\Omega$$



BIFET

$$R_1 = 1 \text{ M}\Omega$$

$$I_2 = \frac{V_o - \text{Triggering voltage}}{R_1} = \frac{11 - 2}{1 \times 10^6} = 9 \mu\text{A}$$

$$R_2 = \frac{\text{Triggering voltage}}{I_2} = \frac{2}{9 \times 10^{-6}} = 222 \text{ k}\Omega \approx 220 \text{ k}\Omega$$

Q. An inverting schmitt trigger is to be designed with triggering voltage $\pm 0.5V$ and to produce the O/P = $\pm 11V$. Use 741 Op Amp.

Soln: $I_2 = 100 I_{B\max} = 50 \mu\text{A}$

$$R_2 = \frac{\text{Triggering voltage}}{I_2} = \frac{0.5}{50 \times 10^{-6}} = 10 \text{ k}\Omega$$

$$R_1 = \frac{11 - 0.5}{50 \times 10^{-6}} = 210 \text{ k}\Omega \approx 180 \text{ k}\Omega$$

Q. Design an inv. schmitt trigger to have triggering points of $\pm 4V$ with a supply of $\pm 15V$

Soln: $I_2 = 100 I_{B\max} = 50 \mu\text{A}$

$$R_2 = \frac{4}{50 \times 10^{-6}} = 80 \text{ k}\Omega$$

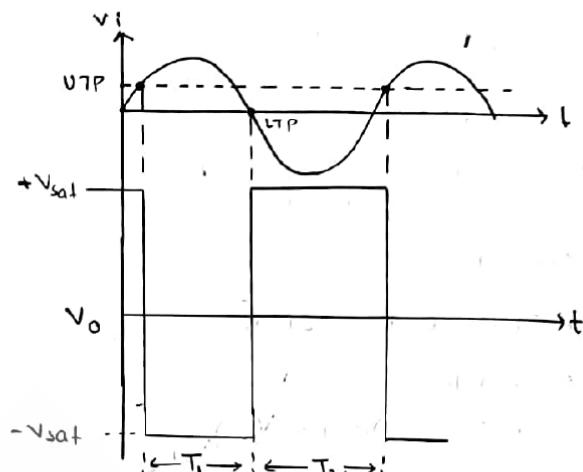
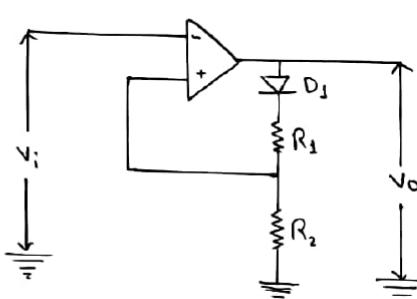
$$R_1 = \frac{14 - 4}{50 \times 10^{-6}} = 200 \text{ k}\Omega$$

Adjusting Triggering points

.6.

Inverting schmitt trigger circuits with different UTP & LTPAsymmetrical schmitt Trigger

a)



- If $V_i < V_{R2}$, $V_o = +V_{sat}$
D₁ is F.B., $V_{R2} = U_{TP}$
- $V_{R2} = U_{TP} = \left(\frac{+V_{sat} - V_F}{R_1 + R_2} \right) \times R_2$
 $V_F \rightarrow$ Diode voltage.
- If $V_i > V_{R2}$, $V_o = -V_{sat}$
D₁ is R.B., $V_{R2} = 0$ (LTP)

In the above circuit, UTP is combined with a zero voltage LTP. When the o/p is $+V_p$, D₁ is forward-biased and UTP is the drop across R₂. When the o/p is $-V_p$, D₁ is reverse biased, only the op-amp input bias current flows in R₂ and the op-amp non-inverting i/p terminal is held close to ground level. The o/p will go $+V_p$ once again when the i/p voltage is reduced below ground level.

The diode D₁ must be selected to have a maximum reverse voltage greater than the circuit supply voltage. Its maximum reverse recovery time (trr) should be much smaller than the min pulse width of the i/p signal.

$$\therefore trr \leq \frac{\text{min. pulse width}}{10}$$

Design:

741:

Let, $I_2 = 500 \mu A$ (To handle diode forward current, $I_2 = 500 \mu A$)

$$\bullet R_2 = \frac{U_{TP}}{I_2}$$

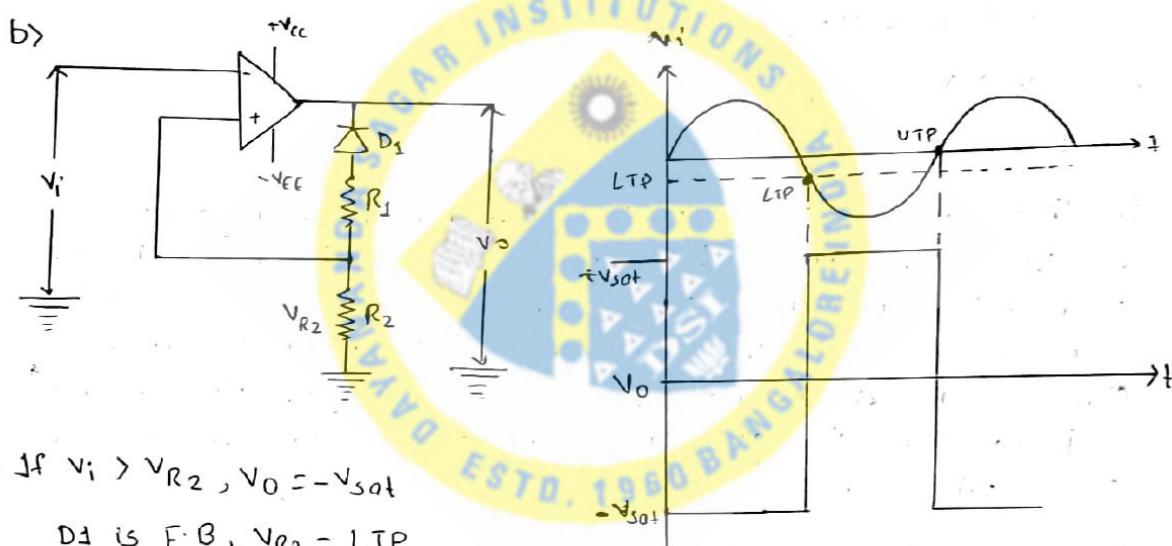
• To find R_1 ,

$$U_{TP} = \left(\frac{+V_{sat} - V_F}{R_1 + R_2} \right) R_2$$

BIFET:• choose $R_1 = 1M\Omega$ • Find R_2 .

$$U_{TP} = \frac{(+V_{sat} - V_F)}{R_1 + R_2} \times R_2$$

——— x —— x —— x —— x —— x —— x —— x ——

• If $V_i > V_{R2}$, $V_o = -V_{sat}$ D1 is F.B., $V_{R2} = LTP$

$$-V_{R2} = \frac{(-V_{sat} + V_F)}{R_1 + R_2} \times R_2$$

Design!

$$I_2 = 500 \mu A$$

• If $V_i < V_{R2}$, $V_o = +V_{sat}$ D1 is R.B., $V_{R2} = 0$

$$R_2 = \frac{LTP}{I_2}$$

Find R_1

Q An inverting schmitt trigger is to have UTP = 1V and LTP = 0V. Design a suitable circuit using bipolar opamp with supply voltage of ±15V.

Soln: $I_2 = 500 \mu A$

$$R_2 = \frac{UTP}{I_2} = \frac{1}{500 \times 10^{-6}} = 2 k\Omega \approx 1.8 k\Omega$$

To find R_1 ,

$$UTP = \frac{(14 - 0.7)}{R_1 + R_2} \times R_2$$

$$\Rightarrow 1 = \frac{(14 - 0.7)}{(R_1 + 1.8 \times 10^3)} \times 1.8 \times 10^3$$

$$\Rightarrow R_1 = (14 - 0.7) \times 1.8 \times 10^3 - 1.8 \times 10^3 \\ = 22.14 k\Omega$$

Q. Design a suitable circuit with UTP = 0V and LTP = 2.5V with power supply ±18V. Use 741 Op Amp.

Soln: $I_2 = 500 \mu A$

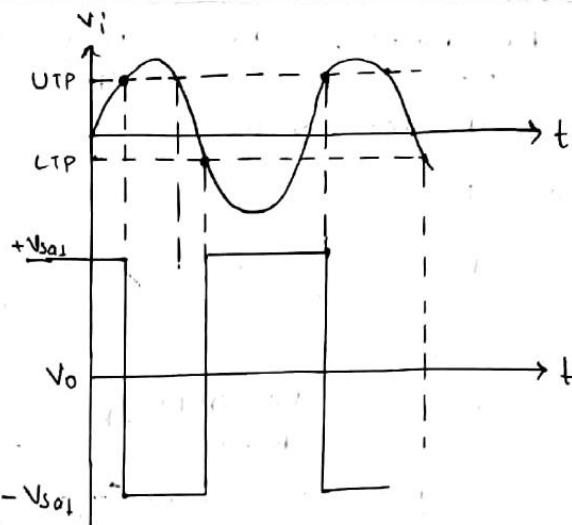
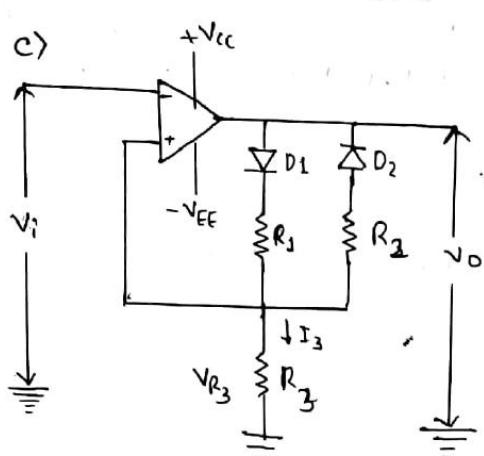
$$R_2 = \frac{LTP}{I_2} = \frac{2.5}{500 \times 10^{-6}} = 5 k\Omega \approx 4.7 k\Omega$$

To find R_1 ,

$$LTP = \left(\frac{-V_{sat} + V_f}{R_1 + R_2} \right) \times R_2$$

$$\Rightarrow -2.5 = \frac{(-17 + 0.7)}{R_1 + 4.7 \times 10^3} \times 4.7 \times 10^3$$

$$\Rightarrow R_1 = 25.84 k\Omega \\ \approx 22 k\Omega$$



The above circuit has two different level trigger points.

- If $V_i < V_{R3} \Rightarrow V_0 = +V_{sat}$

D1 is F-B and D2 is R-B

$$V_{R3} = UTP = \frac{(+V_{sat} - V_F)}{R_1 + R_3} \times R_3, \text{ where } V_F \text{ is forward voltage drop of D1}$$

- If $V_i > V_{R3} \Rightarrow V_0 = -V_{sat}$

D1 is R-B and D2 is F-B

$$V_{R3} = LTP = \frac{(-V_{sat} + V_F)}{R_2 + R_3} \times R_3$$

Design: Choose $I_3 = 500 \mu A$

$$R_3 = \frac{UTP}{I_3}$$

$$\text{To find } R_1 : UTP = \frac{(+V_{sat} - V_F)}{R_1 + R_3} \times R_3$$

$$\text{To find } R_2 : LTP = \frac{(-V_{sat} + V_F)}{R_2 + R_3} \times R_3$$

- Design an Inv. schmitt trigger with $UTP = 1.5V$ & $LTP = -3V$, with $\pm 18V$ supply using bipolar op amp.

Soln: $I_3 = 500 \mu A$

$$R_3 = \frac{1.5}{500 \times 10^{-6}} = 3k\Omega \approx 2.7 k\Omega$$

$$UTP = \left(\frac{+V_{sat} - V_F}{R_1 + R_3} \right) R_3 \Rightarrow R_1 = 26.69 k\Omega \approx 27 k\Omega$$

$$LTP = \left(\frac{-V_{sat} + V_F}{R_2 + R_3} \right) R_3 \Rightarrow R_2 = 13.97 k\Omega \approx 12 k\Omega$$

Multivibrators using Op Amp

8.

Multivibrators are regenerative circuits that are used commonly in timing applications.

There are two types:-

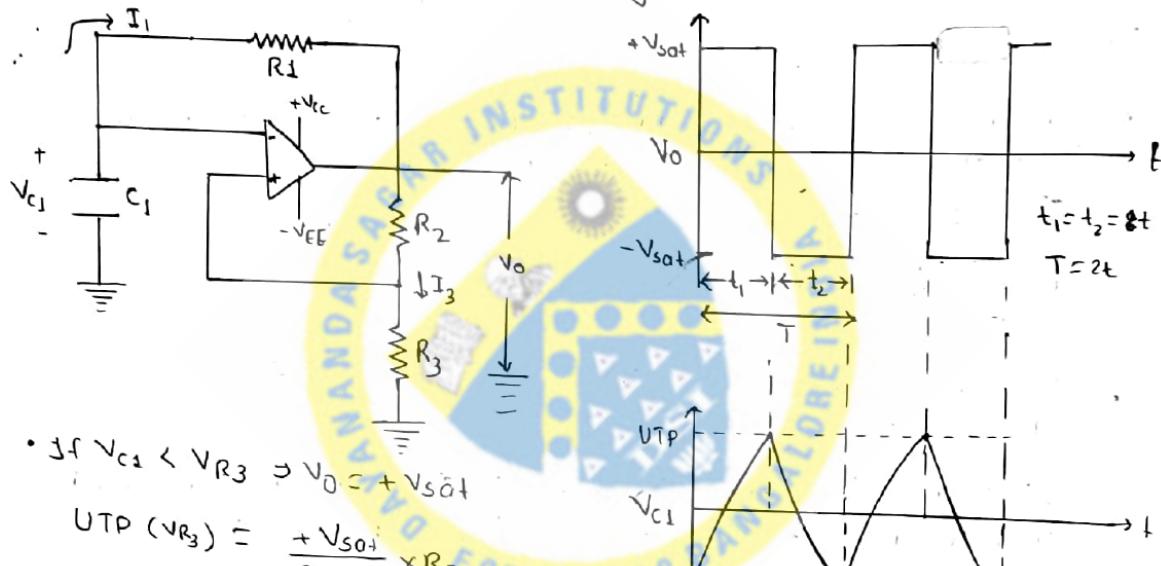
- i) astable multivibrator
- ii) monostable multivibrator

i) Astable Multivibrator using Op Amp

An astable mv is a circuit that is continuously switching its o/p voltage between high and low levels.

It has no stable state.

It is also called a free running multivibrator



- If $V_{C1} < V_{R3} \Rightarrow V_O = +V_{SAT}$

$$UTP (V_{R3}) = \frac{+V_{SAT}}{R_2 + R_3} \times R_3$$

- If $V_{C1} > V_{R3} \Rightarrow V_O = -V_{SAT}$

$$LTP (-V_{R3}) = \frac{-V_{SAT}}{R_2 + R_3} \times R_3$$

The circuit diagram of Amv using schmitt trigger is shown in figure. The op-amp with resistors R₂ and R₃ forms an inverting schmitt trigger circuit. The o/p voltage to schmitt trigger is the voltage across capacitor C₁ which is charged from the op-amp o/p via resistor R₃.

When the power is turned ON, the output automatically swing either to $+V_{sat}$ or to $-V_{sat}$. Since, these are the only stable states allowed by the schmitt trigger.

Let, the circuit O/p be at +ve saturation level, current flows into the capacitor, charging it until the V_{ci} reaches the UTP of the schmitt trigger.

The O/p then rapidly switches to the -ve saturation level.

Now, capacitor starts discharging via R_1 and capacitor charges with opposite polarity. This continues until V_{ci} reaches LTP, then the O/p rapidly switches back to +ve saturation level, and cycle starts again.

Design:

- The minimum current through R_1 is selected to be much larger than the op-amp input bias current
 $I_1 = 100 I_{B\max}$
- $R_1 = \frac{|V_{oi} - UTP|}{I_1}$
- Once R_1 is determined, C_1 can be calculated from the capacitor charging equation.
 If schmitt trigger UTP and LTP are selected to be much smaller than op-amp o/p voltage, the voltage across R_1 will not change much.
 Consequently, the capacitor charging current (I_1) can be a constant & from which C_1 can be obtained.

$$C_1 = \frac{I_1 \times t}{\Delta V}, \quad \Delta V = UTP - LTP = 1V \quad UTP = +0.5V \quad LTP = -0.5V$$

- Let, $I_3 = 100 I_{B\max}$

- $R_3 = \frac{UTP}{I_3}$

- $R_2 = \frac{|V_{oi} - UTP|}{I_3}$

BIFET

Q.

The capacitance of C_1 should be first selected to be much larger than stray capacitance.

- Choose $C_1 = 0.1 \mu F$.

- Find I_1 , $I_1 = \frac{C_1 \Delta V}{t_1}$

- $R_1 = \frac{|V_{O1} - UTP|}{I_1}$

- Choose $R_2 = 1M\Omega$

- Find I_3 , $I_3 = \frac{|V_{O1} - UTP|}{R_2}$

- $R_3 = \frac{UTP}{I_3}$

Q. Using a BIFET opamp, design an Avm to have a $\pm 9V$ o/p with frequency of 1 kHz.

Soln: For $V_o = \pm 9V$

$$V_{CC} = \pm V_o + 1 = \pm 9V + 1 = \pm 10V$$

Select, $UTP = LTP = 0.5V$

Let, $R_2 = 1M\Omega$

$$I_3 = \frac{|V_{O1} - UTP|}{R_2} = \frac{9V - 0.5V}{1M\Omega} = 8.5 \mu A$$

$$R_3 = \frac{UTP}{I_3} = \frac{0.5V}{8.5 \mu A} = 59k\Omega \approx 56k\Omega$$

Let, $C_1 = 0.1 \mu F$

$$t_1 = \frac{1}{2f} = \frac{1}{2 \times 10^3} = 500 \mu s$$

$$I_1 = \frac{C_1 \Delta V}{t_1} = 200 \mu A$$

$$R_1 = \frac{|V_{O1} - UTP|}{I_1} = 47.5k\Omega \approx 39k\Omega$$

Q. Design an OpAmp Amv to have an o/p frequency of 400 Hz
Use a 741 OpAmp with a supply of $\pm 18V$.

$$\text{SOLM: } f = 400 \text{ Hz}, T = 2.5 \text{ ms}, t_1 = 1.25 \text{ ms}$$

$$I_1 = 180 I_{B\max} = 50 \mu\text{A}$$

$$R_1 = \frac{17 - 0.5}{50 \times 10^{-6}} = 330 \text{ k}\Omega$$

$$C_1 = \frac{I_1 \cdot t}{\Delta V} = \frac{50 \times 10^{-6} \times 1.25 \times 10^3}{1} = 62.5 \text{ nF} \approx 0.06 \mu\text{F}$$

$$I_3 = 180 I_{B\max} = 50 \mu\text{A}$$

$$R_3 = \frac{0.5}{50 \times 10^{-6}} = 10 \text{ k}\Omega$$

$$R_2 = \frac{17 - 0.5}{50 \times 10^{-6}} = 330 \text{ k}\Omega$$

BIFET

$$R_2 = 1 \text{ M}\Omega$$

$$I_3 = \frac{180(1 - UTP)}{R_2} = \frac{17 - 0.5}{1 \times 10^6} = 16.5 \mu\text{A}$$

$$R_3 = \frac{UTP}{I_3} = \frac{0.5}{16.5 \times 10^{-6}} = 30.3 \text{ k}\Omega$$

$$C_1 = 0.1 \mu\text{F}$$

$$t = \frac{1}{2f} = \frac{1}{2 \times 400} = \frac{1}{800} = 1.25 \text{ ms}$$

$$I_1 = \frac{C_1 \Delta V}{t} = \frac{0.1 \times 10^{-6}}{1.25 \times 10^{-3}} = 80 \mu\text{A}$$

$$R_1 = \frac{V_o - UTP}{I_1} = \frac{17 - 0.5}{80 \times 10^{-6}} = 206.25 \text{ k}\Omega$$

Q. Design Amv using 741 with $\pm 15V$ supply with $t_{on} = t_{off} = 1 \text{ ms}$.

$$\text{SOLM: } I_1 = 180 I_{B\max} = 50 \mu\text{A}$$

$$R_1 = \frac{14 - 0.5}{50 \times 10^{-6}} = 270 \text{ k}\Omega$$

$$C_1 = \frac{I_1 \cdot t}{\Delta V} = 50 \times 10^{-6} \times 10^3 = 0.05 \mu\text{F}$$

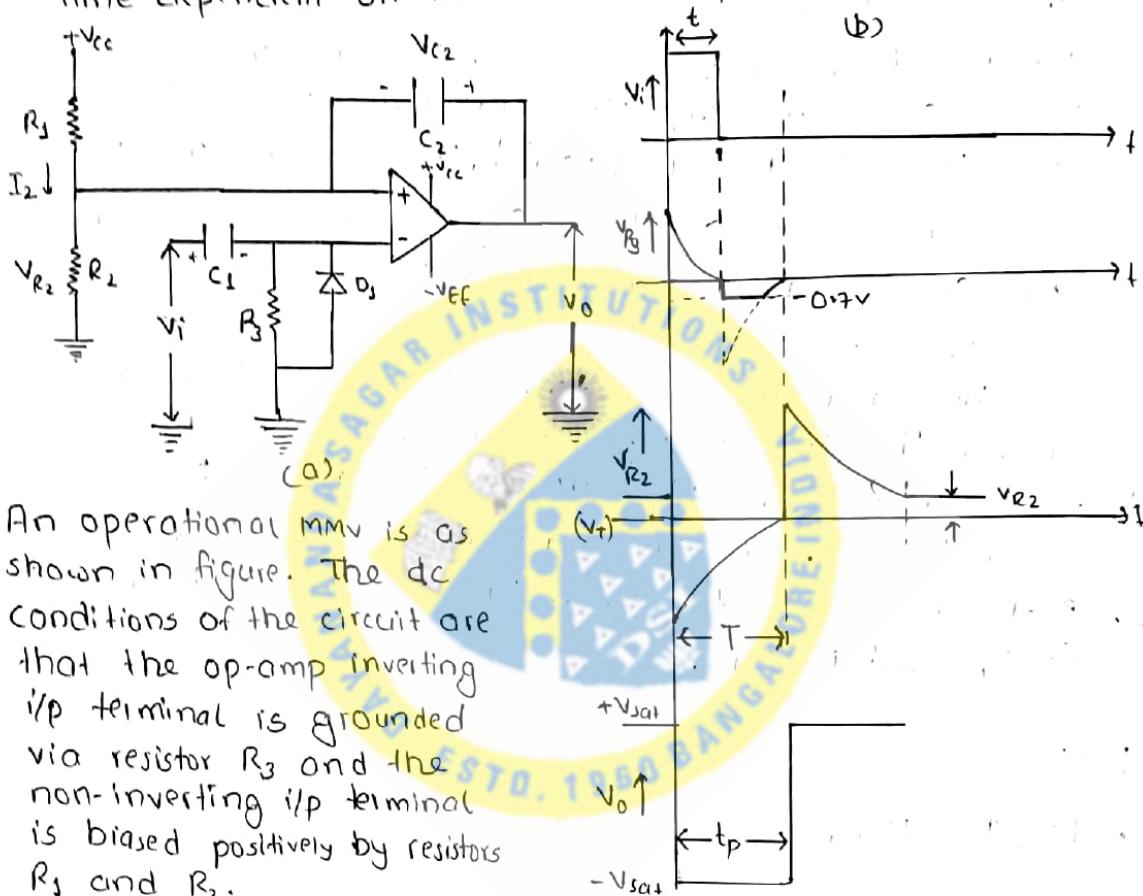
$$I_3 = 180 I_{B\max} = 50 \mu\text{A}$$

$$R_3 = 0.5 / (50 \times 10^{-6}) = 10 \text{ k}\Omega$$

$$R_2 = \frac{14 - 0.5}{50 \times 10^{-6}} = 270 \text{ k}\Omega$$

Monostable Multivibrator

A MMV has one stable output state. Its normal O/p voltage may be low or high and it stays in the normal state until it is triggered. When a trigger I/p is applied, the output switches to its opposite state for a time dependent on the circuit components.



An operational MMV is as shown in figure. The dc conditions of the circuit are that the op-amp inverting i/p terminal is grounded via resistor R_3 and the non-inverting i/p terminal is biased positively by resistors R_1 and R_2 .

Consequently, the op-amp is normally at +ve saturation & capacitor C_2 is charged with the polarity shown.

An input pulse V_i applied to C_1 is differentiated by R_3 & C_1 to produce positive and -ve spikes (V_{R_2}) at the op-amp inverting i/p terminal as shown in figure (b).

The -ve spike is clipped at -0.7v by diode D_1 so that it has no effect on the circuit.

The positive spike lifts the inverting input terminal above the bias level of the non-inverting input and thus causes the

Op-amp o/p to switch to the -ve saturation level. The spike has a short time duration, so the inverting input terminal quickly returns to zero voltage level.

However, when I/p goes to $-V_{sat}$, the charge on C_2 drives the non-inverting input voltage (V_t) down to

$$V_t = -V_{sat} - V_{R2}$$

which is below the ground level. And this voltage is present at non-inverting i/p terminal even after the input triggering spike has disappeared, thus keeping o/p at $-V_{sat}$.

With the o/p at $-V_{sat}$, C_2 discharges via R_1 & R_2 , thus gradually raising non-inverting i/p terminal towards ground level.

When non-inverting terminal goes slightly above ground, the op-amp o/p immediately switches back to $+V_{sat}$ once again and the circuit is returned to its original state. The circuit produces a -ve going pulse each time it is triggered. The pw of o/p depends on C_2 , V_{R2} and R_1 & R_2 .

Design:

- Let, $I_2 = 100I_{Bmax}$
 - Assume, $V_{R2} = 0.5V$
 - $R_2 = \frac{V_{R2}}{I_2}$ and $R_1 = \frac{+V_{cc} - V_{R2}}{I_2}$
 - $R_3' = R_{max} = \frac{0.1V_{BE}}{I_{Bmax}}$
 - To generate spikes from i/p pulse, the time constant $C_2 R_3$ should be approximately one-tenth of i/p pulse width.
- $$C_2 R_3 = 0.1t$$
- $$\Rightarrow C_2 = \frac{0.1t}{R_3}$$

Or, C_1 might be selected first much larger than stray capacitance, then R_3 can be calculated from the above equation.

- To find C_2 ,

consider the capacitor charging equation

$$e_c = E - [E - E_0] e^{-t_p/Rc}$$

$$\Rightarrow e^{-t_p/Rc} = \frac{E - e_c}{(E - E_0)}$$

$$-t_p/Rc = \ln \left(\frac{E - e_c}{E - E_0} \right).$$

$$t_p = R_c \ln \left[\frac{E - E_0}{E - e_c} \right]$$

$$\text{At } t = p\omega, C = C_2 \text{ & } R = R_1 || R_2$$

$$t_p = (R_1 || R_2) C_2 \ln \left[\frac{E - E_0}{E - e_c} \right]$$

- $C_2 = \frac{t_p}{(R_1 || R_2) \ln \left[\frac{E - E_0}{E - e_c} \right]}$

$t_p \rightarrow$ pulse width ($p\omega$)

- $E \rightarrow$ Capacitor charging voltage that is the voltage that it would charge to after triggering if it were allowed to continue charging without the op-amp switching from $-V_{sat}$.

$$\therefore E = V_{R_2} - (-V_{sat})$$

- $E_0 \rightarrow$ E_0 is the initial capacitor voltage before triggering

Taking E as a +ve quantity, E_0 must be assigned a -ve polarity.

$$E_0 = -[+V_{sat} - V_{R_2}] = V_{R_2} - (+V_{sat})$$

$e_c \rightarrow e_c$ is the final capacitor voltage at which op-amp output switches from $-V_{sat}$ to $+V_{sat}$. This is the voltage across C_2 when the non-inverting I/p terminal is at ground level and the o/p is still at $-V_{sat}$.

$$\therefore e_c = 0 - (-V_{sat})$$

$$e_c = +V_{sat}$$

~~~~~

Q: Design a MMV to have an o/p pulse width of 1ms when triggered by a 2v, 100 us input pulse. Use 741 op amp with  $\pm 12V$  supply.

Soln: Let,  $I_2 = 100 \text{ fA}_{\text{max}} = 50 \text{ nA}$

$$\text{but, } V_{R2} < V_I$$

$$V_{R2} = 0.5V$$

$$R_2 = \frac{V_{R2}}{I_2} = 10 \text{ k}\Omega \text{ (std value)}$$

$$R_1 = \frac{V_{cc} - V_{R2}}{I_2} = 230 \text{ k}\Omega \approx 220 \text{ k}\Omega$$

$$E = V_{R2} - [-V_{sat}] \approx 0.5 - [-12+1]$$

$$\approx -10.5V$$

$$e_c = +V_{sat} = (12-1) = 11V$$

$$C_2 = \frac{t_p}{(R_1 || R_2) \ln \left( \frac{E - E_0}{E - e_c} \right)} = 0.027 \mu F \approx 0.03 \mu F$$

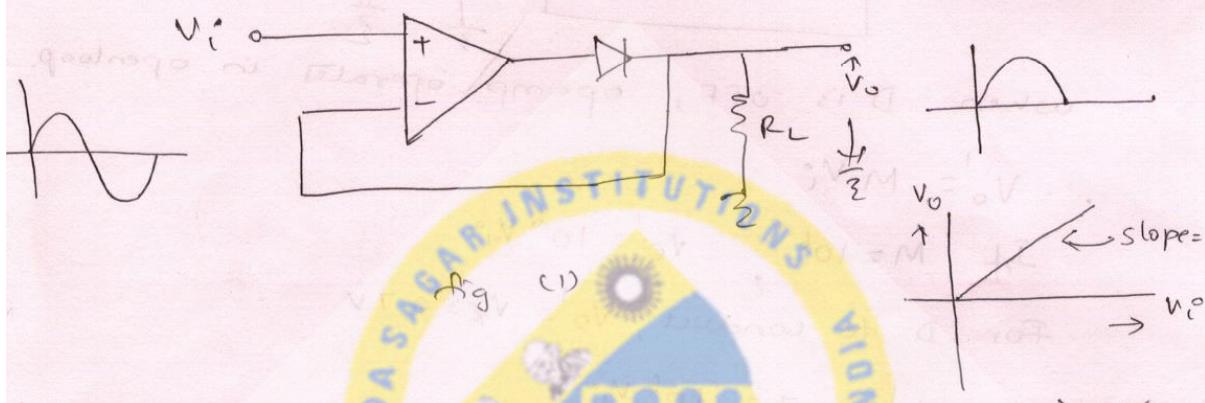
$$R_3(\text{max}) = 140 \text{ k}\Omega \approx 120 \text{ k}\Omega$$

$$C_1 = \frac{0.1t}{R_3} = \frac{0.1 \times 100 \times 10^6}{120 \times 10^3} = 83 \mu F \approx 91 \mu F$$

## Precision Half-wave Circuits

### \* Saturating precision Rectifier

The circuit of an op-amp precision rectifier is shown in fig. It is simply a voltage follower with a diode connected between the op-amp output terminal and the circuit output point.

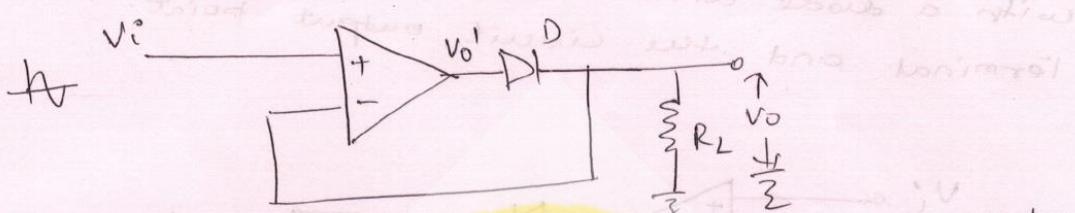


Case (i): During positive half-cycle Diode  $D_1$  is ON. The feed back path is broken. The current through  $R_L$  is zero.  $\therefore V_o = 0$ .

Case (ii): During positive half-cycle and op-amp circuit acts as voltage follower.  $\therefore V_o = V_i$

Case (iii): During negative half cycle  $D_1$  is OFF. The feed back path is broken. The current through  $R_L$  is zero.  $\therefore V_o = 0$ .

Note:- Ordinary Rectifiers using Si diodes have a cut-in voltage of 0.7V. Hence the rectification of Sinusoidal Signal starts above only above the cut-in voltage  $V_f$ . Below  $V_f$  rectification is not possible. In precision Rectifier, rectification below  $V_f$  is possible.



when D is OFF, op-amps operates in openloop.

$$\therefore V_o' = M V_i$$

$$\text{If } M = 10^6, \quad V_o' = 10^6 V_i$$

$$\text{For D to conduct, } V_o' = V_f = 0.7V$$

$$\therefore V_o' = 0.7 = 10^6 V_i$$

$$V_i = 0.7 mV \approx 0$$

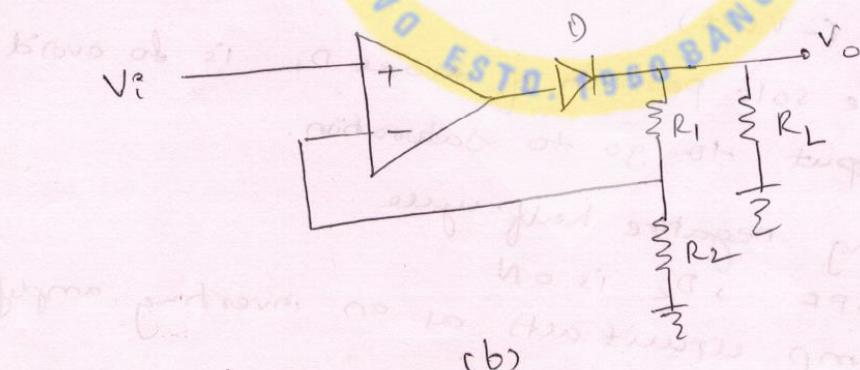
Rectification starts almost down to 0V.  
By reversing the polarity of the diode it is possible to rectify the negative half-cycle.

Advantages of precision Rectifier over ordinary Rectifier

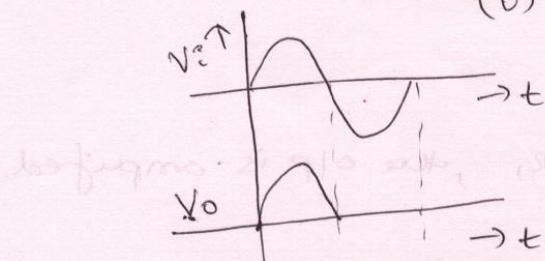
1. No diode drop between input and output.
2. Rectification is possible below  $V_f$ .
3. Amplification is possible.
4. Low output impedance. i.e. it behaves as an ideal diode.

In the above fig., during negative half-cycle diode D is OFF, and op-amp operates in open loop. Open loop voltage gain of opamp is very high and output of opamp goes to  $-V_{sat}$ . This limits the frequency response of the circuit. For high frequency application, a non-saturating precision rectifier must be used.

The fig below shows the precision rectifier with voltage gain. This is a non-inverting amplifier with diode included. The circuit is designed as a non-inverting amplifier. The minimum current through  $R_1$  and  $R_2$  should be a minimum of 100mA to ensure diode is operating correctly. A minimum of 500mA is a good design.



(b)

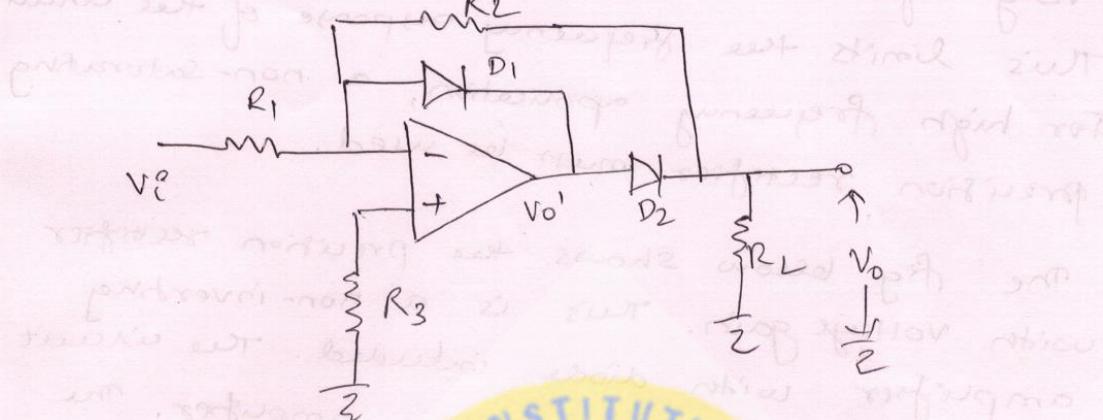


when D is ON,

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_i$$

### A Non-saturating precision Rectifier

Fig below shows inverting precision half wave rectifier, where the o/p of opamp is not driven into saturation.



#### case (i) During positive half-cycle

If  $D_1$  is ON,  $D_2$  is OFF,  $V_o = 0$ .  
Inverting terminal being at Virtual ground,  $V_o'$  and does not reach saturation ( $-V_{sat}$ ).  
The sole position of diode  $D_1$  is to avoid opamp output to go to saturation.

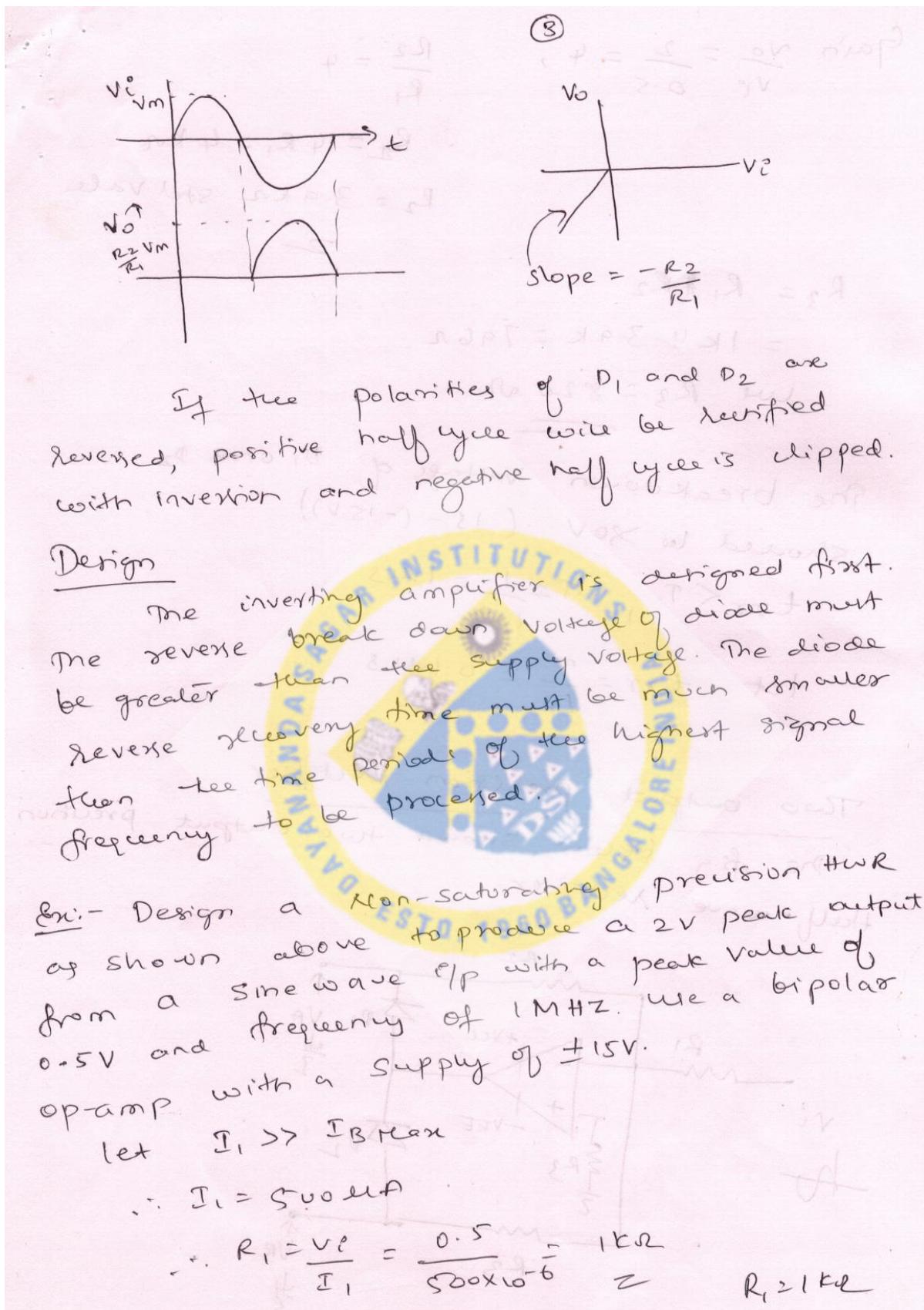
#### case (ii) During negative half-cycle

$D_1$  is OFF,  $D_2$  is ON  
The opamp circuit acts as an inverting amplifier

$$\therefore V_o = -\frac{R_2}{R_1} V_i$$

$$\text{If } R_1 = R_2$$

$V_o = -V_i$ , If  $R_2 > R_1$ , the o/p is amplified.



$$\text{Gain } \frac{V_o}{V_i} = \frac{2}{0.5} = 4,$$

$$\frac{R_2}{R_1} = 4$$

$$\therefore R_2 = 4 R_1 = 4 \text{ k}\Omega$$

$R_2 = 3.9 \text{ k}\Omega$  std value

$$R_3 = R_1 \# R_2$$

$$= 1\text{k} \parallel 3.9\text{k} = 796\Omega$$

$$\text{we } R_3 = 820 \Omega$$

The breakdown voltage of  $D_1$  and  $D_2$  (15V)

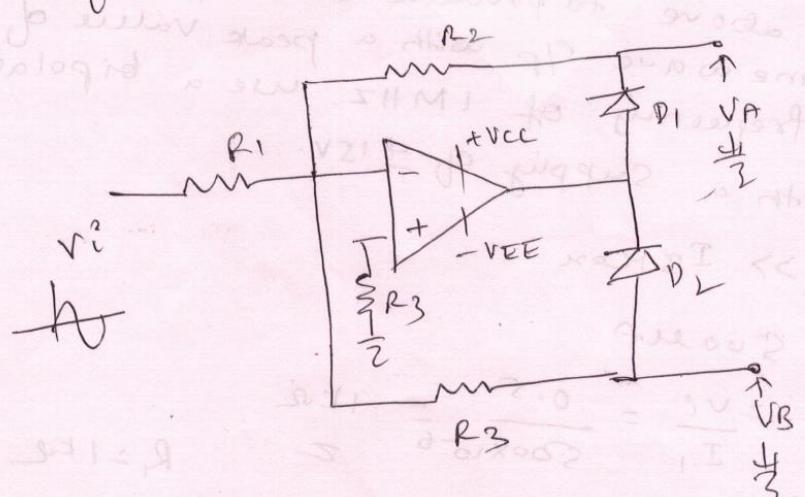
should be  $> 20\text{V}$

transistor  $\tau = \frac{1}{10^6} = 1\text{ ns}$

let  $t_{onr} = \frac{\tau}{10} = 0.1\text{ ns}$

Two output precision Rectifier

The fig below shows two output precision  
Half-wave rectifier



Case (i) During positive half-cycle

$D_1$  is ON,  $D_2$  is OFF

$$\therefore V_A = 0$$

$$V_B = -R_F V_i$$

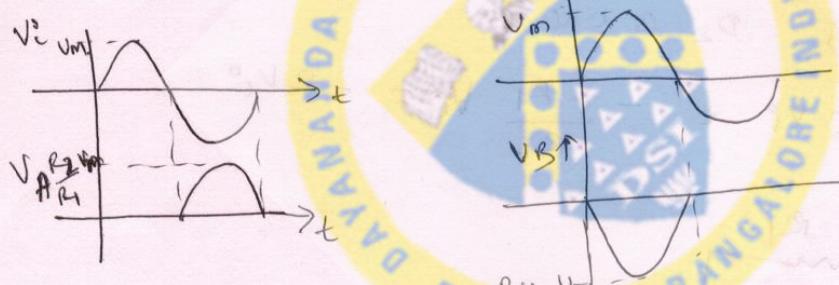
Case (ii) During negative half-cycle

$D_1$  is OFF,  $D_2$  is ON

$$V_A = -\frac{R_2}{R_1} V_C$$

$V_i$  is +ve  
 $V_A$  is +ve.

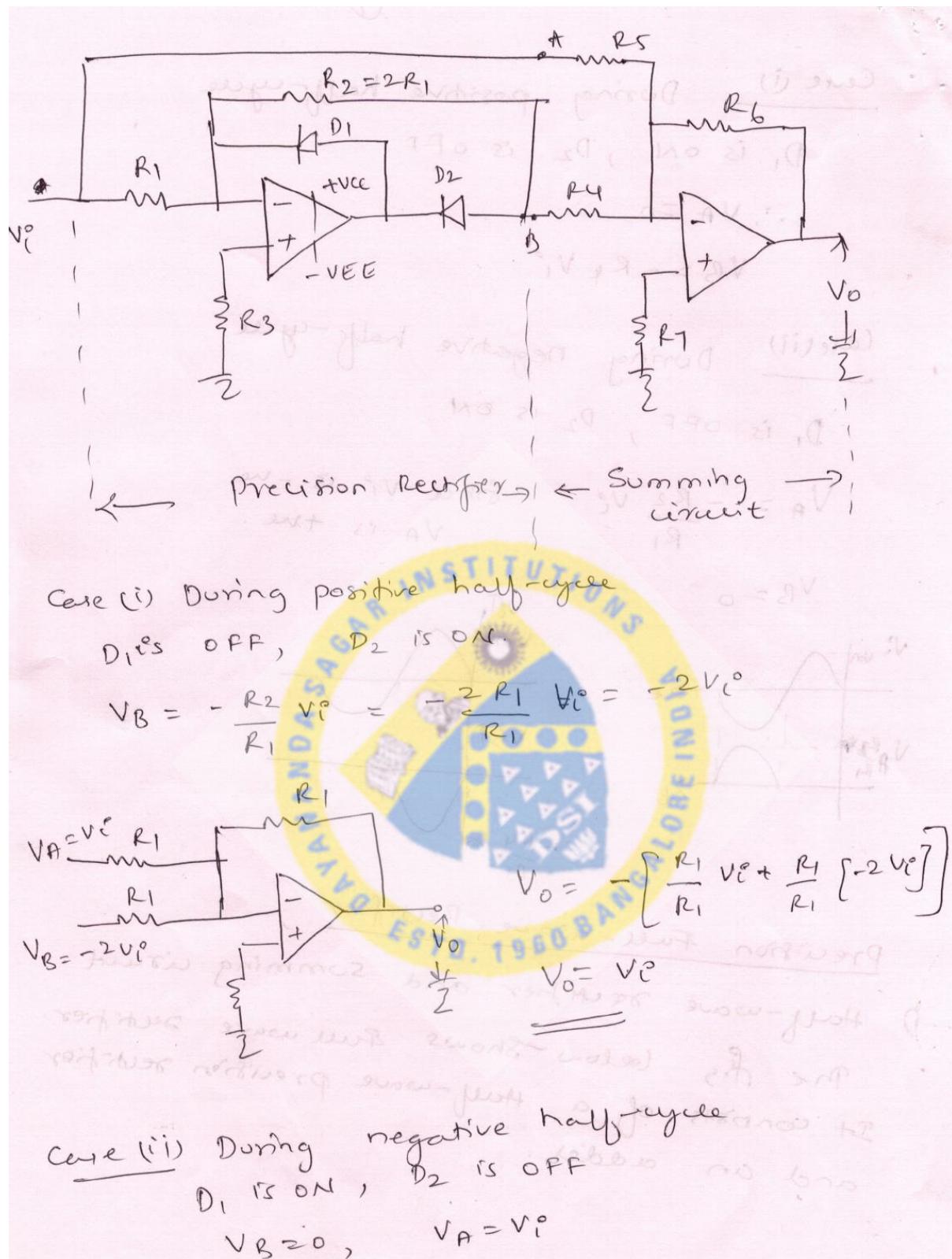
$$V_B = 0$$

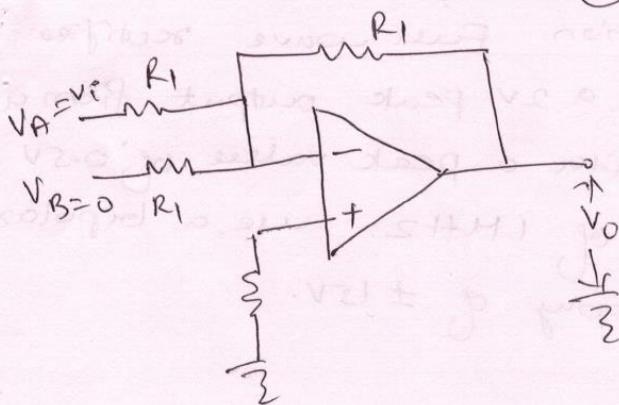


Precision Full-wave Rectifier

i) Half-wave rectifier and summing circuit.

The fig below shows full wave rectifier. It consists of a half-wave precision rectifier and an adder.





$$V_O = -\frac{R_1}{R_1} [V_P] = -V^i$$

since  $V_P$  is negative,  $V_O$  is +ve.



Note

when  $R_6$  is greater than  $R_4$  and  $R_5$  not only rectification but amplification is possible. A precision full wave rectifier is also called as an absolute value unit.

