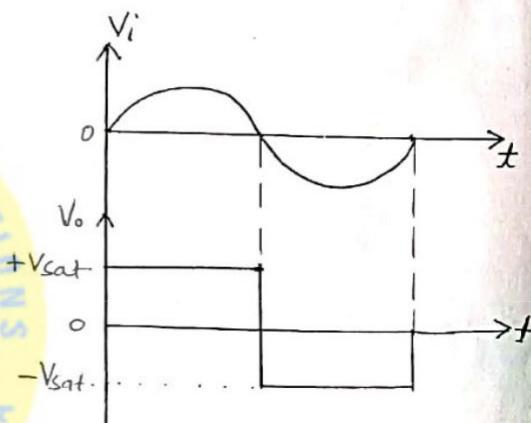
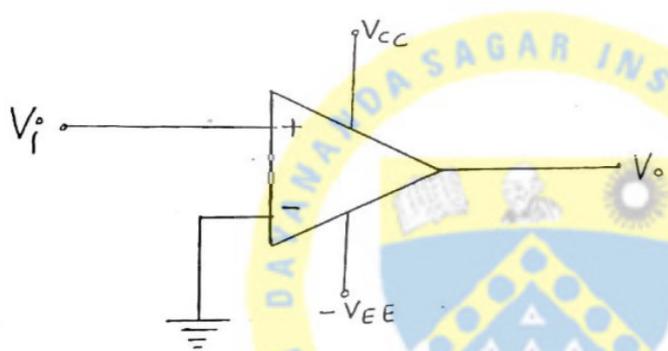


Q.4 With relevant diagrams, explain basic inverting and non-inverting comparator circuit with $V_{ref} = 0V$.

⇒ Comparator ⇒

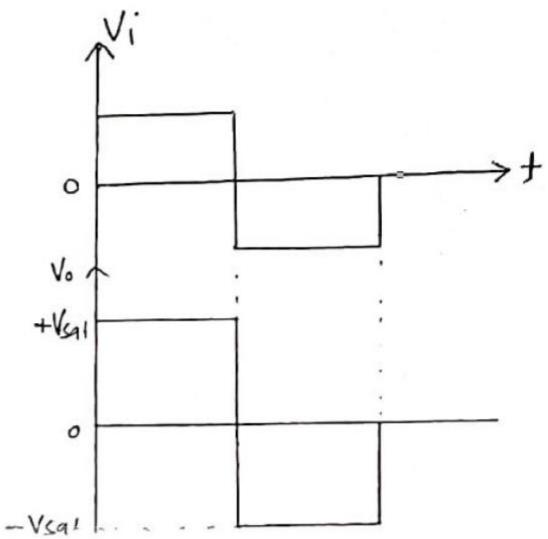
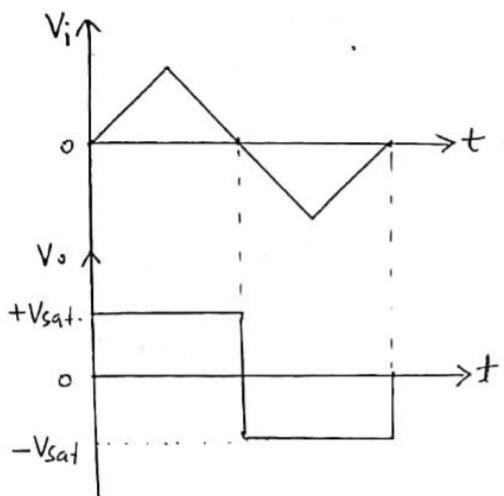
→ A comparator is a ckt which compares a signal voltages applied at one input of an op-amp with a known reference voltage at other end and produce either high or low o/p depending on which i/p is higher.

(i) NON-INV ZCD ⇒



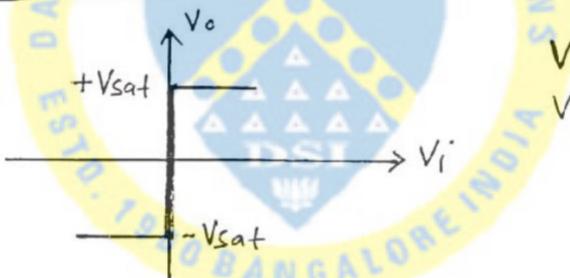
- The input voltage is applied to the non-inv terminal and inv. terminal is grounded.
- When the input signal is positive, the o/p of the op-amp will be at $+V_{sat}$. When the input signal is negative, the o/p of the op-amp will immediately switch to $-V_{sat}$.
- Thus, when the i/p signal crosses the zero level, the o/p vtg switches from one saturation level to another.

i.e. $+V_{sat}$ to $-V_{sat}$. So the circuit is called NON-INV zero crossing detector.



→ Regardless of the i/p waveshape, the o/p is always a rectangular waveform.

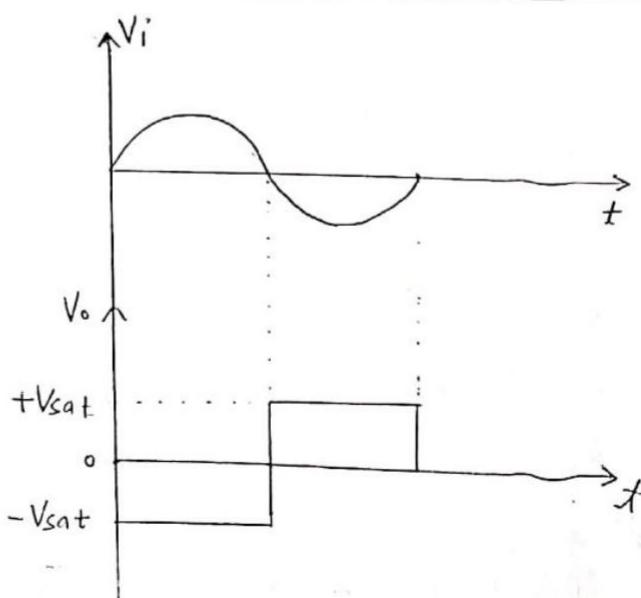
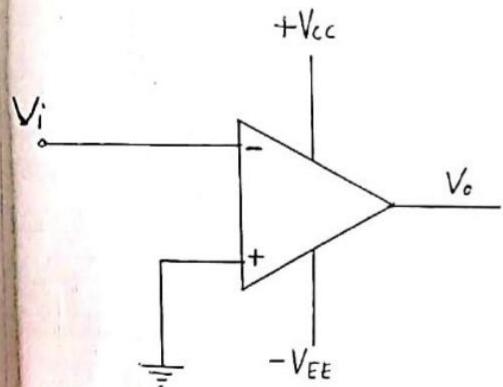
Transfer characteristics:



$$V_i < 0 ; V_o = -V_{sat}$$

$$V_i > 0 ; V_o = +V_{sat} .$$

(2). INV ZCD ⇒

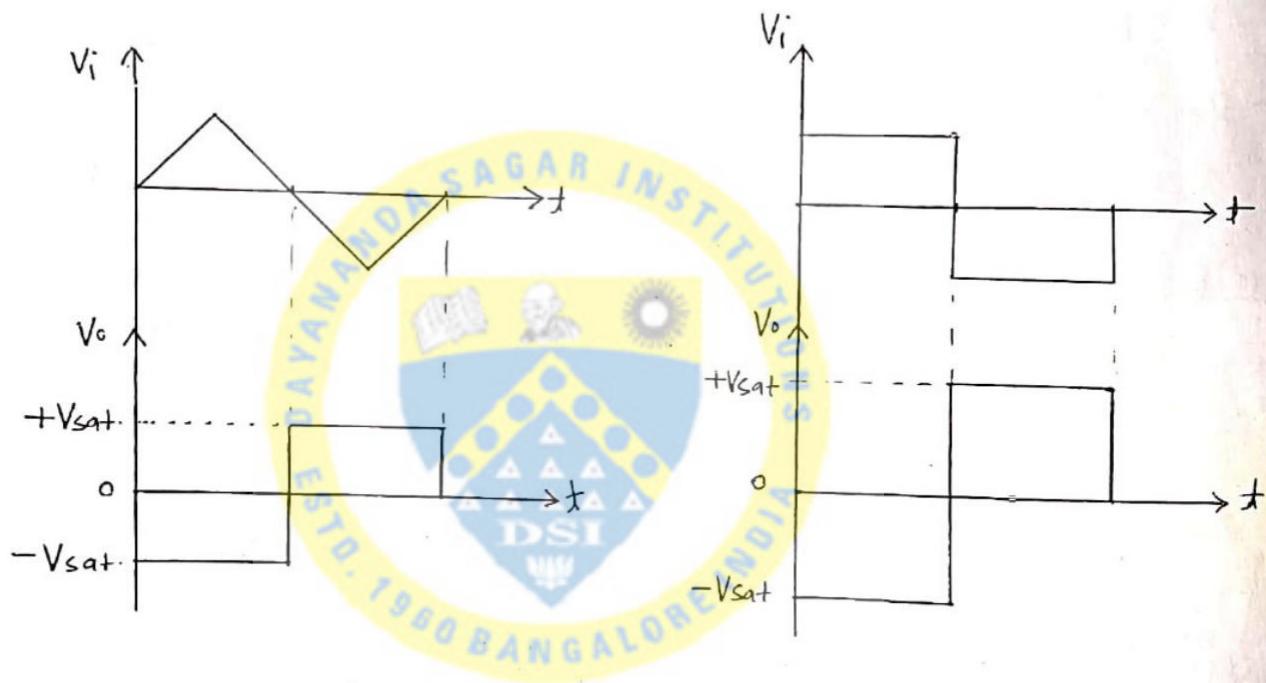


→ When the input signal is (+ve), the o/p of the op-amp will be $-V_{sat}$.

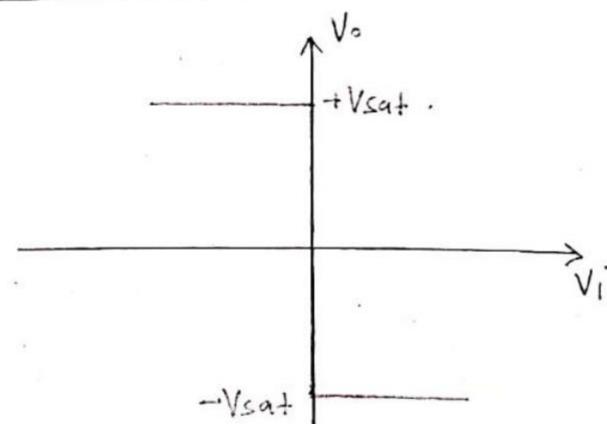
When the input signal is (-ve), the o/p of the op-amp immediately switches to $+V_{sat}$.

→ Thus when the input signal crosses the zero level, the o/p voltage switches from one saturation level to another i.e. $+V_{sat}$ to $-V_{sat}$.

So, the ckt is called INV-ZCD sometimes termed as INVERTER.



Transfer characteristic:



$$V_i < 0 ; V_o = +V_{sat}$$

$$V_i > 0 ; V_o = -V_{sat}$$

- Limitations ⇒
- Rapid switching won't occur
 - There exists an upper limit to the operating frequency of any comp.
 - There exists an uncertainty region.

Q.5. With neat circuit diagram and waveforms, explains the - circuit operation of an op-amp inverting schmitt trigger ckt.

- ⇒ In basic comparator, a feedback is not used and op-amp is used in open-loop mode.
- As the output gain of the op-amp is very large, a very small noise voltage also can cause triggering of the comparator to change its state.
- Such unwanted noise cause the o/p to jump b/w high & low states.
- The comparator ckt used to avoid such unwanted triggering is called regenerative comparator or Schmitt trigger which basically use (+ve) feedback.

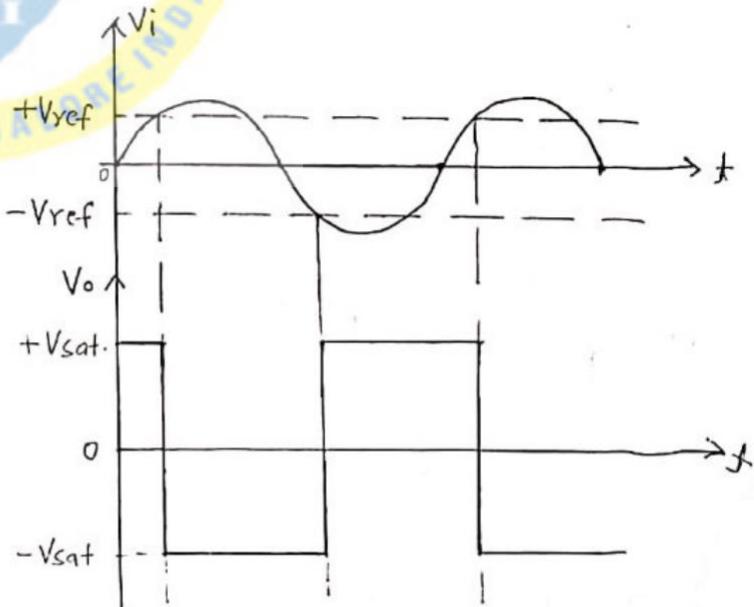
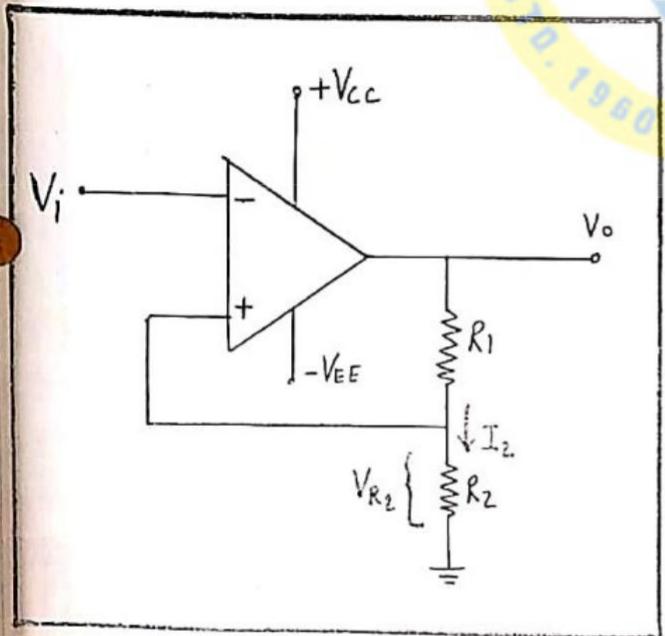


Fig INV schmitt trigger ckt.

- The input is applied to the inverting terminal of the Schmitt trigger ckt.
- The feedback is given to non-inv. terminal. This ensures

(+ve) feedback .

→ The voltage at the NON-INV i/p is :

$$V_{ref} = I_2 R_2$$

$$\text{where, } I_2 = \frac{V_o}{R_1 + R_2}$$

$$\Rightarrow V_{ref} = \frac{V_o \cdot R_2}{R_1 + R_2}$$

→ When the o/p voltage V_o is at $+V_{sat}$, then V_{ref} will be a positive voltage & Voltage at NON-INV terminal will be positive ($+V_{ref}$).

$$\text{i.e. } V_{ref} = \frac{V_o \cdot R_2}{R_1 + R_2}$$

$$\text{Now, } V_o = +V_{sat}$$

$$\therefore +V_{ref} = \frac{+V_{sat} \cdot R_2}{R_1 + R_2}$$

→ When $V_o > +V_{ref}$, then the voltage at INV terminal becomes greater than ($+V_{ref}$) NON-INV terminal & the o/p will switch from $+V_{sat}$ to $-V_{sat}$.

$$\text{i.e. } V_{ref} = \frac{V_o \cdot R_2}{R_1 + R_2}$$

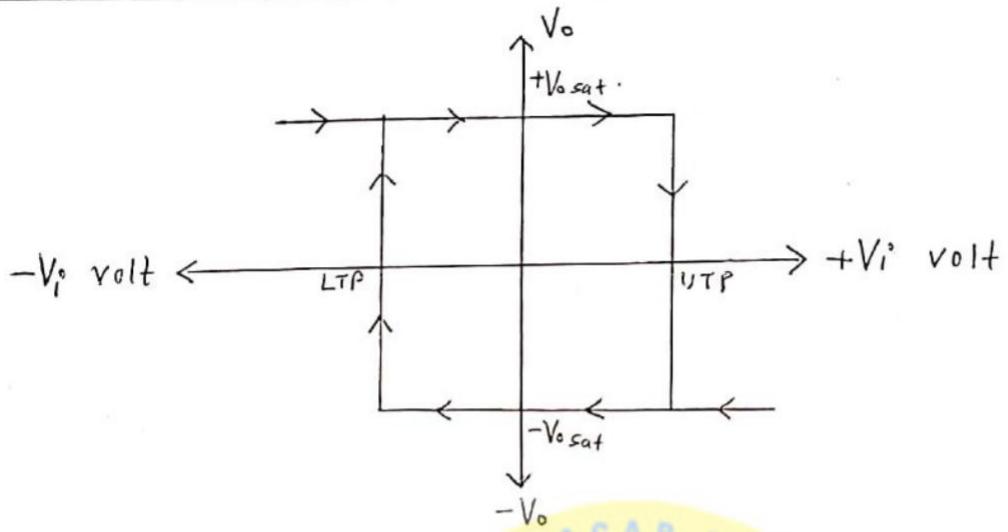
$$\Rightarrow -V_{ref} = \frac{-V_{sat} \cdot R_2}{R_1 + R_2}$$

→ From waveform, the vtg at point $+V_{ref}$ on the waveform at which o/p shifts from $+V_{sat}$ to $-V_{sat}$ is called "Upper Triggering point" (UTP).

→ Similarly, the vtg at point $-V_{ref}$ on the waveform at which o/p shifts from $-V_{sat}$ to $+V_{sat}$ is called "Lower triggering point" (LTP).

→ The o/p of a schmitt trigger is always a square-wave or rectangular wave.

I/p - o/p characteristics or Transfer characteristics:



→ When $V_i = 0V$, o/p will be at $+V_{sat}$.

When $V_i = UTP$, o/p switches from $+V_{sat}$ to $-V_{sat}$.

→ When $V_i < LTP$, o/p will be at $-V_{sat}$.

When $V_i = LTP$, o/p will switch from $-V_{sat}$ to $+V_{sat}$.

→ The voltage difference b/w the upper and lower triggering points is referred to as hysteresis.

$$\begin{aligned}\therefore V_H &= UTP - LTP \\ &= \left[\frac{+V_{sat} \cdot R_2}{R_1 + R_2} \right] - \left[\frac{-V_{sat} \cdot R_2}{R_1 + R_2} \right] \\ &= \frac{2 \cdot V_{sat} \cdot R_2}{R_1 + R_2}.\end{aligned}$$

Schmitt-trigger ckt design ⇒

→ The current I_2 flowing through the resistors R_1 & R_2 is chosen to be 100 times $I_{B(\max)}$.

i.e. $I_2 = 100 I_{B\max}$

→ $R_2 = \frac{\text{Triggering vfg}}{I_2}$

→ $R_1 = \frac{V_o - \text{triggering Vtg}}{I_2}$

$$V_{ref} = I_2 R_2 \Rightarrow R_2 = \frac{V_{ref}}{I_2}$$

Applying KVL from o/p V_o , R_1 & R_2 , we get .

$$V_o - I_2 R_1 - V_{ref} = 0$$

$$\Rightarrow R_1 = \frac{V_o - V_{ref}}{I_2}$$

- Q.6.** With a neat ckt diagram & waveform and expressions , explain the capacitor-Coupled non-inverting cross detector .

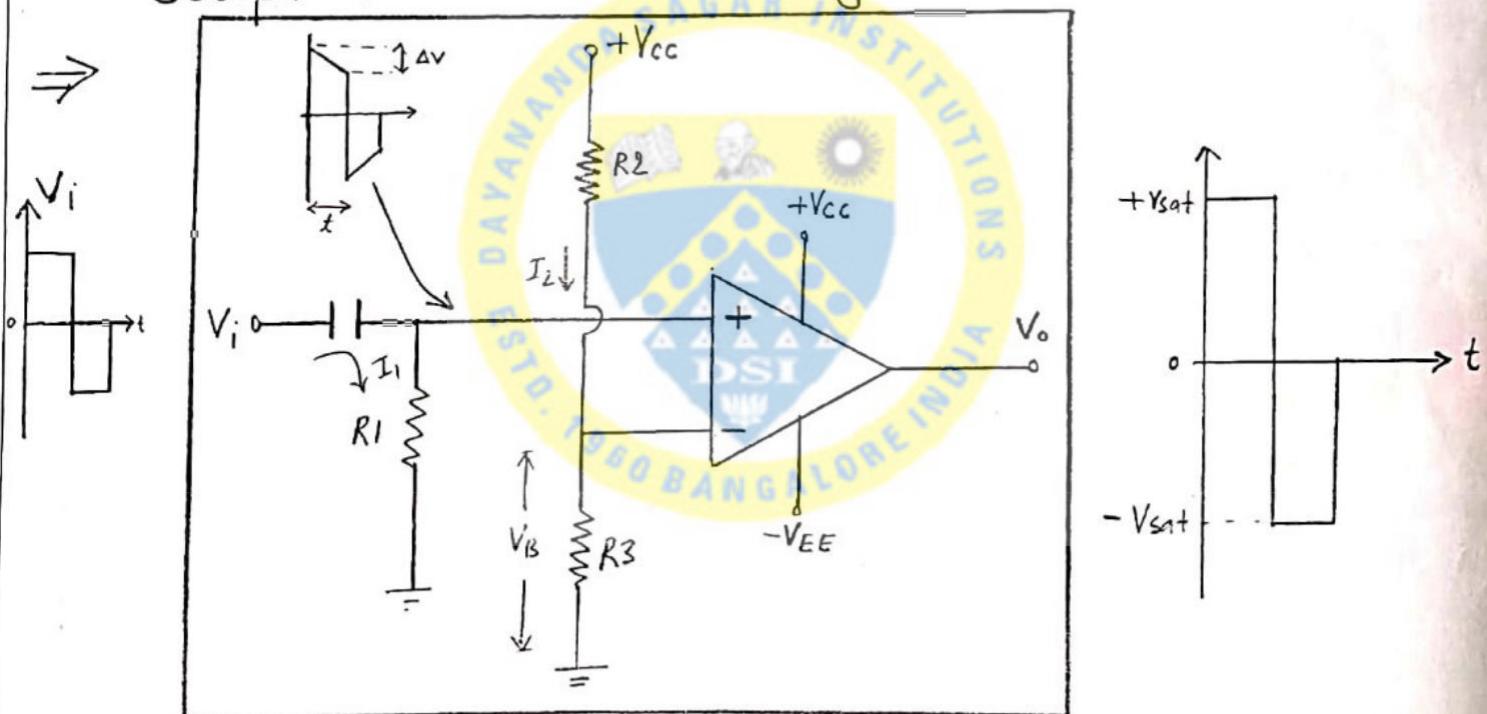


Fig. CC non-inv cross-detector .

- figure shows CC crossing detector with non-inv. terminal connected to ground via resistor R_1 to provide a dc bias current path to the op-amp .
- The inv. terminal connected to a potential divider ck . Due to this inv. terminal is held at a small (+ve) voltage (V_B) .

→ This ensures that the o/p is held at $-V_{sat}$, when no input signal is present.

→ When CC-signal (V_i) drives the non-inv i/p terminal above V_B , the o/p switches to $+V_{sat}$ and when i/p is less than V_B ($V_i < V_B$), the o/p fall back to $-V_{sat}$.

Design ⇒

→ The resistance R_1 is designed as:

$$R_1 = R_{1(\max)} = \frac{0.1 V_{BE}}{I_{B\max}}$$

→ The current I_2 is chosen to be about 100 times $I_{B\max}$.

$$\therefore I_2 = 100 \times I_{B\max}$$

→ The voltage V_B across R_3 is given by:

$$V_B = I_2 R_3$$

$$\Rightarrow R_3 = \frac{V_B}{I_2}$$

V_B is usually chosen to be about 0.1V

→ Applying KVL from V_{cc} , R_2 & R_3 , we get

$$V_{cc} - I_2 R_2 - I_2 R_3 = 0$$

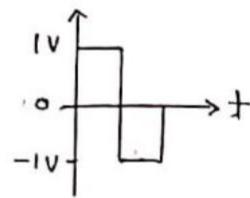
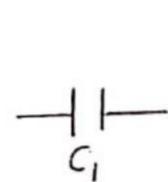
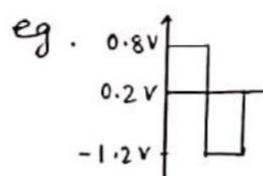
$$\Rightarrow R_2 + R_3 = \frac{V_{cc}}{I_2}$$

$$\Rightarrow R_2 = \frac{V_{cc}}{I_2} - R_3$$

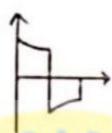
→ At lower frequency: X_C , should be much smaller than R_1 .

$$\text{i.e. } X_{C_1} = \frac{R_1}{2\pi} \Rightarrow C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{2\pi} \right)}$$

→ The i/p vtg to capacitor 'C_i' may not be symmetrical above or below ground level, but it is always symmetrical on the op-amp side of C_i.



→ When square-wave is applied as an input to a capacitor-coupled detector, the waveform at the op-amp i/p terminal can develop considerable tilt as shown in fig.



→ The i/p current I_i is calculated as:

$$I_i = \frac{V_i}{R_i}$$

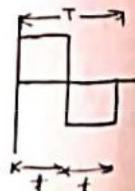
Assuming I_i constant

$$C_i = \frac{I_i \cdot t}{\Delta V}$$

$$C_i = \frac{I_i}{4V \cdot 2f}$$

Assume, $\Delta V = 1V$

$$\left. \begin{aligned} \text{Note: } I_i &= \frac{V_i(\text{peak})}{R_i} \\ &= \frac{V_i(p-p)}{2R_i} \end{aligned} \right\}$$



$$\therefore T = t + t$$

$$\Rightarrow 2t = T$$

$$\Rightarrow t = \frac{T}{2}$$

$$\Rightarrow t = \frac{1}{2} \cdot \frac{1}{f}$$

$$\Rightarrow t = \frac{1}{2f}$$

Q.7. With a neat circuit diagram, Explain how diodes may be used to select the trigger points of an inverting schmitt trigger

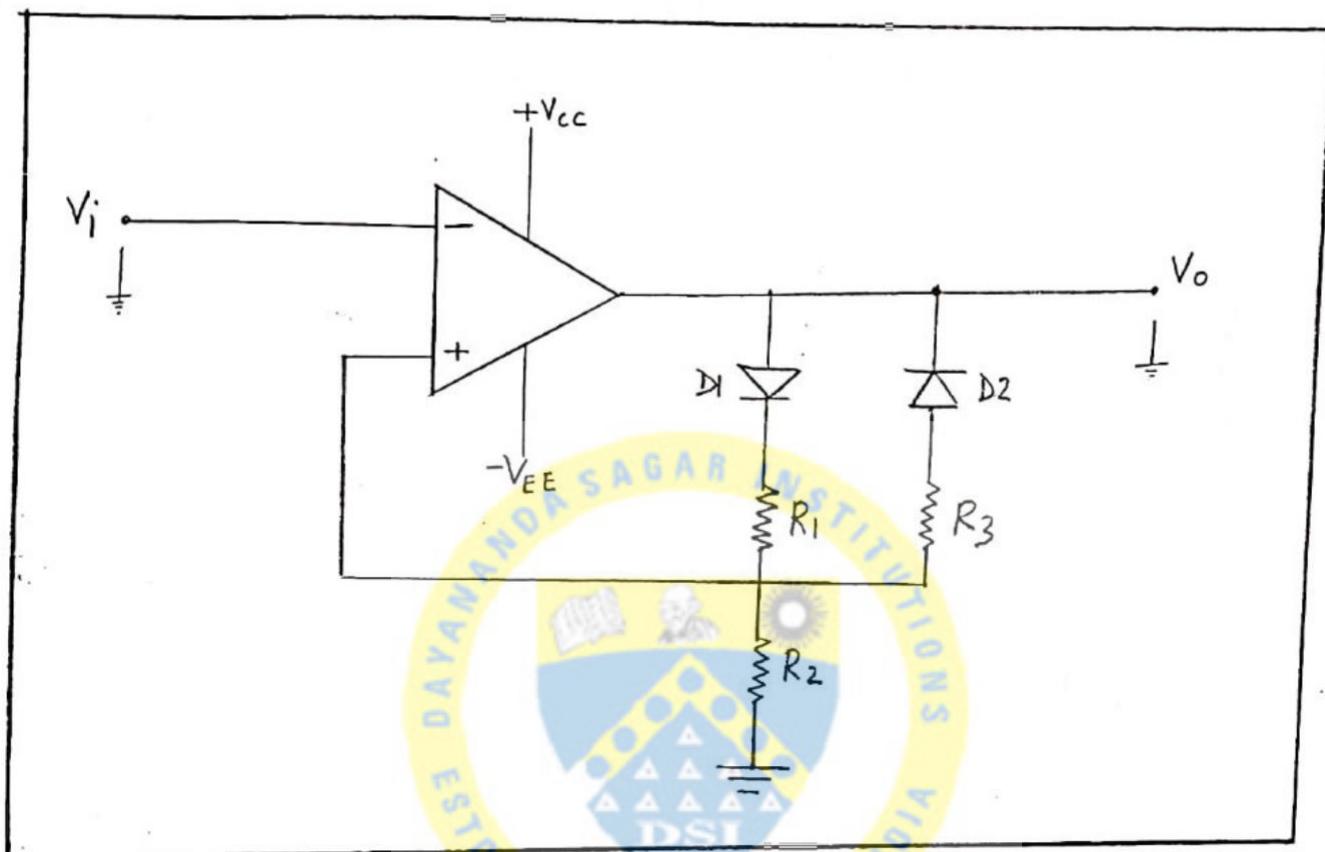


Fig. Inverting schmitt trigger with different LTP & UTP

→ The schmitt trigger ckt shown in fig. uses two diodes D_1 & D_2 and three resistors R_1 , R_2 & R_3 to get different LTP & UTP voltages.

Case - I: When $V_o = +V_{sat}$,
The diode D_1 is forward biased and D_2 is reverse biased.

$$\therefore \text{UTP} = V_{R_2}$$

$$\Rightarrow \text{UTP} = \frac{R_2}{R_1 + R_2} [IV_oI - V_F]$$

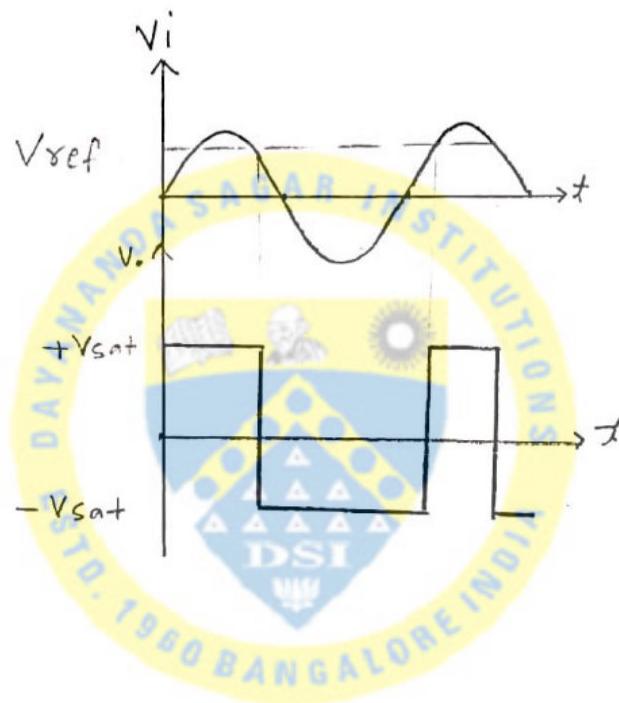
(Case - ii) : When $V_o = -V_{sat}$,
the diode D_1 is reverse biased and D_2 is forward
biased.

$$LTP = V_{R_2}$$

$$\Rightarrow LTP = \frac{R_2}{R_2 + R_3} [|V_o| - V_F]$$

Where, V_F is voltage drop across D_1 & D_2

→ Different values of R_1 & R_2 gives different UTP & LTP voltages.



Design:

Let, $I_2 = 500\text{mA}$

$$(i). R_2 = \frac{V_{R_2}}{I_2} = \frac{UTP}{I_2}$$

$$V_{R_2} = UTP$$

$$(ii). V_{sat} = (V_{cc} - 1\text{V})$$

$$-V_{sat} = (-V_{ee} + 1\text{V})$$

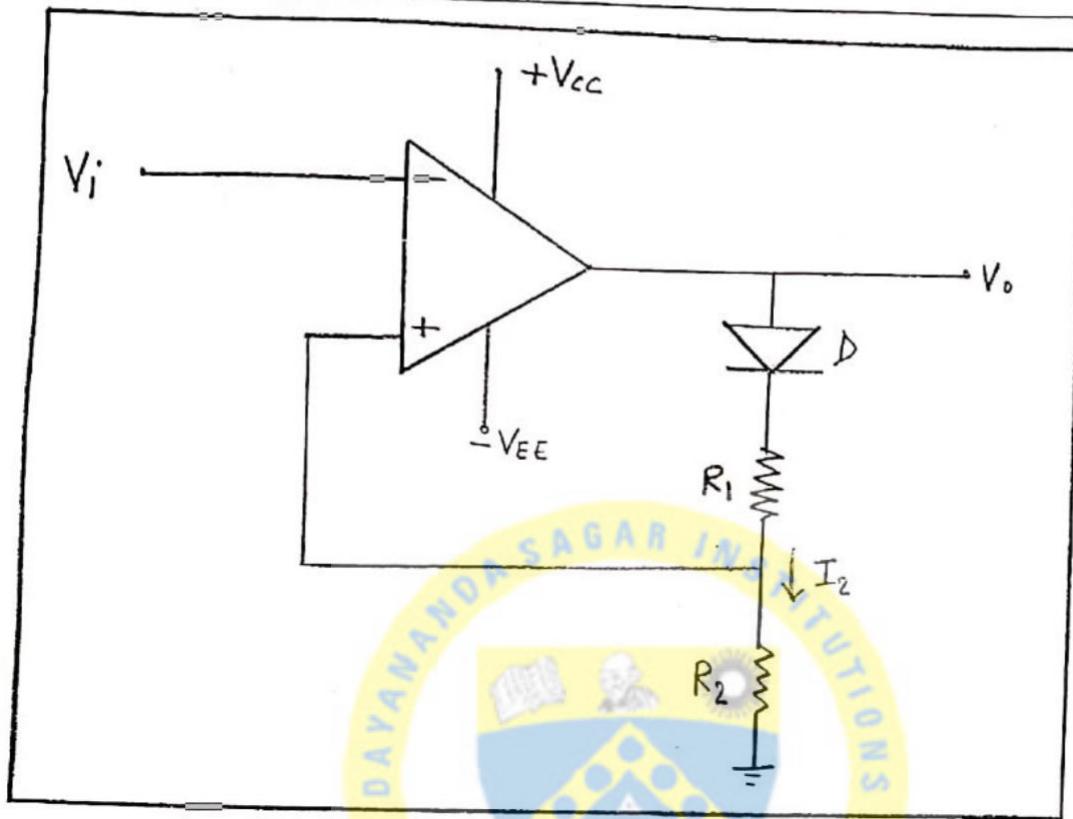
$$(iii). \text{Assume, } V_F = 0.7\text{V}$$

$$(iv). UTP = \frac{R_2}{R_1 + R_2} (|+V_{sat}| - V_F) , \text{ Determine } R_1$$

$$(5). LTP = \frac{R_2}{R_2 + R_3} [1 - V_{sat} | 1 - V_F]$$

Determine, R_3 .

Schmitt trigger with $LTP = 0.4$ $UTP = (+ve) \Rightarrow$



Design:

$$(1). \text{ Let, } I_2 = 500 \mu\text{A}$$

$$(2). R_2 = \frac{V_{R_2}}{I_2}$$

$$\text{Here, } V_{R_2} = UTP$$

$$R_2 = \frac{UTP}{I_2}$$

$$(3). R_1 = \frac{V_{R_1}}{I_2}$$

Applying KVL to o/p ckt.

$$V_{sat} - V_F - I_2 R_1 - V_{R_2} = 0$$

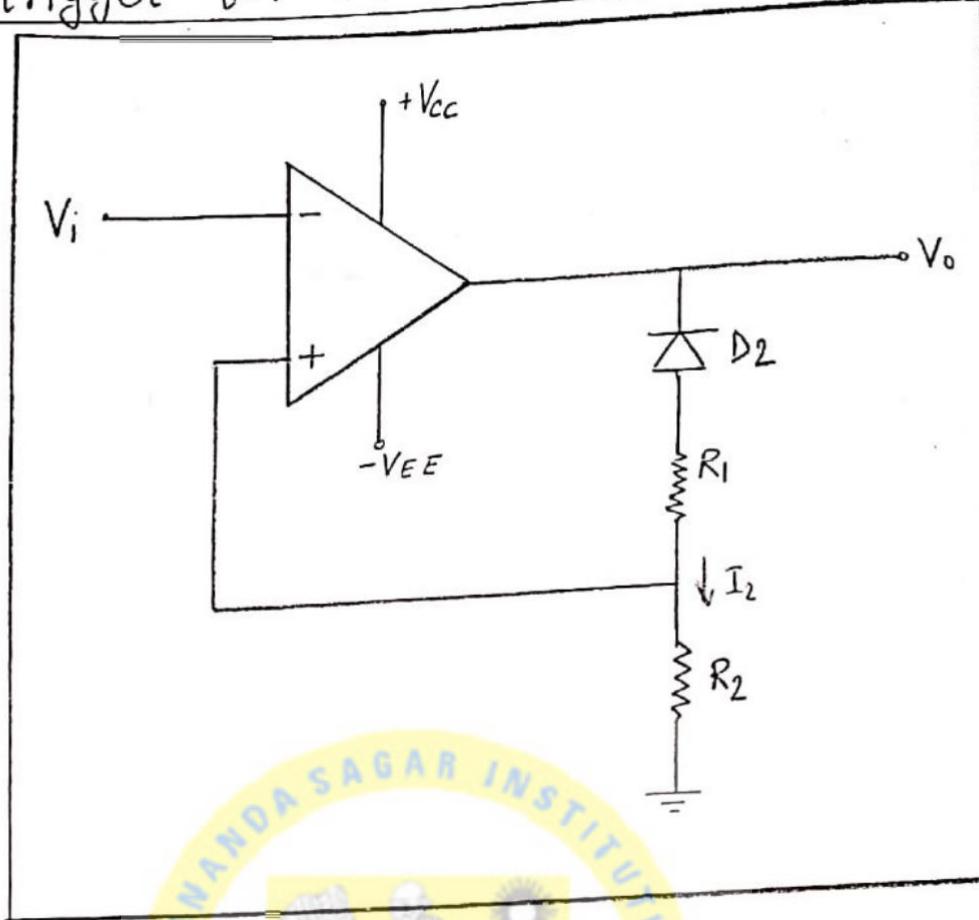
$$\Rightarrow R_1 = \frac{V_{sat} - V_F - V_{R_2}}{I_2}$$

$$\Rightarrow R_1 = \frac{(V_{cc} - 1) - V_F - UTP}{I_2}$$

$$\text{Where, } +V_{sat} = (V_{cc} - 1V)$$

$$V_{R_2} = UTP$$

Schmitt trigger for $V_{TP} = 0$ & $LTP = (+ve)$:



Design:

(1). Let, $I_2 = 500 \mu A$

(2). $R_2 = \frac{V_{R_2}}{I_2}$

Here, $V_{R_2} = LTP$

$$\therefore R_2 = \frac{LTP}{I_2}$$

(3). $R_1 = \frac{V_{R_1}}{I_2}$

Applying KVL to o/p ck

$$V_{sat} - V_F - I_2 R_1 - V_{R_2} = 0$$

$$R_1 = \frac{V_{sat} - V_F - V_{R_2}}{I_2}$$

$$\therefore R_1 = \frac{[V_{cc} - 1V] - V_F - LTP}{I_2}$$

Here, $V_{sat} = V_{cc} - 1V$
 $V_{R_2} = LTP$

With a neat circuit diagram and waveforms, explain the circuit operation of op-amp Astable multivibrator.

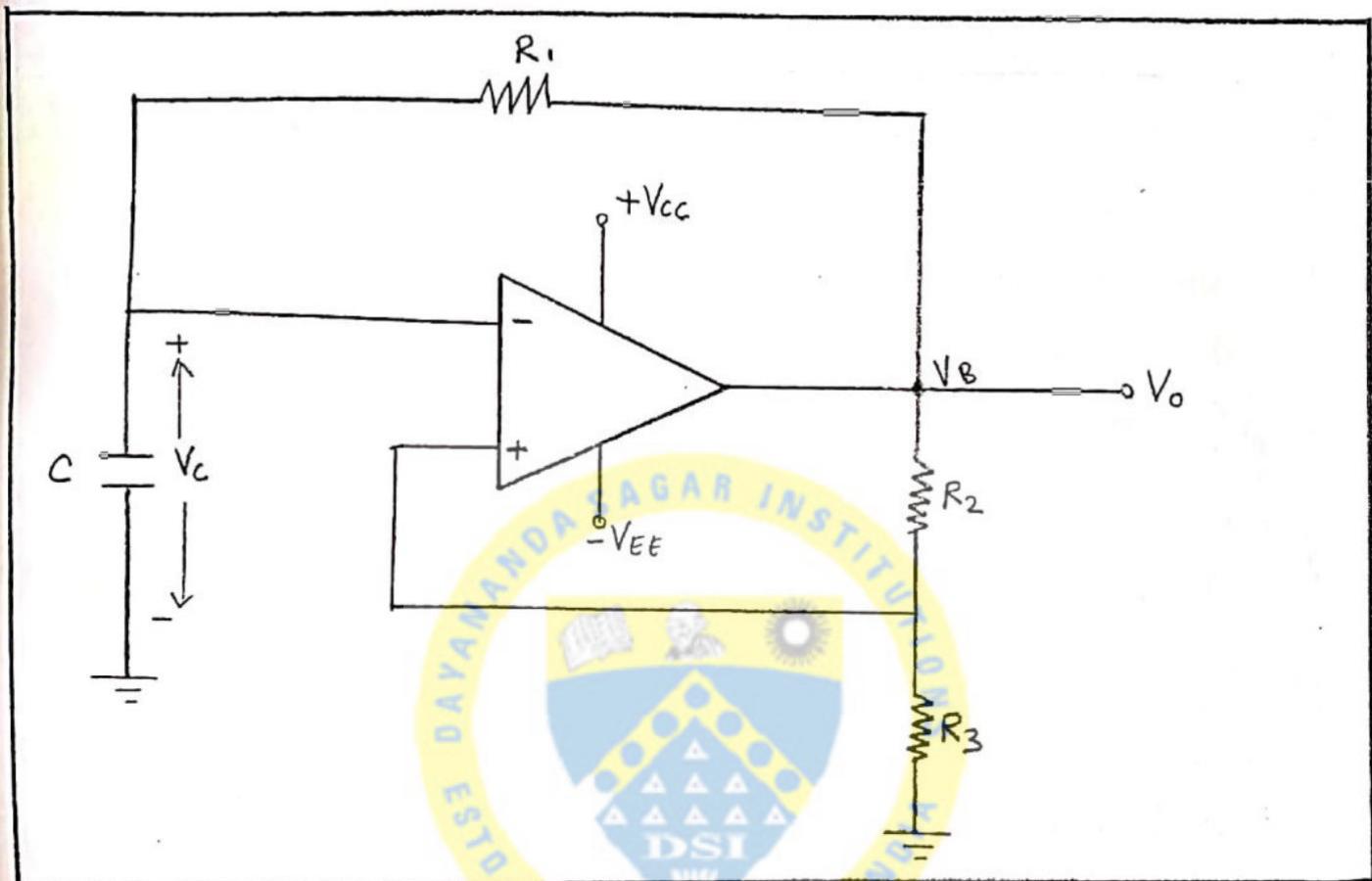


Fig : Astable multivibrator ckt

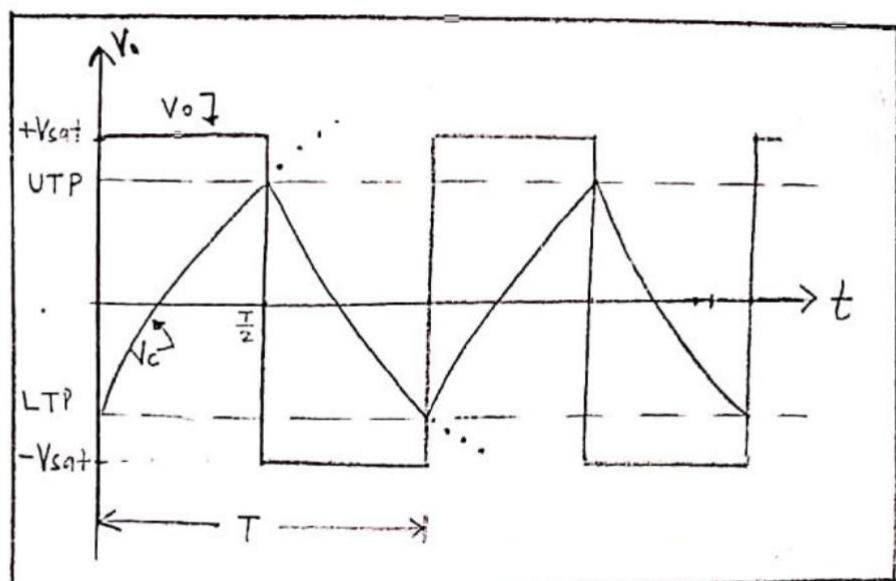


Fig O/p v/tg & Capacitor v/tg waveforms

- Astable multivibrator is also called free-running multivibrator (\because it has no inputs).
 - The output voltage continuously switches between high & low levels without any i/p.
 - It has no stable state.
 - The ckt diagram of AMV using schmitt trigger is as shown in the fig.
- The op-amp with resistors R_2 and R_3 forms a inv. schmitt trigger ckt.
- The input voltage to schmitt trigger is the voltage across capacitor C_1 which is changed from the op-amp o/p through R_1 .
 - When the power is turned ON, o/p automatically switches either to $+V_{sat}$ or $-V_{sat}$, since these are only stable states allowed by schmitt trigger.

Operation \Rightarrow

- Let, the capacitor voltage be initially zero i.e. $V_c = 0$ and let, $V_o = +V_{sat}$. Due to (+ve) f/b, the potential at pt. B in fig is given by:

$$V_B = \frac{R_2}{R_1 + R_2} \cdot V_{sat} = UTP$$

- The capacitor 'c' charges exponentially with a time constant equal to RC with a polarity (+) on top. When the ~~output~~ capacitor voltage V_c just crosses the UTP vtg, the o/p V_o rapidly changes from $+V_{sat}$ to $-V_{sat}$.

Now o/p voltage $V_o = -V_{sat}$. The vtg at point B is given by

$$V_B = \frac{R_2}{R_1 + R_2} (-V_{sat}) = LTP.$$

- Now the capacitor discharges to zero & starts charging in the reverse direction due to o/p V_o being at $-V_{sat}$. The capacitor voltage increases negatively towards $-V_{sat}$. When V_c just crosses LTP voltage, the output V_o rapidly changes from $-V_{sat}$ to V_{sat} . Thus producing a symmetrical square wave o/p V_o as shown in above figure.

Design →

- The minimum current flowing through R_1 is chosen to be 100 times the op-amp input bias current.

$$I_1 = 100 \times I_{B\ max}$$

$$\rightarrow R_1 = \frac{|V_o| - UTP}{I_1}$$

$$\rightarrow R_3 = \frac{V_{R_3}}{I_2} = \frac{UTP}{I_2}$$

$$\rightarrow R_2 = \frac{V_o}{I_2} - R_3 \quad \text{or} \quad R_2 = \frac{V_o - V_{R_3}}{I_2}$$

$$\rightarrow C_1 = \frac{I_1 \times t}{\Delta V}$$

where, $\Delta V = UTP - (-LTP)$.

BIFET design :

Select, $R_2 = 1 \text{ M}\Omega$

Select, $C_1 = 0.1 \text{ nF}$

$$R_3 = \frac{V_{R3}}{I_2}$$

$$R_1 = \frac{|V_o| - UTP}{I_1}$$

$$I_2 = \frac{|V_o| - UTP}{R_2}$$

Q.9. With a neat circuit diagram and waveforms, explain the circuit operation of op-amp monostable multivibrator.

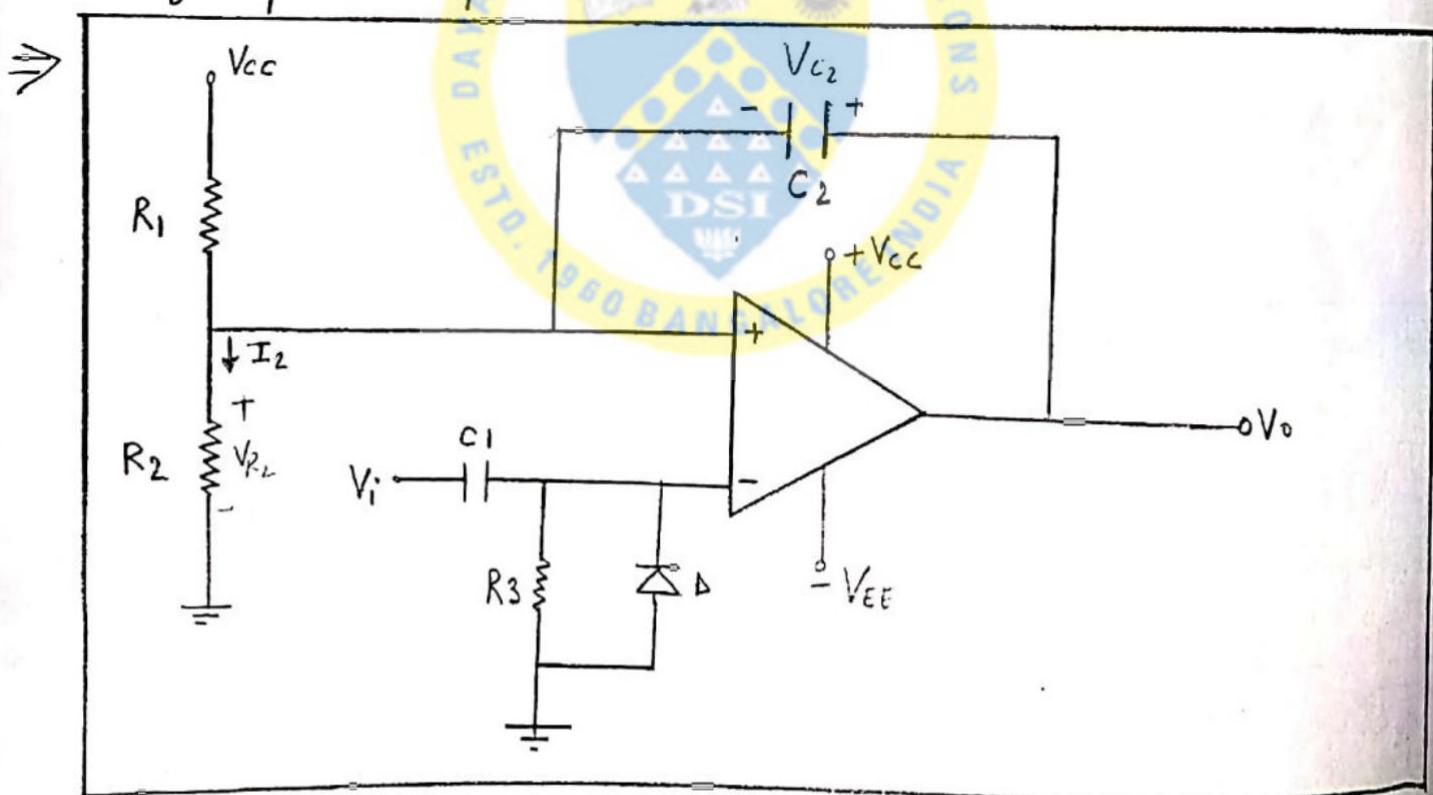


Fig. Mono-stable multivibrator

→ A monostable multivibrator has only one stable o/p state. In this stable state, the o/p vtg may be high or low, and it remains in this state until the multivibrator is triggered.

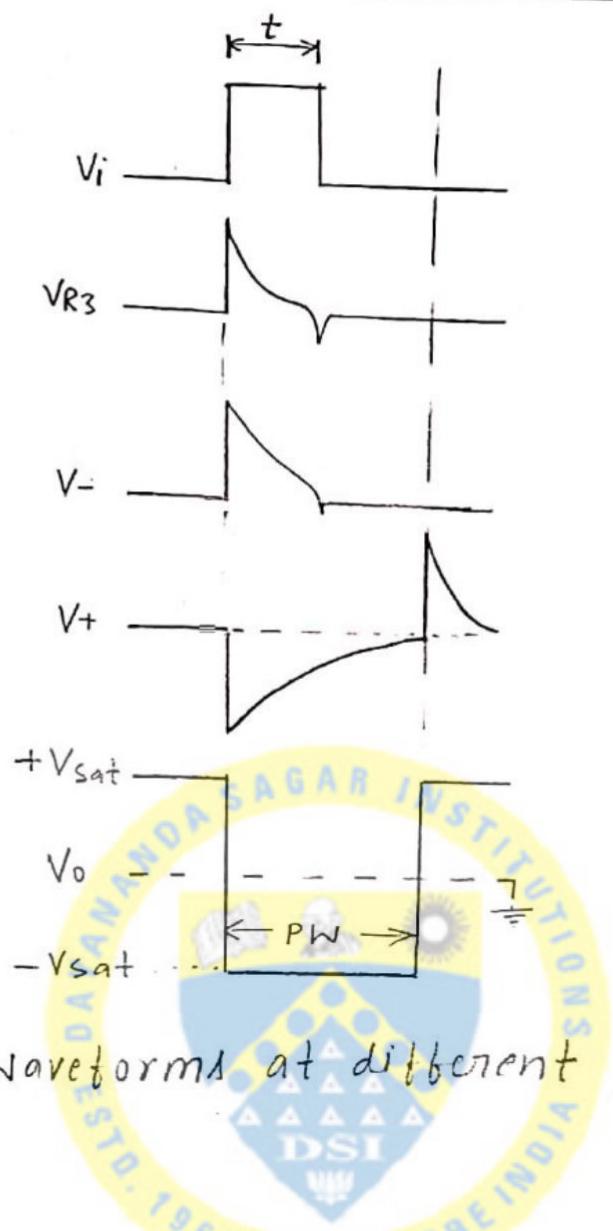


Fig. Waveforms at different points

Operations:

- Before the application of trigger pulse, the INV i/p terminal of op-amp is grounded through resistor R_3 . The non-inv. terminal is connected to voltage divider ckt of R_1 & R_2 connected to $+V_{cc}$.
- The voltage V_{R_2} across R_2 at non-inv. terminal is higher than INV terminal voltage & the o/p voltage is held at $+V_{sat}$ and capacitor C_2 is charged with the polarity shown above.
- The input pulse V_i is now applied to differentiating circuit of R_3 and C_1 to produce positive and negative spikes at op-amp inv. terminal as shown.

- The negative spike is clipped at 0.7V by diode D₁, so that it has no effect on the circuit.
- The (+ve) spike rises the voltage at the INV i/p terminal beyond that at the non-inv terminal and op-amp output switches to $-V_{sat}$.
- The spikes has a relatively short time duration, so the INV i/p terminal quickly returns to the zero voltage level.

When o/p goes to $-V_{sat}$, the non-inv i/p terminal voltage is held at a (-ve) potential of :

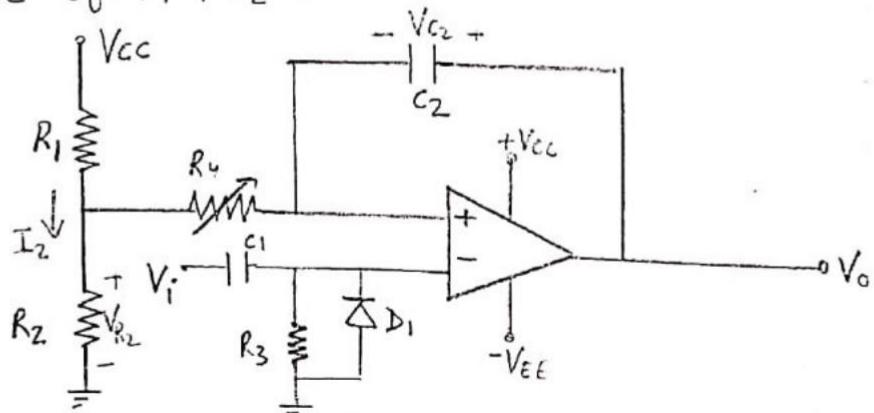
$$V_+ = -V_{sat} - V_{C_2}$$

- Now, capacitor C₂ discharges via R₁ and R₂, thus gradually raising the non-inv i/p terminal toward ground level.

When non-inv i/p terminal voltage goes slightly above ground, the op-amp o/p immediately switches back to $+V_{sat}$ & ckt is return to its original state.

- The ckt produces a negative going o/p pulse each time it is triggered.

The pulse width (PW) of the o/p depends on C₂, V_{R₂}, & the resistance of R₁ & R₂.



- To control the pulse width (PW), a resistor R_4 can be included in the ckt as shown above.
- The total resistances in series with the capacitor is now $\{R_4 + (R_1 \parallel R_2)\}$.
usually, $R_4 \ggg (R_1 \parallel R_2)$
So that, the capacitor charge/discharge resistance is effectively R_4 .
- By adjusting R_4 , the charge/discharge time can be altered thus controlling the o/p pulse-width.

Design ⇒

(1). Let, $I_2 = 100 \times I_{B\max}$

(2). The vtg V_{R_2} is chosen to be in the range 0.5 to 1V

$$\therefore R_2 = \frac{V_{R_2}}{I_1}$$

(3). Applying KVL from V_{cc} , R_1 & R_2 :

$$V_{cc} - I_2 R_1 - \underbrace{I_2 R_2}_{V_{R_2}} = 0$$

$$\Rightarrow R_1 = \frac{V_{cc} - V_{R_2}}{I_2}$$

(4). $R_3 C_1 = 10 \cdot 1 \cdot \text{of } t$

$$\Rightarrow R_3 C_1 = 0.1 \text{f}\mu$$

$$\Rightarrow C_1 = \frac{0.1 \text{f}\mu}{R_3}$$

^(QY)
C₁ might be first selected much larger than stray capacitance

then, $R_3 = \frac{0.1 \text{f}\mu}{C_1}$

$$(5). R_3 = \frac{0.1 \times V_{BE}}{I_B(\text{max})}$$

$$(6). C_2 = \frac{Pw}{(R_1 \parallel R_2) \ln \left(\frac{E - E_0}{e - e_c} \right)}$$

Where, PW → derived o/p pulse width .

E → capacitor charging vtg .

E_0 → initial capacitor vtg before triggering

e_c → final capacitor vtg .

| |
|---------------------------|
| $E = V_{R_2} + V_{sat}$ |
| $E_0 = V_{R_2} - V_{sat}$ |
| $e_c = V_{sat}$ |

Q.10. Sketch the circuit of a second order low pass filter and explain its working.

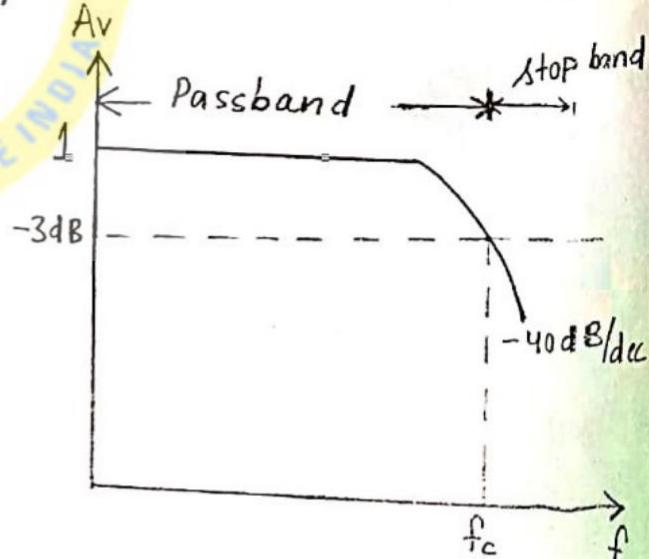
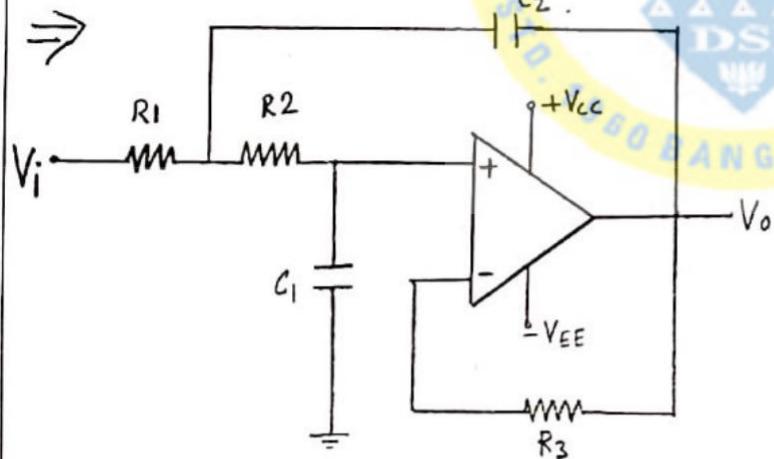


Fig. Second order LPF ckt

- In first-order low pass filter after cutoff frequency, the voltage gain decreases at the rate of 20 dB/decade.
- In second order low pass filter, after cutoff frequency, the voltage gain decreases at the rate of 40 dB/decade.

- Fig (a) shows a second order low pass filter, which has a frequency response that falls off at the rate of 40 dB per decade above the upper cut-off frequency.
- This steeper roll-off rate is achieved by using the $C_1 R_2$ together with feedback from the o/p via capacitor C_2 to the junction of R_1 and R_2 .
- At low frequencies, X_{C_1} & X_{C_2} are much larger than R_1 & R_2 and they have no effect on the ckt. So, the o/p voltage is equal to the i/p giving a voltage gain of 1 ($\therefore A_v = \frac{V_o}{V_i}$)
- At high frequencies, the effect of C_1 & R_2 causes the output to fall off at a rate of 20 dB per decade as the frequency increases.
- The $R_2 + C_1$ introduces a phase lag. The C_2 combined with $R_1 + R_2$ introduced a phase lead.
- The result of these phase difference is that the f/b via C_2 produces a further fall off of 20dB per decade. Thus second order LPF produces a fall-off of 40dB per decade.

Design steps:

$$(1) R_1 + R_2 = \frac{0.1 V_{BE}}{I_B (\text{max})}$$

$$(2) R_1 = R_2$$

$$(3). X_{C_1} = \sqrt{2} R_2 \text{ at } f_c$$

$$\therefore C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2}$$

$$(4). R_3 = R_1 + R_2$$

$$(5). C_2 = 2 C_1$$

$\checkmark D_{23}/S16$ good

Filters \Rightarrow

→ Filters are ckts that pass only a desired band of frequencies & attenuates the undesired band of frequencies.

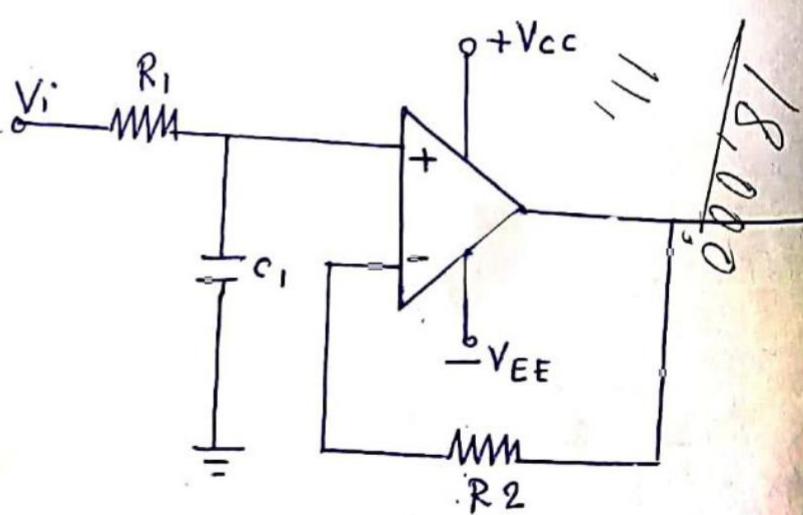
(i). First order - low-pass filter \Rightarrow

$$(i). R_1 = \frac{0.1 V_{BE}}{I_{B\max}}$$

$$(ii). R_1 = R_2$$

$$(iii) X_{C_1} = R_1 \text{ at } f_c$$

$$\therefore C_1 = \frac{1}{2\pi f_c R_1}$$

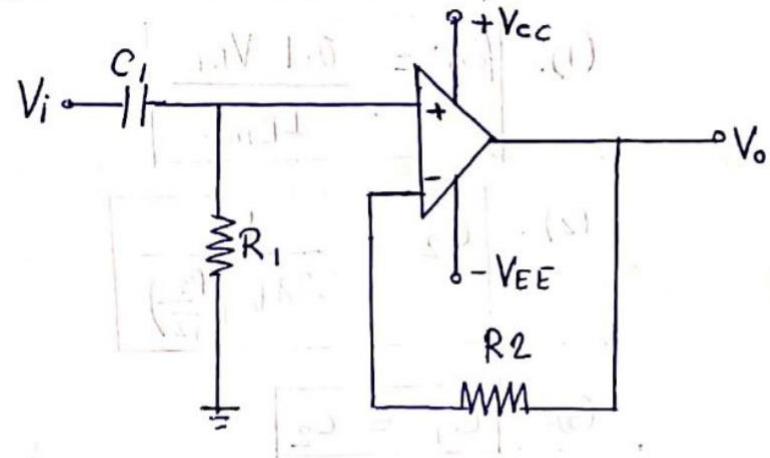


(2). first order high-pass active filters ⇒

$$(i) R_1 = \frac{0.1 V_{BE}}{I_{B\max}}$$

$$(ii) R_2 = R_1$$

$$(iii) C_1 = \frac{1}{2\pi f_c R_1}$$



(3). Second order low-pass active filters ⇒

$$(i) R_1 + R_2 = \frac{0.1 V_{BE}}{I_{B\max}}$$

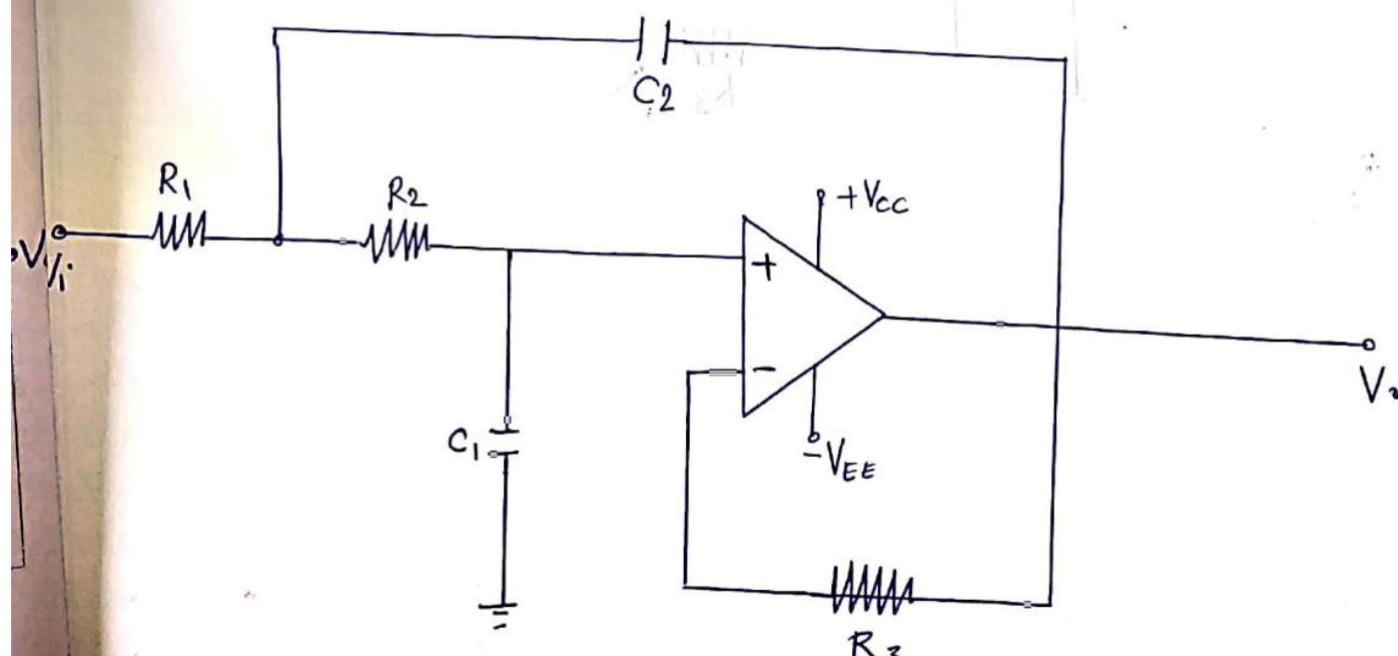
usually, $R_1 = R_2$

$$(ii) X_{C_1} = \sqrt{2} R_2 \text{ at } f_c$$

$$\therefore C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2}$$

$$(iii) R_3 = R_1 + R_2$$

$$(iv) C_2 = 2 C_1$$



(4). Second order high-pass filter

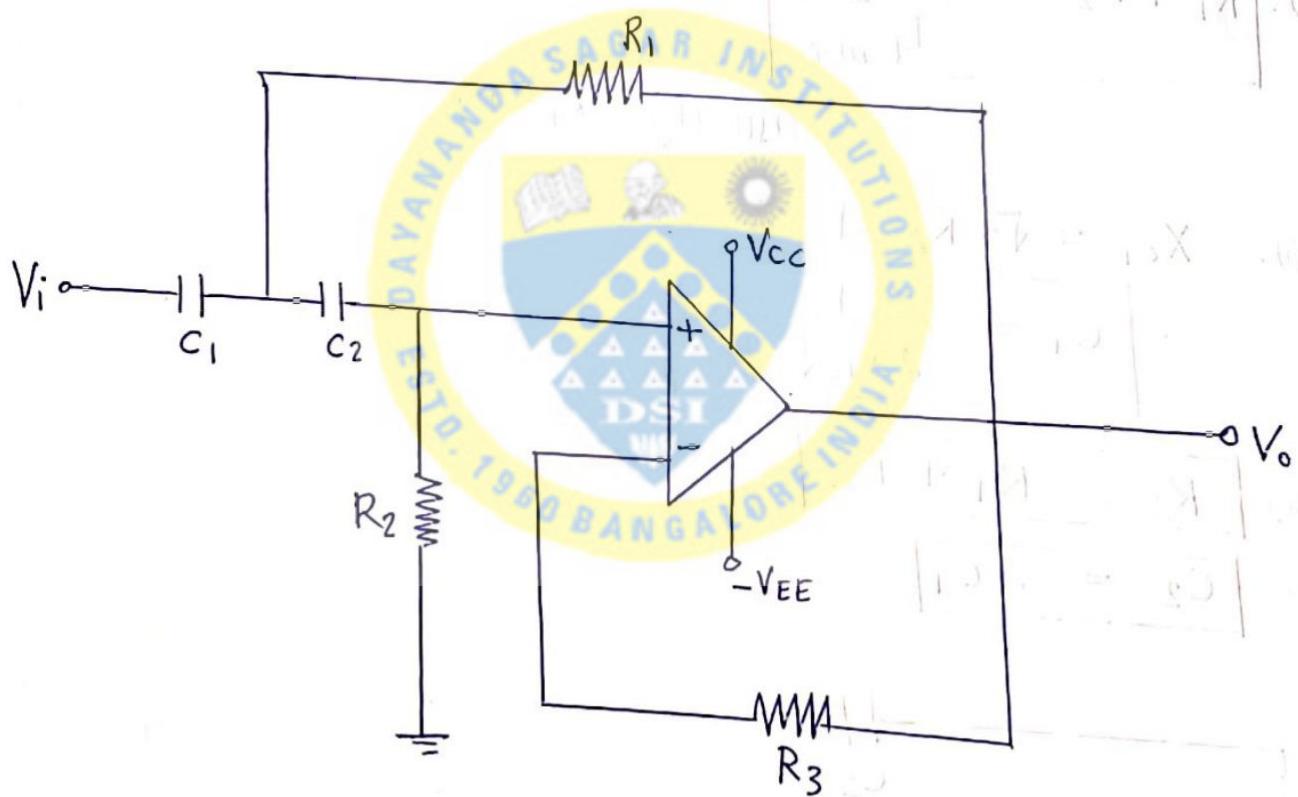
$$(1). R_2 = \frac{0.1 V_{BE}}{I_{B\max}}$$

$$(2). C_2 = \frac{1}{2\pi f_c \left(\frac{R_2}{\sqrt{2}} \right)}$$

$$(3). C_1 = C_2$$

$$(4). R_1 = \frac{R_2}{2}$$

$$(5). R_3 = R_2$$



Numericals \Rightarrow

Q.1. Using a 741 op-amp design a first order and low-pass filter to have a cutoff frequency of 1 kHz.

$$\Rightarrow f_c = 1 \text{ kHz}$$

$$\text{For 741 op-amp} \Rightarrow I_{B\max} = 500 \text{ nA}$$

$$\text{Assume, } V_{BE} = 0.7 \text{ V}$$

$$R_1 = \frac{0.1 V_{BE}}{I_{B\max}} = \frac{0.1 \times 0.7}{500 \text{ nA}} = 140 \text{ k}\Omega$$

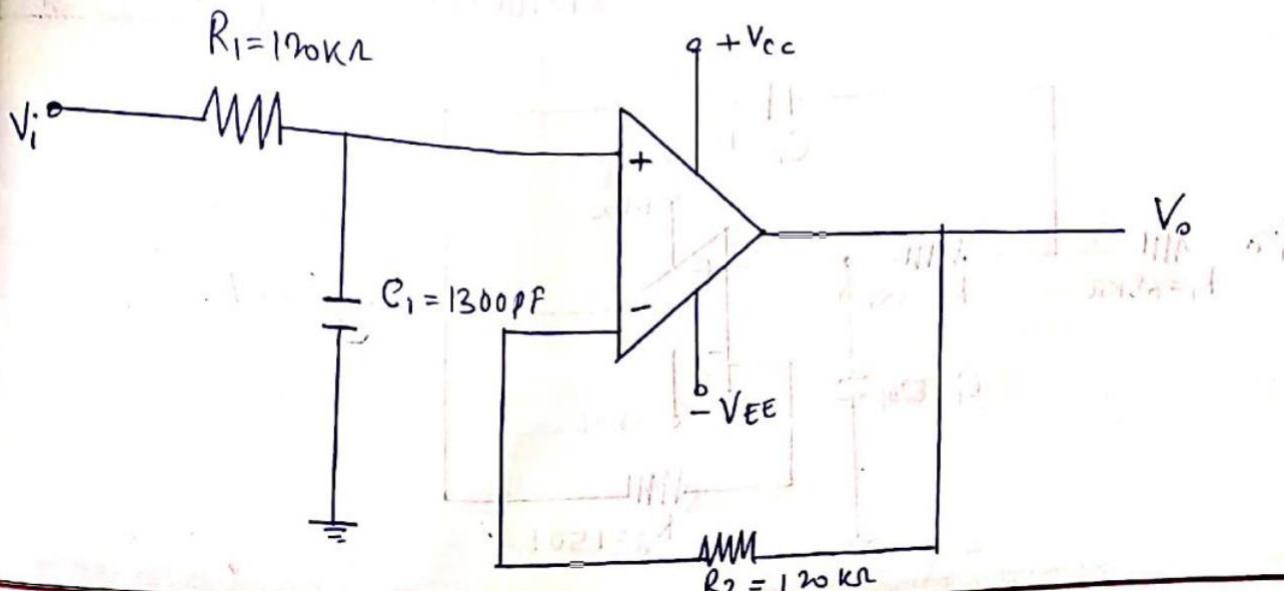
Standard value:

$$R_1 = 120 \text{ k}\Omega$$

$$R_2 = 120 \text{ k}\Omega = R_1$$

$$C_1 = \frac{1}{2\pi f_c R_1} = \frac{1}{2\pi \times 1 \text{ kHz} \times 120 \text{ k}\Omega} = 1326 \text{ pF}$$

$$\text{Standard value: } C_1 = 1300 \text{ pF}$$



Q.2 Design a ~~2~~ order ~~2~~ pass active filter for a cut-off frequency of 2 kHz.

$$\Rightarrow f_c = 2 \text{ kHz}$$

For 741 op-amp: $I_{B\max} = 500 \text{ nA}$

Assume, $V_{BE} = 0.7 \text{ V}$.

$$R_1 + R_2 = \frac{0.1 V_{BE}}{I_{B\max}} = \frac{0.1 \times 0.7}{500 \text{ nA}} = 140 \text{ k}\Omega$$

$$R_1 = R_2 = \frac{140 \text{ k}\Omega}{2} = 70 \text{ k}\Omega$$

Standard value:

| |
|----------------------------|
| $R_1 = 68 \text{ k}\Omega$ |
| $R_2 = 68 \text{ k}\Omega$ |

$$R_3 = R_1 + R_2 = 68 \text{ k}\Omega + 68 \text{ k}\Omega = 136 \text{ k}\Omega$$

Standard value:

$$R_3 = 150 \text{ k}\Omega$$

$$C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi \times 2 \text{ kHz} \times 68 \text{ k}\Omega \times \sqrt{2}} = 827.4 \text{ pF}$$

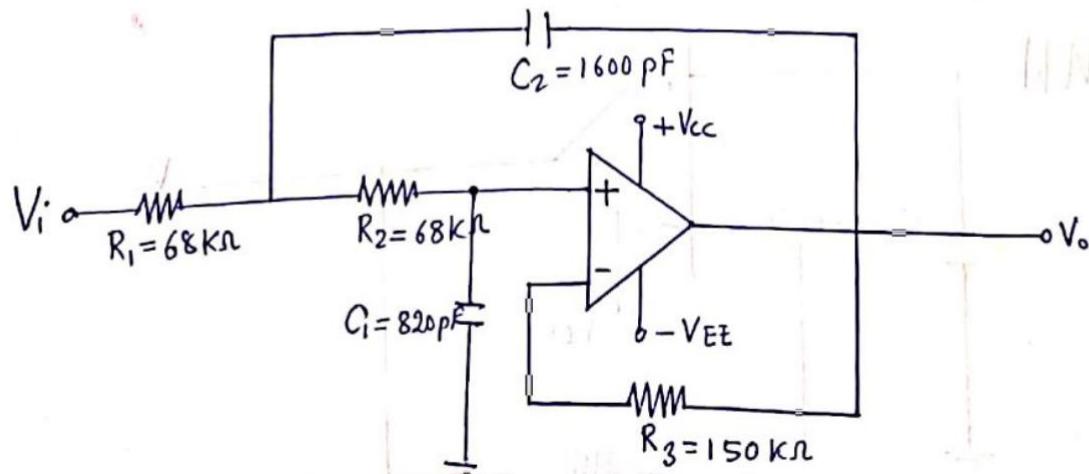
Standard value:

$$C_1 = 820 \text{ pF}$$

$$C_2 = 2C_1 = 2 \times 820 \text{ pF} = 1640 \text{ pF}$$

Standard value:

$$C_2 = 1600 \text{ pF}$$



Q.3. Design a second order high pass filter for a cut-off frequency of 4.5 kHz / 7 kHz

$$\Rightarrow f_c = 7 \text{ kHz}$$

For 741 IC, $I_{B\max} = 500 \text{ nA}$

$$V_{BE} = 0.7 \text{ V} \text{ (assume)}$$

$$R_2 = \frac{0.1 V_{BE}}{I_{B\max}} = \frac{0.1 \times 0.7}{500 \text{ nA}} = 140 \text{ k}\Omega$$

$$R_2 = 120 \text{ k}\Omega$$

$$R_1 = \frac{R_2}{2} = \frac{120 \text{ k}\Omega}{2} = 60 \text{ k}\Omega$$

$$R_1 = 56 \text{ k}\Omega$$

$$R_3 = R_2 = 120 \text{ k}\Omega$$

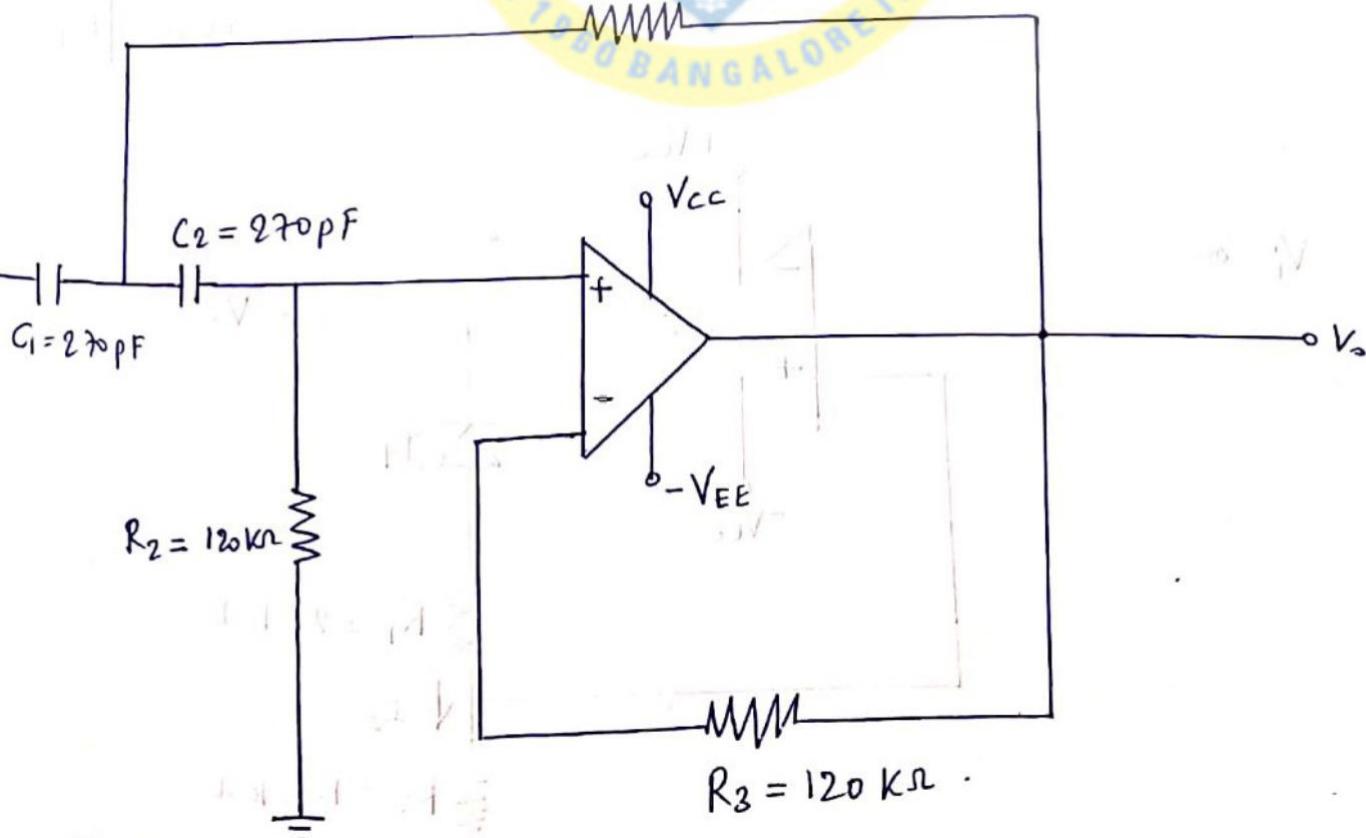
$$R_3 = 120 \text{ k}\Omega$$

$$C_2 = \frac{1}{2\pi f_c \cdot \left(\frac{R_2}{\sqrt{2}}\right)} = 267.9 \text{ pF}$$

$$C_2 = 270 \text{ pF}$$

$$C_1 = C_2 = 270 \text{ pF}$$

$$C_1 = 270 \text{ pF}$$



Q.4. An inv. schmitt trigger circuit is to have
 $U_{TP} = 0V$, $L_{TP} = 1V$.
 Design a suitable ckt using bipolar opamp
 with $\pm 15V$ supply.

$$\Rightarrow U_{TP} = 0V$$

$$|L_{TP}| = 1V$$

$$V_{cc} = 15V$$

$$-V_{EE} = -15V$$

Let, $I_2 = 500 \mu A$

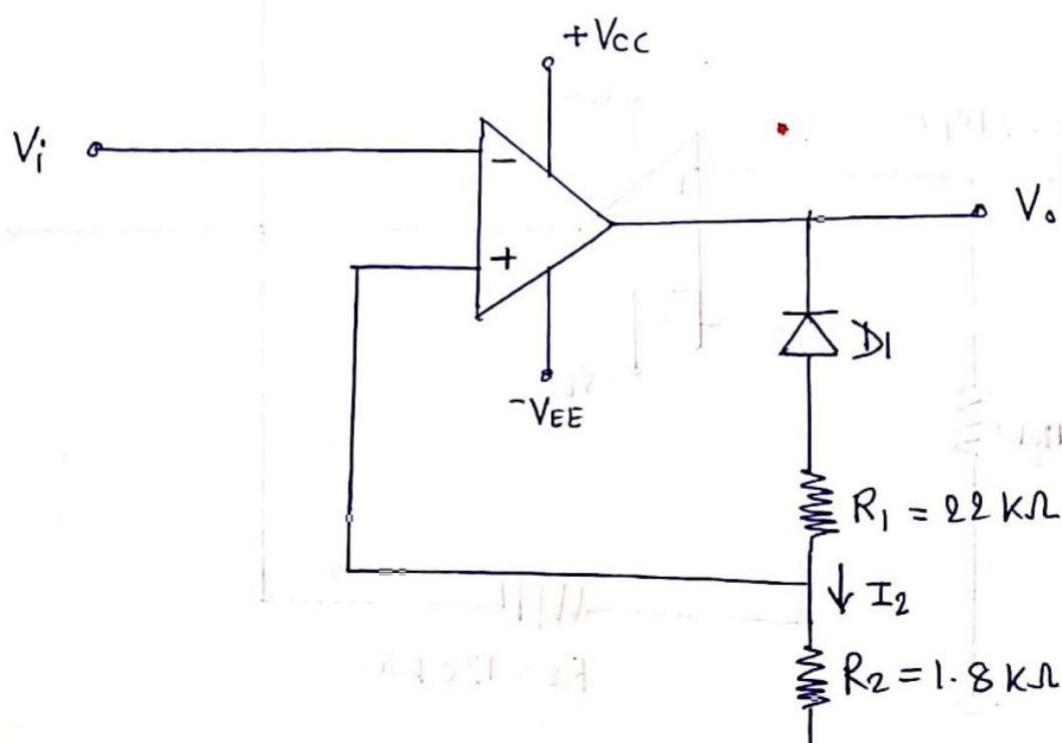
$$R_2 = \frac{V_{R_2}}{I_2} = \frac{L_{TP}}{I_2} = \frac{1V}{500 \mu A} = 2k\Omega$$

choose,
 $R_2 = 1.8 k\Omega$

Now, I_2 becomes $I'_2 = \frac{V_{R_2}}{R_2} = \frac{1V}{1.8 k\Omega} = 555.5 \mu A$.

$$\therefore R_1 = \frac{|-V_{EE} + 1| - V_F - L_{TP}}{I'_2} = \frac{|-15 + 1| - 0.7 - 1}{555.5 \mu A} = 22.14 k\Omega$$

choose,
 $R_1 = 22 k\Omega$



Q.5 Design an op-amp based MMV. to generate pulse of width $PW = 2 \text{ ms}$. The trigger is a pulse of amplitude $3V$ and duration 150 ms . Use a bipolar op-amp and a supply of $\pm 12V$.

$$\Rightarrow V_{CC} = 12V$$

$$PW = 2 \text{ ms}$$

$$V_{sat} = (V_{CC} - 1V) = 11V$$

$$-V_{sat} = (-V_{EE} + 1V) = -11V$$

$$V_i = 3V$$

$$t = 150 \text{ msec}$$

Now.

$$I_{Bmax} = 500 \text{ nA}$$

$$\text{let, } V_{R_2} = 0.5V$$

$$\text{let, } I_2 = 100 \times I_{Bmax} \Rightarrow I_2 = 50 \text{ nA}$$

$$R_2 = \frac{V_{R_2}}{I_2} = \frac{0.5V}{50 \text{ nA}} \Rightarrow R_2 = 10 \text{ k}\Omega$$

$$R_1 = \frac{V_{CC} - V_{R_2}}{I_2} = \frac{12V - 0.5V}{50 \text{ nA}} \Rightarrow R_1 = 230 \text{ k}\Omega \quad \Rightarrow \boxed{R_1 = 220 \text{ k}\Omega} \quad \text{choose:}$$

$$E = V_{R_2} + V_{sat} = 0.5V + 11V \Rightarrow E = 11.5V$$

$$E_o = V_{R_2} - V_{sat} = 0.5V - 11V \Rightarrow E_o = -10.5V$$

$$e_c = V_{sat} \Rightarrow e_c = 11V$$

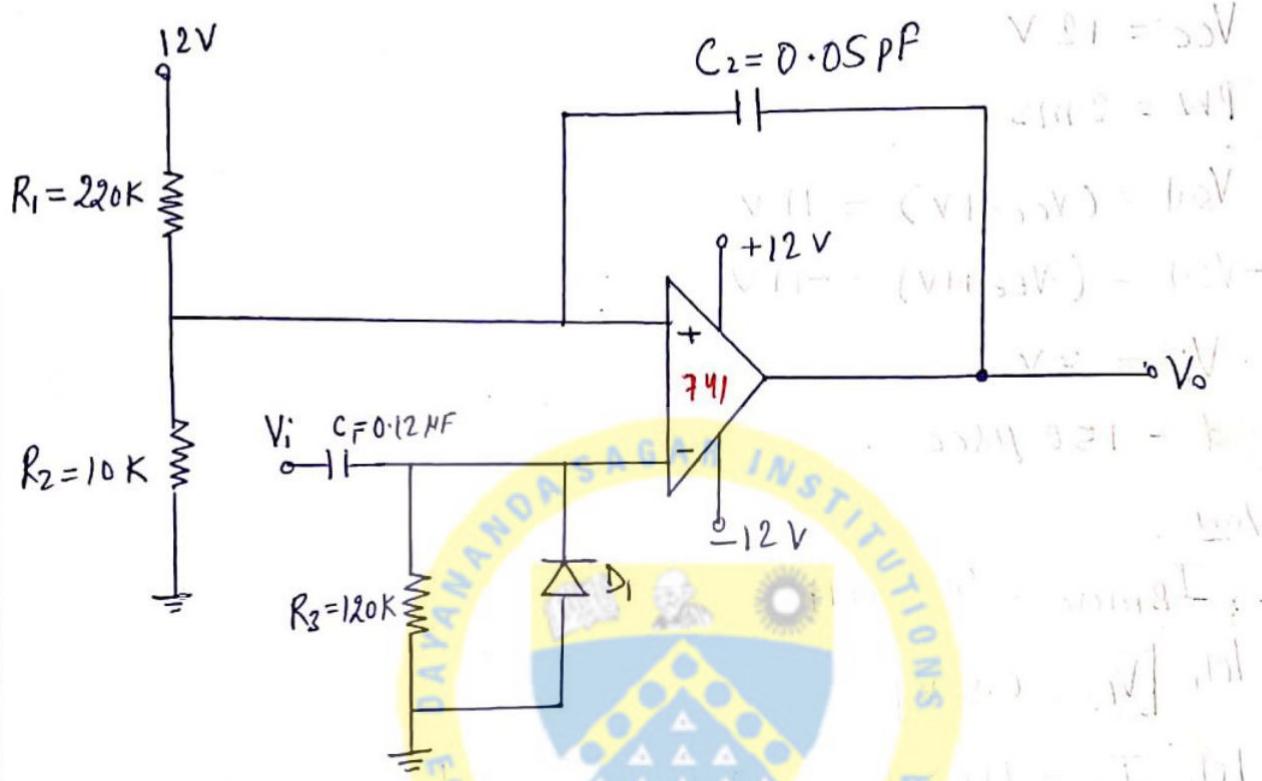
$$C_2 = \frac{PW}{(R_1 \parallel R_2) \cdot \ln \left(\frac{E - E_o}{E - e_c} \right)} = 0.052 \text{ nF} \quad \Rightarrow \boxed{C_2 = 0.05 \text{ nF}}$$

$$R_3 = \frac{0.1 V_{BE}}{I_{B\max}} = 140 \text{ k}\Omega$$

choose, $R_3 = 120 \text{ k}\Omega$

$$C_1 = \frac{0.1}{R_3} = \frac{0.1 \times 150 \text{ k}\Omega}{120 \text{ k}\Omega} = 0.125 \mu\text{F} \quad C_1 = 0.12 \mu\text{F}$$

Voltages across various components are as follows:



$$V_{IN} = 10 \text{ mV} \quad V_{OUT} = 10 \text{ mV} \quad V_{O/I} = 10 \text{ mV}$$

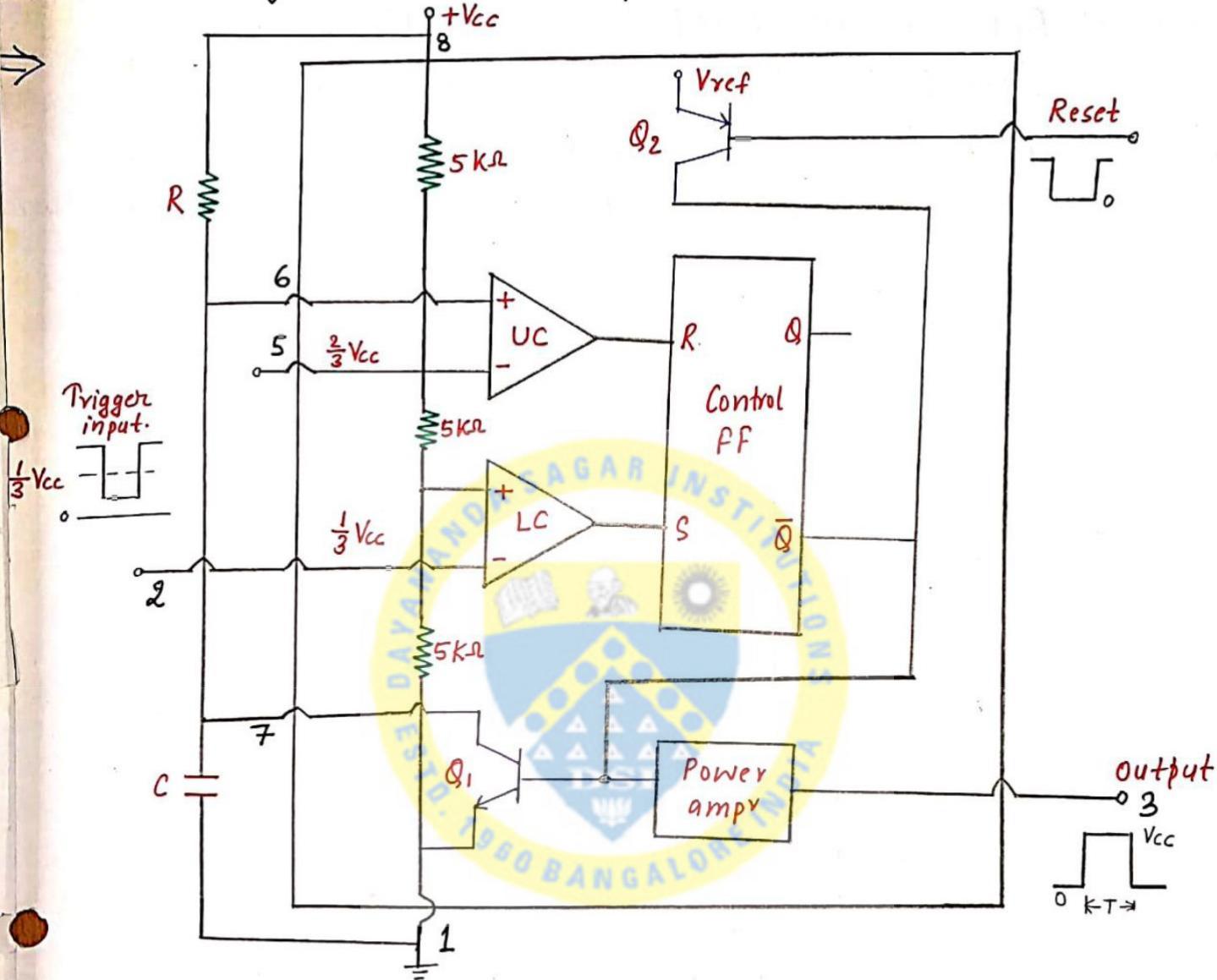
$$V_{IN} = 10 \text{ mV} \quad V_{OUT} = 10 \text{ mV} \quad V_{O/I} = 10 \text{ mV}$$

$$V_{IN} = 10 \text{ mV} \quad V_{OUT} = 10 \text{ mV} \quad V_{O/I} = 10 \text{ mV}$$

$$V_{IN} = 10 \text{ mV} \quad V_{OUT} = 10 \text{ mV} \quad V_{O/I} = 10 \text{ mV}$$

$$V_{IN} = 10 \text{ mV} \quad V_{OUT} = 10 \text{ mV} \quad V_{O/I} = 10 \text{ mV}$$

Q.1. Explain 555 timer Monostable multi-vibrator with relevant circuit diagram, waveforms and expressions.



- In stable state, FF holds transistor $Q_1 = \text{ON}$; thus clamping the external timing capacitor to ground. The o/p remaining at gnd potential. i.e. low.
- At $t=0$; the (-ve) trigger is applied at trigger i/p. As the trigger passes through $\frac{1}{3}V_{cc}$, the FF is set. $Q = 1, \bar{Q} = 0$.
- This makes the transistor $Q_1 = \text{off}$ and short ckt across the timing capacitor C is released.

- At $\bar{Q} = \text{low (0)}$, the O/P goes high i.e. V_{cc} . timing cycle now begins.
 - Since C is unclamped, it charges exponentially thru R towards V_{cc} with a time constant $RC \approx T$.
 - After a time period T_p , when the capacitor voltage just greater than $\frac{2}{3}V_{cc}$, the UC resets the FF.
 $R = 1$, $S = 0$, this makes $\bar{Q} = 1$.
 - Transistor Q_1 goes ON, thereby discharging the cap C , rapidly to ground.
- The output remains to stable states.

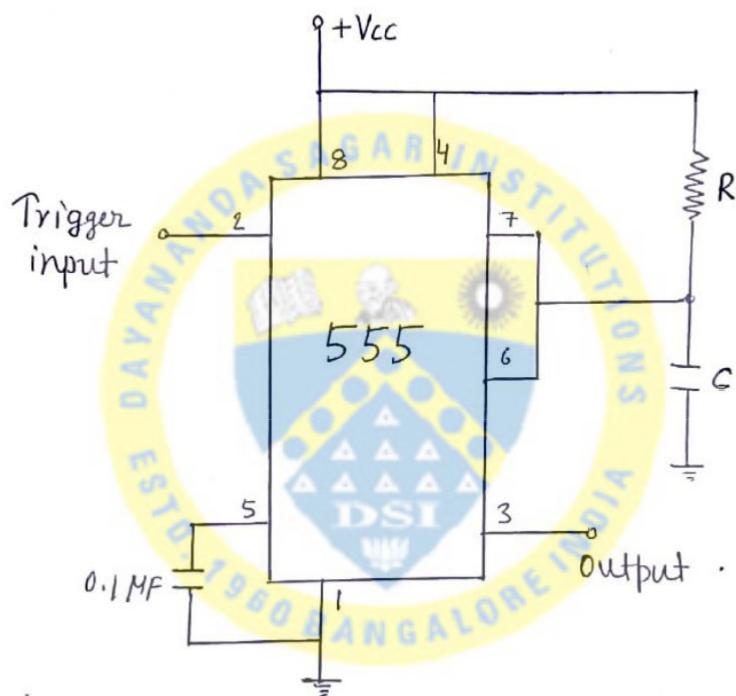


Fig. Monostable multivibrator.

The voltage across capacitor is :

$$V_C = V_{cc} \left(1 - e^{-\frac{t}{RC}}\right)$$

At, $t = T$,

$$V_C = V_{cc} \left(\frac{1}{3}\right) \leftarrow$$

$$\therefore \frac{2}{3} V_{cc} = V_{cc} \left(1 - e^{-\frac{T}{RC}}\right)$$

$$\Rightarrow T = RC \ln\left(\frac{1}{3}\right)$$

$$\Rightarrow \boxed{T = 1.1 RC} \text{ (seconds)}$$

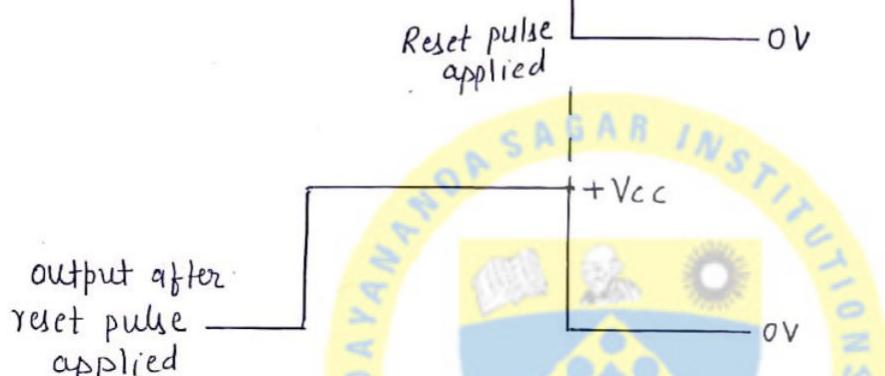
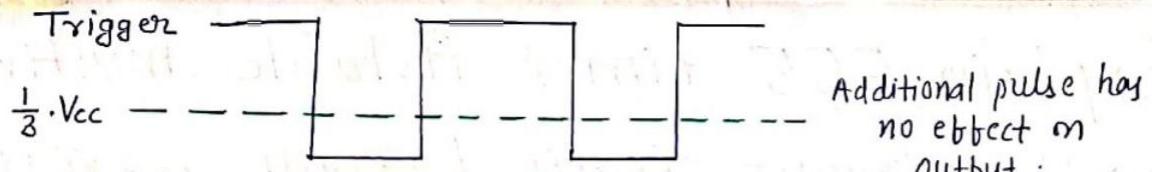


Fig. Timing pulse.

Applications in Monostable mode \Rightarrow

- (1). Missing pulse detector .
- (2). Linear Ramp generator .
- (3). Frequency divider .
- (4). Pulse - width modulation .

Q.2. Explain 555 timer Astable multivibrator with relevant circuit diagram, waveforms and expressions.

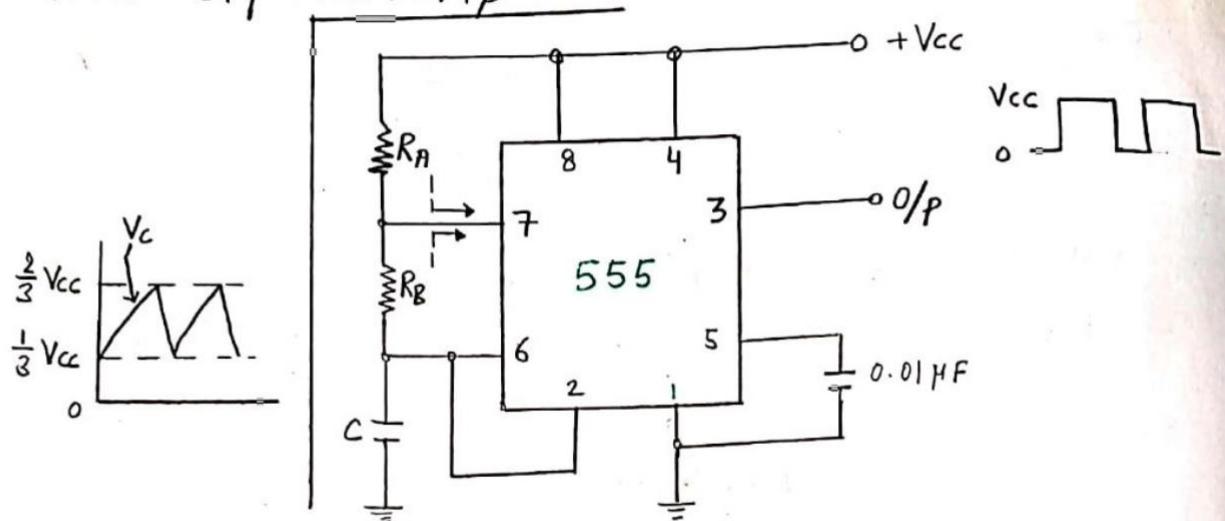


Fig. Astable multivibrator using 555.

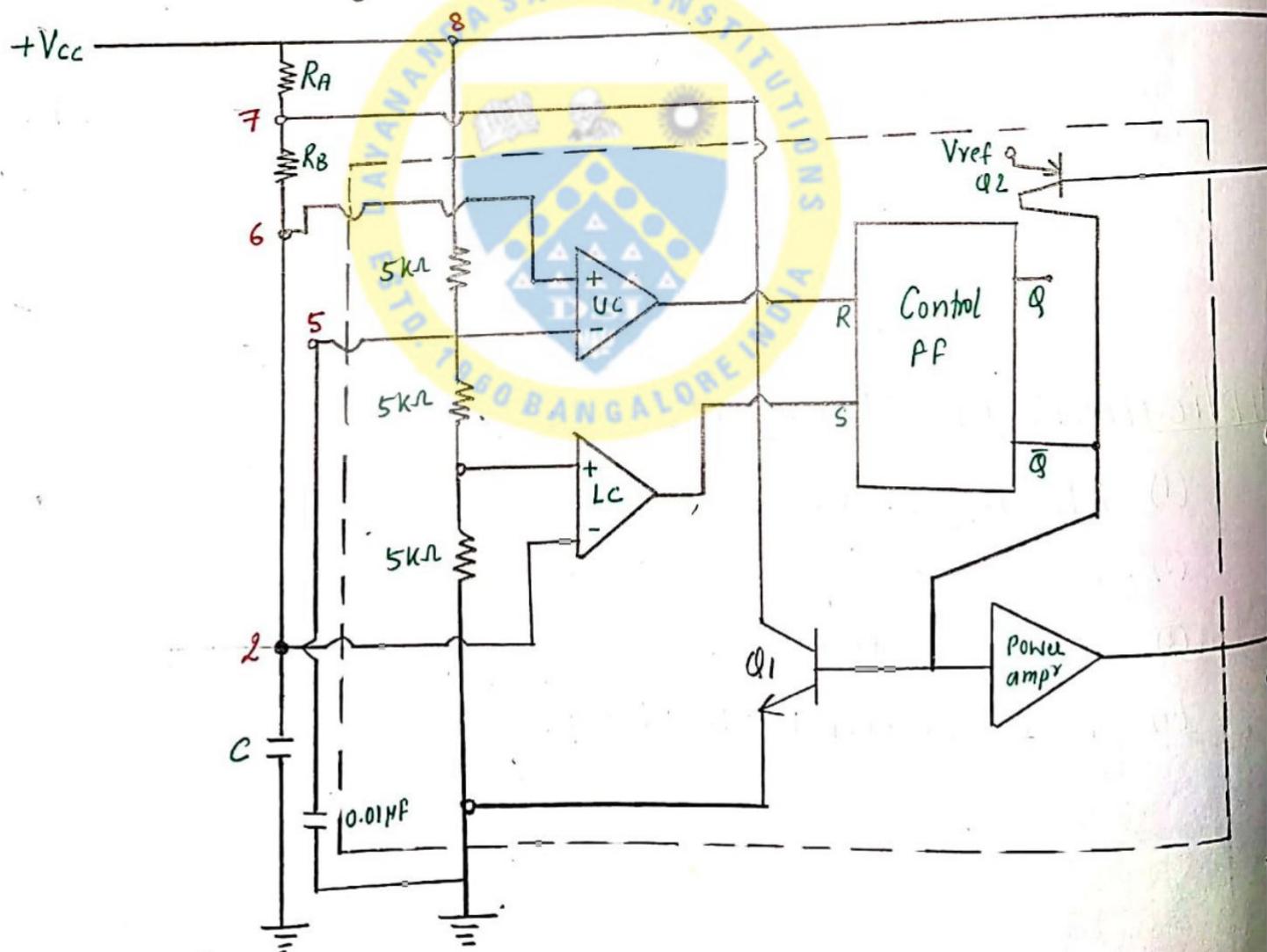


Fig Functional diagram of astable multivibrator using 555 timer.

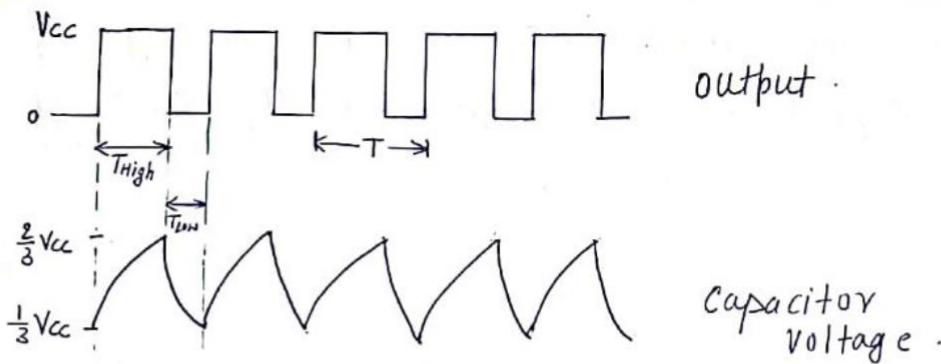


Fig. Timing sequence of A.M.V.

- Astable multivibrator is a rectangular wave generator circuit. This circuit does not require an external trigger to change the state of output (either high or low). Hence it is called free running MV.
- Comparing to MMV operation, the timing resistor is now split into 2 sections R_A and R_B . Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B .
- When the power supply V_{cc} is connected, the external timing capacitor C charges towards V_{cc} with time constant $(R_A + R_B) \cdot C$. During this time, pin 3 is High (V_{cc}). As net $R = 0$, $S = 1$, this makes $\bar{Q} = 0$ which undamps the timing capacitor C .
- When the capacitor voltage just reaches $\frac{2}{3}V_{cc}$, the upper comparator triggers the FF $\bar{Q} = 1$, this in turn, makes transistor $Q_1 = ON$ and capacitor C starts discharging towards ground through R_B and Transistor Q_1 with time constant $R_B \cdot C$.
- During the discharge of the timing capacitor C , as it reaches less than $\frac{V_{cc}}{3}$, the lower comparator is triggered. At this stage $S = 1$, $R = 0$ which turns

$\bar{Q} = 0$, unclamps the external timing capacitor.
The capacitor C thus, periodically charged & discharged b/w $\frac{2}{3} V_{CC}$ & $\frac{1}{3} V_{CC}$.

→ Charging time of capacitor:

$$T_C = T_{ON} = T_{High} = 0.693 [R_A + R_B] \cdot C$$

Discharging time of capacitor:

$$T_D = T_{OFF} = T_{Low} = 0.693 \cdot R_B \cdot C$$

$$\therefore T = T_{High} + T_{Low} \\ = 0.693 [R_A + 2R_B] \cdot C$$

→ Duty cycle $\Rightarrow \% D = \frac{T_{High}}{T} \times 100 \%$.

$$= \frac{0.693 [R_A + R_B] \cdot C}{0.693 [R_A + 2R_B] \cdot C} \times 100 \%$$

$$= \frac{R_A + R_B}{R_A + 2R_B} \times 100 \%$$

→ Frequency of oscillation \Rightarrow

$$f = \frac{1}{T} \\ = \frac{1}{0.693 [R_A + 2R_B] \cdot C}$$

$$= \left(\frac{1}{0.693} \right) \cdot \frac{1}{(R_A + 2R_B)C}$$

$$= \frac{1.45}{(R_A + 2R_B)C} \text{ Hz}$$

Application of Astable mode \Rightarrow

(1). FSK generator

(2). Pulse-position modulator

With neat block diagram, explain the operation of PLL.

Also define (i). Lock in range.

(ii). Capture range

(iii). Pull-in time.

PLL stands for Phase-locked loop.

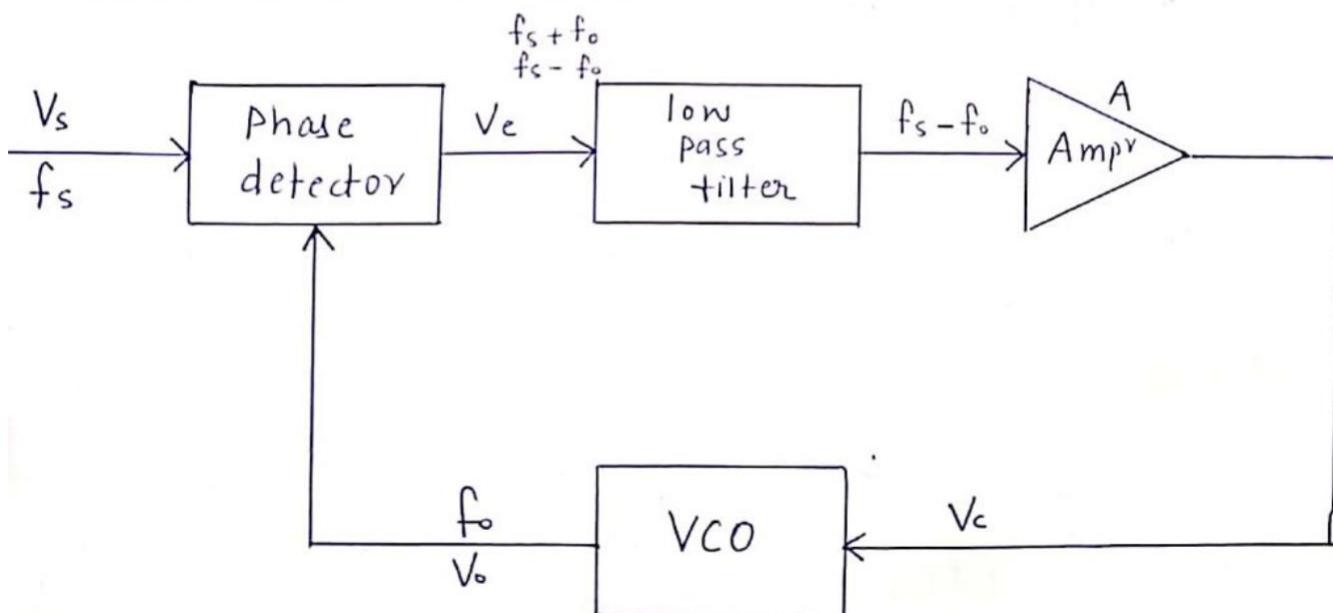
→ The PLL is an important building block of linear system.

→ PLL is basically a closed loop system designed to lock the o/p frequency and phase to freq. & phase of an input signal.

Applications ⇒

- (1). FM communication system.
- (2). Satellite communication system.
- (3). Electronic frequency control
- (4). Computers.

Block diagram of PLL ⇒



Operation of PLL

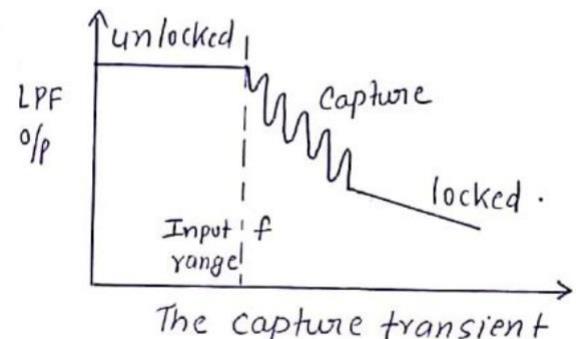
- If an i/p signal V_s of frequency f_s is applied to PLL, the phase detector compares the phase & frequency of the incoming signal to that of o/p V_o of the VCO.
- If the 2 signals differ in freq. or phase, an error voltage V_e is generated.
- The phase detector is basically a multiplier and produces the sum $[f_s + f_o]$ and difference $[f_s - f_o]$ components at its o/p.
- The high frequency ($f_s + f_o$) is removed by LPF and difference frequency component is amplified and then applied as control voltage V_c to VCO.
- The VCO is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage.
- VCO provide the linear relationship between applied voltage and oscillation frequency.
- Applied voltage is called control voltage; when control voltage is zero, VCO is in free running mode.
- Once this action starts, the signal is in capture range, the VCO continues to change frequency till its o/p frequency is exactly the same as the input signal frequency.
The circuit is then said to be locked.
- Once locked, the o/p frequency f_o of VCO is identical to f_s except for small phase difference.

→ This phase difference ϕ generates a corrective control voltage V_c to shift the VCO freq. from f_0 to f_s & thereby gain the lock.

→ Once locked, PLL tracks the frequency change of i/p signal.

→ Thus PLL goes through 3 stages.

- (1). Free running
- (2). Capture
- (3). Locked or tracking



1). lock-in-range ⇒

- When PLL is locked, it can track freqn' changes in incoming signal.
- The range of frequency over which the PLL can maintain the lock with the incoming signal, is called lock-in-range.
- The lock range is expressed as percentage of f_0 , the VCO freq.

2). Capture range ⇒

- The range of freqn' over which the PLL can acquire lock with an i/p signal is called capture range.
- This is also expressed as % of f_0 .

3). Pull-in-time ⇒

- The total-time taken by PLL to establish lock is called pull-in-time.
- This depends on the initial phase & frequency difference between two signals as well as on overall loop gain & filter character.

Q.4. Explain Balanced modulator type phase detector with relevant circuit diagram and waveforms.

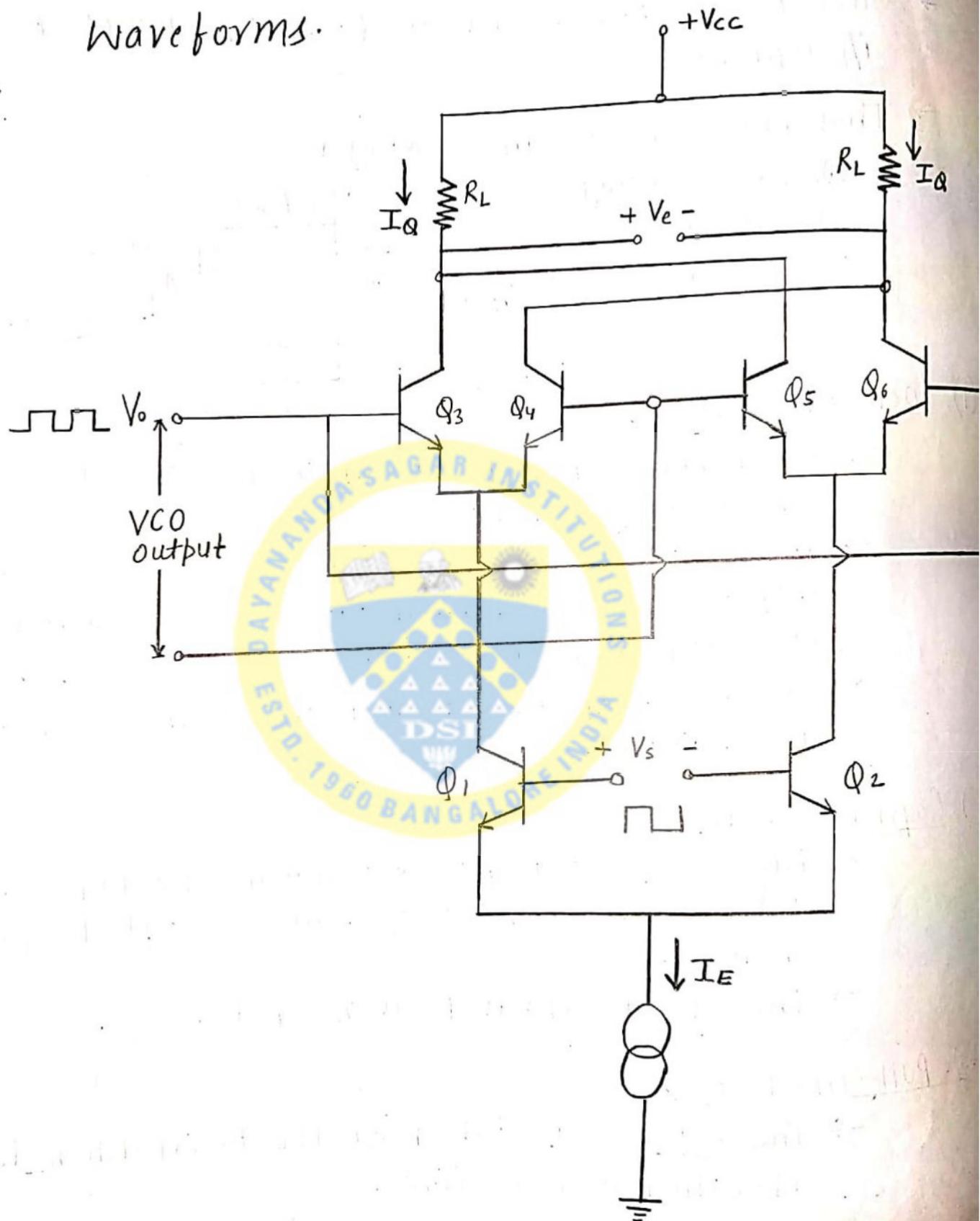


Fig. Ckt for balance modulator used as full-wave switching phase detectors.

P-6

→ There are two problems associated with the switch type phase detector:

- (1). The output voltage V_o is proportional to the input signal amplitude V_s . This is undesirable since it makes phase detector gain & loop gain dependent on the input signal amplitude.
- (2). The output is proportional to $\cos \phi$, not to ϕ making it non-linear.

→ The above limitation can be eliminated by making amplitude of input signal constant.

This can be achieved by converting sinusoidal signal into square wave input signal.

→ The input signal is applied to the differential pair Q_1 and Q_2 . Transistors Q_3 & Q_4 and Q_5 & Q_6 acts as a SPDT (single pole double throw) switches. These switches are controlled by o/p signal from VCO.

→ The amplitude of VCO signal and i/p signal are kept such that transistors are driven into saturation and cut-off is that they can acts as closed and open switches respectively.

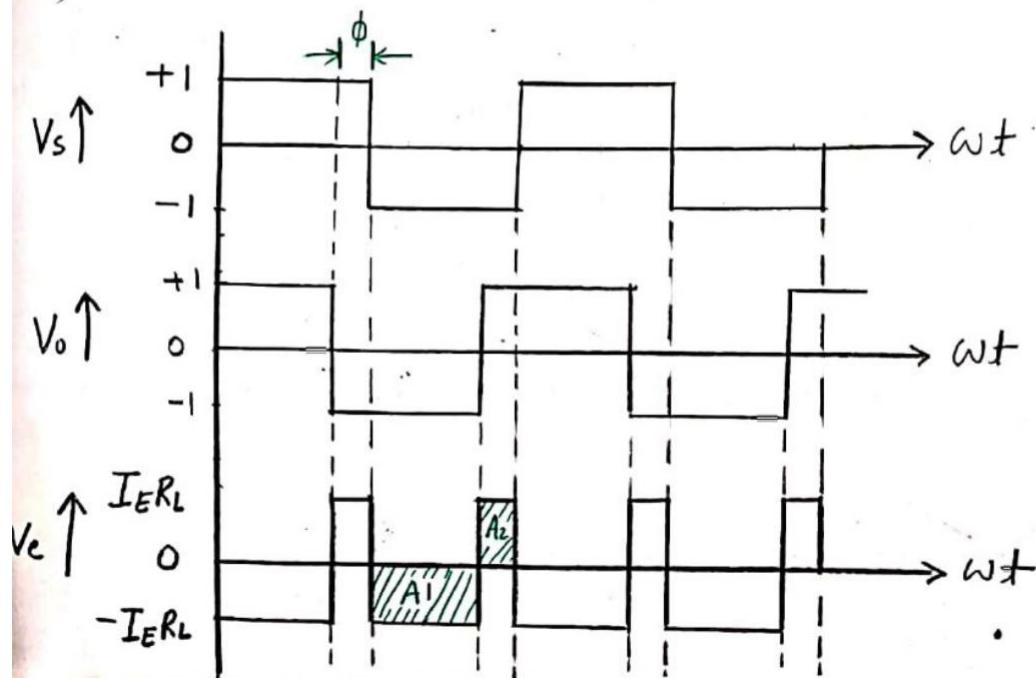


Fig. Timing diagram of i/p + o/p waveforms for balanced modulator ckt.

→ The waveform with phase shift of ϕ b/w I/P signal and VCO o/p signal.

V_s is (+ve) $\Rightarrow Q_1 = ON, Q_2 = OFF$.

V_s is (-ve) $\Rightarrow Q_1 = OFF, Q_2 = ON$.

Thus, when, V_o is (-ve) $\Rightarrow Q_3$ & Q_6 are off.

V_o is (+ve) $\Rightarrow Q_4$ & Q_5 are off.

→ The o/p voltage;

$V_e = -I_E \cdot R_L$ when Q_1 & Q_3 are ON.

Q_2 & Q_5 are ON.

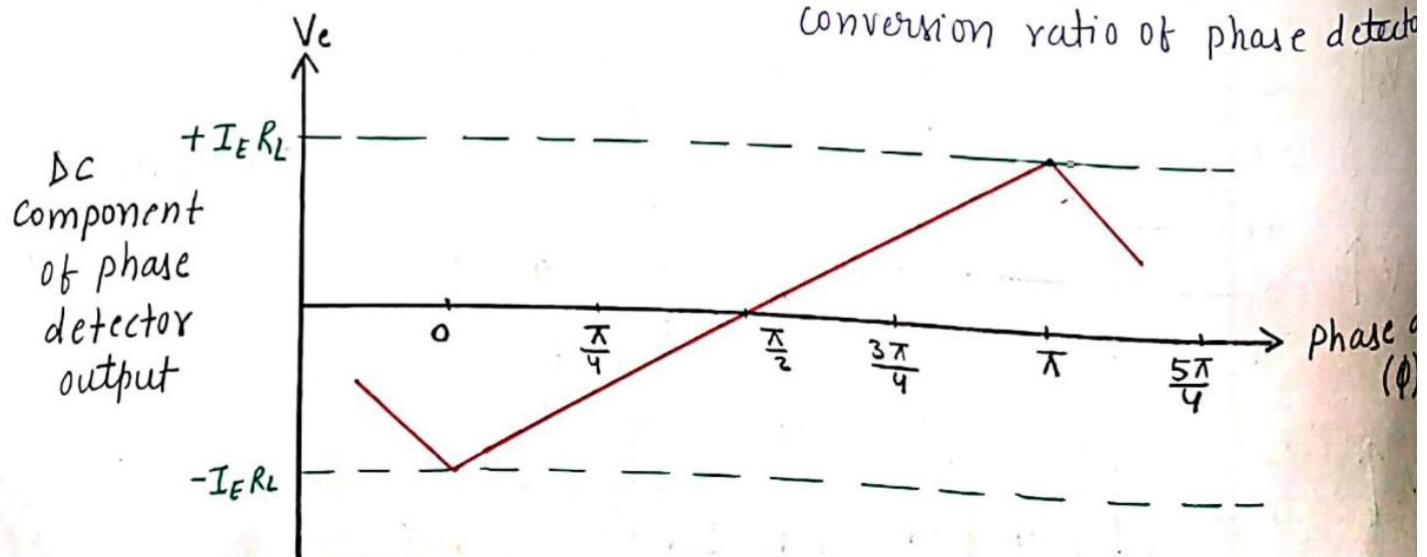
$V_e \rightarrow (+ve)$; either of Q_1 & Q_4 $\overset{ON}{\text{are ON}}$ or Q_2 & Q_6 $\overset{ON}{\text{are ON}}$

$V_e \rightarrow (-ve)$; either of Q_1 & Q_3 or Q_2 & Q_5 $\overset{ON}{\text{are ON}}$

→ The average value of phase detector output V_e can be calculated as:

$$\begin{aligned}
 (V_e)_{av.} &= \frac{1}{\pi} [\text{area } A_1 + \text{area } A_2] \\
 &= \frac{1}{\pi} [I_E R_L \phi + (-I_E R_L)(\pi - \phi)] \\
 &= I_E R_L \left(\frac{2\phi}{\pi} - 1 \right) \\
 &= \frac{4 I_Q R_L}{\pi} \left[\phi - \frac{\pi}{2} \right] \quad ; \quad I_E = 2 I_Q \\
 &= K_\phi \left[\phi - \frac{\pi}{2} \right].
 \end{aligned}$$

Where, K_ϕ is phase angle to the vt transfer coefficient or it is conversion ratio of phase detector.



Explain 566 VCO with relevant circuit diagram & waveform.

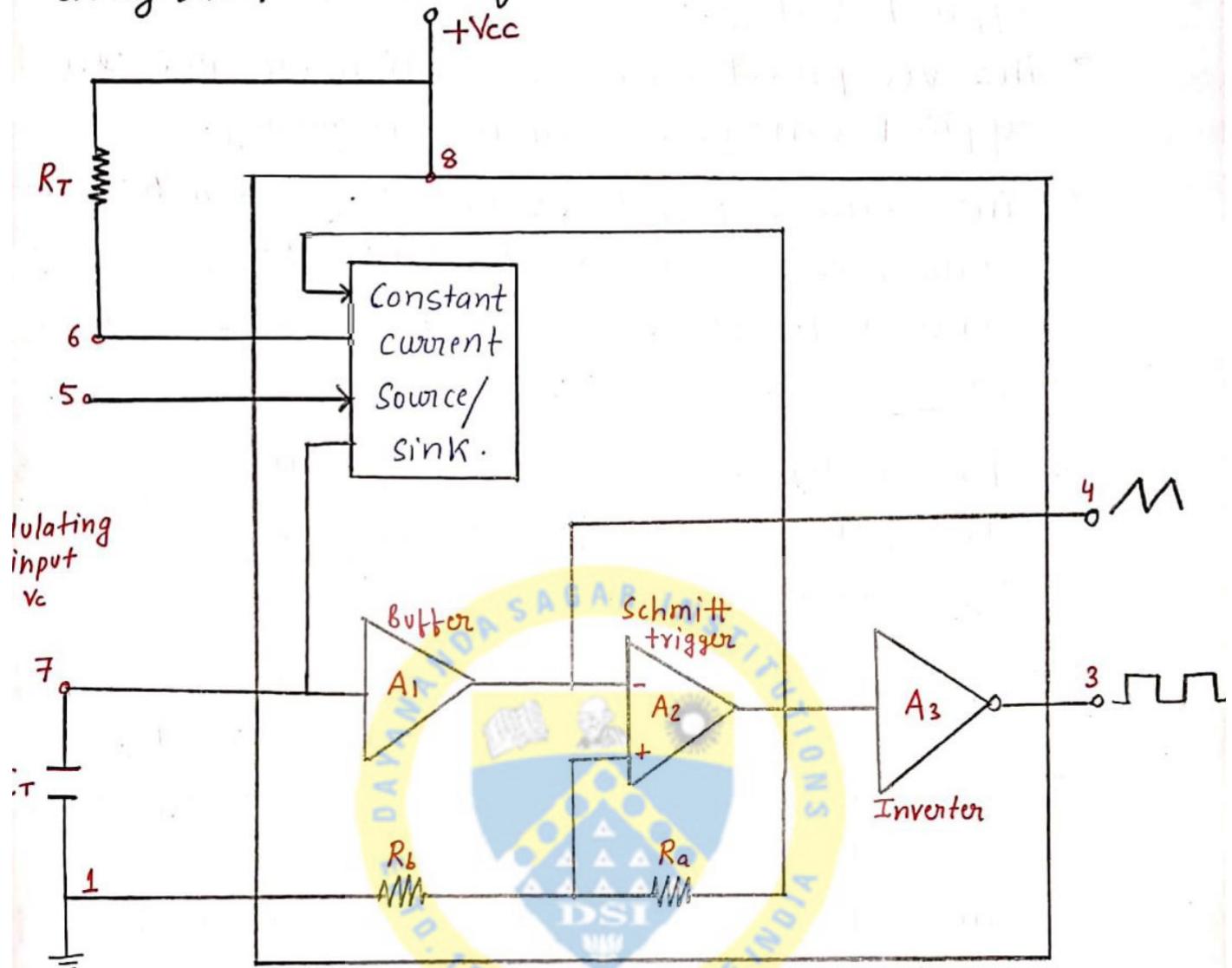


Fig. Block diagram of VCO

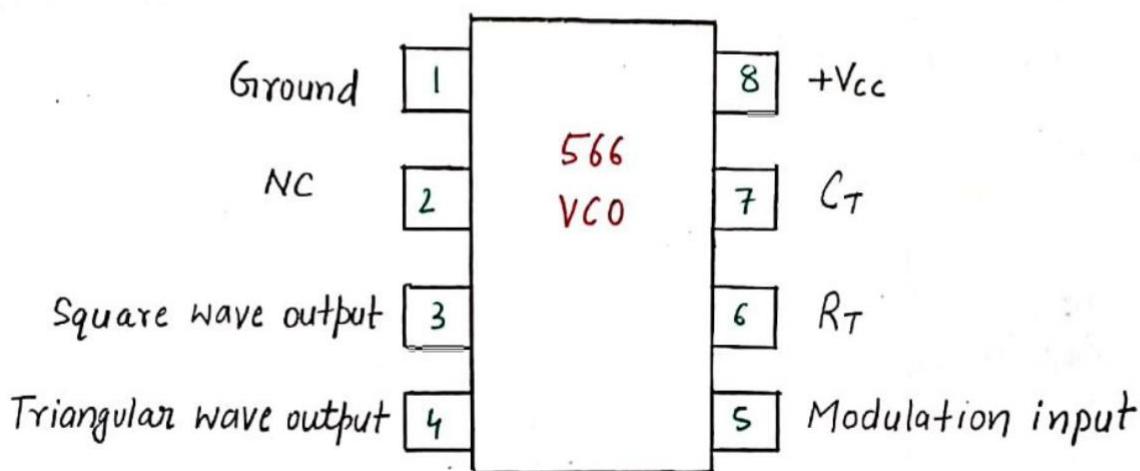
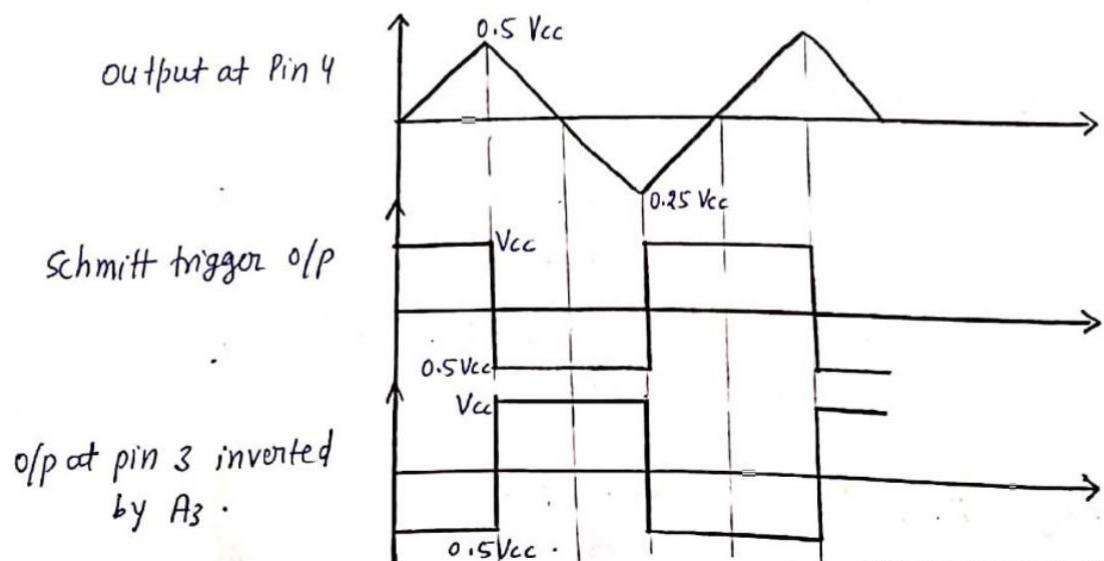


Fig. Pin configuration

- A VCO is an oscillator circuit in which the freq. of oscillations can be controlled by an applied voltage.
- The VCO provides linear relationship between the applied voltage & oscillation frequency.
- The control of ~~voltage~~ frequency with help of control voltage is called voltage to frequency conversion. Hence VCO is also called voltage to frequency conversion.
- Practically VCO is used to produce square or triangular waveform where frequency is controlled by control voltage.
- Op-amp A₁ is used as buffer and A₂ is used as Schmitt trigger and A₃ is used as inverter.
- The voltage V_c is applied to modulation i/p which is control voltage (Applied voltage).
- The capacitor is linearly charged & discharged constant current source.
- The charging current can be controlled by resistor R_T, which is external to IC.
- Charging & discharging levels are determined by the Schmitt trigger.



- The total voltage on the capacitor changes from $0.25 V_{cc}$ to $0.5 V_{cc}$. Thus $\Delta V = 0.25 V_{cc}$.
 The capacitor charges with a constant current source.

$$\frac{\Delta V}{\Delta t} = \frac{i^o}{C_T}$$

$$\Rightarrow \frac{0.25 V_{cc}}{\Delta t} = \frac{i^o}{C_T}$$

$$\Rightarrow \Delta t = \frac{0.25 V_{cc} \cdot C_T}{i^o}$$

- The time period T of the triangular waveform;
 $= 2 \cdot \Delta t$.

The frequency of oscillator f_o is;

$$f_o = \frac{1}{T}$$

$$= \frac{1}{2 \cdot \Delta t}$$

$$= \frac{i^o}{0.5 V_{cc} \cdot C_T}$$

But, $i^o = \frac{V_{cc} - V_c}{R_T}$

Where, $V_c = V_{tg}$ at Pin 5

$$\therefore f_o = \frac{2(V_{cc} - V_c)}{C_T \cdot R_T \cdot V_{cc}}$$

- The output frequency of the VCO can be charged either by (i). R_T ,
 (ii). C_T , or
 (iii) the voltage V_c at the modulating input terminal pin 5.

Q.6. Explain Op-amp D/A converter with R-2R resistor.

Calculate the analog output voltage for the digital input 100.

- ⇒ → To avoid the wide range of R_s used in weight resistor DAC, ladder type DAC is used, here only 2 values of R_s are required.
- The typical values are 2.5K to 10 kΩ.
- It is well suited for integrated circuit realization.
- For simplicity, consider a 3-bit DAC as shown, where the switch position d_1, d_2, d_3 corresponds to the binary word 100.

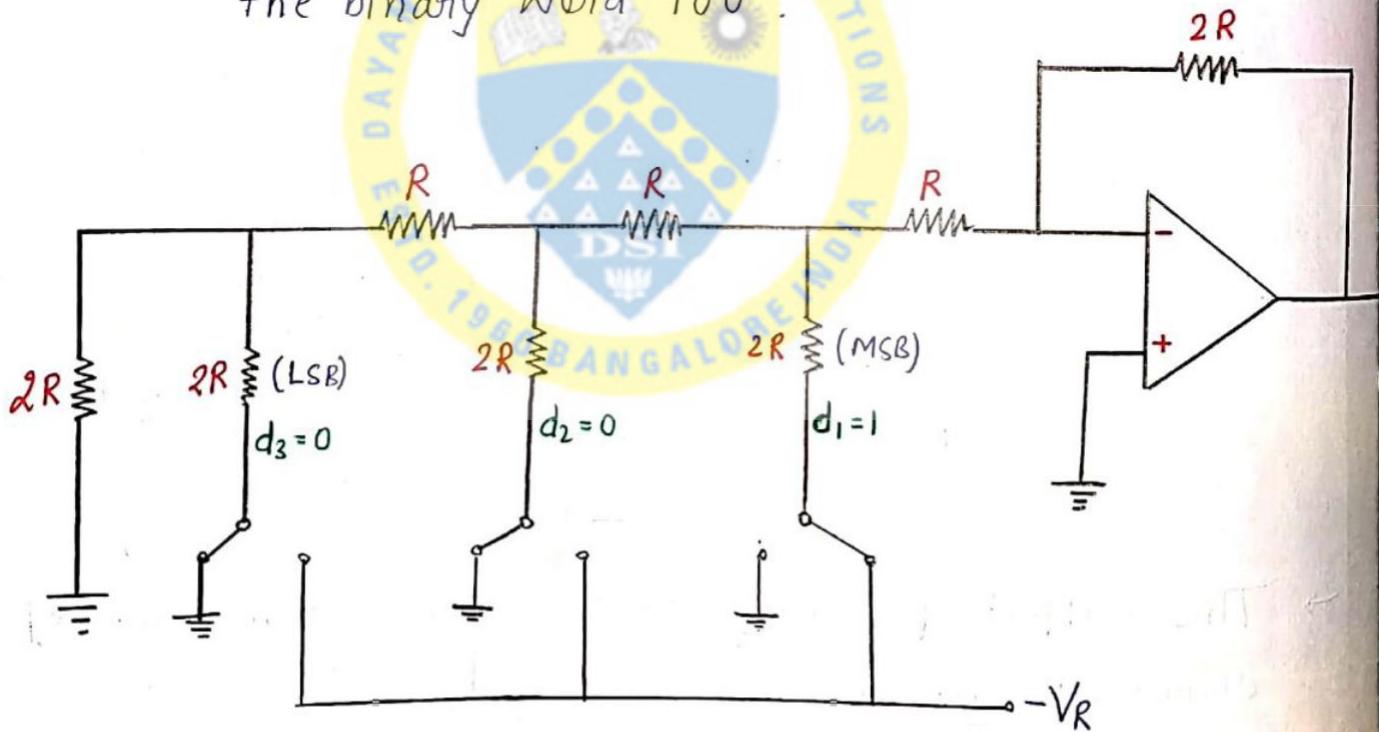


Fig.(a). R-2R ladder DAC.

- The circuit can be simplified to the equivalent form of fig (b) and finally to fig (c).

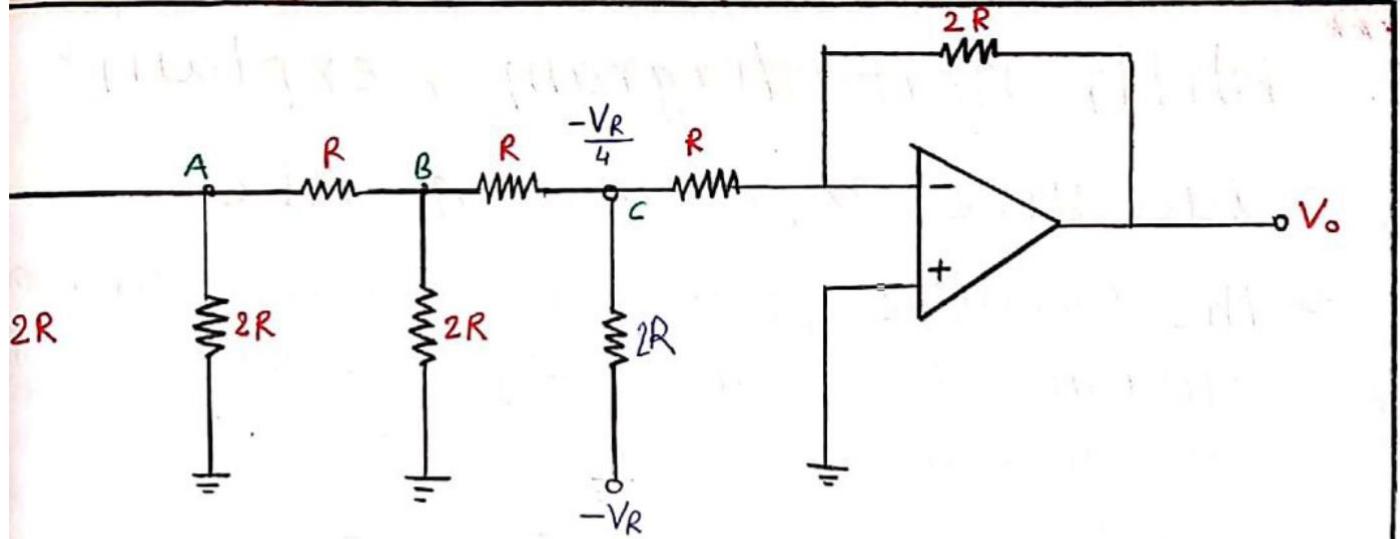


Fig. (b). Equivalent ckt.

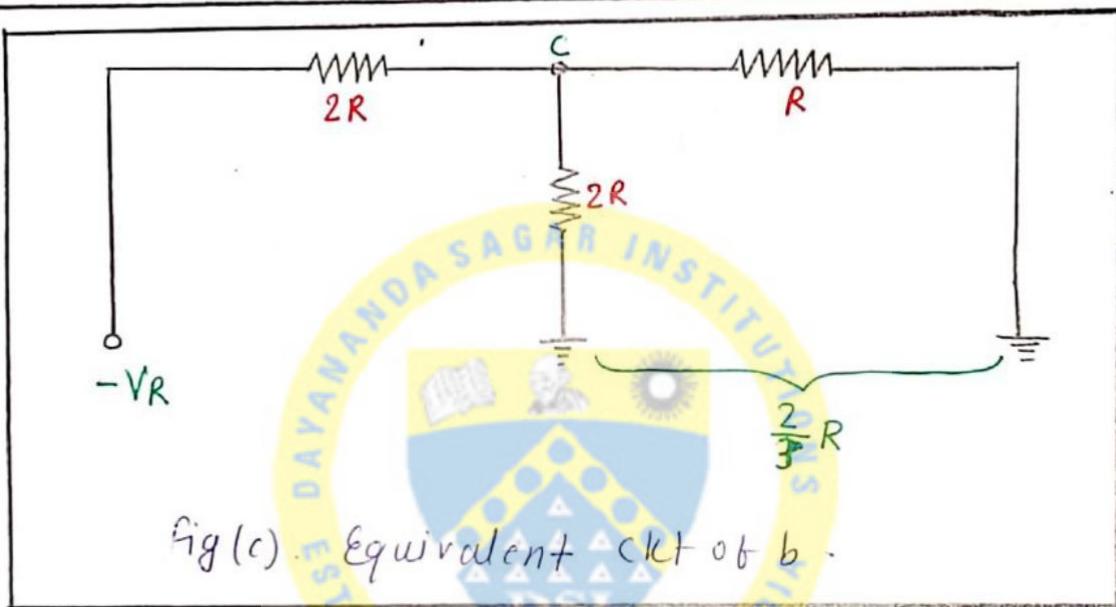


Fig (c) . Equivalent ckt of b .

→ Voltage at node C can be easily calculated by the procedure of network analysis as :

$$\frac{-V_R \left(\frac{2}{3}R \right)}{2R + \frac{2}{3}R} = -\frac{V_R}{4}$$

→ The output voltage is :

$$\begin{aligned} V_o &= -\frac{2R}{R} \left[-\frac{V_R}{4} \right] \\ &= \frac{V_R}{2} \\ &= \frac{V_{FS}}{2} \end{aligned}$$

Q.7. With neat diagram, explain successive approximation ADC.

→ The successive approximation technique uses an efficient code search strategy to complete n-bit conversion in just n-clock period.

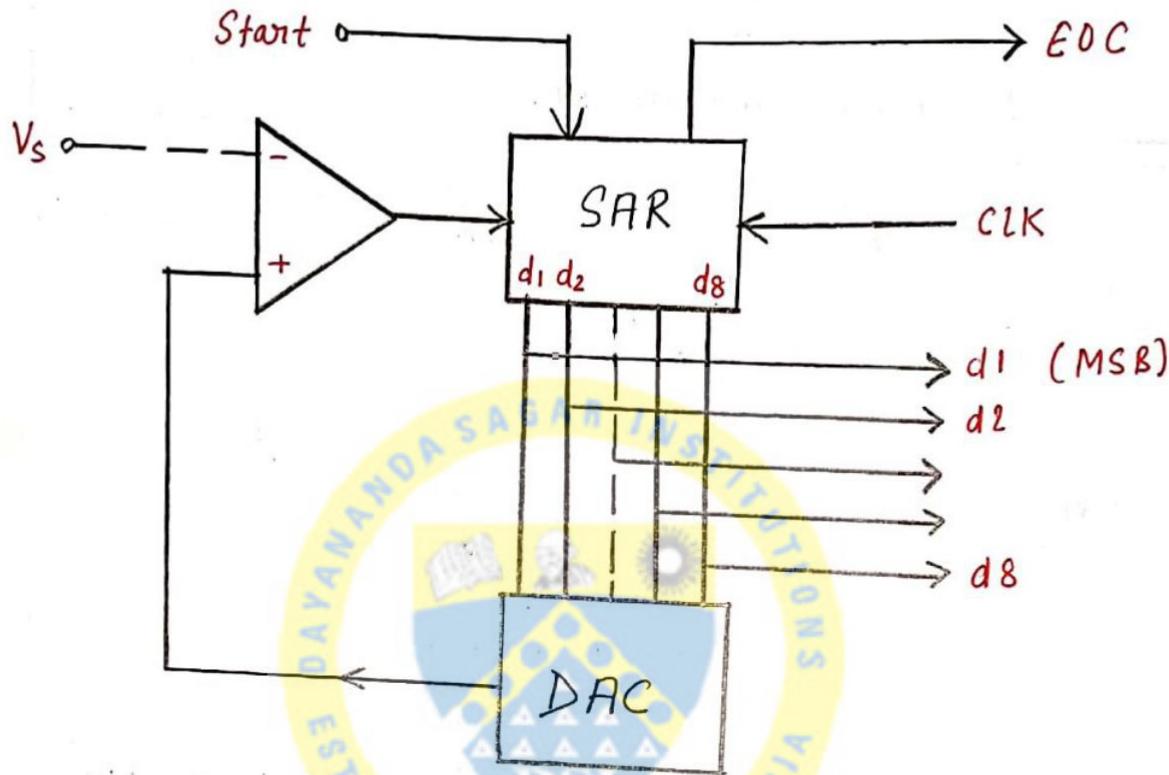


Fig. Functional diagram of the successive approximation ADC.

- The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error.
- The circuit operates as follows:
With the arrival of the START command, SAR sets the MSB $d_1 = 1$ with all other bits zero so that the trial code is 1000 0000.
- The output V_d of the DAC is now compared with analog input V_a .

- If V_a is greater than the DAC output V_d , then 10000000 is less than the correct digital representation.
- The MSB is left at '1' and the next lower significant bit is made '1' and further tested.
- However, if V_a is less than the DAC o/p V_d , then 10000000 is greater than the correct digital representation.
- So reset MSB to '0' and go on to the next lower significant bit.
- This process/procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.
- So it require a maximum of 8 pulse to convert the analog signal to digital for a 8-bit converter.
- Whenever the DAC o/p crosses V_a , the comparator changes state and this has been taken as the end of conversion (EOC) command.

| Correct Digital representation | Successive approximation register o/p V_d at different stages in conversion . | Comparator o/p |
|--------------------------------|---|--------------------|
| 11010100 | 10000000 | 1 (initial output) |
| | 11000000 | 0 |
| | 11100000 | 0 |
| | 11010000 | 1 |
| | 11011000 | 0 |
| | 11010100 | 1 |
| | 11010110 | 0 |
| | 11010101 | 0 |
| | 11010100 | |

Q.8. Explain binary - weighted technique of DA conversion .

What is its major drawbacks.

→

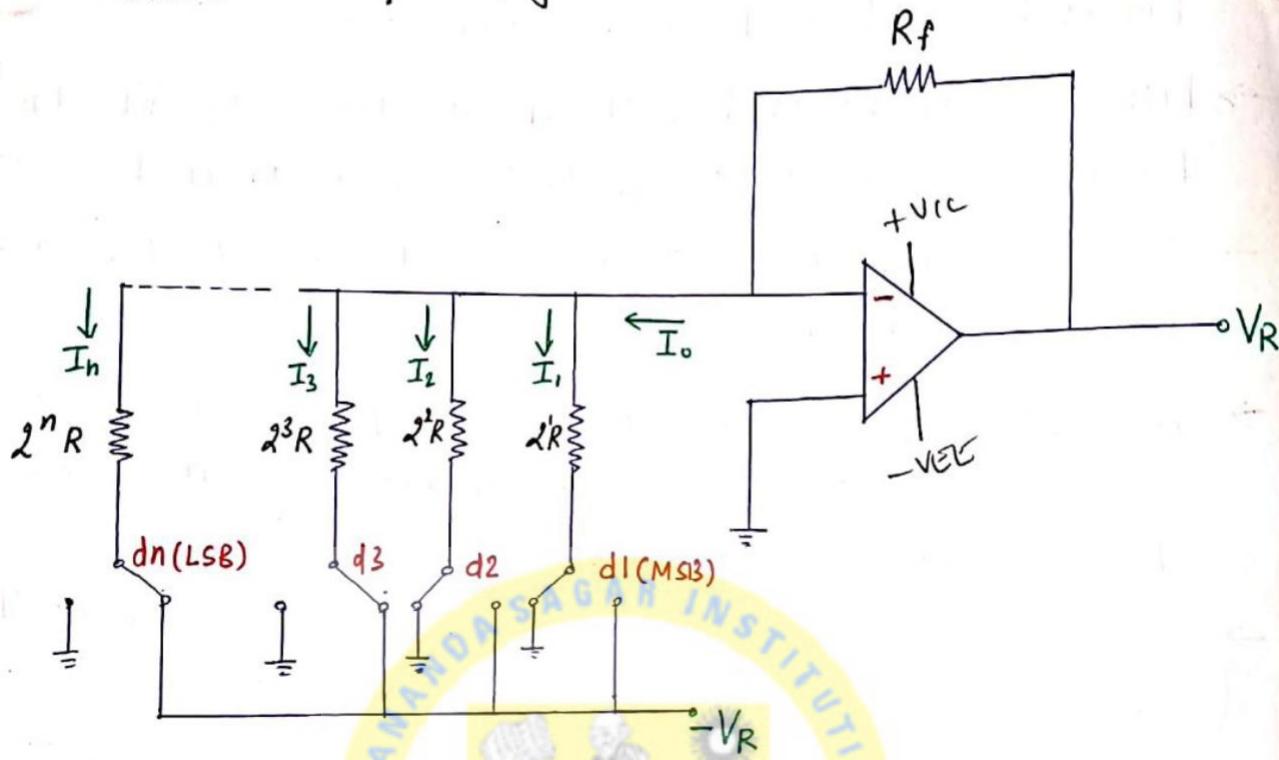


Fig. A simple weighted DAC .

→ In DAC, the n -bit binary word is combined with reference voltage V_R to give an analog o/p signal . The output of DAC can either a vtg or current .

Weighted - Register DAC ⇒

- It uses an inverting summing amp ckt with bin weighted register network
- It has n -electronic switches d_1, d_2, \dots, d_n controlled by binary input word .
- These switches are SPDT type (single pole double throw)
- If binary i/p is 1 , then that particular switch connects to $-V_R$.
- If binary i/p is 0 , then that particular switch connects to gnd .

→ Since the o/p is weighted binary (8421 code) the resistors are also weighted as $2^0 R, 2^1 R, \dots, 2^n R$ from MSB to LSB respectively.

Operation ⇒

→ Let, LSB switch is ON & connected to $-V_R$ and all switches are at 0 (gnd), then the current I_n only flows and all currents $I_{n-1}, I_{n-2}, \dots, I_1, I_0 = 0$.

∴ The o/p current is now:

$$I_o = I_n + I_B$$

$$\text{but } I_B = 0$$

$$e_g = 0$$

$$\Rightarrow I_o = I_n$$

$$\Rightarrow \frac{V_o - e_g}{R_F} = \frac{e_g - (-V_R)}{2^n R}$$

$$\Rightarrow \frac{V_o}{R_F} = \frac{V_R}{2^n R}$$

$$\Rightarrow \boxed{V_o = \frac{R_F \cdot V_R}{R} (2^{-n})} \quad \text{①}$$

→ Similarly, if all switches are in 1 state:

$$I_o = I_1 + I_2 + \dots + I_n$$

$$= \frac{V_R}{2^0 R} d_1 + \frac{V_R}{2^1 R} d_2 + \dots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]$$

$$\therefore V_o = \frac{V_R}{R} \cdot R_F [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]$$

$$If, R = R_F$$

$$\text{then } K = 1$$

$$V_{FS} = V_R$$

$$\Rightarrow \boxed{V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]}$$

Where, d_1, d_2, \dots, d_n are either 0 or 1 depending on binary i/p word.

Eg. for 3-bit:

$$V_o = V_R [2^{-1}d_1 + 2^{-2}d_2 + 2^{-3}d_3]$$

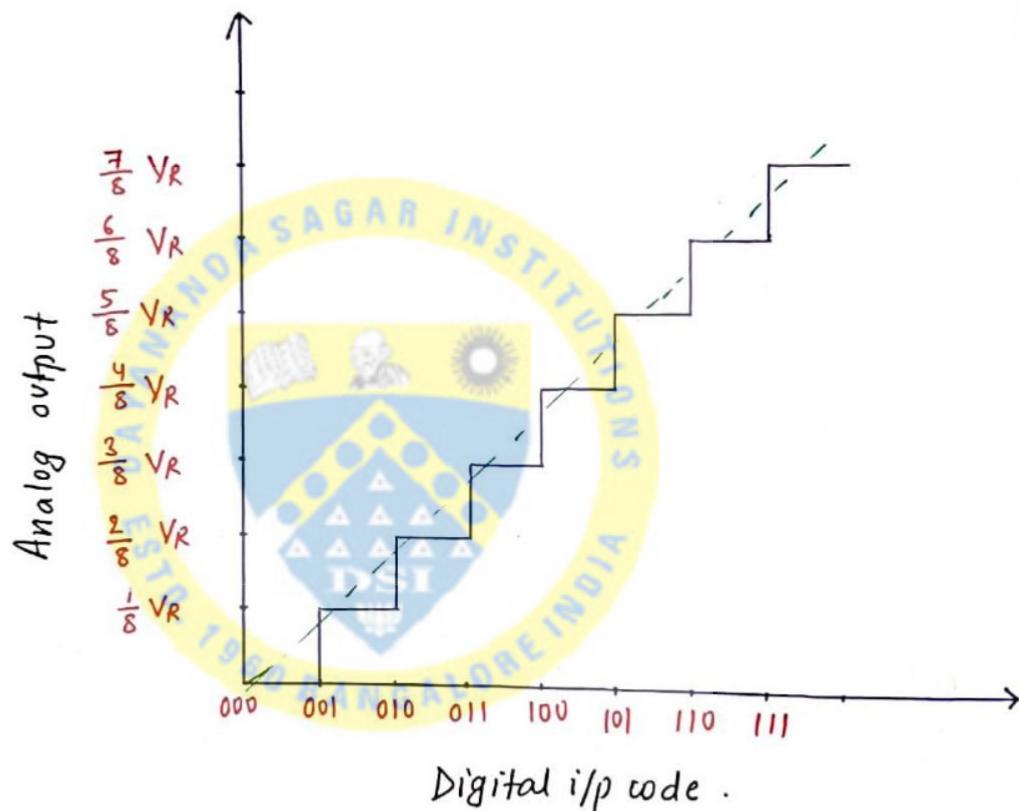
Hence, $d_1 \rightarrow \text{MSB}$
 $d_3 \rightarrow \text{LSB}$

for a digital word 101.

$$V_o = V_R [2^{-1}.1 + 2^{-2}.0 + 2^{-3}.1]$$

$$\Rightarrow V_o = \frac{5}{8} V_R$$

→ The accuracy and stability of DAC depends upon the accuracy of the resistors and tracking of each other with temperature.



Disadvantages ⇒

- (1). It requires wide range of resistor values.
eg. for 8 bit DAC, the largest resistor is 128 times.
- (2). Fabrication of large resistors in IC is impractical.
- (3). The accuracy of DAC depends on accuracy of resistor value and change in them depending on temperature.
- (4). The voltage drop across such a large R due to I_B also affects accuracy.
- (5). To achieve accurate resistor value of 2.5K, 5K, 10K, ... is highly difficult.

P-12

Design an astable multivibrator using 555 timer to obtain a square wave of frequency 5 kHz at 50% duty cycle.

$$\text{Duty-cycle} = 50\% = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

$$\Rightarrow \frac{1}{2} T_{ON} + \frac{1}{2} T_{OFF} = T_{ON}$$

$$\Rightarrow \frac{1}{2} T_{OFF} = T_{ON} - \frac{1}{2} T_{ON}$$

$$\Rightarrow \frac{1}{2} T_{OFF} = \frac{1}{2} T_{ON}$$

$$\Rightarrow \boxed{T_{OFF} = T_{ON}}$$

$$T = \frac{1}{f} = \frac{1}{5 \text{ kHz}} = 0.2 \text{ ms}$$

$$T = T_{ON} + T_{OFF}$$

$$\Rightarrow T = T_{ON} + T_{ON}$$

$$\Rightarrow T = 2 T_{ON}$$

$$\Rightarrow T_{ON} = \frac{T}{2} = \frac{0.2 \text{ ms}}{2} = 0.1 \text{ ms}$$

$$\therefore \boxed{T_{ON} = T_{OFF} = 0.1 \text{ ms}}$$

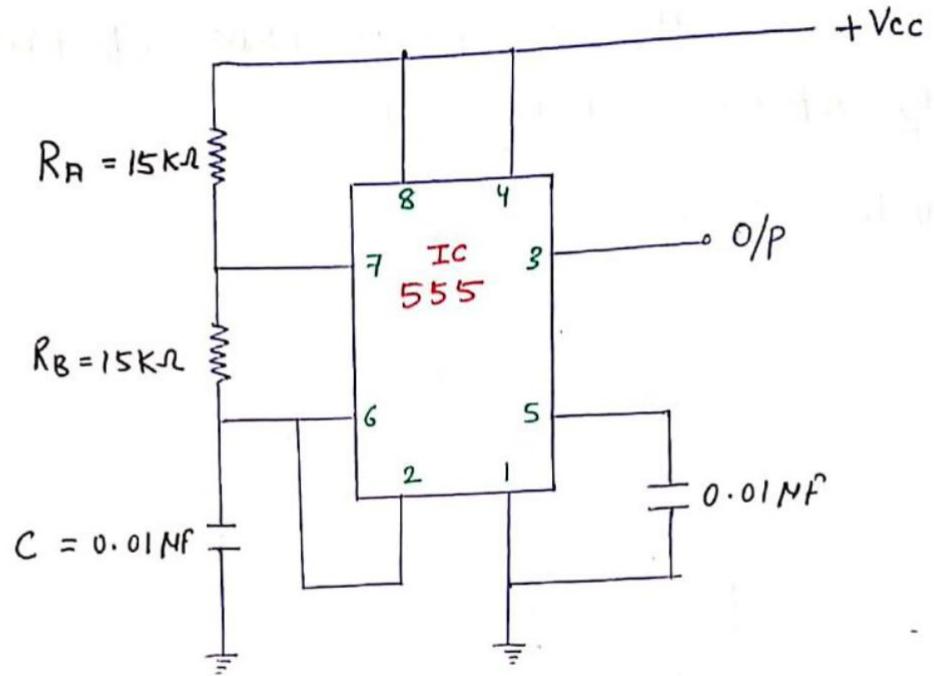
$$\text{But, } T_{ON} = T_{OFF} = 0.693 R_A C$$

$$\text{Let, } \boxed{C = 0.01 \mu F}$$

$$\begin{aligned} \therefore R_A &= \frac{T_{ON}}{0.693 \cdot C} \\ &= \frac{0.1 \text{ ms}}{0.693 \times 0.01 \mu F} \end{aligned}$$

$$= 14.43 \text{ k}\Omega$$

use, $\boxed{R_A = R_B = 15 \text{ k}\Omega}$ as standard value.



Q.10. What output voltage would be produced by a DAC whose O/P range is 0 to 10V and whose input binary number is:

- (i). 10 (2-bit DAC)
- (ii). 0110 (4-bit DAC)
- (iii). 10111100 (8-bit DAC)

\Rightarrow (i). 10 (2-bit DAC) \Rightarrow

$$\begin{aligned} \text{Step size} &= \frac{V_{\max}}{2^n - 1} \\ &= \frac{10}{2^2 - 1} \quad \left\{ (n=2 \text{ for 2-bit DAC}) \right\} \\ &= \frac{10}{3} \\ &= 3.33 \text{ V} \end{aligned}$$

$$\text{Digital data} = 1 \times 2^1 + 0 \times 2^0 = 2$$

$$\therefore V_o = D \times \text{step size} = 2 \times 3.33 \text{ V}$$

$$\Rightarrow V_o = 6.66 \text{ V}$$

(ii). 0110 \Rightarrow

$$\Rightarrow \text{Step-size} = \frac{V_{\max}}{2^n - 1}$$

$$= \frac{10}{2^4 - 1}$$

$$= \frac{10}{15}$$

$$= 0.666 \text{ V}$$

$$\text{Digital data} = 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$$

$$= 0 + 4 + 2 + 0$$

$$= 6.$$

$$\therefore V_o = D \times \text{step-size}$$

$$\Rightarrow V_o = 6 \times 0.666 \text{ V}$$

$$\Rightarrow V_o = 3.996 \text{ V}$$

$$\Rightarrow \boxed{V_o = 4 \text{ V}}$$

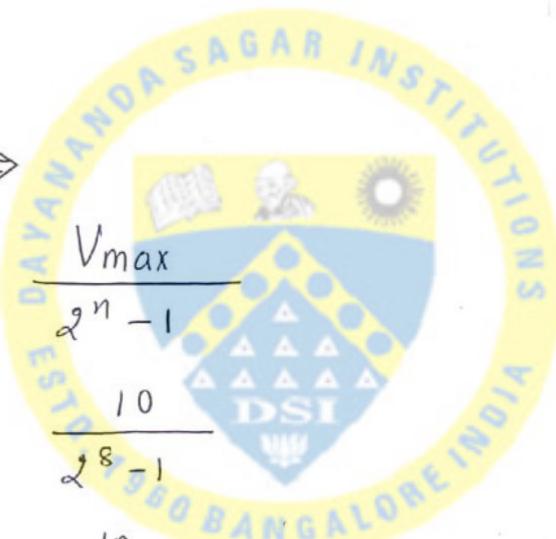
(iii). 10111100 \Rightarrow

$$\Rightarrow \text{Step-size} = \frac{V_{\max}}{2^n - 1}$$

$$= \frac{10}{2^8 - 1}$$

$$= \frac{10}{255}$$

$$= 0.03921 \text{ V}$$



$$\text{Digital data} = (1 \times 2^7) + (0 \times 2^6) + (1 \times 2^5) + (1 \times 2^4) * (1 \times 2^3) * (1 \times 2^2)$$

$$+ (0 \times 2^1) + (0 \times 2^0)$$

$$= 128 + 0 + 32 + 16 + 8 + 4 + 0 + 0$$

$$= 188.$$

$$\therefore V_o = D \times \text{step-size}$$

$$\Rightarrow V_o = 188 \times 0.03921 \text{ V}$$

$$\Rightarrow \boxed{V_o = 7.37 \text{ V}}$$

Q.11. What output voltage would be produced by a ADC whose output range is 0 to 10V and whose input binary number is

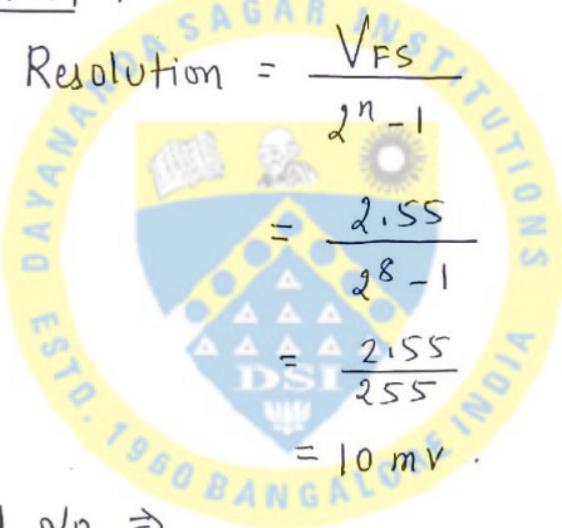
- (i). 10
- (ii). 1001
- (iii). 10110110

Q.12. An 8-bit ADC outputs all 1's when $V_i = 2.55V$

Find its (i). resolution in mV/LSB

(ii) Digital output when $V_i = 1.28V$

\Rightarrow (i). Resolution \Rightarrow

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$
$$= \frac{2.55}{2^8 - 1}$$
$$= \frac{2.55}{255}$$
$$= 10 \text{ mV}$$


(iii) Digital o/p \Rightarrow

$$V_o = \frac{V_i}{\text{Resolution}}$$

$$= \frac{1.28V}{10 \text{ mV}}$$

$$= 128$$



$$V_o = 1000 \ 0000$$

13. With a neat circuit diagram and staircase waveform, explain the operation of counter type analog-to-digital converter.

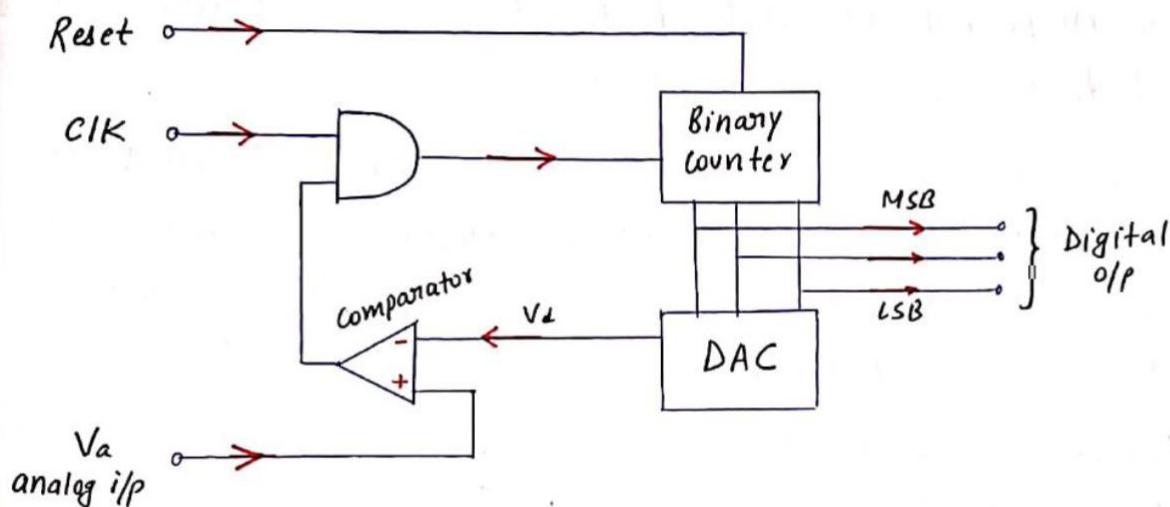
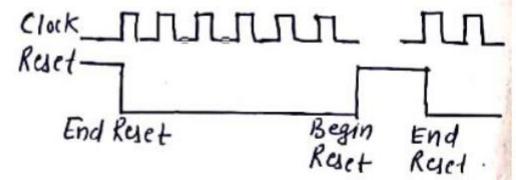
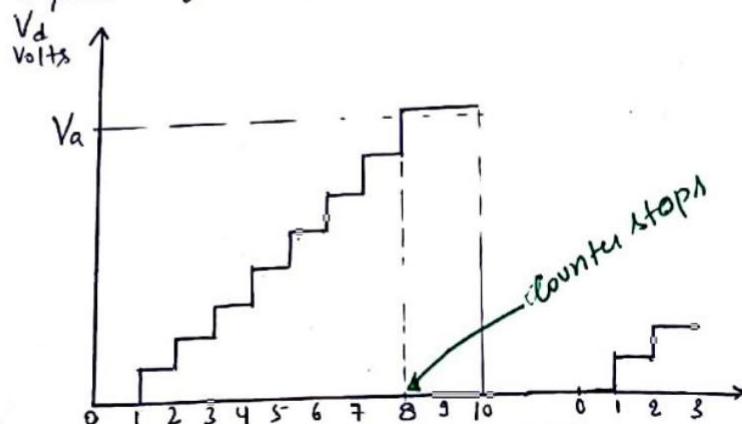


Fig. A counter type DAC .

- The principle is to adjust the DAC's input code until the DAC's output comes within $\pm(\frac{1}{2})$ LSB to the analog input V_a which is to be converted to a binary digital form .
- The counter is reset to zero count by the reset pulse upon the release of RESET .
- The clock pulses are counted by the binary counter .
- These pulses go through the AND gate which is enabled by the voltage comparator high output
- The number of pulses counted increase with time .
- The binary word representing this count is used as the input of a D/A converter whose o/p is staircase type .



- The analog output V_d of DAC is compared to the analog input V_a by the comparator.
- If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of clock pulses to the counter.
- If $V_a < V_d$, the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_a \leq V_d$ and the digital output of the counter gives the analog input voltage V_a .
- For a new value of analog i/p V_a , a second reset pulse applied to clear the counter. Upon the end of the reset, the counting begins again as shown above.
- If the analog input voltage varies with time, then input signal is sampled, using a sample and hold circuit before it is applied to the comparator.
- Low speed is the most serious drawback of this method. The conversion time is $(2^n - 1)$ clock periods.

Q.1. Define the following parameters of a voltage regulator.

- (i). Line regulation .
- (ii) load regulation .
- (iii). Ripple rejection.

⇒ Line regulation ⇒

- It is defined as the percentage change in the output voltage for a change in the input voltage.
- It is usually expressed in mV or as a percentage of the output voltage.
- Typical value of L.R for 7805 is 3 mV.

Load Regulation ⇒

- It is defined as the change in output voltage for a change in load current.
- It is also expressed in mV or as a percentage of V_o .
- Typical value for 7805 is 15 mV for $5\text{mA} < I_o < 1.5\text{A}$

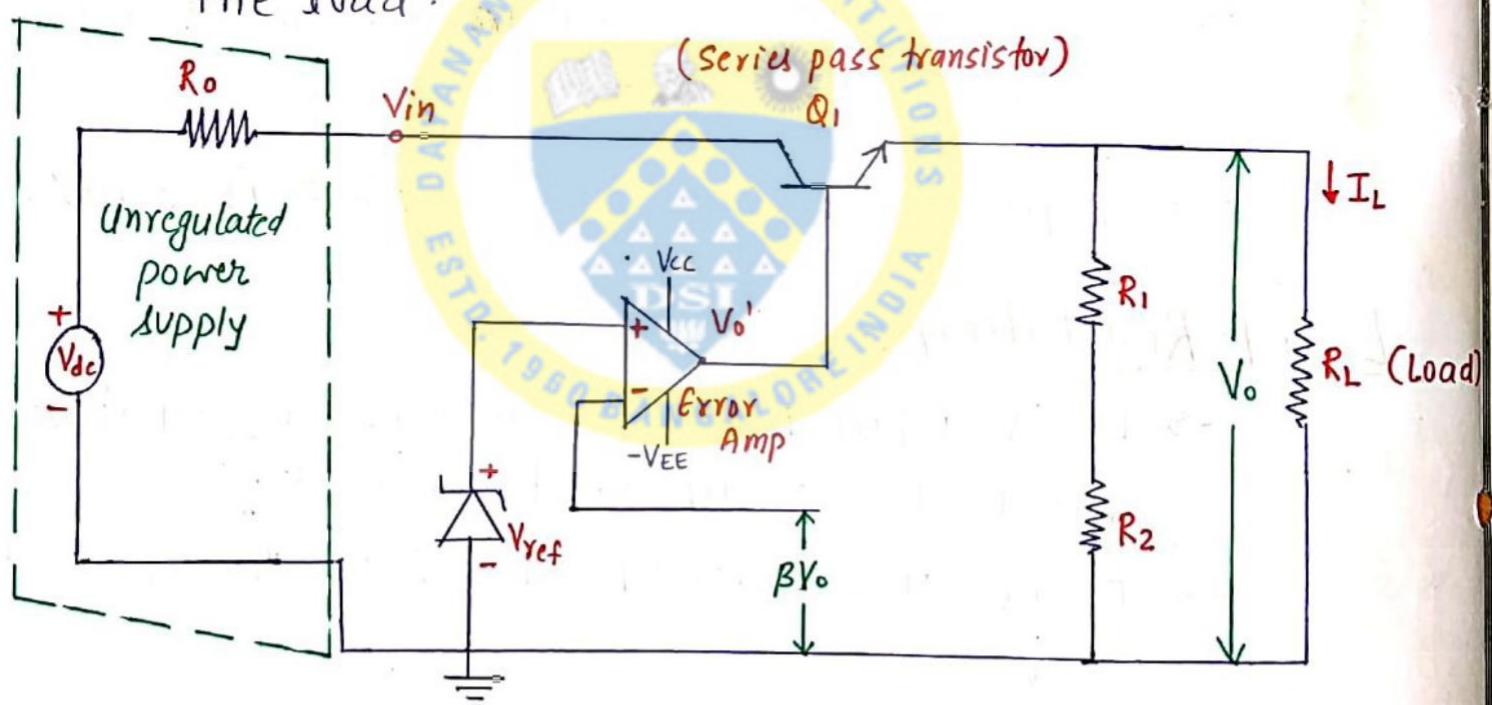
Ripple rejection ⇒

- The IC regulator not only keeps the output voltage constant but also reduces the amount of ripple voltage .
- Usually expressed in dB.
- Typical value for 7805 is 78 dB.

Q.2. What is an Voltage regulator?
 With neat figure explain the working of series op-amp regulator.

⇒ Voltage Regulators ⇒

- A voltage regulator is an electronic circuit that provides a stable dc voltage independent of load current, temp. & ac line vtg variations
- Series regulators use a power transistor connected in series between the unregulated dc input and the load.



- The circuit consists of the following four parts :
 - (1). Reference voltage ckt (Zener diode).
 - (2). Error amp^r. (Difference amp^r).
 - (3). Series pass transistor . (Q_1).
 - (4). Feedback network . (R_1 & R_2).

- In the above ckt, the power transistor Q1 is in series with unregulated DC voltage Vin & regulated o/p voltage Vo.
- So it must absorb the difference between these two voltages whenever any fluctuation in o/p vtg occurs.
- The transistor Q1 is also connected as an emitter follower and therefore provides sufficient gain (current) to drive the load.
- The o/p vtg is sampled by potential divider R_1 & R_2 and fed back to INV i/p terminal of op-amp error amp^r.
- This sampled voltage is compared with reference vtg (V_{ref}) obtained by Zener diode.
- The output vtg V_o' of error amp^r drives the series transistor Q1.
- The output voltage increases due to variations in load current, then sampled vtg (βV_o) also increases.

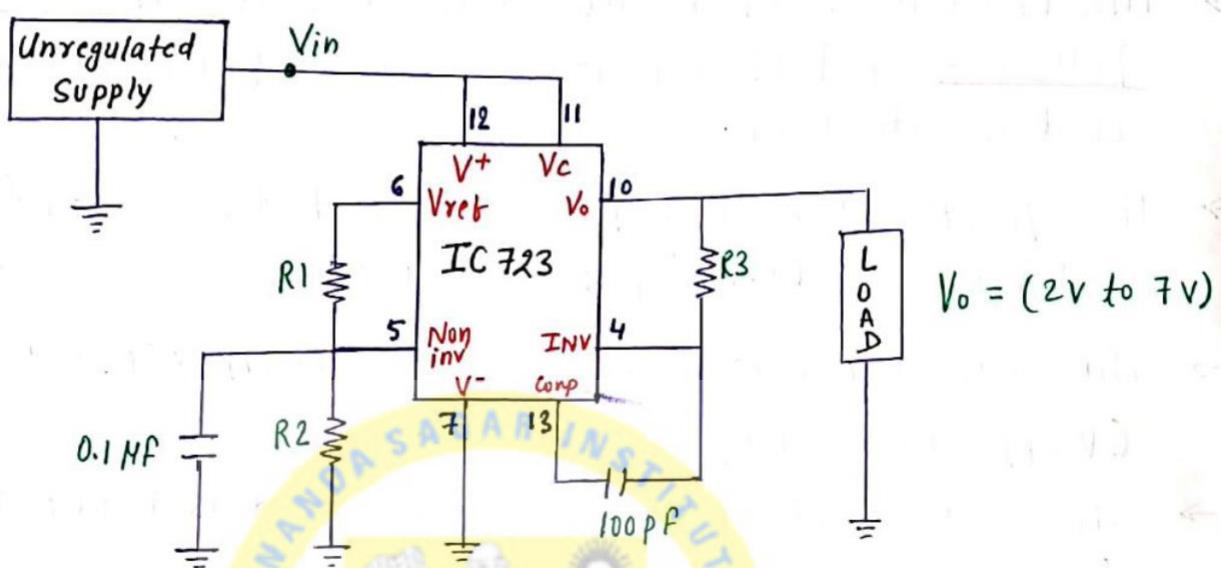
Where,
$$\beta = \frac{R_2}{R_1 + R_2}$$

- The inv. i/p to op-amp increases, therefore o/p of op-amp (V_o') decreases.
- V_o' is applied to base of Q1 which is used as Emitter follower. So, V_o follows V_o' i.e. V_o also decreases.
- Thus, the o/p voltage V_o is constant.

Limitations →

- (1). Flexibility is less.
- (2). Protection ckt are to be applied externally which makes ckt bulkier & costlier.
- (3). Vtg gets affected by various factors such as temp., line variations, etc.

Q.3 With a neat functional diagram, explain the operation of a low-voltage regulator using IC 723.



- A simple positive low vtg (2V to 7V) regulator can be made using 723 as shown in fig.
- The voltage at NON-INV terminal of error amplifier due to $R_1 + R_2$ is

$$V_{NI} = I R_2$$

$$\Rightarrow V_{NI} = \frac{V_{ref}}{R_1 + R_2} \cdot R_2$$

$$\Rightarrow V_{NI} = V_{ref} \cdot \left(\frac{R_2}{R_1 + R_2} \right)$$

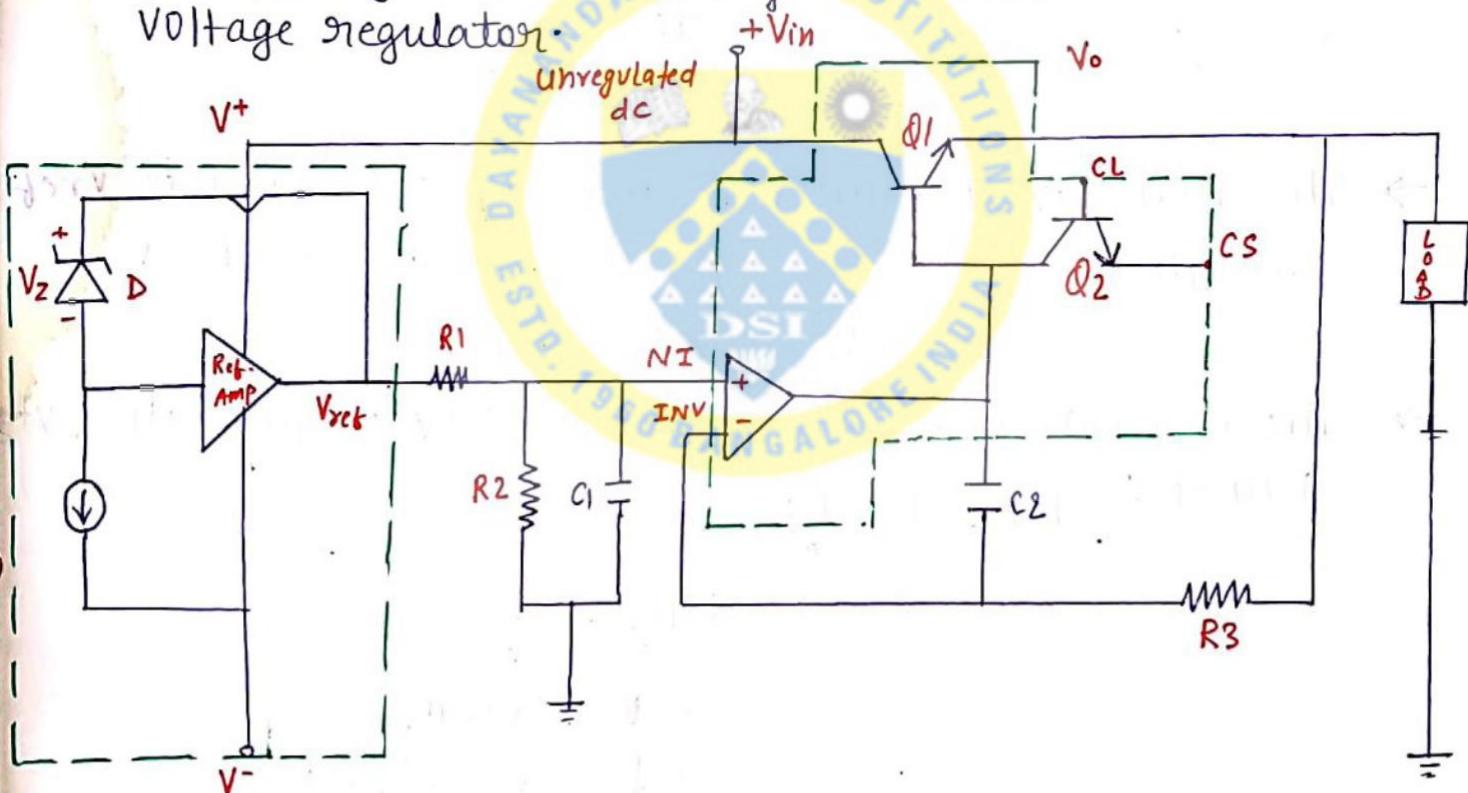
- The diff' between the vtg at non-inv terminal and o/p voltage V_o at inv terminal are the i/p's to the error amplifier.
- The o/p of error amp' drives the pnp transistor Q_1 so as to minimize the diff' between NI & INV i/p of error amp'.
- Since Q_1 is operating as emitter follower;

$$V_o = V_{ref} \left(\frac{R_2}{R_1 + R_2} \right)$$

- The o/p vtg becomes low i.e. voltage at INV terminal goes down, this makes o/p of the error amp to be more positive.
- Thereby increasing the conduction of pass transistor Q1 & thus o/p voltage across load increases. Thus initial drop in voltage is compensated.
- Similarly any increase in load vtg or change in i/p vtg gets regulated.
- The reference voltage is typically 7.15V. So o/p vtg is

$$V_o = 7.15 \cdot \frac{R_2}{R_1 + R_2}$$

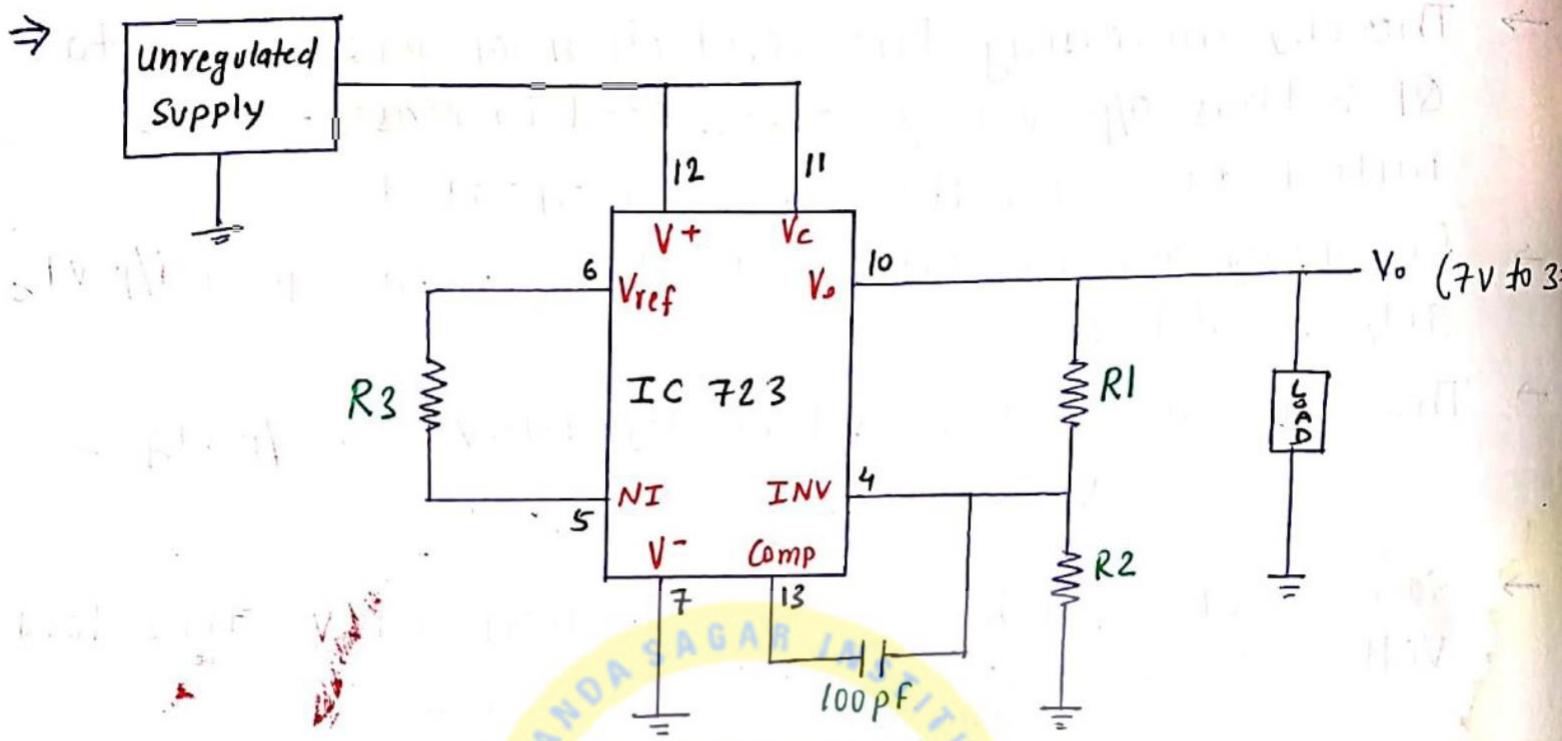
- So, o/p vtg will be always less than 7.15V, thus low voltage regulator.



Features \Rightarrow [723 IC].

- (1). i/p vtg is about 40V maximum.
- (2). o/p vtg is adjustable from 2V to 37V
- (3). 150mA of o/p current is available without transistor (external)
- (4). Output current of 1A is possible by adding external transistors.
- (5). IC 723 can be used as linear or switching regulator.

Q.4. Explain the operation of basic high voltage regulator using IC 723.



→ The non-inv. terminal is directly connected to V_{ref} through R_3 . Hence v_{tg} at NON-INV terminal is $V_{NI} = V_{ref} = 7.15V$.

→ The error amplifier acts as NON-INV amp with a vt gain of : $A_V = 1 + \frac{R_1}{R_2}$

$$\text{as } A_V = \frac{V_o}{V_i}$$

$$\Rightarrow V_o = V_i \cdot A_V$$

$$\Rightarrow V_o = V_{ref} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

$$\Rightarrow \boxed{V_o = 7.15 \left[1 + \frac{R_1}{R_2}\right]}$$

→ Thus o/p voltage is greater than 7.15 V

$$V_{ref} = 7V, V^+ = +V_{cc}$$

$$V_o = 7 \left(1 + \frac{R_1}{R_2}\right), V^- = GND$$

$$R_3 = R_1 R_2$$

Q.5. Design a voltage regulator using IC 723 to get a voltage output of 25V.

$$\Rightarrow V_o = 25V$$

$$V_{ref} = 7V$$

$$V_o = V_{ref} \left[1 + \frac{R_1}{R_2} \right]$$

$$\Rightarrow 25 = 7 \left[1 + \frac{R_1}{R_2} \right]$$

$$\Rightarrow \frac{25}{7} = 1 + \frac{R_1}{R_2}$$

$$\Rightarrow \frac{R_1}{R_2} = \frac{25}{7} - 1$$

$$\Rightarrow \frac{R_1}{R_2} = \frac{18}{7}$$

$$\Rightarrow R_1 = 2.571 R_2$$

Assume, $R_2 = 10\text{ k}\Omega$

$$\Rightarrow R_1 = 25.71\text{ k}\Omega$$

Now

$$R_3 = R_1 \cdot R_2$$

$$= (25.71\text{ k}\Omega) \cdot (10\text{ k}\Omega)$$

$$= 257.1\text{ M}\Omega$$

$$\therefore R_1 = 25.71\text{ k}\Omega$$

$$R_2 = 10\text{ k}\Omega$$

$$R_3 = 257.1\text{ M}\Omega$$

Put these values in high voltage 723 regulator.

Q.6. Design a voltage regulator ckt using LM723
to obtain $V_o = 5V$ and $I_o = 2A$.

$$\Rightarrow V_o = 5V$$

$$V_{ref} = 7V.$$

$$V_o = V_{ref} \cdot \frac{R_2}{R_1+R_2}$$

$$\Rightarrow 5 = 7 \times \frac{R_2}{R_1+R_2}$$

$$\Rightarrow \frac{R_2}{R_1+R_2} = \frac{5}{7}$$

$$\Rightarrow 7R_2 = 5R_1 + 5R_2$$

$$\Rightarrow 5R_1 = 2R_2$$

$$\Rightarrow R_1 = \frac{2}{5}R_2$$

Assume, $R_1 = 10\text{ k}\Omega$

$$\Rightarrow R_2 = 25\text{ k}\Omega$$

Now,

$$R_3 = R_1 \parallel R_2$$

$$\Rightarrow R_3 = \frac{10\text{ k} \times 25\text{ k}}{10\text{ k} + 25\text{ k}}$$

$$\Rightarrow R_3 = 7.14\text{ k}\Omega$$

$$\therefore R_1 = 10\text{ k}\Omega$$

$$R_2 = 25\text{ k}\Omega$$

$$R_3 = 7.14\text{ k}\Omega$$

Put the values in low voltage 723 ckt.

Q.7 Bring out limitations of linear voltage regulators.

→ Limitations of linear voltage regulators are as follows:

- (i). The required input stepdown transformer are bulky and expensive because of low line frequency (50 Hz).
- (ii). Due to low line frequency (50 Hz), large values of filter capacitors are used.
- (iii). The efficiency of a series regulator is very low.
- (iv). The input voltage must be greater than the output voltage.
- (v). As large is the difference between the input and output voltage then more is the power dissipated in the series pass transistor.
- (vi). For higher input voltages, efficiency further decreases.
- (vii). The need for dual supply, is not economical and feasible to achieve with the help of linear regulators.

① Bulky

② Expensive

③ Capacitor filters are required.

④ Low efficiency

⑤ V_i must be $> V_o$

⑥ High power dissipation

⑦ Costly due to dual power supply.

Q.8. Explain basic switching regulator circuit with relevant expressions.

Mention its advantages and disadvantages.

→ The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input.

→ The thermistor R_f limits the high initial capacitor charge current.

→ Transistors Q_1 and Q_2 are alternatively switched ON and OFF at 20 KHz. These transistors are either fully ON or cutoff, so they dissipate very little power.

→ The transistors Q_1 and Q_2 drives the primary of the main transformer.

The secondary is center tapped & full wave rectification is achieved by diodes D_1 & D_2 .

This unidirectional square wave is next filtered through a 2-stage LC filter to produce o/p voltage.

→ The regulation of V_o is achieved by feedback circuit consisting of PWM and steering logic ckt.

→ The fraction of the o/p i.e. $\frac{R_2}{R_1+R_2} \rightarrow V_o$ is feedback to INV input of the comparator 1 & is compared with a fixed reference voltage V_{ref} in comparator 1.

→ The o/p of comparator 1 is called $V_{control}$ & is applied to INV i/p terminal of comparator 2 and a triangular waveform of frequency 40 KHz is applied at NON-INV

(It may be noted that a High frequency triangular waveform is being used to reduce the ripples).

- The comparator 2 functions as a pulse width modulation and its o/p is square wave V_A of period 'T'.
- The duty cycle of square wave is $\frac{T_{ON}}{T_{ON} + T_{OFF}}$ and varies with $V_{control}$ which inturn varies with the variation of o/p voltage V_o .
- The o/p V_A drives a steering logic circuit shown in dashed blocks:

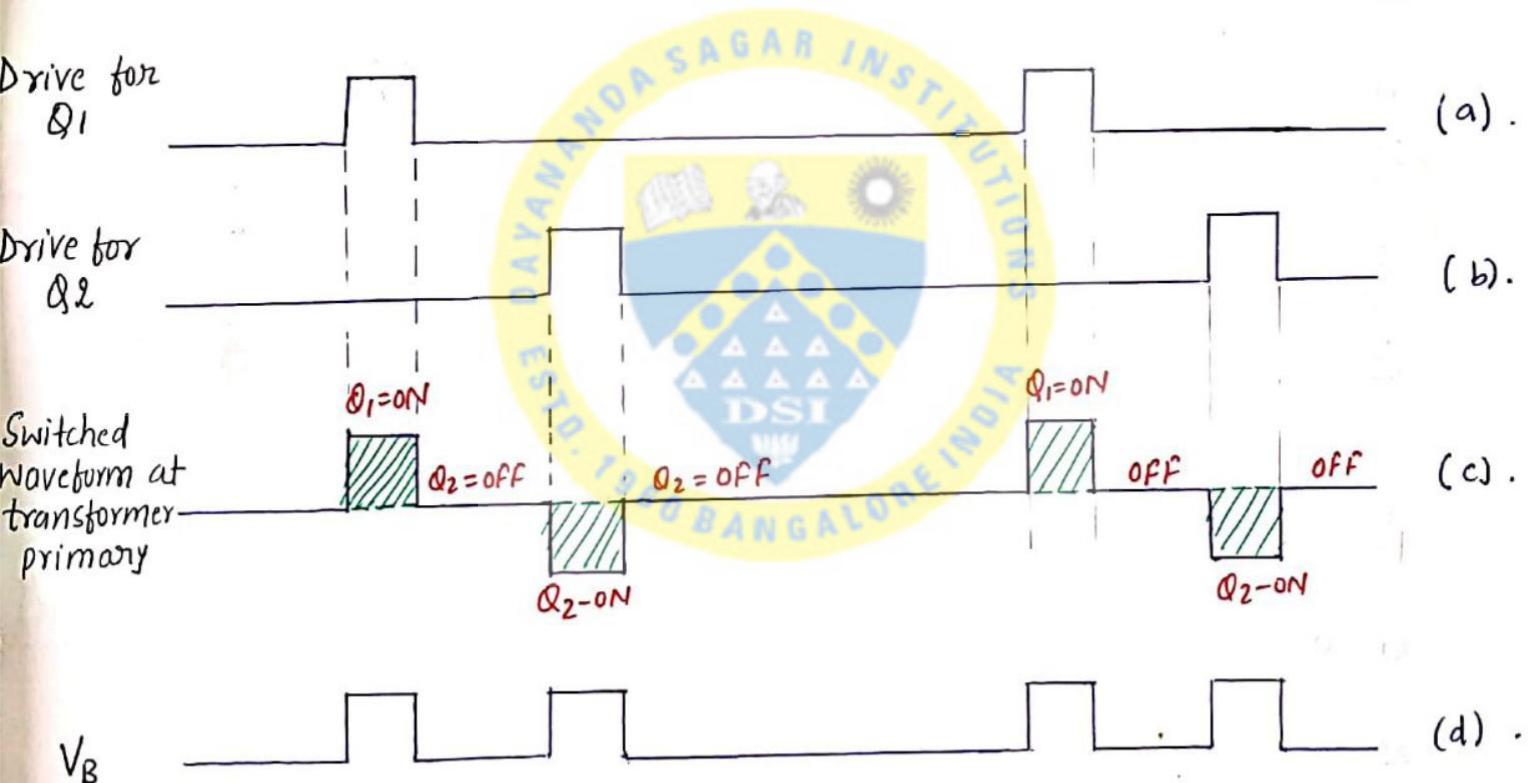


Fig. Switching Power supply waveform .

- The o/p V_{A1} and V_{A2} of AND gates A_1 and A_2 are shown fig (a) & fig (b).
- These waveforms are applied at base of Q_1 and Q_2 depending upon whether Q_1 & Q_2 is ON, the waveform of i/p of the transformer will be a square wave as shown in fig (c).
- The rectified o/p V_B is shown in fig (d).

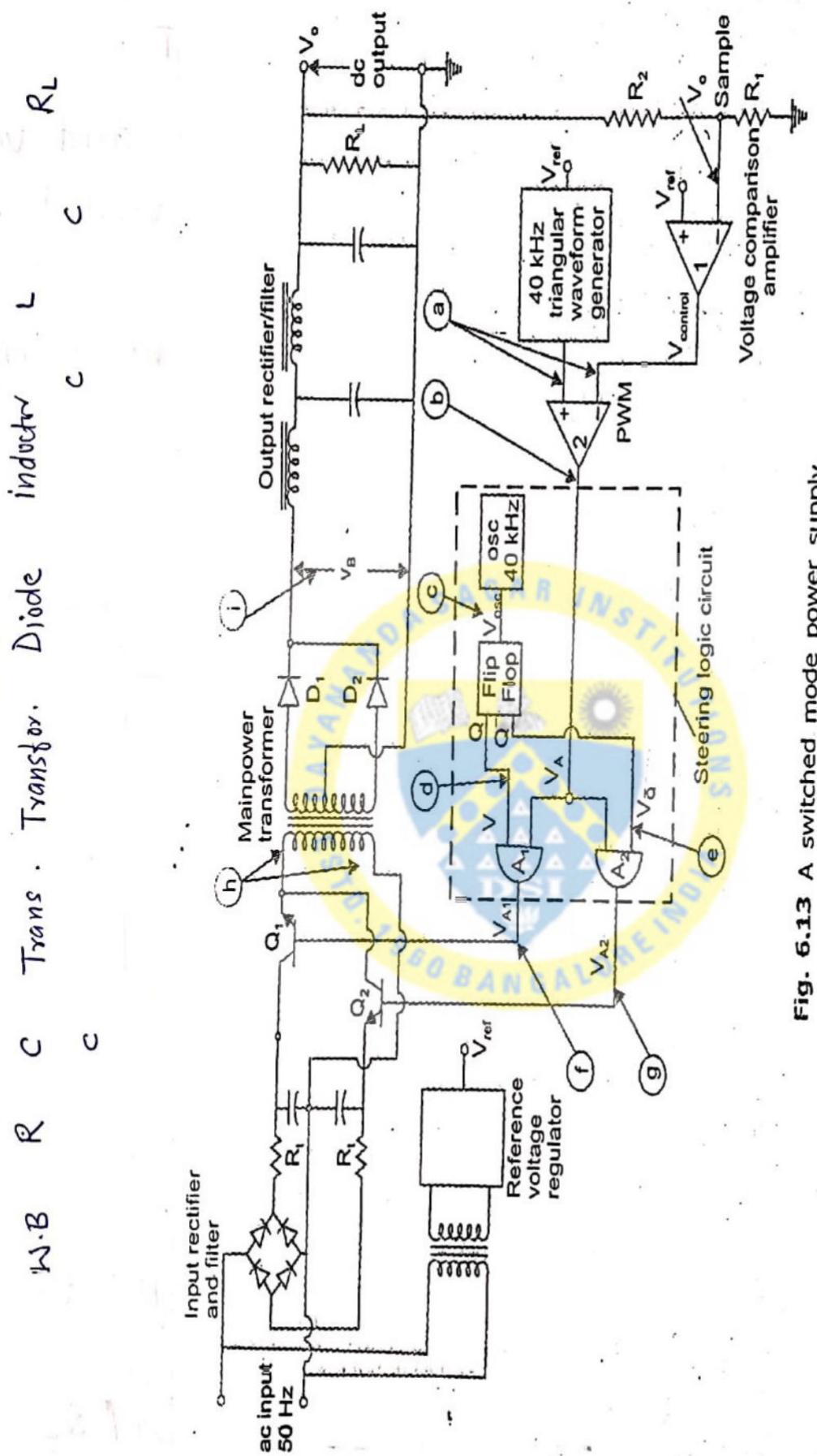


Fig. 6.13 A switched mode power supply

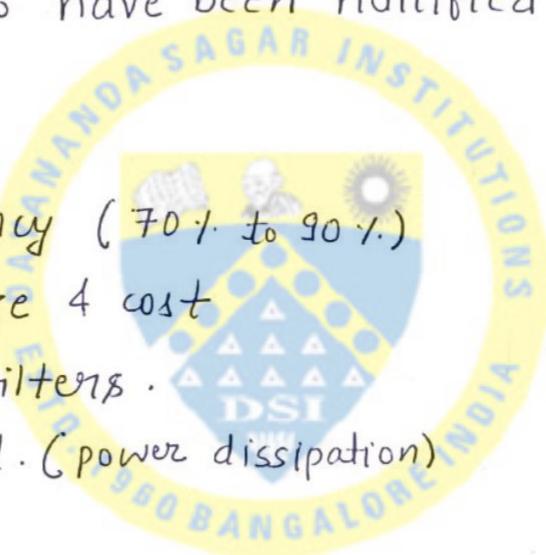
- With high quality factor, the conversion efficiency can easily exceed 90%.
- If there is rise in dc o/p voltage V_o , the voltage control ($V_{control}$) of comparator 1 also rises. Now time period T_1 decreases.

This in turn decrease the pulse width of the waveform driving the main power transformer.

- Reduction in pulse width lowers, the average value of dc o/p voltage V_o . Thus the initial rise in dc o/p voltage V_o have been nullified.

Advantages ⇒

- (1). High efficiency (70% to 90%)
- (2). Decreased size & cost
- (3). Small o/p filters.
- (4). P_d is small. (power dissipation)



Disadvantage ⇒

- (1). Complex design.
- (2). Ripple voltage is higher.
- (3). Electromagnetic & radio frequency interference occurs.
- (4). It SMP's requires external components like inductors & transformer.

Principle ⇒

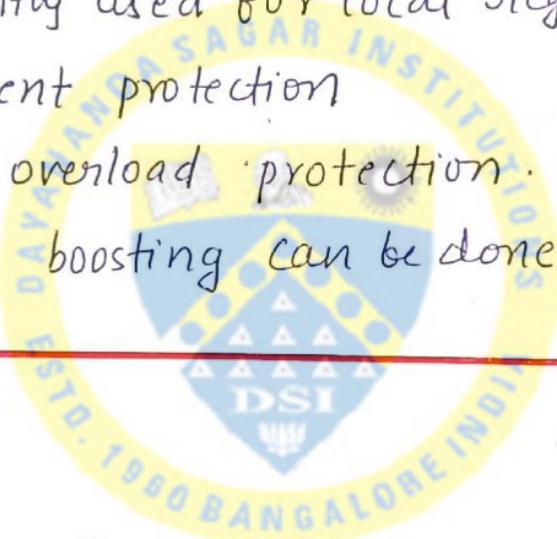
The pulse width modulates the basic principle of switching regulator to control the average value of the o/p voltage.

Q.9. Mention the salient features of a IC 723 regulator?

- ⇒ (1). IC 723 is a general purpose regulator, which can be adjusted over a wide range of both positive and negative regulated output voltage.
- (2). Output voltage ranges from 2V to 37V at $I = 150\text{ mA}$.
- (3). Input and output short circuit protection is provided.
- (4). It has good line and load regulation.
- (5). Low temp. drift and high ripple rejection.
- (6). low stand by current drain.
- (7). Small size.
- (8). Low cost.

Q1) Mention the advantage of IC voltage regulator.

- (1). Easy to use .
- (2) Simplifier power supply design .
- (3). Low cost .
- (4). High reliability .
- (5). Reduction in size .
- (6). Excellent performance .
- (7). Conveniently used for local regulations .
- (8). Over current protection
- (9). Thermal overload protection .
- (10). Current boosting can be done .



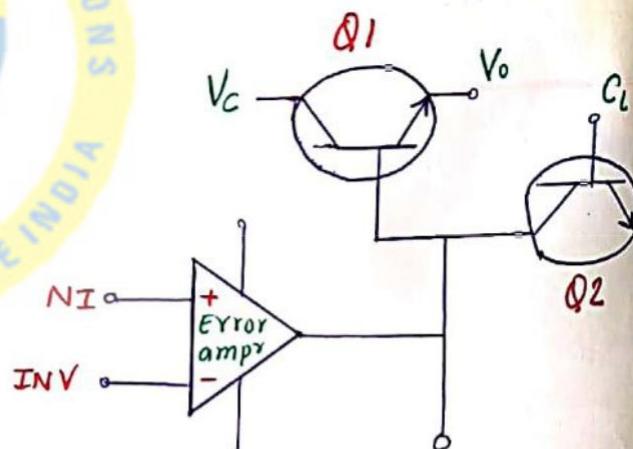
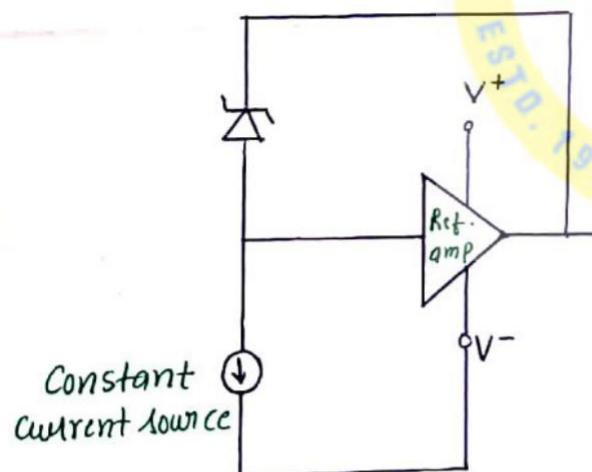
Q.11. With a neat internal diagram of IC 723 explain the functions of each block:

- ⇒ IC 723 is a general purpose voltage regulator, which can be adjusted over a wide range of both positive or negative regulated voltages.
- It is inherently low current device, but can be boosted to provide 5A or more by connecting external components.

Limitations:

- (1). No inbuilt thermal protection.
- (2). No short circuit limits

Function diagram ⇒



section 2.

→ It has two sections:

- (1). The section 1 has Zener diode, a constant current source and reference amplifier produces a fixed voltage of about 7V at terminal V_{ref}.

The constant current source forces the zener to operate at fixed point so that the zener's output is a fixed v_{tg}

Section 2 ⇒

- Section 2 consists of an error amp^r, a series pass transistor Q₁ and a current limit transistor Q₂.
- The error amp^r, compares a sample of the o/p voltage applied at INV terminal with that of reference v_{ref} (V_{ref}) applied at NON-INV terminal.
- The error signal controls the conduction of Q₁.
- Current limit transistor limits the short circuit current by connecting external resistor between CL and CS

These two sections are internally not connected but are available on IC package.

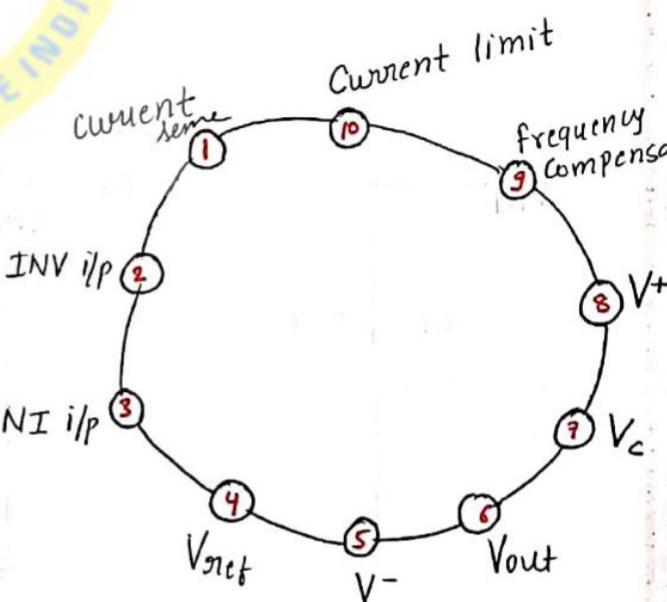
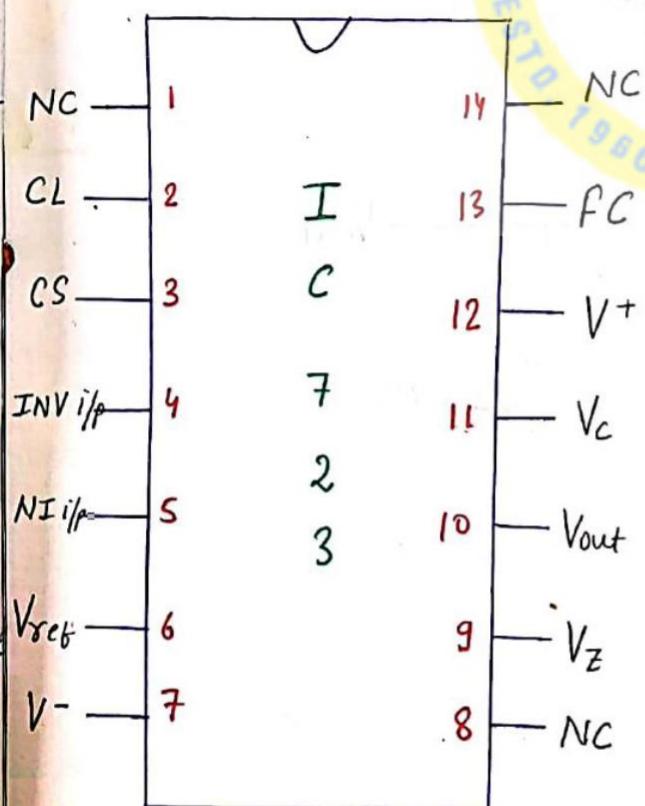
Pin diagram ⇒

Fig. 10-pin metal-can package

Fig. 14-pin dual-in line package

Q.12. Explain briefly 78XX and 79XX series voltage regulators.

⇒ 78XX ⇒

→ 78XX series are 3-terminal **positive fixed** voltage regulators.

→ In 78XX, the last 2 numbers XX indicates voltages.

$$7805 \rightarrow +5V$$

$$7806 \rightarrow +6V$$

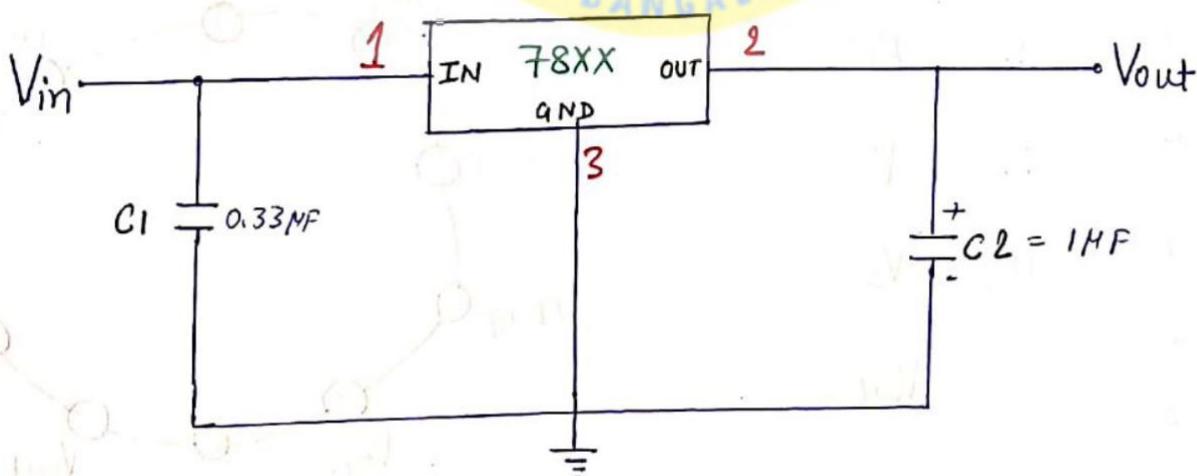
$$7808 \rightarrow +8V$$

$$7812 \rightarrow +12V$$

$$7815 \rightarrow +15V$$

$$7818 \rightarrow +18V$$

$$7824 \rightarrow +24V$$



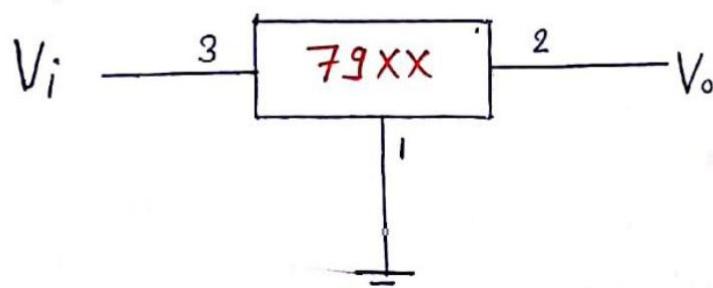
→ Pin 1 is input.
Pin 2 is output
Pin 3 is ground.

→ This IC gives an o/p of +5V and max. load current of 1A for 7805 IC.

- i/p capacitor prevent oscillations.
- o/p capacitor improves frequency response.
- 78XX the input vtg must be 2V greater than o/p vtg . I/p voltage range is 8V to 20V.
- The capacitor C1 usually connected between ~~o/p~~ input and ground terminal to cancel the inductive effect due to long distribution leads.
- The capacitor C2 connected between o/p & gnd terminal improves the transient response.
- Load regulation = 10 mV for load current of 5mA to 1.5A
 Line regulation = 3 mV for i/p vtg of 7V to 25V
 Ripple rejection = 80dB, it reduces ripple by a factor 10,000.
- There are seven o/p voltages options available .
 $5, 6, 8, 12, 15, 18, 24 \text{ V}$

79XX ⇒

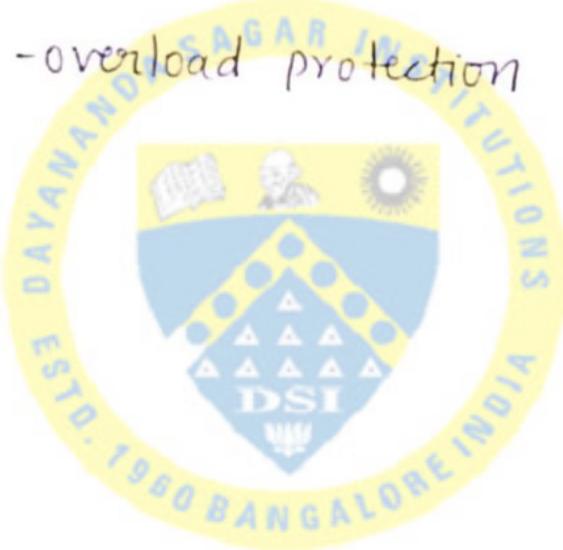
- 79XX series are 3-terminal **negative** fixed voltage regulator .
- last two numbers i.e. XX indicate o/p voltages .
- The IC 79XX series is available for the voltages
 $-5, -6, -8, -10, -12, -15, -18, -24 \text{ V}$.



- In 79XX series two extra voltage options of +5V and -5.2V available.
- These regulators are available in two types of packages : (i) Metal package
(ii) Plastic package.

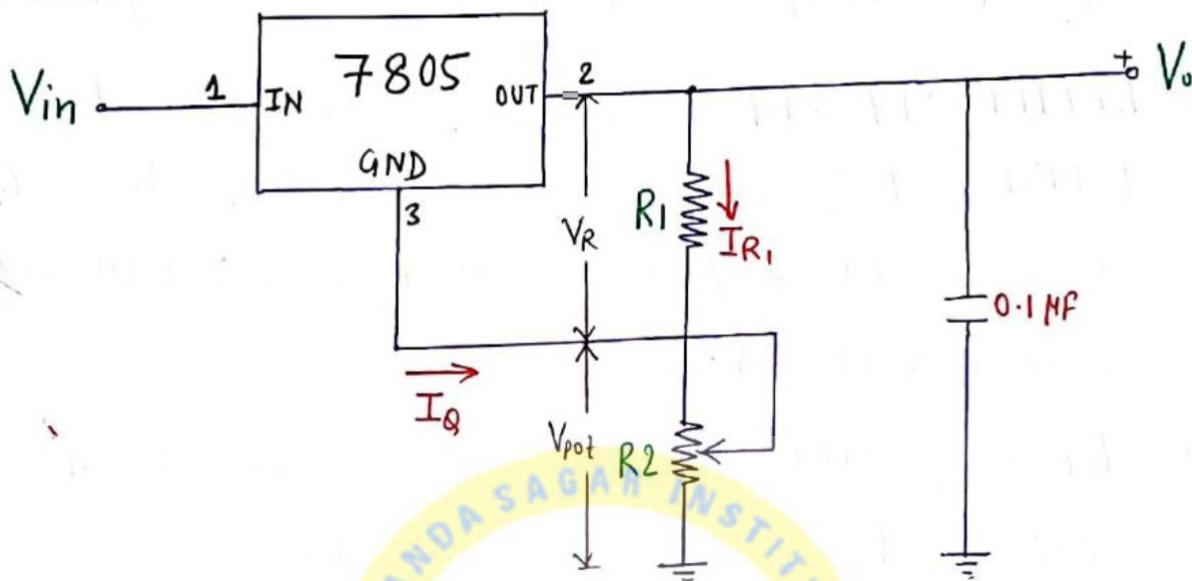
Advantages →

- (1). Easy to use .
- (2). Low cost .
- (3). Over-current protection .
- (4). Thermal -overload protection .



Q.13. With the help of neat diagram, explain the operation of adjustable regulator using fixed 3-terminal regulator.

⇒



- The fixed voltage regulator can be used as variable regulated voltage regulator. The ckt is shown above.
- Here V_{R1} is the regulated voltage difference b/w pin 2 & 3.
- The o/p vtg;

$$\begin{aligned}
 V_o &= V_{R1} + V_{pot} \\
 &= V_{R1} + [I_{R1} + I_Q] R_2 \\
 &= V_{R1} + I_{R1} R_2 + I_Q R_2 \\
 &= V_{R1} + \frac{V_{R1}}{R_1} \cdot R_2 + I_Q R_2
 \end{aligned}$$

$$\Rightarrow V_o = V_{R1} \left[1 + \frac{R_2}{R_1} \right] + I_Q R_2 \quad \text{Neglected}$$

Where, V_{R1} is the regulated voltage diff" between OUT & GND terminal.

- The effect of I_Q is minimized by choosing R_1 small enough to minimize the term $I_Q R_2$.
- The minimum output voltage is the value of fixed voltage available from the regulator.
- LM117, 217, 317 positive regulators and LM137, 237, 337 negative regulators have been specially designed to be used for obtaining adjustable output voltages.
- It is possible to adjust o/p v/tg from 1.2V to 40V and current upto 1.5A.

14. Explain the current limiting feature of 723 regulator.

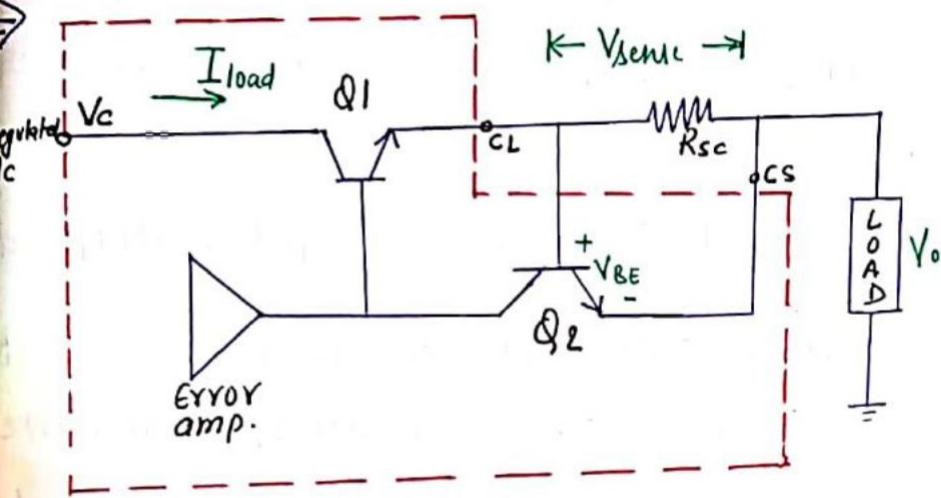
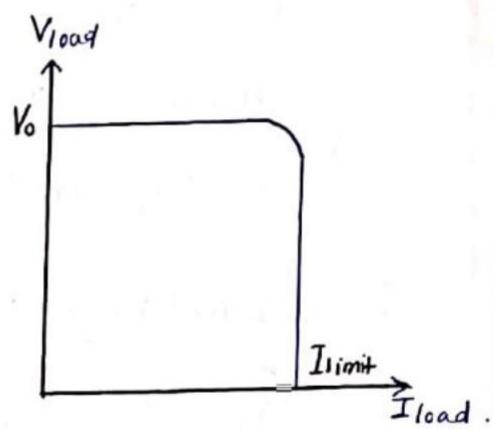


Fig. Current limit protection ckt



(b). Characteristic Curve.

- If load demands more current (example under short circuit conditions) the IC tries to provide it at a constant o/p voltage getting hotter all the time this may ultimately burn the IC.
- Current limiting refers to the ability of a regulator to prevent the load current from increasing above a pre-set value.
- The o/p voltage remains constant for a load current below I_{limit} .
- As current approaches I_{limit} , the output voltage drops. This current limit is set by connecting an external resistor R_{sc} between the terminal CS and CL .
- CL is connected to V_0 and CS is connected to load.
- The load current produces a small voltage drop V_{sense} across R_{sc} . This is applied directly across the base to emitter junction of Q_2 .

