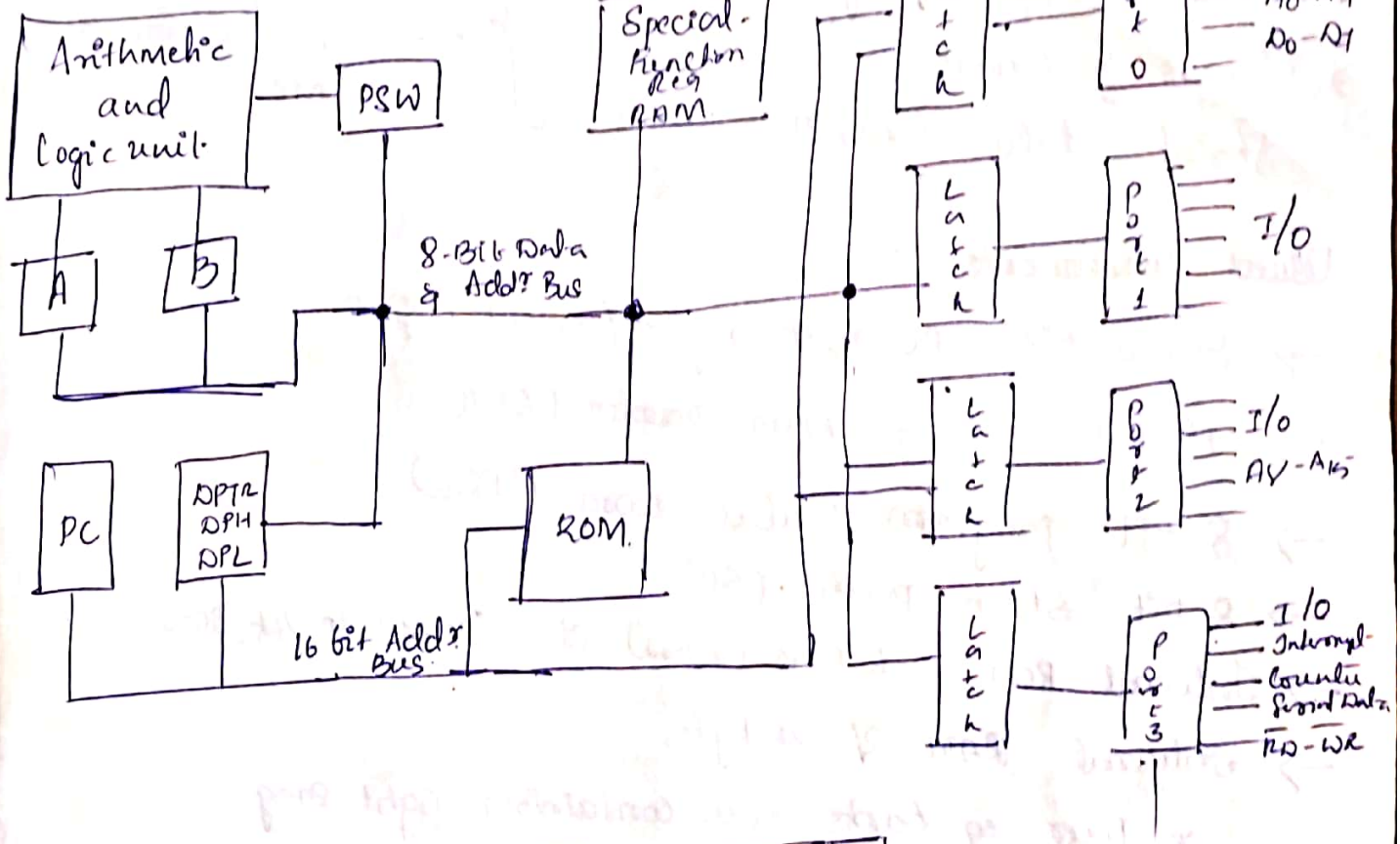
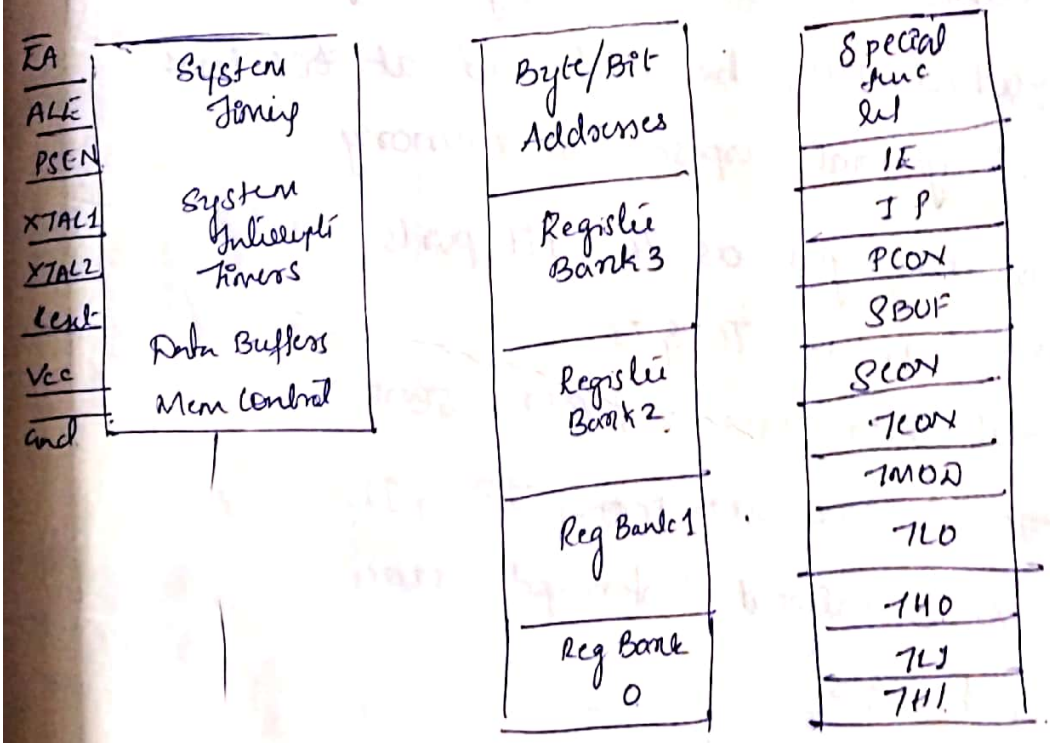
8051 MC Hardware





Port 3
Mem Control

Internal RAM Structure

Block Diagram of 8051

Block diagram of 8051 MC has following features

→ Internal ROM and RAM
→ I/O ports with programmable pins
→ Timers & Counters
→ Serial data I comm^n

} unique features to MC.

~~Usual components~~

→ Eight bit CPU with reg A (accl r) & B
→ 16 bit PC & Data pointer (DPTR)
→ 8 bit program status word (PSW)
→ 8 bit stack pointer (SP)
→ Internal ROM or EPROM (8751) of 0 (8031) to 4k (8051)
→ Internal RAM of 128 bytes
  * Four reg banks, each containing eight reg
  * 16 bytes, which may be addressed at bit level.
  * 80 bytes of general purpose data memory
→ 32 i/p/o/p pins arranged as 4 8 bit ports : P0-P3
→ 2 16 bit timer / counter : T0 & T1.
→ Full duplex serial data receiver / Txr : SBUF.
→ Control Reg : TCON, TMOD, SCON, PCON, IP & IE.
→ Two External & 3 internal interrupt source
→ Oscillator & clock ckts.

8	B8*
IP Reg	

8	A8*
IE Reg	

Interrupt Reg.

8	89
TMOD Reg	

8	88*
TCON reg	

Timer control reg

8	F0*
A Reg	

8	F0*
B reg	

Math Reg

8	8C
TH0 Counter	

8	8A
TL0 Counter	

8	8D
TH1 Counter	

8	8B
TL1 Counter	

Timer / Counter Reg

8	98*
SCON Reg	

8	99
SBUF Reg	

8	87
PCON Reg	

Serial Data Registers.

8	D0*
PSW Reg	

Flags

8	81
SP Register	

Stack pointer Reg.

8	83	8	82
Data pointer			
DPH		DPL	

16	No addr
PC	

Data & Code Addressing Reg.

8	80*
Port-0 latch	

8	90*
Port-1 Latch	

8	A0*
Port-2 latch	

8	B0*
Port-3 latch.	

No of Bit

Direct Byte addr

* Indicates Bit Addressible.

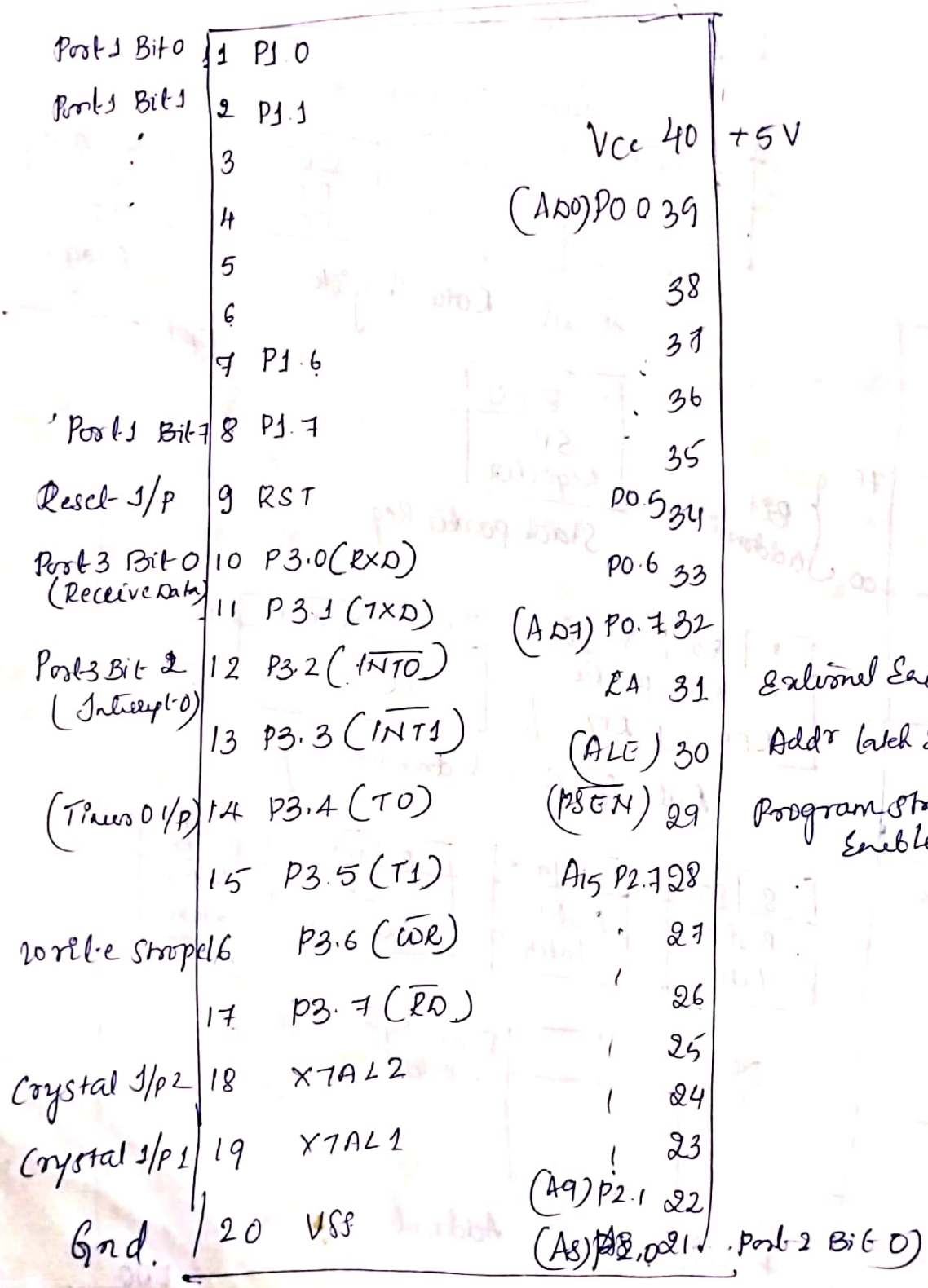
Byte addr	Inbuilt RAM.
7F	General Purpose Area.
30	Bit Address Area (Bit addressible.)
2F	
20	
1F	Reg Bank 3
18	
17	Reg Bank 2
10	
0F	Reg Bank 1.
08	
07	R7
06	R6
05	R5
04	R4
03	R3
02	R2
01	R1
00	R0

Reg Bank 0.

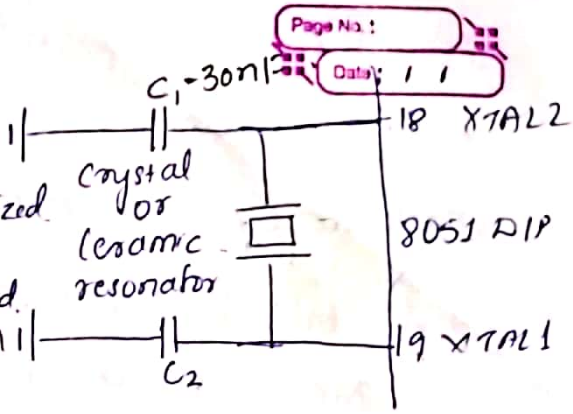
FFF	
000	Inbuilt ROM

Programming Model

→ Collection of 8 & 16 bit reg & 8 bit mem locations
→ These are made to operate using the soft instrs
→ Pinout of 8051 is shown below.



The 8051 Oscillator & Clock



→ The heart of 8051 circuitry that generates the clock pulses by which all internal operations are synchronized.

→ Pins XTAL1 and XTAL2 are provided for connecting a resonating n/w to form an oscillator.

→ A Quartz crystal and capacitors are used as shown.

→ This crystal freq is the basic internal clock frequency of MC.

→ The min freq. to be set should be 1MHz & max 16MHz in classic (basic) 8051 families & the operational freq of classic 8051 is (12MHz.)

→ Ceramic resonators can also be used but it decreases freq stability hence crystal is the better choice.

→ When 8051 MC is connected to oscillator ckt & power supply is given, we can observe the freq on XTAL2 pin. i.e XTAL1 is I/P & XTAL2 is the O/P. & 100 capacitors are of 30PF.

Note:- Capacitors are used because usually the freq we obtain from Crystal Oscl^r is more than what is mentioned so Capacitors of some particular value is provided so that they will bring down the Crystal oscl^r value to the rqd. level.

→ The clock freq. fi establishes the smallest interval of time to accomplish any simple operation by either the MC called its Machine T time.

→ The smallest interval of time to accomplish any simple instⁿ or part of a complex instⁿ is called m/c cycle. The machine cycle is made up of 6 states.

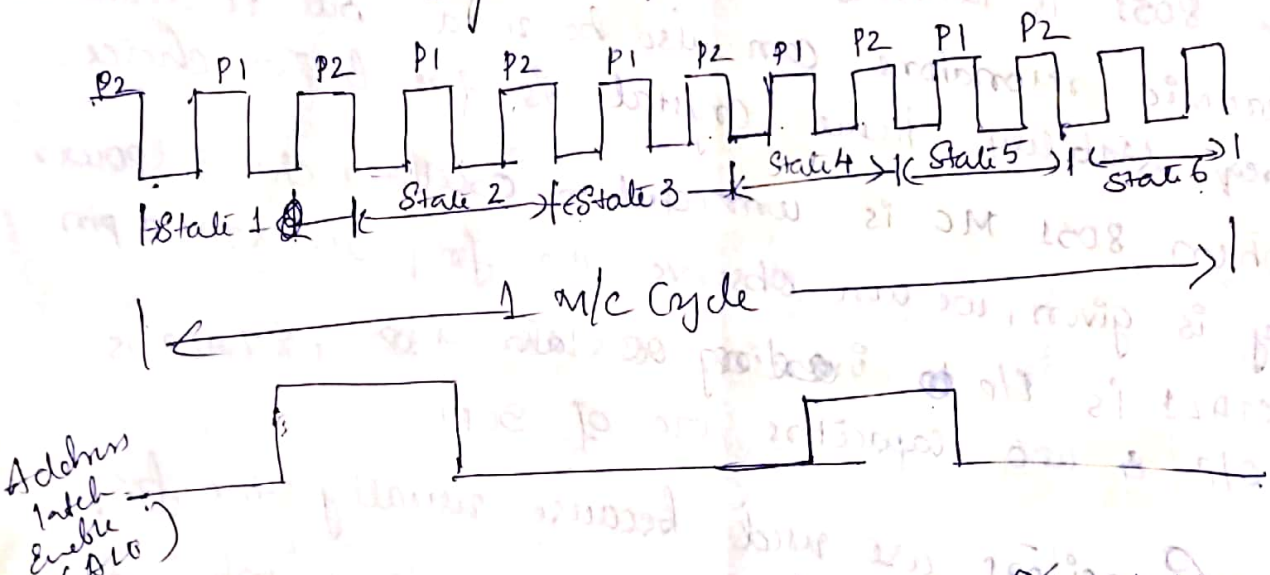
→ A state is the basic time interval for discrete operations of MC such as fetching an opcode byte, decoding an opcode, executing an opcode or writing a data byte.

→ Two oscillator bytes define each state.

→ The time reqd to execute any instⁿ is calculated as

$$T_{inst} = \frac{C \times 12d}{\text{Crystal freq.}}$$

C - no of cycles



There are two ALE pulses per m/c cycle. The ALE p

Program Counter and Data Pointer

→ 8051 has 2 16 bit reg. the Program counter (PC) and the data pointer (DPTR). Each is used to hold the addr of a byte in memory.

→ Program instn bytes are fetched from locations in the chip at addresses 0000h to OFFFh, external to the chip for addr that exceed OFFFh, or totally external for all addresses from 0000h to FFFFh.

→ The PC is automatically incremented after every instr byte is fetched. & may also be altered by some instns.

→ The DPTR reg is made up of 2 8 bit reg. named DPH & DPL, which are used to furnish mem. addresses for internal & external code accesses & external data accesses.

→ DPTR is under the control of pgm instns & can be specified by its 16 bit name, DPTR or by each individual byte name, DPH & DPL.

Note: PC is the only reg that doesn't have any internal addr. DPTR doesn't have single internal addr; DPH & DPL are each assigned an addr.

A & B CPU Reg

→ The 8051 contains 34 GPR, or working reg. Two of these, reg A & B, hold res of many instns, particularly math & logical operations. The other 32 are arranged as part of Internal RAM in 4 banks, R0-R3 of 8 reg.

→ The A (acclr) reg is ~~the~~ most acclr reg which acts as an operand reg. The A reg may be suffered as implicit or specified in the instn by its SFR addr OE0h. It is also bit addressible. After any arithmetic operations res is stored in Acc.

→ B reg is used during multiply & divide operations to store sec operands for multiply & divide instns MUL AB & DIV AB respp. After mult & division, a part of res such as upper 8 bits of mult res & remainder in case of division are stored in the B reg. This is used as temporary reg & can also be accsd by SFR addr of 0F0h. This is also bit addressible.

Flags & Program Status Word (PSW)

→ Flags are 1 bit registers provided to store the results of certain program instns. Other instns can test the conditions of flags & make decision based on flag status.

→ This flag reg in 8051 is called Program status word & resides in SFR space.

→ Thus flags are grouped inside the Program Status Word (PSW) and the power control reg (PCON)

→ The 8051 has 4 math flags that respond automatically to the outcome of math operations & 3 general purpose user flags that can be set(1) or reset(0) by the programmer.

→ Thus PSW is an 8 bit reg also known as flag reg but only 6 bits are used, two unused bits are user definable flags.

→ Four of the flags are called conditional flags, meaning that they indicate some conditions that result after an instn is executed. They are Auxilliary Carry (AC), Overflow (OV), Carry (C) & Parity (P). User flags are named GP0 & GP1 they are GP1= that may be used to record some event in pgm

→ Thus PSW contains 4 math flags, user pgm flag F0 & reg select bits that identify which of four GPR banks is currently in use. GP0 & GP1 are stored in PCON.

PSW Reg

CY	AC	F0	RS1	RS0	OV	-	P

CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary Carry flag.
F0	PSW.5	User flag 0.
RS1	PSW.4	Reg Bank selector bit 1
RS0	PSW.3	Reg Bank selector bit 0
OV	PSW.2	Overflow flag
-	PSW.1	User definable bit
P	PSW.0	Parity flag

RS1	RS0	select reg Bank 0
0	0	0
0	1	1
1	0	2
1	1	3

Cy, Carry flag

→ This flag is set wherever there is a carry out from the D7 bit. This flag bit is affected after an 8 bit add^n or sub^n.

→ It can also be set to 1 or '0' directly by inst^n (SETB C and CLR C). [SETB - Set bit Carry. CLR C - Clear Carry.

Auxiliary Carry

If there is a carry from D3 to D4 during an ADD or SUB operation, this bit is set else cleared. Used by BCD inst^{n}s.

P. Parity flag

Parity flag reflects the no of 1's in A reg only. If it has odd no of 1's then P=1, even no of 1's P=0.

OV, Overflow flag

This flag is set whenever the result of a signed no operation is too large, causing high order bit to overflow to sign bit. Used to detect errors in signed arithmetic.

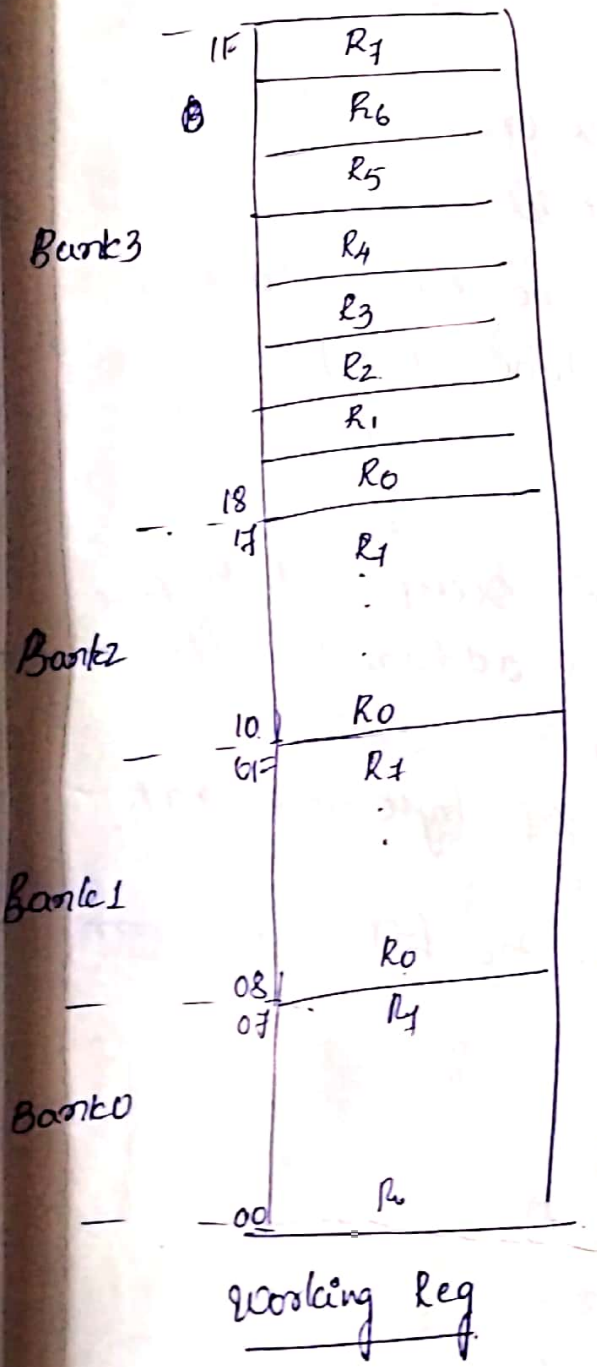
Operations.

```
   38      0011 1000      AC=1      9C      1001 1100
 + 2F    + 0010 1111              + 64    + 0110 0100
 ------  -------------    P=1     ------  -------------
   67      0110 0111 = A            100     1 0000 0000
```

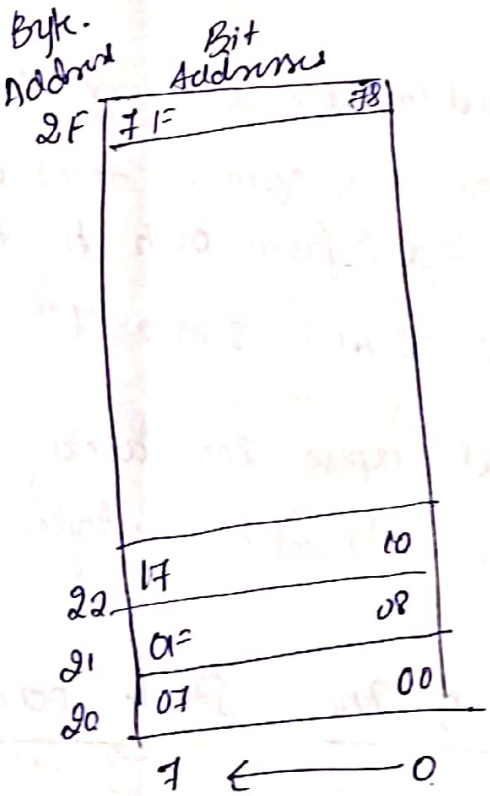
CY=1
AC=1
P=0

Internal Memory

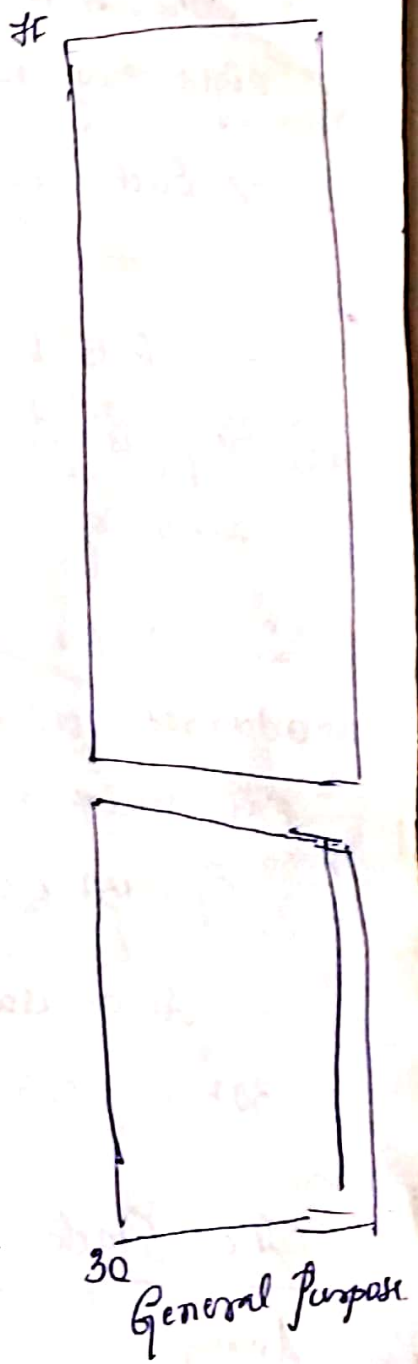
Internal RAM



Working Reg



Bit addressible



General Purpose

The 128-byte internal RAM has 3 areas

1. -> 32 bytes from address 00h to 1Fh that make up 32 working reg organized as 4 banks of eight reg each.
   -> The 4 banks are numbered 0 to 3 and are made up of eight reg named R0 to R7.
   -> Each reg can be addressed by name or its RAM addr
   Eg R0 of Bank 3 is R0 or addr 18h.
   -> Bits RS0 & RS1 in PSW determine which bank of reg is currently in use at any time when pgm is running.

2. A bit addressable area of 16 bytes occupies RAM byte addresses 20h to 2Fh, forming total of 128 addressable bits. Bit addresses are from 00h to 7Fh.
   Eg:- Bit addr 4Fh is also 7th bit of byte addr 29h.

3. A general purpose RAM area above the bit area, from 30h to 7Fh, addressable as bytes.

The Stack & the Stack pointer

Analogy:

* Stack is a section of RAM used by CPU to store information temporarily. The info can be data or address (Explⁿ).

* This is reqd since there is only a limited no of reg

* To access the stack a reg called stack pointer reg is used (SP). which is of 8 bits wide. which means it can take the values from 00 to FFh & hold an internal RAM addr that is called top of stack

* When powered up SP reg contains the value 07, thus loc 08 is the first location used for stack by the 8051

* The storing of a CPU reg in stack is called a PUSH and pulling the contents off the stack back into a CPU reg is called a POP.

Pushing onto stack.

→ SP points to the last used loc. of the stack. Once the data is pushed onto the stack SP is incremented by 1.

→ SP is decremented by 1 when the data is popped from the stack.

Pushing onto stack

→ Whenever data is to be placed on stack, SP increments before storing the data on to the stack. So that stack grows up.

→ To PUSH the reg onto the stack we need the RAM address.

Note: PSW, A, PC to contents are to be stored in most before calling a function.

LIFO

Eg: Bank 0 is selected.

R6 = 25
R1 = 12
R4 = 0F3

PUSH 6
PUSH 1
PUSH 4

Start- SP=07	After push 6 SP=08	PUSH 1 SP=09	PUSH 4 SP=0A.
0B	0B	0B	0B
0A	0A	0A	0A F3
09	09	09 12	09 12
08	08 25	08 25	08 25

Popping from Stack

→ The top byte of stack is copied to reg specified for every POP & SP is decremented once

Eg: POP 3 ; POP Stack into R3
POP 5 R5
POP 2. R2

Start SP=0B	After POP3 SP=0A R3=54	After POP5 SP=09 R5=F9	After POP2 SP=08 R2=76
0B 54	0B	0B	0B
0A F9	0A F9	0A	0A
09 76	09 76	09 76	09
08 6C	08 6C	08 6C	08 6C

* Locations 08 to 1F in RAM can be used for stack. If incremented above 1F it will jump to 30 to 7F because it enters into bit addressible area. Above this stack overflows.

Special Function Registers

→ The Reg A, B, PSW, DPTR and so on also have addresses like R0-R7 & such reg are called Special function Regs (SFR)

→ They can be accessed by their names or address

→ SFR have address b/n 80H & FFH.

SFR list-

A - Accl^r -0E0h

B - B Reg. -0F0h

PSW - Program status word -D0h

SP → Stack pointer - 81H

DPTR → Data ptr (2 bytes)

DPL → low byte -82h

DPH → High byte -83h

8Ch - TH0 - Timer/Counter 0 high byte

8Ah TL0 low byte

TH1 - 8Dh Timer/Counter 1 high byte

8Bh TL1 low byte

SCON - 98h Serial Control

SBUF - 99h Serial Data Buffer

PCON - 87h Power control.

P0	Port-0	80h
P1	1	90h
P2	2	0A0h
P3	3	0B0h

IP Interrupt priority Control -0B8h

IE " Enable Control -0A8h

TMOD Timer/Counter mode Control -89h

TCON Timer/Counter 2 control -88h.

Internal ROM

→ The program code is contained in internal ROM memory occupies the code address space from 0000h to OFFFh.

→ Program addresses higher than OFFFh which exceed the internal ROM capacity makes 8051 to fetch codes from external pgm memory.

→ Also code bytes can be fetched exclusively from external mem address 0000h to FFFFh by connecting external acess pin to gnd (EA).

Code space is decided by the designer.

What is an Architecture? — Internal Design of a Chip

→ is a design which can refer to either H/w or S/w or combination of H/w & S/w. The arch of a sys always defines its broad outlines & may define precise mechanisms as well.

→ An arch diag shows the relationship b/w diff components of sys. which describes the overall concept of a sys.

External Memory

Page No. :
Date : / /

Pin Diagram

Vcc (pin 40):

Vcc provides supply voltage to the chip. The vtg source is +5V.

GND (pin 20) : Ground.

XTAL1 and XTAL2 (pins 19, 18)

RST (pin 9) : reset

- it is an i/p pin & is active high (normally low)
- It is a power on reset. On applying a high pulse to RST, the MC will rst & all values in reg will be lost.

EA (pin 31): External access

→ If EA is connected to GND to indicate the code is stored externally. decide whether using on chip memory or external mem.

PSEN (Program Store Enable)

This is an o/p pin & is connected to the OE pin of the ROM. & is used to read signal from ext program mem. decide whether code or data is stored in ext mem.

ALE (pin 30) Address Latch enable

→ an o/p pin & is active high.

→ is used for demultiplexing the addr & data by connecting to the G pin of 74LS373 latch for P1.0. Enable. External ROM

2 ALE pulses are available for each m/c cycle

I/O port pins.

- The four ports P0, P1, P2 & P3
- Each port uses 8 pins
- All I/O pins are bi-directional.

Pins 32-39 port-0 (P0.0 to P0.7) :- lower order addr & data bus signals are multiplexed with this port.

Pins 21-28. I/O port, higher order addr bus signals are multiplexed. with bi directional port.

Pins 10-17. This port serves other func like interrupts, timer i/p, control signals for external mem interfacing RD & WR, Serial comm signals RXD & TXD

Pins 1-8 purely I/O port.

Port 3

$\overline{INT0}$ $\overline{INT1}$ ⇒ external interrupt pins.