DIGITAL SYSTEM DESIGN USING VERILOG

Course Code: 19EC5DCDSV
(3 Credits)
MODULE-5C

IMPLEMENTATION FABRICS

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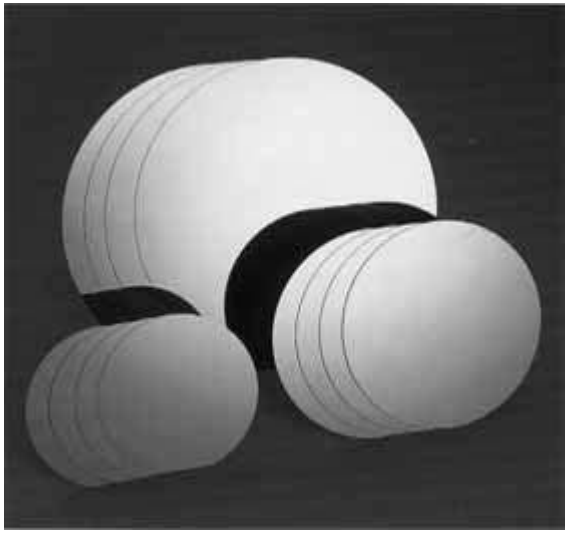
INTEGRATED CIRCUITS

INTEGRATED CIRCUIT MANUFACTURE:

- Silicon chip to refer to a piece of a silicon on which an IC is manufactured.
- Wafer sizes

  50 mm diameter, now more than 300 mm diameter
- Ion implantation: exposing the surface to a plasma of impurity ions that diffuse into the silicon, thus altering its electrical properties in controlled ways
- Etching: chemically eroding an underlying film of material that has been deposited onto the surface.
- Films include insulating materials, such as silicon dioxide; semiconducting materials, such as polycrystalline silicon (also known as polysilicon); and conducting materials, such as aluminum and copper.

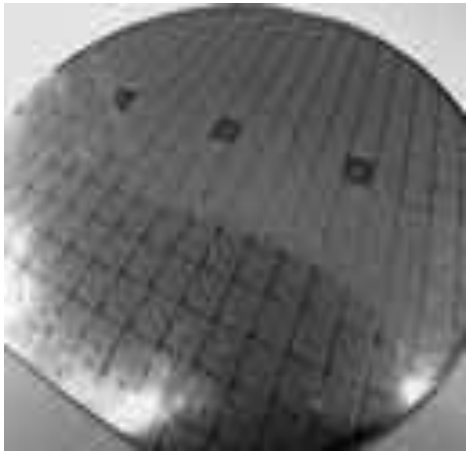
An ingot of crystalline silicon



wafers

- Photolithography: which means using a photographic process to draw on the surface
- The surface is coated with a thin layer of photoresist, a chemical whose resistance to chemical reaction is changed by exposure to light. The surface is then exposed to light through a mask that has opaque and transparent areas in the pattern of features to be drawn.

Graphical representation of the layers of an IC.



A complete wafer containing multiple ICs.

S S I & M S I LOGIC FAMILIES

- 1961 Texas Instruments introduced a family of logic components that designers could use as building blocks for larger circuits.
- 5400 and 7400 families of TTL (transistor-transistor logic) ICs that became the basis of logic design.
- The 5400 family components were manufactured for high-reliability military applications, requiring operation over large temperature ranges, whereas the 7400 family components were for commercial and industrial applications.
- 7400 component provides four NAND gates, a 7427 provides three NOR gates, and a 7474 provides two D flip-flops-small-scale integrated (SSI) components

- 7490 4-bit counter, and the 7494 4-bit shift register- medium-scale integrated (MSI) components.
- 74L00 and 74L74- Low power consumption
- 74S00 and 74S74-Schottky diodes within the internal circuits to reduce switching delays, but with the expense of increased power consumption.
- 74LS00 family-combined the lower-power circuits with Schottky diodes to yield a good compromise between power and speed.
- 74F00 -“fast” family components
- 74ALS00- “advanced low-power Schottky” family
- Operating voltage- 5 V

CMOS

- One of the problems with TTL circuits is that they use bipolar transistors, which have relatively high power consumption even when not switching.
- CMOS -uses field-effect transistors.
- 4000 family
- Power supply range (3V-15V)
- 1980s, some manufacturers introduced a new family of CMOS logic components, the 74HC00 family
- 74AHC00 family, offered improved speed and electrical Characteristics.
- One important characteristic of CMOS circuits is that the power consumption and speed are dependent on the power-supply voltage

- families to operate at the lower voltage with reduced logic thresholds (74LVC00 family) or with TTL-compatible thresholds (74LVT00 family)- operating voltage is 3.3 V.
- advanced variations, such as the 74ALVC00 and 74ALVT00 family.
- during the 1970s, IC technology developed to the level of large-scale integration (LSI)

  Ex: microprocessor,

Example: Use the following components to design a 4-digit decimal counter with a 7-segment LED display: two 74LS390 dual decade counters, four 74LS47 BCD to 7-segment decoders, four 7-segment displays, plus any additional gates required.

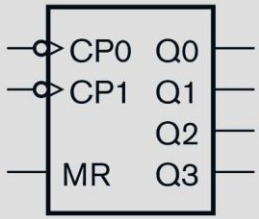
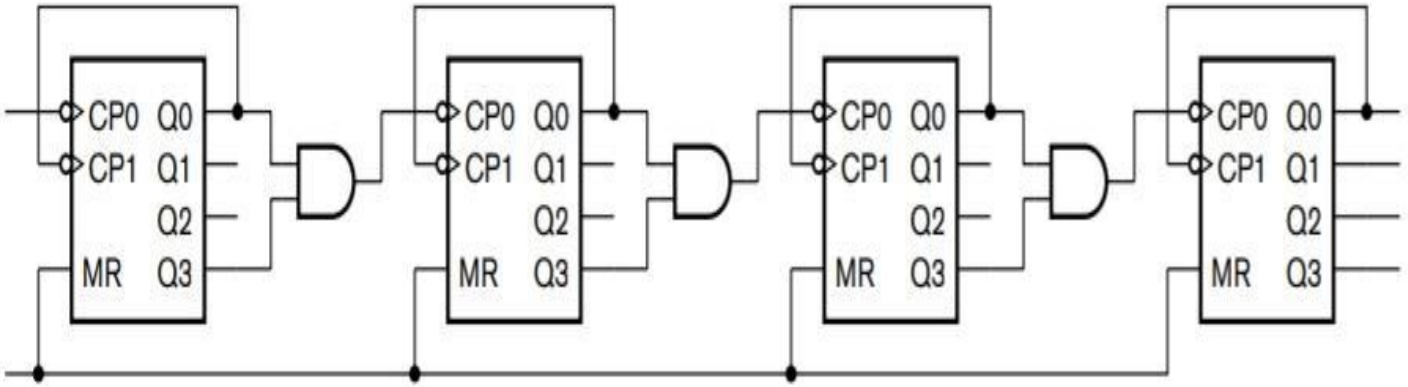


FIGURE 6.5 A symbol for each of the decade counters in a 74LS390 component.

- The 74LS390 component contains two counters
- Internally, the counter consists of a single-bit counter clocked on the falling edge of CP0
- 3-bit divide-by-five counter clocked on the falling edge of CP1.
- A decade (divide-by-ten) counter can be formed by using the single bit counter for the least significant bit and connecting the Q0 output externally to the CP1 input.
- The MR input to the counter is a master reset input. When 1, it forces the counter outputs to 0000



Four 74LS390 decade counters cascaded to make a 4-digit counter.

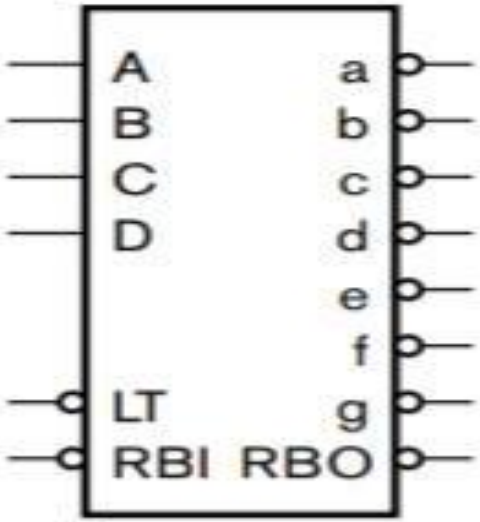
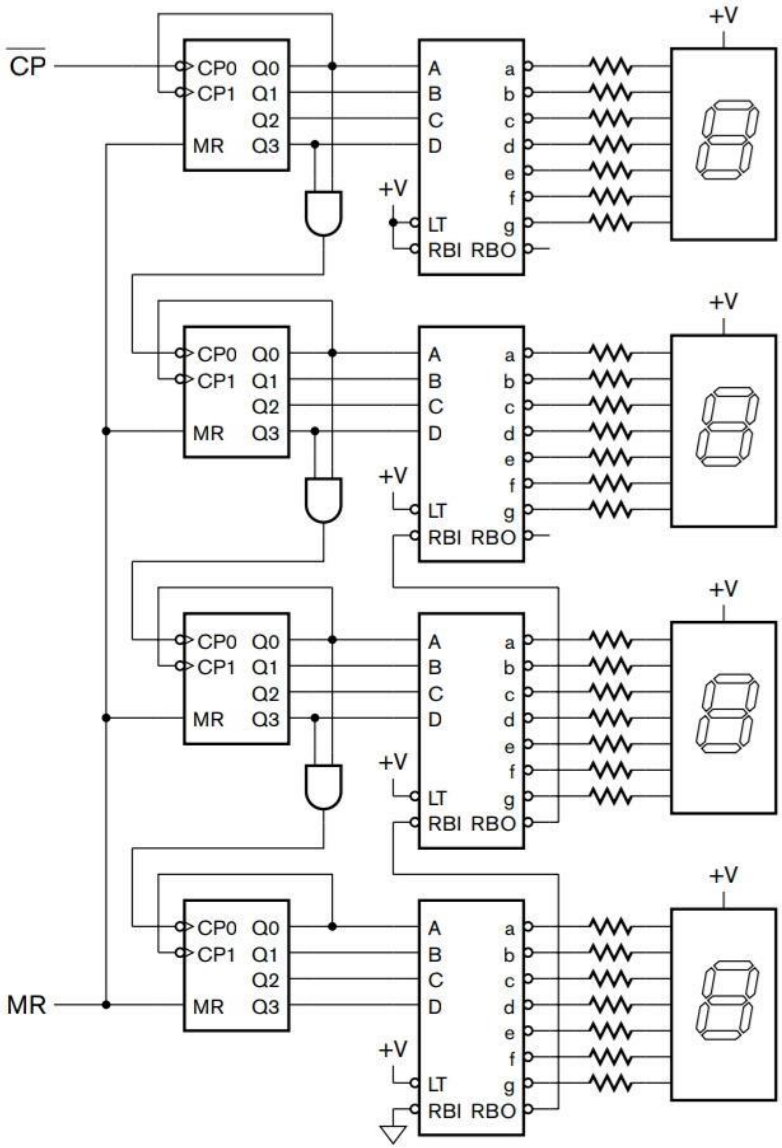


FIGURE 6.7 A symbol for the 74LS47 BCD to 7-segment decoder.

The complete circuit for the 4-digit counter with display.



APPLICATION- SPECIFIC INTEGRATED CIRCUITS (ASICS)

- *ASIC- refers* IC manufactured for a particular application
- It may be designed for a particular end product provided by one manufacturer.

Example: a portable music player, a toy, an automobile, a piece of military equipment, or an industrial machine

- Alternatively, it may be designed for use in a range of products provided by manufacturers in a particular market segment- known as application-specific standard products, or ASSPs

Examples: Examples include ICs for cell phones, which are used by a number of competing cell-phone manufacturers, but which are not of use in, say, automobile control circuits

Advantages:

- It has lower cost per IC than a programmable component such as an FPGA

- Two main design and manufacturing techniques for ASICs.

  * Fully custom integrated circuits: involve detailed design of all of the transistors and connections in an ASIC.
  * This allows the most effective use of the hardware resources on an IC and yields higher performance
  * But has high NRE cost and requires advanced VLSI design expertise within the design team.
  * As a consequence, fully custom ASICs are usually only designed for high-volume products, such as CPUs and ICs for consumer appliances.

- Standard cell ASICs

  - Involve selection of basic cells, such as gates and flip-flops, from a library to form the circuit.
  - The cells have been previously designed by an IC manufacturer or an ASIC vendor, and are used by the synthesis tool during the design process to implement the design.
  - The value of this approach is that the NRE cost for each ASIC design is significantly reduced,
  - Since the cost of designing the cell library is amortized over a number of ASIC designs. The compromise is that the ASIC may not be as dense or have the performance of a fully custom ASIC.

PROGRAMMABLE LOGIC DEVICES

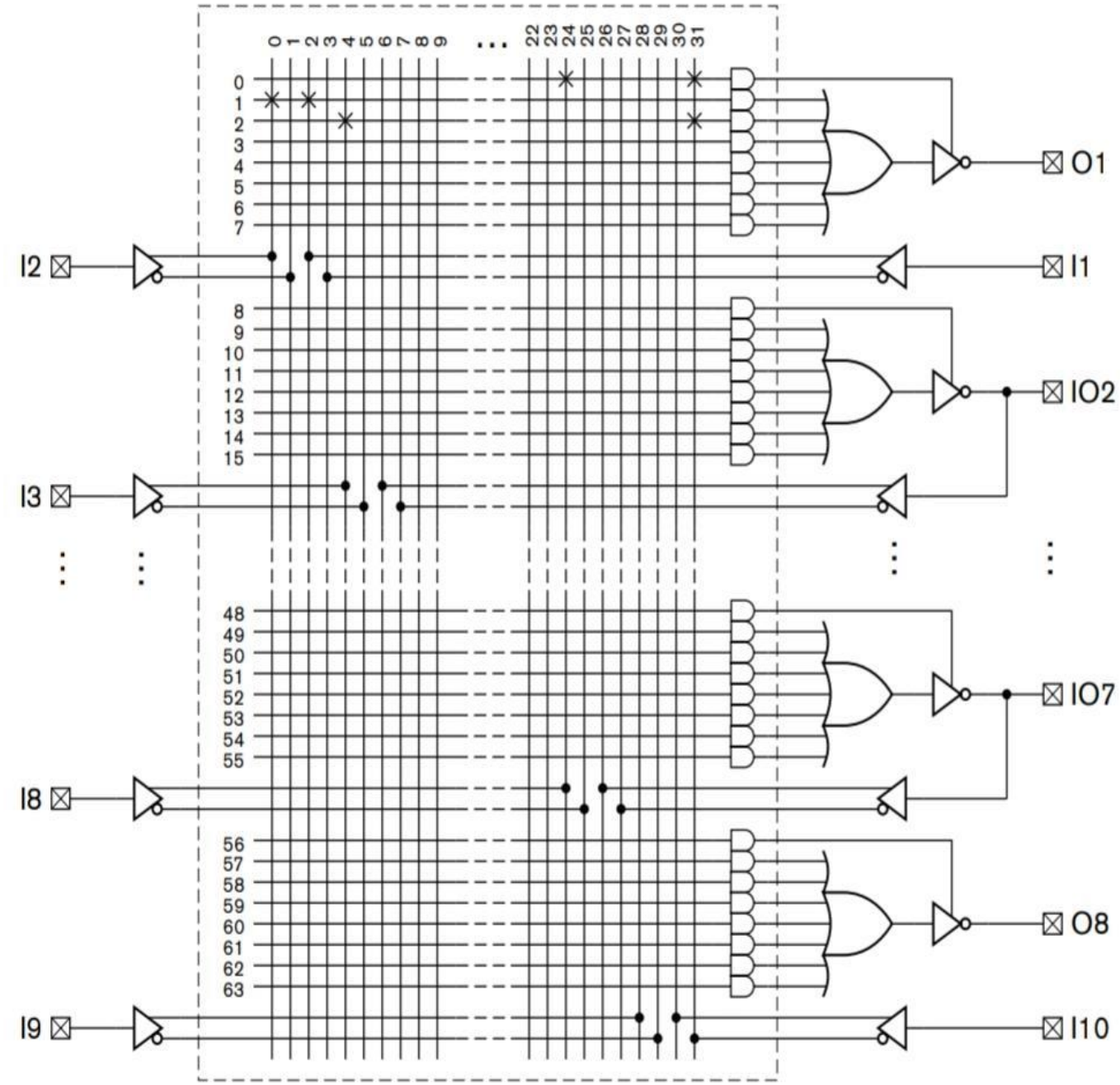
- PROGRAMMABLE ARRAY LOGIC (PAL):

Example: PAL16L8

Features of this PAL are

- The component has 10 input pins, 2 output pins, and 6 pins that are both inputs and outputs total of 16 inputs and 8 outputs
- The symbol at each input in Figure represents a gate that is a combination of a buffer and an inverter. Thus, the vertical signals carry all of the input signals and their negations.
- The area in the dashed box is the programmable AND array of the PAL. Each horizontal signal in the array represents a p-term of the inputs, suggested by the AND-gate symbol at the end of the line.

- In the unprogrammed state, there is a wire called a fusible link, or fuse, at each intersection of a vertical and horizontal signal wire, connecting those signal wires.
- The PAL component can be programmed by blowing some of the fuses to break their connections, and leaving other fuses intact. This is done by a special programming instrument before the component is inserted into the final system.
- Draw an X at the intersection of a vertical and a horizontal signal to represents an intact fuse.
- An intersection without an X means that the intersecting signals are not connected
- A PAL component such as the PAL16L8 can be programmed to implement a variety of combinational functions.


0 1 2 3 4 5 6 7 8 9 ... 22 23 24 25 26 27 28 29 30 31
0
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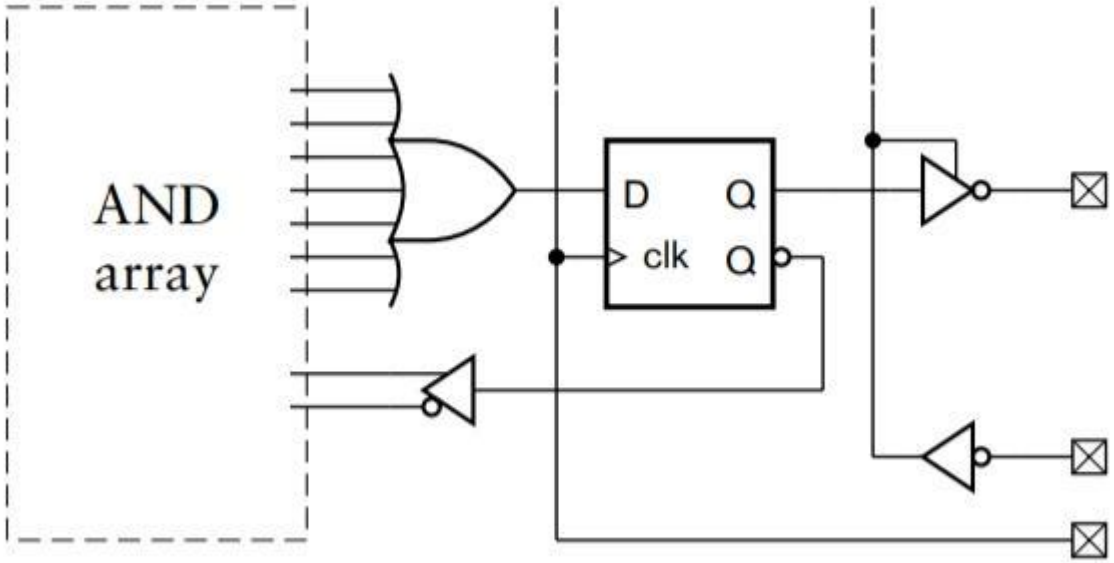
I2
I3
I8
I9
O1
I1
IO2
IO7
O8
I10

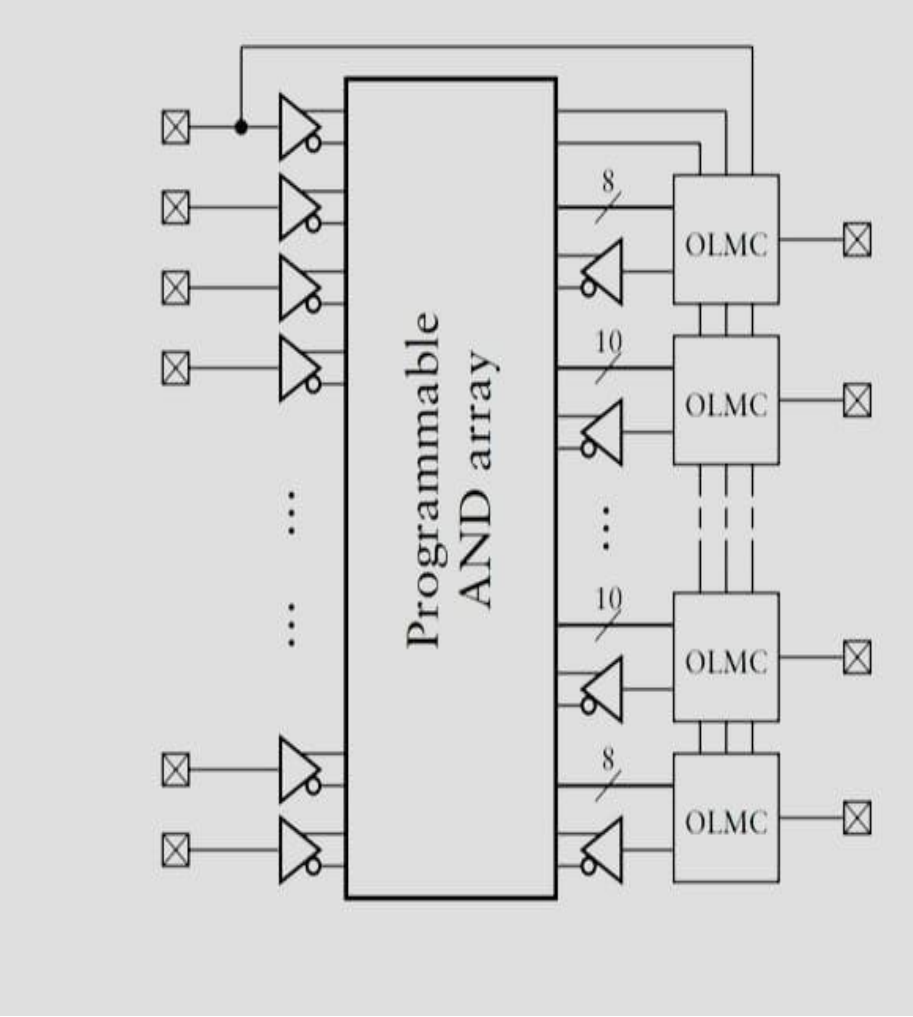
THE OUTPUT CIRCUIT OF A PAL16R8



Registered output circuit of a PAL16R8.

The feedback from the register output to the programmable AND array is useful for implementation of FSMs.

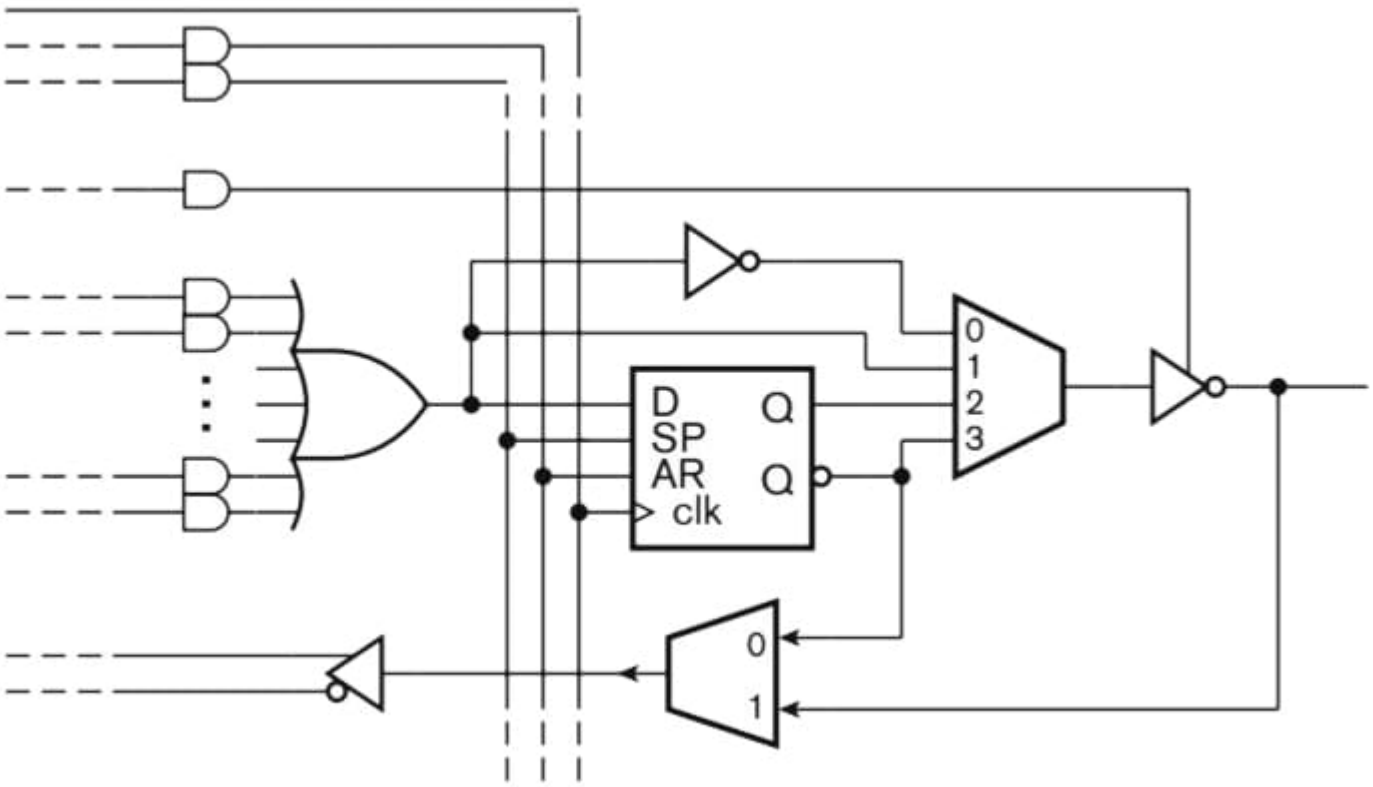
Generic array logic (GAL)



Generic array logic (GAL)

- Figure shows the internal circuit organization of the GAL22V10 component, now manufactured by Lattice Semiconductor Corporation,
- output logic macro cells (OLMCs) that replace the combinations of OR gates, registers and tristate drivers in PAL output circuits.
- Each OLMC includes circuit elements together with programmable multiplexers, allowing the output functionality to be determined as part of programming the component.

Figure shows the OLMC circuit for each section.



- The number of p-terms ranges from 8 for some sections to 16 for others.
- The output of the OR gate connects to a D flip-flop that has clock, asynchronous reset and synchronous preset signals in common with other OLMCs in the component.
- The four-input multiplexer allows selection of registered or combinational output, either inverting or noninverting. The two-input multiplexer allows either registered or combinational feedback, or, if the output driver is in the high-impedance state, direct input from the component pin.

Example: Design a priority encoder that has 16 inputs, I[0:15]; a four-bit encoded output, Z[3:0]; and a valid output that is 1 when any input is 1. Input I[0] has the highest priority, and I[15] the lowest priority. The design is to be implemented in a GAL22V10 component

Solution:

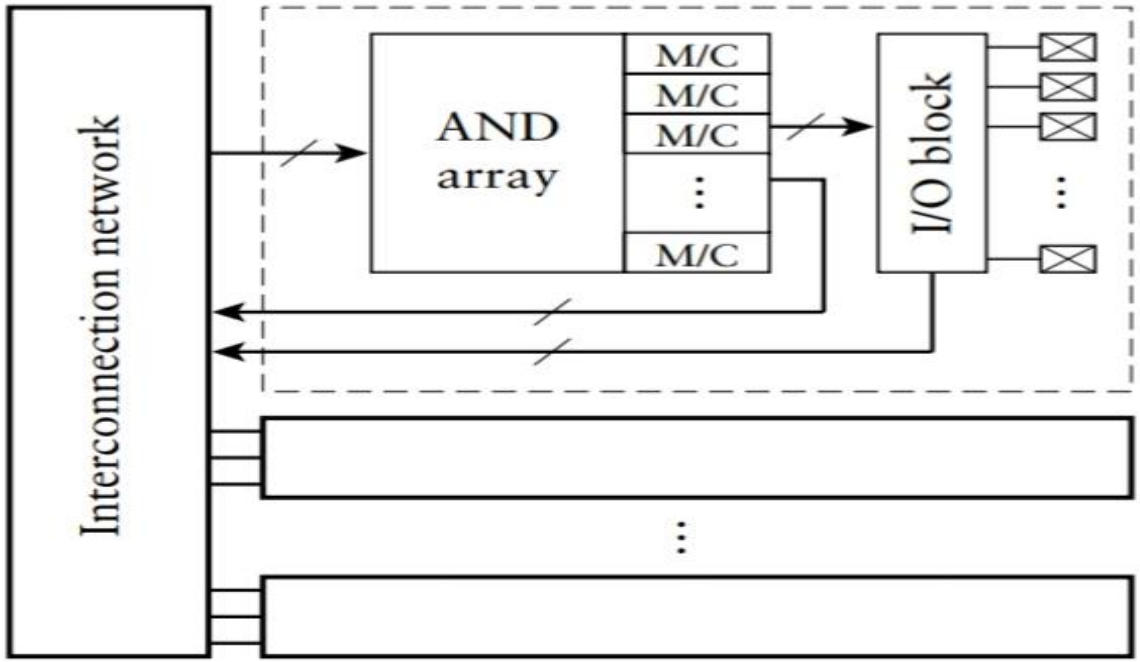
```
assign win[0] = I[0];
assign win[1] = I[1] & ~I[0];
assign win[2] = I[2] & ~I[1] & ~I[0];
...
assign win[15] = I[15] & ~I[14] & ~I[13] & ... & ~I[0];
assign Z[3] = win[15] | win[14] | win[13] | win[12]
| win[11] | win[10] | win[9] | win[8];
assign Z[2] = win[15] | win[14] | win[13] | win[12]
| win[7] | win[6] | win[5] | win[4];
assign Z[1] = win[15] | win[14] | win[11] | win[10]
| win[7] | win[6] | win[3] | win[2];
assign Z[0] = win[15] | win[13] | win[11] | win[9]
| win[7] | win[5] | win[3] | win[1];
assign valid = I[15] | I[14] | I[13] | ... | I[0];
```

- Each of the win elements can be implemented as a p-term in a row of the GAL AND array.
- Each Z output is thus the OR of 8 p-terms. Since each OLMC in a GAL22V10 component has at least 8 p-term inputs, these equations will fit in any of the sections.
- The valid output is the OR of 16 inputs, so it could fit in either of the two sections that have 16 p-term inputs to the OLMC.

- assign valid ~(~I[15] & ~I[14] & ~I[13] & ... & ~I[0]);

COMPLEX PLDS

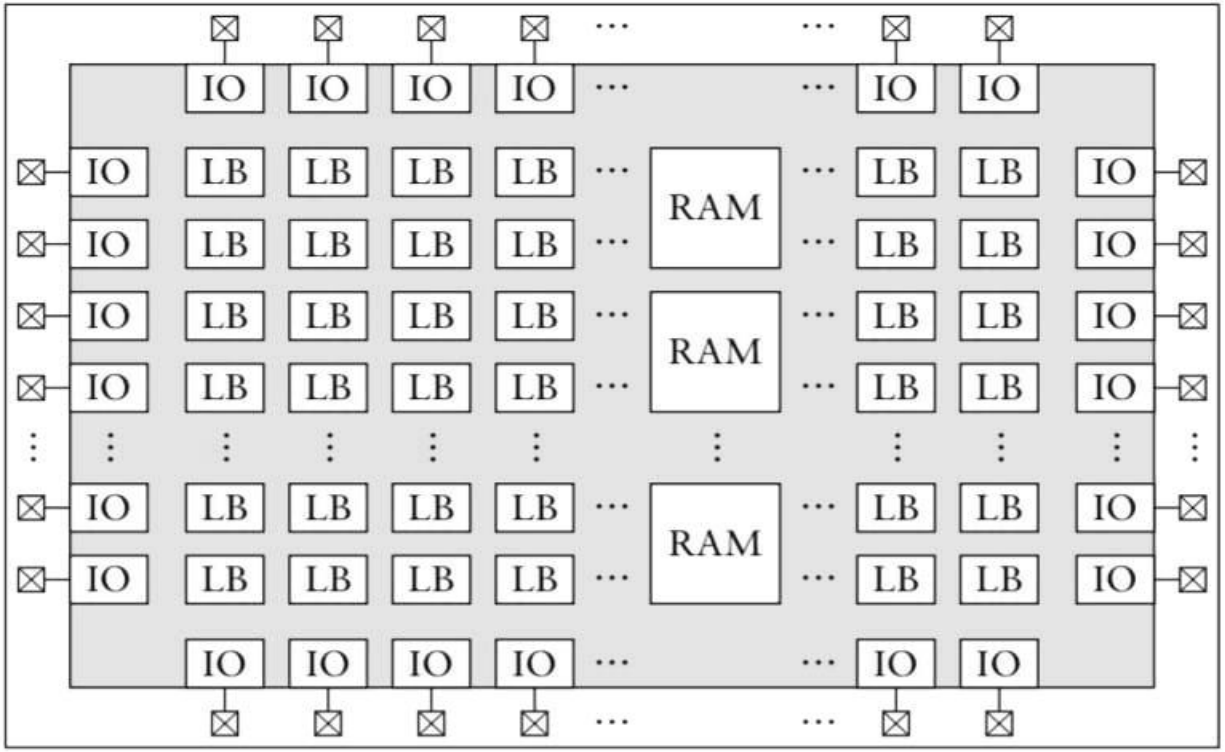
- CPLD as incorporating multiple PAL structures, all interconnected by a programmable network of wires, as shown in Figure



The internal organization of a CPLD.

- Each of the PAL structures consists of an AND array and a number of embedded macro cells (M/Cs in the figure).
- The macro cells contain OR gates, multiplexers and flip-flops, allowing choice among combinational or registered connections to other elements within the component, with or without logical negation, choice of initialization for flip-flops, and so on.
- Rather than using EPROM like technology, they use SRAM cells to store configuration bits that control connections in the AND-OR arrays and the select inputs of multiplexers

FIELD-PROGRAMMABLE GATE ARRAYS



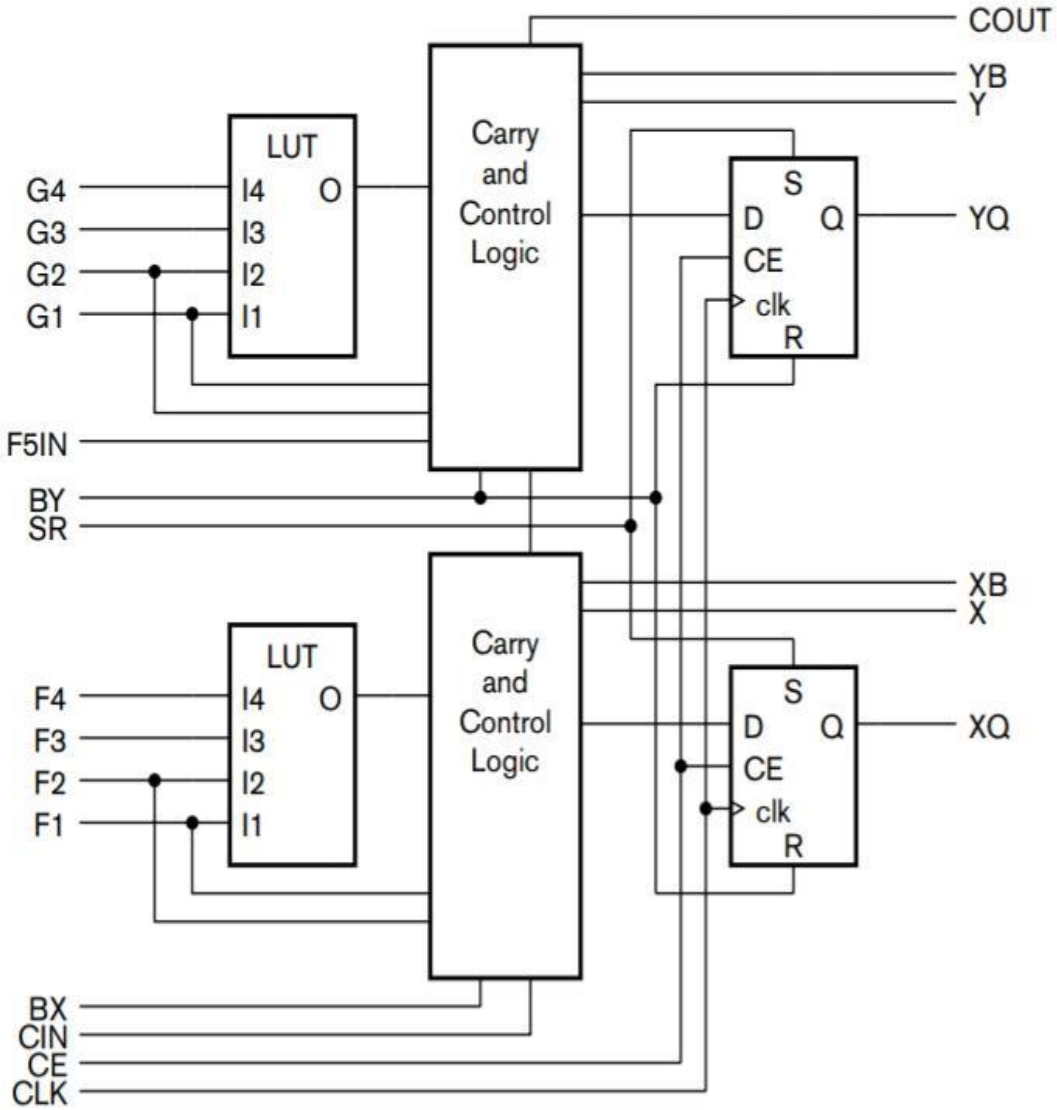
The internal organization of an FPGA consisting of logic blocks (LB), input/output blocks (IO), embedded RAM blocks (RAM) and programmable interconnections (shown in gray).

- FPGA: It is a programmable circuit structure, based on smaller programmable cells to implement logic and storage functions, combined with an interconnection network whose connections could be programmed.
- Increased capacity and performance.
- It include an array of logic blocks that can be programmed to implement simple combinational or sequential logic functions;
- input/output (I/O) blocks that can be programmed to be registered or nonregistered, as well as implementing various specifications for voltage levels, loading and timing; embedded RAM blocks; and a programmable interconnection network.
- Recent FPGAs also include special circuits for clock generation and distribution.

- In many FPGA components, the basic elements within logic blocks are small 1-bit-wide asynchronous RAMs called lookup tables (LUTs).
- The LUT address inputs are connected to the inputs of the logic block.
- By programming the LUT content differently, we can implement any Boolean function of the inputs.
- The logic blocks also contain one or more flipflops and various multiplexers and other logic for selecting data sources and for connecting data to adjacent logic blocks.

LOGIC BLOCK OF A XILINX SPARTAN-II FPGA

The circuit Of a slice of a Xilinx Spartan-II FPGA logic block.



- The logic block contains two such slices, together with a small amount of additional logic.
- Each slice consists of two 4-input LUTs, each of which can be programmed to implement any function of the four inputs.
- The carry and control logic consists of circuitry to combine the LUT outputs, an XOR gate and an AND gate for implementing adders and multipliers, as well as multiplexers that can be used to implement a fast carry chain.
- A number of the connections within the control and carry logic are governed by the programming of the FPGA. The logic block contains SRAM cells for these programming bits

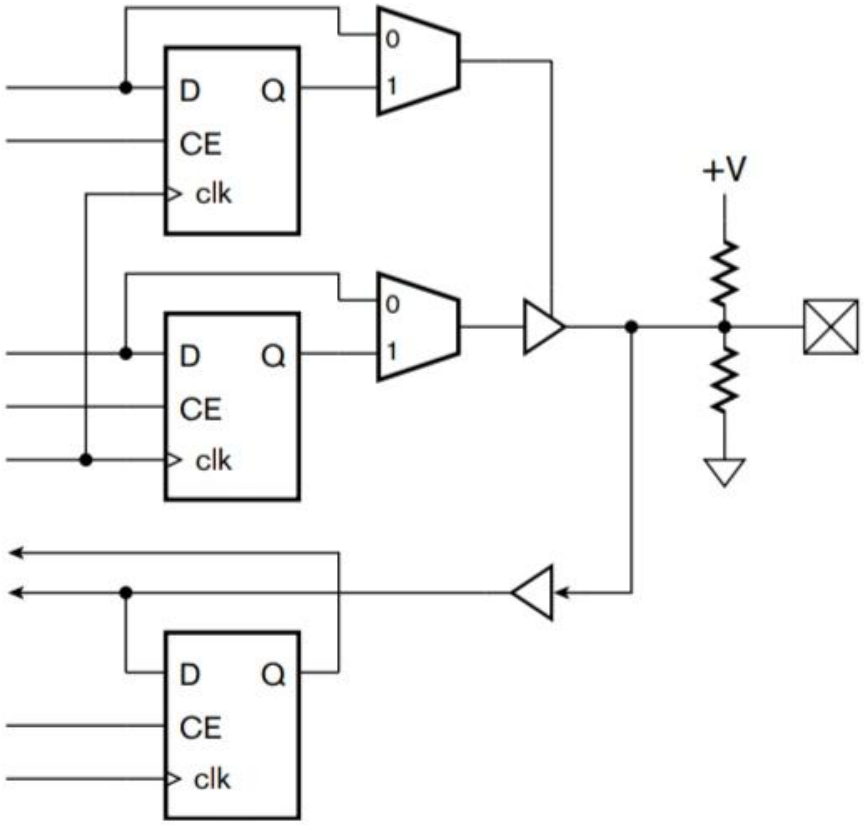
Other features:

- FPGAs have more fine-grained logic blocks.

Example: The logic block of Actel ProASIC3 FPGAs contains just enough gates, multiplexers and switches to implement combinational functions of three inputs, or a flip-flop with set or reset. Since each logic block is smaller and simpler, CAD software that maps a design into the FPGA resources may find it easier to perform its task without leaving parts of logic blocks unused.

The I/O block of an FPGA

Typical organization of an FPGA I/O block.



- The select inputs of the multiplexers are programmed to control whether the output is registered or combinational.
- The top flip-flop and multiplexer control the high-impedance state of the tristate driver that drives the pin as an output, and the middle flip-flop and multiplexer drive the output value.
- The output driver is programmable, allowing selection of logic levels (regular 5V TTL, low voltage TTL, or others) and control of the slew rate, that is, rate of voltage change at the output.
- The input buffer is likewise programmable, allowing selection of threshold voltage and other characteristics.
- The pull-up and pulldown resistors are programmable, allowing them to be connected and their resistance to be selected.

- The RAM blocks in an FPGA provide for storage of information to be processed by the FPGA circuitry.
- Typical modern FPGAs provide synchronous static RAM (SSRAM) blocks that can be programmed to be flow-through or pipelined, and that have two access ports that can be programmed to be read-only or read-write
- The RAM blocks are each relatively small in capacity, but can be interconnected to form larger memories
- Each of the various logic, I/O and RAM blocks on an FPGA connect to interconnection wires through programmable switches.

- There are two forms of FPGA that differ in the way they are configured.
- The first form uses RAM cells to store the configuration information. The main advantage of this approach is that an FPGA can be programmed after the chip has been assembled into a system, without the need for any separate handling during manufacture.
- The second main form of FPGA uses anti-fuses to configure the device. An anti-fuse, as its name suggests, is a conductive connection that is formed during programming, as opposed to being blown. Since programming is done by forming a connection, no storage is needed, either inside the FPGA or externally

PACKAGING AND CIRCUIT BOARDS

Need of IC packaging

- It protects the IC from moisture and airborne contaminants,
- It provides electrical connections, and it removes heat.

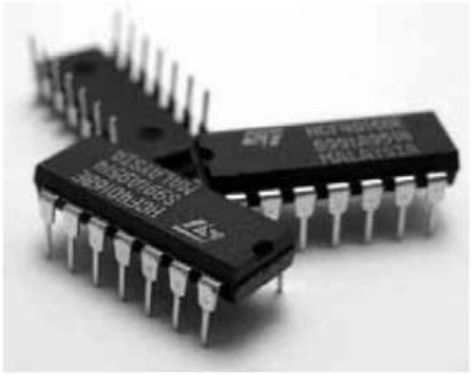
Different kinds of IC package

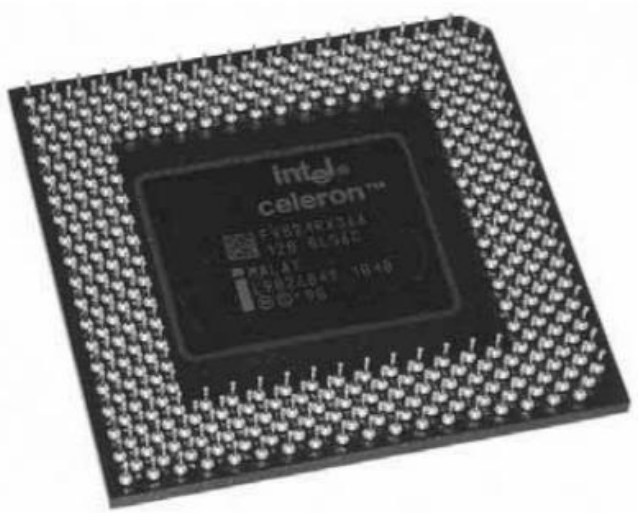
- The packaged ICs and other components in a system are assembled together on a printed circuit board (PCB).

Through-hole PCB: includes additional metal-coated holes into which IC package pins are inserted

FIGURE 6.19 A through-hole PCB.

- Dual in-line packages (DIPs) have two rows of pins with 0.1-inch spacing. These were among the first IC packages to be introduced, being used for SSI and MSI components, but are less common now.





Pin-grid array (PGA) package: More pins can be packaged, having up to 400 or more pins

- Surface-mount PCB: Components are mounted on the surface rather than being inserted in holes.

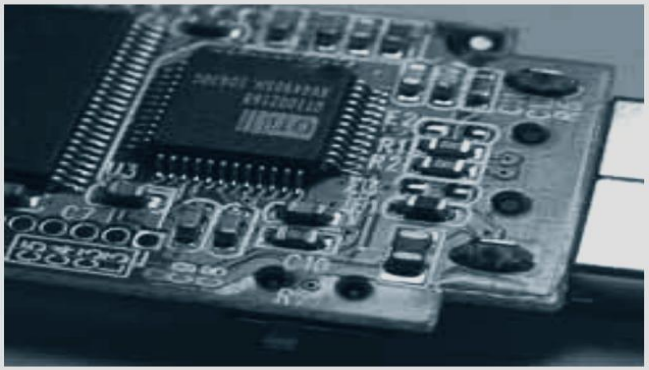
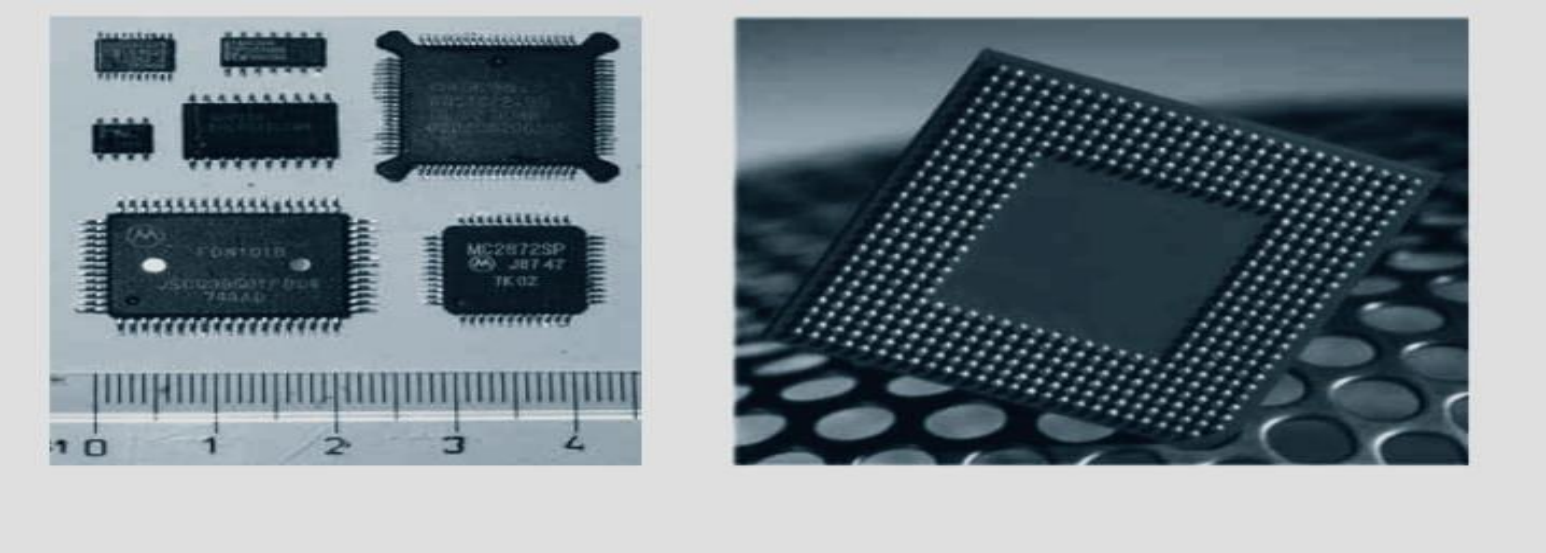


FIGURE 6.21 A surface-mount PCB.

- Quad flat-pack (QFP) packages have pins along all four sides, and are suitable for ICs with up to 200 or so pins. The spacing between pins varies from 1 mm for the packages with fewer pins, down to 0.65mm for the higher pin-count packages.

- The most common package in use now for high pin-count ICs is the ball-grid array (BGA) package. Depending on the package size and the pin spacing, BGA packages can accommodate ICs with up to 1800 pins.



Surface mounting IC packages: QFPs (left) and BGA (right).

- Multichip modules (MCMs): attach the bare chips to a ceramic substrate

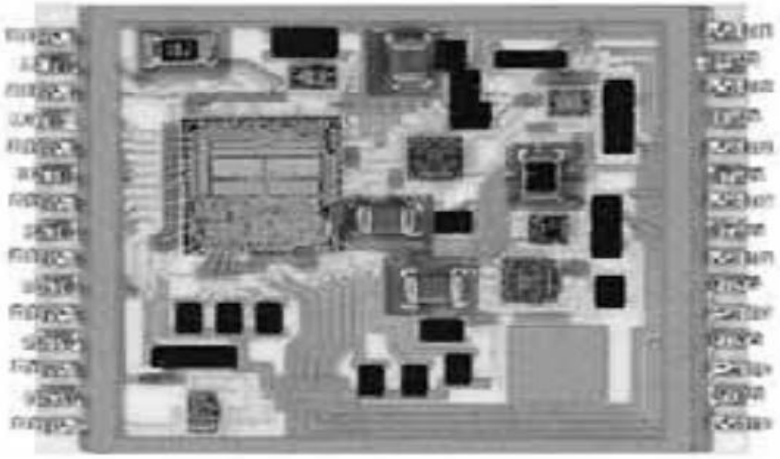


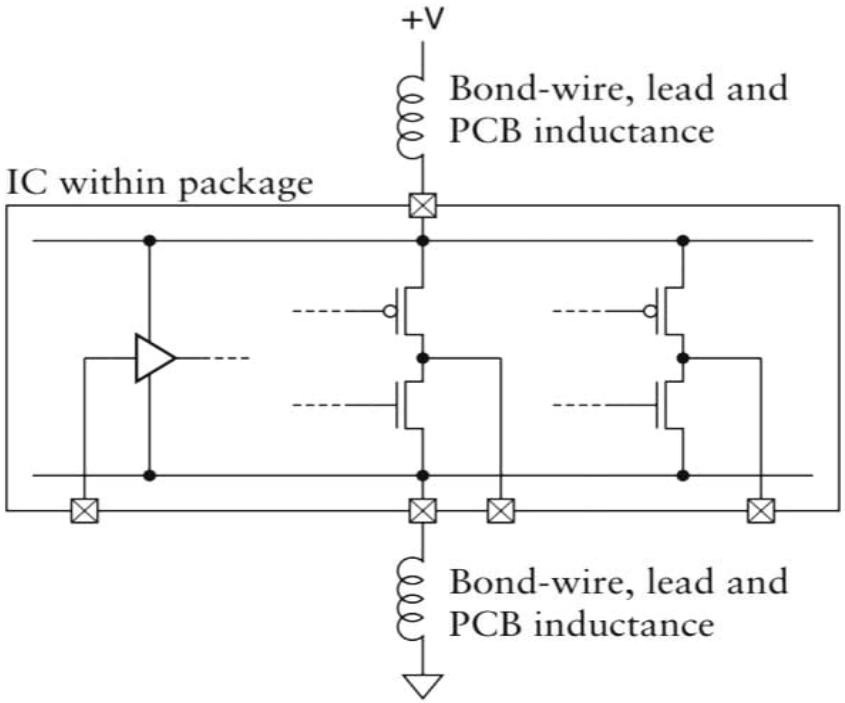
FIGURE 6.23 A multichip module.

MCMs is a High-density packaging technique.

INTERCONNECTION AND SIGNAL INTEGRITY

Signal integrity: SI is the ability of an electrical **signal** to carry information reliably and to resist the effects of high-frequency electromagnetic interference from nearby **signals**. Effects: Crosstalk, EM.

A major signal integrity issue in PCB design is ground bounce.



Remidies:

- Place bypass capacitors between power and ground
- Separate PCB layers for the ground and power supply
- Limit the rate of voltage change (the slew rate) and limit the drive current of the output drivers.
- Use differential signaling

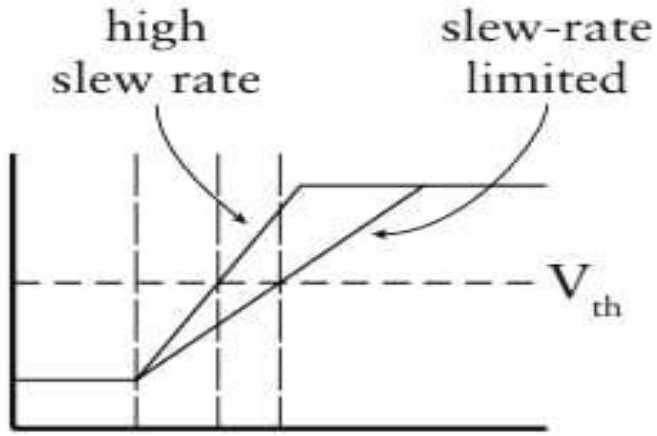
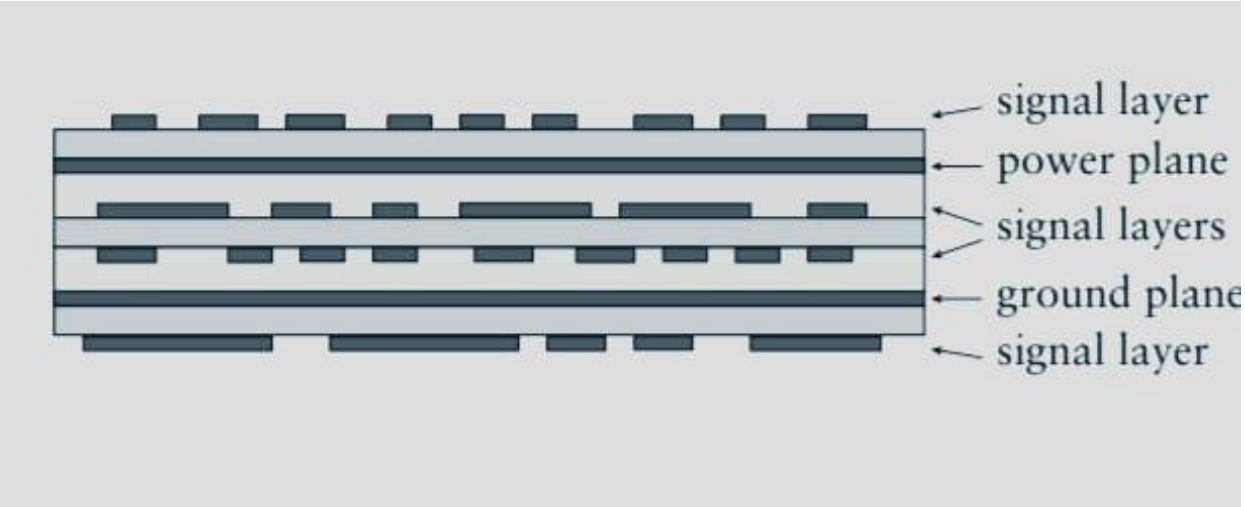
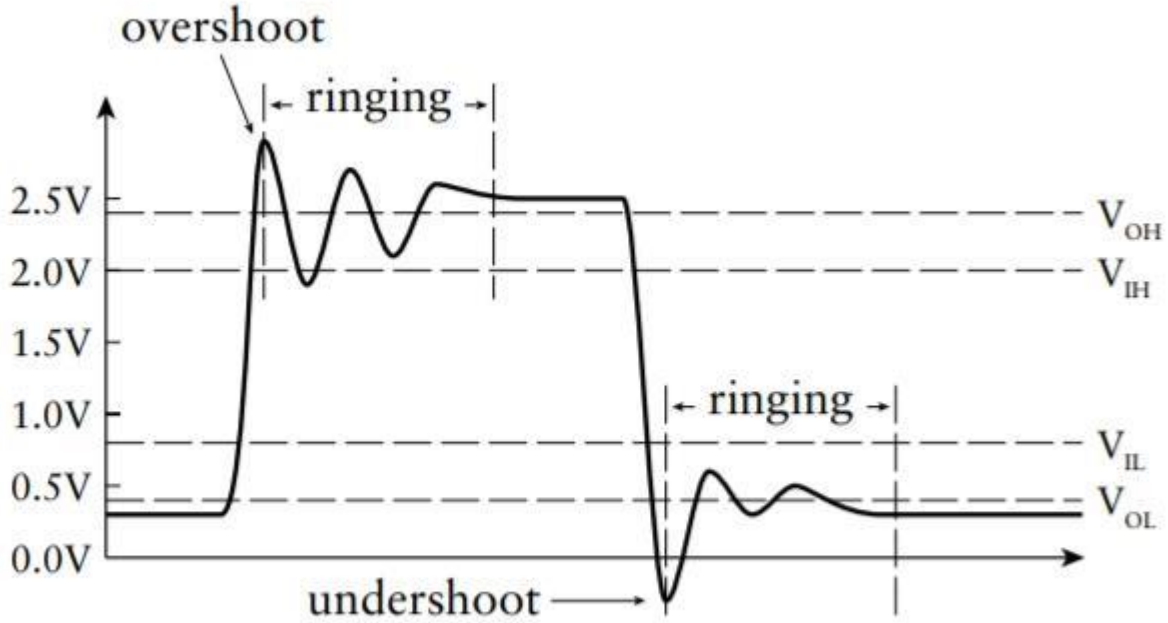


FIGURE 6.25 The effect of slew-rate limiting a signal. The signal takes longer to reach the threshold voltage V_{th}.



Transmission-line effects.

Another signal integrity issue for high-slew rate signals is noise due to transmission-line effects



- The main design techniques for managing transmission-line effects involve appropriate layout and proper termination of PCB traces.
- By running a trace of specific dimensions at a controlled distance between two ground or power planes in the PCB, we create a *strip line* transmission line with a controlled characteristic impedance. Where the transmission line effects are less critical, we can run a trace over just one plane, creating *micro strip* transmission line.
- For critical signals, we can adopt circuit designs and layouts that avoid placing receivers along the PCB trace, or that group them together at the receiving end
- can include termination resistors to ensure proper matching of drivers and receivers to the characteristic impedance of the transmission line

DIFFERETIAL SIGNALING

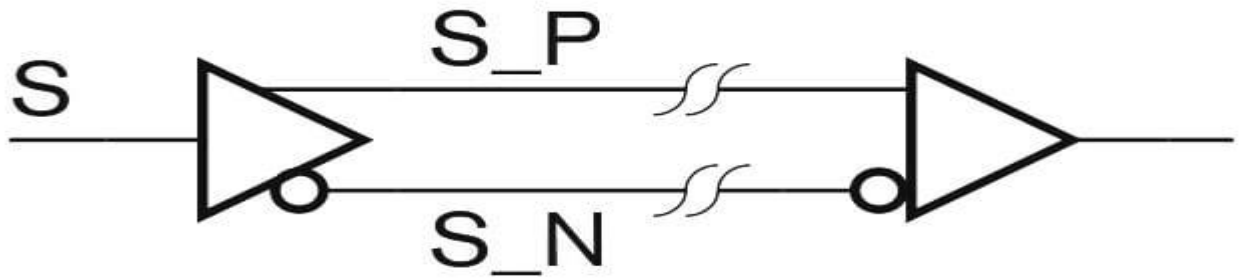


FIGURE 6.28 A differential driver and receiver.