Dayananda Sagar College of Engineering

Department of Electronics & Communication

2018- Scheme of Teaching and Examination

V SEMESTER (AUTONOMOUS COURSE 175 Credits)

Sl. No	Course Code	Course Title	Teaching Department	Teaching Hours / Week			Examination			Total Credits
				L	T	P	CIE	SEE	Total	
1	18HS5ICMEP	Management & Entrepreneurship	ECE	3	0	0	50	50	100	3
2	18EC5DCDSP	Digital Signal Processing	ECE	4	0	0	50	50	100	4
3	18EC5DCDCS	Digital Communication Systems	ECE	4	0	0	50	50	100	4
4	18EC5DCDSV	Digital System Design Using Verilog	ECE	3	0	0	50	50	100	3
5	18EC5DEXXX	Department Elective - A	ECE	3	0	0	50	50	100	3
6	18EC5DEXXX	Department Elective - B	ECE	3	0	0	50	50	100	3
7	18EC5DLDSP	DSP Lab	ECE	0	1	2	50	50	100	2
8	18EC5DLHDL	HDL Lab	ECE	0	1	2	50	50	100	2
9	18EC5DMEMT	Emerging Technologies	ECE	2	0	0	50	50	50	2
Total							450	450	900	**26**

ELECTIVE-A		ELECTIVE-B	
18EC5DEAPL	Advanced Programming language	18EC5DEBPP	Programming in Python
18EC5DEACO	Computer Organization	18EC5DEBSG	Satellite Communication & GPS
18EC5DEANE	Nanoelectronics	18EC5DEBAP	ARM Processor
18EC5DEAVI	Simulations of Electronic Systems using Virtual Instrumentation	18EC5DEBOS	Real Time Operating Systems

Emerging Technologies

a) The dynamics of industry is such that there are rapid advances in technology and systems that drive product, process and organizations. Therefore there is a need for providing opportunities to students for keeping abreast with the latest practices. This course on Emerging technologies is conceptualized with that need in mind.

b) This course would help in preparing the students to meet industry requirements and preparing them for their future professional career. The outcome of the course would be to ensure that the graduates are prepared to meet the future challenges and emerging needs of the society.

c) This course will have CIE only. No SEE for this course. In case the student fails to obtain the minimum CIE marks prescribed the student has to register for the course in fast track semester and earn the CIE marks

d) Scheme of Continuous Internal Evaluation (CIE): Evaluation will be done twice in the Semester.
   a. CIE 1: Quiz + Assignment + Test (10+10+30 = 50 marks)
   b. CIE 2: Quiz + Assignment + Test (10+10+30 = 50 marks)
   c. Total: Average of CIE 1 & CIE 2 = 50 marks (CIE to be obtained is ≥ 20)

MANAGEMENT AND ENTREPRENEURSHIP

Course Code: 18HS5ICMEP **Credits: 03**
L: P: T: S: 3: 0: 0: 0 **CIE Marks: 50**
Exam Hours: 03 **SEE Marks: 50**
Total Hours: 40

COURSE OBJECTIVES:

1. Understand the underlying principles of management.
2. To analyze and identify the functions of entrepreneurial activities and its prerequisites under practical conditions.
3. To develop and enhance one's decision making skills amidst competitive business market.

Course Outcomes: After completion of the course, the graduates will be able to

CO1	Apply the principles of management in business activities.
CO2	Use the managerial and entrepreneurial qualities & skills under real world condition.
CO3	Analyze the functions of Management & Entrepreneurship and apply those in practical situations.
CO4	Identify various schemes provided by government of India to support business enterprise.
CO5	Develop leadership skills to build a small scale industry.
CO6	Develop entrepreneurial personality, able to prepare project report and initiate SSI.

Mapping of Course outcomes to Program outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	-	-	-	-	-	3	3	2	2	-	-	-
CO2	-	-	-	-	-	3	3	2	2	-	-	-
CO3	-	-	-	-	-	3	3	2	2	-	-	-
CO4	-	-	-	-	-	3	3	2	2	-	2	-
CO5	-	-	-	-	-	3	3	2	2	-	2	-
CO6	-	-	-	-	-	3	3	2	2	-	2	-

Unit	Course Content	Hours	COs
1	MANAGEMENT: Introduction – Meaning – nature and characteristics of Management, Scope and Functional areas of management – Management as a science, art and profession – Management & Administration – Roles of Management, Levels of Management. PLANNING: Nature, importance and purpose of planning process –Objectives – Types of plans.	06	CO1 CO2
2	ORGANIZING AND STAFFING: Nature and purpose of organization –Principles of organization – types of organization – Departmentation –Committees-Centralization Vs Decentralization of authority and responsibility – Span of control – MBO and MBE (Meaning Only) Nature and importance of staffing. (Case studies discussion)	10	CO1 CO2
3	DIRECTING & CONTROLLING: Meaning and nature of directing –Leadership styles, Motivation (Definition),characteristics, motivational theories (Maslow's theory, theory 'X' and 'Y'), Meaning and steps in controlling – Essentials of a sound control system – Methods of establishing control (in brief).	06	CO3 CO4
4	ENTREPRENEUR: Meaning of Entrepreneur; Evolution of the Concept, Functions of an Entrepreneur, Types of Entrepreneur, and Entrepreneur – an emerging Class. Stages in entrepreneurial process; Role of entrepreneurs in Economic Development; Entrepreneurship – its Barriers, EDP and its objectives (Case studies discussion, role play / group discussion)	08	CO3 CO4
5	SMALL SCALE INDUSTRY: Definition; Characteristics; Objectives; Scope; role of SSI in Economic Development. Advantages of SSI, Steps to start an SSI, Impact of Liberalization, Privatization, Globalization on S.S.I, Effect of WTO/GATT. Overview of detailed project report/profile. Startup India: Benefits, Policies. Action plan- simplification and Handholding, Funding Support and incentives, Industry-Academia Partnership and Incubation. Salient features of Karnataka Startup Policy 2015-2020, Strategies encouraging entrepreneurship through NAIN. Venture capitalist, SSI funding schemes by banks and financial institutions, Government of India Initiatives on Thrust Areas, (Related case studies, supporting videos)	10	CO5 CO6

SELF-STUDY COMPONENT:

Preparation of Project report/Profile

Note:

1**.** At the end of the course students should have cultivated the ability to prepare project profile based on their selected business idea.

2. One Credit is allocated to project profile prepared by students.

3. Project profile/report shall be submitted before the end of the course.

Contents /Structure of project report/profile:

1. Introduction
2. Market potential
3. Basis and pre assumptions
4. Implementation schedule
5. Technical aspects
6. Financial aspects and analysis
8. Details of machinery and equipment/ service suppliers

TEXT BOOKS:

1. Principles of Management – P.C.Tripathi, P.N.Reddy – Tata McGraw Hill.
2. Dynamics of Entrepreneurial Development & Management – Vasant Desai – Himalaya Publishing House.
3. Entrepreneurship Development – Poornima.M.Charantimath – Small Business Enterprises – Pearson Education – 2006 (2 & 4).
4. Management & Entrepreneurship-N V R Naidu, IK International, 2008

REFERENCE BOOKS:

1 Management Fundamentals – Concepts, Application, Skill Development – Robers Lusier – Thomson.
2. Entrepreneurship Development – S.S.Khanka – S.Chand & Co.
3. Management – Stephen Robbins – Pearson Education/PHI – 17th Edition, 2003.
4. http://www.startupindia.gov.in/
5. http://startup.karnataka.gov.in/docs/Startup_Policy_Karnataka.pdf

Assessment Pattern:

CIE –Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	Tests	Preparation of Project Report/ Profile
Marks (Out of 50)	30	20
Remember	--	02
Understand	10	02
Apply	10	04
Analyze	05	04
Evaluate	05	03
Create		05

SEE –Semester End Examination Theory (50 Marks)

Bloom's Category	Marks Theory(50)
Remember	10
Understand	10
Apply	10
Analyze	10
Evaluate	10
Create	

DIGITAL SIGNAL PROCESSING

Course Code: 18EC5DCDSP
L : P : T : S : 4 : 0 : 1 : 0
Exam Hours: 03
Total Hours: 50

Credits : 04
CIE Marks : 50
SEE Marks : 50
CIE + SEE Marks : 100

COURSE OBJECTIVES:

1.	Understand concepts of DFT and its usage in linear filtering.
2.	Understand the basics of analog and digital filters.
3.	Design analog IIR filters.
4.	Design digital FIR and IIR filters.
5.	Realize filters using various filter structures.
6.	Understand the basics of Digital Signal Processors.

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Compute Discrete Fourier Transform (DFT) using direct method, using properties and using FFT algorithms and compare the computational efficiency.
CO2	Apply the knowledge of DFT to perform linear filtering and relate DFT with other transforms.
CO3	Design and analyze IIR filters.
CO4	Design digital FIR filters.
CO5	Illustrate filters using different structures.
CO6	Discuss the basics of Digital Signal Processors.

Mapping of Course outcomes to Program outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	2	1	-	-	-	-	-	-	-	-
CO2	3	3	2	1	-	-	-	-	-	-	-	-
CO3	3	3	2	2	-	-	-	-	-	-	-	-
CO4	3	3	2	2	-	-	-	-	-	-	-	-
CO5	3	2	1	1	-	-	-	-	-	-	-	-
CO6	2	1	1	1	-	-	-	-	-	-	-	-

Module	Course Content	Hours	COs
1	**Discrete Fourier Transforms (DFT):** DFT as a linear transformation, Relationship of DFT with other transforms. Properties of DFT and Numerical Examples. **Linear filtering using DFT:** Use of DFT in linear filtering. (Text book1)	10	CO1 CO2
2	**FFT algorithms:** Direct computation of DFT, Need for efficient computation of the DFT, Radix2 FFT algorithm for the computation of DFT and IDFT– Decimation in Time (DIT) and Decimation in Frequency (DIF) algorithms. **Analog IIR filter design:** Characteristics of commonly used analog filters, Design of Analog IIR Butterworth filters, Analog to analog frequency transformations. (Text book1,2)	10	CO1 CO2 CO3
3	**Digital IIR filter Design:** Design of digital IIR Butterworth filters using impulse invariance method and bilinear transformation method. **FIR filter design:** Symmetric and Antisymmetric FIR filters, Design of linear phase FIR filters using Windowing Method: Rectangular, Bartlet and Hamming windows. Design of linear phase FIR filter using frequency sampling Method. (Text book1,2)	10	CO3 CO4
4	**Structures for Realization of Discrete time systems:** Realization of FIR and IIR filters using direct form structures and cascade form structures, Lattice structure for FIR Filters. **Introduction to Digital Signal (DS) Processors:** Introduction, Digital Signal Processor Architecture- Von Neumann architecture and Harvard architecture, Fixed- and Floating-Point Format for DS processors. (Text1,4)	10	CO5 CO6
5	**Architecture and Instruction Set of the C6x Processor:** TMS320C6x Architecture, Functional Units, Fetch and Execute Packets, Pipelining, Registers, Linear and Circular Addressing Modes, TMS320C6x Instruction Set, Assembler Directives, Timers, Interrupts. Salient features of TMS320C6713 Digital Signal Processor. (Text3,4)	10	CO6

PRE-REQUISITES:

Signals and Systems, Engg. Maths – I / II / III / IV

NOTE:

1. Questions for CIE and SEE not to be set from self-study component.
2. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS:

Module 1 :	Frequency Domain Sampling & Reconstruction of Discrete Time Signals. Filtering of Long data sequences.
Module 2 :	Design of IIR Chebyshev filters from analog filters.
Module 3 :	Design of FIR Filters Using Kaiser Windows. Design of FIR Differentiator.
Module 4 :	FIR and IIR Filter Implementations in Fixed-Point Systems
Module 5 :	Programming Examples Using C, Assembly and Linear Assembly

TEXT BOOKS:

1.	Proakis & Manolakis, "Digital signal processing – Principles Algorithms & Applications", *Pearson education*, 4th Edition, New Delhi, 2007.
2.	A. Nagoorkani, "Digital Signal Processing", *Tata Mc Graw Hill*, 2nd Edn., New Delhi, 2012.
3.	Rulph Chassaing , "Digital Signal Processing and Applications with the C6713 and C6416 DSK", John Wiley & Sons, Inc., Publication, 2005
4.	Li Tan, "Digital Signal Processing", Academic Press, *Elsevier*, 2007.

REFERENCES BOOKS:

1.	Oppenheim & Schaffer, "Discrete Time Signal Processing", *PHI*, 2003.
2.	Sanjith K. Mitra, "Digital Signal Processing", *Tata Mc-Graw Hill*, New Delhi, India, 3rd Edition, 2010.
3.	Dimitris G. Manolakis, Vinay K. Ingle, "Applied DSP theory and Practice", *Cambridge University Press*,USA,2011.
4.	E.C. Ifeachor, and B. W. Jarvis, "Digital signal processing: A Practitioner's approach", Second Edition, *Pearson Education*, India, 2002.

On-Line Materials & Resources (NPTEL courses / Video lectures / you-tube Videos / Power points / On-line notes / web-links :

1.	www.nptelvideos.in/2012/12/digital-signal-processing.html
2.	https://www.analog.com/en/design-center/landing-pages/001/beginners-guide-to-dsp.html

Scheme of Evaluation of the CIE & Assessment Pattern :

Assignment : Only one assignment (open book test normally) will be of 10 marks & conducted in the class during the course of the semester (normally midway thro' the semester or in between 2nd & 3rd test). Generally, 2- 4 questions can be given which has to be solved in 1 hour duration, the assignment question has to be from the self-study component or it can be a coding demo done in the laptop & shown on the spot to the teacher in the class, the questions has to be set according to easy, medium, tough & severe and evaluation has to be done as per the assignment evaluation rubrics.

Quiz : There will be 1 quiz of 10 questions of 1 marks each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).

CIE : There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totaled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)			

Remember	5		2
Understand	5	5	2
Apply	10	5	3
Analyze	5		3
Evaluate	5		
Create			

SEE –Semester End Examination Theory (50 Marks)

Bloom's Category	Marks Theory(50)
Remember	10
Understand	10
Apply	10
Analyze	10
Evaluate	10
Create	

DIGITAL COMMUNICATION SYSTEMS

Course Code: 18EC5DCDCS | **Credits :** 04
L : P : T : S : 4 : 0 : 0 : 0 | **CIE Marks :** 50
Exam Hours : 03 | **SEE Marks :** 50
Total Hours : 40 | **CIE + SEE Marks :** 100

COURSE OBJECTIVES:

7.	To provide knowledge about source coding techniques.
8.	Analyze the channel capacity using Shannon's theorem.
9.	Introduce error control coding techniques.
10.	Get knowledge of theoretical aspects of detection of the transmitted data from the noisy received data
11.	Analyze the generation and detection of basic digital modulation techniques and arrive at the respective probability of errors and PSD.
12.	Develop communication system for specific application by taking example of Spread spectrum communication

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Apply the concept of Probability to measure information and capacity of channel.
CO2	Apply various channel coding techniques for error detection and correction.
CO3	Recognize the theoretical models, ideal receivers for the detection of the message from noisy received signal.
CO4	Analyze transmitter and receiver blocks for binary and quaternary modulation techniques to arrive at probability of error and Power Spectral Density.
CO5	Interpret Spread spectrum concepts, its types and applications.
CO6	Work in a team to simulate digital communication systems for different applications.

Mapping of Course outcomes to Program outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	2	1	-	-	-	-	-	-	-	-
CO2	3	3	2	1	-	-	-	-	-	-	-	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-
CO4	3	3	-	-	-	-	-	-	-	-	-	-
CO5	3	3	2	-	-	-	-	-	-	-	-	-
CO6	3	3	3	2	3	-	-	-	2	2	-	-

Module	Course Content	Hours	COs
1	**Information Theory:** Digital Communication block diagram, Information, Entropy, Shannon's Encoding Algorithm, Huffman coding, Discrete memoryless channels, BSC, channel capacity, Shannon Hartley Theorem and its implications.	8	CO1
2	**Error control codes:** Linear Block codes-G and H matrix, Generation and Decoding, Cyclic codes-g(x) and h(x), Encoding using an (n-k) bit shift register, syndrome calculation, Convolution Codes: Code generation-Time domain and Transfer domain approach and Code Tree	8	CO2
3	**Detection concepts:** Digital Communication block diagram, Model of DCS, Gram-Schmidt Orthogonalization procedure, geometric interpretation of signals, Optimum receivers-Matched and correlator receivers **ISI:** Inter Symbol Interference, eye pattern, adaptive equalization for data transmission	8	CO3 CO6
4	**Digital Modulation Techniques:** Digital Modulation formats, Coherent binary modulation techniques, Probability of error derivation of PSK and FSK, M-ary modulations-QPSK, QAM, PSD for different digital modulation techniques, Non-coherent binary modulation techniques -DPSK	8	CO4 CO6
5	**Spread Spectrum Modulation:** Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum, Frequency Hop Spread Spectrum, Applications	8	CO5 CO6

PRE-REQUISITES :

Knowledge of subjects like : Basics of Probability Theory, Signals and Systems, Analog communication.

NOTE :

3. Questions for CIE and SEE not to be set from self-study component.
4. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS :

Module 1 :	Mutual Information and its Properties, extension of source, other discrete channels, Simulation
Module 2 :	Types of Errors, Methods of Controlling Errors, Simulation.
Module 3 :	Matched filter for RF pulse, Simulation
Module 4 :	Simulation of digital modulation techniques: ASK, FSK, PSK, QPSK, DPSK
Module 5 :	Construction of state Diagrams, Counter Design and Maximum length sequence generation by simulation.

TEXT BOOKS :

5.	Simon Haykin, "Digital communication", ISBN-9971-51-205-X, *John Wiley & Sons* (*Asia*), *Pvt. Ltd*, 2008
6.	K. Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.
7.	Shu Lin, Daniel J Costello Jr., "Error Control Coding", Pearson Education Asia, Second Edition, 2011.
8.	John. G.Proakis, "Communication Systems Engineering", 2nd Edition, Pearson.
9.	John. G. Proakis, Masoud Salehi, "Digital Communications", Mac Graw Hill, 2008

REFERENCES BOOKS:

5.	Simon Haykin, "Digital and Analog Communication", John Wiley, India Pvt. Ltd., 2008.
6.	Bernard Sklar, "Digital Communication", Pearson Education, 2007.

7.	John G. Proakis , Masoud Salehi, Gerhard Bauch, "Contemporary Communication Systems Using MATLAB", 3rd Edition.
8.	B.P. Lathi, "Modern digital and analog Communication systems", Oxford University Press, 4thedn., 2010.
9.	Ranjan Bose, " ITC and Cryptography", TMH, 2nd edition, 2007

On-Line Materials & Resources (NPTEL courses / Video lectures / You-tube Videos / Power points / On-line notes / web-links :

3.	Mathuranathan Viswanathan, "Simulation of digital communication systems using Matlab".
4.	http://nptel.ac.in/course.php?disciplineId=117
5.	Shannon's Channel capacity : https://youtu.be/qzjdzjmQgA8
6.	Video on Information Theory : https://www.youtube.com/playlist?list=PLExwcJn_jXqFhXpUrVswwmRlKStQqwR6H
7.	Gram-Schmidt Orthogonalization procedure :https://youtu.be/fdsgsMP9JnA
8.	Digital Modulation Techniques: https://youtu.be/qGwUOvErR8Q
9.	Digital Modulation Techniques: https://youtu.be/cPSt8AzCYfg
10.	SSM: https://youtu.be/xltpukBncs8
11.	Frequency Hopping Spread Spectrum : https://youtu.be/CkhA7s5GIGc

Scheme of Evaluation of the CIE & Assessment Pattern :

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Quiz : There will be 1 quiz of 10 questions of 1 marks each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).
CIE : There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totaled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)	**30**	**10**	**10**
Remember	05	02	01
Understand	05	02	03
Apply	10	03	02
Analyze	10	03	02
Evaluate			02
Create			

SEE – Semester End Examination Theory (50 Marks)

Bloom's Category	Marks Theory (50)
Remember	10
Understand	10
Apply	15
Analyze	15
Evaluate	
Create	

DIGITAL SYSTEM DESIGN USING VERILOG

Course code: 18EC5DCDSV
L : P : T : S : 3 : 0 : 0 : 0
Exam Hours : 03
Total Hours : 40

Credits: 03
CIE Marks : 50
SEE Marks : 50

Course Objectives:

1. To study Verilog HDL in high-level synthesis of digital system designs.
2. To learn Verilog HDL for modelling, simulating and synthesizing various digital modules.
3. To study the additional features of Verilog HDL
4. To be able to design and develop Test bench for Combinational and sequential modules
5. To be able to design fixed and floating point arithmetic
6. To be able to design and implement synchronous sequential circuits using FSM

Course Outcomes:

After completion of the course, the graduates will be able to

CO1	Describe & model digital blocks of computing systems using Verilog hardware description language..
CO2	Apply hardware description language for writing test benches to check combinational & sequential modules.
CO3	Design clocked synchronous circuits and perform timing analysis
CO4	Analyze digital System and model using Verilog HDL.
CO5	Apply design Knowledge to FSM based digital Modules.
CO6	Synthesize and implement a given digital system.

Mapping of Course outcomes to Program outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	-	1							
CO2	3	2	1	-	1							
CO3	2	2	2	2								
CO4	2	2	1	-	1							
CO5	2	2	1	-	1							
CO6	2	2	1	-	1							

Unit	Contents of the Module	Hours	COs
1	Computer-Aided Design , Hardware Description Languages, Module modelling styles(ming bo lin), Verilog Description of Combinational Circuits, Data flow modelling-dataflow modelling, operands, operators, (ming bo lin), Verilog Modules, Verilog Assignments, Procedural Assignments), Modeling Flip-Flops Using Always Block, Always Blocks Using Event Control Statements.[Text book 1 and 3] Delays in Verilog, Compilation, Simulation, and Synthesis of Verilog Code , Simple Synthesis Examples,	08	

2	Verilog Models for Multiplexers, Modeling Registers and Counters Using Verilog Always Statements, Constants, Arrays, Loops in Verilog, Hazards(ming-bo-lin) Testing a Verilog Model **Additional topics in Verilog**: Verilog Functions, Verilog Tasks, Multivalued Logic and Signal Resolution, Built-in Primitives User-Defined Primitives, Named Association, Generate Statements , System Functions, File I/O Functions.[Text Book 1]	08	
3	**Sequential Basics**: Storage elements Counters[book 2], Sequential circuit timing : Propagation Delays, Setup, and Hold Times, Timing Conditions for Proper Operations, Glitches In Sequential Circuits, Synchronous Design. Tristate Logic and Busses [book 1]. Design flow of ASIC and FPGA based systems. Logic Synthesis, Synthesis Design Flow Coding guidelines[book1,2,3,6]	08	
4	**Numeric Basics**: Unsigned and Signed Integers, Fixed and Floating-point Numbers. [Book 2]. Sequential Design examples: BCD to 7 segment decoder, 32 bit adders, Shift and add Multiplier, Array Multiplier, signed integer / fraction multiplier. [Text book 1]	08	
5	**Synchronous sequential circuits:** Moore and Mealy machines, definition of state machines, FSM Design – overlapping and non-overlapping sequence detector. Design example- BCD to excess-3, NRZ to Manchester, Serial adder.[Book 1 and 4] **Implementation Fabrics**: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. [Book 2]	08	

Note:

1. Questions for CIE and SEE not to be set from self-study component.
2. Assignment Questions should be from self-study component only.

Pre-requisites: Logic design

Self-Study Component:

Unit 1 : Switch level Modelling,HDL code for flip-flops, carry look ahead adder
Unit 2 : SRAM Model Model for SRAM Read/Write System Rise and Fall Delays of Gates,Compliler directives
Unit 3 : Complex Multiplier, Asynchronous inputs
Unit 4 : Traffic Light Controller,Keypad scanner, binary divider
Unit 5 : Field programmable gate arrays (FPGA), Complex programmable logic devices (CPLDs).

Text Books:

1. Charles H Roth Jr., Lizy Kurian John, Byeong –kill-lee "Digital System Design using Verilog", *publisher Cengage learning*
2. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", *Elesvier*, 2010.
3. Ming-Bo Lin, "Digital System designs and Practices using Verilog HDL and FPGAs", *John Wiley & Sons*, 2008
4. Stephan Brown, Zvonko Vranesic "Fundamentals of Digital Logic with Verilog Design", Reprint 2016, *McGrawHill*, 2nd Edition, 2007
5. Micheal .D. Ciletti "Advanced Digital Design with the Verilog HDL" Prentice hall PTR, 2nd editions.ISBN:0136019285
6. Samir Palnitkar, "Verilog HDL-A guide to digital design and synthesis", *Sunsoft Press*, 1996

Reference Books:

1. Cyril Prasanna Raj, "Fundamentals of HDL", *Pearson / Sanguine*, 2010.
2. Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic Design with VHDL", Second Edition, *The McGraw-Hill*, 2009.
3. Nazeih M. Botros, "HDL Programming (VHDL and Verilog)", *John Wiley India Pvt. Ltd*. 2008
4. J. Bhaskar, "A Verilog HDL Primer", *BS Publications*, India.
5. Volnei A. Pedroni, "Circuit Design with VHDL", *PHI*, New Delhi, India
6. Wayne Wolf, "FPGA based system design", Reprint 2005, *Pearson Education* "Electronic Communication Systems", *McGrawHill*, 4th Edition,1992

E Books:

1. http://ece.niu.edu.tw/~chu/download/fpga/verilog.pdf
2. http://www.ics.uci.edu/~alexv/154/VHDL-Cookbook.pdf
3. http://access.ee.ntu.edu.tw/course/dsd_99second/2011_lecture/W2_HDL_Fundamentals_2011-03-02.pdf

MOOCs:

1. Fundamentals of HDL : https://www.youtube.com/watch?v=rdAPXzxeaxs&index=8&list=PLE3BC3EBC9CE15FB0
2. Digital system design with PLDs and FPGAs http://nptel.ac.in/courses/117108040/
3. Electronic Design Automation http://nptel.ac.in/courses/106105083/

Assessment Pattern:

CIE –Continuous Internal Evaluation Theory (50 Marks) :

Bloom's Category	**Tests - 3 CIEs**	**Assignments - 1 No.**	**AAT - 1 No.**
Marks (out of 50)	**30**	**10**	**10**
Remember		02	02
Understand	10	05	04
Apply	10	03	04
Analyze	05		
Evaluate			
Create	05		02

ADVANCED PROGRAMMING LANGUAGES

Course Code : 18EC5DEAPL
L : P : T : S : 3 : 0 : 1 : 0
Exam Hours : 03
Total Hours : 40

Credits : 03
CIE Marks : 50
SEE Marks : 50
CIE + SEE Marks : 100

COURSE OBJECTIVES:

1.	
2.	
3.	
4.	
5.	
6.	

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	
CO2	
CO3	
CO4	
CO5	
CO6	

Mapping of Course outcomes to Program outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1												
CO2												
CO3												
CO4												
CO5												
CO6												

Module	**Course Content**	**Hours**	**COs**
1	**Introduction OOPs:** Evolution and New Paradigm of programming, structured vs object oriented development, Elements of OOP – Objects, Classes, Abstraction, Encapsulation, Inheritance, Polymorphism, Pointers, Merits and Demerits of OO methodology.	8	
2	**OOP based Programming**: Classes and Objects, Modular programming with functions – Overloading, Overriding, Inline and Virtual functions, Operators overloading, Constructors & destructors, Structures & Unions.	8	
3	**Memories and the Memory Subsystem**: Static & Dynamic memory allocation, Dynamic objects, Generic programming templates, Stream computation with files, Exception handling,	8	

4	**Introduction to Java**: Java Lineage, Features and characteristics of Java, Java's influence on the Internet, Lexical issues, Data type conversion and casting, Type promotion rules. Variable length arguments.	8	
5	**Java Programming**: Super class variables, Defiing package, Finding package and CLASSPATH, Access protection, Importing packages, Interfaces – Defining, implementing, Nesting, Applying interfaces, Variables in interface .	8	

PRE-REQUISITES :

Knowledge of subjects like :

NOTE :

5. Questions for CIE and SEE not to be set from self-study component.
6. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS :

Module 1 :	
Module 2 :	
Module 3 :	
Module 4 :	
Module 5 :	

TEXT BOOKS :

	Mastering C++, K R Venugopal and Rajkumar Buyya 2nd Edition, Mc Graw Hill Education.
	The Complete Refernce Java, 7th Edition, Herbert Schildt, Mc Graw Hill Education.

REFERENCES BOOKS:

10.	
11.	
12.	
13.	

On-Line Materials & Resources (NPTEL courses / Video lectures / You-tube Videos / Power points / On-line notes / web-links :

12.	
13.	
14.	

15.	
16.	
17.	
18.	
19.	
20.	

Scheme of Evaluation of the CIE & Assessment Pattern :

Assignment : Only one assignment (open book test normally) will be of 10 marks & conducted in the class during the course of the semester (normally midway thro' the semester or in between 2nd & 3rd test). Generally, 2- 4 questions can be given which has to be solved in 1 hour duration, the assignment question has to be from the self-study component or it can be a coding demo done in the laptop & shown on the spot to the teacher in the class, the questions has to be set according to easy, medium, tough & severe and evaluation has to be done as per the assignment evaluation rubrics.

Quiz : There will be 1 quiz of 10 questions of 1 marks each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).

CIE : There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totaled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)			
Remember			
Understand			
Apply			
Analyze			
Evaluate			
Create			

SEE – Semester End Examination Theory (50 Marks)

Bloom's Category	**Marks Theory (50)**
Remember	
Understand	
Apply	
Analyze	
Evaluate	
Create	

COMPUTER ORGANIZATION

Course Code : 18EC5DEACO
L : P : T : S : 3 : 0 : 1 : 0
Exam Hours : 03
Total Hours : 40

Credits : 03
CIE Marks : 50
SEE Marks : 50
CIE + SEE Marks : 100

COURSE OBJECTIVES:

13.	To familiarize the students with basic structure of computers and machine instructions
14.	To Illustrate instructions and instruction sequencing with Assembly language programming.
15.	Design of different techniques for binary arithmetic units.
16.	Describe the operation of complete instruction execution.
17.	Determine the organizational details of memory design.
18.	To expose the students with different ways of communicating with I/O devices.

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Illustrate the concepts of Computer system.
CO2	Analyse design issues in terms of speed, technology, cost and performance.
CO3	Analyse different algorithms used to perform fast multiplication and division also represent the floating-point number in IEEE format
CO4	Carryout processor execution and its internal functional units.
CO5	Distinguish between organization of the memory, its hierarchy, design and working.
CO6	Describe the organization of I/O devices, storage, I/O performance and I/O access.

Mapping of Course outcomes to Program outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	1	-	-	-	-	-	-	-	-	-	-
CO2	3	2	1	-	-	-	-	-	-	-	-	-
CO3	3	2	2	-	-	-	-	-	-	-	-	-
CO4	3	2	2	-	-	-	-	-	-	-	-	-
CO5	3	2	2	-	-	-	-	-	-	-	-	-
CO6	3	2	2	-	-	-	-	-	-	-	-	-

Module	Course Content	Hours	COs
1	**Introduction :** Function and structure of a computer, Basic Operational Concepts, Bus Structures, Performance, Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement, Multiprocessor and Multicomputer. Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing, Addressing Modes, Assembly Language, Basic Input and Output Operations. Stacks and Queues, Subroutines, Additional Instructions, Encoding of Machine Instructions.	8	CO1 CO2
2	**Arithmetic:** Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers, Signed Operand Multiplication, Fast Multiplication, Integer Division, Floating-point Numbers and Operations.	8	CO3
3	**Basic Processing Unit** : Fundamental Concepts of a processor – Register Transfers, Performing an Arithmetic or Logic Operation, Fetching and storing a word from memory , Execution of a complete Instruction, Branch Instructions Multiple Bus Organization - Operations of a control unit, Hardwired control unit, A Complete Processor, Micro-programmed control unit.	8	CO4
4	**Memory Organization**: Basic Concepts, Semiconductor RAM Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations and Virtual Memories.	8	CO5
5	**Input /Output Organization**: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Exceptions, Direct Memory Access, Buses Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, USB	8	CO6

PRE-REQUISITES :

Knowledge of subjects : Computer concepts and Logic Design

NOTE :

7. Questions for CIE and SEE not to be set from self-study component.
8. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS :

Module 1:	History and Evolution of Computers, Types of Computers.
Module 2:	Atomic Instructions, Instruction Set for CISC and RISC architectures.
Module 3:	Pipelining and Super scalar Architecture, Branch Prediction Unit.
Module 4:	Different types of Memory, Types of SRAM, Read Only Memories, Secondary Storage.
Module 5:	External Devices, External Interface.

TEXT BOOKS:

10.	Carl Hamacher, ZvonkoVranesic, SafwatZaky, "Computer Organization", 5th Edition, McGraw Hill, India, 2002.
11.	D.A. Patterson and J.L. Hennessy, "Computer Organization and Design - The Hardware / Software Interface", Morgan Kaufmann, 1998.
12.	William Stallings, "Computer Organization and Architecture - Designing for Performance", Ninth Edition, Pearson India, 2013.

REFERENCES BOOKS:

14.	J.P. Hayes, "Computer Architecture and Organization", McGraw-Hill, 1998.
15.	Vincent P. Heuring& Harry F. Jordan, "Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.
16.	Govindarajalu, "Computer Architecture & Organization, Design Principles and Applications", 1st edition, Tata McGraw Hill, New Delhi, 2005.

On-Line Materials & Resources (NPTEL courses / Video lectures / You-tube Videos / Power points / On-line notes / web-links:

21.	NPTEL courses: • Fundamentals of computer system by Shri. Mangala Prasad Mishra, Indira Gandhi National Open University • Computer Architecture and organization by Prof.Indranil Sengupta, Prof.Kamalika Datta, IIT Kharagpur • Computer Fundamentals by Prof. Sanjay Tanwani, Devi Ahilya Viswavidyalaya, Indore
22.	Video lectures/ You Tube Videos • Gate Lectures by Ravindrababu Ravula • GATEBOOK Video Lectures • Engineering Drive • Introduction to Computer Organisation & Architecture | Bharat Acharya Education
23.	Online PPT's https://sites.google.com/site/uopcog/ppts
24.	Online notes https://www.geeksforgeeks.org/last-minute-notes-computer-organization/
25.	Web Links http://www.4shared.com/dir/32321017/5af1e412/Digital_Design__Computer_Archi.html

Scheme of Evaluation of the CIE & Assessment Pattern :

Assignment : Only one assignment (open book test normally) will be of 10 marks & conducted in the class during the course of the semester (normally midway through the semester or in between 2nd & 3rd test). Generally, 2- 4 questions can be given which has to be solved in 1 hour duration, the assignment question has to be from the self-study component

or it can be a coding demo done in the laptop & shown on the spot to the teacher in the class, the questions has to be set according to easy, medium, tough & severe and evaluation has to be done as per the assignment evaluation rubrics.

Quiz : There will be 1 quiz of 10 questions of 1 marks each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).

CIE : There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totaled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)	30	10	10
Remember	10	5	
Understand	10	5	
Apply	5		
Analyze	5		
Evaluate			
Create	-		

SEE – Semester End Examination Theory (50 Marks)

Bloom's Category	**Marks Theory (50)**
Remember	25
Understand	10
Apply	
Analyze	10
Evaluate	5
Create	

NANOELECTRONICS

Course Code : 18EC5DEANE **Credits :** 03
L : P : T : S : 3 : 0 : 1 : 0 **CIE Marks :** 50
Exam Hours : 03 **SEE Marks :** 50
Total Hours : 40 **CIE + SEE Marks :** 100

COURSE OBJECTIVES:

19.	To Introduce the Nanotechnology and the basic concepts of semiconductor physics.
20.	To describe the chemistry of carbon and carbon nano structures.
21.	To describe the structure, characteristics of MOSFET and CMOS technology.
22.	To analysis the advanced concepts in Nanoscale MOSFET also discuss the new technologies.
23.	To introduce the concepts of nanoelectronics in different applications.

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Apply the basic concepts of semiconductor physics to understand nanoelectronics
CO2	Analyze the concepts of Field Effect Transistor characteristics using band diagrams
CO3	Interpret the non-ideal effects of short channel MOSFETs
CO4	Discuss the basic knowledge of carbon nanostructures and carbon nano tubes
CO5	Gain the concepts of advanced MOSFET structures
CO6	Discuss the applications of nanoelectronics

Mapping of Course outcomes to Program outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	1	1									
CO2	3	2	1									
CO3	3	2	1	1								
CO4	3	1	1	1								
CO5	3	3	2	1								
CO6	3	2	1	1								

Module	Course Content	Hours	COs
1	**Nanotechnology**: What is nanotechnology? Classification of nanostructures, Bottom-Up and Top-Down Approaches, Impact of nanotechnology on conventional electronics. **Semiconductor Physics:** Classification of semiconductors, Energy bands in intrinsic and extrinsic silicon; Carrier transport: diffusion current, drift current, mobility and resistivity, Generation and recombination of carriers; Poisson and continuity equation	08	CO1
2	**Fundamentals of MOSFET:** Basic MOS Transistor-Types, Modes of operation, n-MOS operation, Drain Current, Threshold Voltage, CMOS technology, Ideal MOS Structure, Formation of three layers in MOS with energy band diagram, Ideal Capacitance-Voltage Characteristics.	08	CO2
3	**MOSFET- Additional Concepts:** Non ideal effects- sub threshold conduction, channel length modulation, mobility variation, velocity saturation, Ballistic Transport, MOSFET Scaling-Constant field scaling, Reason for Scaling, Short Channel Effects.	08	CO3
4	**Advanced MOSFET Structures:** SOI technology, Introduction to FINFET and its type, Gate All Around MOSFET, Tunnel FET **Carbon Nanostructures:** Nature of carbon bond, discovery of C-60, Carbon Nanotube- Types of carbon nanotubes, Fabrication, Properties and Applications.	08	CO4, CO5
5	**Applications:** Microelectromechanical Systems (MEMS), Nanoelectromechanical Systems (NEMS). Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, Resonant Tunneling Devices in Nanoelectronics, Nanodevices and Breakthroughs in Space Exploration	08	CO6

PRE-REQUISITES :

Knowledge of subjects like: Basic Electronics, Logic Design, Electronic Devices

NOTE :

9. Questions for CIE and SEE not to be set from self-study component.
10. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS :

Module 1:	Nano Structure- Size dependent properties
Module 2:	Conduction electrons and dimensionality
Module 3:	MOSFET Frequency Limitations
Module 4:	Radiation and Hot electron Effects, Threshold Voltage Modifications.
Module 5:	Molecular and super molecular switches.

TEXT BOOKS :

13.	G.Streetman, and S.K.Banerjee, "Solid State Electronic Devices," 7th edition, Pearson, 2014.
14.	Donald A.Neamen, "Semiconductor Physics and Devices",3rd edition, McGraw-Hill Education, 2010
15.	J.P.Colinge,"FinFETs and Other Multi-Gate Transistors",Springer, 2008

REFERENCES BOOKS:

17.	G. Cao, "Nanostructures and Nanomaterials: Synthesis, Properties and Applications", Imperial College Press, 2004.

18.	David Ferry, "Transport in Nano structures", Cambridge University press 2000.
19.	Y. Imry, "Introduction to Mesoscopic Physics", Oxford University press 1997.

On-Line Materials & Resources (NPTEL courses / Video lectures / You-tube Videos / Power points / On-line notes / web-links :

26.	**http://article.sapub.org/10.5923.j.nn.20130303.06.html**
27.	**https://nptel.ac.in/courses/117/108/117108047/**
28.	**http://thegateacademy.com/img/content/2018/03/Electronic-Devices-Circuits.pdf**
29.	**http://www.doe.carleton.ca/~tjs/AMOS.pdf**
30.	**https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-701-introduction-to-nanoelectronics-spring-2010/readings/MIT6_701S10_notes.pdf**
31.	**https://www.youtube.com/watch?v=wdNFCWLuC10**

Scheme of Evaluation of the CIE & Assessment Pattern :

Assignment : Only one assignment (open book test normally) will be of 10 marks & conducted in the class during the course of the semester (normally midway thro' the semester or in between 2nd & 3rd test). Generally, 2- 4 questions can be given which has to be solved in 1 hour duration, the assignment question has to be from the self-study component or it can be a coding demo done in the laptop & shown on the spot to the teacher in the class, the questions has to be set according to easy, medium, tough & severe and evaluation has to be done as per the assignment evaluation rubrics.

Quiz : There will be 1 quiz of 10 questions of 1 marks each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).

CIE : There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totaled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)			
Remember	10		03
Understand	10	05	03
Apply	10	05	02
Analyze			02
Evaluate			
Create			

SEE – Semester End Examination Theory (50 Marks)

Bloom's Category	**Marks Theory (50)**

Remember	10
Understand	20
Apply	10
Analyze	10
Evaluate	
Create	

PROGRAMMING IN PYTHON

Course Code : 18EC5DEBPP
L : P : T : S : 3 : 0 : 1 : 0
Exam Hours : 03
Total Hours : 40

Credits : 03
CIE Marks : 50
SEE Marks : 50
CIE + SEE Marks : 100

COURSE OBJECTIVES:

24.	Understand the core syntax and semantics of Python programming language. Define the need for working with the strings and functions.
25.	Illustrate the process of structuring the data using lists, dictionaries, tuples and sets.
26.	Indicate the use of regular expressions and built-in functions to navigate the file system.
27.	Infer the Object-oriented Programming concepts in Python.
28.	Understand the functional programming and Demonstrate the application of Numpy and pandas Modules.
29.	Implement an application using python programming.

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Apply the fundamental Python syntax and semantics to solve simple computational problems and Interpret the concepts of strings and functions in Python.
CO2	Identify the methods to create and manipulate lists, tuples and dictionaries.
CO3	Recognize the operations in file systems and regular expressions.
CO4	Illustrate object oriented concepts using python programming.
CO5	Analysis the functional programming and Demonstrate the application of Numpy and pandas Modules.
CO6	Design and develop applications for a given requirements.

Mapping of Course outcomes to Program outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	2	1	-	-	-	-	-	-	-	-
CO2	2	2	1	-	-	-	-	-	-	-	-	-
CO3	2	2	1	-	-	-	-	-	-	-	-	-
CO4	2	2	1	-	-	-	-	-	-	-	-	-
CO5	2	2	1	-	-	-	-	-	-	-	-	-
CO6	3	3	2	1	3	-	-	-	-	-	-	-

Module	Course Content	Hours	COs
1	**Introduction to Python Programming:** History, Application of Python, Identifiers, Keywords, Statements and Expressions, Variables, Operators, Data Types, Type Conversions. **Control Flow Statements:** The if, if…else, if…elif…else, Decision Control Flow Statement, Nested if Statement, The while, for Loop, The continue and break Statements, **Functions**: Built-In Functions, Commonly Used Modules, Function Definition and Calling the Function, The return Statement and void Function, **Strings:** Basic String Operations, Accessing Characters in String by Index Number, String Slicing and Joining, String Methods.	08	
2	**Lists:** Basic List Operations, Indexing and Slicing in Lists, Built-In Functions used on Lists, List Methods, The del Statement. **Dictionaries:** Creating Dictionary, Accessing and Modifying key: value Pairs in Dictionaries, Built-In Functions Used on Dictionaries, Dictionary Methods, The del Statement, **Tuples and Sets:** Basic Tuple Operations, Indexing and Slicing in Tuples, Built-In Functions Used on Tuples, Relation between Tuples and Lists, Relation between Tuples and Dictionaries, Tuple Methods, Sets, Set Methods, Traversing of Sets, Frozenset.	08	
3	**Files:** Types of Files, Creating and Reading Text Data, File Methods to Read and Write Data, Reading and Writing Binary Files, The Pickle Module, Reading and Writing CSV Files, **Regular Expression Operations:** Using Special Characters, Regular Expression Methods, Named Groups in Python Regular Expressions, Regular Expression with glob Module.	08	
4	**Object-Oriented Programming,** Classes and Objects, Creating Classes in Python, Creating Objects in Python, The Constructor Method, Classes with Multiple Objects, Class Attributes versus Data Attributes, Encapsulation, Inheritance, The Polymorphism.	08	
5	**Packages in Python:** Functional Programming: Lambda, Iterators , Generators ,List Comprehensions, NumPy with Python: NumPy Arrays Creation Using array() Function, Array Attributes, NumPy Arrays Creation with Initial Placeholder Content, Integer Indexing, Array Indexing, Boolean Array Indexing, Slicing and Iterating in Arrays, Basic Arithmetic Operations on NumPy Arrays, Mathematical Functions in NumPy , Changing the Shape of an Array, Stacking and Splitting of Arrays, Broadcasting in Arrays, Pandas, Pandas Series, Pandas Data Frame, Altair	08	

NOTE :

11. Questions for CIE and SEE not to be set from self-study component.
12. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS:

Module 1 :	Precedence and Associativity, Indentation, Comments, Reading Input, Print Output, The type() Function and Is Operator, Dynamic and Strongly Typed Language, Catching Exceptions Using try and except Statement, Scope and Lifetime of Variables, Default Parameters, Keyword Arguments, *args and **kwargs, Command Line Arguments. Formatting Strings, Programming using tool.
Module 2 :	Using zip () Function, Programming using tool.
Module 3 :	Python os and os.path Modules. Programming using tool.
Module 4 :	Programming using tool.
Module 5 :	JSON and XML in python, using JSON with python, using XML with python, Develop an application using Python.

TEXT BOOKS :

16.	Kenneth Lambert – "Fundamentals of Python_ Data Structures", *Cengage Learning PTR* (2013).
17.	Gowrishankar S, Veena A, "Introduction to Python Programming", 1st Edition, *CRC Press/Taylor & Francis*, 2018. ISBN-13: 978-0815394372.
18.	Mark Lutz, "Programming Python", 4th Edition, *O'Reilly Media*, 2011.ISBN-13: 978-9350232873.
19.	Zed A. Shaw, ""Learn Python 3 the Hard Way: A Very Simple Introduction to the Terrifyingly Beautiful World of Computers and Code", Addison-Wesley Professional, Year: 2017, ISBN: 0134692888, 9780134692883.

REFERENCES BOOKS:

20.	Cody Jackson ,"Learning to Program using Python", Second Edition, 2014.
21.	Michael DAWSON, "Python Programming",3rd Edition, Course technology PTR, 2010
22.	Charles R. Severance, "Python for Everybody: Exploring Data Using Python 3", 1st Edition, *CreateSpace Independent Publishing Platform*, 2016. http://do1.drchuck.com/pythonlearn/EN_us/pythonlearn.pdf
23.	Allen B. Downey, "Think Python: How to Think Like a Computer Scientist", 2nd Edition, *Green Tea Press*, 2015. (http://greenteapress.com/thinkpython2/thinkpython2.pdf)

On-Line Materials & Resources (NPTEL courses / Video lectures / You-tube Videos / Power points / On-line notes / web-links :

32.	https://nptel.ac.in/courses/106/106/106106182/
33.	https://nptel.ac.in/courses/115/104/115104095/
34.	https://www.edx.org/learn/python
35.	https://www.coursera.org/courses?query=python
36.	https://www.udemy.com/topic/python/
37.	https://online-learning.harvard.edu/subject/python
38.	https://www.codecademy.com/learn/learn-python
39.	https://www.geeksforgeeks.org/python-programming-language/
40.	https://www.lynda.com/Python-training-tutorials/415-0.html
41.	https://www.python.org/

Scheme of Evaluation of the CIE & Assessment Pattern :

Assignment : Only one assignment (open book test normally) will be of 10 marks & conducted in the class during the course of the semester (normally midway thro' the semester or in between 2nd & 3rd test). Generally, 2- 4 questions can be given which has to be solved in 1 hour duration, the assignment question has to be from the self-study component or it can be a coding demo done in the laptop & shown on the spot to the teacher in the class, the questions has to be set according to easy, medium, tough & severe and evaluation has to be done as per the assignment evaluation rubrics.

Quiz : There will be 1 quiz of 10 questions of 1 marks each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).

CIE : There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totaled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)	30	10	10
Remember	10		
Understand	10		
Apply	10		05
Analyze		05	05
Evaluate		05	
Create			

SEE – Semester End Examination Theory (50 Marks)

Bloom's Category	**Marks Theory (50)**
Remember	10
Understand	10
Apply	10
Analyze	10
Evaluate	5
Create	5

SATELLITE COMMUNICATION & GPS

Course Code : 18EC5DEBSG
L : P : T : S : 3 : 0 : 1 : 0
Exam Hours : 03
Total Hours : 40

Credits : 03
CIE Marks : 50
SEE Marks : 50
CIE + SEE Marks : 100

COURSE OBJECTIVES:

30.	To learn about the communication technology of satellite communication, advantages and applications.
31.	To understand the functioning of various sub-systems of a satellite.
32.	To predict the losses that occur in the link.
33.	To calculate link budget equation.
34.	To understand the basics of GPS systems, signal structure and applications.
35.	To understand the GPS signal acquisition and tracking process.

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Employ the concepts of Satellite communication to maintain the satellite in its orbit and to have a reliable communication.
CO2	Analyze the different satellite subsystems in order to know its internal functioning.
CO3	Predict different types of losses that occur in the link between satellite and earth.
CO4	Compute the link power budget equations and analyze different noises that occur in satellite system.
CO5	Discuss the GPS systems, signal structure and applications.
CO6	Analyze the GPS signal acquisition and tracking.

Mapping of Course outcomes to Program outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	-	-	-	-	-	-	-	-	-
CO2	3	3	2	-	-	-	-	-	-	-	-	-
CO3	3	3	1	-	-	-	-	-	-	-	-	-
CO4	3	3	2	1	-	-	-	-	-	-	-	-
CO5	3	3	1	-	-	1	-	-	-	-	-	-
CO6	3	3	2	-	-	-	-	-	-	-	-	-

Module	Course Content	Hours	COs
1	**Overview of Satellite Communication:** Introduction, Advantages of Satellite communication, Frequency Allocations for Satellite Services, Satellite orbits, Kepler laws, Definitions of terms for earth orbiting satellites, Orbital elements, Apogee and perigee heights, Orbit perturbations, Inclined orbits-Calendars, Universal Time, Sidereal Time, Orbital Plane. **Geostationary orbit:** Introduction, Antenna look angles, Polar mount antenna, Limits of visibility, Earth eclipse of satellite, Sun transit outage. (Text Book 1 & 3)	08	CO1
2	**Satellite Subsystems:** Transponders, Satellite antennas (concept only), Satellite Control System, Power system, Telemetry, Tracking and Command system (TTC), Structures, Thermal Control System, Reliability, Steps in satellite mission realization. Test and Evaluation of the Satellite components, Satellite subsystems and Satellite as a system. **Radio wave Propagation:** Atmospheric Losses, Ionospheric effects, Rain Attenuation, Other Propagation Impairments. (Text Book 1 & 3)	08	CO2 CO3
3	**Satellite Link Design:** The space link: EIRP, Transmission losses, Link power budget equations, System noise, Carrier to Noise ratio, Uplink C/N_o, Downlink C/N_o, Combined uplink and downlink C/N_o ratio. **Interference:** Interference between satellite circuits, Combined C/I due to interference. (Text Book 1)	08	CO3 CO4
4	**Introduction and Fundamentals of Satellite Navigation:** Introduction, Condensed GPS Program History, GPS Overview, PPS, SPS, Concept of Ranging Using TOA Measurements, Reference Coordinate Systems: Earth-Centered Earth-Fixed Coordinate System, Position Determination Using PRN Code, GPS Satellite Constellation Description, User Receiver, Navigation Message Format, Modernized GPS Signals. (Text Book 2)	08	CO5
5	**Satellite Signal Acquisition, Tracking:** GPS Receiver Code and Carrier Tracking, Measurement Errors and Tracking Thresholds, Signal Acquisition, Sequence of Initial Receiver Operations. Use of Digital Processing, Considerations for Indoor Applications. **GPS Applications:** Civil Navigation Applications of GNSS, GIS, Government and Military Applications. (Text Book 2)	08	CO5 CO6

PRE-REQUISITES :

Knowledge of subjects like : Analog Communication, Signals and Systems.

NOTE :

13. Questions for CIE and SEE not to be set from self-study component.
14. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS :

Module 1 :	Sun synchronous orbit, Launching orbits.
Module 2 :	Isotropic antenna, Phased array antenna
Module 3 :	Effects of Rain, Rain fade margin, Inter modulation noise.
Module 4 :	Earth-Centered Inertial Coordinate System, World Geodetic System, Obtaining User Velocity, Time and GPS, Space Segment Phased Development
Module 5 :	Carrier Tracking Loops, Code Tracking Loops, Loop Filters

TEXT BOOKS :

20.	Dennis Roddy, "Satellite Communication", 3rd edition, *Tata McGraw Hill Education*, 2001.
21.	Elliott D. Kaplan and Christopher J. Hegarty, "Understanding GPS Principles and Applications", 2nd Edition, *Artech House Inc.*, 2006.
22.	S.K Raman, "Fundamentals of Satellite Communications", *Pearson Education*, 2011.

REFERENCES BOOKS:

24.	Timothy Pratt, Charles Bostien, Jeremy Allnut, "Satellite Communications", 2nd edition, *John Wiley Pvt. Ltd & Sons Publications*, 2008.
25.	W.L. Pitchand, H.L. Suyderhoud, R.A. Nelson, "Satellite Communication Systems Engineering", 2nd Edition, *Pearson Education*, 2007
26.	Bruce R. Elbert, "Introduction to Satellite Communication", 3rd Edition, *Artech House*, UK, 2008.

On-Line Materials & Resources (NPTEL courses / Video lectures / You-tube Videos / Power points / On-line notes / web-links :

42.	https://nptel.ac.in/courses/117/105/117105131/
43.	https://gnss-sdr.org/
44.	https://www.isro.gov.in/applications/satellite-communication
45.	https://www.gps.gov/systems/gps/space/
46.	https://www.faa.gov/about/office_org/headquarters_offices/ato/service_units/techops/navservices/gbng/

Scheme of Evaluation of the CIE & Assessment Pattern :

Assignment : Only one assignment (open book test normally) will be of 10 marks & conducted in the class during the course of the semester (normally midway thro' the semester or in between 2nd & 3rd test). Generally, 2- 4 questions can be given which has to be solved in 1 hour duration, the assignment question has to be from the self-study component

or it can be a coding demo done in the laptop & shown on the spot to the teacher in the class, the questions has to be set according to easy, medium, tough & severe and evaluation has to be done as per the assignment evaluation rubrics.

Quiz : There will be 1 quiz of 10 questions of 1 marks each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).

CIE : There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totaled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)			
Remember	10		02
Understand	10	05	02
Apply	10	05	04
Analyze			02
Evaluate			
Create			

SEE – Semester End Examination Theory (50 Marks)

Bloom's Category	**Marks Theory (50)**
Remember	10
Understand	20
Apply	10
Analyze	10
Evaluate	
Create	

ARM PROCESSOR

Course Code: 18EC5DEBAP | **Credits:** 03
L: P: T: S: 3: 0: 1: 0 | **CIE Marks:** 50
Exam Hours: 03 | **SEE Marks:** 50
Total Hours: 40 | **CIE + SEE Marks:** 100

COURSE OBJECTIVES:

36.	To provide exposure to ARM processors (RISC system)
37.	To impart knowledge on ARM fundamental instruction set and also THUMB instruction sets with assembly level coding.
38.	To disseminate knowledge on handling exceptions (errors, interrupts and other events from external system) on ARM processors efficiently to improve its performance.
39.	To deliver comprehensive knowledge on cache memory and memory protection units.

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Understand the fundamental concepts of ARM and RISC design philosophy.
CO2	Apply the knowledge of ARM instruction set for efficient assembly level coding.
CO3	Analyze THUMB state in assembly level ARM programming.
CO4	Analyze the concepts of exception handling and interrupts of ARM.
CO5	Understand the need of cache memory and memory protection units in embedded systems.
CO6	Compare and contrast ARM processor with others processors in terms of instruction and memory architectures.

Mapping of Course outcomes to Program outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2										
CO2	3	2	1									
CO3	3	2	1									
CO4	3	2	1									
CO5	3	2	-									
CO6	3	-	-									

Module	Course Content	Hours	COs
1	**ARM Embedded Systems: The** RISC Design Philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software. **Fundamentals of ARM**: ARM core data flow model, Registers, Current Program Status Register, Core Extensions, Architecture Revisions **ARM Instruction Set:** Data processing instructions, Branch Instructions, Load Store Instructions, Software Interrupt Instruction, Program status Register Instructions, Loading Constants., and Conditional Execution.	8	CO1
2	**Introduction to the THUMB Instruction set:**	8	CO3

	Thumb register Usage, ARM-Thumb Interworking, other branch instructions, Data Processing Instructions, Single register Load – store Instructions, Multiple register Load Store Instruction, Stack Instructions, and Software Interrupt Instruction.		
3	**ARM Programming:** General Structure of ARM assembly module, Assembler directives- AREA, ENTRY, END, SPACE, DCD, DCB, DCW, DCI, DCQ, EQU, EXPORT, ALIGN, CODE16, CODE32, DATA Simple ALP programs and verify in different IDE environment.	8	CO2
4	**Interrupts & Exception Handling:** Exception handling- ARM processor exceptions and modes, vector table, exception priorities, link register offsets. Interrupts- assigning interrupts, interrupt latency, IRQ and FIQ exceptions with example-code for enabling and disabling IRQ and FIQ exceptions, Comparison between exception and interrupts. Interrupt handling schemes- nested interrupt handler, non-nested interrupt handler. Basic interrupt stack design.	8	CO4
5	**Caches and memory management:** The Memory Hierarchy and Cache Memory, Cache architecture (Basic architecture, operation, relationship between main memory and cache) **Memory protection unit: Protected Regions,** Overlapping Regions, Background Regions Initializing the MPU, Caches, and Write Buffer**,** Defining Region Size and Location, Access Permission, Setting Region Cache and Write Buffer Attributes, Enabling Regions and the MPU Memory management units:	8	CO5

PRE-REQUISITES :

Knowledge of subjects like : Microcontrollers.

NOTE:

15. Questions for CIE and SEE not to be set from self-study component.
16. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS:

Module 1:	Pipelining concepts, Comparison of arm with other processors. ARMv5E Extension instructions.
Module 2:	Compare ARM and THUMB instructions.
Module 3:	C programming for ARM
Module 4:	Interrupt handling schemes. (Non nested Interrupt Handler, Nested Interrupt Handler, Reentrant Interrupt Handler, Prioritized Simple Interrupt Handler, Prioritized Standard Interrupt Handler, Prioritized Direct Interrupt Handler, Prioritized Grouped Interrupt Handler VIC PL190 Based Interrupt Service Routine)
Module 5:	Moving from an MPU to an MMU, How Virtual Memory Works, Defining Regions Using Pages, Multitasking and the MMU, Memory Organization in a Virtual Memory System.

TEXT BOOKS:

23.	Andrew N Sloss, Dominic Symes, Chris Wright, "ARM systems Developer's Guide "Elsevier Publication, 2004
24.	ARM System-on-Chip Architecture, Second Edition, by Steve Furber, PEARSON, 2013

REFERENCES BOOKS:

27.	ARM Assembly Language – William Hohl, CRC Press, ISBN:978-81-89643-04-1

On-Line Materials & Resources (NPTEL courses / Video lectures / You-tube Videos / Power points / On-line notes / web-links:

47.	www.arm.com
48.	Infocenter.arm.com
49.	https://youtube/iqQy45e14_M

Scheme of Evaluation of the CIE & Assessment Pattern:

Assignment: Only one assignment (open book test normally) will be of 10 marks & conducted in the class during the course of the semester (normally midway through' the semester or in between 2nd & 3rd test). Generally, 2- 4 questions can be given which has to be solved in 1 hour duration, the assignment question has to be from the self-study component or it can be a coding demo done in the laptop & shown on the spot to the teacher in the class, the questions has to be set according to easy, medium, tough & severe and evaluation has to be done as per the assignment evaluation rubrics.

Quiz: There will be 1 quiz of 10 questions of 1 mark each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).
CIE: There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totalled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)			
Remember	10	05	
Understand	10	05	
Apply	10		
Analyze			
Evaluate			
Create			

SEE – Semester End Examination Theory (50 Marks)

Bloom's Category	Theory Marks (50)
Remember	10
Understand	10
Apply	15
Analyze	15
Evaluate	
Create	

REAL TIME OPERATING SYSTEMS

Course Code : 18EC5DEBOS
L : P : T : S : 3 : 0 : 1 : 0
Exam Hours : 03
Total Hours : 40

Credits : 03
CIE Marks : 50
SEE Marks : 50
CIE + SEE Marks : 100

COURSE OBJECTIVES:

40.	To understand the difference between GPOS and RTOS.
41.	To Aquire the knowledge of Scheduling and Scheduling Policies.
42.	To familiarize with the Task Communication and Task Synchronization Techniques.
43.	To Analyse the resource requirements.
44.	To differenciate between the different feasibility tests.
45.	To be able to draw cycle diagrams for RM and DM policies.

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Describe theoretical and practical concepts, and functioning of operating system.
CO2	Distinguish a real-time operating system and its applications system from other systems.
CO3	Discriminate between Task , Process ,Threads ,Multitasking and Multiprocessing.
CO4	Be able to draw the sequence diagrams and calculate timings for non preemptive and preemptive scheduling policies.
CO5	Analyse the feasibility and utility in case of RM policy.
CO6	Illustrate RM and DM policies for multiple tasks.

Mapping of Course outcomes to Program outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	1	-	1	-	-	-	-	-	-	-	2
CO2	3	1	-	1	1	1	-	1	1	1	-	2
CO3	3	1	-	1	-	-	-	1	1	1	-	2
CO4	3	3	-	-	-	--	-	-	-	-	-	2
CO5	3	2	-	-	-	-	-	-	-	-	-	2
CO6	3	3	-	-	-	--	-	1	-	-	-	2

Module	**Course Content**	**Hours**	**COs**
1	Operating systems basics, Types of Operating systems, Tasks, Process and threads, Thread Preemption, Thread v/s Process, Multi processing and Multitasking, Types of Multi-tasking	8	
2	Task Scheduling, Non Preemptive Scheduling Preemptive Scheduling, Threads, Processes and Scheduling: Putting them all together Task Communication, Shared Memory, Message Passing, Remote Procedure Call(RPC) and Sockets,	8	
3	Task Synchronization, Task Communication/Synchronization Issues, Task Synchronization Techniques. Device Drivers, How to choose an RTOS System.	8	
4	Resources: Resource Analysis, Real-Time Service Utility, Scheduling: Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Pre-emptive and Fixed Priority Scheduling Policies,Thread Safe Re-entrant Functions.	8	

5	Processing: Introduction, Preemptive Fixed-Priority Policy, The formal differences between sufficient, necessary and necessary and sufficient, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies, EDF and LLF(in brief)	8	

PRE-REQUISITES :

Knowledge of subjects like : Basic Computer Architechture, C language

NOTE :

17. Questions for CIE and SEE not to be set from self-study component.
18. Assignment Questions may or may not be from self-study component only.

SELF-STUDY COMPONENTS :

Module 1 :	Program examples in Module 1
Module 2 :	Program examples in Module 1
Module 3 :	2.7, Real-Time Operating Systems from text book 2.
Module 4 :	Practice thread creation,deletion,semaphores,message passing in Linux
Module 5 :	Study of Overload scenario in RM,DM

TEXT BOOKS :

2	**Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009**
2	."Real-Time Embedded Systems and Components", Sam Siewert, Cengage Learning India Edition, 2007.

REFERENCES BOOKS:

28.	.D.M.Dhamdhere: System Programming and Operating Systems, 2nd Edition, Tata McGraw - Hill, 1999.
29.	**Raj Kamal,"Embedded Systems ,Architechture,Programming and Design",Second Edition**

On-Line Materials & Resources (NPTEL courses / Video lectures / You-tube Videos / Power points / On-line notes / web-links :

50.	**Real Time Operating System ,NPTEL**
51.	**Mastering RTOS ,UDEMY**
52.	**Real Time Operating System ,SWAYAM**
53.	**Development of Real Time Systems,Coursera**
54.	**Embedded System DesignPPT by Institute of Aernautical Engg,Dindigul**
55.	**RTOS Concepts PPT,by Pantech Prolabs**
56.	**What is RTOS,Video**
57.	**RTOS Tutorial**
58.	**Free rtos.org**

Scheme of Evaluation of the CIE & Assessment Pattern :

Assignment : Only one assignment (open book test normally) will be of 10 marks & conducted in the class during the course of the semester (normally midway thro' the semester or in between 2nd & 3rd test). Generally, 2- 4 questions can be given which has to be solved in 1 hour duration, the assignment question has to be from the self-study component or it can be a coding demo done in the laptop & shown on the spot to the teacher in the class, the questions has to be set according to easy, medium, tough & severe and evaluation has to be done as per the assignment evaluation rubrics.

Quiz : There will be 1 quiz of 10 questions of 1 marks each, which may be conducted along with the 2nd CIE test or at the appropriate time during the course of the semester and written in the answer booklet at the end (may be conducted on-line also).

CIE : There will be 3 CIE tests in a semester conducted for 50 marks with 10 Marks MCQs, remaining 40 Marks descriptive (with theory & problems). Finally, each CIE will be reduced to 10 Marks and totaled up for 30 Marks. There will be choices in the descriptive questions and evaluation has to be done as per the scheme of evaluation rubrics given. There has to be choices in the descriptive questions & the questions has to be set module/unit-wise. Total CIE marks for 50 will be finally rounded off to the nearest integer if the sum turns out to be a fraction.

CIE – Continuous Internal Evaluation Theory (50 Marks)

Bloom's Category	**Tests - 3 CIEs 30 Marks**	**Assignment-1 No. 10 Marks**	**Quiz-1 No. 10 Marks**
Marks (Out of 50)	**30**	**10**	**10**
Remember	10		5
Understand	10		2
Apply	10	5	2
Analyze	5	5	1
Evaluate	3		
Create	2		

SEE – Semester End Examination Theory (50 Marks)

Bloom's Category	**Marks Theory (50)**
Remember	10
Understand	10
Apply	10
Analyze	10
Evaluate	5
Create	5

DSP LAB

Course Code: 18EC5DLDSP
L : P : T : S : 0 : 2 : 1 : 0
Exam Hours : 03
Total Hours : 26

Credits : 02
CIE Marks : 50
SEE Marks : 50
CIE + SEE Marks : 100

COURSE OBJECTIVES:

46.	Simulate and verify the results of various signal processing concepts by using build in MATLAB functions.
47.	Practice to implement the required signal processing concepts by means of user defined MATLAB function.
48.	Compare the performance characteristics of IIR and FIR filter through MATLAB simulation.
49.	Familiarize with Simulink environment by constructing models for simple LTI systems.
50.	Realize the concepts of convolution, DFT and system responses using Digital Signal Processors (hardware interface).
51.	Verify digital filtering operation in real time

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1	Simulate, verify and analyze the spectra of Sampled signal and DFT.
CO2	Analyze through simulation the response of an LTI system by using various approaches - Convolution and difference equation.
CO3	Design, simulate IIR & FIR filters and analyze the magnitude and phase spectra.
CO4	Explore Auto correlation and Cross-correlation concepts and their properties through MATLAB simulation.
CO5	Construct the Simulink models for discrete time systems and verify the response.
CO6	Implement DT LTI systems on Digital Signal Processor and verify the response.

Mapping of Course outcomes to Program outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	-	1	3	-	-	-	1	-	-	1
CO2	3	3	1	1	3	-	-	-	1	-	-	1
CO3	3	3	3	1	3	-	-	-	1	-	-	1
CO4	3	3	-	1	3	-	-	-	1	-	-	1
CO5	3	3	2	1	3	-	-	-	1	-	-	1
CO6	3	3	3	1	3	-	-	-	1	-	-	1

Module	Expt No.	Content of the Lab Module	Hours	COs
		Introduction to MATLAB: different operators & functions. Introduction to SIMULINK: different block sets & tools		
Software: Programs				
PART-A	1.	Verification of Sampling theorem.	**18**	CO 1
	2.	Impulse response of a given system by solving a given difference equation.		CO 2
	3.	Linear & circular convolution of two given sequences.		CO 2
	4.	Autocorrelation and Cross-correlation of a given sequence with its property's verification.		CO 4
	5.	Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.		CO 1
	6.	Linear and Circular convolution of two sequences using DFT and IDFT.		CO 2
	7.	Design and implementation of FIR filter to meet given specifications.		CO 3
	8.	Design and implementation of IIR filter to meet given specifications.		CO 3
	9.	Determination of system response : with step, impulse, sinusoidal ramp inputs various		CO2
	10.	Construct a Simulink model for a system represented by second order difference equation and verify the system response		CO2, 5
	11.	Construct a Simulink model of a FIR LPF for given specifications and observe the time domain waveform and spectrum of filtered signal.		CO 3, 5
Hardware : Interfacing experiments				
PART-B	12.	Linear & circular convolution of two given sequences.	**8**	CO 2, 6
	13.	Computation of N- Point DFT of a given sequence		CO 1, 6
	14.	Impulse response of first order and second order system		CO 2, 6
	15.	Realization of an FIR filter (any type) to meet given specifications. The input can be a signal from function generator / speech signal.		CO 3, 6

PRE-REQUISITES:

1. Fundamentals of Signals and Systems.
2. Theoretical knowledge of Digital Signal Processing.
3. Basic programming knowledge.

Scheme of Evaluation of the CIE & Assessment Pattern:

CIE – Continuous Internal Evaluation (**50** Marks)	
Record writing	**10** Marks
Conduction	**10** Marks
Viva-voce	**05** Marks

SEE – Semester End Examination (50 Marks)

Bloom's Category	**Performance (Day To Day)**	**Internal Test**
Marks (Out of 50)	**25**	**25**
Remember		
Understand		
Apply	05	05
Analyze	10	10
Evaluate	05	05
Create	05	05

H D L LAB

Course Code : 18EC5DLHDL
L : T : P : S : 0 : 1 : 2 : 0
Exam Hours : 03
Total Hours : 26

Credits : 02
CIE Marks : 50
SEE Marks : 50
CIE + SEE : 100

COURSE OBJECTIVES:

1. To describe the functionality of combinational and sequential circuits using HDL.
2. Learn how to simulate, analyze the designed program.
3. To know how to debug the written code.
4. To justify the design on FPGA kit through implementation.
5. To illustrate interfacing concepts using FPGA kit.
6. To give an in-depth exposure to the various tools in Xilinx ISE.

COURSE OUTCOMES:

At the end of the course, student will be able to

CO1	Gain the knowledge of using XILINX ISE tool.
CO2	Design the HDL code for digital circuits and simulate using XILINX ISE tool
CO3	Analyze and debug VHDL and Verilog code for digital circuits using XILINX tool and ModelSim simulator
CO4	Synthesize digital circuit with FPGA kit.
CO5	Design VHDL program and synthesise hardware interfacing experiments
CO6	Develop digital system for small real time problems and Implement on FPGA kit.

Mapping of Course Outcomes to Program Outcomes:

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	2	2	3	-	-	-	-	-	-	2
CO2	3	3	3	3	3	-	-	-	-	-	-	2
CO3	3	3	2	2	3	-	-	-	-	-	-	2
CO4	3	3	3	3	3	-	-	-	-	-	-	2
CO5	3	3	3	3	3	-	-	-	-	-	-	2
CO6	3	3	3	3	3	-	-	-	-	-	-	2

Module	Expt No.	Content of the Lab Module with Expt. Nos.	Hours	COs
Software : Programming Using Verilog				
Part A	NOTE: 1.Design using Verilog ♦ RTL Development 2.Verification using Verilog ♦ Testbench through testcsases 3.Simulation and Debug			
	1	Write HDL code to realize all the logic gates	03	CO 1-4
	2	Write a HDL program for the following combinational designs a. 2 to 4 decoder b. 8 to 3 (encoder without priority & with priority) c. 8 to 1 multiplexer d. 4 bit binary to gray converter e. Multiplexer, de-multiplexer, comparator	06	CO 1-4
	3	Write a HDL code to describe the functions of a Full Adder using three modelling styles.	03	CO 1-4
	4	Develop the HDL code for the following flip-flops, a. SR Flip-Flop b. D Flip-Flop c. JK Flip-Flop d. T Flip-Flop	03	CO 1-4
	5	Write a model for 8bit ALU. ALU should use combinational logic to calculate an output based on the 3bit op-code input. ALU should decode the 3 bit op-code according to the given in example below. Opcode (2:0) OPCODE ALU OPERATION i). A + B ii). A – B iii). A Complement iv). A * B v). A AND B vi). A OR B vii). A NAND B viii). A XOR B	03	CO 1-4
	6	Design 4 bit Binary and BCD counters (Synchronous reset and Asynchronous reset) and "any sequence" counters	06	CO 1-4
Hardware : INTERFACING (using VHDL)				
Part B	7	Write HDL code to control speed, direction of DC and Stepper motor.	03	CO 1-6
	8	Write HDL code to generate different waveforms (Square, Triangle, Ramp etc.,) using DAC.	03	CO 1-6
	9	Write HDL code to control external lights using relays.	03	CO 1-6

EMERGING TECHNOLOGIES
5G TECHNOLOGY

Course Code : 18EC5DCEMT
L : P : T : S : 2 : 0 : 0 : 0
Exam Hours : 00
Total Hours : 25

Credits : 02
CIE Marks : 50
SEE Marks : 00
CIE + SEE : 00

COURSE OBJECTIVES:

1. Acquire knowledge about different generations of mobile communication
2. Understanding LTE features which led to 5G
3. Familiarising 5G key features and architecture
4. Application of 5G in enabling IOT
5. Understand software defined radio and cognitive radio.

COURSE OUTCOMES:

After the end of the course, the students will be able to

CO1	To know about different generations of mobile communications
CO2	Analyze the difference between 4G and 5G services
CO3	Interpret the working principle of , SDR , Cognitive concepts
CO4	Acquire knowledge about 5G Technology features
CO5	Understand the Application of 5G in enabling IOT
CO6	Preparing report on emerging wireless technologies

Mapping of Course Outcomes to Program Outcomes :

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	3	2	-	-	-	-	-	-	-	-	-	-
CO3	3	2	-	-	-	-	-	-	-	-	-	-
CO4	3	2	-	-	-	-	-	-	-	-	-	-
CO5	3	2	-	-	-	-	-	-	-	-	-	-
CO6	3	2	-	-	-	-	-	-	-	-	-	-

Module	Contents of the Module	Hours	CO
1	Communication Technology from 1G to 5G-Overview. LTE features and its impact on services. 5G Technology Key Features. 5G architecture. Enabling Massive IOT.	12	 CO1 CO2 CO3
2	Massive MIMO. Coherent Optical Transmission Systems (GHz speed). Software Defined Radio & its evolution. Cognitive Radio & its evolution. Quality of service and management in 5G. Overview of next generation communications & its applications.	13	 CO4 CO5 CO6

REFERENCE BOOKS:

1. Kalyan Sundar, Lawrence C. Miller, "5G for dummies", Ixia Special Edition, *John Wiley and Sons inc.*, 2017.
2. Akhil Gupta, Rakesh Kumar Jha, "A Survey of 5G Networks : Architecture and emerging technology", *IEEE Access*, Jul. 22, 2015.
3. Alexander M. Wyglinski, "Cognitive Radio Communications and Networks", 2010, *Elsevier Publications*.

WEB RESOURCES:

1. https://5g-ppp.ru/
2. http://www.massivemimo.eu/
3. http://www.3gpp.org

ASSESSMENT PATTERN:

Project : Only one mini project report to be submitted & at the end of the course & the write-up will be evaluated, the work has to be done in the 5th semester only, it can be in groups also.

CIE, Assignment & Quiz : There will be no quiz, no assignment as well as no CIE tests, but instead of these 3 items, there will be a write-up submission with an evaluation at the end.

Evaluation Pattern : The rubrics is 30 Marks for Report/Developed model & 20 Marks is for the presentation or evaluation.

CIE – Continuous Internal Evaluation Theory (50 Marks) :

Bloom's Category	Tests – 3 CIEs (Nil)	Assignments – Nil	Quizzes – Nil	Report / Model Building	Presentation / Evaluation
Marks (Out of 50)	**-**	**-**	**-**	**30**	**20**
Remember	-	-	-	-	-
Understand	-	-	-	-	-
Apply	-	-	-	-	-
Analyze	-	-	-	-	-
Evaluate	-	-	-	-	-
Create	-	-	-	-	-

SEE –Semester End Examination Theory (50 Marks) :

Bloom's Category	Theory Marks (50)
Remember	5
Understand	5
Apply	10
Analyze	10
Evaluate	10
Create	10