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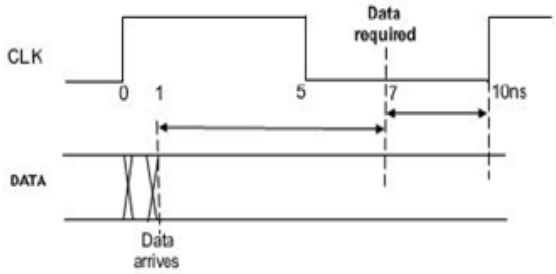
(Accredited by National Assessment & Accreditation Council (NAAC) with 'A' grade)

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – II

Course Name : Digital System Design Using Verilog	Date :	10.11.2020
Course Code : 18EC5DCDSV	Day :	Tuesday
Semester : V	Timings :	1 to 2.30 P.M
Max Marks : 50 M	Duration :	1½ Hrs.

No.		Question Description	Mks	CO & Levels
Q1	(a)	A _____ is a set of procedures that allows designers to progress from a specification for an ASIC/FPGA based system to final ship i) design space ii) design flow iii) RTL iv) None of these	1	
	(b)	What do you mean by synthesizable Verilog? i. A software tool that can synthesize a given Verilog description. ii. A subset of the language Verilog that can be synthesized by the synthesis tool. iii. A subset of the language Verilog that is more efficient for synthesis than the rest. iv. None of these.	1	
	(c)	Calculate the slack for the following figure, if t_{setup} of capture flop = 3ns:  i) 6 ns ii) 7ns iii) 8ns iv) 9ns	1	
	(d)	Which of the following statements are true? i) The $display command prints the values of the text / variables as soon as it is executed. ii) The $display command prints the values of the text / variables when one or more of the specified variables changes value. iii) The $monitor command prints the values of the text / variables as soon as it is executed. iv) All of these	1	
	(e)	The difference between the clock arrivals of capturing register and launching register is called: i) uncertainty ii) skew iii) latency iv) none	1	

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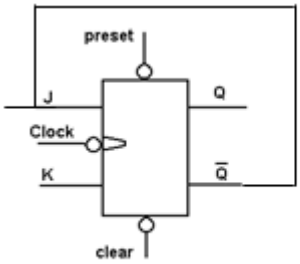
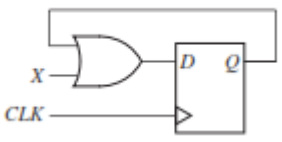
	(f)	The number of Flip flops required to represent Synchronous counter to count up to 22 are : i) 2 ii) 4 iii) 5 iv) 6	1	
	(g)	In a JK flip flop, we have J = Q' and K = 1. Assume the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be  i) 010000 ii) 011001 iii) 010010 iv) 010101	1	
	(h)	Which of the following is a difference between a Function and a Task? i) A Function cannot call a task; a Task can call another task. ii) A Function can call another function; a Task cannot. iii) A Function has one or more inputs; a Task has no inputs. iv) A Function argument may be an output; a Task's argument may only be an input.	1	
	(i)	Which of the following is/are not true for "generate" blocks? i) Multiple copies of code blocks are generated dynamically before simulation synthesis. ii) Can be used to instantiate multiple copies of some module. iii) Must be used along with a variable of type "genvar". iv) None of these.	1	
	(j)	When does the $monitor statement in a Verilog test bench print the specified values? i) At the start of the simulation. ii) When the $monitor statement is first encountered. iii) Whenever the value of any of the specified variables change. iv) None of the above.	1	
Q2	a)	A D flip-flop has a setup time of 5 ns, a hold time of 3 ns, and a propagation delay from the rising edge of the clock to the change in flip-flop output in the range of 6 to 12 ns. An OR gate delay is in the range of 1 to 4 ns.  a) What is the minimum clock period for proper operation of the following circuit? b) What is the earliest time after the rising clock edge at which *X* is allowed to change?	4	L3,CO2

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		c) What is the latest time before the rising clock edge that input *X* can safely change?		
	b)	Develop a Verilog model for a pipelined circuit that computes the average of corresponding values in streams of input values, a, b, c and d. The pipeline consists of three stages: the first stage sums values of a,b and c and saves the value of d; the second stage adds on the saved value of d; and the third stage divides by four. The inputs and output are all signed fixed-point numbers indexed from 5 down to -8.	6	L3,CO3
Q3	a)	Design a circuit that counts 16 clock cycles and produces a control signal, "ctrl", that is '1', during every fifth and Tenth cycle. Also, develop a Verilog model for the same.	7	L3,CO3
	b)	A digital alarm clock needs to generate a periodic signal at a frequency of approximately 1024Hz to drive the speaker for the alarm tone. Use a counter to divide the system's master clock signal with a frequency of 2 MHz to derive the alarm	3	L3,CO3
Q4	(a)	Define $display, $write, $strobe, $setup	4	L2,CO3
	(b)	Illustrates a function using 'for loop'. Write a Verilog function for generating an even parity bit for a 4-bit number.	6	L2,CO2
		OR		
5	a)	Design an n bit shift register using D flip-flop and Multiplexers	4	L2,CO2
	b)	Design a 4 bit subtractor using generate statement.	3	L2,CO2
	c)	List the Compiler Directives in Verilog	3	L2,CO2
6		Compare ASIC and FPGA in detail with design flow diagram	10	L2,CO2
		OR		
7	a)	Discuss guidelines for clocks and resets	5	L3,CO2
	b)	List the built in primitives. Explain any two with example	5	L2,CO3