DIGITAL SYSTEM DESIGN USING VERILOG

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(3 CREDITS)

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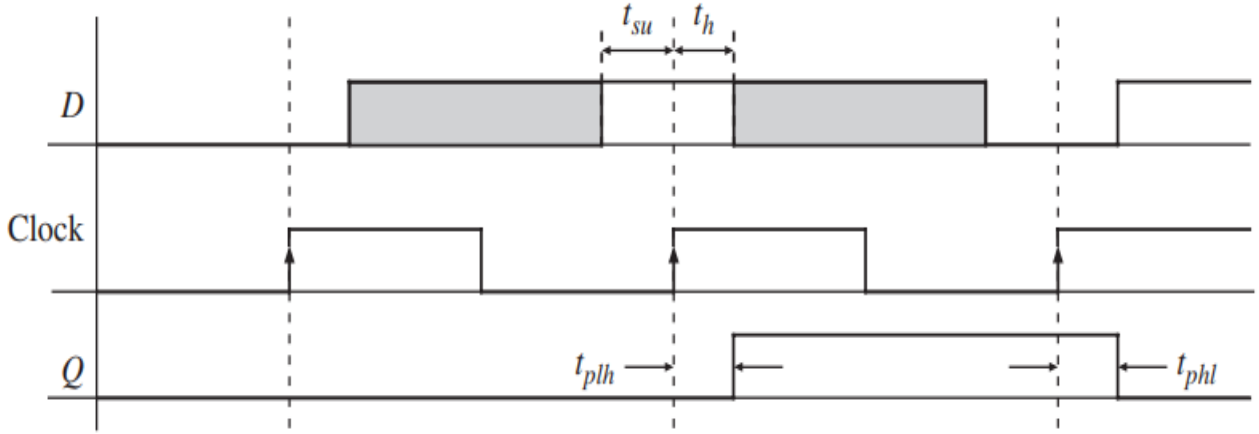
Sequential Circuit Timing

The correct functioning of sequential circuits involves several timing issues. These are

- Propagation delays of flip-flops, gates and wires;
- setup times and hold times of flip-flops;
- clock synchronization; clock skew, etc., become important issues in designing sequential circuits.

Propagation Delays, Setup, and Hold Times:

There is a certain amount of time, that elapses from the time the clock changes to the time the Q output changes. This time is called propagation delay or clock-to-Q delay of the flip-flop is indicated in Figure.



- The propagation delay can depend on whether the output is changing from high to low or vice versa. In the figure, the propagation delay for a low-to-high change in Q is denoted by t_{plh}, and for a high-to-low change it is denoted by t_{phl}.
- For an ideal D flip-flop, if the D input changed at exactly the same time as the active edge of the clock, the flip-flop would operate correctly.
- However, for a real flip-flop, the D input must be stable for a certain amount of time before the active edge of the clock. This interval is called the setup time (t_{su}).
- Furthermore, D must be stable for a certain amount of time after the active edge of the clock. This interval is called the hold time (t_h).
- The above figure illustrates setup and hold times for a D flip-flop that changes state on the rising edge of the clock. D can change at any time during the shaded region on the diagram, but it must be stable during the time interval t_{su} before the active edge and for t_h after the active edge.
- Flip-flops typically have a setup time about 3–10x of the propagation delay of an inverter (NOT) gate. The hold times are typically 1–2x of the delay of an inverter.

Timing Conditions for Proper Operation:

- In a synchronous sequential circuit, state changes occur immediately following the active edge of the clock. The maximum clock frequency for a sequential circuit depends on several factors. The clock period must be long enough so that all flip-flop and register inputs will have time to stabilize before the next active edge of the clock.
- Static timing analysis (STA) is a method of validating the timing performance of a design by checking all possible paths for timing violations under worst-case conditions.
- A static analysis path starts at a source flip-flop (or at a primary input) and terminates at a destination flip-flop (or primary output).
- A static timing path between two flip-flops starts at the input to the source flip-flop and terminates at the input of the destination flip-flop.

- The timing paths in a synchronous digital system can be classified into 4 types:

I. Register to register paths (i.e., flip-flop to flip-flop)

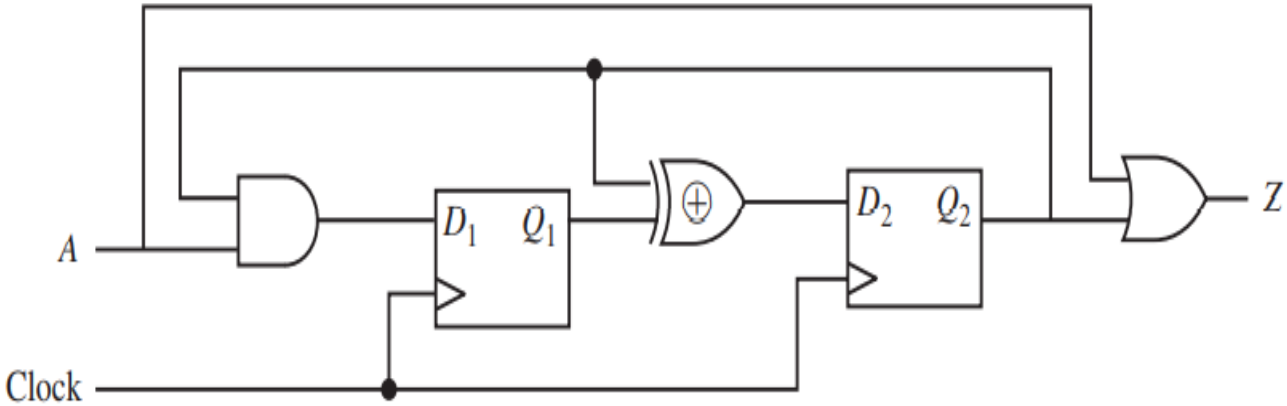
II. Primary input to register paths (i.e., input to flip-flop)

III. Register to primary output paths (i.e., flip-flop to output)

IV. Input to output paths (i.e., no flip-flop)

- Static timing analysis checks how the data arrives with respect to clock. It detects setup and hold-time violations in the design so that they can be corrected.
- A setup time violation occurs if the data changes just before the clock without providing enough setup time for the flip-flop.
- A hold-time violation occurs if the data changes just after the clock without providing enough hold time for the flip-flop.
- Slack is the amount of time still left before a signal will violate a setup or hold-time constraint. Paths must have a positive or zero slack in order to have no violations.

Example: Identify the static timing paths in the following circuit



There are six static timing paths in this circuit:

I. From A to D1 (primary input to flip-flop)
II. From D1 to D2 including the XOR (flip-flop to flip-flop)
III. From D2 via XOR to D2 (flip-flop to flip-flop)
IV. From D2 to D1 via AND (flip-flop to flip-flop)
V. From D2 to Z via the OR gate (flip-flop to output)
VI. From A to Z via the OR gate (input to output)

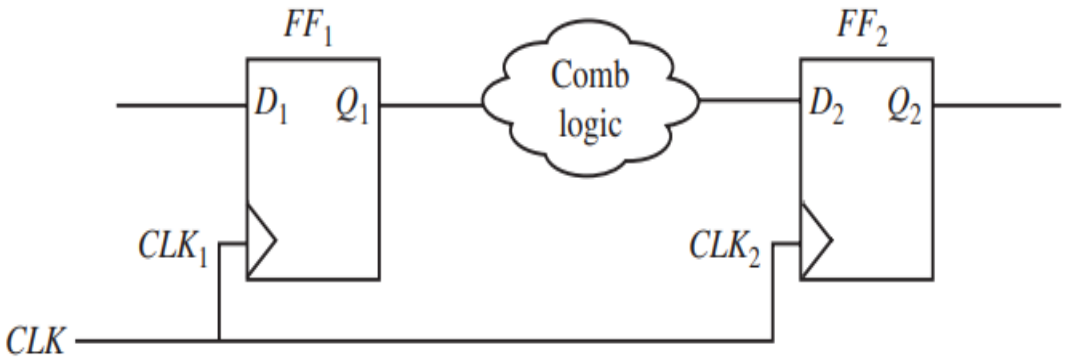
The most complicated paths are the flip-flop to flip-flop paths; the other paths can be treated as special cases of this type of path.

- Timing Rules for Flip-Flop to Flip-Flop Paths

For a circuit of the general form of Figure shown, assume that the

tcmax is the maximum propagation delay through the combinational circuit

tpmax is the maximum propagation delay from the time the clock changes to the time the flip-flop output change, where tpmax is the maximum of tplh and tphl.



(a) Circiut

Also assume that the

t_{cmin} minimum propagation delay through the combinational circuit

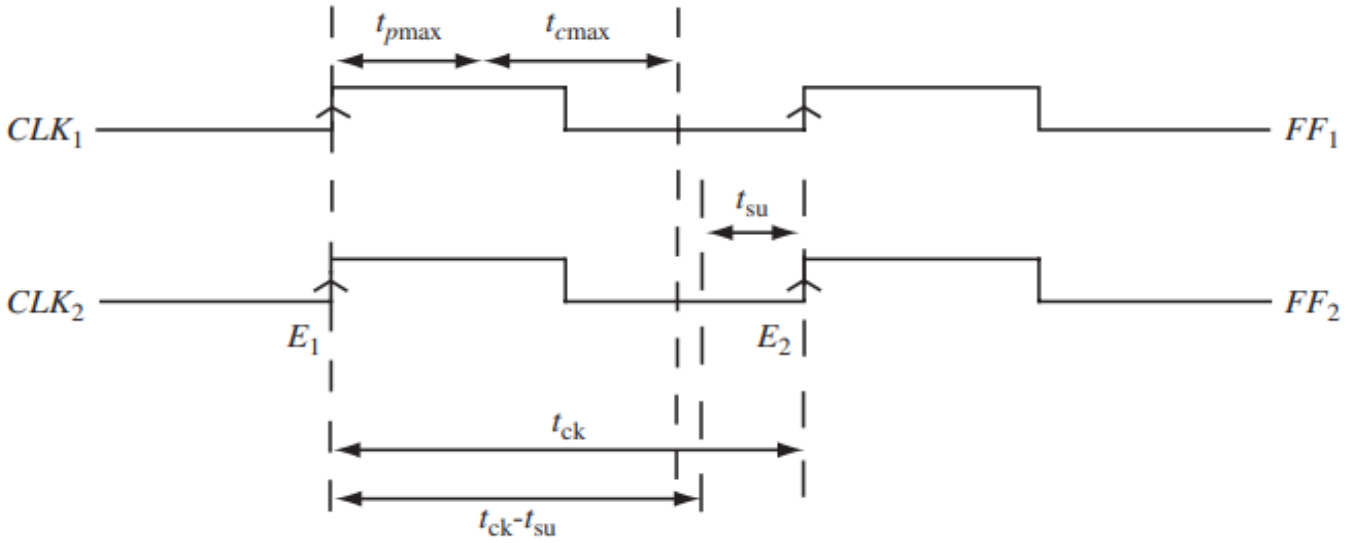
t_{pmin} the minimum propagation delay from the time the clock changes to the time the flip-flop output changes.

where t_{pmax} data is launched from flip-flop D1 to FF1 ’s Q1 at the positive edge of clock at FF1 (i.e., CK1).

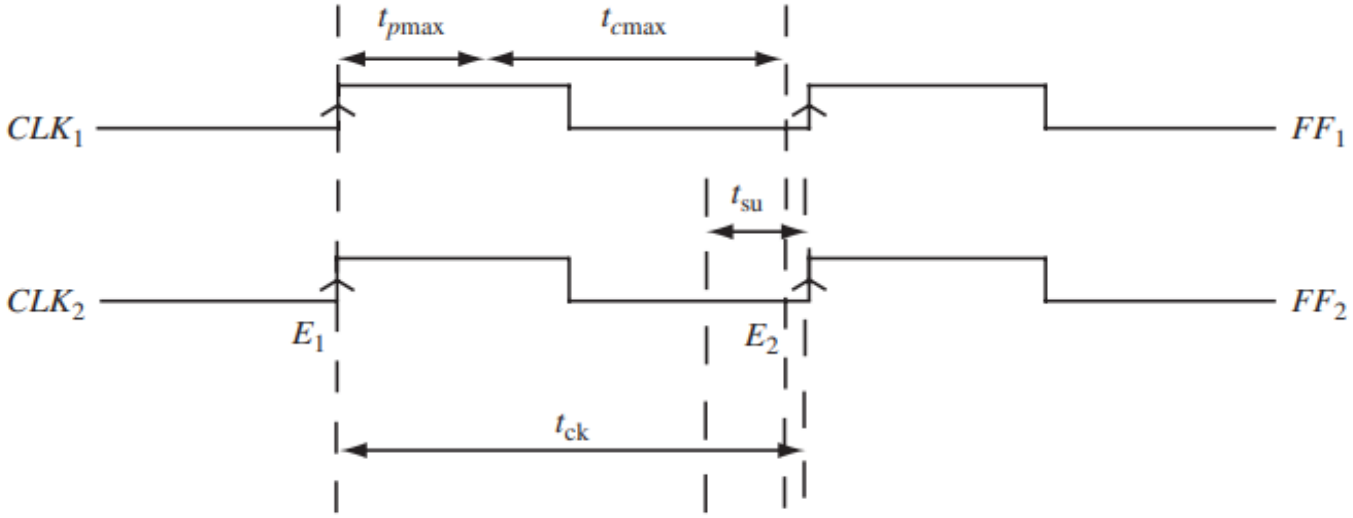
Data is captured at FF2 ’s D (i.e., D2) at the positive clock edge at FF2 (i.e., CLK2).

FF1 is called the launching flip-flop, and FF2 is called the capturing flip-flop.

(a) Circiut



(b) Timing diagram when setup time is met



(c) Timing diagram when setup time is violated

There are two rules this circuit has to meet in order to ensure proper operation.

Rule No. 1: Setup time rule for flip-flop to flip-flop path: Clock period should be long enough to satisfy flip-flop setup time.

For proper synchronous operation, the data launched by FF1 at edge E1 of clock CK1 should be captured by FF2 at edge E2 of clock CK2 . The clock period should be long enough to allow the first flip-flop's outputs to change and the combinational circuitry to change while still leaving enough time to satisfy the setup time.

Once the clock CK1 arrives, it could take a delay of up to t_{pmax} before FF1 's output changes. Then it could take a delay of up to t_{cmax} before the output of the combinational circuitry changes. Thus the maximum time from the active edge E1 of the clock CK1 to the time the change in Q1 propagates to the second flip-flop's input (i.e., D2) is $t_{pmax} + t_{cmax}$.

- In order to ensure proper flip-flop operation, the combinational circuit output must be stable at least tsu before the end of the clock E2 reaches FF2 . If the clock period is tck,

$$tck \geq tpmax + tcmax + tsu$$

- The above equation relates the clock frequency of operation of the circuit with setup time of the flip-flops. Therefore, setup time violations can be solved by changing the clock frequency. The difference between t_{ck} *and* $(t_{pmax} + t_{cmax} + tsu)$ *is* referred to as the **setup time margin. The setup margin has to be zero or positive in** order to have a circuit pass timing checks.

$$t_{ck} - t_{pmax} - t_{cmax} - t_{su} \geq 0$$

Rule No. 2 Hold-time rule for flip-flop to flip-flop path: Minimum circuit delays should be long enough to satisfy flip-flop hold time.

According to Rule No. 1, in Figure at edge E2 , FF2 should capture the data launched by FF1 on the previous edge (i.e., edge E1).

For this to happen successfully, the old data should remain stable at edge E2 until FF2 's hold time elapses.

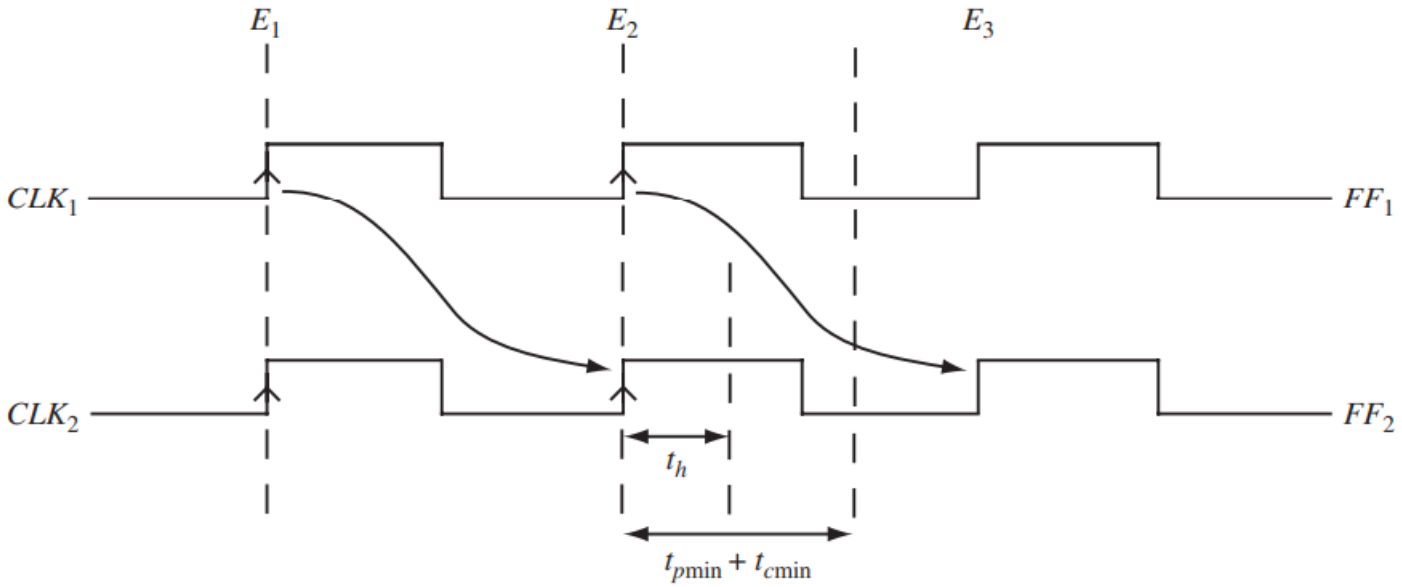
When FF2 is capturing this old data at edge E2 , FF1 has started to launch new data on edge E2 , which should be captured by FF2 only at edge E3 .

A hold-time violation could occur if the data launched by FF1 at E2 is fed through the combinational circuit and causes D2 to change too soon after the clock edge E2 .

The new data being launched by FF1 takes at least t_{pmin} time to pass through FF1 and at least t_{cmin} to pass through the combinational circuitry. Hence, the hold time is satisfied if

$$t_{pmin} + t_{cmin} \geq t_h$$

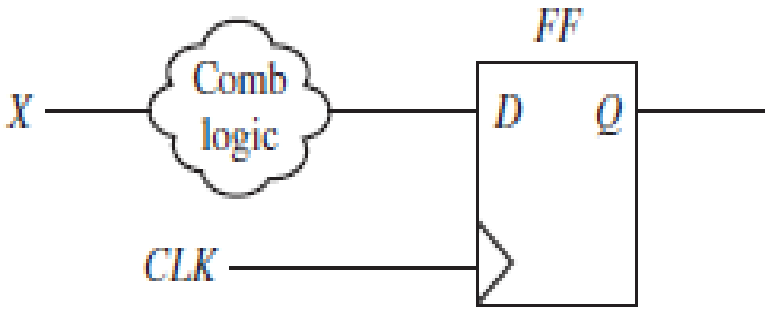
- Figure illustrates a situation where hold-time is satisfied.



The equation shown above, does not have the clock frequency in it. Therefore, if a circuit has a hold-time violation, it cannot be corrected by changing the clock frequency of the circuit. To correct a hold-time violation, the circuit must be redesigned.

Timing Rules for Input to Flip-Flop Paths:

- Consider a timing path from primary input to flip-flop as in Figure. The changes in primary input *X should happen such that the value propagates to the* flip-flop input satisfying both setup and hold-time constraints.

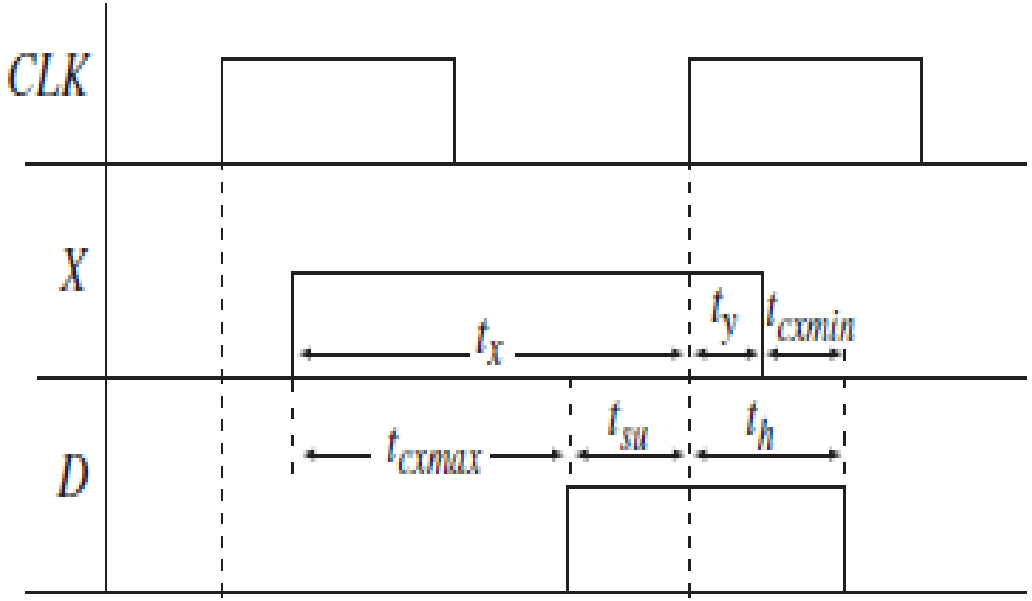


Rule No. 3 Setup time rule for input to flip-flop path: External input changes to the circuit should satisfy flip-flop setup time.

- A setup time violation could occur if the X input to the circuit changes too close to the active edge of the clock.
- If X changes at time t_x before the active edge of the clock, shown in Figure, then it could take up to the maximum propagation delay of the combinational circuit before the change in X propagates to the flip-flop input. There should still be a margin of tsu left before the edge of the clock. Hence, the setup time is satisfied if

$$t_x \geq t_{cx\max} + t_{su}$$

where t_{cxmax} *is the maximum propagation delay from X to the flip-flop input.*



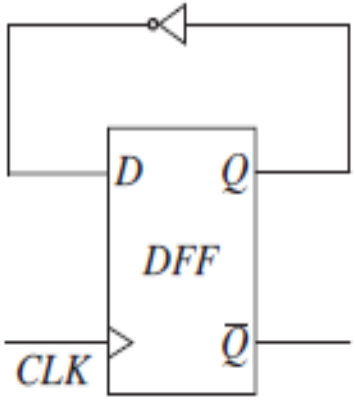
Rule No. 4 Hold-time rule for input to flip-flop path: External input changes to the circuit should satisfy flip-flop hold times.

- In order to satisfy the hold time, we must make sure that X does not change too soon after the clock. If a change in X propagates to the flip-flop input in zero time, X should not change for a duration of t_h after the clock edge.
- The hold time is satisfied if

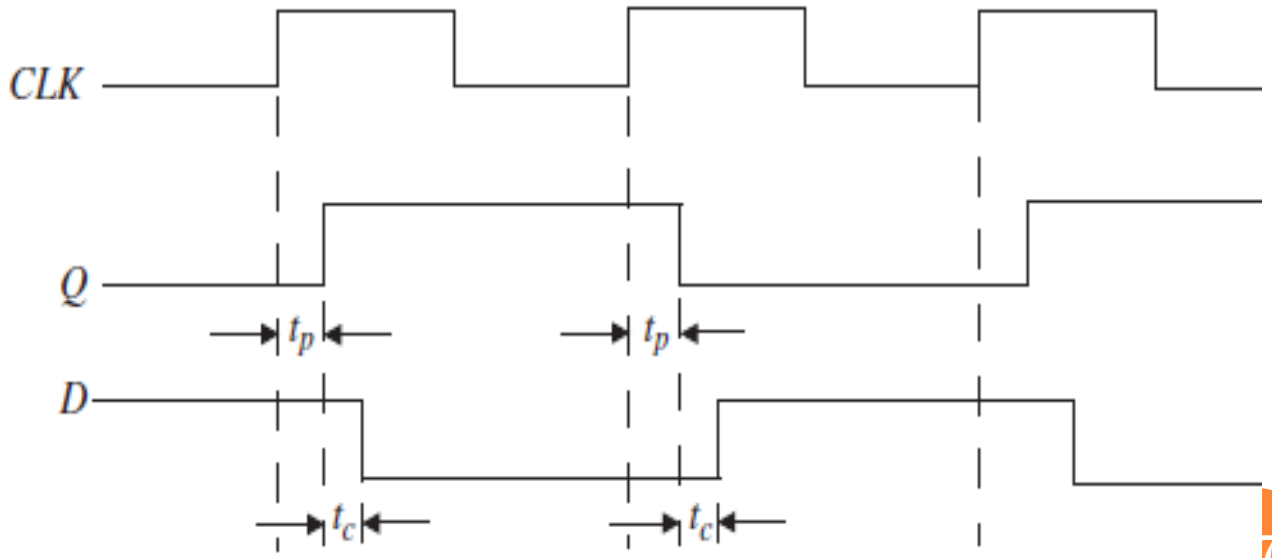
$$t_y \geq t_h - t_{cx\min}$$

- If t_y is negative, X can change before the active clock edge and still satisfy the hold time.

- Consider a simple circuit of the form of Figure (a). The output of a D flip-flop is fed back to its input through an inverter.
- Assume a clock as indicated by the waveform CLK in Figure (b). If the current output of the flip-flop is 1, a value of 0 will appear at the flip-flop's *D input after the propagation delay of the* inverter.
- Assuming that the next active edge of the clock arrives after the setup time has elapsed, the output of the flip-flop will change to 0. This process will continue yielding the output *Q of the flip-flop to be a waveform with twice the period*



(a) A frequency divider



(b) Frequency divider timing diagram

- If we increase the frequency of the clock slightly, the circuit will still work, yielding half of the increased frequency at the output.
- However, if we increase the frequency to be very high, the output of the inverter may not have enough time to stabilize and meet the setup time requirements.
- Similarly, if the inverter was very fast and fed the inverted output to the D input extremely quickly, timing problems will occur, because the hold time of the flip-flop may not be met.
- Timing Rules Nos. 1 and 2 can be applied to this circuit, and it can be seen that the maximum clock frequency of this circuit for proper operation. If the minimum clock period is denoted by t_{ckmin},

$$t_{ckmin} = t_{pmax} + t_{cmax} + t_{su}$$

- Hence maximum clock frequency f_{max} *is given by*

$$f_{max} \quad 1/(t_{pmax} + t_{cmax} + t_{su})$$

- If the minimum and maximum delays of the inverter are 1 ns and 3 ns, and if t_{pmin} and t_{pmax} *are 5 ns and 8 ns, the maximum frequency at which it can be clocked can be* derived using above equation. Assume that the setup and hold times of the flip-flop are 4 ns and 2 ns.
- For proper operation,

$$t_{ck} \geq t_{pmax} + t_{cmax} + t_{su}$$

$$t_{ck} \geq 8 + 3 + 4 = 15\,\text{ns}$$

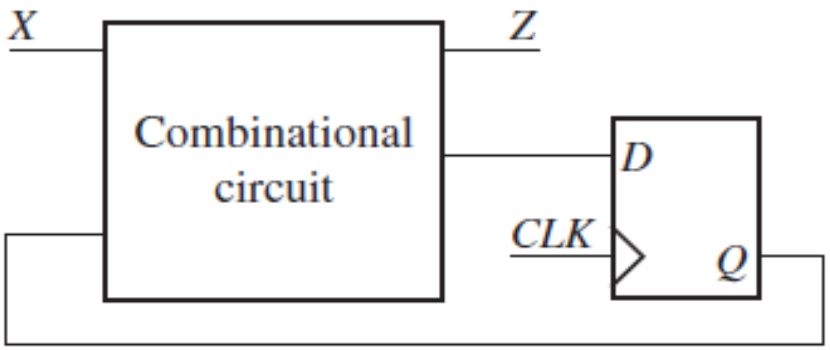
The maximum clock frequency is then $1/t_{ck} = 66.67\ MHz$.

- Hold-time requirement is satisfied. Hold-time requirement means that the *D input should not change before 2 ns after the clock edge.* This will be satisfied if

$$t_{pmin} + t_{cmin} \geq 2\,\text{ns}.$$

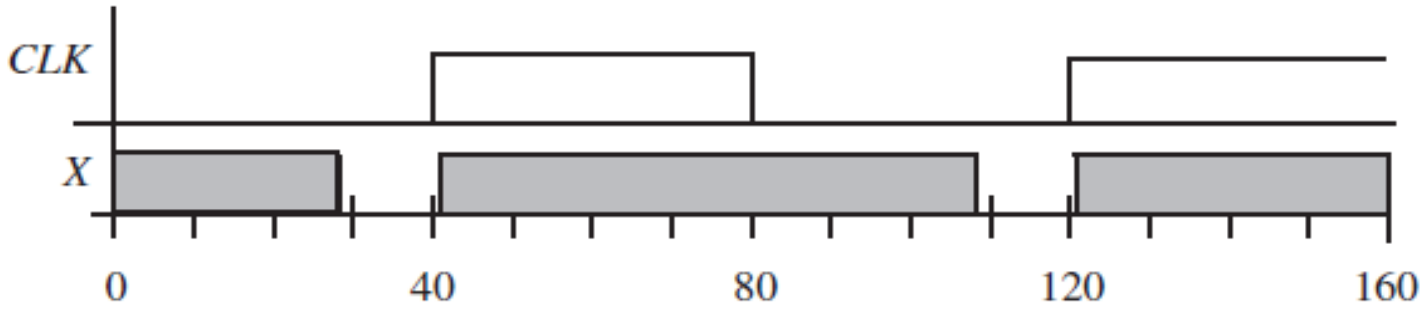
- Thus the *Q output* is guaranteed not to change until 5 ns after the clock edge and at least 1 ns more should elapse before the change can propagate through the inverter. Hence the *D* input will not change until 6 ns after the clock edge, which automatically satisfies the hold-time requirements.

Consider a circuit as shown in Figure



	Q^+		Z	
Q	0	1	0	1
0	0	1	0	1
1	0	0	1	0

(a) A sequential circuit



(b) Safe regions for changes in X

- Assume that the delay of the combinational circuit is in the range 2 to 4 ns, the flip-flop propagation delays are in the range 5 to 10 ns, the setup time is 8 ns, and hold time is 3 ns. In order to satisfy the setup time, the clock period has to be greater than $t_{pmax} + t_{cmax} + tsu$. So

$$t_{ck} = 10 + 4 + 8 = 22 \text{ ns}$$

- The hold-time requirement is satisfied if the output does not change until 3 ns after the clock. Here, the output is not expected to change until $t_{pmin} + t_{cmin}$. Since t_{pmin} is 5 ns and t_{cmin} is 2 ns, the output is not expected to change until 7 ns, which automatically satisfies the hold-time requirement.
- The X input should be stable for a duration of $t_{cxmax} + t_{su}$ (i.e., 4 ns + 8 ns) before the clock edge. Similarly, it should be stable for a duration of $t_h - t_{cxmin}$ (i.e., 3 ns - 2 ns) after the clock edge. Thus, the X input should not change 12 ns before the clock edge and 1 ns after the clock edge.
- Although the hold time is 3 ns, we see that the input X can change 1 ns after the clock edge, because it takes at least another 2 ns (minimum delay of combinational circuit) before the input change can propagate to the D input of the flip-flop.
- The shaded regions in the waveform for X indicate safe regions where the input signal X may change without causing erroneous operation in the circuit.

- Consider the circuit in Figure with the following minimum/maximum delays:

  CLK-to-Q for flip-flop A: 7 ns/9 ns

  CLK-to-Q for flip-flop B: 8 ns/10 ns

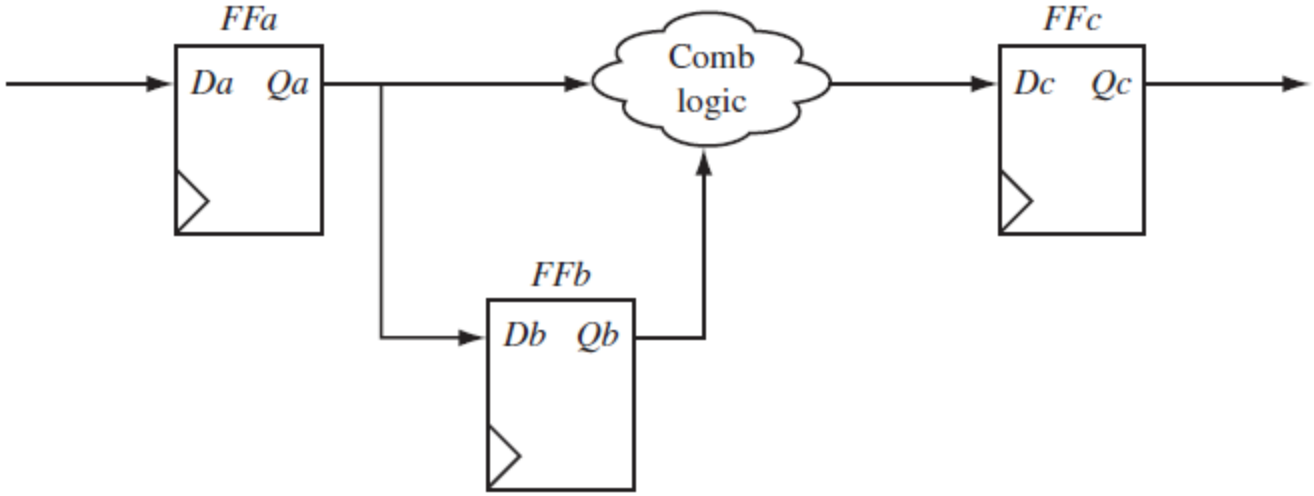
  CLK-to-Q for flip-flop C: 9 ns/11 ns

  Combinational logic: 3 ns/4 ns

  Setup time for flip-flops: 2 ns

  Hold time for flip-flops: 1 ns

  Compute the delays for all timing paths in this circuit and determine the maximum clock frequency allowed in this circuit.



Answer: Remember that a timing path starts at either a primary input or at the input of a flip-flop. A path terminates at the input of a flip-flop or at a primary output.

Delay for path from flip-flop A to B = $t_{clk\text{-}to\text{-}Q(A)} + t_{su}(B) = 9\,ns + 2\,ns = 11\,ns$

Delay for path from flip-flop A to C = $t_{clk\text{-}to\text{-}Q(A)} + t_{combo} + t_{su}(C) = 9\,ns + 4\,ns + 2\,ns = 15\,ns$

Delay for path from flip-flop B to C = $t_{clk\text{-}to\text{-}Q(B)} + t_{combo} + t_{su}(C) = 10\,ns + 4\,ns + 2\,ns = 16\,ns$

Delay for path from input to flip-flop A = $t_{su}(A) = 2\,ns = 2\,ns$

Delay for path from flip-flop C to output = $t_{clk\text{-}to\text{-}Q(C)} = 11\,ns$

Since the delay for path from B to C is the largest of the path delays, the maximum clock frequency is determined by this delay of 16 ns. The frequency is $1/t_{min} = 1/16\ ns = 62.5$ MHz.

- Consider the circuit in Figure with the following minimum/maximum delays:

  CLK-to-Q for flip-flop 1: 5 ns/8 ns

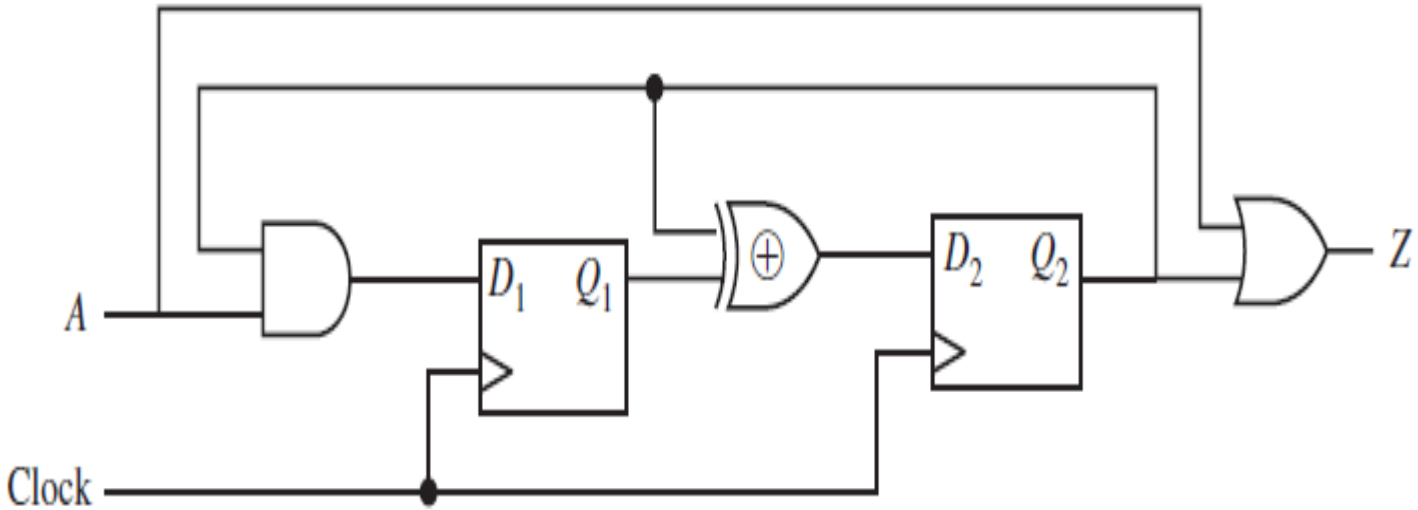
  CLK-to-Q for flip-flop 2: 7 ns/9 ns

  XOR Gate: 4 ns/6 ns

  AND Gate: 1 ns/3 ns

  Setup time for flip-flops: 5 ns

  Hold time for flip-flops: 2 ns



(a) **What is the minimum clock period that this circuit can be safely clocked at?**

Answer: Since XOR gate delay is higher than the AND gate delay, and the second flip-flop's delay is greater than that of the first flip-flop, the path from the second flip-flop to input of the second flip-flop via the XOR is the longest path. This path determines the maximum clock frequency. The maximum frequency is dictated by

$$f_{max} = 1/(t_{flip\text{-}flop\text{-}max} + t_{XORmax} + t_{su})$$

$$= 1/(9 + 6 + 5) = 1/20\,\text{ns} = 50\ \text{MHz}$$

(b)What is the earliest time after the rising clock edge that input *A can safely change?*

Answer: The earliest time after the rising clock edge that *A can safely change* can be obtained from equation $t_y \geq t_h - t_{cxmin}$

$$t_y = t_h - t_{ANDmin} = 2\,\text{ns} - 1\,\text{ns} = 1\,\text{ns}$$

- **(c) What is the latest time before the rising clock edge that input *A can safely change?***

Answer:

The latest time before the rising clock edge that *A can safely change* can be obtained from equation $t_x \geq t_{cx\max} + t_{su}$

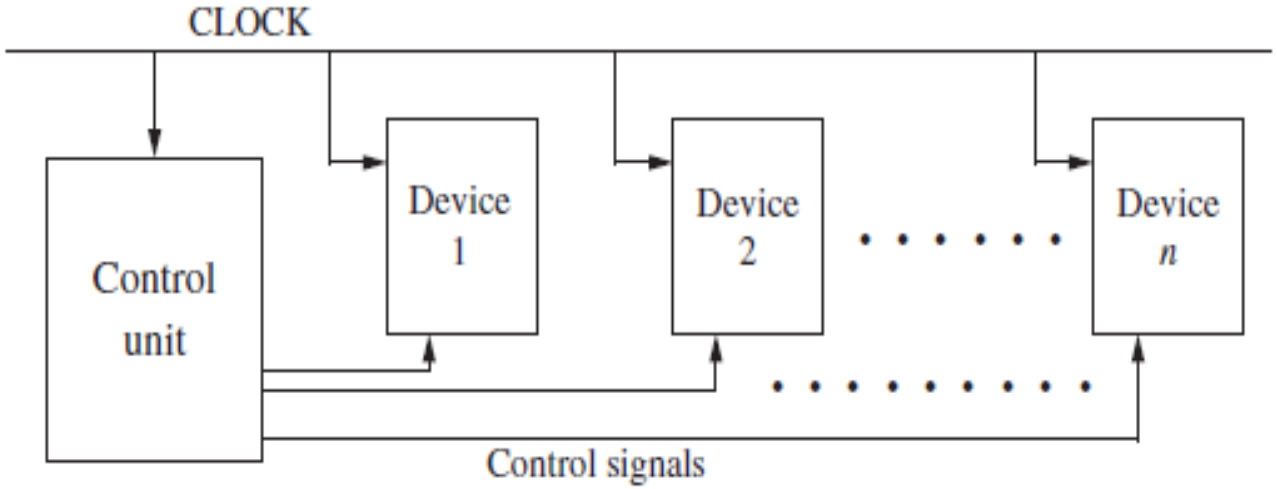
$$t_x = t_{AND\max} + t_{su} = 3\,\text{ns} + 5\,\text{ns} = 8\,\text{ns}$$

- **Glitches In Sequential Circuits:**
- Temporary false values called glitches can appear at the outputs and next states
- For example, if the state table of Figure 1-23(b) is implemented in the form of Figure 1-17, the timing waveforms are as shown in Figure 1-44. Propagation delays in the flip-flop have been neglected; hence state changes are shown to coincide with clock edges.
- In this example, the input sequence is 00101001, and *X is assumed to change in* the middle of the clock pulse. At any given time, the next state and *Z output can* be read from the next state table. For example, at time *ta, State 5 S5 and X 5 0,* so Next State 5 *S0 and Z 5 0. At time tb following the rising edge of the clock,*

Synchronous Design:

- One of the most commonly used digital design techniques is *synchronous design*. In this design, a clock is used to synchronize the operation of all flip-flops, registers, and counters in the system.
- Synchronous circuits are more reliable than asynchronous circuits. In synchronous circuits, events are expected to occur immediately following the active edge of the clock. Outputs from one part have a full clock cycle to propagate to the next part of the circuit.
- Synchronous design philosophy makes design and debugging easier as compared with asynchronous techniques. But synchronous designs consume more power than asynchronous designs because of the power consumed in the clock distribution network.
- Although asynchronous designs can reduce power consumption, it is very difficult to get timing issues under control; hence, despite their high power consumption, designers favor synchronous designs.

- The following figure illustrates a synchronous digital system. Assume that the system is built from several modules or devices. The devices could be flip-flops, registers, counters, adders, multipliers, and so forth. All of the sequential devices are synchronized with respect to the same clock in a synchronous system.



- Synchronous digital system consists of control section and a data section.
- The control section is a sequential machine that generates control signals to control the operation of the data section.
- The data section may generate status signals (not shown in this figure) that affect the control sequence

- In a synchronous digital system, one desires to see all changes happen immediately at the active edge of the clock, but that might not happen in a practical circuit. Modern integrated circuits (ICs) are fabricated at feature sizes such as or smaller than 0.1 microns.
- Modern microprocessors are clocked at several gigahertz. In these chips, wire delays are significant as compared with the clock period. Even if two flip-flops are connected to the same clock, the clock edge might arrive at the two flip-flops at different times due to unequal wire delays. If unequal amounts of combinational circuitry (e.g., buffers or inverters) are used in the clock path to different devices, that also could result in unequal delays, making the clock reach different devices at slightly different times.
- This problem is called clock skew. Clock skew refers to the absolute time difference in clock signal arrival between two points in the clock network.
- Clock skew is often caused by delays in the interconnect within the clock distribution network. It can also be caused by the combinational logic used to selectively gate the clock of certain devices.

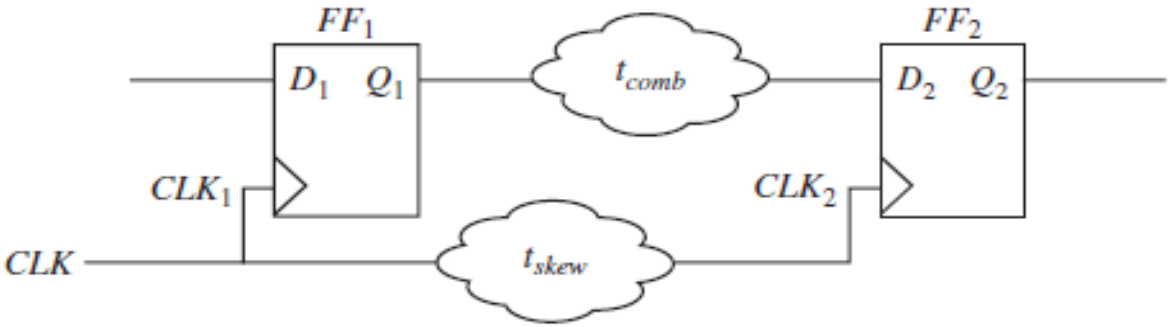
Timing Rules for Circuits with Skew:

- When clock skew is present in a circuit, the timing rules Nos. 1 and 2 get appropriately modified. A positive skew means the capturing flip-flop gets the clock delayed with reference to the launching flip-flop. For a circuit with a positive skew as shown in Figure (a), the timing rules are as follows:

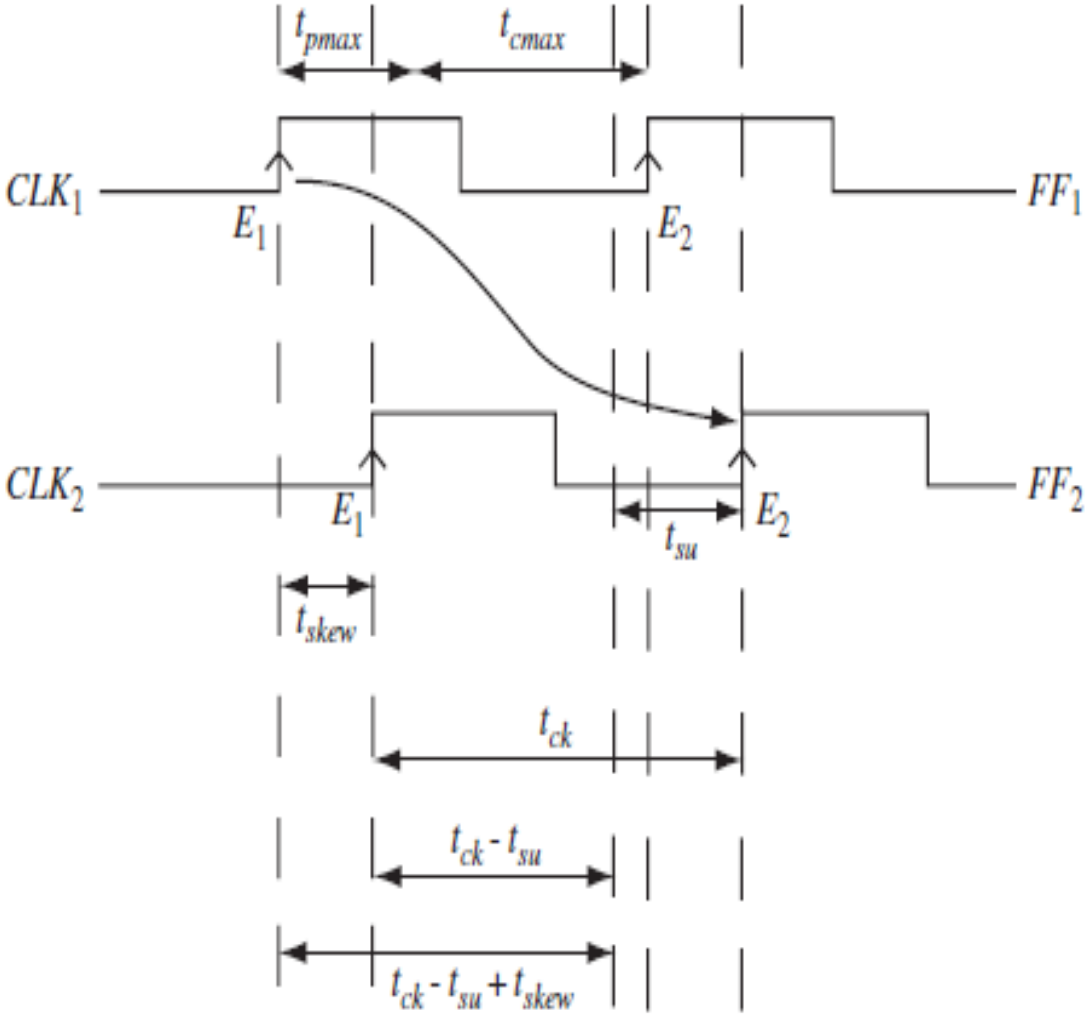
Rule No. 5: $$t_{ck} \geq t_{pmax} + t_{cmax} - t_{skew} + t_{su}$$

Rule No. 6: $$t_{pmin} + t_{cmin} \geq t_h + t_{skew}$$

- Positive skew is good for setup time, but it is bad for hold time.

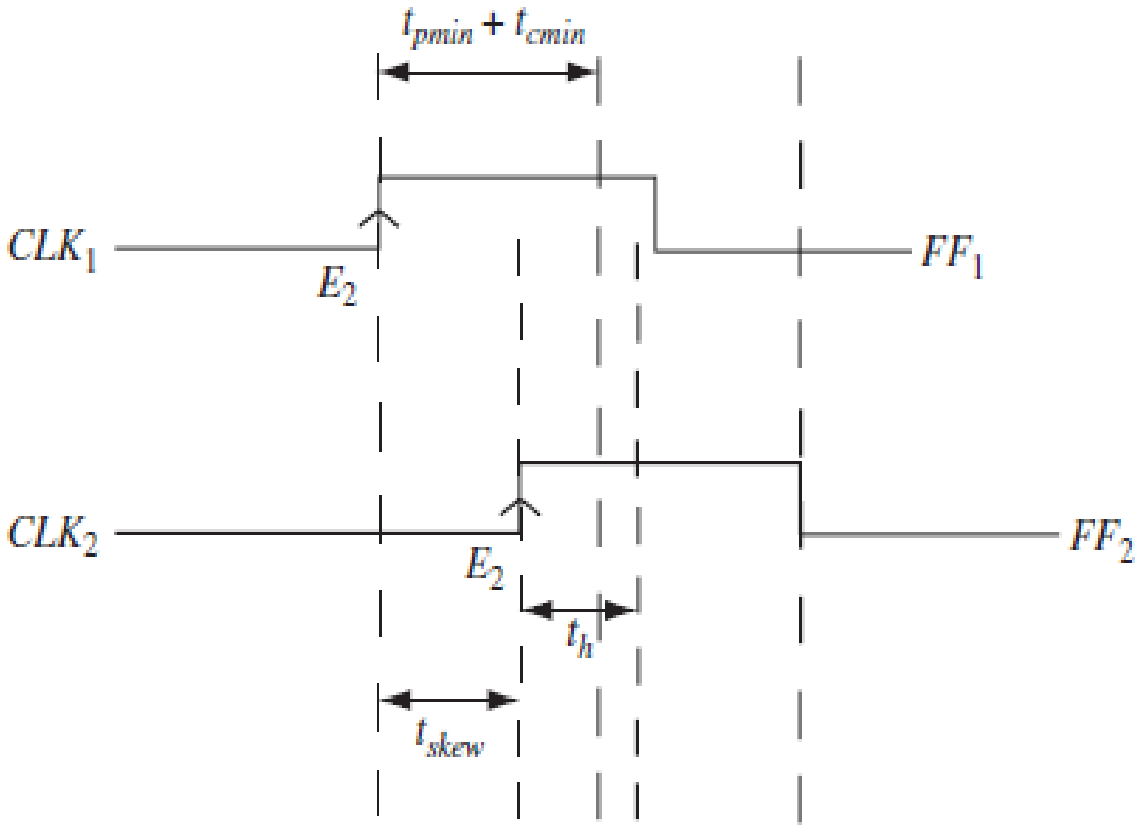


(a) Positive Skew



Condition $t_{pmax} + t_{cmax} \leq t_{ck} - t_{su} + t_{skew}$ not satisfied

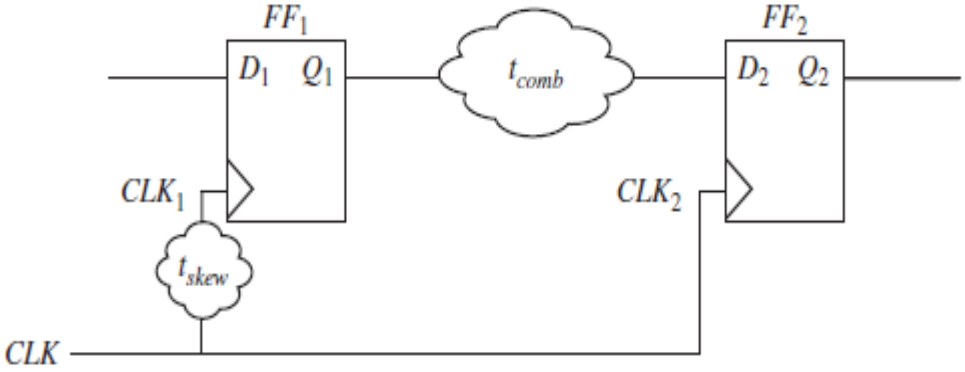
(b) Setup-Time Violation



Condition $t_{pmin} + t_{cmin} \geq t_{skew} + t_{hold}$ not satisfied

(c) Hold-Time Violation

- Negative skew means that the launching flip-flop gets the clock delayed with reference to the capturing flip-flop. Negative skew is illustrated in Figure



- For a circuit that has a negative skew, the timing rules are given by the following equations:

$$t_{ck} \geq t_{pmax} + t_{cmax} + t_{skew} + t_{su}$$

$$t_{pmin} + t_{cmin} \geq t_h - t_{skew}$$

Negative skew is good for hold time, but it is bad for setup time.

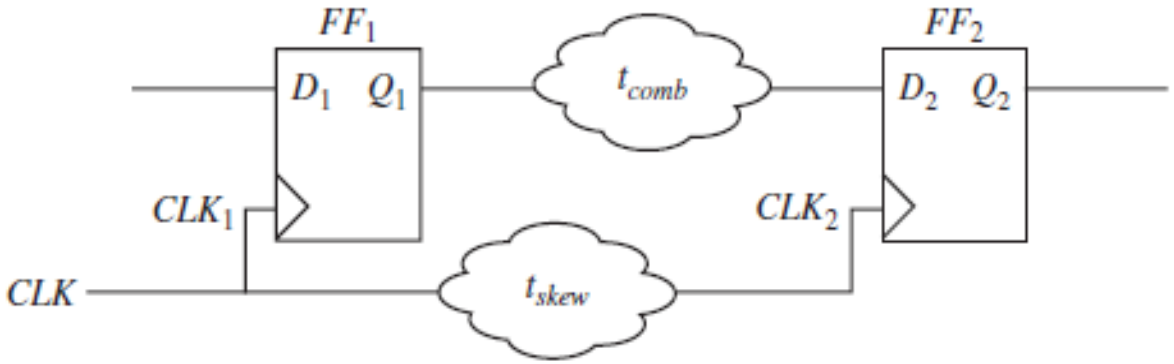
- Consider the circuit shown in Figure with the following delays:

  CLK-to-Q for Flip-flops: 7 ns/9 ns

  Combinational Delay: 4 ns/6 ns

  Setup Time for Flip-Flops: 5 ns

  Hold Time for Flip-Flops: 2 ns



(a) Positive Skew

(a) If skew for the second flip-flop is 3 ns, what is the maximum clock frequency? Compare it with the clock frequency if no skew is present.

Answer: This is a case of positive skew.

$$t_{ck} = t_{pmax} + t_{cmax} - t_{skew} + t_{su}$$

$$= 9\,\text{ns} + 6\,\text{ns} - 3\,\text{ns} + 5\,\text{ns}$$

$$= 17\,\text{ns}$$

The maximum clock frequency when skew is present is 1/17 ns (i.e., 58.82 MHz), whereas without skew the circuit could handle only a maximum frequency of 1/20 ns (i.e., 50 MHz).

- (b) What is the biggest skew that the circuit in Figure can take while meeting the hold-time constraint for this circuit?

Answer:

$$t_{pmin} + t_{cmin} \geq t_h + t_{skew}$$

$$7\,\text{ns} + 4\,\text{ns} \geq 2\,\text{ns} + t_{skew}$$

$$9\,\text{ns} \geq t_{skew}$$

Skew must be less than 9 ns.

(c) If skew for the first flip-flop in Figure 1-48 is 3 ns, what is the maximum clock frequency? Compare it with the clock frequency if no skew is present.

Answer:

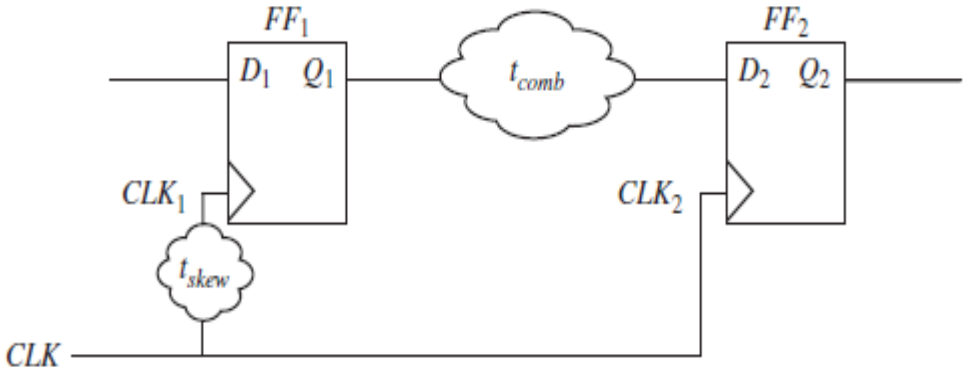
$$t_{ck} = t_{pmax} + t_{cmax} + t_{skew} + t_{su}$$

$$= 9\,\text{ns} + 6\,\text{ns} + 3\,\text{ns} + 5\,\text{ns}$$

$$= 23\,\text{ns}$$

The maximum clock frequency when skew is present is 1/23 ns (i.e., 43.47 MHz), whereas without skew the circuit could handle a maximum frequency of 1/20 ns (i.e., 50 MHz).

(d) What is the biggest skew that the circuit in the following Figure can take while meeting the hold-time constraint for this circuit?



Answer:

$$t_{pmin} + t_{cmin} \geq t_h - t_{skew}$$

$$7\,\text{ns} + 4\,\text{ns} + t_{skew} \geq 2\,\text{ns}$$

Since the first flip-flop's clock is delayed by t_{skew} and it takes an additional 11 ns to reach the second flip-flop, there is no possibility this signal change can cause a hold-time violation.

$$t_{skew} \geq -9\,\text{ns}$$

If the skew at flip-flop 1 increases, there will be no hold-time violation, but of course the maximum allowable clock frequency will reduce.