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(Accredited by National Assessment & Accreditation Council (NAAC) with 'A' grade)

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – 3

Course Name : Digital System Design Using Verilog	Date :	05.12.2020
Course Code : 18EC5DCDSV	Day :	Tuesday
Semester : V	Timings :	1 to 2.30 P.M
Max Marks : 50	Duration :	1½ Hrs.

No.		Question Description	Marks	CO & Levels
Q1	(a)	What is the minimum number of bits needed to encode information with 56 possible values? i)8 ii) 7 iii) 6 iv) 7	1	
	(b)	The _____ configuration memory burns a noticeable amount of power, even when the program is not changed. i)DRAM ii) Flash iii)SRAM iv)PLD	1	
	(c)	How many bits are required for the product of two *fixed-point* numbers with 5 pre-binary-point bits and 9 post-binary-point bits? i) 18 bits ii) 14 bits iii) 28 bits iv) 36 bits	1	
	(d)	Determine the minimum number of Mantissa bits required for a precision of at least 5 decimal digit. i) 17 ii) 14 iii) 13 iv) 16	1	
	(e)	Which of the following statements is True? i) Moore machine is more general than Mealy machine ii) The number of states in a Moore machine must be finite. iii) A Moore machine can be realized using a combinational circuit. iv) None of these	1	
	(f)	For an IC with 1800 pins, what kind of package would most likely be used? i) BGA ii) PLCC iii) TQFP iv)None of these	1	
	(g)	A _____ is an array of basic logic elements, like an FPGA and it is not programmable and omits the programmable interconnect. i) Platform FPGA ii) ASIC iii) ASSP iv)Structured ASIC	1	
	(h)	What is the 7-segment code corresponding to the BCD code 0110? i) 1111001 ii) 1111101 iii) 1100101 iv) 1011111	1	
	(i)	ASSP stands for i) Application specific standard product ii) Application specific standard protocol	1	

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		iii) Analog specific standard product iv) Analog specific standard protocol		
	(j)	To reduce the effects of ground bounce _____ can be placed between power and grounds. i)inductor ii)Variable Resistor iii)Bypass Capacitor iv) none of these	1	
Q2	a)	What is the range and precision of each of the following signed 2s-complement fixed-point representations, with *m* pre-binary-point and *f* post-binary-point bits: i) 14 bits, with *m*=6 and *f* =8 ii) 8 bits, with *m*=4 and *f*=12	03	L3,CO5
	b)	Convert the 55.2546 decimal floating point numbers in to 32 bit single precision IEEE floating point representation.	03	L2,CO5
	c)	With necessary equations show two alternate implementations of Fast carry- Chain full adder cells used in adder	04	L3,CO5
Q3		Design a BCD to Ex-3 code converter. Also write the Verilog code for same.	10	L4,CO6
Q4		Show the multiplication of 14 x 9 using add and shift method with steps, generate the control state graph and table which defines the operation of a binary multiplier and write the Verilog code for same.	10	L4,CO6
		OR		
5	a)	Develop a Verilog model of a code converter to convert the 4-bit Binary to a 4-bit unsigned Gray code integer.	4	L3,CO5
	b)	Design a 4-digit decimal counter with a 7-segment LED display: two 74LS390 dual decade counters, four 74LS47 BCD to 7-segment decoders, four 7-segment displays, plus any additional gates required	6	L3,CO5
6	a)	Bring out the difference between Mealy and Moore sequential circuits	4	L3,CO6
	b)	Multiply two numbers -3/8 and -5/8 using add and shift method. Write the block diagram of 2's complement multiplier and state graph for multiplier control.	6	L3,CO6
		OR		
7	a)	Discuss the signal integrity issues in PCB design and techniques used to solve the signal integrity issues.	6	L3,CO5
	b)	Design the state diagram of a Mealy machine to detect an input sequence 10110 which could overlap. An output 1 is generated when the sequences is detected	4	L4,CO6