



Dayananda Sagar College of Engineering

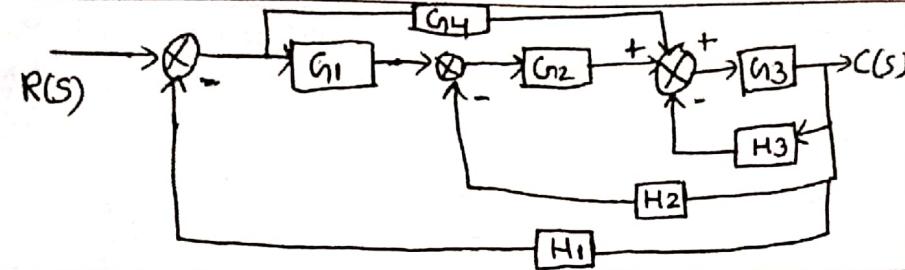
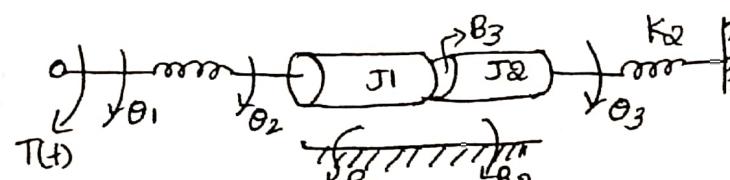
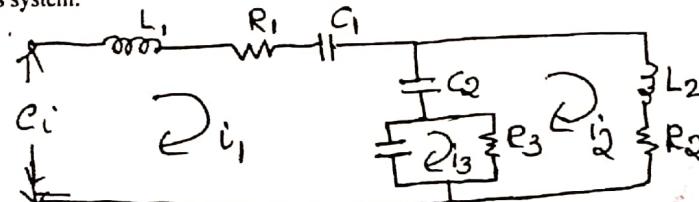
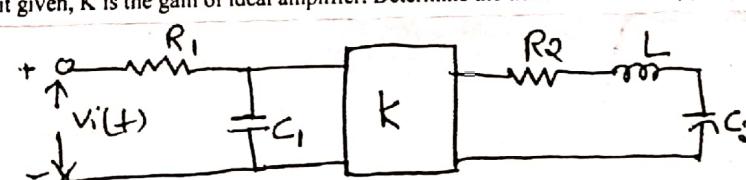
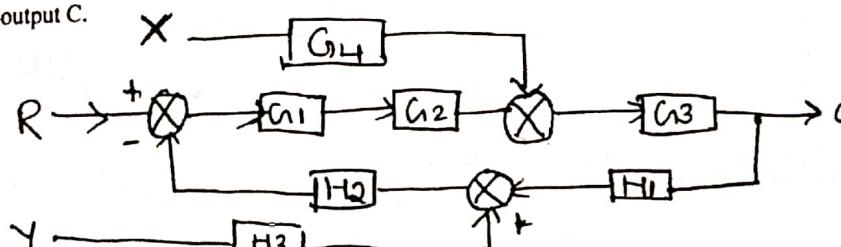
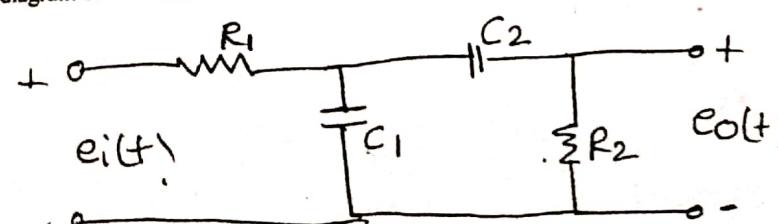
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Department of Electronics & Communication Engg. Continuous Internal Evaluation - I

Course Name :Control System Engineering	Date :	/09/2019
Course Code :17EC5DECSE	Day :	day
Semester :5	Timings :	
Max Marks :50 M	Duration :	1½ Hrs.

No.	Question Description	Mar ks	CO & Levels
Q1	<p>(a) For open loop control system whch. of the following statement is incorrect?</p> <p>i) Errors are caused by disturbances ii) Less expensive</p> <p>iii) Construction is simple iv) Recalibration is required for maintaining the quality of the output</p>	1	CO1 CO2 L4 L6
	<p>(b) Any externally introduced signal affecting the controlled output is called a</p> <p>i) Feedback ii) Stimulus iii) Gain control iv) signal</p>	1	
	<p>(c) While shifting a take-off point after the summing point, which among the following should be added?</p> <p>i) Summing point in series with take-off point ii) Block of reciprocal transfer function</p> <p>iii) Summing point in parallel with take-off point iv) Block of inverse transfer function</p>	1	
	<p>(d) Consider the assertions related to block diagram. Which among them represents the precise condition?</p> <p>A. Block diagram is used for analysis & design of control system. B. Block diagram also provides the information regarding the physical construction of the system.</p> <p>i) A is true, B is false ii) A is false, B is true iii) Both A & B are true iv) Both A & B are false</p>	1	
	<p>(e) A linear system at rest is subject to an input signal $r(t)=1-e^{-t}$. The response of the system for $t>0$ is given by $c(t)=1-e^{-2t}$. The transfer function is</p> <p>i) $(s+2)/(s+1)$ ii) $2(s+1)/(s+2)$ iii) $(s+1)/(s+2)$ iv) $(s+1)/2(s+2)$</p>	1	
	<p>(f) The principle of homogeneity and superposition are applied to</p> <p>i) Lumped system ii) Linear system iii) Stochastic system iv) None of the above</p>	1	
	<p>(g) A control system working under unknown random actions is called</p> <p>i) Adaptive control system ii) Lumped parameter control system</p> <p>iii) Stochastic control system iv) None of the above</p>	1	
	<p>(h) The output signal is fed back at the input side from the _____?</p> <p>i) Summing point ii) Take-off point iii) Reference Signal iv) None of the above</p>	1	
	<p>(i) If finite number of blocks are connected in series or cascade configuration, then how are the blocks combined algebraically?</p> <p>i) By addition ii) By multiplication iii) By differentiation iv) By integration</p>	1	
	<p>(j) In a system zero initial condition means that</p> <p>i) The system is at rest and no energy is stored on any of its components. ii) The system is working with zero stored energy iii) The system is working with zero reference signal iv) None of the above</p>	1	
Q2	<p>For the mechanical system shown in fig.</p> <p>i) Draw the mechanical network ii) Write the differential equations of performance. iii) Obtain electrical analogue circuit based on Direct and Indirect analogy.</p>	10	CO1 1.4
			DD
Q3	<p>(a) Reduce the given block diagram shown in fig. and then obtain the transfer function of the system if $G_1=G_2=2$; $G_3=G_4=3$; $H_1=H_2=1$; $H_3=2$;</p>	10	CO2 L6

				
Q4	(a)	For the mechanical system shown in fig, write mechanical network and obtain mathematical model and electrical analogue circuit based on force-current analogy.	5	CO1 L4
				
	(b)	The force voltage analogy of a mechanical translational system is given in fig. Obtain its analogous system.	5	CO1 L4
				
		OR		
Q5	(a)	Derive the force voltage quantities for simple mechanical system and mention all analogous quantities for translational and rotational system.	5	CO1 L4
	(b)	In the circuit given, K is the gain of ideal amplifier. Determine the transfer function I(s)/V _o (s).	5	CO1 L4
				
Q6	(a)	Using block diagram reduction techniques, find the transfer function from each input to the output C.	10	CO2 L6
				
		OR		
Q7	(a)	Draw block diagram of electric circuit shown and hence determine transfer function E_o(s)/E(s)	10	CO2 L6
				

Department of Electronics & Communication Engg., DSCE, Bangalore
Continuous Internal Evaluation - III

Course Name : Control System Engineering	Date :	/10/2019	
Course Code : 17EC5DECSE	Day :		
Semester : V	Timings :		
Max Marks : 50 M	Duration :	1½ Hrs.	
No.	Question Description	M ks	CO & Levels
Q1 (a)	The root loci starts from _____ i) Poles and ends on zeros ii) Zeros and ends on poles iii) Zero and ends on infinity iv) Poles and ends so infinity	1	
(b)	The open-loop transfer function of a unity feedback control system is $G(s) = 1/(s+2)^2$. The closed loop transfer function will have poles at i) -2,-2 ii) -2,-1 iii) $-2 \pm j1$ iv) -2,2	1	
(c)	Which of the following point is NOT on the root locus of a system with the open loop transfer function $G(s) = K/(s(s+2)(s+3))$ has the breakaway point located at i) (-0.5,0) ii) (-2.548,0) iii) (-4,0) iv) (-0.784,0)	1	
(d)	If the open loop transfer function is the ratio of the numerator polynomial of degree m and a denominator polynomial of degree n, then the integer n-m represents i) Breakaway points ii) Unstable poles iii) Separate root low iv) asymptotes	1	
(e)	The bode plot of T.F $G(s) = S$ is _____ i) Zero magnitude & phase shift ii) Const. magnitude & const. phase shift iii) 20db/decade and phase shift of 90° iv) -20db/decade and const phase shift angle	1	
(f)	The Bode magnitude plot is drawn as i) Decibel Vs ω ii) Decibel Vs $\log \omega$ iii) Decibel Vs $\log_{10} \omega$ iv) Magnitude Vs ω	1	
(g)	In bode plot the transfer function of the given system is marginally stable when i) ω_{gc} is 0db and ω_{pc} is 0° ii) ω_{gc} is 0db and ω_{pc} is 180° iii) ω_{gc} is 3db and ω_{pc} is 0° iv) None of these	1	
(h)	Which among the following plays a crucial role in determining the state of dynamic system? i) State Variable ii) State Space iii) State Vector iv) State Scalar	1	
(i)	State model representation is possible using i) Physical Variables ii) Phase Variable iii) Canonical State Variables iv) All the these	1	
(j)	According to the property of state transition method, $e^A t$ is equal to _____ i) Identity Matrix ii) 0 iii) e^{At} iv) None of these	1	
Q2	The open-loop transfer function of a control system is given by $G(s) = \frac{K}{s(s+2)(s^2 + 6s + 25)}$ Sketch the complete root-locus as K is varied from 0-to Infinity	10	CO4/L4
Q3	A unity feedback control system has $G(s) = \frac{80}{s(s+2)(s+20)}$ Draw the Bode plot. Determine GM, PM, ω_{gc} and ω_{pc} . Comment on the stability.	10	CO5/L5
Q4	Sketch the root locus plot for a closed loop system having an open loop transfer function $G(s)H(s) = \frac{K(s+2)(s+1)}{s(s-1)}$ for all values of K ranging from 0 to infinity. Prove that root locus is a part of circle	10	CO4/L4
	OR		
Q5 (a)	List the four properties of state-transition matrix	4	CO6/L2
(b)	Obtain the state model of the given electrical network	6	CO6/L6
Q6	Plot Bode magnitude and phase diagram for open loop transfer function $G(s) = \frac{100(s+2)}{s(s+1)(s+5)}$	10	CO5/L5
Q7 (a)	Find the state transition matrix for $A = \begin{bmatrix} 0 & -1 \\ 2 & -3 \end{bmatrix}$	5	CO6/L6
(b)	A Linear time invariant system is characterized by the homogeneous state equation $\begin{bmatrix} \cdot \\ X_1 \\ \cdot \\ X_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix}$ Compute the solution of homogeneous equation, assume the initial state vector $X_0 = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$	5	CO6/L6



Department of Electronics & Communication Engg.

Continuous Internal Evaluation - II

Course Name : Control System Engineering	Date :	/10/2019
Course Code : 17EC5DECSE	Day :	
Semester : V	Timings :	
Max Marks : 50 M	Duration :	1½ Hrs.

No.	Question Description	Mks	CO & Levels
Q1	(a) A node having only outgoing branches is i) Input node ii) Output node iii) Incoming node iv) Outgoing node (b) Loop which do not possess any common node are said to be.....loops. i) Forward gain ii) Touching iii) Non touching iv) Feedback gain (c) Velocity error constant of a system is measured when the input to the system is unit function. i) Parabolic ii) Ramp iii) Impulse iv) step (d) Rise time of under damped control system is the time required to rise from i) 10% to 90% of final value ii) 0 to 100% of final value iii) Rise time is undefined for under damped systems. iv) 0 to 50% of final value (e) What is the steady state error of the first order system when subjected to unit step input? i) Zero ii) Infinity iii) Equal to time constant iv) Cannot be determined (f) What is the nature of response of 2nd order system with unit step input for the case when damping ratio (Zeta) tends to zero? i) Exponential ii) Oscillatory iii) Step function iv) Cannot determine with given information about the system. (g) First column elements of the Routh's tabulation are 3, 5, -3/4, 1/2, 2. It means that there are: i) Is one root in the left half of s-plane ii) Are two roots in the left half of s-plane iii) Are two roots in the right half of the s-plane iv) Is one root in the right half of s-plane (h) The necessary condition for the stability of the linear system is that all the coefficients of characteristic equation $1+G(s)H(s)=0$, be real and have the: i) Positive sign ii) Negative sign iii) Same sign iv) Both positive and negative (i) When the number of poles is equal to the number of zeroes, how many branches of root locus tends towards infinity? i) 1 ii) 2 iii) 0 iv) Equal to number of zeros (j) Root locus lies in the real axis of s-plane, when the summation of poles and zeros to the right half of the given point is i) Even ii) Odd iii) Given, data is insufficient iv) Zero	1	
Q2	The performance equations of a controlled system are given by the following linear algebraic equations. Draw the signal flow graph and determine its transfer function using signal flow graph method. $E_1(S)=R(S)-H_1(S)C(S)$ $E_2(S)=E_1(S)-H_1(S)E_4(S)$ $E_3(S)=G_1(S) E_2(S) -H_2(S) C(S)$ $E_4(S)=G_2(S) E_1(S)$ $E_5(S)=G_3(S) E_4(S)$	10	CO2/L3
Q3	Derive the unit step response of a 2 nd order system with underdamped system.	10	CO3/L2
Q4	(a) The open loop transfer function $G(S)=\frac{K}{S(ST+1)}$. i) By what factor the amplitude gain K should be multiplied so that damping ratio is increased from 0.2 to 0.8 ii) By what factor the time constant T should be multiplied so that damping ratio is reduced from 0.6 to 0.3 (b) Determine the number of roots on LHS, RHS and imaginary axis for the system having characteristic equation $S^4+2S^2+1=0$	6	CO3/L3
	OR		
Q5	A given system oscillates with frequency two rad/sec. Find the value of Km margin and P. (a)	5	CO4/L1
	(b) Find the range of K such that the characteristic equation $S^3+3(K+1)S^2+(7K+5)S+(4K+7)=0$ has root more negative than $S = -1$	5	CO4/L1
Q6	Evaluate peak time, rise time, settling time and maximum overshoot for a unity feedback system having transfer function $G(S)=\frac{1}{S(S+2)}$. Also find steady state error when the input to the system is $R(s)=\frac{3}{s}-\frac{2}{s^2}+\frac{1}{s^3}$ $G(S) = \frac{1}{S(S+2)}$	10	CO3/L6
Q7	Construct the root locus diagram for a closed loop system whose loop transfer function is given by $G(s)H(s)=\frac{K}{s(s+5)(s+10)}$. Comment on stability.	10	CO4/L3

Explain the construction rules of root locus



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Department of Electronics & Communication Engg. QUIZ

Course Name : CONTROL SYSTEM ENGINEERING	Date :	/10/2019
Course Code : 17EC5DECSE	Day :	
Semester : V	Timings :	
Max Marks : 10 M	Duration :	10 Mins

No.	Quiz Question Description	Mks
Q1	Characteristic equation is obtained by equating the _____ of a Transfer function to Zero a) Numerator b) denominator c) System resultant gain d) None of the mentioned	1
Q2	Highest power of 'S' in characteristic equation is called as _____ a) Zero b) pole c) Order d) Gain	1
Q3	In Routh's criteria, the number of sign changes equals the number of _____ lying in the right half of S-plane. a) Order b) Zeros c) Roots d) None of the mentioned	1
Q4	The transfer function is applicable to which of the following? a) Linear and Time Variant system b) Linear and Time-Invariant system c) Non- linear system d) None of the mentioned	1
Q5	In signal flow graph, Node having incoming and outgoing branches is known as _____ a) Source node b) Sink node c) Chain node d) None of the mentioned	1
Q6	According to signal flow graph, which among the following represents the relationship between nodes by drawing a line between them? a) Branch b) Self-loop c) Semi-node d) Mesh	1
Q7	If a system is subjected to step input, which type of static error coefficient performs the function of controlling steady state error? a) Position b) Velocity c) Acceleration d) Retardation	1
Q8	Associative law for summing point is applicable only to those summing points which are _____ connected to each other. a) Directly b) Indirectly c) Orthogonally d) Diagonally	1
Q9	What should be the nature of root locus about the real axis? a) Asymmetric b) Symmetric c) Decaying d) Exponential	1
Q10	The capacitance, in force-current analogy, is analogous to _____ a) Momentum b) Mass c) Velocity d) Displacement	1

-T-



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Department of Electronics & Communication Engg. Continuous Internal Evaluation – I

Course Name : Digital Signal Processing

Date : 17/09/2019

Course Code : 17EC5DCDSP

Day : Tuesday

Semester : 5

Timings :

Max Marks : 50 M

Duration : 1½ Hrs.

Marks CO &
Levels

- | | | |
|----|--|--------|
| Q1 | (a) Nature of DTFT is _____
i) Continuous and periodic
ii) Discrete and periodic
iii) Continuous and non-periodic
iv) Discrete and non-periodic | 1 |
| | (b) N-point DFT $X(k)$ and Fourier series coefficients C_k are related by
i) $C_k = X(k)$ ii) $C_k = X(k) / N$ iii) $X(k) = C_k / N$ iv) $C_k = X'(k)$ | 1 |
| | (c) Number of real additions needed for the computation of N point DFT are
i) $2N$ ii) $N(N-1)$ iii) N^2 iv) $2N(N-1)$ | 1 |
| | (d) The twiddle factor is also known as
i) N^{th} root of unity ii) Square root of -1 iii) square root of j iv) None | 1 |
| | (e) Which of the following statements is not true
i) FFT increases speed of operation ii) FFT is an efficient technique
iii) Direct computation of DFT is always preferred iv) $N^2 - N$ addition are needed for direct computation of DFT | 1 |
| | (f) The twiddle factor matrix is
i) an Upper triangular matrix ii) Symmetric matrix
iii) a conjugate symmetric matrix iv) diagonal matrix | 1 |
| | (g) N-point DFT of unit step function $u(n)$ is
i) $NU(k)$ ii) $k\delta(k)$ iii) $N\delta(k)$ iv) $Nu(n)$ | 1 |
| | (h) Which of the following is symmetry property of twiddle factor
i) $W_N^k = W_N^{-k}$ ii) $W_N^k = -W_N^k$ iii) $W_N^{k+N} = W_N^k$ iv) None | 1 |
| | (i) Number of stages(v) of DIT-FFT algorithm are
i) N ii) $N/2$ iii) $\log N / \log 2$ iv) $2N$ | 1 |
| | (j) If v stands for number of stages of DIT-FFT then Number of butterfly structures for computation of N-point DFT are
i) $2Nv$ ii) $N/2v$ iii) Nv^2 iv) $Nv/2$ | 1 |
| Q2 | (a) Use relation between N-point DFT and Z-transform to find N-point DFT of $x(n)$ from its Z-transform $X(Z) = 2 + 3Z^{-1} + (-2/3)Z^{-2} + Z^{-3}$ | 4 |
| | | CO1/L2 |
| | (b) Find 5 point DFT of $x(n) = \delta(n) + 3\delta(n-2) - 5\delta(n-3)$ and draw its magnitude and phase spectrum. | 6 |
| | | CO1/L3 |
| Q3 | Compute 8-point DFT of $x(n) = \cos(n\pi)$ using DIT-FFT algorithm. | 10 |
| | | CO2/L3 |

- Q4** (a) For $x(n)=\{-1, 3, 5, -7, 9, 1\}$ without computing its DFT find the following 5
 1) $X(0)$ 2) $\sum_{k=0}^5 |X(k)|^2$ 3) $\sum_{k=0}^5 (-1)^k X(k)$
- (b) If $x(n)$ is a 6 point sequence with $X(k)$ as its DFT, without computing IDFT
 find sequence $y(n)$ whose 6 point DFT is given by $Y(k)=W_6^{5k} X(k)$. 5 CO2/L3
 OR
- Q5** (a) If $X(k)=\{2, (1+2j), 3, (1-2j)\}$ find $x_1(n)$ corresponding to $X_1(k)=X((k+2))_N$. 4 CO2/L3
 (b) State and prove circular time shifting property of N-point DFT. 6 CO2/L3
- Q6** (a) Find circular convolution $y(n)$ of the sequences $x_1(n)=\{1, -1, 1, -1\}$ and
 $x_2(n)=\{2, 3, -2, -3, 4\}$. 6 CO2/L2
 (b) Derive the expression for speed improvement factor when DIT-FFT used over
 direct method of computation of N-point DFT. 4 CO2/L3
- Q7** Find response $y(n)$ of the LTI system whose impulse response $h(n)=\{1/3, 1/3, 1/3\}$ for the input $x(n)=\{1, -2\}$ using DFT-IDFT. 10 CO2/L3
 OR

Staff : KSG/YBJ/NRS/KP

UG Internal Assessment Test-II**Course: Digital Signal Processing****Course Code: 17EC5DCDSP****Semester: 5****Maximum marks: 50****Duration: 90 min**

1a.	Inputs of DIF-FFT algorithm are in i) Natural order ii) Bit reversed order iii) Gray code iv) None	1 x 10
b.	Number of Twiddle factors needed to compute N-point DFT using DIF-FFT algorithm are i) N ii) $N/2$ iii) $\log_2 N$ iv) $N \log_2 N$	
c.	Number of multiplications needed for the computation of N point DFT using DIF-FFT algorithm are i) $2N$ ii) $N(N-1)$ iii) $(N/2) \log_2 N$ iv) $N \log_2 N$	
d.	The value of twiddle factor W_{16}^7 is _____ $0.9238+j0.3826$ ii) $-0.9238+j0.3826$ iii) $-0.9238 - j0.3826$ iv) None	
e.	Which of the following statements are true? 1) FFT algorithms increase speed of operation 2) FFT is an efficient technique 3) Direct computation of needs more memory than using FFT algorithms 4) Number of computations needed for DIT-FFT and DIF-FFT are same i) all ii) 1,2,3 iii) 1,2,4 iv) 2,3,4	
f.	Chebyshev-I LP filters have _____ i) flat pass band and monotonically decreasing transition band ii) ripples in pass band and monotonically decreasing transition band iii) flat pass band and ripples in stop band iv) None of the answers are true.	
g.	For the given specifications Butterworth filters need order _____ Chebyshev filters. i) higher than ii) lower than iii) same as iv) None	
h.	The poles of stable Chebyshev filters _____ i) Distributed on unit circle ii) lie inside the unit circle iii) lie on ellipse iv) may be i) or ii)	
i.	Chebyshev filters have _____ i) ripple in both pass band and stop band ii) only in pass band iii) only in stop band iv) either in pass band or in stop band	
j.	Number of distinct poles of Butterworth filter of order N i) $2N$ ii) $N/2$ iii) $N-1$ iv) N	
2a.	Find response of an averaging system whose impulse response is $h(n)=\{\frac{1}{4}, \frac{1}{4}, \frac{1}{4}, \frac{1}{4}\}$ for a long input sequence $x(n)=\{0.5, 0.25, 0.125, 0, -0.125, -0.5, -0.125, 0, 0.25, 0.125\}$ using overlap add method.	8 CO2 L2
b	Explain bit reversal ordering of data in FFT algorithms.	2 CO2 L2
3	Design and verify Butterworth HPF filter for the following specifications: $0.8 \leq H_a(s) \leq 1$; for $f \geq 5\text{KHZ}$ $ H_a(s) \leq 0.2$; for $0 \leq f \leq 1\text{KHZ}$	10 CO3 L2

4	Use DIF-FFT algorithm to find 8-point sequence $x(n)$ if $X(k)=\{0.25, -0.3018j, 0, 0, 0.125 - 0.3018j, 0, 0, 0.3028j\}$	10 CO2 /L3
(OR)		
5	Find response $y(n)$ of the LTI system whose impulse response $h(n)=\{0.25, 0.5, 0.25\}$ for the causal input $x(n)=2^{\gamma}(-n)$, $-1 < n < 2$ using DIFFFT algorithm.	10 CO2 /L3
6a. Derive expression for order of Butterworth filter		
b.	Find and plot the poles of the filter having monotonically decaying frequency response with pass band attenuation ≥ 0.8 , up to the cutoff frequency of 100 r/s and stop band attenuation not more than -20 dB for frequency > 400 r/s.	6 CO3 /L3
(OR)		
7	Design a Chebyshev Analog filter (low pass) that has a -3dB cutoff frequency of 100 rad/sec and a stopband attenuation 25dB or greater for all frequencies post 250 rad/sec.	10 CO3 /L3

QUIZ

USN | D S I T G C | | |

Q1	Discretization of DTFT is needed because i) It is proper only in discrete form ii) It convenient to process for digital Devices iii) It gives better information in discrete than continuous iv) None of the answers are proper.	1
Q2	The condition for reconstruction of original an L-point signal from its N-point DFT is i) $N=L$ ii) N must be at least of length L iii) $N < L$ iv) $L=2N$	1
Q3	Circular representation and shifting are used while working with DFTs because i) It is easy to perform circular operations ii) DFT and IDFT are periodic in nature iii) It is convenient to handle while using on hardware iv) None	1
Q4	Value of N to find linear convolution of two L point sequences using N -point DFT is N=L ii) $N=2L$ iii) $N=2L-1$ iv) $N=2L+1$	1
Q5	The DFT of circularly shifted signal _____ i) is also circularly shifted ii) is linearly shifted iii) can be obtained by multiplying DFT of original sequence by a proper complex exponential iv) can be obtained by shifting DFT of original sequence by a proper complex value.	1
Q6	In practice FFT algorithms are preferred over Direct computation to find DFT, because i) Butterfly structure is available for computation ii) They use minimum number of computations iii) Processors are capable of performing complex computations iv) both methods are equally good.	1
Q7	Filters with ripples in both pass band and stop band are known as i) Butterwrth filters ii) Chebyshev typeI filters iii) Lattice filters iv) Chebyshev typeII filters	1
Q8	The order of the filter with 3db cutoff frequency 1kHz and attenuation not more than 20dB at 4kHz is _____ Butterworts i) 3 ii) 2 iii) 4 iv) None	1
Q9	Which of the above statements are true with reference to poles of normalized stable butter worth filters. A) Are distributed on unit circle. B) They lie on the left side of S plane C) Have one pole on real axis if N odd odd. D) No pole on real axis if N is even i) A,B ii) C,D iii) Both i) and ii) iv) None	1
Q10	The cut-off frequency of 3 rd order butterworts filter for a passband edge frequency of 2r/s and maximum allowable ripple of .05 is _____ r/s i) 3 ii) 1.474 iii) 2.898 iv) None	1



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Department of Electronics & Communication Engg. Continuous Internal Evaluation - I

Course Name : Computer Organization

Date : 18/09/2019

Course Code : 17EC5DEC0N

Day : Wednesday

Semester : 5th Semester

Timings :

Max Marks : 50 M

Duration : 1½ Hrs.

No

Question Description

Mks CO & Levels

Q1 (a) Assembly language

- (i) uses alphabetic codes in place of binary numbers used in machine language
- (ii) is the easiest language to write programs
- (iii) need not be translated into machine language
- (iv) None of the above

1

(b) SPEC stands for _____

- (i) Standard Performance Evaluation Code
- (ii) System Processing Enhancing Code
- (iii) System Performance Evaluation Corporation
- (iv) Standard Processing Enhancement Corporation

1

(c) If the length of clock cycle(P) is 0.8ns then the clock rate is

- (i) 1.25Ghz
- (ii) 500MHz
- (iii) 1.45Ghz
- (iv) 250MHz

1

(d) Big-endian is used when lower byte addresses are used for

- (i) LSB
- (ii) MSB
- (iii) Both LSB & MSB
- (iv) None of the above

1

(e) Positive integers can be represented as

- (i) Signed numbers
- (ii) Unsigned number
- (iii) Negative integers
- (iv) Both a and b

1

(f) The address bus is

- (i) Bi-directional
- (ii) Uni-direction
- (iii) Multidirectional
- (iv) None of the above

1

(g) To reduce the memory access time we generally make use of

- (i) Heaps
- (ii) Higher capacity Ram's
- (iii) SDRAM's
- (iv) Cache

1

(h) The instruction : Add LOCA, R0 does _____

- (i) Adds the value of LOCA to R0 and stores in the temp register
- (ii) Adds the value of R0 to the address of LOCA
- (iii) Adds the values of both LOCA and R0 and stores it in R0
- (iv) Adds the value of LOCA with a value in accumulator and stores it in R0

1

(i) Single Precision format comprises of _____ bits.

- (i) 4
- (ii) 8
- (iii) 16
- (iv) 32

1

(j) In the case of Zero-address instruction method the operands are stored in _____

- (i) Registers
- (ii) Accumulators
- (iii) Push down stack
- (iv) Cache

1

Q2

Registers R1 and R2 of a computer contains the decimal values 2900 and 3300. Determine the effective- address of the memory operand in each of the following instructions. Also mention the type of addressing mode.

10 CO1 & L4

- (a) Load R1,55(R2)
- (b) Move #2000,R7
- (c) Store 95(R1,R2),R5
- (d) Add (R1)+,R5
- (e) Subtract -(R2),R5

- Q3 Represent the decimal values 5, -2, -10, -19, 51 and -43 as signed 7 bit numbers 10 CO1 &L2
- (i) Sign Magnitude
 - (ii) 1's Complement
 - (iii) 2's Complement
- Q4 (a) Use a Process with 50 instructions set, of which 40% instructions consume 1 machine cycle, 20% instruction consume 2 machine cycle and remaining instructions consume 3 machine cycle time. Calculate the execution time of the process if operating frequency is 1Mhz and 6 clock cycles make 1 machine cycle. 5 CO2 &L3
- (b) Give the Comparative analysis between RISC and CISC with example. 5 CO2 & L2
- OR**
- Q5 (a) There are 5 processes, P1 is consuming $50\mu\text{Sec}$ and every successive process consumes double the time of previous process. Calculate the SPEC rating of each process and SPEC of entire suite. (Assume reference system which can execute P1 in $100\mu\text{Sec}$ and each successive process with increase of $50\mu\text{Sec}$). 5 CO2 &L3
- (b) Write a program to evaluate the expression $A*B+C*D$ using two address and one address machine instruction. 5 CO1 &L4
- Q6 Describe functional operation of a computer with neat block diagram. 10 CO1 & L1
- OR**
- Q7 (a) Interpret the Basic input output operation with a neat Block diagram. 5 CO1
- (b) Explain the two ways in which byte addresses are arranged with example. 5 & L2

Department of Electronics & Communication Engg, DSCE

Continuous Internal Evaluation – III

Course Name : Computer Organization			Date :	19/11/2019
Course Code : 17EC5DECON			Day :	Wednesday
Semester : 5 A,B,C,D			Timings :	
Max Marks : 50			Duration :	1½ Hrs.
No.		Question Description	Mks	CO & Levels
Q1	(a)	Which of the following is the slowest means of memory access for CPU? i) Registers ii) Secondary Memory iii) Main memory iv) Cache	1	
	(b)	The Maximum address capacity of a processor with 8 bit data bus and 32 bit address bus is i) 64KB ii) 256KB iii) 4GB iv) 8GB	1	
	(c)	A memory device in which a bit is stored as a charge across the stray capacitance i) SRAM ii) EPROM iii) DRAM iv) Bubble memory	1	
	(d)	The minimum time delay between two successive memory read operations is _____. i) Cycle time ii) Latency iii) Delay iv) None of the above	1	
	(e)	Virtual memory is _____. i) memory on the hard disk that the CPU uses an extended RAM ii) in RAM iii) only necessary if you do not have any RAM in your computer iv) a backup device for floppy disk	1	
	(f)	In _____ mapping, the data can be mapped anywhere in the Cache Memory. i) Associative ii) Direct iii) Set Associative iv) Indirect	1	
	(g)	In memory-mapped I/O _____ i) The I/O devices and the memory share the same address space ii) The I/O devices have a separate address space iii) The memory and I/O devices have an associated address space iv) A part of the memory is specifically set aside for the I/O operation	1	
	(h)	To overcome the lag in the operating speeds of the I/O device and the processor we use ----- i) Buffer spaces ii) Status flags iii) Interrupt signals iv) Exceptions	1	
	(i)	The method of accessing the I/O devices by repeatedly checking the status flags is i) Program-controlled I/O ii) Memory-mapped I/O iii) I/O mapped iv) None of the mentioned	1	
	(j)	The method which offers higher speeds of I/O transfers is _____ i) Interrupts ii) Memory mapping iii) Program-controlled I/O iv) DMA	1	
Q2		Sketch and explain organization of 256 x 8 SRAM memory.	10	C05&L3
Q3		Describe the operation of DMA in detail.	10	C06&L1
Q4	(a)	Interpret the operation of 2M x 8 asynchronous DRAM chip.	6	C05&L2
	(b)	Show the working of a single-transistor dynamic memory cell.	4	C05&L2
		OR		
Q5	(a)	Examine the Read/Write operation of an SRAM cell designed using CMOS, with the help of a neat diagram.	6	C05&L4
	(b)	Discuss the following: i) PROM ii) EPROM	4	C05&L2
Q6		With flow diagram, explain each step involved in interrupt driven I/O processing	10	C06&L3
		OR		
Q7		Elaborate and Explain SCSI, USB and PCI Bus	10	C06&L2



Department of Electronics & Communication Engg. Continuous Internal Evaluation - II

Course Name : Computer Organization	Date :	19/10/2019
Course Code : 17EC5DECON	• Day :	Saturday
Semester : 5 th Semester	Timings :	
Max Marks : 50 M	Duration :	1½ Hrs.

No	Question Description	Mk s	CO & Levels
Q1	(a) Which representation is most efficient to perform arithmetic operations on the numbers? i) Sign-magnitude ii) 1's complement iii) 2'S complement iv) None of the mentioned	1	
	(b) If n bit is multiplied with n bit generates i) n/2 bit product ii) n bit product iii) 2n bit product iv) n² bit product	1	
	(c) The Booth recorded multiplier for 01110 is i) +1 0 0 -1 0 ii) -1 1 0 +1 0 iii) 0 +1 0 0 -1 iv) None of them	1	
	(d) Bit pair recording multiplier for -20 (6bits) is i) +1 0 -1 ii) -1 0 -1 iii) -2 0 -1 iv) 0 -1 0	1	
	(e) (+1.5) ₁₀ is represented in single precision Floating point number as i) BFC00000 ii) 3FC00000 iii) CF300000 iv) 2FC00000	1	
	(f) The decoded instruction is stored in _____ i) IR ii) PC iii) Registers iv) MDR	1	
	(g) _____ is used to choose between incrementing the PC or performing ALU operations. i) Conditional codes ii) Multiplexer iii) Control unit iv) None of the mentioned	1	
	(h) If the control signals are generated by combinational logic, then they are generated by a type of controlled unit. i) Micro programmed ii) Software iii) Logic iv) Hardwired	1	
	(i) A set of microinstructions for a single machine instruction is called _____ i) Program ii) Command iii) Micro program iv) Micro command	1	
	(j) Temporary registers used in single bus organization are.... i) R0, Y, Z ii) Y, Z, Temp iii) IR, Y, Z iv) None of the above	1	
Q2	Perform signed multiplication of following 2's complement numbers using i) Booth's Algorithm ii) bit-pair recoding method. a) A=110011 and B=101100 b) A=001111 and B=001111	10	C03&L3
Q3	Elaborate the working of single bus organization with neat diagram.	10	C04&L2
Q4	(a) Perform the multiplication of 9X15 using sequential multiplication with neat diagram. (5 bits)	5	C03&L3
	(b) Represent the following number in single precision floating point notation. (-35.125) ₁₀	5	C03&L3
	OR		
Q5	(a) Perform the division of 16/5 using Non-restoration technique with neat diagram.(5 bits)	5	C03&L3
	(b) Convert the following single precision floating point number into actual decimal number. (C4900000)	5	C03&L3
Q6	(a) List the control sequences required to execute the instruction ADD R1,(R3) in single bus organization.	5	C04&L3
	(b) Describe with neat diagram detailed Hardwired control organization.	5	C04&L3
	OR		
Q7	(a) Explain with neat diagram the organization of storing a word in memory.	5	C04&L3
	(b) Describe with neat diagram Micro programmed control organization.	5	C04&L3



Department of Electronics & Communication Engg.

QUIZ

Course Name : COMPUTER ORGANIZATION		Date :	19/10/2019
Course Code : 17EC5DECON		Day :	SATURDAY
Semester : 5 TH SEMESTER		Timings :	
Max Marks : 10 M		Duration :	10 Mins
No.	Quiz Question Description	Mks	
Q1	What is the need for reduced instruction chip? (a) Relatively large instruction types and addressing modes. (b) Fixed and easily decoded instruction formats. (c) Slow multiple-cycle instruction execution. (d) Microprogrammed control.	1	
Q2	Define interface. (a) refers to the boundary between two circuits or devices (b) refers to the no boundary between two circuits or devices (c) refers to the boundary between two hardware devices (d) none of the above	1	
Q3	Represent the decimal value of 14 in 2's complement (a) 0001111(b) 1110000 (c) 0001110(d) 0101110	1	
Q4	In the case of, Zero-address instruction method the operands are stored in _____ (a) Registers (b) Accumulators (c) Push down stack (d) Cache	1	
Q5	When 1101 is used to divide 100010010 the remainder is _____ (a) 101 (b) 11 (c) 0 (d) 1	1	
Q6	The order in which the return addresses are generated and used is _____ (a) LIFO (b) FIFO (c) Random (d) Highest priority	1	
Q7	The assembler stores the object code in _____ (a) Main memory (b) Cache (c) RAM (d) Magnetic disk	1	
Q8	The most efficient method followed by computers to multiply two unsigned numbers is _____ (a) Booth algorithm (b) Bit pair recording of multipliers (c) Restoring algorithm (d) Non restoring algorithm	1	
Q9	For the addition of large integers, most of the systems make use of _____ (a) Fast adders (b) Full adders (c) Carry look-ahead adders (d) None of the mentioned	1	
Q10	The addressing mode/s, which uses the PC instead of a general purpose register is _____ (a) Indexed with offset (b) Relative (c) direct (d) both Indexed with offset and direct	1	

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**Department of Electronics & Communication Engg.****Continuous Internal Evaluation - I**

Course Name : Management and Entrepreneurship	Date :	/09/2019
Course Code : 17HS51MEP	Day :	
Semester : 5 th	Timings :	
Max Marks : 50 M	Duration :	1½ Hrs.

No.	Question Description	Mks	CO & Levels
Q1 (a)	At what level of an organisation does a corporate manager operate? (1) Functional. (2) Operational. (3) Middle level. (4) Top level	1	
	Which of these is not part of the recognised challenges for modern managers? (b) (1) Micro-managing the workforce. (2) Managing communications. (3) Managing change. (4) Managing the learning organisation	1	
	(c) Which one is not a recognised key skill of management? (1) Conceptual skills. (2) Human skills. (3) Technical skills. (4) Writing skills	1	
	What is a social enterprise concerned with? (d) (1) Profit maximization. (2) Maximising market share. (3) Providing public service. (4) Running a business to create social benefit	1	
	What is the guiding principle of scientific management? (e) (1) Experimentation (2) Fluid working relationships (3) Freedom of association (4) One best way to do a job	1	
	What is the optimal span of control? (f) (1) 2 (2) 5 (3) 7 (4) None of the above	1	
	Which of the following is not a recognised type of plan? (g) (1) Business (2) Succession (3) Ad hoc (4) Financial	1	
	What time-frame do strategic plans relate to (h) (1) Long-term (2) Medium-term (3) Short-term (4) Unspecified time it takes to achieve an aim	1	
	What does authority refer to (i) (1) The ability to organise people (2) The power to command and direct (3) The need for order (4) The right to change jobs	1	
	What does a chain of command extend from (j) (1) Bottom to top (2) Top to bottom (3) Diagonally (4) Laterally	1	
Q2 (a)	Outline the principal functions of management.	6	CO3/L4
(b)	Analyze the roles of a manager in a modern Indian company.	4	CO3/L4
Q3 (a)	Illustrate the concept of centralization and decentralization. Differentiate between decentralization and delegation.	10	CO1/L3
Q4 (a)	Elaborate the importance of planning & explain the hierarchy of Planning OR	10	CO3/L5
Q5 (a)	Differentiate between Line and Staff Organization.	5	CO1/L4
(b)	Outline the importance of Matrix organization & list 2 industries where it is used.	5	CO1/L4
Q6 (a)	Develop the general principles of management as laid down by Henri Fayol OR	10	CO1/L3
Q7 (a)	Examine the importance of departmentalization? Summarize different types of departmentalization.	10	CO3/L4



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Dayananda Sagar
College of Engineering

Department of Electronics & Communication Engg. QUIZ

Course Name : Management and Entrepreneurship	Date :	17/10/2019
Course Code : 17HS51MEP	Day :	Thursday
Semester : 5th	Timings :	
Max Marks : 10 M	Duration :	10 Mins

No.	Quiz Question Description	Mks
Q1	A typical inventor is usually _____ a) Highly creative & in love with the invention b) Does not encourage change c) Willing to modify the invention in order to augment commercial benefit d) None of the given options	1
Q2	As a company grows, the entrepreneur should focus on his/her: a) technical ability to complete a task b) written communication. c) management and motivation skills. d) public speaking	1
Q3	One of the first steps needed to determine the break-even point is to: a) do a ten-year sales projection. b) separate the company's expenses into the fixed and variable categories c) take a full-item inventory. d) Determine current assets.	1
Q4	The most common form of organization for a small business is: a) partnerships b) corporations c) sole proprietorships d) limited companies	1
Q5	Which of the following is the backbone of financial plan? a) Budgeting b) Capital c) Nature of business d) All of the given options	1
Q6	:- A business center that offers working space and specialized support for new ventures is called: a) Isolator b) Injector c) Incubator d) Integrator	1
Q7	:- A network entrepreneur is an individual who identifies his or her business idea a) On their own b) Through the assistance of a paid consultant c) Through social contacts d) With one or more partners	1
Q8	:- The increase in home businesses has occurred for several reasons. Which of the following is one of the reasons? a) The increase in utility prices b) The increase in tax rates c) The increasing use of the Internet d) Fewer people seeking financial security	1
Q9	The practice of using outside firms to perform tasks that could be performed internally is called: a) Flexibility b) Fragmentation c) Greening d) Outsourcing	1
Q10	:- Which of the following is the career solution for many underemployed managers? a) Fortune 500 companies b) Entrepreneurship c) Downsizing d) To remain unemployed	1

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – II

Course Name : Management and Entrepreneurship	Date :	/09/2019
Course Code : 17HS51MEP	Day :	
Semester : 5 th	Timings :	
Max Marks : 50 M	Duration :	1½ Hrs.

No.	Question Description	Mks	CO & Levels
Q1	<p>Employee motivation is considered a very important element in achieving overall goal of organization. In order to keep employees motivated, an employer needs to understand that</p> <ol style="list-style-type: none"> Every employee is satisfied by increase in salary Every employee is different, motivate them according to their needs. Each employee will work hard if they get paid on time Rewards are the key to keep the employees motivated and self-satisfied 	1	
	<p>(b) Which of the below is an example of democratic leadership?</p> <ol style="list-style-type: none"> "We can go to the zoo or bird park for this outing. I am OK with anything." "I need your feedback before I make decision. Please speak out." "Everybody will fall in at 1400 hour sharp." None of these 	1	
	<p>(c) Regarding leadership, which statement is false?</p> <ol style="list-style-type: none"> Leadership does not necessarily take place within a hierarchical structure of an organisation When people operate as leaders their role is always clearly established and defined Not every leader is a manager All of the above 	1	
	<p>(d) Leadership in India is mostly based upon:</p> <ol style="list-style-type: none"> Management by inheritance Management by chromosomes Both 1 & 2 None of the above 	1	
	<p>(e) Challenging the status quo and enabling creativity is</p> <ol style="list-style-type: none"> Work of an entrepreneur Leadership role Need in self – fulfillment All of the above 	1	
	<p>(f) Target coaching, work planning, mutual goal setting and performance objectives are all terms used to specify concept called</p> <ol style="list-style-type: none"> behavioral rating approach management by objectives combination method critical incident method 	1	
	<p>(g) The resistance of employees in an organization against flexibility, growth, and diversification can be overcome by developing _____.</p> <ol style="list-style-type: none"> Entrepreneurship Managerial domain Intrapreneurship Administrative domain 	1	
	<p>(h) If you own your own business you will need to know how to calculate your profit. Which one is a calculation of profit?</p> <ol style="list-style-type: none"> Sales-months in a year Sales-expenses Total sales-expenses Monthly sales expenses 	1	
	<p>(i) What type of entrepreneurial business sells products directly to the people who use or consume them?</p> <ol style="list-style-type: none"> Manufacturing Wholesaling Retailing Service 	1	
	<p>(j) People who own, operate, and take risk of a business venture:</p> <ol style="list-style-type: none"> Aptitude Employee Entrepreneurs Entrepreneurship 	1	
Q2	(a) Distinguish between various leadership types.	10	C05/L2
Q3	(a) Identify Maslow's theory of hierarchical needs, how do you apply these principles in motivating?	10	C02/L3
Q4	(a) Outline the functions of an entrepreneur.	10	C03/L2
	OR		
Q5	(a) Outline the characteristics of an Entrepreneur, summarize the differences between Intrapreneur and Entrepreneur.	10	C02/L2
Q6	(a) Compare between various kinds of entrepreneurs.	10	C03/L2
	OR		
Q7	(a) In the management process, identify the steps in controlling	6	C01/L2
	(b) List the various principles of directing.	4	C01/L2

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Department of Electronics & Communication Engg., DSCE
Continuous Internal Evaluation – III

Course Name: Hardware Description Language
 Course Code: 17EC5DCHDL
 Semester: V
 Max Marks: 50 M

Date : /10/2019
 Day :
 Timings :
 Duration : 1½ Hrs.

No		Question Description	Mk s	CO & Levels
Q1	(a)	Synthesis is the process of _____ between the simulation domain and the hardware domain. a) function b) operation c) mapping d) assignment	1	
	(b)	_____ provides Verilog Synthesis information on the inputs and outputs and their types. a) module b) process c) architecture d) entity	1	
	(c)	In the hardware domain, we do not have a mapping for _____ a) procedure b) task c) variable d) All the above	1	
	(d)	The only loop supported for synthesis is _____ a) while b) for c) case d) all the above	1	
	(e)	_____ is used to understand the basic primitives and operators in the RTL description during Synthesis mapping. a) Translation b) RTL c) Logic optimization d) Unoptimized representation	1	
	(f)	PLAs, PALs, and FPGAs are all which type of device? a) SLD b) EPROM c) PLD d) SRAM	1	
	(g)	_____ usually have built-in programming and erase capability. a) EEPROM b) EPROM c) PROM d) Flash memory	1	
	(h)	The general arrangement of PLA is _____ structure. a) AND/OR b) OR/AND c) NAND/NOR d) EX-OR/OR	1	
	(i)	In mealy machine, the O/P depends upon? a) State b) Previous State c) State and Input d) Only Input	1	
	(j)	If the input bit sequence 0110, then the Manchester code is _____ i) 1001 ii) 0110 iii) 01101001 iv) 10010110	1	
Q2		Write VHDL code for signal assignment statement Y=5X with X as 2 bit. Show the synthesized logic symbol and gate level diagram. Write structural code in Verilog using gate level diagram.	10	CO-5 L-3
Q3		Design a BCD to Ex-3 code converter using D flip-flops.	10	CO-6 L-2
Q4	(a)	Explain the VHDL synthesis information extracted from entity when inputs and outputs are declared as Bit_vector and Signed respectively.	2	CO-5 L-3
	(b)	Write a behavioural code in Verilog for a 2X1 multiplexer. Show the gate level synthesis diagram and write structural code in Verilog using gate level diagram.	8	
		OR		
Q5	(a)	Explain in detail about the synthesis design flow with diagram.	6	CO-5 L-3
	(b)	Show the synthesis information extracted from the example given below: package codes is type op is (add, mul, divide, none); end; use work.codes; entity ALUS2 is port (a,b: in std_logic_vector(3 downto 0); Cin: in std_logic; opc: in op; z: out std_logic_vector (7 downto 0); Cout: out std_logic; err: out Boolean); end ALUS2;	4	
Q6		Explain all the code conversion techniques. Also, Design of a Moore Sequential network for NRZ to Manchester Conversion.	10	CO-6 L-2
		OR		
Q7	(a)	Write a note on Read Only Memory (ROM)	4	CO-6 L-3
	(b)	Find the reduced PLA table to realize the following function using PLA. F1 (a,b,c) = $\Sigma m(0,3,5,6,7)$ F2 (a,b,c) = $\Sigma m(0,2,3,5,7)$	6	



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Department of Electronics & Communication Engg. Continuous Internal Evaluation - II

Course Name: Hardware Description Language
Course Code: 17EC5DCHDL
Semester: V
Max Marks: 50 M

Date : /10/2019

Day :

Timings :

Duration : 1½ Hrs.

Mk CO &
s Levels

No	Question Description	
Q1	<p>(a) In a VHDL behavioural description, the statements are executed _____ (i) Concurrently (ii) Sequential (iii) Both (a) and (b) (iv) None of the above</p> <p>(b) The Common use for "forever" loop is to generate _____ (i) pointers (ii) Clocks (iii) Components (iv) Global Constants</p> <p>(c) Variable assignment statements are calculated and assigned immediately with _____ time between calculation and assignment. (i) Delta delay (ii) no delay (iii) Simulation screen delay (iv) None</p> <p>(d) _____ loop is used only in Verilog. (i) Next (ii) for (iii) repeat (iv) while</p> <p>(e) Equivalent signed number for 9 is _____ (i) 1001 (ii) 01001 (iii) 10111 (iv) None of the above</p> <p>(f) The predefined word generate is mainly used for _____ (i) Repetition of concurrent statements (ii) Repetition of Sequential statements (iii) Both (i) and (ii) (iv) none of above</p> <p>(g) Generic in VHDL and parameter in Verilog are used to define _____ (i) Variables (ii) Global Constants (iii) arrays (iv) pointers</p> <p>(h) Procedures and functions in VHDL are _____ (i) Dataflow statements (ii) Behavioral statements (iii) Structural statements (iv) All the above</p> <p>(i) "return" is the keyword used by _____ function to return the output value. (i) Verilog (ii) VHDL (iii) both (iv) None of the above</p> <p>(j) VHDL Packages can include the declarations of _____ (i) constant (ii) function (iii) type (iv) All the above</p>	1
Q2	Design BOOTH's algorithm to Multiply 5*-7 and write Verilog program.	10 CO-3 L-4
Q3	Write structural VHDL and Verilog code for N bit Asynchronous up counter using Generate statement.	10 CO-4 L-3
Q4	Write a VHDL program for behavioural description of D latch using signal assignment statements and variable assignments statements with timing diagram.	10 CO-3 L-3
OR		
Q5	<p>(a) Explain the execution of process statement.</p> <p>(b) Explain the following sequential statements in HDL with examples i) caseX and caseZ ii) repeat iii) forever iv) next and exit</p> <p>Write a structural description using VHDL and Verilog to implement for JK flip-flop.</p>	2 CO-3 8 L-2 10 CO-4 L-3
OR		
Q7	Write VHDL and Verilog function to find the largest of the two signed numbers.	10 CO-4 L-3



Department of Electronics & Communication Engg.

QUIZ

Course Name: Hardware Description Language

Date : /10/2019

Course Code: 17EC5DCHDL

Day :

Semester: V

Timings :

Max Marks : 10 M

Duration : 10 Mins

No.	Quiz Question Description	Mks
Q1	If $A = 4'b011$ and $B = 4'b0011$, then the result of $A**B$ will be (a) 6 (b) 9 (c) 27 (d) Invalid expression	1
Q2	Port Buffer supported in Verilog. (i) True (ii) False	1
Q3	In Net-list language, the net-list is generated after _____ of VHDL code. (a) Simulation (b) Synthesis (c) Compile (d) None of the above	1
Q4	The 'abs' operator has only one operand. (i) True (ii) False	1
Q5	Values belonging to an _____ data type are pointers. (a) Record (b) Array (c) Access (d) Integer	1
Q6	A major difference between VHDL and Verilog structural description is the (a) Availability of primitive gates to the user (b) Verilog recognizes all the primitive gates (c) VHDL packages do not recognize any gates unless package is linked (d) all of the above	1
Q7	Which of the following is the correct order for a structural model in VHDL? (a) Libraries, Entity declaration, Component declaration, Component instantiation (b) Libraries, Component declaration, Entity declaration, Component instantiation (c) Libraries, Entity declaration, Component instantiation, Component declaration (d) Component declaration, Libraries, Entity declaration, Component instantiation	1
Q8	All statements in structural description are executed _____ (a) Concurrently (b) Sequential (c) Both (a) and (b) (d) None of the above	1
Q9	Which statements are true based on Behavioural description? (a) Process is inactivated only on event occurs in sensitivity list (b) All Verilog statements are concurrent (c) Both (i) and (ii) (d) None of the above	1
Q10	Which sequential statement is used only as a latch? (a) for (b) while (c) if (d) case	1

DAYANANDA SAGAR COLLEGE OF ENGINEERING

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UG Internal Assessment Test-I**Course: Hardware Description Language****Course Code: 17EC5DCHDL****Maximum****marks: 50****Semester: 5****Duration: 90 min**

1a.	Which of the following statements is/are false for Verilog modules? a. A module can contain one or more definitions of other modules. b. If a module X is instantiated 4 times within another module Y, only one copy of X is created, which is linked 4 times. c. A module can be instantiated within another module any number of times. d. If a module X is instantiated 4 times within another module, 4 copies of X are created.	1 x 10
b.	What does the statement “assign f = (a b) & (c d)” signify? a. A gate level netlist consisting of two OR gates, and one AND gate. b. A behavioral description of the function f. c. A structural description of the function f. d. None of these.	
c.	Which of the following is/are true for register type variables? a. They always map to a hardware register after synthesis. b. They can be used in an expression on the RHS of an “assign” statement. c. They may also be used to model a combinational circuit. d. None of these.	
d.	For the following Verilog code segment, what will be the number of bits in “sum” as deduced during synthesis? <code>wire [6:0] data1, data2; reg [7:0] dummy; integer sum; sum = (data1 + data2) + dummy;</code> a. 7 b. 8 c. 9 d. None of these	
e.	For the following Verilog code segment, if the initial value of IR is 2D00 023A (in hexadecimal), what will be the value of “memaddr” in decimal? <code>wire [31:0] IR; wire [7:0] opcode; wire [23:0] address; wire [23:0] memaddr; assign opcode = IR[31:24]; assign address = IR[23:0]; assign memaddr = address + 100;</code> a. 685 b. 670 c. 723 d. None of these	
f.	Which of the following does not represent a behavioral representation for the function $f = A \cdot B + B \cdot C + C \cdot A$? a. A truth table of the function f b. The Verilog specification: assign f = (A & B) (B & C) (C & A); c. A netlist consisting of three 2-input AND and one 3-input OR gate d. None of these	
g.	What does Moore's law specify?	

	a. The number of transistors in a VLSI chip will increase exponentially with time. b. The power consumption in a VLSI chip will increase linearly with time. c. The clock speed of a VLSI chip will increase exponentially with time. d. None of these.	
h.	What function do the following Verilog module implement? module guess (f, a, b, c); input a,b,c; output f; wire t; assign t = (a ^ b); assign f = t & c; endmodule a. $f = a' \cdot b \cdot c + a \cdot b' \cdot c$ b. $f = a' \cdot b \cdot c + a \cdot b \cdot c'$ c. $f = a' \cdot c + a \cdot b \cdot c'$ d. None of these	
i.	Collection of different data types can be defined in VHDL using the predefined word..... a. Array b. bit-vector c. record d. type	
j.	Reduction type logical operators operate on a. Single Operand b. Sequential c. Both a, b d. None of the above	
2a.	Describe the structure of VHDL and Verilog module	4 CO2 /L3
b	With neat timing diagram and evaluation of expressions for sum and carry write a VHDL code for Full Adder	2 CO2 /L2
3	Mention the verilog reduction operators and explain them with an example	5 CO3 /L2
3b.	Write a verilog code to find the LCM of two numbers	5
4	Explain how does Composite type data is operated in VHDL with required format and an example	10 CO2 /L3
	(OR)	
5	Write a Verilog module to implement a 2-bit full adder at the behavioral level. The module will take the following arguments: i. Two 2-bit input bits A and B, ii. One 1-bit carry input Cin, iii. One 2-bit output Sum, iv. One 1-bit carry output Cout	10 CO2 /L3
6a.	Write a Verilog module to implement a D-type latch at the behavioral level. The module will take as arguments the following: 1-bit data input D 1-bit latch enable input En 1-bit output Q	10 CO3 /L2
	(OR)	
7	Write a VHDL behavioral description for a 4 X 1 Mux with tri state output using else if statement	10 CO3 /L3

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – III

Course Name : Microwave and Antenna Theory	Date :	19/11/2019
Course Code : 17EC5DCMAT	Day :	Tuesday
Semester : 5	Timings :	9.30 AM
Max Marks : 50 M	Duration :	1½ Hrs.

No	Question Description	Mar-ks	CO & Levels
I	<p>(a) In broadside array, all the elements in the array should have similarexcitation along with similar amplitude excitation for maximum radiation. i) Phase ii) Voltage iii) Current iv) None</p> <p>(b) The directivity for an isotropic source is</p> <p>(c) Which pattern is generated due to plotting of square of amplitude of an electric field? i) Field Pattern ii) Voltage Pattern iii) Power Pattern iv) All of these</p> <p>(d) The radiation pattern of a half-wave dipole has the shape of a</p> <p>(e) At 20 GHz, the gain of a parabolic dish antenna of 1 meter diameter and 70% efficiency is.. i) 45 dB ii) 15dB iii) 35dB iv) 25dB</p> <p>(f) The gain of the helical antenna is proportional to..... i) $1/\text{HPBW}$ ii) HPBW iii) $(\text{HPBW})^2$ iv) $1/(\text{HPBW})^2$</p> <p>(g) Patch antennas are the antennas of small size and are made of: i) Coaxial cables ii) Microstrip lines iii) Waveguides iv) Strip Lines</p> <p>(h) When an electromagnetic wave travels from transmitter to receiver, which factor/s affect/s the propagation level? i) Curvature of Earth ii) Roughness of Earth iii) Magnetic field of earth iv) All of these</p> <p>(i) Which kind of polarization is provided by helical antennas? i) Linear ii) Elliptical iii) Circular iv) All of these</p> <p>(j) Which antennas are renowned as patch antennas especially adopted for space craft applications? i) Aperture ii) Microstrip iii) Array iv) Lens</p>	1	
2	Develop an expression for total field at a far distance r and analyze the radiation pattern for a two point source spaced half wavelength apart and fed with source of same magnitude and phase.	10	L4/ CO5
3	Illustrate the working principle of Yagi-Uda Antenna with neat diagram.	10	L2/ CO6
4	Develop an expression for radiation resistance of short electric dipole and determine the maximum effective aperture of a short dipole. OR	10	L3/ CO2
5	Justify the statement - Radiation resistance of $\lambda/2$ antenna is 73 ohms.	10	L3/ CO4
6	Illustrate the working of Log Periodic antenna with structural geometry and neat sketches. OR	10	L2/ CO6
7	<p>a) A free-space LOS microwave link operating at 10 GHz consists of a transmitter and a receiver antenna each having a gain of 25dB. The distance between the two antennas is 30 km and the power radiated by the transmit antenna is 10 W. Calculate the path loss of the link and the received power.</p> <p>b) Illustrate the working of Parabolic reflectors.</p>	05	L4/ CO4
		05	L2/ CO6

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – Make Up

Course Name : Microwave and Antenna Theory	Date :	22/11/2019
Course Code : 17EC5DCMAT	Day :	Friday
Semester : 5	Timings :	9.30 AM
Max Marks : 50 M	Duration :	1½ Hrs.

No	Question Description	Marks	CO & Levels
1	(a) The leakage current in the transmission lines is referred to as the i) Resistance ii) Radiation iii) Conductance iv) Polarization (b) Which of the following parameters is not a primary parameter? i) Resistance ii) Attenuation constant iii) Capacitance iv) Conductance (c) The characteristic impedance of a transmission line with impedance and admittance of 16 and 9 respectively is i) 25 ii) 1.33 iii) 7 iv) 0.75 (d) The incident wave amplitude is 24 units. Find the reflected wave amplitude if the reflection coefficient is 0.6 i) 14.4 ii) 16.6 iii) 13.3 iv) 11.1 (e) The incident and the reflected voltage are given by 15 and 5 respectively. The transmission coefficient is i) 1/3 ii) 2/3 iii) 1 iv) 3 (f) The basic equation of radiation that is applied to any antenna irrespective of the type of the antenna is i) $iL = Qv$ ii) $iQ = Lv$ iii) $i/L = Q/v$ iv) $L/i = v/Q$ (g) As the beam area of an antenna decreases, the directivity of the antenna i) Increases ii) Decreases iii) Remains unchanged iv) Depends on the type of the antenna (h) of an antenna is defined as the ratio of the induced voltage to the incident electric field. i) Effective height ii) Gain iii) Directivity iv) Loss (i) A dipole antenna is also called as? i) Marconi antenna ii) Yagi antenna iii) Bidirectional antenna iv) Hertz antenna (j) Which one of the following statement is true for log periodic antenna? Frequency dependent antenna Frequency independent iii) Isotropic antenna iv) None of the above	1 1	
2	a. Elaborate on standing wave with necessary mathematical expressions and draw the standing wave pattern for lossless line. b. S-parameters of a two port network are given by $S_{11}=0.2 0^\circ$, $S_{12}=0.6 90^\circ$, $S_{21}=0.6 90^\circ$, $S_{22}=0.1 0^\circ$. Justify that the network is reciprocal but not lossless. Also determine the return loss at port 1 when port 2 is short circuited.	06 04	
3	Analyze the three different wave polarization techniques with necessary equations.	10	
4	Starting from the geometry of helical antenna, distinguish between different modes of operation.	10	
	OR		
5	Differentiate any three antennas in terms of their parameters and applications.	10	
6	Elaborate the characteristics of Magic Tee with the schematic diagram. A Magic Tee is terminated at collinear port 1 and 2 and difference port 4 by impedances of reflection coefficients $\Gamma_1 = 0.5$, $\Gamma_2 = 0.6$, $\Gamma_4 = 0.8$ respectively. If 1W power is fed at the sum port 3, estimate the power reflected at the port 3 and power transmitted to the other three ports.	10	
	OR		
7	Develop an expression for T and inspect the relation $T = Zl/Zo(1 - \Gamma_l^2)$ for $Zl = 70 + j 50 \Omega$ and $Zo = 75 + j 0.01 \Omega$	10	



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Department of Electronics & Communication Engg. Continuous Internal Evaluation - II

Course Name : Microwave and Antenna Theory	Date :	/09/2019
Course Code : 17EC5DCMAT	Day :	
Semester : 5	Timings :	
Max Marks : 50 M	Duration :	1 1/2 Hrs.

No	Question Description	Mks	CO & Levels
Q1	(a) Rectangular waveguide acts as filter i) High Pass ii) Low Pass iii) Band Pass iv) Band Rejection (b) Which mode is not possible in rectangular waveguide? i) TE ii) TEM iii) TM iv) None (c) In a two-hole directional coupler, the holes are separated by i) $\lambda_g / 8$ ii) $\lambda_g / 2$ iii) $\lambda_g / 4$ iv) λ_g	1	
	(d) Which of the following relations would be correct for the magic T-Junction shown in the Fig. ? (I) $S_{13} = S_{23}$ (II) $S_{14} = S_{24}$ (III) $S_{12} = 0$ (IV) $S_{34} = 0$ (i) (I), (II) & (III) (ii) (I), (II) & (IV) (iii) (II), (III) & (IV) (iv) (I), (III) & (IV)	1	
	(e) Choose the wrong statements related to rectangular waveguide: (I) Dominant mode has the lowest cutoff frequency (II) Dominant mode has highest cutoff frequency (III) Dominant mode has the highest cutoff wavelength (IV) Dominant mode has the lowest cutoff wavelength	1	
	(f) An EM wave is said to be vertically polarized when the angle between the electrical field and earth is i) 50° ii) 20° iii) 90° iv) 180°	1	
	(g) With an increase in the operating frequency of a micro strip line, the effective dielectric constant of a micro strip line: i) Increases ii) Decreases iii) Independent of frequency iv) Depends on the material of the substrate used as the Microstrip line	1	
	(h) The solid area through which all the power radiated by the antenna is: i) Beam area ii) Effective area iii) Aperture area iv) Beam efficiency	1	
	(i) The number N of radio transmitters or point sources of radiation distributed uniformly over the sky which an antenna can resolve is given by: i) $4\pi / \Omega A$ ii) $2\pi / \Omega A$ iii) $\pi / \Omega A$ iv) None	1	
	(j) An antenna has a field pattern of $E(\theta) = \cos 2\theta$, θ varies between 0 and 90° . Half power beam width of the antenna is: (i) 33° (ii) 66° (iii) 1200° (iv) None	1	
Q2	a. For a rectangular waveguide: <ul style="list-style-type: none"> • What is the critical condition for the evanescence and obtain the expression for cutoff frequency? • Obtain the guide propagation constant when the wave is propagating. • Obtain the guide propagation constant when the wave is attenuated. 	06	L3CO2
	b. The cutoff wave lengths of a rectangular waveguide was measured to be 8 cm and 4.8 cm when excited in TE_{10} and TE_{11} modes respectively. Determine the dimensions of the wave guide.	04	L4CO4
Q3	Illustrate the operation of Precision phase shifter with relevant mathematical equations.	10	L3CO3
Q4	a. A 20 mW signal is fed into one of the collinear port 1 of a lossless H-plane T-junction. Determine the power delivered through each port when other Ports are terminated in matched load.	05	L4CO4

	b.	Assess the directivity of the source using direct method and approximate method for the pattern $u = u_m \sin \theta \sin^3 \phi$ $0 < \theta < \pi, 0 < \phi < \pi$	05	L4CO4
		OR		
Q5	a.	The normalized radiation intensity of an antenna is represented by $U(\theta) = \cos^2(\theta) \cos^2(3\theta)$, ($0 \leq \theta \leq 90^\circ, 0 \leq \phi \leq 360^\circ$). Determine the <ul style="list-style-type: none"> • Half-Power Beam Width HPBW (in radians and degrees) • First-Null Beam Width FNBW (in radians and degrees) 	06	L4CO4
	b.	For a directional coupler incident power is 550 mW. Determine the power in main arm and auxiliary arm where coupling factor is 30 dB.	04	L4CO4
Q6		Apply the concepts of Maxwell's equation to construct the Hz expression for TE mode of rectangular wave guide.	10	L3CO2
		OR		
Q7		Outline important antenna parameters (at least five) and support with final mathematical expression for each.	10	L3CO2

Course Name : Microwave and Antenna Theory

Course Code : 17EC5DCMAT

Semester : 5

Max Marks : 10 M

Date : /10/2019

Day :

Timings :

Duration : 10 Mins

No.	Quiz Question Description	Marks
Q1	If in an airline, adjacent maxima are found at 12.5cm and 37.5cm, then operating frequency is a) 1.5 GHz b) 600 MHz c) 300 MHz d) 1.2 GHz	1
Q2	Consider a transmission line of characteristic impedance 50Ω . Let it be terminated at one end by $+j50\Omega$. The VSWR produced by it in the transmission line will be a) 1 b) 0 c) infinity d) $+j$	1
Q3	When used as a duplexer, the H-plane arm of an E-H plane junction is terminated in a a) transmitter b) receiver c) matched load d) antenna	1
Q4	In a rectangular waveguide there is one half wave variation of electric field across the narrow dimension and two half variations of electric field across the wider dimension. What is the mode? a) TM12 b) TE12 c) TE21 d) TM21	1
Q5	What are the directions of E and H in TEM mode transmission lines with respect to direction of propagation ? a) Both E and H are entirely transverse to the direction of propagation. b) E is entirely transverse to H and H has a component in the direction of propagation. c) H is entirely transverse to E and E has a component in the direction of propagation. d) Both E and H have components in the direction of propagation	1
Q6	A rectangular waveguide having TE ₁₀ mode as dominant mode is having cut off frequency of 18GHz for the TE ₃₀ mode. The broad wall dimension of rectangular waveguide is a) 5/3 cms b) 5 cms c) 5/2 cms d) 10 cms.	1
Q7	The effective area of a transmitting antenna is 1sqm, the effective area of receiving antenna is 0.9 sqm and wavelength is 0.03m. If the distance between transmitter and receiver is 100m and power transmitted is 100W, then power received will be a) 1 W b) 10 W c) 30 W d) 40 W.	1
Q8	An antenna when radiating has a highly directional radiation pattern. When receiving its radiation pattern a) is more directive b) is less directive c) is the same d) exhibits no directivity at all	1
Q9	A rectangular waveguide of internal dimensions (a=4cm and b=3cm) is to be operated in TE ₁₁ mode. The minimum operating frequency is a) 6.25 GHz b) 6.0 GHz c) 5.0 GHz d) 3.75 GHz.	1
Q10	A microwave network is supposed to be matched at all ports if in the S matrix a) All diagonal elements are zero b) All diagonal elements are equal but non-zero c) All diagonal elements are complex d) Any row or column is zero	1