

USN **DAYANANDA SAGAR COLLEGE OF ENGINEERING***(An Autonomous Institute Affiliated to VTU, Belagavi)***UG Semester End Examination, December 2017****Course: Hardware Description language****Code: EC55****Maximum marks: 100****Duration: 3 hours****Answer five full Questions. All questions carry equal marks**

- | | | Marks |
|---|---|----------------|
| 1 | a Describe VHDL scalar data types with an example.
b Mention the different types of description used in HDL? Explain any two in brief with example.
c Distinguish between VHDL and Verilog HDL. | 08
08
04 |
| | (OR) | |
| 2 | a Explain the structure of VHDL and Verilog module with an example.
b Design an unsigned 2x2 combinational array multiplier and write VERTILOG code for the same using data flow description.
c Name the different types of operators in HDL (Both VHDL and Verilog). Explain the bitwise, unary and Boolean logical operations present in Verilog with examples. | 08
08
04 |
| 3 | a Design a 2 bit magnitude comparator and write the VHDL code for the same using data flow description.
b Write the syntax of the following sequential statements with example in VHDL i) If statement ii) if-else statement iii) Case statement iv) loop statement
c Explain Verilog repeat & forever with an example. | 08
08
04 |
| | (OR) | |
| 4 | a Develop a VHDL code to realize a 3 bit counter using case statement.
b Explain Booth algorithm with flow chart and Write a Verilog description to multiply two 4 bit numbers. | 08
12 |
| 5 | a Design a VHDL structural description code to realize full adder using two half adders and OR gate.
b Write structural VHDL/Verilog code for (N+1) bit Magnitude comparator using Generate statement. | 10
10 |
| | (OR) | |
| 6 | a Explain the format of Procedure and Task with suitable examples.
b Develop a VHDL/Verilog function to find the largest of the two signed numbers.
c Write short notes on VHDL package with examples. | 10
06
04 |



- 7 a Define Synthesis. With flowchart, explain the steps involved in Synthesis process. 08
b Generate VHDL code for signal assignment statement $Y=2*X+5$. Show the synthesized logic symbol and gate level diagram. Write structural code in Verilog using gate level diagram. 12
- (OR)
- 8 a Illustrate the following with examples 06
i. Synthesis information extraction from entity in VHDL
ii. Verilog synthesis information extraction from module inputs and outputs
- b Implement the gate level circuit for the following Verilog code: 06
- ```
module if_st(a,y);
 input[2:0]a;
 output y;
 reg y;
 always @ (a)
 begin
 if (a<3'b101)
 y=1'b1;
 else
 y=1'b0;
 end
 endmodule
```
- c Explain the mapping of else if statement by taking the following example. 08  
The system with BP (input) and ADH (output) are of natural type ranging 0 to 7 and 0 to 15 respectively. Assume that if BP less than or equal to 2, then  $ADH=15$  or if BP greater than or equal to 5 then  $ADH=0$  otherwise  $ADH = BP *(-5) +25$ .
- 9 a Write a note on Read Only Memory (ROM), Programmable Logic Array (PLA), and Programmable Array Logic (PAL). 10  
b Implement a Mealy sequential network with ROM and D flip-flops. Draw the ROM truth table and ROM realization code. 10
- (OR)
- 10 a Implement  $f_1(a, b, c) = \sum m(3, 5, 6, 7)$  and  $f_2(a, b, c) = \sum m(0, 2, 4)$  using PLA 06  
b Design a BCD to Ex-3 code converter using D flip-flops and implement the same using VHDL code. 14

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**DAYANANDA SAGAR COLLEGE OF ENGINEERING**

(An Autonomous Institute Affiliated to VTU, Belagavi)

**UG Make-up Examination, January/ February 2018****Course: Hardware Description language****Code: EC55****Maximum marks: 100****Duration: 3 hours****Answer five full Questions. All questions carry equal marks**

- |   |                                                                                                                                                                                                                                                                                                                                                                                                   | Marks          |
|---|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 1 | a Elaborate on the general structure of VHDL and Verilog module with suitable examples.<br>b Mention different styles of describing a digital system. Give a brief explanation of any two types in both VHDL and Verilog.                                                                                                                                                                         | 10             |
|   | (OR)                                                                                                                                                                                                                                                                                                                                                                                              |                |
| 2 | a Describe the arithmetic operators used in VHDL and Verilog with examples.<br>b Design a HDL code for 2 bit magnitude comparator using VHDL and Verilog.<br>c Explain the shift operators used in VHDL.                                                                                                                                                                                          | 08<br>07<br>05 |
| 3 | a Explain Booth algorithm with flow chart and Write a VHDL description to multiply two 4 bit numbers.<br>b Design a behavioral description for a 2x1 multiplexer with tri state output using else if statement (VHDL and Verilog).                                                                                                                                                                | 12<br>08       |
|   | (OR)                                                                                                                                                                                                                                                                                                                                                                                              |                |
| 4 | a Develop a behavioral description for D latch using signal assignment statements and variable assignments statements with timing diagram (VHDL only).<br>b Elaborate on different types of looping statements available in HDL. Explain any 3 in detail.                                                                                                                                         | 10<br>10       |
| 5 | a Design structural code for a 3 bit ripple carry adder (VHDL & Verilog).<br>b Explain the concepts of Procedure and Task with suitable examples.                                                                                                                                                                                                                                                 | 10<br>10       |
|   | (OR)                                                                                                                                                                                                                                                                                                                                                                                              |                |
| 6 | a Write structural code for (N+1) bit Magnitude comparator using Generate statement (VHDL only).<br>b Develop a function to find the largest of the two signed numbers (VHDL & Verilog).<br>c Explain the use of Generic (VHDL) and parameter (Verilog) with an example.                                                                                                                          | 10<br>08<br>02 |
| 7 | a Define Synthesis. With flowchart, explain the steps involved in Synthesis process.<br>b Explain the mapping of else if statement(VHDL) by taking the following example. The system with BP (input) and ADH (output) are of natural type ranging 0 to 7 and 0 to 15 respectively. Assume that if BP less than 2, then ADH=15 or if BP greater than 5 then ADH is 0 otherwise ADH = BP *(-5) +25. | 08<br>12       |



- 8      a With suitable examples extract information from entity and module. Show the mapping in hardware domain.  
       b Illustrate the mapping of if, if else and case statements used in HDL. Show synthesized logic symbol and gate level diagram.

9      a Write a note on i) PLA     ii) PAL  
       b Design a BCD to Ex-3 code converter using D flip-flops.

(OR)

10     a Realize the following using PLA  
           $F_1(a,b,c) = \Sigma m(3,4,5,7)$   
           $F_2(a,b,c) = \Sigma m(0, 2, 5, 6)$   
           $F_3(a,b,c) = \Sigma m(2,3,4,6,7)$   
       b Explain the basic structure of ROM with suitable diagram.  
       c Using 4 input and 3 output PAL, implement the function.  
           $F_1(a,b,c) = \Sigma m(0,3,5,6,7)$   
           $F_2(a,b,c) = \Sigma m(1,2,3,5,7)$

plain the basic structure of ROM with suitable diagram.  
ing 4 input and 3 output PAL, implement the function.  
 $(a,b,c) = \Sigma m(0,3,5,6,7)$   
 $(a,b,c) = \Sigma m(1,2,3,5,7)$

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**DAYANANDA SAGAR COLLEGE OF ENGINEERING**(An Autonomous Institute Affiliated to VTU, Belagavi)  
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560078**UG Semester End Examination, December 2018/January 2019**

Course: **Hardware Description Language**  
 Course Code: **EC55**  
 Semester: **V**

Maximum marks: **100**  
 Duration: **3 hours**

**Note:** i). Question **ONE** (a to t) has to be answered from pages 5 to 7 only.  
 ii). Question 1 to 4 is compulsory.  
 iii). Any missing data should be suitably assumed.

| <b>Q. No.</b> |                                                                                                                                                              | <b>Marks</b> |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
| 1             | a) How the Signal acts within a Process and outside the Process.                                                                                             | 01           |
|               | b) Verilog is an IEEE standard of,<br>(i)IEEE 1346 (ii)IEEE 1364 (iii)IEEE 1394 (iv)IEEE 1349                                                                | 01           |
|               | c) The hardware delay in HDL code is considered as _____ delay.                                                                                              | 01           |
|               | d) In VHDL, the user can define their own data type by using the predefined word called _____                                                                | 01           |
|               | e) "always" in Verilog is ----- kind of statement                                                                                                            | 01           |
|               | f) If A= 4'b0100 and B= 4b'0011, then the result of A**B will be<br>(i)16 (ii) 12 (iii) 64 (iv) Invalid expression                                           | 01           |
|               | g) Which type of Assignment Statements will be used in Data Flow Level and Behavioural Level VHDL?                                                           | 01           |
|               | h) The 'next' and 'Exit' statements are used in VHDL (i) True (ii) False VHDL structural description recognizes all gates.<br>(i) True (ii) False            | 01           |
|               | i) Generic in VHDL and parameter in Verilog are used to define                                                                                               | 01           |
|               | j) In a Verilog behavioural description, the statements are executed _____<br>(i) Concurrently (ii) Sequential (iii) Both (a) and (b) (iv) None of the above | 01           |
|               | k) _____ is the keyword used by VHDL function to return the output value.                                                                                    | 01           |
|               | l) Synthesis mapping of the case statement is very similar to mapping the _____ statement                                                                    | 01           |
|               | m) Synthesis information extracted from the following code is:<br><pre>module system1v (a,b,d);   input a, b;   output [3:0] d;   -----   Endmodule</pre>    | 01           |
| n)            | In the hardware domain, we have a mapping for procedure, task and function.<br>(i)True (ii) False                                                            | 01           |
| o)            | VHDL structural description recognizes all gates<br>True or False                                                                                            | 01           |



- p) A major difference between VHDL and Verilog structural description is the  
(a) Availability of primitive gates to the user  
(b) Verilog recognizes all the primitive gates  
(c) VHDL packages do not recognize any gates unless package is linked  
(d) all of the above
- q) In case of \_\_\_\_\_ machine, present output is not a function of present inputs but is a function of past inputs.
- r) Output of Mealy machine only depends on its current state and not on the current input.
- s) PLAs perform the same basic function as  
i) a ROM    ii) a PLD    iii) a PAL    iv) a SRAM
- t) Procedures and functions in VHDL are  
(i) Dataflow statements (ii) Behavioral statements (iii) structural statements
- 2 a) Explain the following Data type  
i) Physical data type, ii) user defined data type, iii) Array type iv) Nets & parameters.
- b) Explain how to assign a delay to the signal assignment statement? Write a HDL code for 2x1 multiplexer with active low using signal declaration and assignment statements.
- 3 a) Develop HDL behavioural description code for SR flip-flop using case statement and variable declaration.  
b) Multiply  $7 \times 4$  (Multiplier  $X = -4$  and Multiplicand  $Y = 7$ ) using BOOTH algorithm and write VHDL program and draw the flow chart.
- 4 a) Write HDL behavioural description of a full adder using procedure and task.  
b) Write structural VHDL/Verilog code for N bit Asynchronous down counter using Generate statement.
- 5 a) Find the gate level mapping for the following Verilog code:  

```
module if_st(a,y);
 input[2:0]a;
 output y;
 reg y;
 always @ (a)
 begin
 if (a<3'b101)
 y=1'b1;
 else
 y=1'b0;
 end
 endmodule
```
- b) Write VHDL code for signal assignment statement  $Y=2*X+3$ . Show the synthesized logic symbol and gate level diagram. Write structural code in Verilog using gate level diagram.

OR

6 a) Explain the mapping of the signal assignment statement,  $Y \leq X$ ; to gate level, with suitable example. 08

b) Draw the gate level synthesis information, extracted from the following Verilog code. 08

```
always @ (s,a,b)
begin
if (s == 1'b1)
Y=b;
else
Y=a;
end
```



7 a) Show the nMOS PLA design to realize the following functions 08

$$\begin{aligned}F1(a, b, c) &= \Sigma m(0, 1, 4, 6) \\F2(a, b, c) &= \Sigma m(2, 3, 4, 6, 7) \\F3(a, b, c) &= \Sigma m(0, 1, 2, 6) \\F4(a, b, c) &= \Sigma m(0, 1, 2, 6)\end{aligned}$$

b) Implement the state table using Rom and D flip-Flops. Write VHDL code that describe the systems. 08

| Q1, Q2 | Q1', Q2' |     | Z   |     |
|--------|----------|-----|-----|-----|
|        | X=0      | X=1 | X=0 | X=1 |
| 00     | 01       | 10  | 0   | 1   |
| 01     | 10       | 00  | 1   | 1   |
| 10     | 00       | 01  | 1   | 0   |

OR

8 a) Implement  $f1(a, b, c) = \Sigma m(3, 5, 6, 7)$  and  $f2(a, b, c) = \Sigma m(0, 2, 4)$  with a PLA 08

b) Design a BCD to Ex-3 code converter using D flip-flops. 08

|     |  |  |  |  |  |  |  |
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## DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi)  
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560078

### UG Semester End Examination, May-June 2019

Course: **DIGITAL SYSTEM DESIGN USING VERILOG** Maximum marks: 100  
 Course Code: **TE43** Duration: 03 hours  
 Semester: **IV**

**Note:** i). Question ONE (a to t) has to be answered from pages 5 to 7 only.  
 ii). Question 1 to 4 is compulsory.  
 iii). Any missing data should be suitably assumed.

| Q. No. |                                                                                                                                                                                                                          | Marks |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| 1      | a Define digital systems?                                                                                                                                                                                                | 01    |
|        | b How information is represented in digital systems?                                                                                                                                                                     | 01    |
|        | c Define noise margin?                                                                                                                                                                                                   | 01    |
|        | d Give an example of combinational circuit                                                                                                                                                                               | 01    |
|        | e Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?<br>i. Data selector ii. Data distributor iii. Data sharing iv. data mixer | 01    |
|        | f Define decoder?                                                                                                                                                                                                        | 01    |
|        | g Devise a binary code for the state of a road traffic light. The possible states are red, yellow and green                                                                                                              | 01    |
|        | h Can parity checking be used to correct the effect of a bit flip? Yes or no                                                                                                                                             | 01    |
|        | i What number is represented by the unsigned binary number 1011012?                                                                                                                                                      | 01    |
|        | j What is the disadvantage of ripple carry adder                                                                                                                                                                         | 01    |
|        | k Show the addition of the unsigned binary numbers 10101111002 and 00110100102.                                                                                                                                          | 01    |
|        | l Write the binary number 01011101 in octal and in hexadecimal.                                                                                                                                                          | 01    |
|        | m What are registers?                                                                                                                                                                                                    | 01    |
|        | n What is the function of clock enable input in flip-flop                                                                                                                                                                | 01    |
|        | o Write the difference between synchronous and asynchronous circuits                                                                                                                                                     | 01    |
|        | p What are latches?                                                                                                                                                                                                      | 01    |
|        | q Expand FPGA                                                                                                                                                                                                            | 01    |
|        | r If a memory has 32,768 locations, each of 32 bits, what is the total capacity of the memory                                                                                                                            | 01    |



- s What is the effect of a write operation? What is the effect of a read operation? 01
- t The memory that can only be read, are called\_\_\_\_\_ 01
- 2 a What are sequential circuits? Develop a sequential circuit that has a single data input signal, S, and produces an output Y. the output is 1 whenever S has the same value over three successive clock cycles, and 0 otherwise. Assume that the value of S for a given clock cycle is defined at the time of the rising clock edge at the end of the clock cycle. 08
- b Describe the following terms used in the design of digital systems  
i. Simulation and synthesis ii. Floor planning iii. Mapping ,Placing and routing 08
- 3 a Elaborate the concept of Bit errors in digital systems. 08
- b Develop a verilog model for a Decoder for use in the ink-jet printer. The decoder has three input bits representing the choice of color cartridges and six output bits, one to select each cartridge. And the cartridges are black, cyan, magenta, yellow, light cyan and light magenta. 08
- 4 a Explain fast-carry-chain adder. And also discuss the advantages over ripple carry adder. 08
- b Draw and explain a circuit composed of a gate that implements the 4-bit wide carry-look ahead generator. 08
- 5 a Design 4 bit ripple counter and also write its timing diagram. 08
- b Design a circuit for modulo 8 counter and develop a verilog code for the decade counter. 08
- OR
- 6 a Design a circuit that counts 16 clock cycles and produces a control signal, ctrl, which is 1 during every eighth and twelfth cycle. Develop a verilog model. 08
- b Develop a Verilog model for negative-edge-triggered flip-flop with clock enable, negative-logic asynchronous preset and clear, and both active-high and active-low outputs. It is illegal for both preset and clear to be active together. 08
- 7 a What is meant by the terms volatile and nonvolatile? Explain Asynchronous Static RAM with timing for write and read operations. 08
- b Test whether there is an error in ECC word 000111000100 and if so correct it. 08
- OR
- 8 a Design 64X8 bit composite memory using 16K X 8 bit memory component. 08
- b Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001. 08

**DAYANANDA SAGAR COLLEGE OF ENGINEERING**(An Autonomous Institute Affiliated to VTU, Belagavi)  
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560078**UG Makeup Examination, July 2019**

Course: **Digital System Design Using Verilog**  
 Course Code: **TE43**  
 Semester: **IV**

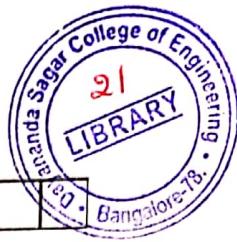
Maximum marks: **100**  
 Duration: **03 hours**

**Note:** i). Question ONE (a to t) has to be answered from pages 5 to 7 only.  
 ii). Question 1 to 4 is compulsory.  
 iii). Any missing data should be suitably assumed.

| Q. No. |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Marks |
|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| 1      | a) According to the IC fabrication process logic families can be divided into two broad categories as<br>i. RTL and TTL ii. HTL and MOS iii. ECL and DCL iv. BIPOLAR and MOS                                                                                                                                                                                                                                                                                                           | 01    |
|        | b) Define sequential circuits.                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 01    |
|        | c) What is active high logic?                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 01    |
|        | d) What are the two values used in binary represent?                                                                                                                                                                                                                                                                                                                                                                                                                                   | 01    |
|        | e) Do wires contribute to delay in a circuit?                                                                                                                                                                                                                                                                                                                                                                                                                                          | 01    |
|        | f) Devise a one-hot code for the state of the traffic light. The possible states are red, yellow and green.                                                                                                                                                                                                                                                                                                                                                                            | 01    |
|        | g) Define bit flip.                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 01    |
|        | h) What is the purpose of a multiplexer?                                                                                                                                                                                                                                                                                                                                                                                                                                               | 01    |
|        | i) What decimal digit is represented by the BCD code 0101?                                                                                                                                                                                                                                                                                                                                                                                                                             | 01    |
|        | j) Keyword used to define integer values in Verilog.                                                                                                                                                                                                                                                                                                                                                                                                                                   | 01    |
|        | k) The keyword wire is used to represent _____                                                                                                                                                                                                                                                                                                                                                                                                                                         | 01    |
|        | l) What is the difference in verilog representation between unsigned binary and 2s-complement signed binary?                                                                                                                                                                                                                                                                                                                                                                           | 01    |
|        | m) What are floating point numbers?                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 01    |
|        | n) How many bits can be stored in one SR flip-flop?                                                                                                                                                                                                                                                                                                                                                                                                                                    | 01    |
|        | o) List the difference between latches and flip-flop.                                                                                                                                                                                                                                                                                                                                                                                                                                  | 01    |
|        | p) Write a Verilog always block for a simple rising-edge-triggered register.                                                                                                                                                                                                                                                                                                                                                                                                           | 01    |
|        | q) What is a decade counter?                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 01    |
|        | r) Write abbreviation for FPGA.                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 01    |
|        | s) What is the difference between RAM and ROM?                                                                                                                                                                                                                                                                                                                                                                                                                                         | 01    |
|        | t) What is the capacity in bits of a memory with 4096 locations, each of 24 bits?                                                                                                                                                                                                                                                                                                                                                                                                      | 01    |
| 2      | a) Suppose a factory has two vats, only one of which is used at a time. The liquid in the vats to be at right temperature, between 25° C and 30° C. Each vat has two temperature sensors indicating whether the temperature is above 25° C and above 30° C respectively. The vats also have low level sensors. Design a circuit of gates to activate the buzzer when the temperature is too high or too low or the level of vat is too low. Also develop a verilog model for the same. | 08    |
|        | b) With flowchart, discuss about the digital design methodology used in IC industry.                                                                                                                                                                                                                                                                                                                                                                                                   | 08    |



- 3 a) Design an encoder to use in a domestic burglar alarm that has sensors from each of the eight zones. Each sensor signal is 1, when intrusion is detected in that zone, 0 otherwise. Write a verilog code for this encoder. Also consider the priority such that zone 1 having highest priority and zone 8 having lowest. 08
- b) Develop a verilog module for the following Boolean expression. 04  
 $y = (A+B.C) + (DC)$
- c) Develop a verilog module for the 3 bit 2 to 1 multiplexer. 04
- 4 a) Develop a verilog model of a code convertor to convert the 4 - bit gray code to a 4 - bit unsigned binary integer. 08
- b) Draw and explain a circuit composed of a gate that implements the 4-bit wide carry-look ahead generator. 08
- 5 a) Design a circuit for modulo 10 counter and develop a verilog code for the decade counter. 08
- b) Develop a schematic for a 6 bit register, constructed from D-flip flops, that updates the stored value on every clock cycle. 08
- OR
- 6 a) Develop a Verilog model for negative-edge-triggered flip-flop with clock enable, negative-logic asynchronous preset and clear, and both active-high and active-low outputs. It is illegal for both preset and clear to be active together. 08
- b) Discuss the operation of shift register with neat block diagram. 08
- 7 a) Test whether there is an error in ECC word 110111000110 and if so correct it. 08
- b) Describe synchronous Static RAM with timing for write and read operations. 08
- OR
- 8 a) Design 64X8 bit composite memory using 16K X 8 bit memory component. 08
- b) Explain different types of memory. 08



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## DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi)

### UG Semester End Examination, April May 2017

Course: Digital System Design Using Verilog

Code: TE43

Maximum marks: 100

Duration: 3 hours

**Answer five full Questions. All questions carry equal marks**

- |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Marks |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| 1      a    With neat timing diagram of a D - FF, Define Setup time, Hold Time and Clock to Q time.                                                                                                                                                                                                                                                                                                                                                                                                                         | 06    |
| b    Brief out noise margin constraints pertaining to digital ICs                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 04    |
| c    Explain the design methodology process involved in digital ICs with a neat flowchart.                                                                                                                                                                                                                                                                                                                                                                                                                                  | 10    |
| <b>(OR)</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |       |
| 2      a    Bring out the important aspects of the following parameters involved in real world circuits i) Wire delays ii) Propagation delay iii) Area and Packaging.                                                                                                                                                                                                                                                                                                                                                       | 08    |
| b    Illustrate Behavioral description, data flow description and structural description styles with aid of appropriate examples in Digital ICs manufacturing.                                                                                                                                                                                                                                                                                                                                                              | 12    |
| 3      a    With circuit diagram, write about parity tree for generating and checking even parity for an 8 - bit code word.                                                                                                                                                                                                                                                                                                                                                                                                 | 10    |
| b    Develop a verilog module for the n - bit 2 to 1 multiplexer.                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 04    |
| c    Develop a verilog model for a combinational circuit that implements the following three Boolean equations, representing part of the control logic for an air conditioner: <ul style="list-style-type: none"> <li>• Heater_on = temp_low . auto_temp + manual_heat</li> <li>• Cooler_on = temp_high . auto_temp + manual_heat</li> <li>• Fan_on = Heater_on + Cooler_on + manual_fan</li> </ul>                                                                                                                         | 06    |
| <b>(OR)</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |       |
| 4      a    Develop a test bench model for the light_controller_and_enable module for the traffic light control circuit. Verify the conditions that, when the enable input is 1, the output is the same as the light input, and when the enable input is 0, all light output are inactive.                                                                                                                                                                                                                                  | 10    |
| b    Briefly write about one - hot code with its advantages. Assume that the one hot code for the traffic light controller is represented using a 3-element vector with element 1 corresponding to red, 2 to yellow and 3 to green. Develop a verilog model for a light controller that has an encoded input, an encoded output, and a single-bit input that enables the lights. When the enable input is 0, the encoded output is the same as the encoded input. When the enable input is 1, all bits of the output are 0. | 06    |
| c    Develop a verilog model for the Boolean expression $f = (a.b) + (b.c)$                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 04    |

- 5 a Analyze with examples, the addition of signed integers and the importance of overflow and underflow concept. Also Represent Overflow concept in verilog. 10  
b Design a Magnitude comparator to test for lesser than inequality. Also develop a verilog code for the above. 10

(OR)

- |   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |    |
|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 6 | a Develop a verification test bench for the adder/Subtractor that compares the result of addition or subtraction performed on the values of type integer.<br>b Explain fast - carry chain adder. And also discuss its advantages over ripple carry adder.                                                                                                                                                                                                                                                                                                                                                                                                                          | 10 |
| 7 | a Develop a Verilog model for a pipelined circuit that computes the average of corresponding values in three streams of input values, a, b and c. The pipeline consists of three stages: the first stage sums values of a and b and saves the value of c; the second stage adds on the saved value of c; and the third stage divides by three. The inputs and output are all signed fixed-point numbers indexed from 5 down to -8.<br>b Develop a Verilog model for negative-edge-triggered flip-flop with clock enable, negative-logic asynchronous preset and clear, and both active-high and active-low outputs. It is illegal for both preset and clear to be active together. | 10 |

(OR)

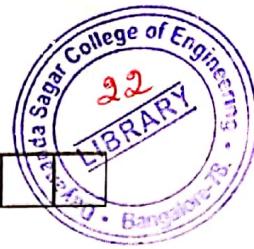
- |   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |    |
|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 8 | a Design circuits for modulo 10 counter and develop a verilog code for the decade counter.                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 10 |
|   | b Develop a data path to perform a complex multiplication of two complex numbers. The operands and product are all in Cartesian form. The real and imaginary parts of the operands are represented as signed fixed point numbers with 4 pre-binary-point and 12 post-binary-point bits. The real and imaginary parts of the product are similarly represented, but with 8 pre binary-point and 24 post-binary-point bits. The complex multiplier is subject to constraints that strongly limit the circuit area. Develop a Verilog model for the complex multiplier. | 10 |
| 9 | a Design 32K X 8 bit composite memory using 8K X 8 bit memory component.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 10 |
|   | b i). Compute the 12-bit ECC word corresponding to the 8-bit data word 01100101.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 10 |
|   | ii). Test whether there is an error in ECC word 000111000100 and if so correct it.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 10 |

(OR)

- 10 a Explain the internal organization of a Field Programmable Gate Arrays (FPGAs) with a neat diagram. 10  
b Explain Asynchronous Static RAM with timing for write and read operations. 10

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## DAYANANDA SAGAR COLLEGE OF ENGINEERING

*(An Autonomous Institute Affiliated to VTU, Belagavi)*

### UG Make-up Examination, June 2017

Course: Digital System Design Using Verilog

Code: TE43

Maximum marks: 100

Duration: 3 hours

**Answer five full Questions. All questions carry equal marks**

- |   |                                                                                                                                                                                                                                                                                                                                    |             |
|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 1 | a Develop a sequential circuit that has a single data input signal S and produce an output Y. The output is 1 whenever S has the same value over three successive clock cycles, and 0 otherwise. Assume that the value of S for a given clock cycle is defined at the time of the rising clock edge at the end of the clock cycle. | Marks<br>10 |
|   | b Explain the following constraints imposed in Real World Circuits                                                                                                                                                                                                                                                                 |             |
|   | i) Capacitive load and propagation delay   ii) Wire Delay.                                                                                                                                                                                                                                                                         | 10          |

**(OR)**

- |   |                                                                                                                                                                                                                                                                                                                     |             |
|---|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 2 | a Explain with flow chart the design methodology used in IC industry.                                                                                                                                                                                                                                               | Marks<br>10 |
|   | b Suppose a factory has two vats, only one of which is used at a time. The liquid in the vats to be at the right temperature, between 25°C and above 30° C, respectively. The vats also have low level sensors. Design a circuit of gates to activate the buzzer as required. Write Verilog model also.             | 10          |
| 3 | a Design an encoder to use in a domestic burglar alarm that has sensors from each of the eight zones. Each sensors signal is 1, when intrusion is detected in that zone, 0 otherwise. Write Verilog code for this encoder. Also consider the priority such that zone 1 having highest priority and 8 having lowest. | 10          |
|   | b Develop a Verilog model for a 7-segment decoder. Include an additional input, blank that overrides the BCD input and causes all segments not to lit                                                                                                                                                               | 10          |

**(OR)**

- |   |                                                                                                                                                                                                                                                                                        |             |
|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 4 | a Develop a Verilog model for 3-bit 2 -to-1 multiplexer.                                                                                                                                                                                                                               | Marks<br>05 |
|   | b Develop a Verilog model for a decoder for use in the ink jet printer. The decoder has three input bits representing the choice of color cartridges and six output bits, one to select each cartridge. And cartridges are black, cyan, magenta, yellow, light cyan and light magenta. | 06          |
|   | c Design a test bench model for the light_controller_and_enable for the traffic light control circuit using task. Verify the conditions that, when the enable input is 1, the output is the same as the light input, and when the eable input is 0, all light outputs are inactive.    | 09          |

- 5 a Design a magnitude comparator to test for greater than inequality. Also develop a Verilog code for the same. 10  
 b Draw and explain a circuit composed of a gate that implements the 4 bit wide carry look ahead generator. 10
- (OR)
- 6 a Develop a verilog model of a code converter to convert the 4-bit gray code to a 4 bit unsigned binary integer. 10  
 b Explain the fixed point numbers and its Verilog representation with examples. Convert signed fixed point binary number 11110.1011 to decimal fraction number 10
- 7 a Design a circuit that counts 16 clock cycles and produce a control signal, ctrl that is 1 during every eighth and twelfth cycle. 10  
 b Develop a Verilog model for a pipelined circuit that computes the average of corresponding values in three streams of input values, a, b and c. The pipeline consists of three stages: the first stage sums values of a and b and saves the value of c; the second stage adds on the saved value of c; and the third stage divides by three. The inputs and output are all signed fixed-point numbers indexed from 5 down to -8. 10
- (OR)
- 8 a Develop a Verilog model for an interval timer that has clock, load and data input ports and a terminal-count output port. The timer must be able to count intervals of up to 1000 clock cycles. The interval timer reloads the previously loaded value rather than wrapping around to the largest count value. 10  
 b Describe Finite State Machines (FSM) with schematic representation. 10
- 9 a Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001. 10  
 b What is the difference between RAM and ROM? Explain Asynchronous Static RAM with timing for write and read operations. 05  
 c Design 64X8 bit composite memory using 16K X 8 bit memory component. 05
- (OR)
- 10 a Design a circuit that computes the function  $y = c_i \times x^2$ , where  $x$  is a binary-coded input value and  $c_i$  is a coefficient stored in a flow-through SSRAM.  $x$ ,  $c_i$  and  $y$  are all signed fixed-point values with 8 pre-binary-point and 12 post-binary-point bits. The index  $i$  is also an input to the circuit, encoded as a 12-bit unsigned integer. Values for  $x$  and  $i$  arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using a single multiplier to multiply  $c_i$  by  $x$  and then by  $x$  again. Develop a verilog model. 10  
 b Explain the internal organization of a Field Programmable Gate Arrays (FPGAs) with a neat diagram. 10



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## DAYANANDA SAGAR COLLEGE OF ENGINEERING

*(An Autonomous Institute Affiliated to VTU, Belagavi)*

### UG Supplementary Examination July - August 2017

**Course: Digital System Design Verilog**

**Code: TE43**

Maximum marks: 100

Duration: 3 hours

**Answer five full Questions. All questions carry equal marks**

- |   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Marks          |
|---|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 1 | a Suppose a factory has two vats, only one of which is used at a time. The liquid in the vats to be at right temperature, between 25° C and 30° C. Each vat have two temperature sensors indicating whether the temperature is above 25° C and above 30° C respectively. The vats also have low level sensors. Design a circuit of gates to activate the buzzer when the temperature is too high or too low or the level of vat is too low. Also write a Verilog model.<br>b Explain the following constraints imposed in Real World Circuits.<br>i). Capacitive Load and Propagation delay<br>ii). Area and Packing                                                                                                                                                                                         | 10             |
|   | (OR)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                |
| 2 | a Explain Dataflow and Behavioral description style with an example for each.<br>b With neat timing diagram of a D - FF, Define Setup time, Hold Time and Clock to Output time.<br>c Develop a sequential circuit with a single data input A and single data output Y. The output is 0 whenever S has the same value over three successful clock cycles and 1 otherwise. Assume that the value of S for a given clock cycle is defined at the time of the rising clock edge at the end of the clock cycle.                                                                                                                                                                                                                                                                                                   | 05<br>05<br>10 |
| 3 | a What is one hot code? And explain the advantages of it. Assume that the one hot code for the traffic light controller is represented using a 3-element vector with element 1 corresponding to red, 2 to yellow and 3 to green. Develop a Verilog model for a light controller that has an encoded input, an encoded output, and a single-bit input that enables the lights. When the enable input is 1, the encoded output is the same as the encoded input. When the enable input is 0, all bits of the output are 0.<br>b Develop a test bench model for the light_controller_and_enable module for the traffic light control circuit. Verify the conditions that, when the enable input is 1, the output is the same as the light input, and when the enable input is 0, all light output are inactive. | 10<br>10       |
|   | (OR)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                |
| 4 | a Develop a Verilog module and a circuit for the 3 bit 2 to 1 multiplexer<br>b Write a Verilog model for a combinational circuit that implements the following three Boolean equations, representing part of the control logic for air conditioner:<br>$Heater\_on = temp\_low \cdot auto\_temp + manual\_heat$<br>$Cooler\_on = temp\_high \cdot auto\_temp + manual\_heat$<br>$fan\_on = heater\_on + cooler\_on + manual\_fan$<br>c Design an encoder to use in a domestic burglar alarm that has sensors from each of the eight zones. Each sensor signal is 1, when intrusion is detected in that zone, 0 otherwise.                                                                                                                                                                                    | 06<br>08<br>06 |

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 5           | a Analyze with examples, the addition of signed integers and the importance of overflow and underflow concept.<br>b Develop a verification test bench for the adder/Subtractor that compares the result of addition or subtraction performed on the values of type integer.<br>c Develop a Verilog model of a 4 to 1 multiplexer that selects among four unsigned 6-bit integers.                                                                                                                                                                                                                                                                                                                                      | 05<br>10<br>05 |
| <b>(OR)</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                |
| 6           | a Explain fast-carry-chain adder. And also discuss the advantages over ripple carry adder.<br>b Design a Magnitude comparator to test for greater than inequality. Also develop a Verilog code for the same.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 10<br>10       |
| 7           | a Describe Finite State Machines (FSM) with schematic representation.<br>b Develop a Verilog model for a pipelined circuit that computes the average of corresponding values in three streams of input values, a, b and c. The pipeline consists of three stages: the first stage sums values of a and b and saves the value of c; the second stage adds on the saved value of c; and the third stage divides by three. The inputs and output are all signed fixed-point numbers indexed from 5 down to -8.<br>c Design and explain a ripple counter with timing diagram.                                                                                                                                              | 06<br>08<br>06 |
| <b>(OR)</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                |
| 8           | a Develop a Verilog model for an accumulator that calculates the sum of a sequence of fixed-point numbers. Each input number is signed with 4 pre-binary-point and 12 post-binary-point bits. The accumulated sum has 8 pre-binary-point and 12 post-binary-point bits. A new number arrives at the input during a clock cycle when the data_en control input is 1. The accumulated sum is cleared to 0 when the reset control input is 1. Both control inputs are synchronous.<br>b Explain structure of ripple counter with timing diagram.<br>c Design a circuit that counts 16 clock cycles and produces a control signal, ctrl that is 1 during every eighth and twelfth cycle. Develop a Verilog model.          | 05<br>10<br>05 |
| 9           | a What is the difference between RAM and ROM? Explain Asynchronous Static RAM with timing for write and read operations.<br>b Design 64X8 bit composite memory using 16K X 8 bit memory component.<br>c Explain the internal organization of a Field Programmable Gate Arrays (FPGAs) with a neat diagram.                                                                                                                                                                                                                                                                                                                                                                                                             | 08<br>06<br>06 |
| <b>(OR)</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                |
| 10          | a Test whether there is an error in ECC word 000111000100 and if so correct it.<br>b Design a circuit that computes the function $y = c_i \times x^2$ , where x is a binary-coded input value and $c_i$ is a coefficient stored in a flow-through SSRAM. x, $c_i$ and y are all signed fixed-point values with 8 pre binary-point and 12 post-binary-point bits. The index i is also an input to the circuit, encoded as a 12-bit unsigned integer. Values for x and i arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using a single multiplier to multiply $c_i$ by x and then by x again. Develop a Verilog model.<br>c Explain different memory types. | 04<br>10<br>06 |

**DAYANANDA SAGAR COLLEGE OF ENGINEERING**(An Autonomous Institute Affiliated to VTU, Belagavi)  
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560078**UG Make-Up Examination, February 2019**

Course: **Hardware Description Language**  
 Course Code: **EC55**  
 Semester: **V**

Maximum marks: **100**  
 Duration: **3 hours**

- Note:** i). Question ONE (a to t) has to be answered from pages 5 to 7 only.  
 ii). Question 1 to 4 is compulsory.  
 iii). Any missing data should be suitably assumed.

| Q. No. |                                                                                                                                                                              | Marks |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| 1      | a) In VHDL, the user can define their own data type by using the predefined word _____.                                                                                      | 01    |
|        | b) In composite data type of VHDL, the record type comprises the elements of _____ data types.                                                                               | 01    |
|        | c) If A= 3'b111 and B= 3'b'010, then the result of A%B will be<br>(i) 3'b011      (ii) 3'b001      (iii) 3'b111      (iv) None of above                                      | 01    |
|        | d) How many values are support by a package Std_logic_1164.all?                                                                                                              | 01    |
|        | e) Which type of Assignment Statements will be used in Data Flow and Behavioural description VHDL?                                                                           | 01    |
|        | f) How the Signal acts within a Process and outside the Process?                                                                                                             | 01    |
|        | g) 'Repeat' sequential statement is used in VHDL. (i)True      (ii)False                                                                                                     | 01    |
|        | h) In a Verilog behavioural description, the statements are executed _____<br>(i)Concurrently (ii)Sequential (iii)Both (a) and (b) (iv)None of the above                     | 01    |
|        | i) VHDL structural description recognizes all gates. (i) True (ii) False                                                                                                     | 01    |
|        | j) Structural description simulates the system by describing its _____.                                                                                                      | 01    |
|        | k) The order of appearance of statements in structural Verilog module is _____.                                                                                              | 01    |
|        | l) What is the difference between Verilog function and Task?                                                                                                                 | 01    |
|        | m) The net-list is generated _____ synthesizing VHDL code.<br>(i) Before (ii) At the time of (during) (iii)After (iv)None of the above                                       | 01    |
|        | n) The only loop supported for synthesis is _____                                                                                                                            | 01    |
|        | o) Synthesis mapping of the case statement is very similar to mapping the _____ statement.                                                                                   | 01    |
|        | p) _____ provides Verilog Synthesis information on the inputs and outputs and their types.                                                                                   | 01    |
|        | q) What is the advantage of flash memory?                                                                                                                                    | 01    |
|        | r) In a Mealy sequential network, _____ part can be realized using a ROM.                                                                                                    | 01    |
|        | s) What is the difference between a PLA and a PAL?                                                                                                                           | 01    |
|        | t) If the input bit sequence 01100111, then the RZ (return-to-zero) code is _____.                                                                                           | 01    |
| 2      | a) List all the Verilog data types and explain any two in detail.                                                                                                            | 06    |
|        | b) Explain how to assign a delay to the signal assignment statement? Write a HDL code for 2x1 multiplexer with active low using signal declaration and assignment statements | 10    |



including delay.

- 3 a) Explain Booth algorithm with flow chart and write Verilog code. Also Multiply  $3 * -6$  (Multiplier X = -6 and Multiplicand Y = 3) using Booth algorithm. 12  
b) Explain the general formats of FOR loop and WHILE loop statements in VHDL. 04
- 4 a) Write VHDL and Verilog code using function to find the largest of the two signed numbers. 10  
b) Explain a 3-bit ripple carry adder with VHDL structural description. 06
- 5 a) Sketch the flowchart for the steps involved in synthesis process flow. 06  
b) Elaborate the mapping of else if statement by taking the following example. 10  
The system with BP (input) and ADH (output) are of natural type ranging 0 to 7 and 0 to 15 respectively. Assume that if BP is less than or equal to 1, then ADH = 15 or if BP is greater than or equal to 4 then ADH is 0 otherwise  $ADH = BP * (-5) + 25$ . Also, write structural code in Verilog using gate level diagram.

**OR**

- 6 a) Design VHDL code for signal assignment statement  $Y = 2 * X + 3$  with 2-bit input. Show the synthesized logic symbol and gate level diagram. Write structural code in Verilog using gate level diagram. 12  
b) Show the synthesis information extracted from the example given below: 04
- ```
package day is
    type weekdays is (Mon, Tue, Wed, Thru, Fri, Sat, Sun);
    end day;
    use work.day;
    entity temperature is
        port (Day1: in weekdays;
              temp1: out integer range -100 to 100);
    end temperature;
```

- 7 a) Design a BCD to Ex-3 code converter using D flip-flops. 12
b) Implement the following function using PLA,
 $F1(a,b,c) = \sum m(0,3,5,6,7)$
 $F2(a,b,c) = \sum m(1,2,3,5,7)$

OR

- 8 a) Write a note on, 08
(i) Read only Memory (ROM)
(ii) Programmable Array Logic (PAL)
b) Design of a Moore Sequential network for NRZ to Manchester Conversion. 08

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DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi)

UG Semester End Examination, May 2018**Course: Fundamentals of HDL****Code: EI45****Maximum marks: 100****Duration: 3 hours****Answer five full Questions. All questions carry equal marks**

- | | | Marks |
|---|--|----------|
| 1 | a What is HDL? Discuss the different types of descriptions available in HDL.
b Discuss the structure of VHDL and Verilog giving example for each. | 10
10 |
| | (OR) | |
| 2 | a Discuss the data types used in VHDL and Verilog.
b Explain the operators in VHDL and Verilog. | 10
10 |
| 3 | a Write a VHDL code in data flow description for a 3-bit carry look ahead adder.
b Write a Verilog code in data flow description for a 2:1 multiplexer with active low enable, with the help of truth table and logic diagram. | 10
10 |
| | (OR) | |
| 4 | a Write a VHDL code for 2*2 unsigned combinational array multiplier using dataflow description.
b Write a Verilog code in data flow description for a 2-bit comparator, with the help of truth table and logic diagram. | 10
10 |
| 5 | a Explain D-latch with the help of its truth table and gate level implementation. Write Verilog code in data flow description for D-latch.
b Using Booth algorithm find the product of two unsigned 4 bit numbers -5 and 3. Write a Verilog code using Behavioral style of description. | 10
10 |
| | (OR) | |
| 6 | a Write behavioral description of a Positive Edge triggered JK Flip-Flop using case statement in VHDL and Verilog.
b What is binding? Explain how binding between entity and architecture is done in VHDL and also binding between library and module in VHDL. | 10
10 |
| 7 | a What is meant by synthesis? List and explain the steps involved in synthesis.
b Write Verilog code for signal assignment statement $y = 2*x+3$. Show the synthesized logic symbol and gate level diagram. | 10
10 |
| | (OR) | |

- 8 a Define synthesis. Design a gate level synthesis and write VHDL description for the information given below 10

Inputs		Outputs
a	b	z
00 (cent)	0-7	$z = \text{temperature}$
01 (offset)	0-7	$z = \text{temperature} + 4$
10 (half)	0-7	$z = \text{temperature}/2$
11	xx	$z = 15$
xx	>7	$z = 15$

- b Synthesize the VHDL code given below 10

```
entity Ex is
    Port (a: in natural range 0 to 7;
          Y: out integer range 0 to 15);
end Ex;
```

```
architecture Ex1 of Ex is
begin
    process(a)
        variable temp: integer range 0 to 15;
    begin
        if (a<3) then temp:=15;
        elsif (a>=5) then temp:=0;
        else
            temp:= a * (-5) + 25;
        end if;
    end process;
end ex1;
```

- 9 a Explain Procedures and tasks. Write a VHDL description of full adder using Procedure. b Write the procedure for converting an unsigned binary to an integer. 10 (OR)

- 10 a With the help of a block diagram explain mixed language description of half adder. b What is a function? Write the code for finding greater of two signed numbers in Verilog using function. 10 10



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DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi)

UG Makeup Examination, June/July 2018

Course: Fundamental of HDL

Code: EI45

Maximum marks: 100

Duration: 3 hours

Answer five full Questions. All questions carry equal marks

- | 1 | Marks |
|---|-------|
| a Discuss the various types of descriptions available in HDL. | 10 |
| b Distinguish between VHDL and Verilog Languages. | 05 |
| c Explain the logical operators in Verilog Language. | 05 |
| (OR) | |
| 2 a Discuss the VHDL data types with examples each. | 12 |
| b Discuss the following: | 08 |
| i. Std_logic_vector | |
| ii. Bit type | |
| iii. Boolean type | |
| iv. integer type | |
| 3 a Explain the structure of VHDL and Verilog module and give example of half adder circuit. | 10 |
| b Write a VHDL code for 2*2 unsigned combinational array multiplier using dataflow description. | 10 |
| (OR) | |
| 4 a Write a VHDL code in data flow description for a 3-bit carry look ahead adder. | 10 |
| b Write a VHDL code in data flow description for a 2:1 multiplexer with active low enable, with the help of truth table and logic diagram. | 10 |
| 5 a Distinguish between signal assignment and variable assignment statements in VHDL. | 06 |
| b Write Verilog code in behavioral description for calculating the factorial of positive integers. | 06 |
| c Write behavioral description of a Positive Edge triggered JK Flip-Flop using case statement in VHDL. | 08 |
| (OR) | |
| 6 a What is binding? Explain how binding between entity and architecture is done in VHDL and also binding between library and module in VHDL. | 10 |
| b Using Booth algorithm find the product of two unsigned 4 bit numbers -3 and 5. Write a Verilog code using Behavioral style of description. | 10 |

- 7 a What is meant by synthesis? List and explain the steps involved in synthesis. 10
 b Write a VHDL or Verilog code for the following signal assignment statement $y = 2 * a + 5$ for an entity with one input 'a' of 3-bits and one output 'y' of 4-bits. Show the mapping of this signal assignment to gate level.

(OR)

- 8 a Design a gate level synthesis and write VHDL description for the information given below 10

Inputs		Outputs
A	b	Z
00(cent)	0-7	$z = \text{temperature}$
01 (offset)	0-7	$z = \text{temperature} + 4$
10(half)	0-7	$z = \text{temperature}/2$
11	xx	$z = 15$
Xx	>7	$z = 15$

- b Write Verilog code for signal assignment statement $y = 2*x+3$. Show the synthesized logic symbol and gate level diagram. 10

- 9 a What is the need of procedure and task? Explain the declaration and body of the task. 06
 b Write a code to convert the fraction binary (4-bit) to real using procedure.
 c Write a VHDL description of a full adder using procedure. 07 07

(OR)

- 10 a Why is a mixed type description needed? Write the VHDL code to find largest element in an array. 10
 b Write a mixed language description of a JK master slave flip-flop with clear input. 10



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DAYANANDA SAGAR COLLEGE OF ENGINEERING*(An Autonomous Institute Affiliated to VTU, Belagavi)***UG Semester End Examination, May 2018****Course: Digital system Design using Verilog****Code: TE43****Maximum marks: 100****Duration: 3 hours****Answer five full Questions. All questions carry equal marks**

- | | | |
|---|--|-------------------------|
| 1 | a Explain Structural description style and Data flow style with an example for each.
b Develop a sequential circuit with a single data input S and single data output Y. The output is 1 whenever S has the same value over three successful clock cycles and 0 otherwise. Assume that the value of S for a given clock cycle is defined at the time of the rising clock edge at the end of the clock cycle.
c Explain with flowchart, the design methodology used in IC industry
(OR) | Marks
06
08
06 |
| 2 | a Explain the following constraints imposed in Real World Circuits.
i) Noise Margin ii) Static Load Levels
b Define Setup time, Hold Time and Clock to Output time.
c Write about the Area and Packaging involved in Real World Circuits. | 10
06
04 |
| 3 | a Design an encoder to use in a domestic burglar alarm that has sensors from each of the eight zones. Each sensor signal is 1, when intrusion is detected in that zone, 0 otherwise. Write a verilog code for this encoder. Also consider the priority such that zone 1 having highest priority and zone 8 having lowest.
b Explain bit error in digital systems.
c Develop a verilog module for the 3 bit 2 to 1 multiplexer.
(OR) | 10
05
05 |
| 4 | a Develop a verilog model for a 7 – segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to lit.
b With circuit diagram, write about parity tree for generating and checking even parity for a 12 – bit code word.
c Develop a verilog model for the Boolean expression $f = (x \cdot y + z) \cdot (y \cdot z)$. | 08
06
06 |
| 5 | a Explain the methods for adapting adder to perform addition and subtraction of unsigned integers. Also develop a Verilog code for the same.
b Develop a verilog model of a code convertor to convert the 4 – bit gray code to a 4 – bit unsigned binary integer.
c Explain the Floating-point number representation.
(OR) | 10
06
04 |
| 6 | a Draw and explain a circuit composed of a gate that implements the 4-bit wide carry-lookahead generator. | 10 |

- 22/01/2023
- | | | |
|----|--|----|
| | b Explain fast-carry-chain adder. And also discuss the advantages over ripple carry adder. | 10 |
| 7 | a Develop a Verilog model for negative-edge-triggered flip-flop with clock enable, negative-logic asynchronous preset and clear, and both active-high and active-low outputs. It is illegal for both preset and clear to be active together. | 06 |
| | b Design a circuit for modulo 10 counter and develop a verilog code for the decade counter. | 08 |
| | c A digital alarm clock needs to generate a periodic signal at a frequency of approximately 500Hz to drive the speaker for the alarm tone. Use a counter to divide the system's master clock signal, with a frequency of 1 MHz, to derive the alarm tone. | 06 |
| | (OR) | |
| 8 | a Develop a data path to perform a complex multiplication of two complex numbers. The operands and product are all in Cartesian form. The real and imaginary parts of the operands are represented as signed fixed point numbers with 4 pre-binary-point and 12 post-binary-point bits. The real and imaginary parts of the product are similarly represented, but with 8 pre-binary point and 24 post-binary-point bits. The complex multiplier is subject to constraints that strongly limit the circuit area. Develop a Verilog model for the complex multiplier. | 10 |
| | b Explain structure of ripple counter with timing diagram. | 10 |
| 9 | a Explain the internal organization of a Field Programmable Gate Arrays (FPGAs) with a neat diagram. | 07 |
| | b Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001 | 06 |
| | c Explain different memory types. | 07 |
| | (OR) | |
| 10 | a What is meant by the terms volatile and nonvolatile? Explain flow through SRAM with timing for write and read operations. | 08 |
| | b Test whether there is an error in ECC word 000111000100 and if so correct it. | 06 |
| | c Design 64X8 bit composite memory using 16K X 8 bit memory component. | 06 |

USN **DAYANANDA SAGAR COLLEGE OF ENGINEERING***(An Autonomous Institute Affiliated to VTU, Belagavi)***UG Makeup Examination, June 2018****Course: Digital Systems design using Verilog****Code: TE43****Maximum marks: 100****Duration: 3 hours****Answer five full Questions. All questions carry equal marks**

- | | | |
|---|---|----------------|
| 1 | a Describe the digital design methodology used in IC industry with appropriate flow chart.
b Describe the different types of descriptions in Verilog with suitable example.
(OR) | Marks 10 |
| 2 | a Explain abstraction with example.
b Develop a verilog model to devise a one hot code to represent days of the week.
c What are sequential circuits? Develop a sequential circuit that has a single data input signal, S, and produces an output Y. the output is 1 whenever S has the same value over three successive clock cycles, and 0 otherwise. Assume that the value of S for a given clock cycle is defined at the time of the rising clock edge at the end of the clock cycle. | 04
06
10 |
| 3 | a Develop a verilog model for 4_1 Mux.
b Develop a verilog model for a 7 - segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to light.
c Explain the concept of parity error checking. Discuss the parity trees for generating and checking even parity to augment 8-bit code.
(OR) | 04
08
08 |
| 4 | a Develop a verilog code for the burglar alarm to be a priority encoder, with zone1 having highest priority, down to zone 8 having lowest priority.
b Develop a test bench model for the light_controller_and_enable module for the traffic light control circuit. Verify the conditions that, when the enable input is 1, the output is the same as the light input, and when the enable input is 0, all light output are inactive.
c Why is it better to use logic low level than logic high level? | 07
10
03 |
| 5 | a Design a Magnitude comparator to test for lesser than inequality. Also develop a verilog code for the above.
b Implement a structural verilog model for a 4-bit carry look ahead adder.
(OR) | 10
10 |
| 6 | a Analyze with examples, the addition of signed integers and the importance of overflow and underflow concept. Also Represent Overflow concept in verilog.
b Develop verilog model of a code converter to convert 4-bit gray code to 4-bit unsigned binary integer. | 10
10 |

- Date: 02/07/2024
- | | | |
|----|--|----|
| 7 | a Design a circuit that counts 16 clock cycles and produces control signal,ctrl, that is 1 during every 8 th and 12 th cycles. Develop a verilog model for the same. | 10 |
| | b Develop a verilog code for a positive edge triggered D flip flop with clock enable positive logic asynchronous preset and clear and both active high and active low outputs. It is illegal for both preset and clear to be active together. | 10 |
| | (OR) | |
| 8 | a Design a circuit and develop a verilog code for BCD counter. | 06 |
| | b Develop a datapath to perform a complex multiplication of two complex numbers. The operands and product are all in Cartesian form. The real and imaginary parts of the operands are represented as signed fixed point numbers with 4 pre-binary-point and 12 post-binary-point bits. The real and imaginary parts of the product are similarly represented, but with 8 prebinary-point and 24 post-binary-point bits. The complex multiplier is subject to constraints that strongly limit the circuit area. Develop a Verilog model for the complex multiplier. | 10 |
| | c Develop a verilog model for SR latch. | 04 |
| 9 | a Design 64K X 8 bit composite memory using 16K X 8 bit memory component. | 06 |
| | b Differentiate between RAM and ROM? Explain Asynchronous Static RAM with timing for write and read operations. | 10 |
| | c Test whether there is an error in ECC word 000111000100 and if so correct it. | 04 |
| | (OR) | |
| 10 | a Define the terms volatile and nonvolatile? Explain flow through SSRAM with timing for write and read operations. | 10 |
| | b Explain the internal organization of a Field Programmable Gate Arrays (FPGAs) with a neat diagram. | 10 |

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DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi)

UG Semester End Examination, May 2018**Course: Digital System Design Using Verilog**

Maximum marks: 100

Code: EC661

Duration: 3 hours

**Answer five full Questions. All questions carry equal marks**

- a A combinational logic circuit has four inputs (A, B, C, and D) and one output Z. The output is 1 iff the input has three consecutive 0's or three consecutive 1's. For example, if A = 1, B = 0, C = 0, and D = 0, then Z = 1 (Derive truth table). Design the circuit and write the verilog code for same. Marks 07
- b Develop a sequential circuit with a single data input S and a single data output Y. The output is 1 when the input value in the current clock cycle is same from the input value in the previous clock cycle. 05
- c Develop a verilog model for the 5-bit 2-to-1 multiplexer. 04
- d Suppose, for a family of logic components, V_{IL} is 0.6V and V_{IH} is 1.2V. What voltages are required for V_{OL} and V_{OH} to provide a noise margin of 0.2V. 04

(OR)

- a Suppose a factory has two vats, only one of which is used at a time. The liquid in the vat in use needs to be at the right temperature, between 23°C and 33°C. Each vat has two temperature sensors indicating whether the temperature is above 23°C and above 33°C, respectively. The vats also have low level sensors. The supervisor needs to be woken up by a buzzer when the temperature is too high or too low or the vat level is too low. He has a switch to select which vat is in use. Design a circuit of gates to activate the buzzer as required. Develop the Verilog code for the same 10
- b Design an encoder to use in a domestic burglar alarm that has sensors from each of the eight zones. Each sensor signal is '1', when intrusion is detected in that zone, '0' otherwise. Write a Verilog code for this encoder, considering the priority such that zone 1 having the highest priority and zone 8 having the least 06
- c The alarm will ring iff the alarm switch is turned on and the door is not closed, or it is after 6 P.M. and the window is not closed. Develop the Verilog code for same. 04

- a With necessary equations show two alternate implementations of Fast carry- Chain full adder cells used in adder. 06
- b Resize the 2s-complement numbers 01110001 and 11110011 to 12 bits and 6 bits. In each case, does the result correctly represent the same value as the original. 04
- c i) Express the number 40.15625 in floating-point format with 8 bits of exponent and 23 bits of mantissa magnitude.
ii) What values are represented by the following bit vectors, interpreted in floating-point format with 4 bits of exponent and 11 bits of mantissa magnitude: 01000100000000000000. 06
- d What numbers are represented by the following signed 2s-complement fixed-point numbers, assuming the binary point is four places from the right: 00101100 and 111011. 04

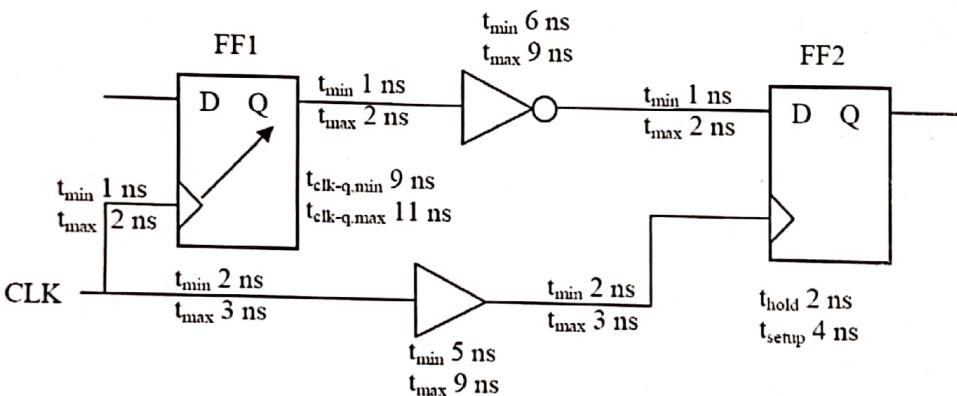
(OR)

- a Design a circuit that computes the function $y=c_i * x^2$, where x is a binary-coded input value and c_i is a coefficient stored in a flow-through SSRAM. x , c_i and y are all signed fixed point values with 8 pre-binary point and 12 post-binary point bits. The index i is also input to the circuit, encoded as a 12 bit-unsigned integer. Values for x and i arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using a single multiplier to multiply C_i by x and then by x again. Develop the verilog code for same. 10
- b Design a 256M X 16 bit memory using 256 M X 4 bit memory component. 05

- c Using the Hamming code, determine whether there is an error in each of the following ECC words, and if so, determine the corrected ECC word and the original data value. 05
 i) 110111000110 ii) 000110111000?
- 5 a Develop a Verilog model for a pipelined circuit that computes the average of corresponding values in three streams of input values, a, b and c. The pipeline consists of three stages: the first stage sums values of a and b and saves the value of c; the second stage adds on the saved value of c; and the third stage divides by five. The inputs and output are all signed fixed-point numbers indexed from 5 down to -8. 06
 b Design a circuit that counts 16 clock cycles and produces a control signal, "ctrl", that is '1', during every ninth and fourteenth cycle. Also, develop a verilog model for the same. 08
 c Describe Synchronous V/S Asynchronous Reset with an Example and RTL circuit for same. 06

(OR)

- 6 a A digital alarm clock needs to generate a periodic signal at a frequency of approximately 1024Hz to drive the speaker for the alarm tone. Use a counter to divide the system's master clock signal, with a frequency of 2 MHz, to derive the alarm tone. 05
 b For the circuit shown below. Find the Maximum clock frequency of the Circuit and also check is there any Set-up and Hold Time violation with necessary equations. 15



- 7 a Develop the Mealy and Moore type FSM for the sequence detector sequence shown below. The circuit has one input X and Output Z. Realize the circuit for Mealy type FSM. Develop the verilog code for same. 12

$$X = 0\ 0\ 1\ 1\ 0\ 1\ 1\ 0\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 0$$

$$Z = 0\ 0\ 0\ 0\ 0\ 1\ 0\ 0\ 0\ 0\ 0\ 1\ 0\ 1\ 0\ 0$$

- b Design a mealy State machine for the sequence shown below. The output Z should be 1 if the input sequence ends in either 010 or 1001, and Z should be 0 otherwise. 08

$$X = 0\ 0\ 1\ 0\ 1\ 0\ 0\ 1\ 0\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 0$$

↑ ↑ ↑ ↑ ↑ ↑ ↑

a b c d e f

$$Z = 0\ 0\ 0\ 1\ 0\ 1\ 0\ 1\ 1\ 0\ 0\ 0\ 1\ 0\ 1\ 0\ 0$$

(OR)

- 8 a Compare the design flow of ASIC and FPGA with flowchart and explain the same. 10
 b Differentiate between Mealy and Moore State Machines 04
 c Discuss guidelines for clocks and resets. 06

- | | | |
|---|--|----|
| 9 | a Design a 4-digit decimal counter with a 7-segment LED display: two 74LS390 dual decade counters, four 74LS47 BCD to 7-segment decoders, four 7-segment displays, plus any additional gates required. | 10 |
| b Discuss about: i) Programmable array logic, ii) Complex PLDs | | 10 |
| (OR) | | |
| 10 | a Illustrate the parameters related to FPGA Architecture. | 06 |
| b Discuss about abstractions for FPGA design with flow diagram. | | 07 |
| c Discuss the CLB in the 7 series FPGA. | | 07 |





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DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi)
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560078

UG Semester End Examination, December 2018/January 2019

Course: **DIGITAL SYSTEM DESIGN USING HDL** Maximum marks: 100
 Course Code: **ML561** Duration: 3 hours
 Semester: **V**

- Note:** i). Question ONE (a to t) has to be answered from pages 5 to 7 only.
 ii). Question 1 to 4 is compulsory.
 iii). Any missing data should be suitably assumed.

Q. No.		Marks
1	a ANSI stands for _____	01
	b In VHDL is Half_ADDER and half_adder are same _____	01
	c _____ port can be used for Input & Output in Verilog.	01
	d _____ predefined word wire with respect to Verilog data types.	01
	e How many architectures can be associated with an entity.	01
	f Find the value of the expression ~ (A and B) for A=1010, B= 1011	01
	g In VHDL _____ is a predefined operator that describes width of vector.	01
	h Define vector data type.	01
	i Define Behavioral Description.	01
	j _____ is mainly used for repetition of concurrent statement.	01
	k Write execution of IF as Latch in Verilog.	01
	l Component instantiation is done in which type of HDL description.	01
	m Z : out integer range -7 to 7 ; determine the numbers of outputs.	01
	n Number of steps in General synthesis.	01
	o _____ is the o/p of synthesis.	01
	p Signal and variable which will be updated first.	01
	q What is the uniqueness of Verilog in abstraction level.	01
	r If A= 4b 010x and B= 4b 1100 then result of A + B will be _____	01
	s If x = 4b 1011 then x << 2 is	01
	t In Verilog inout ports must be always _____	01
2	a Analyze full adder Design with respect to, behavioral and Data flow Description types of HDL Programming.	08
	b Explain Verilog Reduction Logical operators and VHDL Relational operators.	08



- | | | |
|-----------|--|----|
| 3 | a Explain the use of data type Vector with data flow description of D Latch in HDL. | 08 |
| | b Describe 2 bit magnitude Comparator and write data flow Description for its Boolean function in Verilog. | 08 |
| 4 | a Implement 3 - bit binary counter using the case statement Description with Verilog and VHDL. | 08 |
| | b Illustrate various Loop statement of VHDL and Verilog. | 08 |
| 5 | a Define synthesis Describe various synthesis steps. | 08 |
| | b Compare if else statement in VHDL and Verilog with an example. | 08 |
| OR | | |
| 6 | a With an example, explain else if case statement show the RTL synthesis. | 08 |
| | b Explain synthesis of the Loop statement. | 08 |
| 7 | a Write HDL code for full adder using Procedure and task. | 08 |
| | b Illustrate how an VHDL entity can be invoked from Verilog with an example. | 08 |
| OR | | |
| 8 | a Write HDL code for N - bit Ripple carry Adder using Procedure and Task. | 08 |
| | b Describe the Need for mixed Type Description. | 08 |

DAYANANDA SAGAR COLLEGE OF ENGINEERING(An Autonomous Institute Affiliated to VTU, Belagavi)
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560078**UG Make-Up Examination, February 2019**

Course: **Digital System Design using HDL**
 Course Code: **ML561**
 Semester: **V**

Maximum marks: 100**Duration: 3 hours**

Note: i). Question ONE (a to t) has to be answered from pages 5 to 7 only.
 ii). Question 1 to 4 is compulsory.
 iii). Any missing data should be suitably assumed.

Q. No.		Marks
1	a) An entity can have _____ number of architecture.	01
	b) What data type has to be used to represent voltage, time?	01
	c) In Verilog inout ports must always be _____.	01
	d) Which level of abstraction level is available in Verilog but not in VHDL?	01
	e) Variables can be used only with _____ type of description.	01
	f) VHSIC stands for _____.	01
	g) State the two phases that are involved in signal assignment statement execution.	01
	h) Which logic level is not supported in Verilog?	01
	i) Determine whether the following statements are VHDL, Verilog or can be both.	01
	i) input D,E	
	ii)begin	
	iii)port(i1:in bit;o1:out bit)	
	j) _____ is mainly used for repetition of concurrent statement.	01
	k) Write execution of IF as Latch in Verilog.	01
	l) Functions can have only a single output. Is it true or false.	01
	m) Tasks can have more than one output. Is it true or false.	01
	n) Digital hardware domain in which the HDL code is synthesized does not include _____ signals.	01
	o) In hardware domain the integer is represented by _____.	01
	p) Component instantiation is done in which type of HDL description.	01
	q) Can packages and libraries have explicit mapping?	01
	r) The key word "port map" is used in _____ description.	01
	s) Wire in Verilog is similar to _____ in VHDL.	01
	t) If A=1100 then A >>1 is equal to _____.	01
2	a) Discuss the scalar data types supported by VHDL with relevant examples.	10
	b) Explain the structure of HDL module with the help of an example.	06



- 3 a) Identify the errors in the code given below 06
- ```
module mult(a,b,P)
 input (1:0) b;
 output [3:0] A;
 P[0]=a[0] & b[0];
 assign P[0]= a[0] and b[0];
endmodule;
```
- b) Develop a VHDL code to implement 3-bit carry look ahead adder. 10
- 4 a) Develop a Verilog code to compute the factorial of a positive integer. 05
- b) Identify the situation in which the **casex** statements are used. 05  
And illustrate it with an example.
- c) Develop a VHDL code to realize 2X1 MUX using if-else statements. 06
- 5 a) Summarize the general synthesis steps with a neat flow diagram. 06
- b) Write a Verilog code to synthesis the following statement, 10  
 $Y=2*X+3$ , where X is a two bit input and Y is output. Draw the gate level logic diagram.
- OR
- 6 a) Demonstrate the mapping of if, if-else case statements in HDL and draw the gate level diagram. 10
- b) Explain the mapping of functions that are implemented using Verilog. 06
- 7 a) Develop a Verilog code to evaluate an expression using the functions. The expression to be evaluated is  $Y=(a \text{ xor } b)+(a \text{ and } b)$  10
- b) Illustrate the mixed language description of an AND gate. 06
- OR
- 8 a) Write a VHDL function to find the largest of three signed numbers. 06
- b) Realize JK flip flop using both VHDL and Verilog. 10