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Dayananda Sagar College of Engineering
Department of Electronics & Communication Engg.
Continuous Internal Evaluation – III

Course Name : Digital Signal Processing	Date :	4/1/2021
Course Code : 18EC5DCDSP	Day :	Monday
Semester : 5	Timings :	1PM-2.30PM
Max Marks : 50 M	Duration :	1½ Hrs.

Q. No	Question Description	Mar-ks	CO & Levels
1	(a) Which one of the following is true with Von Neuman architecture i) pipelining is possible ii) dedicated address and data bus for program and data memory iii) Always preferred iv) memory is shared by both program and data	1	
	(b) Circular buffer is a i) LIFO register ii) FIFO register iii) FILO register iv) LIFO register	1	
	(c) TMS C3X CPU contains an ALU which is capable of operating on i) both integer and floating-point arithmetic ii) floating point iii) fixed point iv) Fractional points	1	
	(d) HPI in TMS320CXX is i) Host port interface ii) Host peripheral interface iii) House port interface iv) Host port interrupt	1	
	(e) MAC in a DSP processor is i) CPU of DSP processor ii) ALU of DSP processor iii) decoder iv) None of the above	1	
	(f) An assembler directive is the i) message for the DSP Processor ii) message for the compiler iii) Instruction iv) message for the assembler	1	
	(g) Number of timer interrupts in TMS320C6X processor is i) 4 ii) 12 iii) 2 iv) None of the above	1	
	(h) CSR in interrupt concept is i) current sequence register ii) control status register iii) control sequence register iv) current status register	1	
	(i) All interrupts remain pending while the i) IE is not enabled ii) CPU has a pending branch instruction iii) ICR is having a zero iv) None of the above	1	
	(j) Which of the below is correct to store a 40 bit value	1	

	i) A3:A2 ii) A2:A3 iii) A5:A4 iv) Both i and iii			
2	a)	Explain in detail the Von Neuman architecture and Harvard architecture	4	
	b)	Compute the lattice coefficients for the FIR filter given below **Y(n)=x(n)+1/3x(n-1)+1/2x(n-2)+1/3 x(n-3). Draw the lattice form**	6	
3	a)	Draw the functional block diagram of TMS320C6713 architecture and explain in detail.	8	
	b)	List the Salient features of TMS320C6713 Digital Signal Processor	2	
4		Perform the following operations 1)Convert the Q-15 signed number **1.010101110100010** to the decimal 2)Find the Q-15 representation for the decimal number **-0.2160123** 3)Add the following two-Q-bit numbers **1.101010111000001 + 0.010001111011010** 4) Convert the following IEEE single precision format to the decimal format 101000000.010…0000.	10	
		OR		
5		Convert each of the following decimal numbers to the floating point number using the format of 4 bits for exponent and 12 bits for mantissa **1) 0.2683** **2) -0.1890** **3) 0.1101235** **4) -10.430527**	10	
6	a)	Illustrate the mode of operation of indirect addressing mode with examples (TMS320C6X processor)	6	
	b)	Explain in brief the Pipelining operation of TMS320C6X processor with one example	4	
		OR		
7	a)	Explain in brief the following with respect to TMS320C6X processor 1.Functional units 2.Fetch and execute packets	4	
	b)	Illustrate the working of add/subtract/multiply instruction with respect to TMS320C6X processor showing example.	6	