

### 11.3 TMS320C5x Family of Digital Signal Processors

The TMS320C5x family of processors are fifth-generation digital signal processors from Texas Instruments, USA. They are 16-bit fixed point processors fabricated using high performance static CMOS technology. These processors have advanced Harvard architecture, with a variety of on-chip peripherals and memory and highly specialized instructions. They can execute 50 Million Instructions Per Second(MIPS).

Some of the features of TMS320C5x family of digital signal processors are,

- 16-bit CPU
- 20 to 50 ns single cycle instruction execution time
- Single cycle  $16 \times 16$ -bit MAC (Multiply/Accumulate) unit
- $64k \times 16$ -bit external program memory address space
- $64k \times 16$ -bit external data memory address space
- $64k \times 16$ -bit external IO address space

- $32k \times 16$ -bit external global memory address space
- 2k to  $32k \times 16$ -bit single-access On-chip PROM
- 1k to  $9k \times 16$ -bit single-access On-chip program/data RAM
- 1k  $\times 16$ -bit dual-access On-chip program/data RAM
- Synchronous, TDM and buffered serial ports
- Programmable timer and PLL (Phase Locked Loops)
- IEEE standard JTAG ports
- 5 V/3 V operation with low power dissipation and power down modes
- DMA interface
- 100/128/132/144 pins in plastic QFP and TQFP

### 11.3.2 Architecture of TMS320C5x Processors

The TMS320C5x processors have an advanced version of Harvard architecture, with separate buses for program and data, which facilitate simultaneous access of program and data. The program bus has separate lines to transmit data and address. Similarly the data bus has separate lines to transmit data and address.

The internal architecture of TMS320C5x processor is shown in fig 11.9. The architecture of TMS320C5x processors can be broadly divided into three major areas. They are, CPU (Central Processing Unit), memory and peripherals.

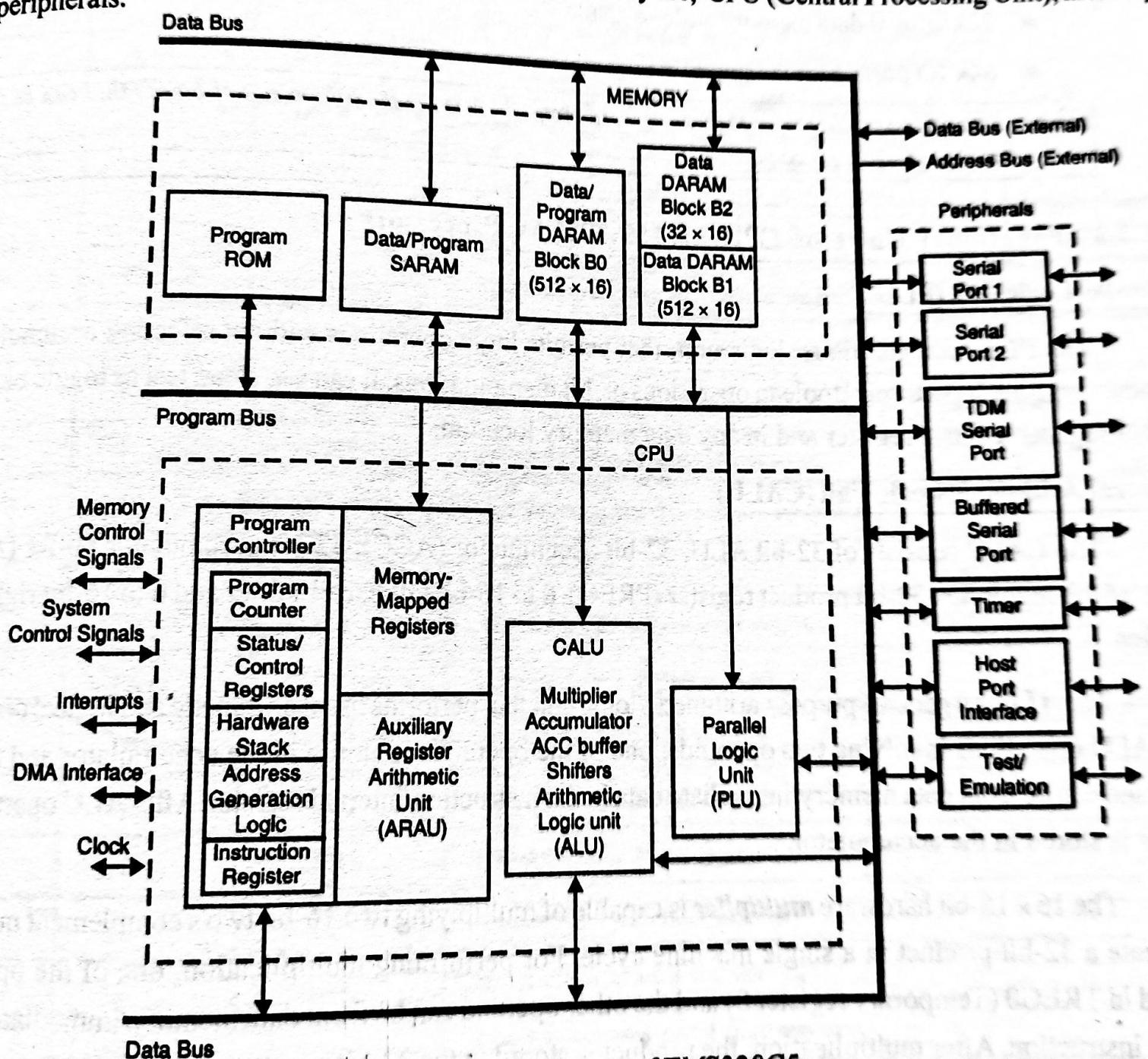


Fig 11.9 : Internal architecture of TMS320C5x.

The functional units of CPU are Parallel Logic Unit (PLU), central ALU, memory mapped registers, Auxiliary Register Arithmetic Unit (ARAU) and program controller.

The TMS320C5x processors has the following internal (or on-chip) memory.

- Program ROM (2k to 32k words)
- Data/Program Dual Access RAM (DARAM) ( $1024 + 32 = 1056$  words)
- Data/Program Single Access RAM/(SARAM) (1k to 9k words)

The various on-chip or internal peripherals of TMS320C5x processors are clock generator, hardware timer, software programmable wait state generators, parallel IO ports, Host Port Interface (HPI), serial port, Buffered Serial Port (BSP), Time Division Multiplexed (TDM) serial port and user maskable interrupts.

The TMS320C5x processors have a total memory address space of 224k (including on-chip memory) with addressability of 16 bits. This address space is divided into four individually selectable address spaces as follows.

- 64k Program memory address space
- 64k Local data memory address space
- 32k Global data memory address space
- 64k IO ports address space

**Note :** The addressability refer to memory word size, which is the maximum size of binary that can be stored in one memory location.

### 11.3.3 Functional Units of CPU of TMS320C5x Processors

#### Parallel Logic Unit (PLU)

The **PLU** is an additional logic unit, that permits logic operations without affecting accumulator or product register. It performs Boolean operations or bit manipulations. It can set, clear, test or toggle bits in the status register, control register and in any data memory location.

#### Central Arithmetic Logic Unit (CALU)

The **CALU** consists of 32-bit ALU, 32-bit accumulator (ACC), 32-bit accumulator buffer (ACCB),  $16 \times 16$ -bit multiplier, 32-bit product register (PREG), 0 to 16-bit left barrel shifter and 0 to 16-bit right barrel shifter.

The **ALU** is a general-purpose arithmetic/logic unit that performs usual arithmetic and logical operations. For ALU operations involving two operands, one of the operands is stored in the accumulator and the other operand can be from data memory/immediate data in the instruction/internal register. After ALU operation, the result is stored in the accumulator.

The  $16 \times 16$ -bit hardware **multiplier** is capable of multiplying two 16-bit two's complement numbers to generate a 32-bit product in a single machine cycle. For performing multiplication, one of the operands is stored in TREG0 (Temporary register 0) and the other operand can be from data memory/immediate operand in the instruction. After multiplication, the product is stored in the 32-bit **product register** (PREG).

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The 0 to 16-bit left and right shifter permit the content of memory to be shifted before loading into ALU and vice versa. The content of accumulator (ACC) and product register (PREG) can also be shifted using these shifters.

### Memory-Mapped Registers

The TMS320C5x has 96 numbers of 16-bit memory-mapped registers, and they are mapped into page-0 of data memory space. The memory-mapped registers includes various control and status registers for CPU, serial port, timer and software wait-state generators. Also they include 16 memory-mapped IO ports.

### Auxiliary Register Arithmetic Unit (ARAU)

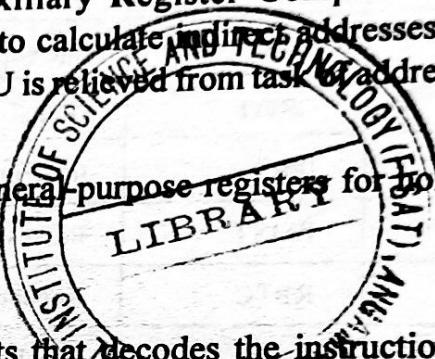
The *ARAU* contains eight 16-bit auxiliary registers AR0-AR7, a 3-bit Auxiliary Register Pointer (ARP), a 16-bit index register (INDX) and a 16-bit Auxiliary Register Compare Register (ARCR). An unsigned 16-bit arithmetic unit in the ARAU is used to calculate indirect addresses, using the contents of ARP, INDX and ARCR registers. Therefore, the CALU is relieved from task of address manipulation and so it is free for other operations in parallel.

The auxiliary registers can also be used as general-purpose registers for holding the operands for arithmetic and logical operation in CALU.

### Program Controller

The *program controller* contains logic circuits that decodes the instructions, manages the CPU pipeline, stores the status of CPU operations and decodes the conditional operations. Due to parallelism in architecture, the program controller can perform three concurrent or simultaneous memory operations in any given machine cycle. They are fetch an instruction, read an operand and write an operand.

The program controller unit consists of a 16-bit Program Counter (PC), 16-bit status registers ST0 and ST1, Processor Mode Status register (PMST) and Circular Buffer Control Register (CBCR), a  $16 \times 16$ -bit hardware stack, address generation logic, instruction register, interrupt flag register and interrupt mask register.



### 11.3.4 On-Chip Memory in TMS320C5x Processors

The TMS320C5x family of processors consists of three different types of on-chip memory and they are mask-programmable ROM, Single-Access RAM (SARAM) and Dual-Access RAM (DARAM). The various members of TMS320C5x will have different capacity of on-chip memory which are listed in table 11.4.

#### Program ROM

The various models of TMS320C5x processors have internal maskable-Program ROM (PROM) of size 2k to 32k words. The processor has an option for including or excluding the on-chip PROM addresses in the processor program memory address space.

The main purpose of PROM is to permanently store the program code for a specific application during manufacturing of the chip itself. The processor has an option of boot loading the content of PROM to internal/external RAM during power-ON reset. The content of the PROM can be protected so that any external device cannot have access to the program code. This feature provides security for proprietary algorithms.

#### Data / Program Dual-Access RAM (DARAM)

The TMS320C5x processor has 1056 words [ $1056 \times 16$  bits] on-chip Dual-Access RAM (DARAM), which is divided into three blocks, B0, B1 and B2.

- The block B0 has 512 words [ $512 \times 16$  bits] data / program RAM.
- The block B1 has 512 words [ $512 \times 16$  bits] data RAM.
- The block B2 has 32 words [ $32 \times 16$  bits] data RAM.

#### Data / Program Single-Access RAM (SARAM)

The various models or TMS320C5x processor has 1k words to 9k words of SARAM.

The internal SARAM can be configured as data memory, program memory and combination of data and program memory

The SARAM can be divided into block of 1k/2k words with continuous address. The processor CPU can access one block for reading while writing in another block.

### 11.3.5 On-Chip Peripherals of TMS320C5x Processors

The various on-chip peripherals of TMS320C5x processors are clock generator, hardware timer, software-programmable wait-state generators, parallel IO ports, Host Port Interface (HPI) and serial ports.

#### Clock Generator

The **clock generator** of the TMS320C5x processor consists of an internal oscillator and a Phase Locked Loop (PLL) circuit. The clock generator can be driven by an external crystal resonator circuit or supplied by an external clock source. The **PLL** circuit can generate an internal CPU clock by multiplying the clock source by a specified factor, so that CPU is driven by high frequency clock and clock source can be used as source for other peripherals which runs at low frequency clock.

## Hardware Timer

A 16-bit hardware timer with a 4-bit prescaler is available in TMS320C5x processor. This programmable timer generates clock at a rate that is between 1/2 and 1/32 of the machine cycle rate (CLKOUT1), depending upon the timer divide-down ratio. The timer can be stopped, restarted, reset or disabled by specific status bits. The processor has three registers to control and operate the timer and they are Timer Control Register (TCR), timer counter register (TIM) and timer period register (PRD). The timer counter register gives the current count of the timer. The timer period register defines the period for the timer. The 16-bit timer control register controls the operations of the timer.

## Software Programmable Wait - State Generators

The TMS320C5x processor has software-programmable *wait-state generators*, which can insert/generate wait-states in external bus cycles for interfacing with slow speed external memory and IO devices. The processor consists of multiple wait-state generating circuits, and each circuit is user-programmable to insert different number of wait states for external memory accesses. These wait-state generators can extend the external bus cycles up to seven machine cycles.

## Parallel IO Ports

The TMS320C5x processor has 64k *IO address space* which can be used as 64k IO ports and 16 of these ports are memory-mapped in data memory space. Each of the IO ports can be addressed by the IN or the OUT instruction. The memory-mapped IO ports can be accessed with any instruction that reads from or writes to data memory. The TMS320C5x generates a hardware signal  $\overline{IS}$  during IO access to indicate a read or write operation through an IO port. The TMS320C5x can easily interface with external IO devices through the IO ports with minimal external address decoding circuits.

## Host Port interface (HPI)

The HPI is available on the TMS320C57S and TMS320LC57 processors. The *HPI* is an 8-bit parallel IO port that provides an interface to a host processor for information exchange between the Digital Signal Processor (DSP) and the host processor. The DSP has 2k word on-chip memory that is accessible to both the host processor and the DSP. The HPI is connected to this memory through a dedicated bus, so that the CPU can work uninterrupted while the host processor accesses the memory through host port.

**Note :** A host processor is an independent microprocessor/micorcontroller that is designed to carry out some specific tasks and deliver the results to digital signal processor.

## Serial Ports

Three different kinds of serial ports are available in TMS320C5x processors and they are general-purpose serial port, Time-Division Multiplexed (TDM) serial port and Buffered Serial Port (BSP). Every TMS320C5x processor contains at least one general-purpose, high-speed synchronous, full-duplexed serial port which can be used to provide direct communication with serial devices such as codec, serial analog-to digital (A/D) converters and other serial systems. The serial port is capable of operating at a clock rate up to one-fourth the machine cycle rate (CLKOUT1). The serial port transmitter and receiver are double-buffered and individually controlled by maskable external interrupt signals. For serial communication the data is framed either as bytes or as words.