Kintex-7 FPGAs
Optimized for Best Price-Performance
(1.0V, 0.9V)

		XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
	Part Number							
	™ Cost Reduction Solutions[1]	—	—	XCE7K325T	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices	10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kb)	838	2,188	4,000	5,088	5,663	5,938	6,788
	RAM/FIFO w/ ECC (36 Kb each)	135	325	445	715	795	835	955
	Total Block RAM (Kb)	4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O	300	400	500	300	500	400	400
	Maximum Differential I/O Pairs	144	192	240	144	240	192	192
Embedded Hard IP Resources	DSP48E1 Slices	240	600	840	1,440	1,540	1,680	1,920
	PCI Express®[2]	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) /	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTX 12.5 Gb/s Transceivers	8	8	16	24	16	32	32
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Package[4] / Dimensions (mm)	Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX Transceivers)						
	FBG484 / 23 x 23	185, 100 (4)	185, 100 (4)					
Footprint Compatible	FBG676 / 27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)		250, 150 (8)		
	FFG676 / 27 x 27		250, 150 (8)	250, 150 (8)		250, 150 (8)		
Footprint Compatible	FBG900 / 31 x 31			350, 150 (16)		350, 150 (16)		
	FFG900 / 31 x 31			350, 150 (16)		350, 150 (16)		
	FFG901 / 31 x 31				300, 0 (24)		380, 0 (28)	380, 0 (28)
	FFG1156 / 35 x 35						400, 0 (32)	400, 0 (32)

XMP085 (v3.6)

FBG 1.0mm Lidless flip-chip; **FFG**: 1.0mm Flip-chip fine-pitch

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com