Benjamin Newcomer

Feb 9th, 2015

CS 3220 Assignment 1 Report

In this project, the system had to display a digital clock with two modes. The first, display mode, simply displays the time using the seven segment displays and the green LEDs. The other mode, set mode, tracks button presses, blinks the display, and allows the user to change the time. In order to store minutes and hours the system uses two registers the same way centiseconds, deciseconds, and seconds are handled. To display time on the SevenSeg modules, the hours and minutes registers are split into decimal digits and fed into the SevenSeg modules. The system checks SW[0] to switch between display mode and set mode, which are represented as parameters in the Verilog design. For each mode, there are blocks that define mode specific behavior, like blinking or registering button presses. To enable blinking, the system disables the SevenSeg modules (by modifying the modules and adding a DISABLE input signal) and outputs 0 to the LEDGs when the decisecond count is less than five. To enable button presses, the system uses the strategy described in class that stores button press transitions by comparing old button signals and new button signals and asserting transitions as signals that can be checked on clock edges. The following actions are taken on button presses: Key[0] increments.

Displaying the clock was the simplest component of the assignment because the template that was given included most of the logic needed. Enabling blinking and tracking button presses were more difficult because there was no strategy given. The button tracking strategy was fairly simple to implement after being introduced to it in class. In total, 258 logic elements and 51 registers were used when modulo was used to display the time. After changing

the design to get rid of modulo, 216 logic elements and 56 registers were used. Instead of storing minutes and hours in single registers, they were split up into individual registers for each digit. The registers are incremented independently and can simply be assigned to the SevenSeg modules, no modulo or division required.