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ENEE359F

HW4

16-Bit Wallace Tree Multiplier

DESIGN AND IMPLEMENTATION

To design a 16-bit multiplier, we used the Wallace tree because it is the most efficient structure that allows for fast computations using as many Carry Save Adders working in parallel as possible. CSA’s add three numbers at a time and does not propagate the carry. Instead, they output two numbers, one which is the raw value of the numbers added together, and the other the carry bits that need to be added to get the correct final answer. At the end of the Wallace tree of CSAs, we add the final sum and carry values together using a Carry Propagate Adder to get the final answer. We can design a 16-bit multiplier using CSA’s whose widths are 16-bit, 18-bit, 19-bit, 20-bit, and 24-bit to do all the calculations. In my implementation I used all 32-bit CSA’s because the ease of use was much greater than the cost benefit of cheaper hardware. In the future when optimizations are necessary, using the smaller width adders would be much more beneficial. The a diagram of the circuit I used is at the bottom, lines representing wires, and the blue boxes representing CSA’s, while the final box is a CPA.

OUTPUTS



