CSCI 564 Advanced Computer Architecture

Lecture 06: Cache Optimizations

Ismet Dagli (credit to Dr. Bo Wu and Sumner Evans)

January 31, 2024

Colorado School of Mines

Quick Look into Feedback

- **7x** Going so fast, we need more examples/details
- **5x** Going so slow, we already learned these!!!
- **4x** Slides not available on Canvas
- **3x** More readable / well presented slides / more references for further reading
- **21x** Good/Perfect/Great

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Midterm

Midterm date: 13 March, Wednesday

Midterm review: 11 March

Details:

- 75 minute
- In-class (same class, MET)
- Closed book (Considering on one-page data/formula sheet)

Please reach out to Ismet Dagli if you have any concern, request, special situation etc. about exam

Performance Enemy: Cache Misses

5 step approach for cache hits/misses

Repeat the steps below for each cache access

- **Access Request:** When the CPU needs to access data, it first checks the cache. The address of the data is divided into the tag, index, and offset.
- **Indexing:** The index part is used to find a cache line.
- **Tag comparison:** The tag is compared to the tag part of the address. If they match, it's a cache hit.
- **Data Retrieval:** If the data is found (cache hit), it's sent back to the CPU. If not (cache miss), the data is fetched from the main memory, stored in the cache for future access.
- **Updating the Cache:** When new data is fetched from memory due to a cache miss, it replaces an existing entry in the cache.

A Simple Example: Increased Associativity

Consider a **2-way set-associative** cache with **8 blocks**, a block size of **32 bytes**.

We have an application which repeats the following memory access sequence:

- 0x80000000
- 0x80000008
- 0x80000010
- 0x80000018
- 0x30000010

Cache Geometry Calculations

Index bits $= \log_2(8/2) = 2$

Offset bits $= \log_2(32) = 5$

Tag bits $= 32 - (2 + 5) = 25$

Example:

0x80000010 =

$\underbrace{10000000000000000000000}_{\text{tag}}\ \underbrace{00}_{\text{index}}\ \underbrace{10000}_{\text{offset}}$

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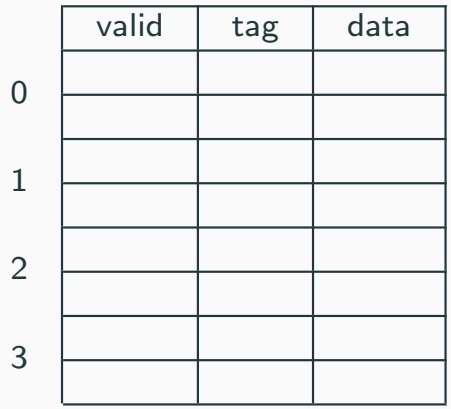

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2			
3			

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Reducing Each Type of Cache Miss

Reducing Compulsory Misses: Increase Cache Line Size

The processor will request larger chunks of memory at a time.

This only works if there is good *spacial locality*, otherwise, you are bringing in data you don't need.

- If you are reading bytes effectively at random (a few bytes here, a few bytes there), this will hurt performance.
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    sum += data[i];
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Reducing Compulsory Misses: Prefetching

The idea is to *speculate* on future instruction and data accesses and fetch them into cache.

- Instruction accesses are easier to predict than data accesses.

Varieties of prefetching:

- Hardware prefetching
- Software prefetching
- Mixed schemes

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Reducing Compulsory Misses: Hardware Prefetching

Consider the following code:

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In this case, the processor could identify the pattern and proactively prefetch data the program will ask for.

What's the address access pattern?

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What's the address access pattern? $\text{nextAddr} = \text{curAddr} + 4$.

Reducing Compulsory Misses: Hardware Prefetching

There are many variants of hardware prefetching

- **Prefetch-on-miss:** prefetch $b + 1$ upon miss on b.
- **One block lookahead scheme:**
  - Initiate prefetch for block $b + 1$ when block b is accessed
  - Can extend to N-block lookahead.
- **Strided prefetch:** If the sequence of accesses observed is $b, b + N, b + 2N$, then prefetch $b + 3N$, etc.

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Reducing Compulsory Misses: Hardware Prefetching: Issues

We want our prefetching to be

- **Useful**: should produce cache hits
- **Timely**: should be not too late and not too early

We also have to be wary of cache and bandwidth pollution.

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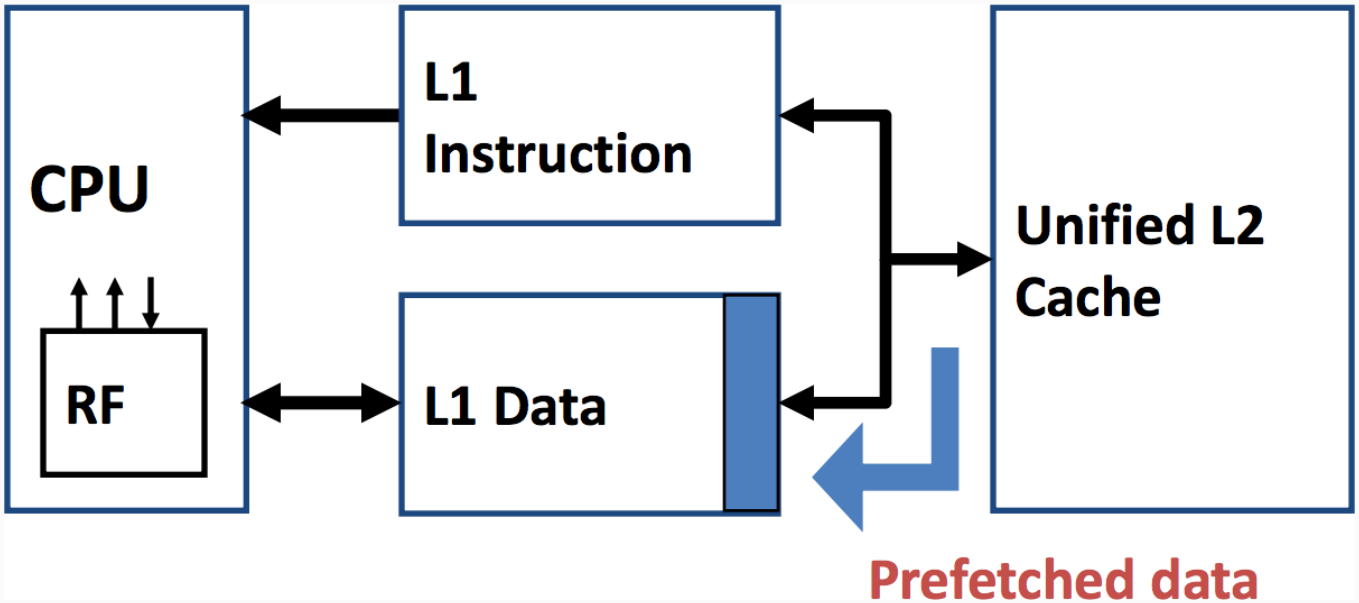

Reducing Compulsory Misses: Software Prefetching

We can attempt to have the hardware prefetch for us by accessing data before we need it.

```
for (int i = 0; i < N; i++) {
    prefetch( &a[i + P] );
    prefetch( &b[i + P] );
    SUM = SUM + a[i] * b[i];
}
```

Although accesses are *predictable*, we will run into issues with getting the prefetch *timing* right.

- If you prefetch very close to when the data is requested, you may be too late.
- If you prefetch too early, you will cause pollution.
- You can estimate how long it will take for the data to come into L1 cache and set `P` accordingly.
- Why is this hard to do?

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Reducing Compulsory Misses: Hardware Instruction Prefetching

- Fetch two blocks on miss: the requested block (`i`) and the next consecutive block (`i + 1`).
- Place the requested block in cache, and the next block in the instruction stream buffer.
- If miss in the cache but a hit in the stream buffer, move the stream buffer block into cache and prefetch the next block (`i + 2`).

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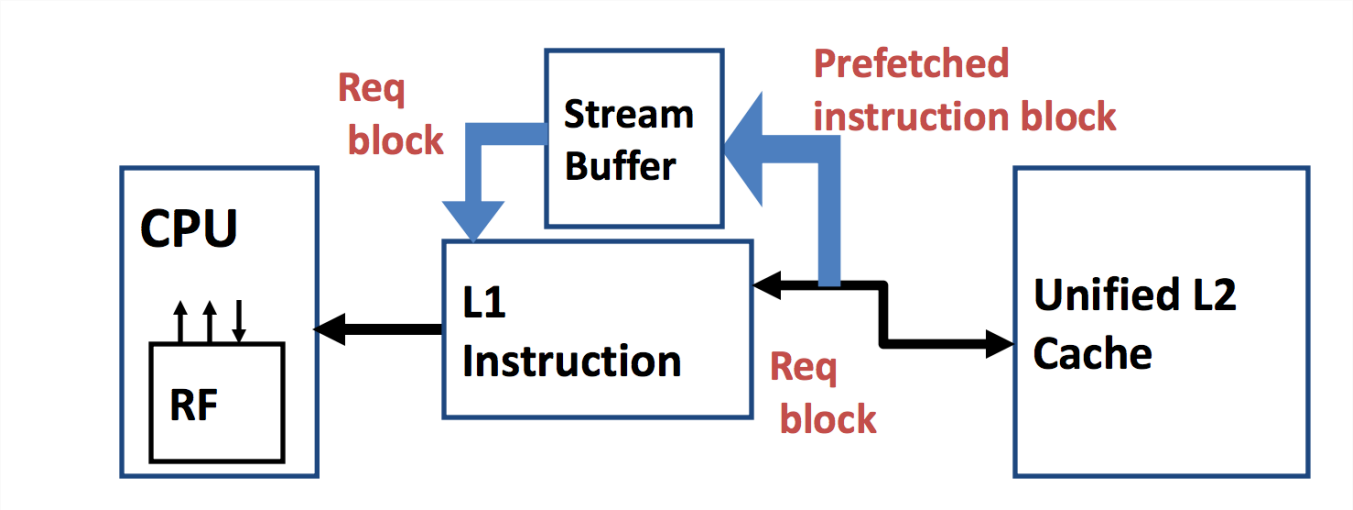

Reducing Compulsory Misses: Restructuring

We can restructure the code to take advantage of the memory access pattern.

```
struct Atom {
    double v;
    double f;
    double3 p;
};

struct Atom atoms[N];

for (i = 0; i < N; i++)
    ... = atoms[i].v + ...

for (i = 0; i < N; i++)
    ... = atoms[i].f + ...

for (i = 0; i < N; i++)
    ... = atoms[i].p + ...
```

→

```
double vs[N];
double fs[N];
double3 ps[N];

for (i = 0; i < N; i++)
    ... = vs[i] + ...

for (i = 0; i < N; i++)
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for (i = 0; i < N; i++)
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$\rightarrow$

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Reducing Conflict Misses: Why They Happen

Conflict misses occur when the data we need was in the cache previously, but got evicted.

When do evictions occur?

- Direct-mapped: another request mapped to the same cache line
- Associative: too many requests mapped to the same set

Example: assume a 4 KiB cache

```
while (1) {
    for (i = 0; i < 1024 * 1024; i += 4096) {
        sum += data[i];
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Reducing Conflict Misses: Colliding Threads and Data

- The stack and the heap tend to be aligned to large chunks of memory (maybe 128 MiB).
  - Threads often run the same code in the same way.
  - This means that thread stacks will end up occupying the same parts of cache.
  - Randomize the base of each thread's stack.

- Large data structures (for example, arrays) are also often aligned. Randomizing `malloc` can help.

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Reducing Conflict Misses: Colliding Threads and Data

- The stack and the heap tend to be aligned to large chunks of memory (maybe 128 MiB).
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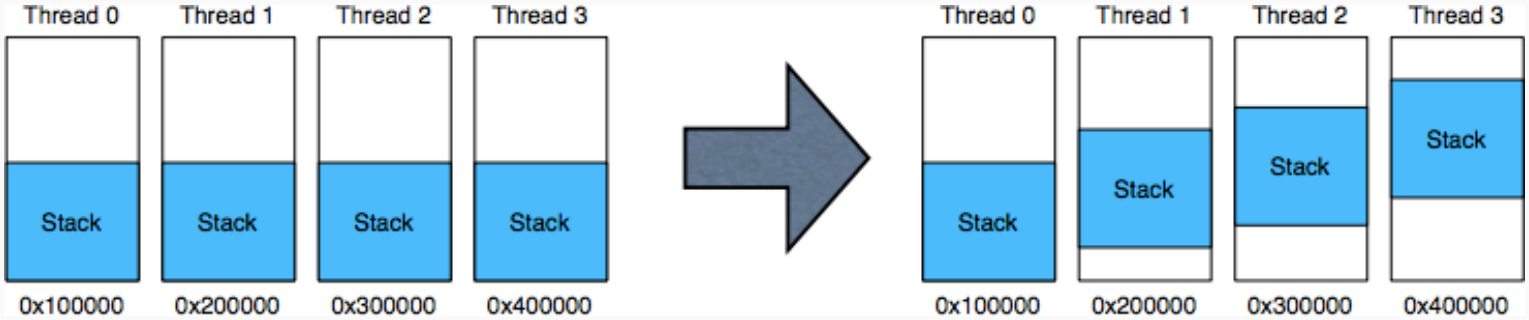

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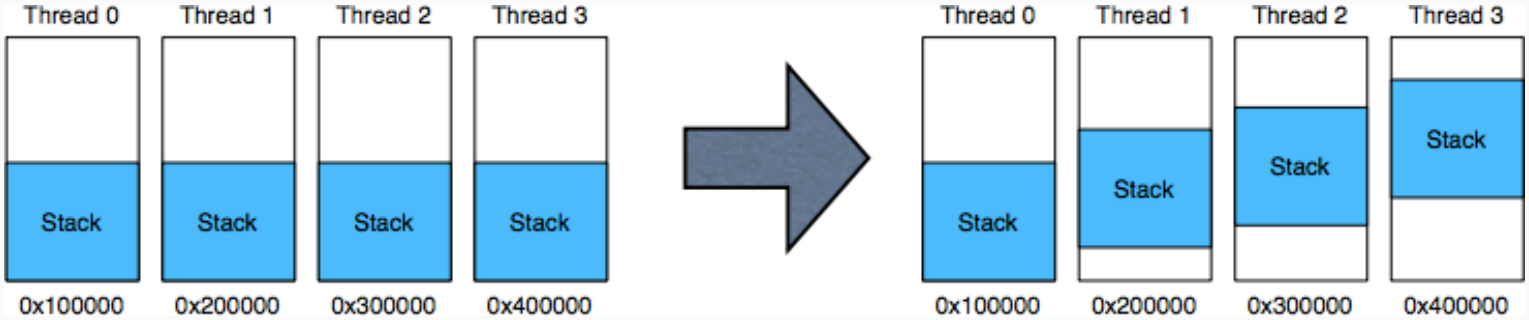

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Reducing Capacity Misses: Why They Happen

Capacity misses occur because the processor is trying to access too much data.

- *Working set*: the data that is currently important to the program
- If the working set is bigger than the cache, you are going to miss frequently.

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Reducing Capacity Misses: Basic Mitigations

- Increase capacity
- More associativity or more associative "sets"
  - Costs area and makes the cache slower
- Cache hierarchy does this implicitly already
  - If the working set "falls out" of the L1 cache, L2 cache can still be utilized
- In practice, you make L1 as big as you can within your cycle time and the L2 and L3 as big as you can while keeping it on chip.

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Reducing Capacity Misses: Tiling

Say we have an application that needs to make several passes over a large array. Doing each pass in turn will "blow out" our cache.

"Blocking" or "tiling" the loops will prevent the blowout, but whether or not it's possible to do so depends on the structure of the loop.

You can tile hierarchically to fit into each level of the memory hierarchy.

Example: `http://polaris.cs.uiuc.edu/~garzaran/doc/lcr04.pdf`

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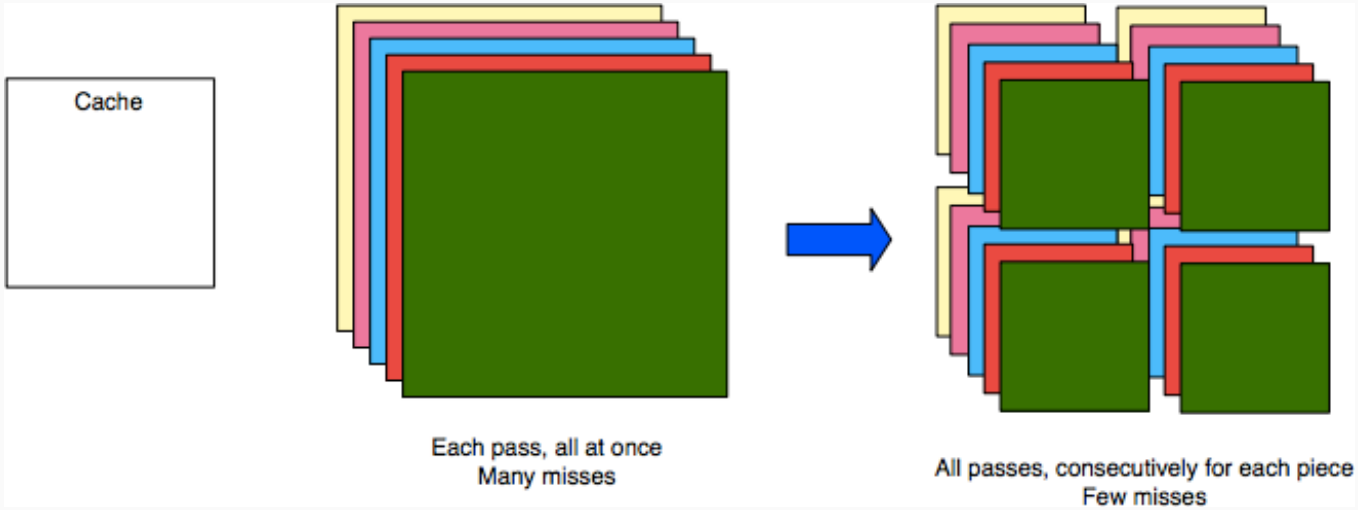

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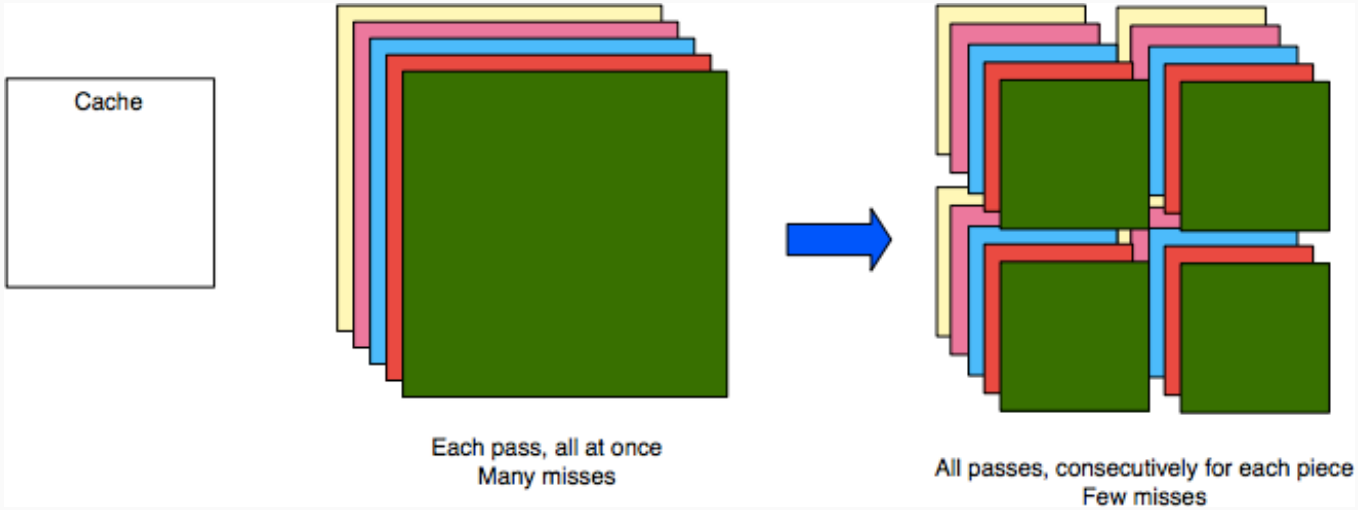

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Practice

Practice: Affects of Prefetching: Problem 1: Question

What affects may prefetching have on

1. compulsory misses?
2. capacity misses?
3. conflict misses?

Practice: Affects of Prefetching: Problem 1: Answer

What affects may prefetching have on

1. Q: Compulsory misses?
   A: Likely reduces compulsory misses (data that gets used later is already in the cache)
2. Q: Capacity misses?
   A: Will not affect capacity misses (the working set is still the same, we just happened to prefetch more of it into the cache)
3. Q: Conflict misses?
   A: May increase conflict misses since it may evict lines that are needed to make room for prefetched lines

Practice: Prefetching Strategies: Problem 2: Question

Assume you have a cache where cache lines are 32 bytes. Also assume that integers take 4 bytes.

Write a loop in C that performs significantly better when using a *strided prefetcher* than when using a *one block lookahead scheme*.

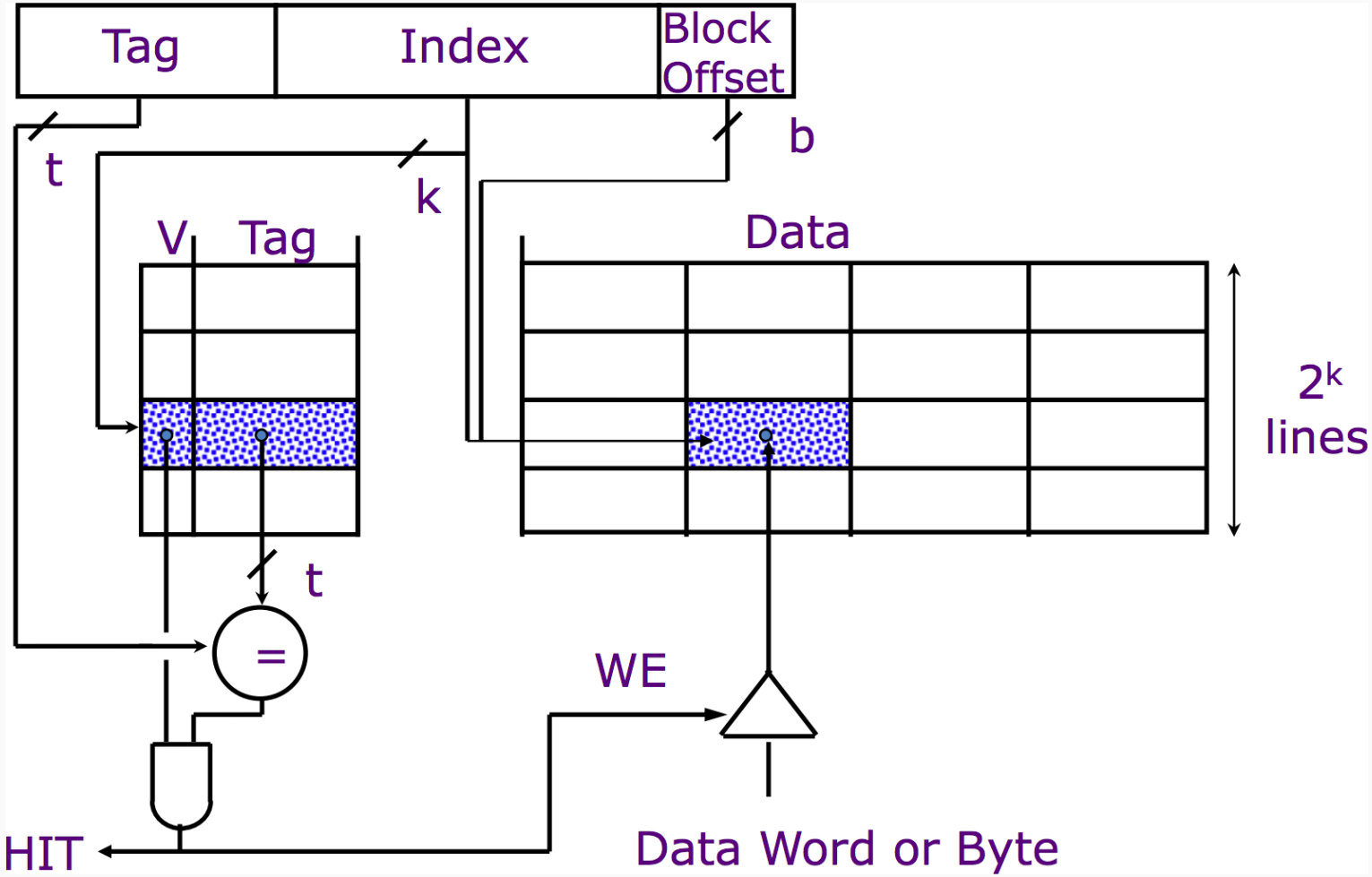
Practice: Prefetching Strategies: Problem 2: Answer

Write a loop in C that performs significantly better when using a *strided prefetcher* than when using a *one block lookahead scheme*.

```
1  int *A = malloc(1024 * 1024 * sizeof(int));
2  int j = 0;
3  while (j < 1024 * 1024) {
4      int sum = 0;
5      for (int i = 0; i < 8; i++)
6          sum += A[j+i];
7      j += 16; // skip two cache lines
8  }
```

A Few More Considerations

Write Performance: Process



Write Performance: Reducing Write Time

Problem: Writes take two cycles. One for tag check and another for writing the data.

Solution 1:

1. Check tag, put old data and write data into a buffer
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Solution 2: pipeline the writes

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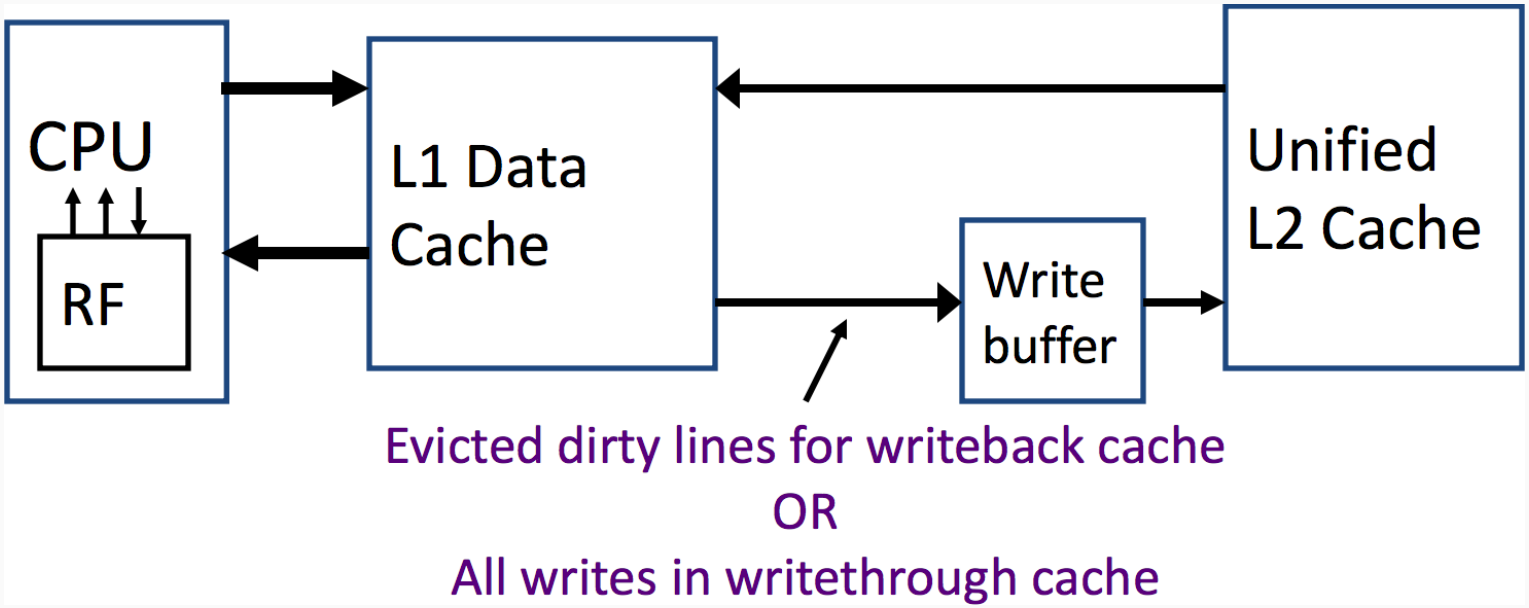

Problem: Write buffer may hold updated value of location needed by write miss

- Simple solution: on read miss, wait for write buffer to drain
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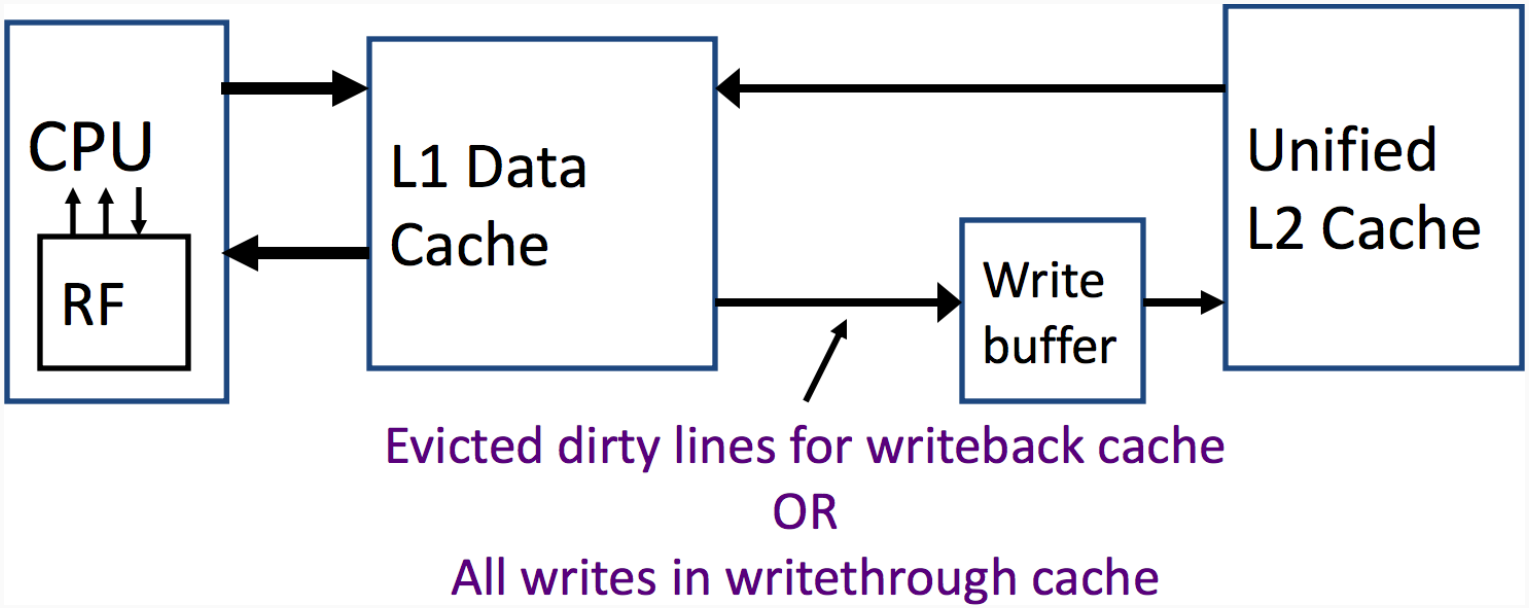

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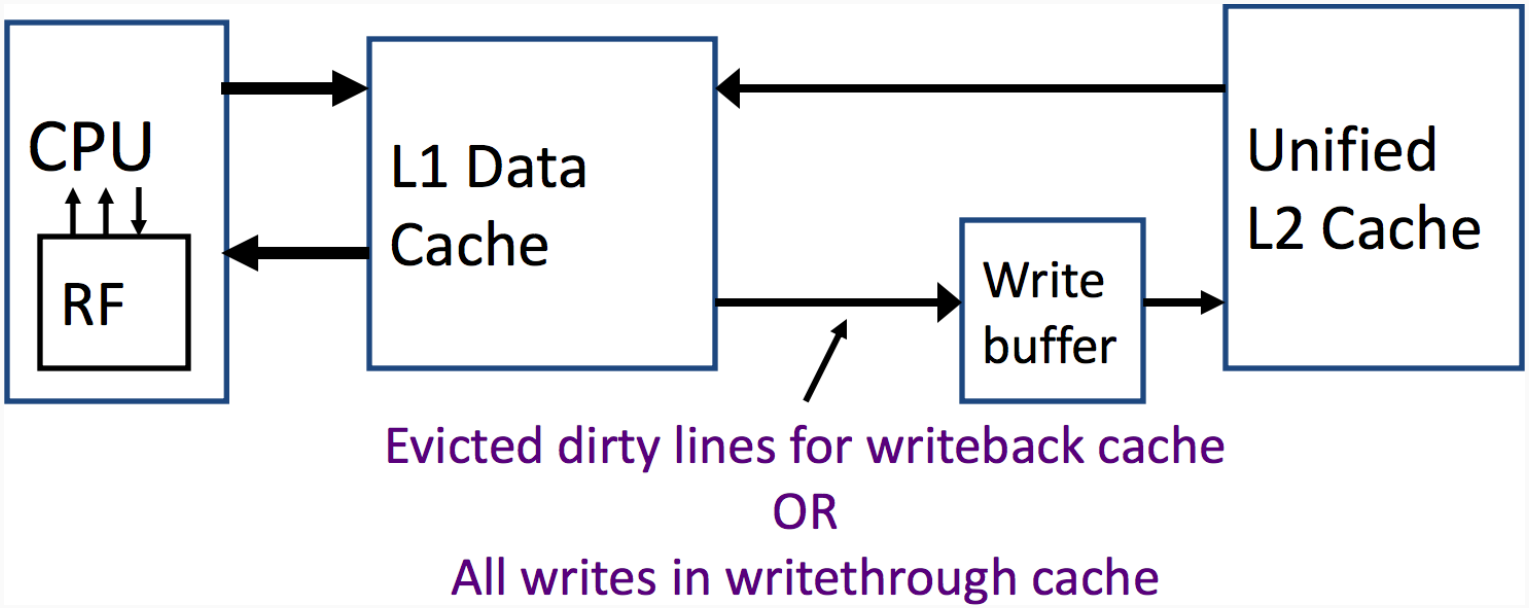

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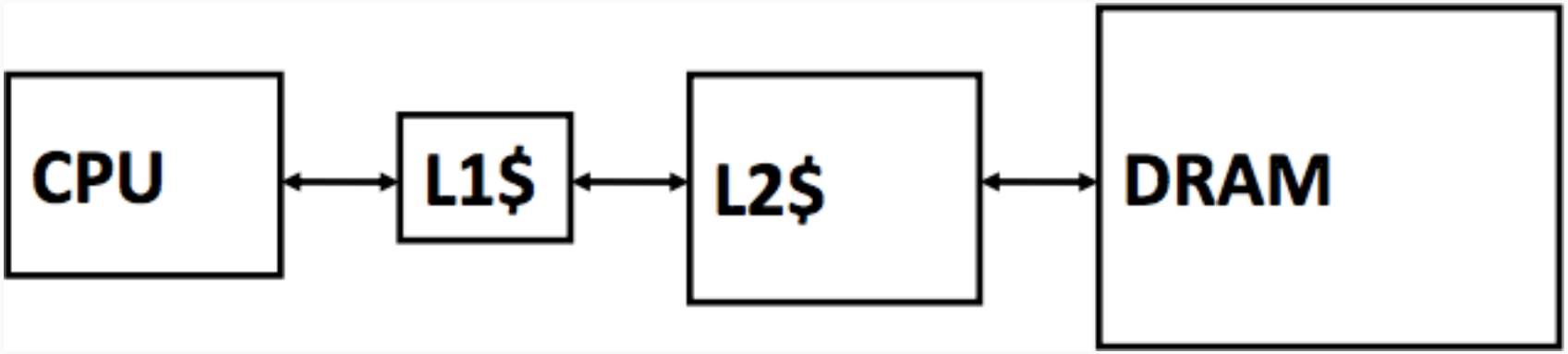
Problem: a memory level cannot be both large and fast

Solution: increasing sizes of cache at each level



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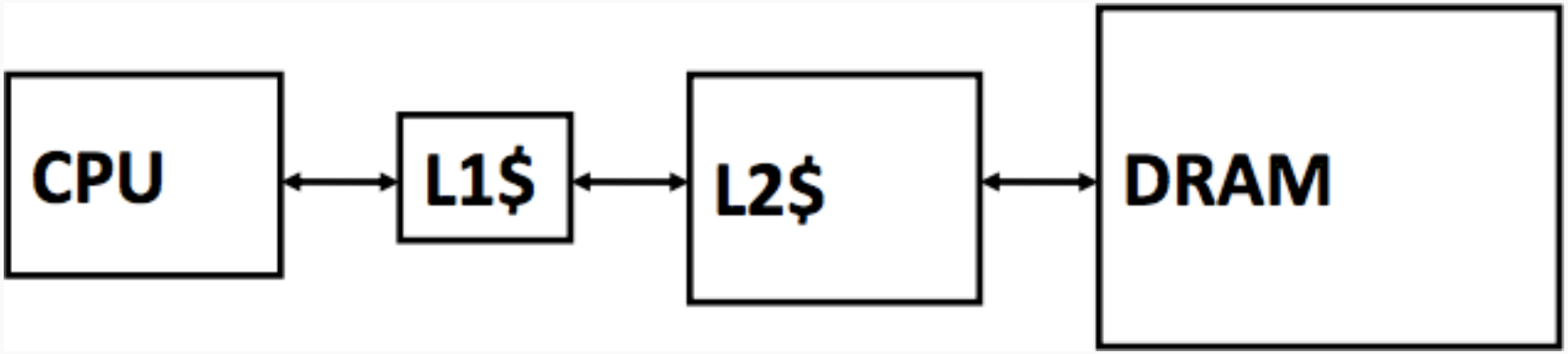

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We can have a smaller L1 if there's also L2

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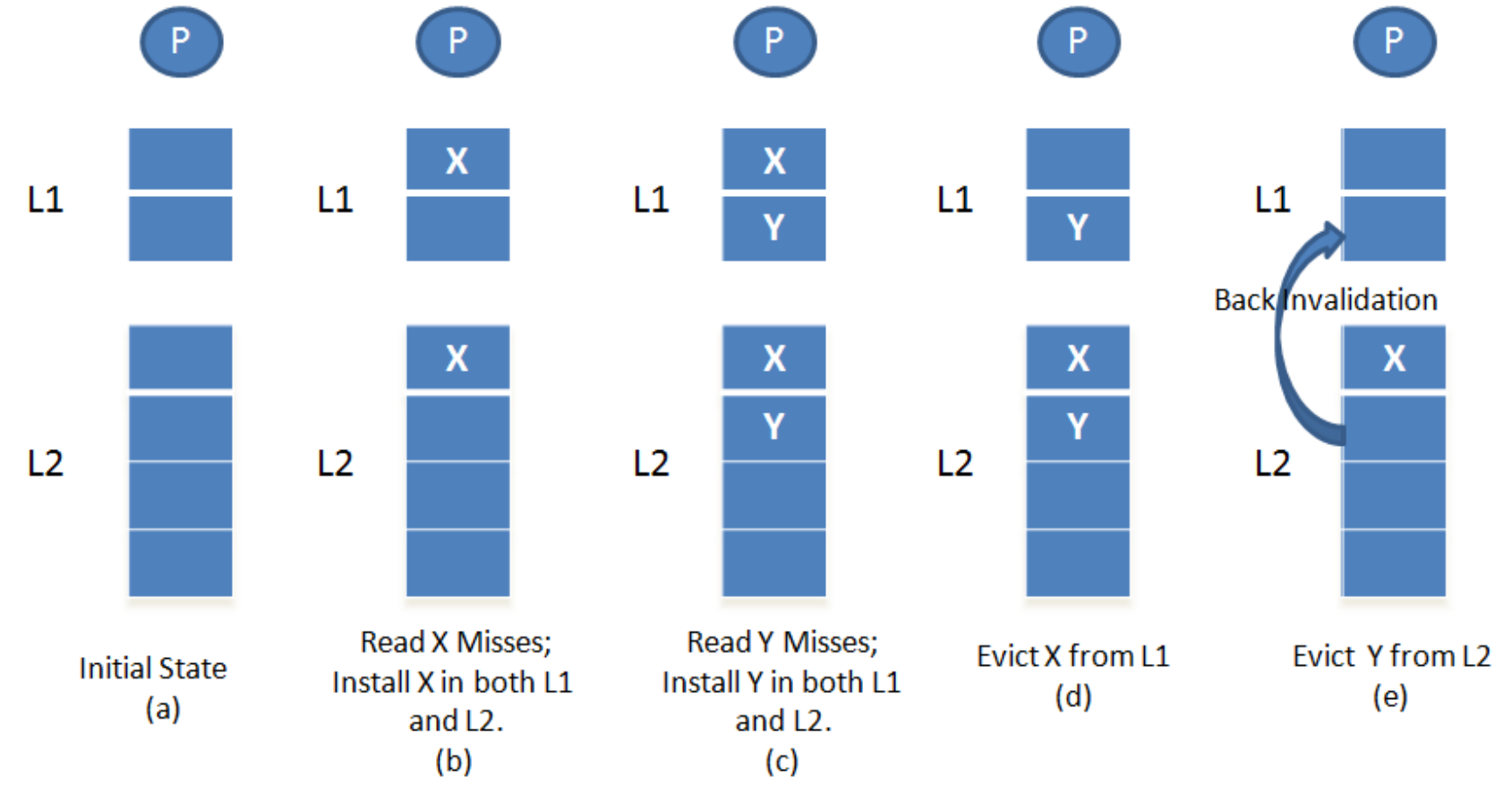
Inclusion Policy: Inclusive

Inclusive multi-level cache: L2 cache holds copies of data in L1 cache



https://en.wikipedia.org/wiki/Cache_Inclusion_Policy

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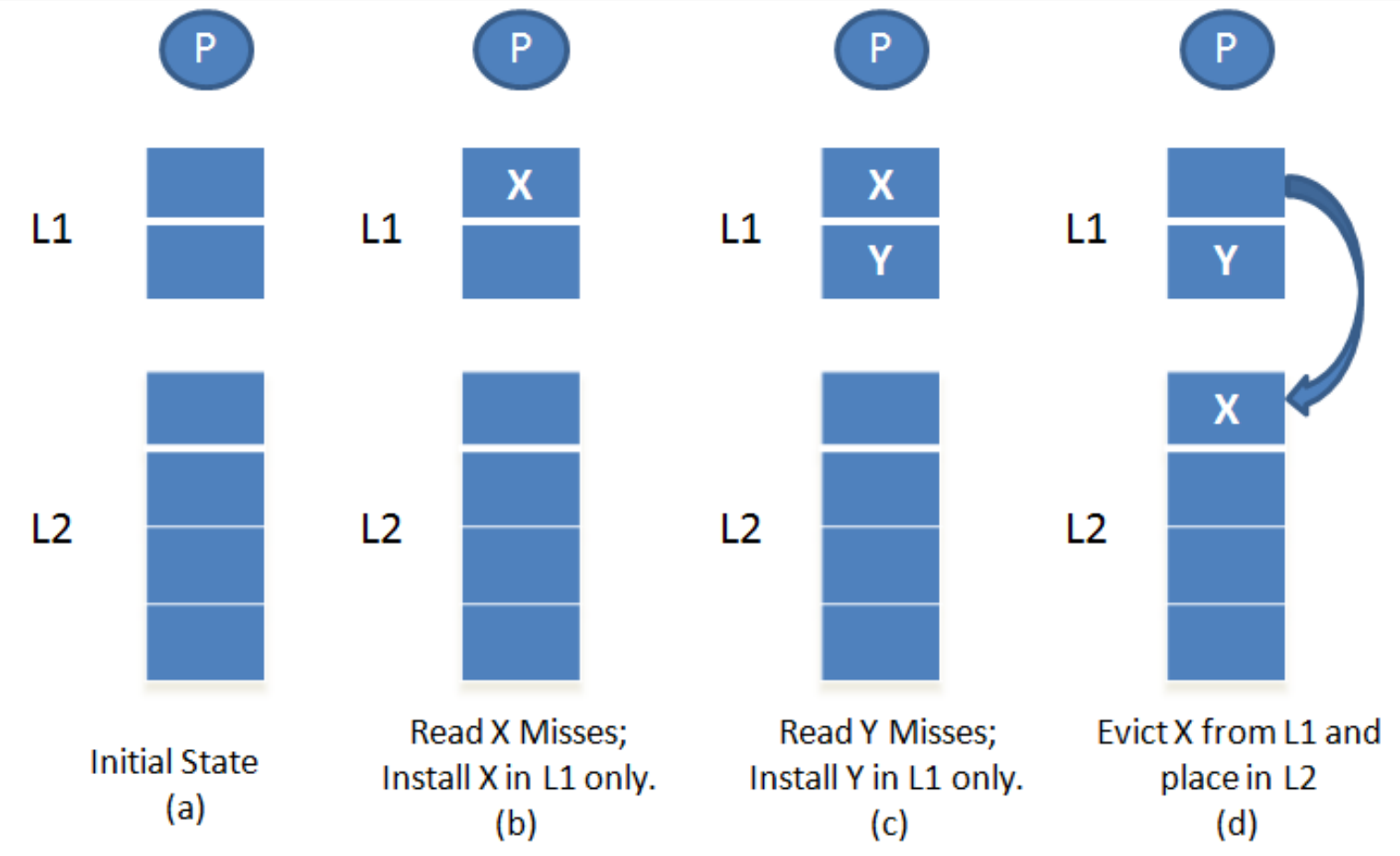

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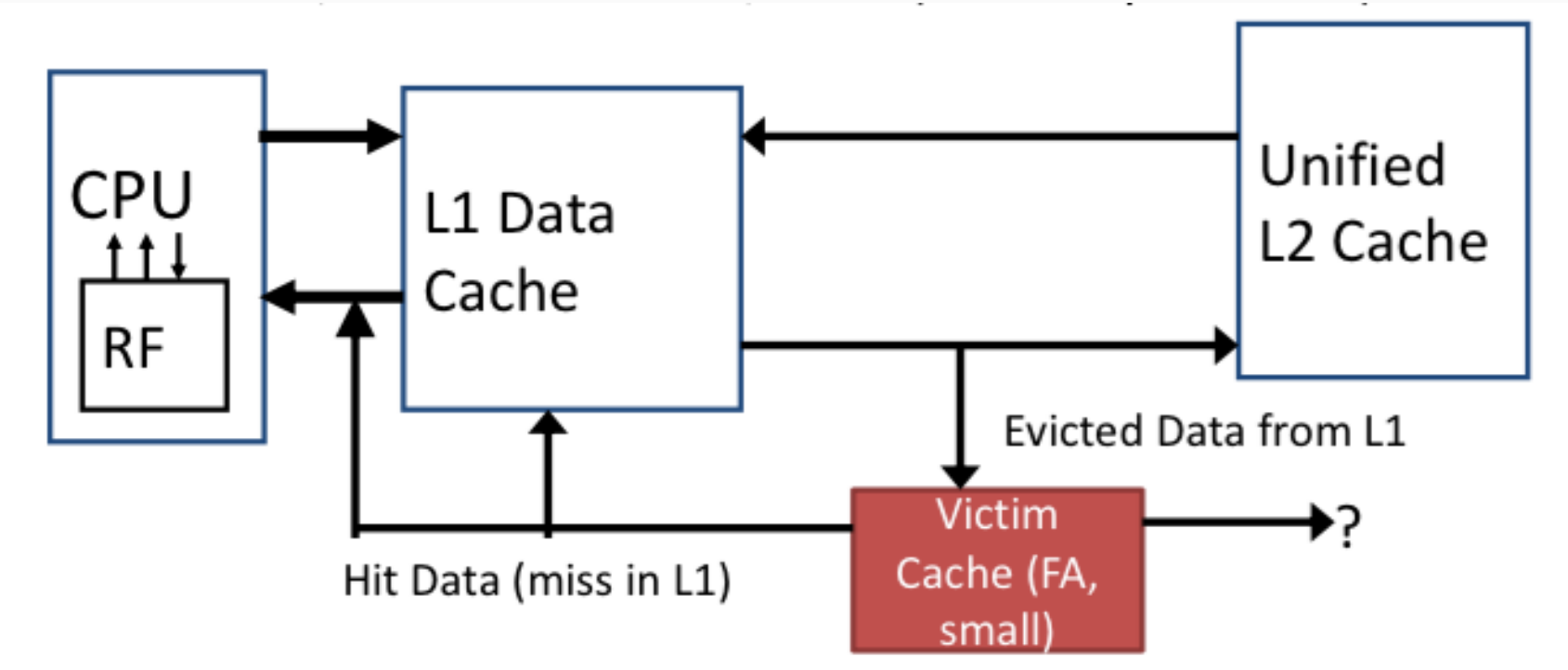
Victim Cache

What happens if the cache is W-way associative, but there are $W + 2$ lines mapped to each set?



Victim cache: `https://en.wikipedia.org/wiki/Victim_cache`

More about Stream buffers, victim cache `https://en.wikipedia.org/wiki/Victim_cache`