Bon Woong Ku

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SUMMARY

EDA R&D engineer with **10+ years** of experience designing **production-grade feasibility, placement, routing, timing, and signoff optimization services** for advanced nodes and advanced multi-die packaging systems. Proven track record of shipping core EDA algorithms used at scale in commercial tools. Recipient of the **Synopsys Technology & Product Development Group Award (2025)** and **IEEE TCAD Donald O. Pederson Best Paper Award (2022)**. Ph.D. with deep expertise spanning PPA optimization and physical design methodologies for 3D ICs, and their neuromorphic applications, interested in building **self-improving chip design systems**.

ACTIVE ROLES

- **DAC 2026** Technical Program Committee member
- **Synopsys 3DIC Compiler** — Lead R&D engineer for advanced multi-die rdl routing

CORE EXPERTISE

Multi-Die & 3D IC Physical Design

Synopsys 3DIC Compiler (2024–present) · Synopsys StarRC (2016) · IMEC (2015–2016) · Georgia Tech Ph.D. (2014–2019)

- Architecting **interposer routing** and **feasibility-aware global optimization**, shipped to 10+ customers with 10× exploration speedup at 3DIC Compiler
- Developed **tier-partitioning algorithms** and full-chip physical design flows for gate-level monolithic 3D ICs at IMEC
- Built **extraction-PDN co-optimization** flows for 3D integration at StarRC
- Created scalable M3D methodologies validated on 10+ designs; developed experimental M3D PDKs at 10nm/7nm for PPA analysis at Georgia Tech

Timing-Driven ECO & Signoff Optimization

Synopsys PrimeTime ECO / PrimeECO / PrimeClosure (2019–2024)

- Shipped **timing-aware ECO legalization** with **timer–router–legalizer co-optimization**, improving QoR by 20% across 10+ customer signoff flows, certified for TSMC N3/N2
- Led signoff timer integration for Tweaker ECO merge

Learning-Guided Physical Design & Neuromorphic Computing

Intel Labs (2019) · Georgia Tech Ph.D. (2014–2019)

- Automate standard cell routing at advanced Intel nodes, replacing manual heuristics with **reinforcement learning** at Intel microarchitecture group
- Built **C++ MPI-based parallel spiking neural network simulators** on Oak Ridge supercomputing infrastructure
- Designed **3D neuromorphic accelerators** and **RISC-V gate-level M3D systems** for emerging memory technologies at DARPA CHIPS project

Skills

- **C/C++:** production EDA engines — placement, routing, legalization, parasitic extraction, signoff optimization
- **Tcl/Shell:** EDA flow integration, customer-facing scripting (PrimeSuite, 3DIC Compiler)
- **Rust:** systems programming for next-generation EDA tooling
- **Python / PyTorch:** ML pipelines, design automation for physical design

ACHIEVEMENTS

Honors

- **Technology & Product Development Group Award** — Shankar Krishnamoorthy (CPDO, Synopsys, 2025)
- **Donald O. Pederson Best Paper Award** — IEEE TCAD (2022)
- **Team Award** — Jacob Avidan (SVP, Synopsys, 2022)
- **Customer Success Award** — Jacob Avidan (SVP, Synopsys, 2021)
- **Contribution Award** — Jacob Avidan (SVP, Synopsys, 2021)
- **Signoff Platform & Innovation Recognition Award** — Jacob Avidan (SVP, Synopsys, 2020)
- **Best Paper Award Nomination** — ACM ISPD (2018)
- **Presidential Science Scholarship** — Korea Student Aid Foundation (2008–2014)

Patent

- **B. W. Ku**, N. Oh, C. Moon. “Timing-aware Surgical Optimization for Engineering Change Order in Chip Design.” U.S. Patent No. 12,175,181, granted Dec. 2024.

Selected Publications

26 total publications · 6 papers at DAC/ICCAD · full list upon request

- **B. W. Ku**, K. Chang, S. K. Lim, “Compact-2D: A Physical Design Methodology to Build Two-Tier Gate-level 3D ICs,” **IEEE TCAD**, 2020 — *Donald O. Pederson Best Paper Award*
- **B. W. Ku**, K. Chang, S. K. Lim, “Compact-2D: A Physical Design Methodology to Build Commercial-Quality Face-to-Face-Bonded 3D ICs,” **ISPD**, 2018 — *Best Paper Nomination*
- **B. W. Ku**, Y. Liu, Y. Jin, S. Samal, P. Li, S. K. Lim, “Design and Architectural Co-optimization of Monolithic 3D Liquid State Machine-based Neuromorphic Processor,” **DAC**, 2018

EDUCATION

Georgia Institute of Technology — Ph.D. & M.S., Electrical and Computer Engineering, 2019
Thesis: Physical Design Solutions for 3D ICs and their Neuromorphic Applications

Seoul National University — B.S., Electrical and Computer Engineering, 2014