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Summary

EDA algorithm engineer with **10+ years** of experience designing **production-grade placement, routing, timing, and signoff optimization systems** for advanced nodes and 3D ICs. Proven track record of shipping core algorithms used at scale in commercial tools and applying machine learning to augment or replace heuristic design loops. Ph.D. with deep expertise spanning **PPA optimization, signoff closure, and ML-driven physical design**, interested in building **self-improving chip design systems**.

Core expertise

- **EDA algorithms & systems:** placement, routing, legalization, timing closure, physical ECO, signoff flows (EM/IR, DRC/LVS), RC extraction
- **Optimization methods:** heuristic search, co-optimization loops, experiment design & QoR evaluation, ML-guided physical design (CNN/RNN, surrogate modeling)
- **Software engineering:** performance-critical C/C++; Python automation; Rust; Tcl/Shell in EDA environments

Experience

Synopsys — PrimeTime ECO / PrimeECO / PrimeClosure

Senior Staff R&D Engineer · Mountain View, CA · *Aug 2019 – Present*
Focus: Timing-driven physical ECO and signoff optimization at scale

- Designed and shipped **timing-aware ECO placement and legalization algorithms** integrated with commercial signoff flows.
- Built **co-optimized timer–router–legalizer loops** improving timing QoR while maintaining legality.
- Developed **surgical wire ECO optimization** techniques for noise and timing closure in post-route signoff stages.
- Led algorithm work from concept → production, impacting large-scale customer designs.
- **Patent:** signoff timing-aware surgical wire optimization for ECO.

Keywords: timing closure, heuristic optimization, production EDA, large-scale design systems

Intel Labs — Microarchitecture Research Lab

Research Intern · Santa Clara, CA · *Jan 2019 – Apr 2019*
Focus: ML-driven routing automation

- Applied **deep learning (CNN, RNN)** to automate routing decisions in advanced Intel technology nodes.
- Designed feature extraction and evaluation pipelines to reduce or replace manual routing heuristics.
- Demonstrated feasibility of **learning-guided routing optimization** using PyTorch on real design data.

Keywords: ML for EDA, routing automation, learned heuristics

Synopsys — StarRC

Research Intern · Mountain View, CA · *May 2016 – Aug 2016*

- Developed transistor-level parasitic extraction and power integrity flows for monolithic 3D ICs.
- Explored co-optimization of RC extraction and PDN design for emerging integration technologies.

IMEC — Design Technology Exploration Team

Research Intern · Leuven, Belgium · *Jun 2015 – Apr 2016*

- Developed full-chip physical design flows and tier-partitioning algorithms for gate-level monolithic 3D ICs.
- Evaluated PPA-cost tradeoffs at 10nm and 7nm using experimental PDKs.

Research

Georgia Institute of Technology — GTCAD Lab

Ph.D. Research Assistant · Atlanta, GA · *Aug 2014 – May 2019*
Thesis: Physical Design Solutions for 3D ICs and their Neuromorphic Applications

- Designed scalable physical design methodologies for monolithic 3D ICs across logic, memory, and heterogeneous systems.
- Built C++ MPI-based large-scale spiking neural network simulators on supercomputing infrastructure (Oak Ridge).
- Co-designed architecture + physical design for 3D neuromorphic accelerators.
- Developed RISC-V-based gate-level M3D systems targeting emerging memory and device technologies.

Education

Georgia Institute of Technology — Ph.D. & M.S., Electrical and Computer Engineering

- IEEE TCAD Donald O. Pederson Best Paper Award (2022)
- 26 publications (8 top-tier conferences/journals)

Seoul National University — B.S., Electrical and Computer Engineering

Honors

- Donald O. Pederson Best Paper Award — IEEE TCAD (2022)
- Customer Success Award — Synopsys (Q4 FY21)
- Signoff Platform & Innovation Recognition Award — Synopsys (Q4 FY20)
- Best Paper Award Nomination — ACM ISPD (2018)
- Presidential Science Scholarship — Korea Student Aid Foundation (2008–2014)

Patent

- Bon Woong Ku, Nahmsuk Oh, Cho Moon, “Signoff Timing-aware Surgical Wire Optimization for Engineering Change Orders,” App No. 63/121,853.

Selected publications

(Full list available upon request.)

- “Compact-2D: A Physical Design Methodology to Build Two-Tier Gate-level 3D ICs,” **IEEE TCAD** (Best Paper Award)
- “ML-based Wire RC Prediction in Monolithic 3D ICs with an Application to Full-Chip Optimization,” **ISPD**
- “RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs,” **DAC**
- “Machine Learning Integrated Pseudo-3D Flow for Monolithic 3D ICs,” **IEEE JXCDC**