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Summary

EDA algorithm engineer with **10+ years** of experience designing **production-grade placement, routing, timing, and signoff optimization systems** for advanced nodes and 3D ICs.

Experience

Synopsys — PrimeTime ECO / PrimeECO / PrimeClosure

- Designed and shipped timing-aware ECO placement and legalization algorithms integrated with commercial signoff flows.

Intel Labs — Microarchitecture Research Lab

- Applied deep learning (CNN, RNN) to automate routing decisions in advanced Intel technology nodes.

Education

- Georgia Institute of Technology — Ph.D. & M.S., ECE
- Seoul National University — B.S., ECE