集成电路工艺原理

上海电力大学

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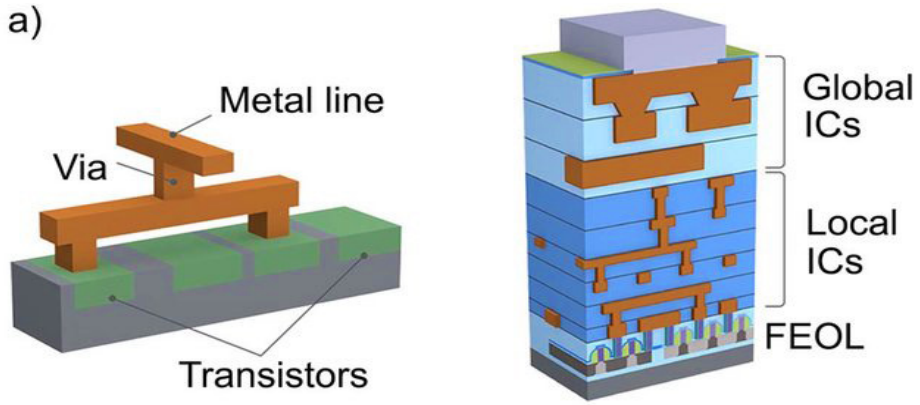
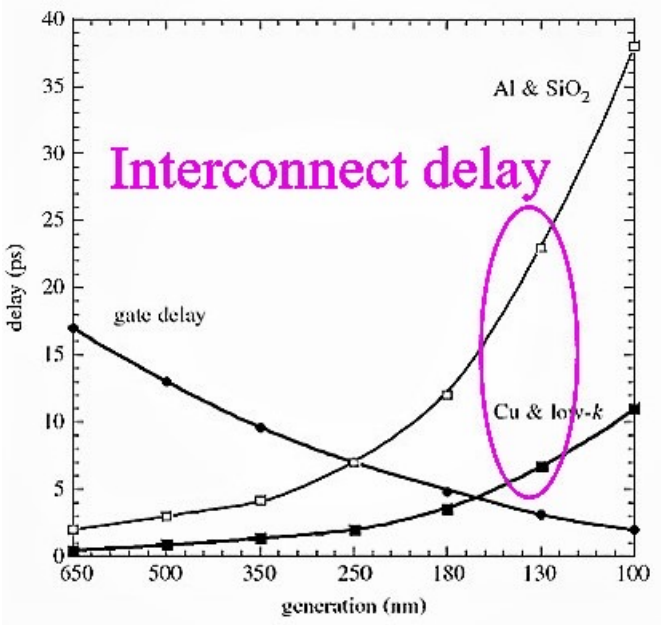
第九章 后端工艺

引言



集成电路结构示意图



互连延迟与晶体管栅极延迟比较

- 随着工艺技术节点的推进，晶体管的尺寸在不断缩小。单位面积上晶粒管数量在增加，使得互连线的长度与结构复杂性在不断增加。
- 互连延迟远远超过晶体管栅极延迟，已经成为影响芯片性能提升的瓶颈。

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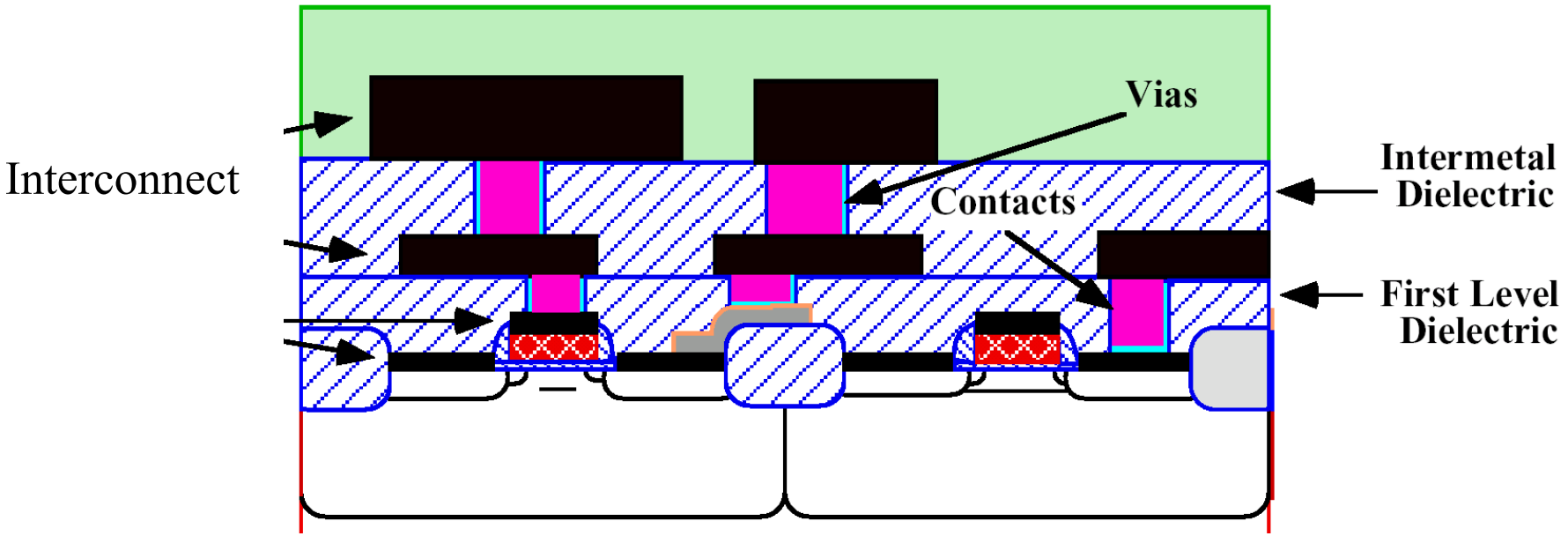
1．概述

后端工艺 backend of line technology (BEOL) ——

将器件连接成特定的电路结构：互连线及介质制作，使得金属线在电学和物理上均被介质隔离。



通孔(via)—用于连接不同层的金属连线；金属间介质(IMD)；

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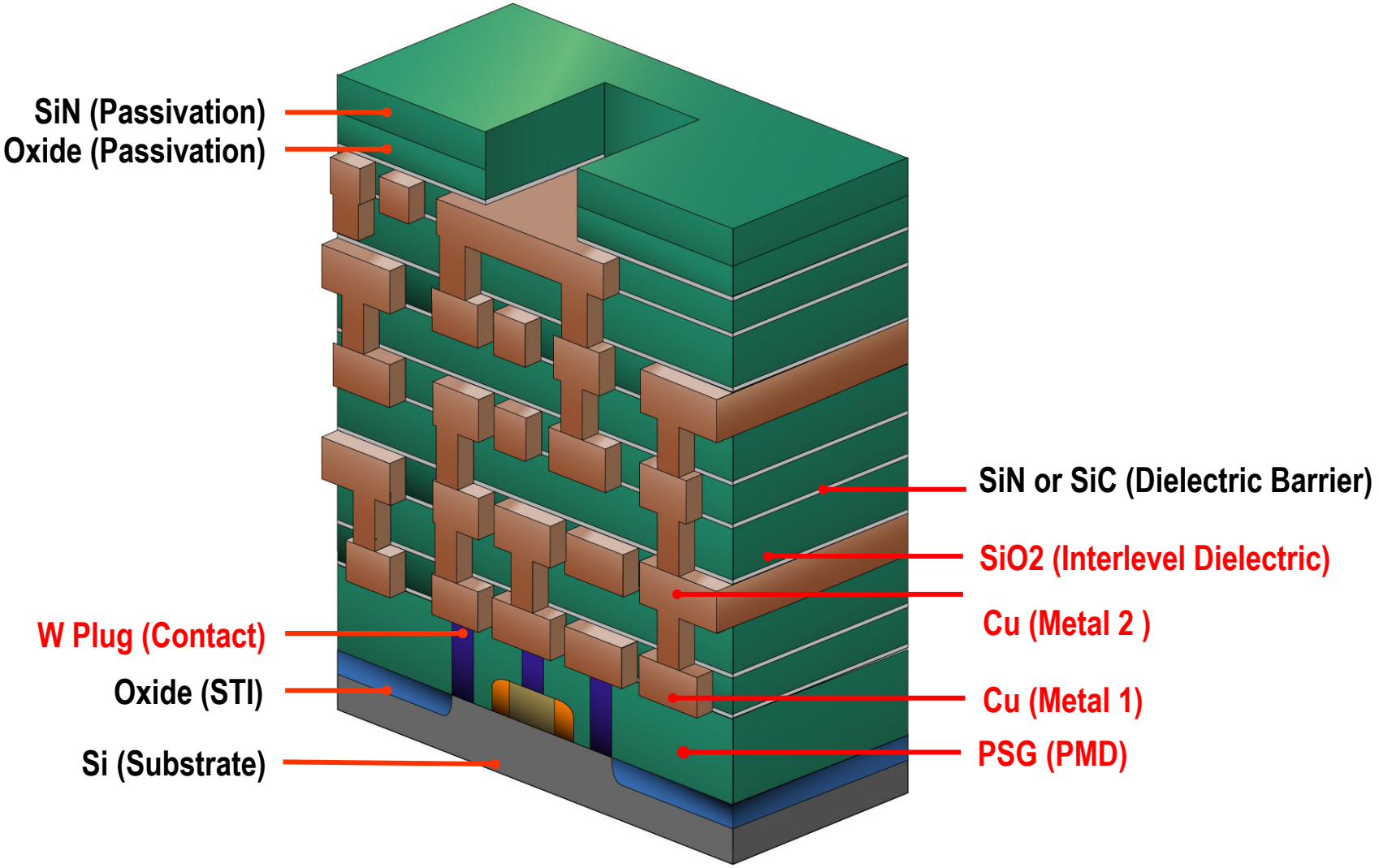

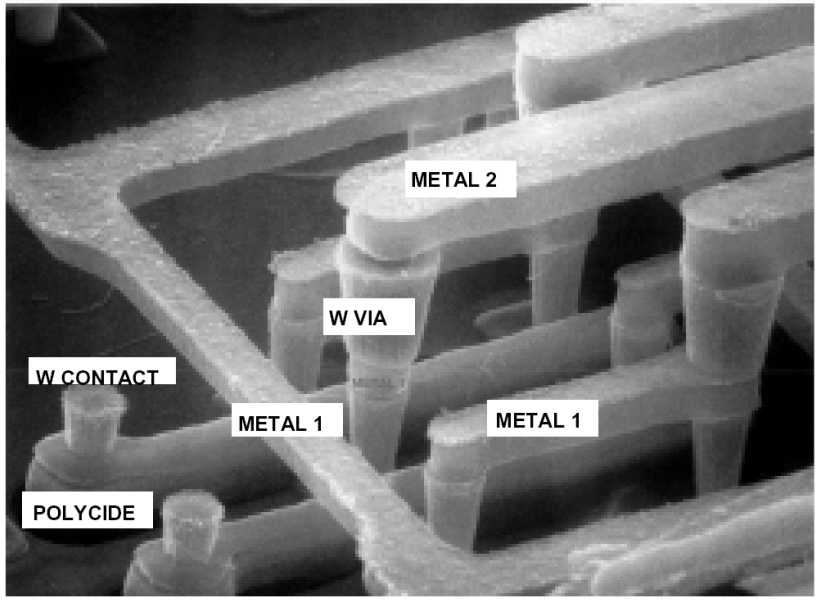

multilayer interconnect

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- 后端工艺越来越重要
- 占了工艺步骤中大部分
- 影响IC芯片的速度

国际半导体技术路线图的预测

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Number of metal levels	**13**	**13**	**13**	**14**	**14**	**14**	**14**
Number of optional levels – ground planes/capacitors	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	**3571**	**4000**	**4545**	**5000**	**5555**	**6250**	**7143**

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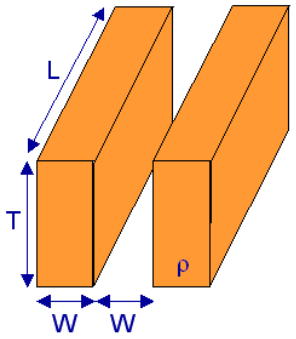
$$R = \rho \frac{L}{WT}$$

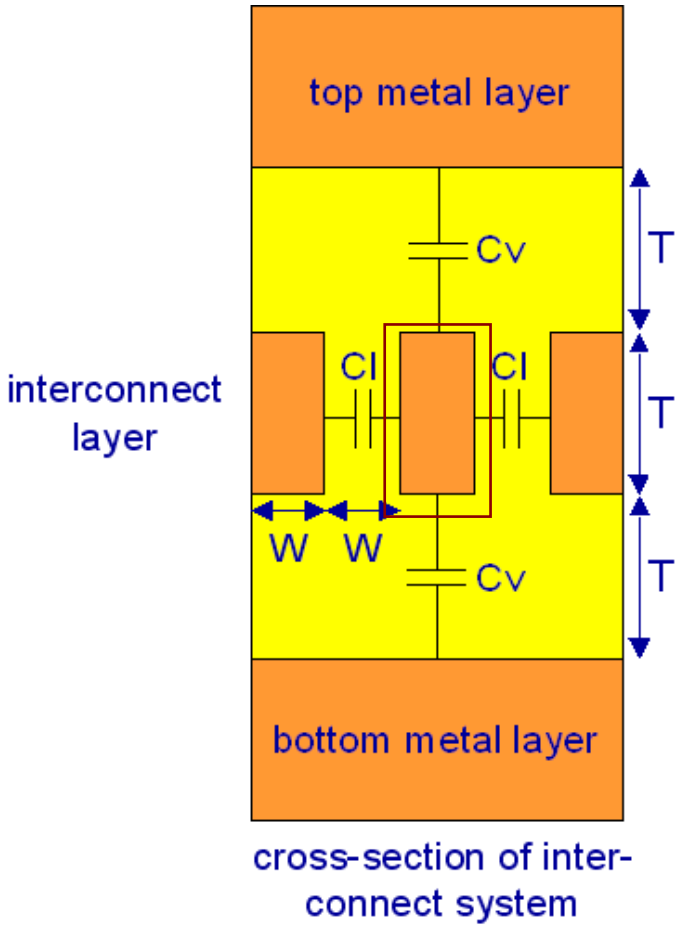
$$C_l = k\varepsilon_0 \frac{LT}{W} \qquad (Interline\ C)$$

$$C_v = k\varepsilon_0 \frac{LW}{T} \qquad (Interlevel\ C)$$

$$C = 2(C_v + C_l) = 2k\varepsilon_0 LTW\left(\frac{1}{W^2} + \frac{1}{T^2}\right)$$

$$RC\ delay = 2\rho k\varepsilon_0 L^2\left(\frac{1}{W^2} + \frac{1}{T^2}\right)$$





interconnect layer

cross-section of inter-connect system

降低RC延迟：降低寄生电容，降低互连电阻。

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介质层(inter-metal dielectric)： SiO_2－CVD (SiH_4源)、PECVD SiO_2(TEOS) 、Si_3N_4…

低介电常数材料必须满足诸多条件，例如：

- ✓足够的机械强度以支撑多层连线的架构
- ✓高击穿电压(>4 MV/cm)
- ✓低漏电(<10^{-9} A/cm^2 at 1 MV/cm)
- ✓高热稳定性(>450 ºC)
- ✓良好的粘合强度
- ✓低吸水性
- ✓低薄膜应力
- ✓高平坦化能力
- ✓与化学机械抛光工艺的兼容性等等

Low-k integration

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介质层(inter-metal dielectric)

low k

Material Classification	Material	*k* value	Deposition Method
Inorganic	Fluorinated glass (SiOF)	2.8	CVD
	SiCOH	2.8/2.3	PECVD
	Hydrogen silesquioxane (HSQ)	2.9	SOD
Inorganic/Organic Hybrid	Si-O-C polymers (e.g. MSQ)	2.0	SOD
Organic	Poly(arylene ether) PAE	2.6	SOD
	Polyimides / Flourinated	2.9 / 2.3	SOD
	Parylene-N / Parylene-F	2.7 / 2.4	CVD
	B-stage polymers（SiLK）	2.6	SOD
	DLC-Diamond-like Carbon / Fourinated	2.7 / 2.4	CVD
	Amorphous C / Flourinated	2.0	CVD
	PTFE (Teflon)	1.9	SOD
Porous	Porous MSQ	1.8	SOD
	Porous PAE	1.8	SOD
	Porous SiLK	1.5	SOD
	Porous SiO2	1.1	SOD
Air gaps/bridges		1.0	???

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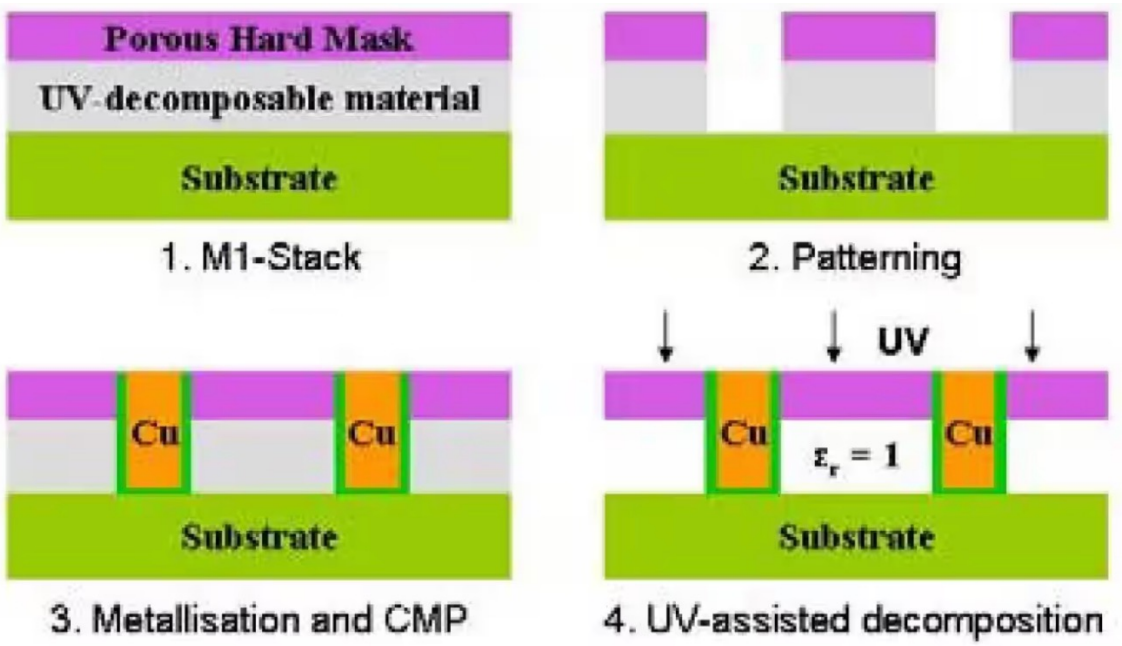

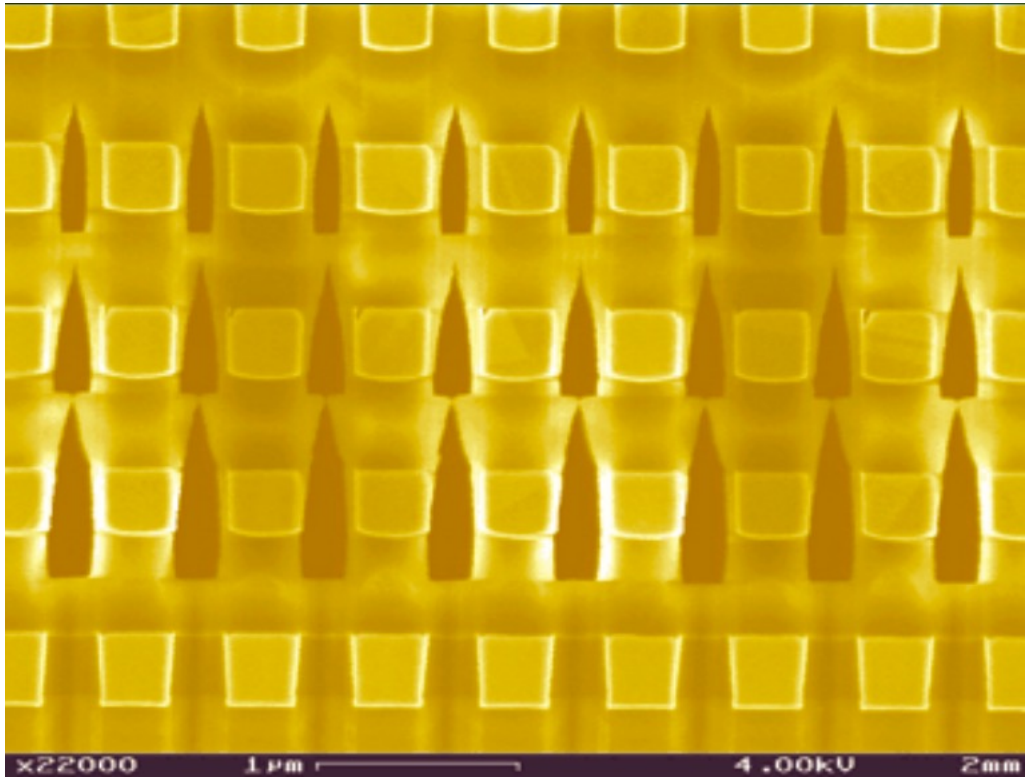

32工艺5层互连线结构

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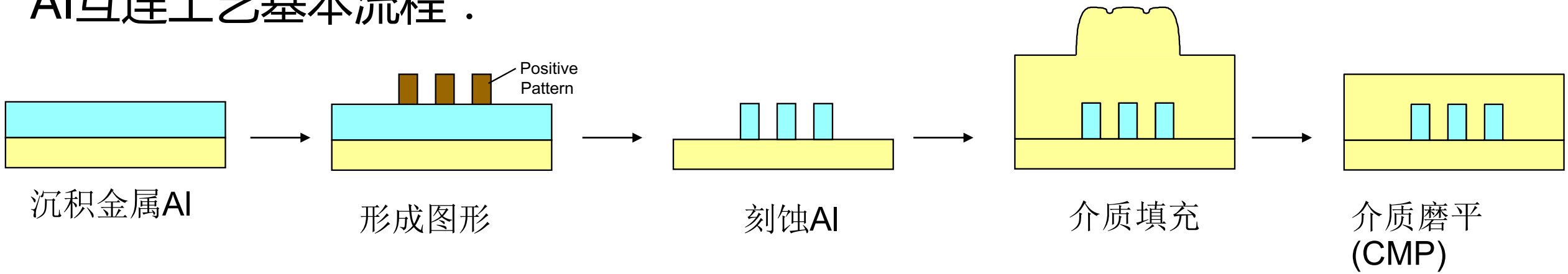
互连线

最早使用的是铝互连，优点包括：

1. 与SiO2粘附性好；
2. 价格便宜，电阻率较低（2.7 μΩ·cm）；
3. 刻蚀铝的工艺简单（干法/湿法）；
4. 沉积铝的工艺简单（CVD/PVD）；

Al互连工艺基本流程：



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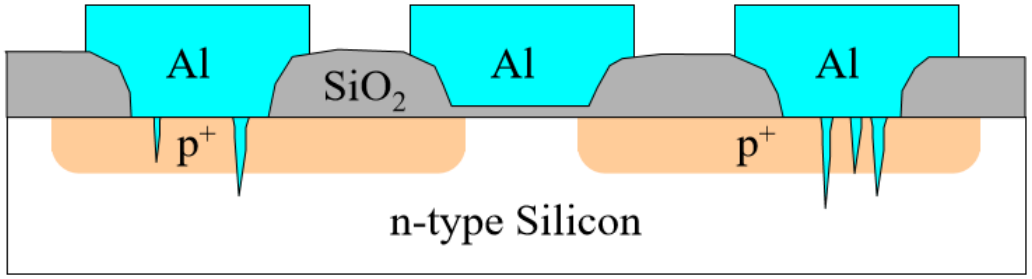
Al互连存在的问题：

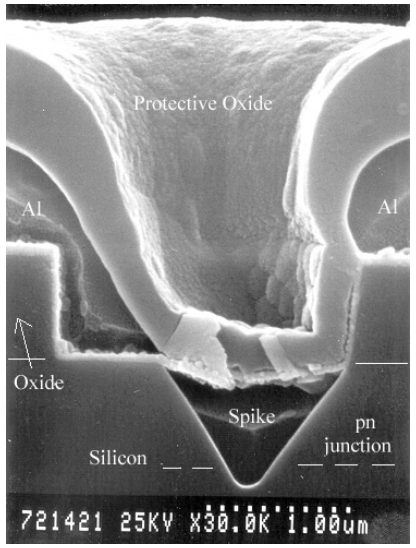
1. Al和Si会发生互扩散，Al穿过有源区进入衬底；

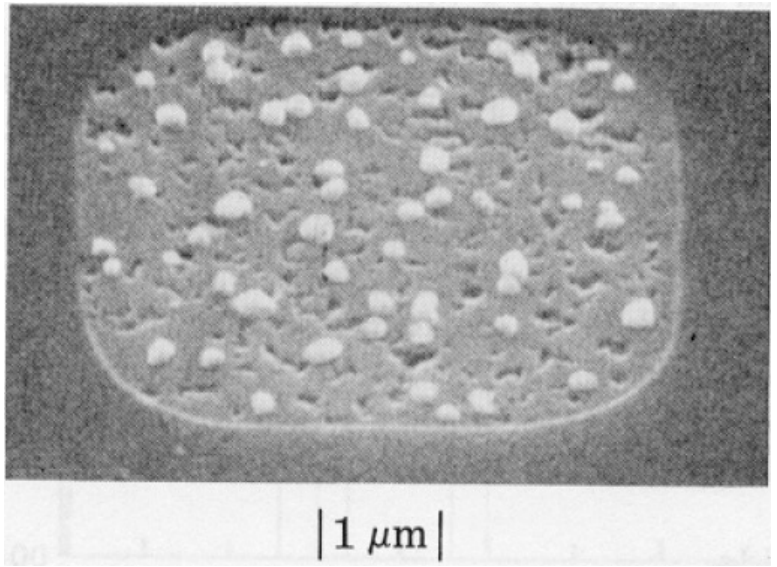
2. Al容易发生电迁移而形成空洞，断线问题。

硅和铝在退火温度下(400-500 °C)，硅在铝中的固溶度较高(固溶度随温度呈指数增长)，会造成严重的尖楔现象。



铝尖楔





铝尖楔SEM照片

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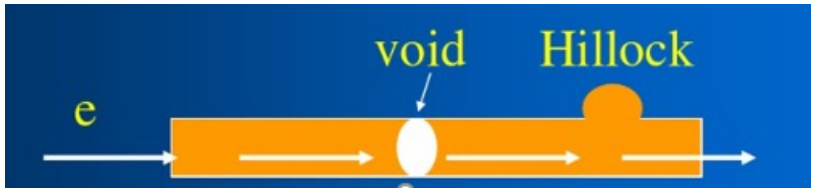
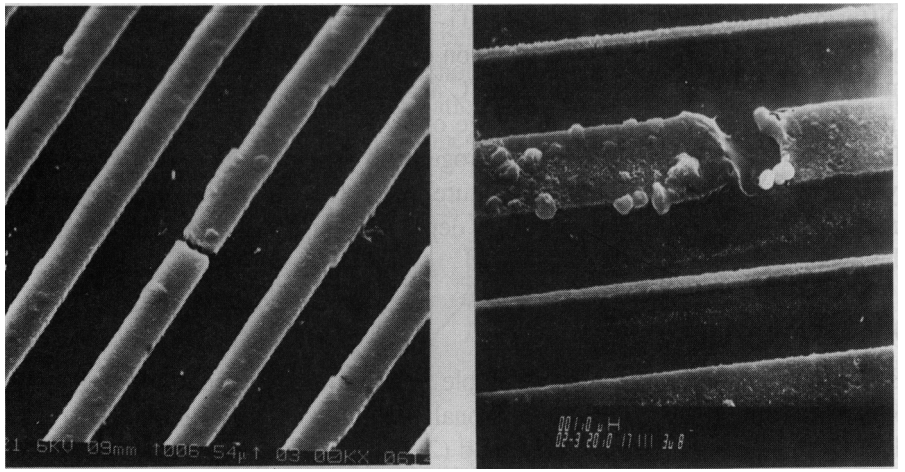
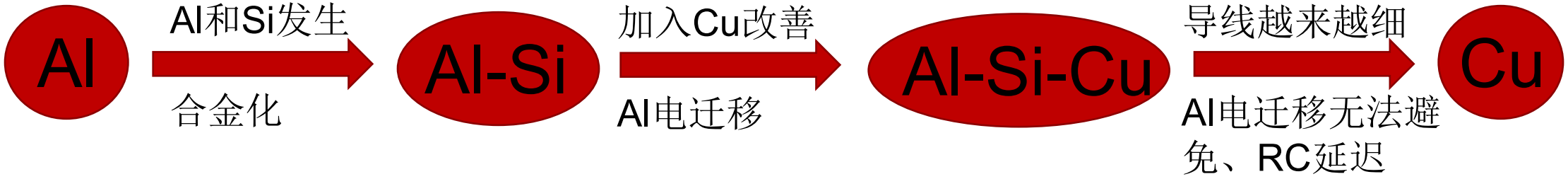
电迁移：当大密度电流流过金属薄膜时，具有大动量的导电电子将与金属原子发生动量交换，使金属原子沿电子流的方向迁移，这种现象称为金属电迁移。电迁移会使金属空位积聚而形成空洞，导致电路开路。



电迁移



电迁移断线



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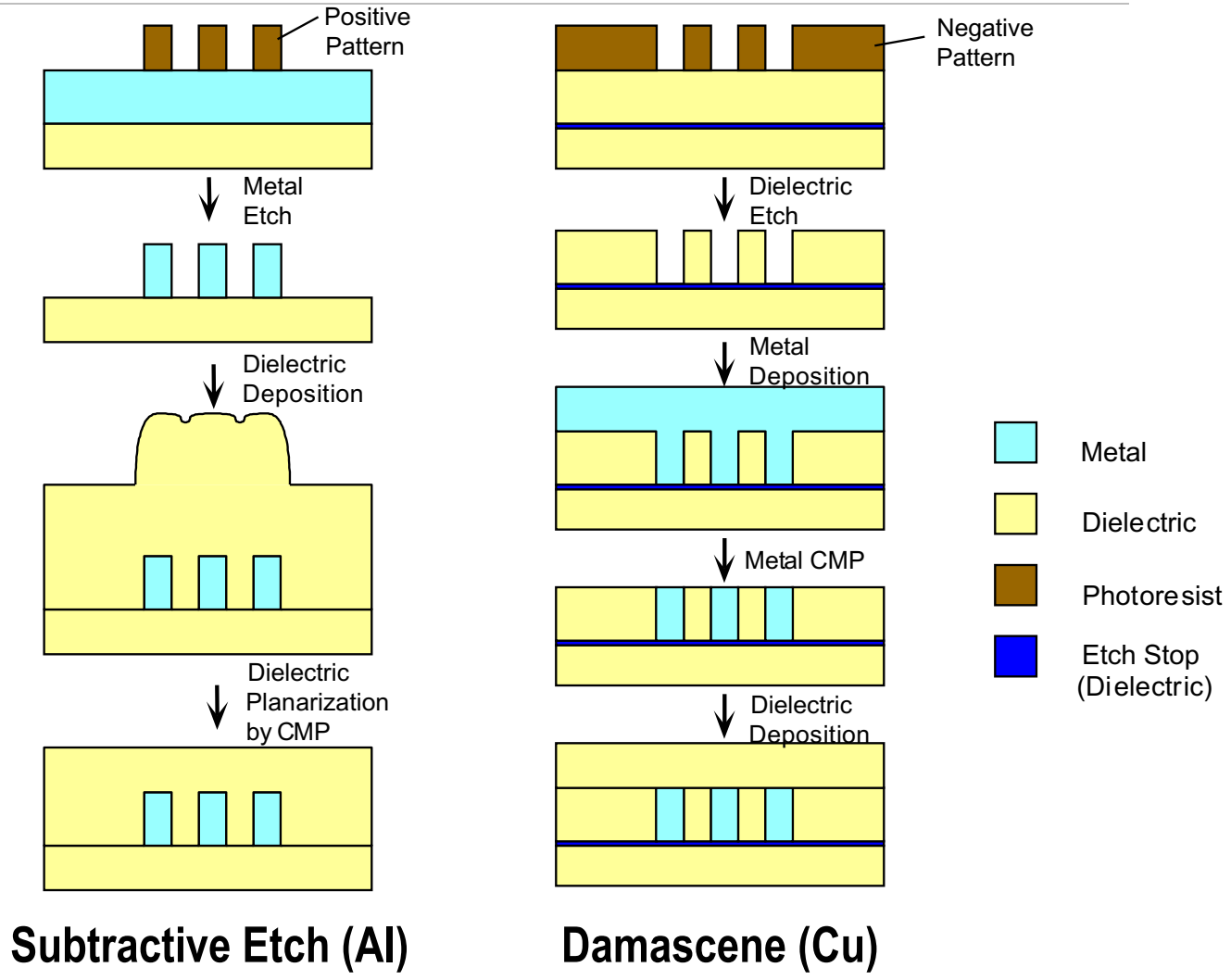
铜互连技术优点：

1. Cu的电阻率为1.7 μΩ·cm（Al的电阻率为2.7μΩ·cm），比Al降低了约37%，可以显著减小RC延迟；

2. Cu具有更强的抗电迁移能力。

铜互连技术：

被称为镶嵌工艺，源自Damascene一词。衍生自古代的Damascus工匠之嵌刻技术，故亦称为大马士革技术。



Al刻蚀工艺与Cu镶嵌工艺的比较

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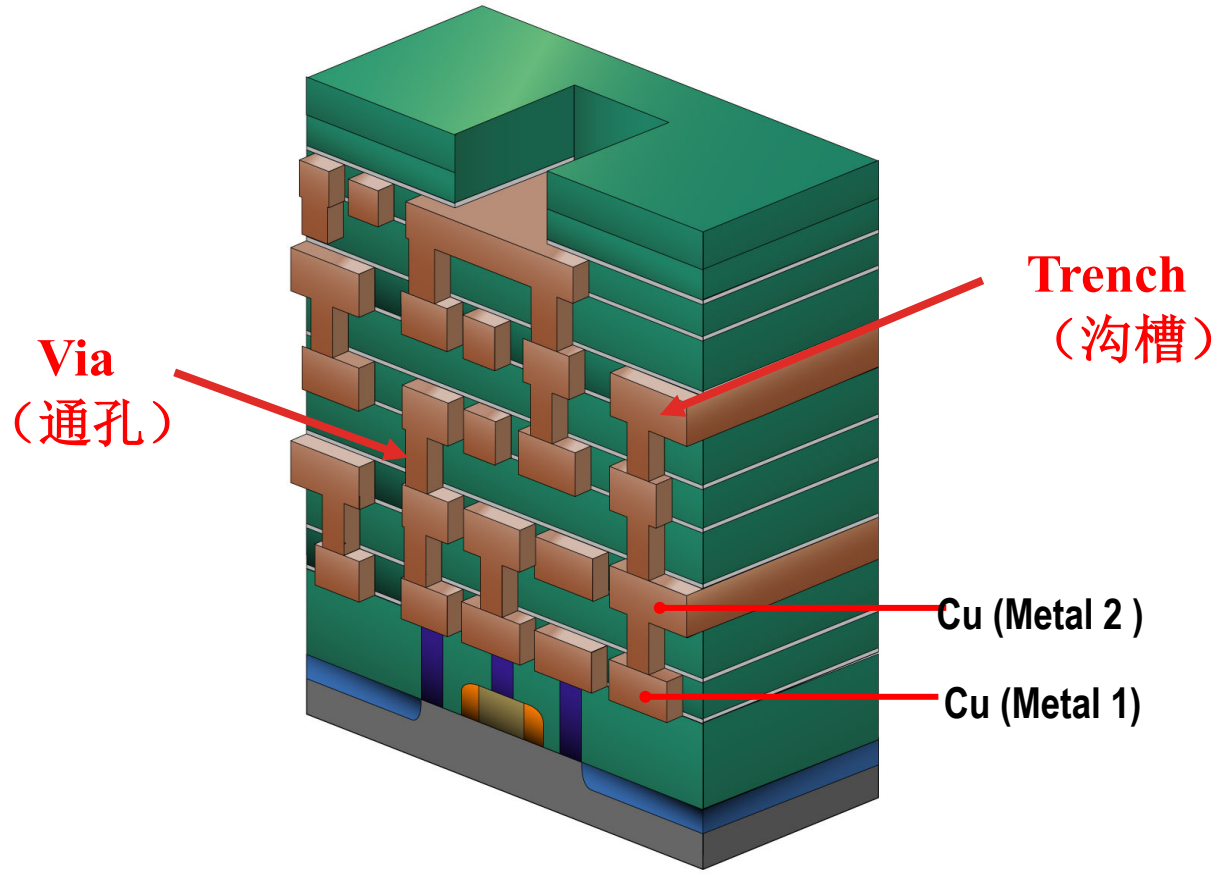
Cu单镶嵌工艺（Single Damascene): Metal 1

Cu双镶嵌工艺（Dual Damascene): Metal 1以上

通孔优先双镶嵌工艺

沟槽优先双镶嵌工艺



Materials for multilayer interconnection

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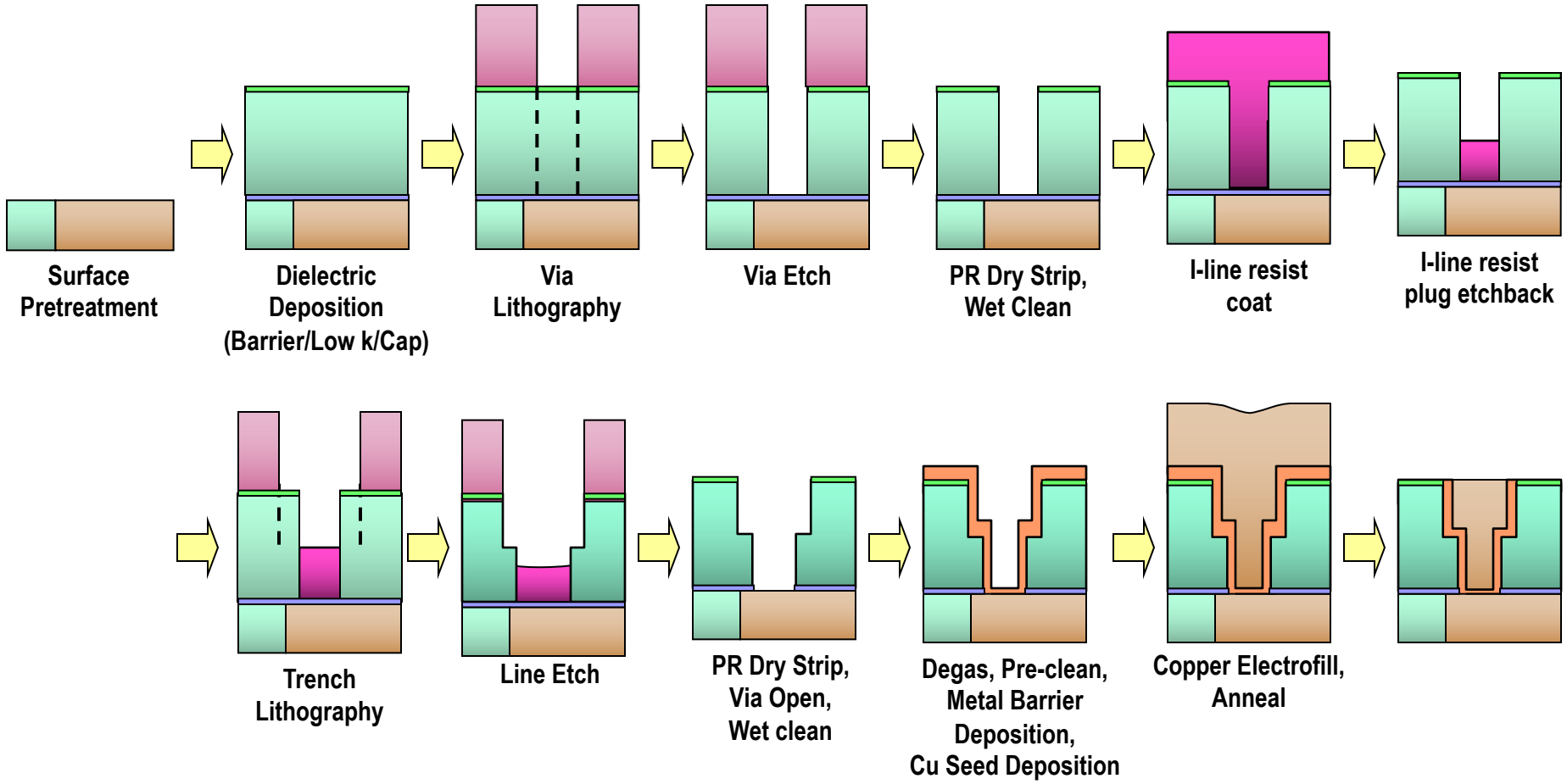

通孔优先双镶嵌工艺主要步骤

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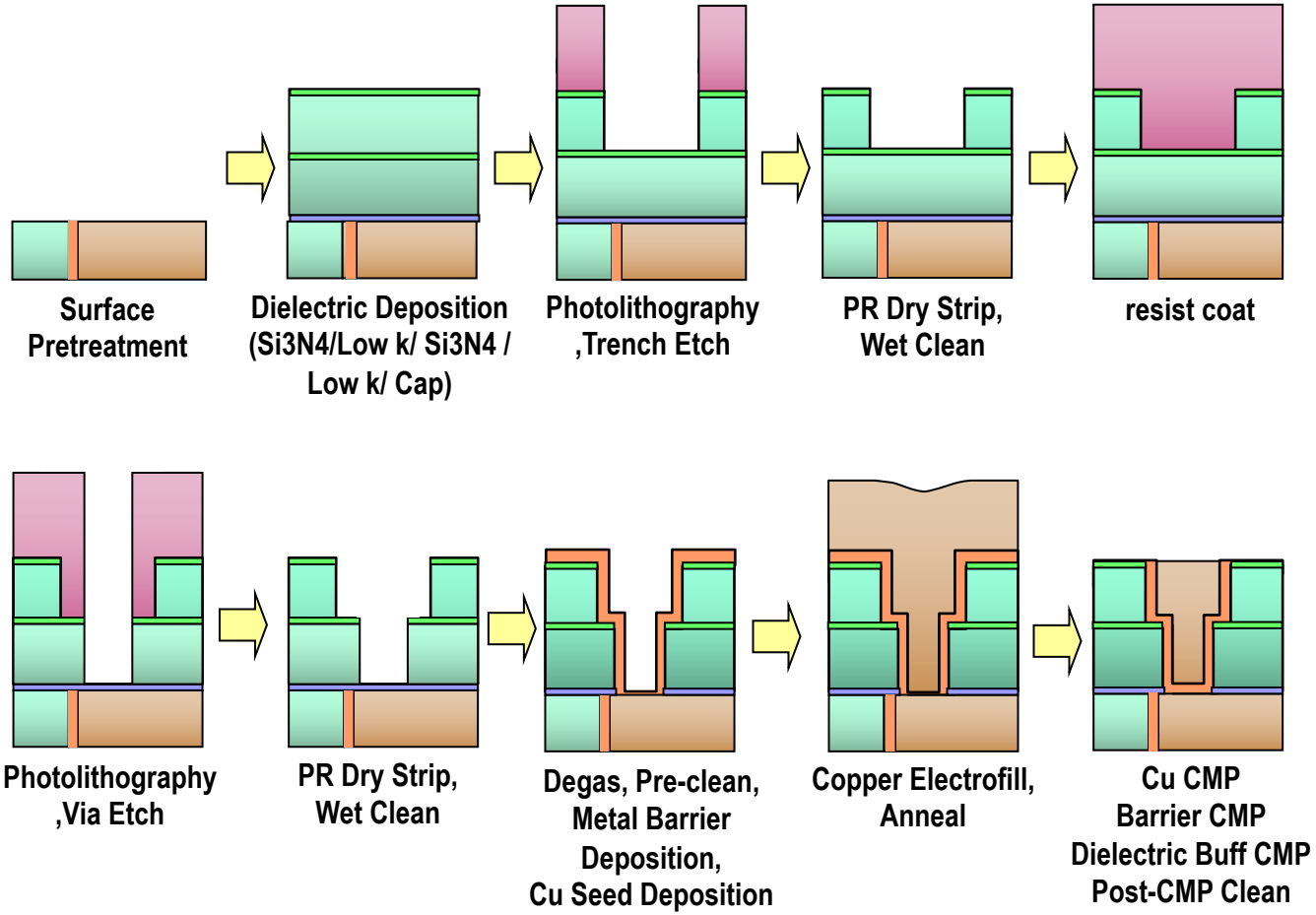

沟槽优先双镶嵌工艺主要步骤

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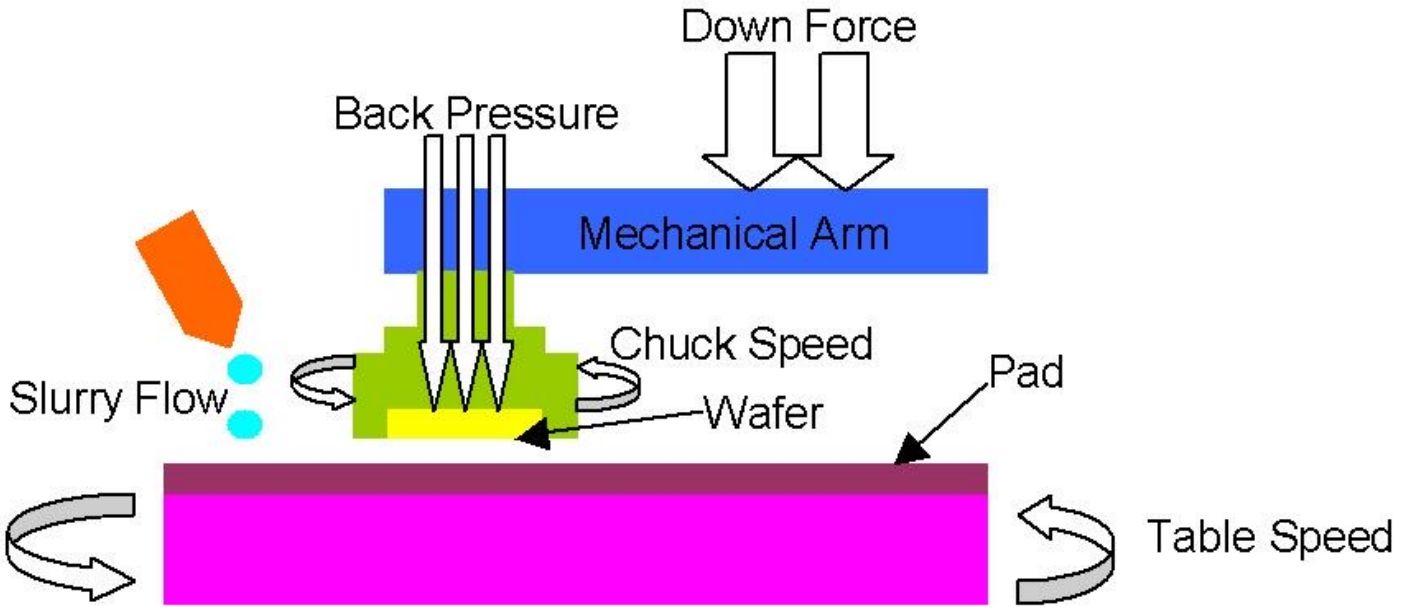
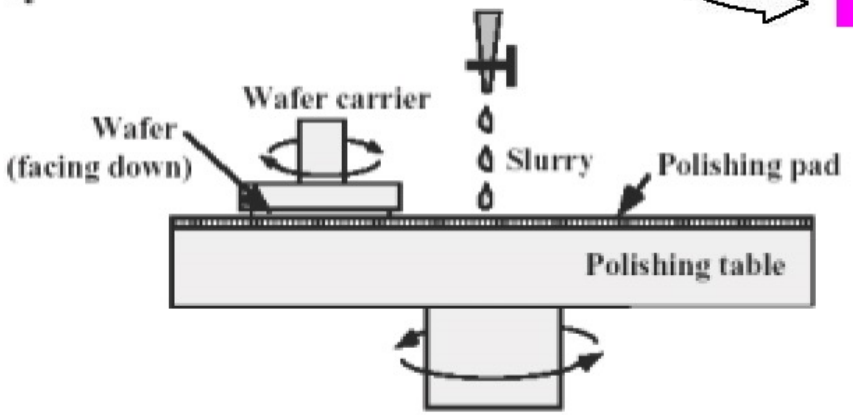
CMP





Slurry非常重要——选择性

三个关键硬件：

✓Polishing pad

✓Wafer carrier

✓Slurry dispenser

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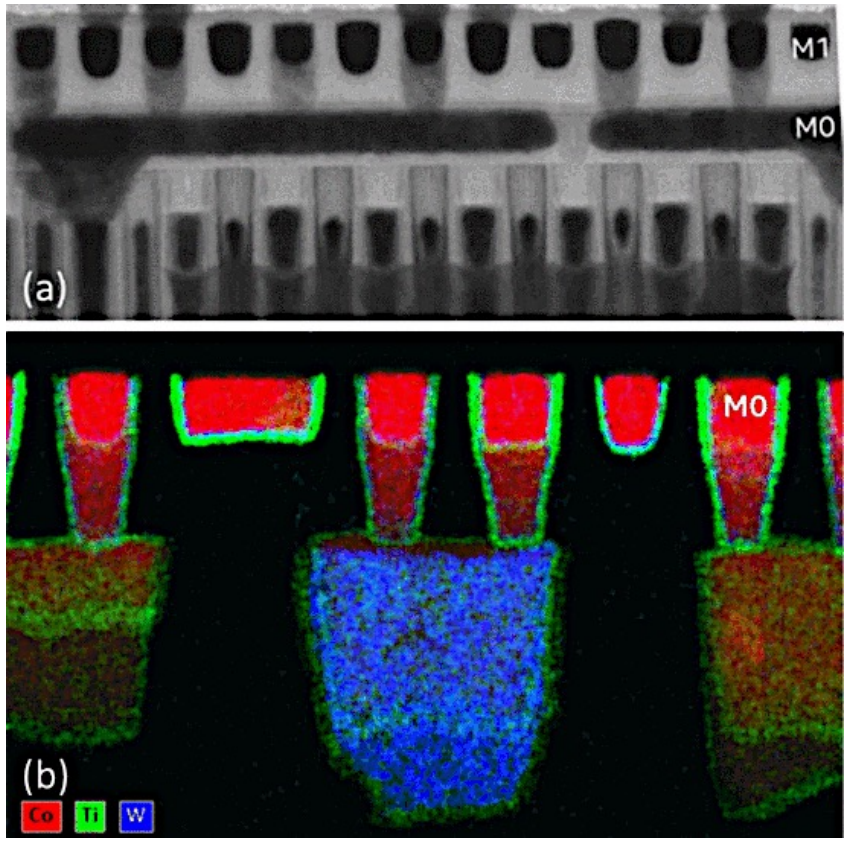
拓展文献阅读：钴互连技术



Intel在10 nm技术中引入Co互连[1]

[1]Auth C, Aliyarukunju A, Asoro M, et al. A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects[C]. 2017 IEEE International Electron Devices Meeting (IEDM), 2017: 29.1.1-29.1.4.

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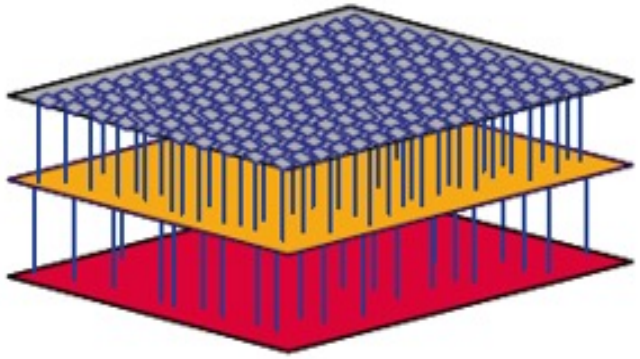
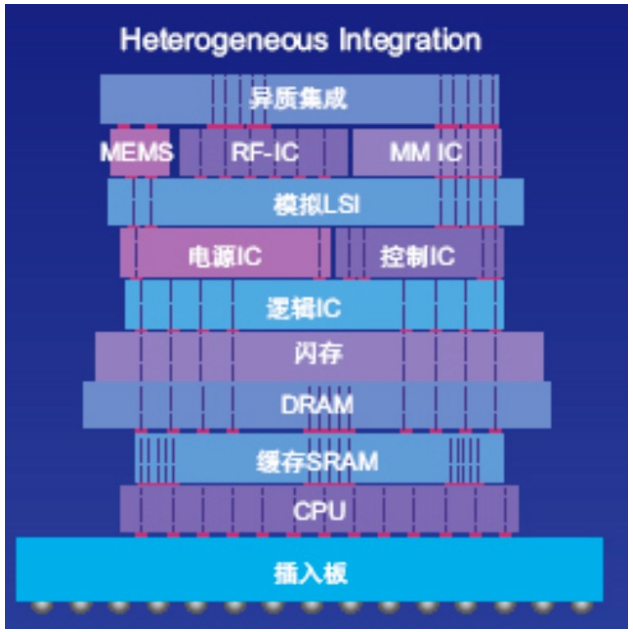
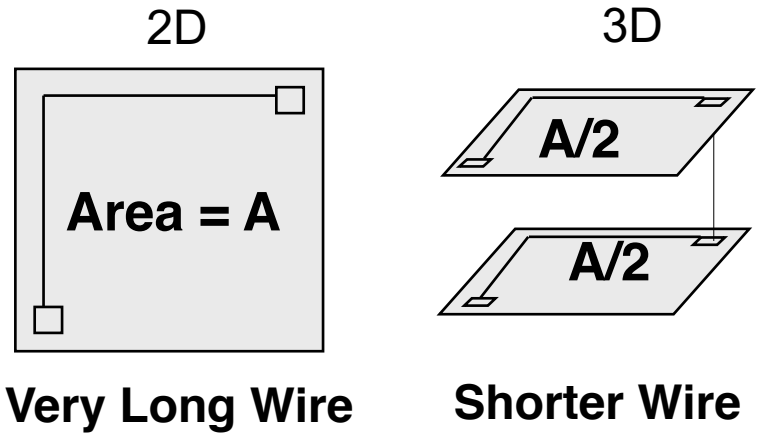
拓展文献阅读：三维互连新技术

1. 高密度
2. 小尺寸
3. 高性能



TSV孔来实现垂直互连





Wen-Wei Shen and Kuan-Neng Chen， Three-Dimensional Integrated Circuit (3D IC) Key Technology: Through-Silicon Via (TSV)[J] Nanoscale Research Letters (2017) 12:56

本章小结

后端互连总结

降低RC延迟方法：
1. 使用low k 介质
2. 降低互连电阻

Al：尖楔、电迁移

掺Si/ Cu

Cu：单镶嵌工艺、双镶嵌工艺

通孔优先工艺、沟槽优先工艺

平坦化技术： CMP