BSIM3v3.3 MOSFET Model

Users' Manual

Weidong Liu, Xiaodong Jin, Xuemei Xi, James Chen, Min-Chie Jeng, Zhihong Liu, Yuhua Cheng, Kai Chen, Mansun Chan, Kelvin Hui, Jianhui Huang, Robert Tu, Ping K. Ko and Chenming Hu

Department of Electrical Engineering and Computer Sciences

University of California, Berkeley, CA 94720

Developers:

The BSIM3v3.3.0 MOSFET model is developed by

- Prof. Chenming Hu, UC Berkeley
- Dr. Xuemei Xi, UC Berkeley
- Mohan Dunga, UC Berkeley

Developers of Previous Versions:

- Dr. Mansun Chan, USTHK
- Dr. Kai Chen, IBM
- Dr. Yuhua Cheng, Rockwell
- Dr. Jianhui Huang, Intel Corp.
- Dr. Kelvin Hui, Lattice Semiconductor
- Dr. James Chen, UC Berkeley
- Dr. Min-Chie Jeng, Cadence Design Systems
- Dr. Zhi-Hong Liu, BTA Technology Inc.
- Dr. Robert Tu, AMD
- Prof. Ping K. Ko, UST, Hong Kong
- Prof. Chenming Hu, UC Berkeley

Web Sites to Visit:

BSIM web site: **http://www-device.eecs.berkeley.edu/~bsim3**

Compact Model Council web site: **http://www.eia.org/eig/CMC**

Technical Support:

Dr. Xuemei (Jane) Xi: janexi@eecs.berkeley.edu

Acknowledgment:

The development of BSIM3v3.3 benefited from the input of many BSIM3 users, especially the Compact Model Council (CMC) member companies. The developers would like to thank Keith Green, Tom Vrotsos, David Zweidinger and Claude R. Cirba at TI, Joe Watts at IBM, Colin McAndrew at Motorola, Min-Chie Jeng, Zhihong Liu at Cadence, Weidong Liu at Synopsys, Paul Humphries at Analog Devices, Shiuh-Wuu Lee, Paul Packan, Wei-Kai Shih at Intel, Judy An at AMD, Mohamed Ahmed, Mohamed Hassan, and Mohamed Selim at Mentor Graphics, Peter Lee at Renesas, Takahiro Iizuka at NEC, Sally Liu, Ke-Wei Su at TSMC, Daniel Wan, Jin Shyong Jan at UMC for their valuable assistance in identifying the desirable modifications and testing of the new model.

Special acknowledgment goes to Dr. Josef Watts, chair of CMC, Dr. Keith Green, former Chairman of the Technical Issue Subcommittee of CMC; and Bhaskar Gadepally, Britt Brooks, former chairs of CMC.

The BSIM3 project is partially supported by SRC, CMC and Rockwell Intern:ational.

Table of Contents

CHAPTER 1: Introduction

1.1 General Information

BSIM3v3 is the latest industry-standard MOSFET model for deep-submicron digital and analog circuit designs from the BSIM Group at the University of California at Berkeley. BSIM3v3.3 is based on its predecessor, BSIM3v3.2.4, with the following changes:

- **A channel thermal noise formulation varying smoothly from linear region to saturation region. The formulation comes from Cadence Spectre.**
- **A BSIM4 ACNQS model that enbles the NQS effect in AC simulation.**
- **A new parameter LINTNOI introducing an offset to the length reduction parameter(Lint) to improve the accuracy of the flicker noise model;**
- **Known bugs are fixed.**

1.2 Organization of This Manual

This manual describes the BSIM3v3.3 model in the following manner:

- Chapter 2 discusses the physical basis used to derive the I-V model.
- Chapter 3 highlights a single-equation I-V model for all operating regimes.
- Chapter 4 presents C-V modeling and focuses on the charge thickness model.
- Chapter 5 describes in detail the restrutured NQS (Non-Quasi-Static) Model.
- Chapter 6 discusses model parameter extraction.
- Chapter 7 provides some benchmark test results to demonstrate the accuracy and performance of the model.

- Chapter 8 presents the noise model.
- Chapter 9 describes the MOS diode I-V and C-V models.
- The Appendices list all model parameters, equations and references.

CHAPTER 2: Physics-Based Derivation of I-V Model

The development of BSIM3v3 is based on Poisson's equation using gradual channel approximation and coherent quasi 2D analysis, taking into account the effects of device geometry and process parameters. BSIM3v3.2.2 considers the following physical phenomena observed in MOSFET devices [1]:

- **Short and narrow channel effects on threshold voltage.**
- **Non-uniform doping effect (in both lateral and vertical directions).**
- **Mobility reduction due to vertical field.**
- **Bulk charge effect.**
- **Velocity saturation.**
- **Drain-induced barrier lowering (*DIBL*).**
- **Channel length modulation (*CLM*).**
- **Substrate current induced body effect (*SCBE*).**
- **Subthreshold conduction.**
- **Source/drain parasitic resistances.**

2.1 Non-Uniform Doping and Small Channel Effects on Threshold Voltage

Accurate modeling of threshold voltage (V_{th}) is one of the most important requirements for precise description of device electrical characteristics. In addition, it serves as a useful reference point for the evaluation of device operation regimes. By using threshold voltage, the whole device operation regime can be divided into three operational regions.

First, if the gate voltage is greater than the threshold voltage, the inversion charge density is larger than the substrate doping concentration and MOSFET is operating in the strong inversion region and drift current is dominant. Second, if the gate voltage is smaller than V_{th}, the inversion charge density is smaller than the substrate doping concentration. The transistor is considered to be operating in the weak inversion (or subthreshold) region. Diffusion current is now dominant [2]. Lastly, if the gate voltage is very close to V_{th}, the inversion charge density is close to the doping concentration and the MOSFET is operating in the transition region. In such a case, diffusion and drift currents are both important.

For MOSFET's with long channel length/width and uniform substrate doping concentration, V_{th} is given by [2]:

$$V_{th} = V_{FB} + \Phi_s + g\sqrt{\Phi_s - V_{bs}} = V_{Tideal} + g\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) \tag{2.1.1}$$

where V_{FB} is the flat band voltage, V_{Tideal} is the threshold voltage of the long channel device at zero substrate bias, and γ is the body bias coefficient and is given by:

$$g = \frac{\sqrt{2e_{si}qN_a}}{C_{ox}} \tag{2.1.2}$$

where N_a is the substrate doping concentration. The surface potential is given by:

$$\Phi_s = 2\frac{k_B T}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{2.1.3}$$

Equation (2.1.1) assumes that the channel is uniform and makes use of the one dimensional Poisson equation in the vertical direction of the channel. This model is valid only when the substrate doping concentration is constant and the channel length is long. Under these conditions, the potential is uniform along the channel. Modifications have to be made when the substrate doping concentration is not uniform and/or when the channel length is short, narrow, or both.

2.1.1 Vertical Non-Uniform Doping Effect

The substrate doping profile is not uniform in the vertical direction as shown in Figure 2-1.

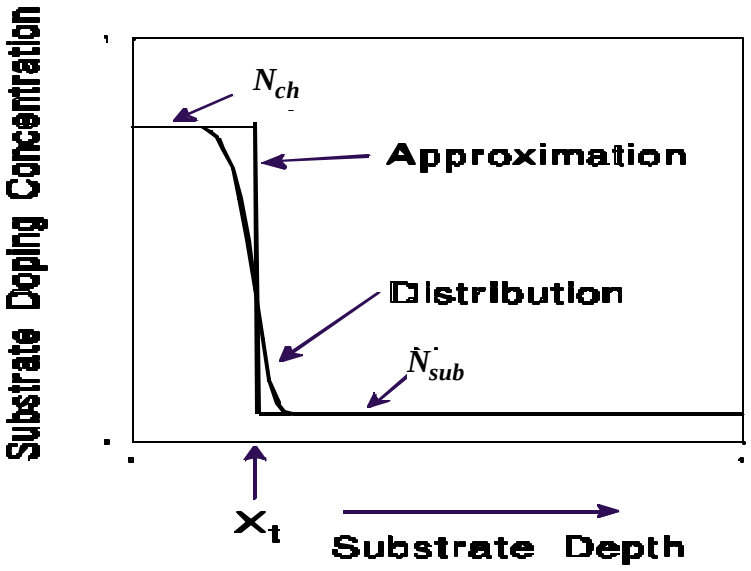

Figure 2-1. Actual substrate doping distribution and its approximation.

The substrate doping concentration is usually higher near the Si/SiO_2 interface (due to V_{th} adjustment) than deep into the substrate. The distribution of impurity atoms inside the substrate is approximately a half

gaussian distribution, as shown in Figure 2-1. This non-uniformity will make γ in Eq. (2.1.2) a function of the substrate bias. If the depletion width is less than X_t as shown in Figure 2-1, N_a in Eq. (2.1.2) is equal to N_{ch}; otherwise it is equal to N_{sub}.

In order to take into account such non-uniform substrate doping profile, the following V_{th} model is proposed:

$$V_{th} = V_{Tideal} + K_1\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) - K_2 V_{bs} \tag{2.1.4}$$

For a zero substrate bias, Eqs. (2.1.1) and (2.1.4) give the same result. K_1 and K_2 can be determined by the criteria that V_{th} and its derivative versus V_{bs} should be the same at V_{bm}, where V_{bm} is the maximum substrate bias voltage. Therefore, using equations (2.1.1) and (2.1.4), K_1 and K_2 [3] will be given by the following:

$$K_1 = g_2 - 2K_2\sqrt{\Phi_s - V_{bm}} \tag{2.1.5}$$

$$K_2 = \frac{(g_1 - g_2)\left(\sqrt{\Phi_s - V_{bx}} - \sqrt{\Phi_s}\right)}{2\sqrt{\Phi_s}\left(\sqrt{\Phi_s - V_{bm}} - \sqrt{\Phi_s}\right) + V_{bm}} \tag{2.1.6}$$

where γ_1 and γ_2 are body bias coefficients when the substrate doping concentration are equal to N_{ch} and N_{sub}, respectively:

$$g_1 = \frac{\sqrt{2qe_{si}N_{ch}}}{C_{ox}} \tag{2.1.7}$$

$$g_2 = \frac{\sqrt{2qe_{si}N_{sub}}}{C_{ox}} \tag{2.1.8}$$

V_{bx} is the body bias when the depletion width is equal to X_t. Therefore, V_{bx} satisfies:

$$\frac{qN_{ch}X_t^2}{2e_{si}} = \Phi_s - V_{bx} \tag{2.1.9}$$

If the devices are available, K_1 and K_2 can be determined experimentally. If the devices are not available but the user knows the doping concentration distribution, the user can input the appropriate parameters to specify doping concentration distribution (e.g. N_{ch}, N_{sub} and X_t). Then, K_1 and K_2 can be calculated using equations (2.1.5) and (2.1.6).

2.1.2 Lateral Non-Uniform Doping Effect

For some technologies, the doping concentration near the source/drain is higher than that in the middle of the channel. This is referred to as lateral non-uniform doping and is shown in Figure 2-2. As the channel length becomes shorter, lateral non-uniform doping will cause V_{th} to increase in magnitude because the average doping concentration in the channel is larger. The average channel doping concentration can be calculated as follows:

(2.1.10)

$$N_{eff} = \frac{N_a(L-2L_x)+Npocket2L_x}{L} = N_a\left(1+\frac{2L_x}{L}\cdot\frac{Npocket-N_a}{N_a}\right)$$
$$\equiv N_a\cdot\left(1+\frac{Nlx}{L}\right)$$

Due to the lateral non-uniform doping effect, Eq. (2.1.4) becomes:

(2.1.11)

$$V_{th} = V_{th0} + K_1\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) - K_2V_{bs} + K_1\left(\sqrt{1+\frac{Nlx}{L_{eff}}} - 1\right)\sqrt{\Phi_s}$$

Eq. (2.1.11) can be derived by setting V_{bs} = 0, and using $K_1 \propto (N_{eff})^{0.5}$. The fourth term in Eq. (2.1.11) is used to model the body bias dependence of the lateral non-uniform doping effect. This effect gets stronger at a lower body bias. Examination of Eq. (2.1.11) shows that the threshold voltage will increase as channel length decreases [3].

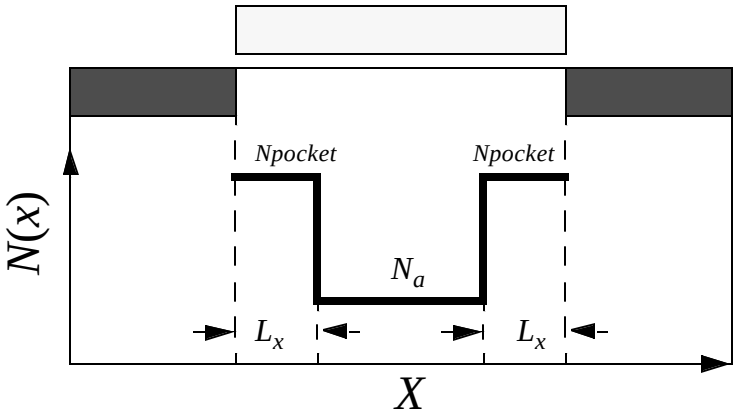

Figure 2-2. Lateral doping profile is non-uniform.

2.1.3 Short Channel Effect

The threshold voltage of a long channel device is independent of the channel length and the drain voltage. Its dependence on the body bias is given by Eq. (2.1.4). However, as the channel length becomes shorter, the threshold voltage shows a greater dependence on the channel length and the drain voltage. The dependence of the threshold voltage on the body bias becomes weaker as channel length becomes shorter, because the body bias has less control of the depletion region. The short-channel effect is included in the V_{th} model as:

$$V_{th} = V_{th0} + K_1\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) - K_2 V_{bs} + K_1\left(\sqrt{1+\frac{Nlx}{L_{eff}}} - 1\right)\sqrt{\Phi_s} - \Delta V_{th} \tag{2.1.12}$$

where ΔV_{th} is the threshold voltage reduction due to the short channel effect. Many models have been developed to calculate ΔV_{th}. They used either numerical solutions [4], a two-dimensional charge sharing approach [5,6], or a simplified Poisson's equation in the depletion region [7-9]. A simple, accurate, and physical model was developed by Z. H. Liu *et al.* [10]. This model was derived by solving the quasi 2D Poisson equation along the channel. This quasi-2D model concluded that:

$$\Delta V_{th} = q_{th}(L)\left(2\left(V_{bi} - \Phi_s\right) + V_{ds}\right) \tag{2.1.13}$$

where V_{bi} is the built-in voltage of the PN junction between the source and the substrate and is given by

$$V_{bi} = \frac{K_B T}{q} \ln\left(\frac{N_{ch} N_d}{n_i^2}\right) \tag{2.1.14}$$

where N_d in is the source/drain doping concentration with a typical value of around 1×10^{20} cm^{-3}. The expression $\theta_{th}(L)$ is a short channel effect coefficient, which has a strong dependence on the channel length and is given by:

$$q_{th}(L) = [\exp(-L/2l_t) + 2\exp(-L/l_t)] \tag{2.1.15}$$

l_t is referred to as the *characteristic length* and is given by

$$l_t = \sqrt{\frac{e_{si} T_{ox} X_{dep}}{e_{ox} h}} \tag{2.1.16}$$

X_{dep} is the depletion width in the substrate and is given by

$$X_{dep} = \sqrt{\frac{2e_{si}(\Phi_s - V_{bs})}{qN_{ch}}} \tag{2.1.17}$$

X_{dep} is larger near the drain than in the middle of the channel due to the drain voltage. X_{dep} / η represents the average depletion width along the channel.

Based on the above discussion, the influences of drain/source charge sharing and *DIBL* effects onV_{th} are described by (2.1.15). In order to make the model fit different technologies, several parameters such as D_{vt0}, D_{vt2},

Dsub, *Eta*0 and *Etab* are introduced, and the following modes are used to account for charge sharing and *DIBL* effects separately.

$$q_{th(L)} = D_{vt0}[\exp(-D_{vt1}L/2l_t) + 2\exp(-D_{vt1}L/l_t)] \tag{2.1.18}$$

$$\Delta V_{th}(L) = q_{th}(L)(V_{bi} - \Phi_s) \tag{2.1.19}$$

$$l_t = \sqrt{\frac{e_{si}T_{ox}X_{dep}}{e_{ox}}}(1 + D_{vt2}V_{bs}) \tag{2.1.20}$$

$$q_{dibl(L)} = [\exp(-D_{sub}L/2l_{t0}) + 2\exp(-D_{sub}L/l_{t0})] \tag{2.1.21}$$

$$\Delta V_{th}(V_{ds}) = q_{dibl(L)}(E_{ta0} + E_{tab}V_{bs})V_{ds} \tag{2.1.22}$$

where l_{t0} is calculated by Eq. (2.1.20) at zero body-bias. D_{vt1} is basically equal to $1/(\eta)^{1/2}$ in Eq. (2.1.16). D_{vt2} is introduced to take care of the dependence of the doping concentration on substrate bias since the doping concentration is not uniform in the vertical direction of the channel. X_{dep} is calculated using the doping concentration in the channel (N_{ch}). D_{vt0}, D_{vt1},D_{vt2}, *Eta*0, *Etab* and *Dsub*, which are determined experimentally, can improve accuracy greatly. Even though Eqs. (2.1.18), (2.1.21) and (2.1.15) have different coefficients, they all still have the same functional forms. Thus the device physics represented by Eqs. (2.1.18), (2.1.21) and (2.1.15) are still the same.

As channel length L decreases, ΔV_{th} will increase, and in turn V_{th} will decrease. If a MOSFET has a *LDD* structure, N_d in Eq. (2.1.14) is the doping concentration in the lightly doped region. V_{bi} in a *LDD*-MOSFET will be smaller as compared to conventional MOSFET's; therefore the threshold voltage reduction due to the short channel effect will be smaller in *LDD*-MOSFET's.

As the body bias becomes more negative, the depletion width will increase as shown in Eq. (2.1.17). Hence ΔV_{th} will increase due to the increase in l_t. The term:

$$V_{Tideal} + K_1\sqrt{\Phi_s - V_{bs}} - K_2 V_{bs}$$

will also increase as V_{bs} becomes more negative (for NMOS). Therefore, the changes in

$$V_{Tideal} + K_1\sqrt{\Phi_s - V_{bs}} - K_2 V_{bs}$$

and in ΔV_{th} will compensate for each other and make V_{th} less sensitive to V_{bs}. This compensation is more significant as the channel length is shortened. Hence, the V_{th} of short channel MOSFET's is less sensitive to body bias as compared to a long channel MOSFET. For the same reason, the *DIBL* effect and the channel length dependence of V_{th} are stronger as V_{bs} is made more negative. This was verified by experimental data shown in Figure 2-3 and Figure 2-4. Although Liu *et al*. found an accelerated V_{th} roll-off and non-linear drain voltage dependence [10] as the channel became very short, a linear dependence of V_{th} on V_{ds} is nevertheless a good approximation for circuit simulation as shown in Figure 2-4. This figure shows that Eq. (2.1.13) can fit the experimental data very well.

Furthermore, Figure 2-5 shows how this V_{th} model can fit various channel lengths under various bias conditions.

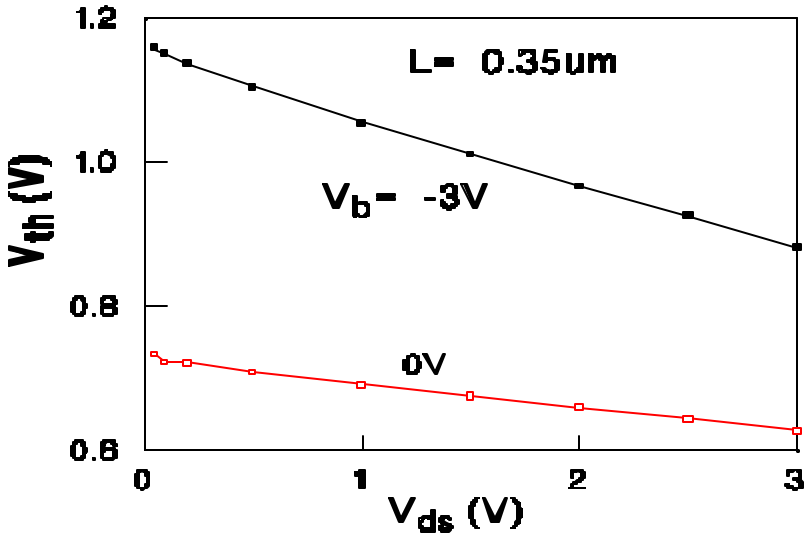

Figure 2-3. Threshold voltage versus the drain voltage at different body biases.

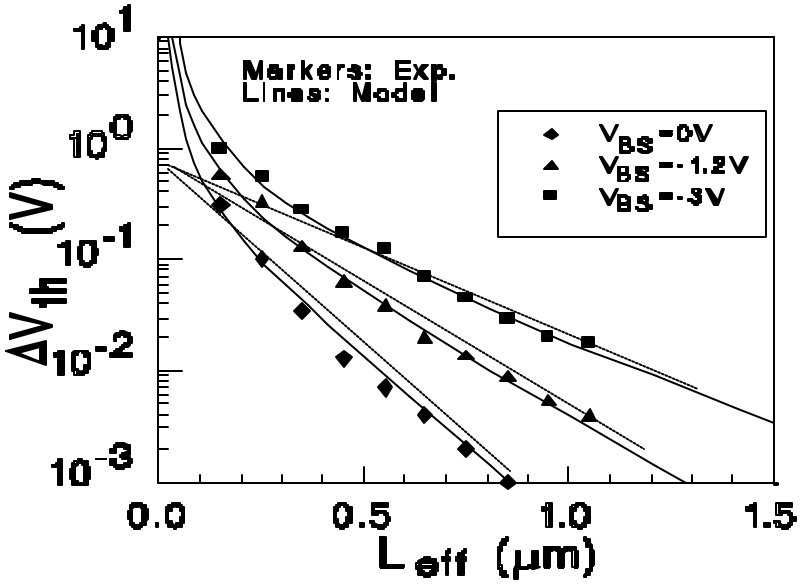

Figure 2-4. Channel length dependence of threshold voltage.

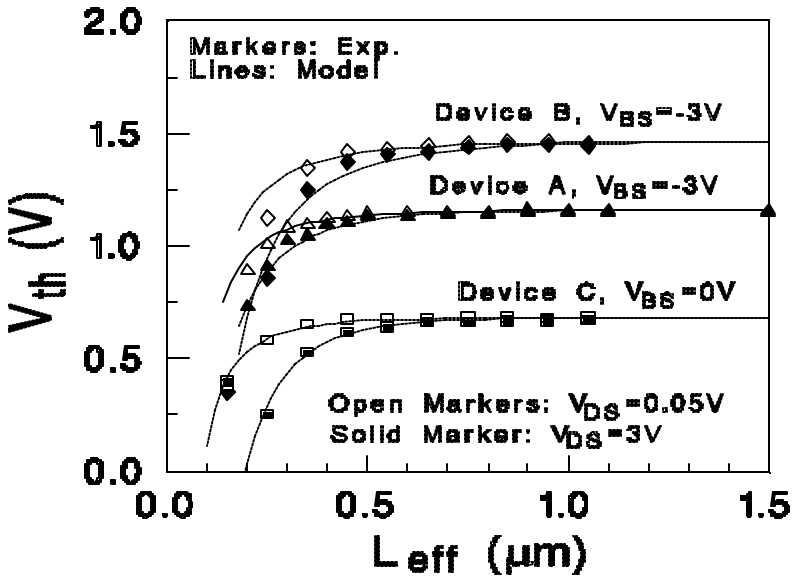

Figure 2-5. Threshold voltage versus channel length at different biases.

2.1.4 Narrow Channel Effect

The actual depletion region in the channel is always larger than what is usually assumed under the one-dimensional analysis due to the existence of fringing fields [2]. This effect becomes very substantial as the channel width decreases and the depletion region underneath the fringing field becomes comparable to the "classical" depletion layer formed from the vertical field. The net result is an increase in V_{th}. It is shown in [2] that this increase can be modeled as:

(2.1.23)

$$\frac{pqN_a X_{d\max}^2}{2C_{ox}W} = 3p\,\frac{T_{ox}}{W}\,\Phi_s$$

The right hand side of Eq. (2.1.23) represents the additional voltage increase. This change in V_{th} is modeled by Eq. (2.1.24a). This formulation includes but is not limited to the inverse of channel width due to the fact that the overall narrow width effect is dependent on process (i.e. isolation technology) as well. Hence, parameters K_3, K_{3b}, and W_0 are introduced as

(2.1.24a)

$$\left(K_3 + K_{3b}V_{bs}\right)\frac{T_{ox}}{W_{eff}'+W_0}\Phi_s$$

W_{eff}' is the effective channel width (with no bias dependencies), which will be defined in Section 2.8. In addition, we must consider the narrow width effect for small channel lengths. To do this we introduce the following:

(2.1.24b)

$$D_{VT0w}\left(exp(-D_{VT1w}\frac{W_{eff}' L_{eff}}{2l_{tw}}) + 2\,exp(-D_{VT1w}\frac{W_{eff}' L_{eff}}{l_{tw}})\right)(V_{bi} - F_s)$$

When all of the above considerations for non-uniform doping, short and narrow channel effects on threshold voltage are considered, the final complete V_{th} expression implemented in SPICE is as follows:

(2.1.25)

$$
\begin{aligned}
V_{th} &= V_{th0ox} + K_{1ox}\cdot\sqrt{\Phi_s - V_{bseff}} - K_{2ox}V_{bseff} \\
&+ K_{1ox}\left(\sqrt{1+\frac{Nlx}{L_{eff}}}-1\right)\sqrt{\Phi_s} + \left(K_3 + K_{3b}V_{bseff}\right)\frac{T_{ox}}{W_{eff}'+W_0}\Phi_s \\
&- D_{VT0w}\left(\exp\left(-D_{VT1w}\frac{W_{eff}'L_{eff}}{2l_{tw}}\right)+2\exp\left(-D_{VT1w}\frac{W_{eff}'L_{eff}}{l_{tw}}\right)\right)\left(V_{bi}-\Phi_s\right) \\
&- D_{VT0}\left(\exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right)+2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)\left(V_{bi}-\Phi_s\right) \\
&- \left(\exp\left(-D_{sub}\frac{L_{eff}}{2l_{to}}\right)+2\exp\left(-D_{sub}\frac{L_{eff}}{l_{to}}\right)\right)\left(E_{tao}+E_{tab}V_{bseff}\right)V_{ds}
\end{aligned}
$$

where T_{ox} dependence is introduced in the model parameters K_1 and K_2 to improve the scalibility of V_{th} model with respect to T_{ox}. V_{th0ox}, K_{1ox} and K_{2ox} are modeled as

$$V_{th0ox} = V_{th0} - K_1\cdot\sqrt{\Phi_s}$$

and

$$K_{1ox} = K_1\cdot\frac{T_{ox}}{T_{oxm}}$$

$$K_{2ox} = K_2\cdot\frac{T_{ox}}{T_{oxm}}$$

T_{oxm} is the gate oxide thickness at which parameters are extracted with a default value of T_{ox}.

In Eq. (2.1.25), all V_{bs} terms have been substituted with a V_{bseff} expression as shown in Eq. (2.1.26). This is done in order to set an upper bound for the body bias value during simulations since unreasonable values can occur if this expression is not introduced (see Section 3.8 for details).

$$V_{bseff} = V_{bc} + 0.5[V_{bs} - V_{bc} - d_1 + \sqrt{(V_{bs} - V_{bc} - d_1)^2 - 4d_1V_{bc}}\ ] \tag{2.1.26}$$

where δ_1 = 0.001V. The parameter V_{bc} is the maximum allowable V_{bs} value and is calculated from the condition of dV_{th}/dV_{bs}=0 for the V_{th} expression of 2.1.4, 2.1.5, and 2.1.6, and is equal to:

$$V_{bc} = 0.9\left(\Phi_s - \frac{K_1^{\ 2}}{4K_2^{\ 2}}\right)$$

2.2 Mobility Model

A good mobility model is critical to the accuracy of a MOSFET model. The scattering mechanisms responsible for surface mobility basically include phonons, coulombic scattering, and surface roughness [11, 12]. For good quality interfaces, phonon scattering is generally the dominant scattering mechanism at room temperature. In general, mobility depends on many process parameters and bias conditions. For example, mobility depends on the gate oxide thickness, substrate doping concentration, threshold voltage, gate and substrate voltages, etc. Sabnis and Clemens [13] proposed an empirical unified formulation based on the concept of an effective field E_{eff} which lumps many process parameters and bias conditions together. E_{eff} is defined by

$$E_{eff} = \frac{Q_B + (Q_n/2)}{e_{si}} \tag{2.2.1}$$

The physical meaning of E_{eff} can be interpreted as the average electrical field experienced by the carriers in the inversion layer [14]. The unified formulation of mobility is then given by

$$m_{eff} = \frac{m_0}{1+(E_{eff}/E_0)^n} \tag{2.2.2}$$

Values for μ_0, E_0, and ν were reported by Liang *et al.* [15] and Toh *et al*. [16] to be the following for electrons and holes

Parameter	Electron (surface)	Hole (surface)
μ_0 ($cm^2/Vsec$)	670	160
E_0 (MV/cm)	0.67	0.7
ν	1.6	1.0

Table 2-1. Typical mobility values for electrons and holes.

For an NMOS transistor with n-type poly-silicon gate, Eq. (2.2.1) can be rewritten in a more useful form that explicitly relates E_{eff} to the device parameters [14]

$$E_{eff} \cong \frac{V_{gs}+V_{th}}{6T_{ox}} \tag{2.2.3}$$

Eq. (2.2.2) fits experimental data very well [15], but it involves a very time consuming power function in SPICE simulation. Taylor expansion Eq. (2.2.2) is used, and the coefficients are left to be determined by experimental data or to be obtained by fitting the unified formulation. Thus, we have

(mobMod=1) (2.2.4)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})\left(\frac{V_{gst} + 2V_{th}}{T_{OX}}\right) + U_b\left(\frac{V_{gst} + 2V_{th}}{T_{OX}}\right)^2}$$

where $V_{gst}=V_{gs}-V_{th}$. To account for depletion mode devices, another mobility model option is given by the following

(mobMod=2) (2.2.5)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})\left(\frac{V_{gst}}{T_{OX}}\right) + U_b\left(\frac{V_{gst}}{T_{OX}}\right)^2}$$

The unified mobility expressions in subthreshold and strong inversion regions will be discussed in Section 3.2.

To consider the body bias dependence of Eq. 2.2.4 further, we have introduced the following expression:

(For mobMod=3) (2.2.6)

$$\mu_{eff} = \frac{\mu_o}{1 + \left[U_a\left(\frac{V_{gst} + 2V_{th}}{T_{OX}}\right) + U_b\left(\frac{V_{gst} + 2V_{th}}{T_{OX}}\right)^2\right](1 + U_c V_{bseff})}$$

2.3 Carrier Drift Velocity

Carrier drift velocity is also one of the most important parameters. The following velocity saturation equation [17] is used in the model

(2.3.1)

$$v = \frac{\mu_{eff} E}{1 + (E/E_{sat})}, \qquad E < E_{sat}$$
$$= v_{sat}, \qquad E > E_{sat}$$

The parameter E_{sat} corresponds to the critical electrical field at which the carrier velocity becomes saturated. In order to have a continuous velocity model at $E = E_{sat}$, E_{sat} must satisfy:

(2.3.2)

$$E_{sat} = \frac{2 v_{sat}}{\mu_{eff}}$$

2.4 Bulk Charge Effect

When the drain voltage is large and/or when the channel length is long, the depletion "thickness" of the channel is non-uniform along the channel length. This will cause V_{th} to vary along the channel. This effect is called bulk charge effect [14].

The parameter, A_{bulk}, is used to take into account the bulk charge effect. Several extracted parameters such as A_0, B_0, B_1 are introduced to account for the channel length and width dependences of the bulk charge effect. In addition, the parameter *Keta* is introduced to model the change in bulk charge effect under high substrate bias conditions. It should be pointed out that narrow width effects have been considered in the formulation of Eq. (2.4.1). The A_{bulk} expression is given by

(2.4.1)

$$A_{bulk} = \left(1 + \frac{K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}}\left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}\left(1 - A_{gs} V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}\right)^2\right) + \frac{B_0}{W_{eff}' + B_1}\right)\right) \cdot \frac{1}{1 + Keta V_{bseff}}$$

where A_0, A_{gs}, B_0, B_1 and *Keta* are determined by experimental data. Eq. (2.4.1) shows that A_{bulk} is very close to unity if the channel length is small, and A_{bulk} increases as channel length increases.

2.5 Strong Inversion Drain Current (Linear Regime)

2.5.1 Intrinsic Case (R_{ds}=0)

In the strong inversion region, the general current equation at any point *y* along the channel is given by

$$I_{ds} = WC_{ox}(V_{gst} - A_{bulk}V_{(y)})v_{(y)} \tag{2.5.1}$$

The parameter $V_{gst} = (V_{gs} - V_{th})$, W is the device channel width, C_{ox} is the gate capacitance per unit area, $V(y)$ is the potential difference between minority-carrier quasi-Fermi potential and the equilibrium Fermi potential in the bulk at point *y*, *v(y)* is the velocity of carriers at point *y*.

With Eq. (2.3.1) (i.e. before carrier velocity saturates), the drain current can be expressed as

$$I_{ds} = WC_{ox}(V_{gs} - V_{th} - A_{bulk}V_{(y)})\frac{m_{eff}E_{(y)}}{1 + E_{(y)}/E_{sat}} \tag{2.5.2}$$

Eq. (2.5.2) can be rewritten as follows

$$E_{(y)} = \frac{I_{ds}}{\mu_{eff} WC_{ox}(V_{gst} - A_{bulk}V_{(y)}) - I_{ds}/E_{sat}} = \frac{dV_{(y)}}{dy} \tag{2.5.3}$$

By integrating Eq. (2.5.2) from $y = 0$ to $y = L$ and $V(y) = 0$ to $V(y) = V_{ds}$, we arrive at the following

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \frac{1}{1 + V_{ds}/E_{sat}L}(V_{gs} - V_{th} - A_{bulk}V_{ds}/2)V_{ds} \tag{2.5.4}$$

The drain current model in Eq. (2.5.4) is valid before velocity saturates.

For instances when the drain voltage is high (and thus the lateral electrical field is high at the drain side), the carrier velocity near the drain saturates. The channel region can now be divided into two portions: one adjacent to the source where the carrier velocity is field-dependent and the second where the velocity saturates. At the boundary between these two portions, the channel voltage is the saturation voltage (V_{dsat}) and the lateral electrical is equal to E_{sat}. After the onset of saturation, we can substitute $v = v_{sat}$ and $V_{ds} = V_{dsat}$ into Eq. (2.5.1) to get the saturation current:

$$I_{ds} = WC_{ox}(V_{gst} - A_{bulk}V_{dsat})v_{sat} \tag{2.5.5}$$

By equating eqs. (2.5.4) and (2.5.5) at $E = E_{sat}$ and $V_{ds} = V_{dsat}$, we can solve for saturation voltage V_{dsat}

$$V_{dsat} = \frac{E_{sat}L(V_{gs} - V_{th})}{A_{bulk}E_{sat}L + (V_{gs} - V_{th})} \tag{2.5.6}$$

2.5.2 Extrinsic Case (R_{ds}>0)

Parasitic source/drain resistance is an important device parameter which can affect MOSFET performance significantly. As channel length scales down, the parasitic resistance will not be proportionally scaled. As a result, R_{ds} will have a more significant impact on device characteristics. Modeling of parasitic resistance in a direct method yields a complicated drain current expression. In order to make simulations more efficient, the parasitic resistances is modeled such that the resulting drain current equation in the linear region can be calculateed [3] as

(2.5.9)

$$I_{ds} = \frac{V_{ds}}{R_{tot}} = \frac{V_{ds}}{R_{ch} + R_{ds}}$$
$$= \mu_{eff} C_{ox} \frac{W}{L} \frac{1}{1 + V_{ds}/(E_{sat} L)} \frac{(V_{gst} - A_{bulk} V_{ds}/2) V_{ds}}{1 + R_{ds} \mu_{eff} C_{ox} \frac{W}{L} \frac{(V_{gst} - A_{bulk} V_{ds}/2)}{1 + V_{ds}/(E_{sat} L)}}$$

Due to the parasitic resistance, the saturation voltage V_{dsat} will be larger than that predicted by Eq. (2.5.6). Let Eq. (2.5.5) be equal to Eq. (2.5.9). V_{dsat} with parasitic resistance R_{ds} becomes

(2.5.10)

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

The following are the expression for the variables *a*, *b*, and *c*:

(2.5.11)

$$a = A_{bulk}^2 R_{ds} C_{ox} W v_{sat} + (\frac{1}{l} - 1) A_{bulk}$$

$$b = -(V_{gst}(\frac{2}{l} - 1) + A_{bulk} E_{sat} L + 3A_{bulk} R_{ds} C_{ox} W v_{sat} V_{gst})$$

$$c = E_{sat} L V_{gst} + 2R_{ds} C_{ox} W v_{sat} V_{gst}^2$$

$$l = A_1 V_{gst} + A_2$$

The last expression for λ is introduced to account for non-saturation effect of the device. The parasitic resistance is modeled as:

(2.5.11)

$$R_{ds} = \frac{R_{dsw}\left(1 + P_{rwg} V_{gsteff} + P_{rwb}\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right)\right)}{\left(10^6 W_{eff}'\right)^{W_r}}$$

The variable R_{dsw} is the resistance per unit width, W_r is a fitting parameter, P_{rwb} and P_{rwg} are the body bias and the gate bias coeffecients, repectively.

2.6 Strong Inversion Current and Output Resistance (Saturation Regime)

A typical I-V curve and its output resistance are shown in Figure 2-6. Considering only the drain current, the I-V curve can be divided into two parts: the linear region in which the drain current increases quickly with the drain voltage and the saturation region in which the drain current has a very weak dependence on the drain voltage. The first order derivative reveals more detailed information about the physical mechanisms which are involved during device operation. The output resistance (which is the reciprocal of the first order derivative of the I-V curve)

curve can be clearly divided into four regions with distinct R_{out} *vs.* V_{ds} dependences.

The first region is the triode (or linear) region in which carrier velocity is not saturated. The output resistance is very small because the drain current has a strong dependence on the drain voltage. The other three regions belong to the saturation region. As will be discussed later, there are three physical mechanisms which affect the output resistance in the saturation region: channel length modulation (*CLM*) [4, 14], drain-induced barrier lowering (*DIBL*) [4, 6, 14], and the substrate current induced body effect (*SCBE*) [14, 18, 19]. All three mechanisms affect the output resistance in the saturation range, but each of them dominates in only a single region. It will be shown next that channel length modulation (*CLM*) dominates in the second region, *DIBL* in the third region, and *SCBE* in the fourth region.

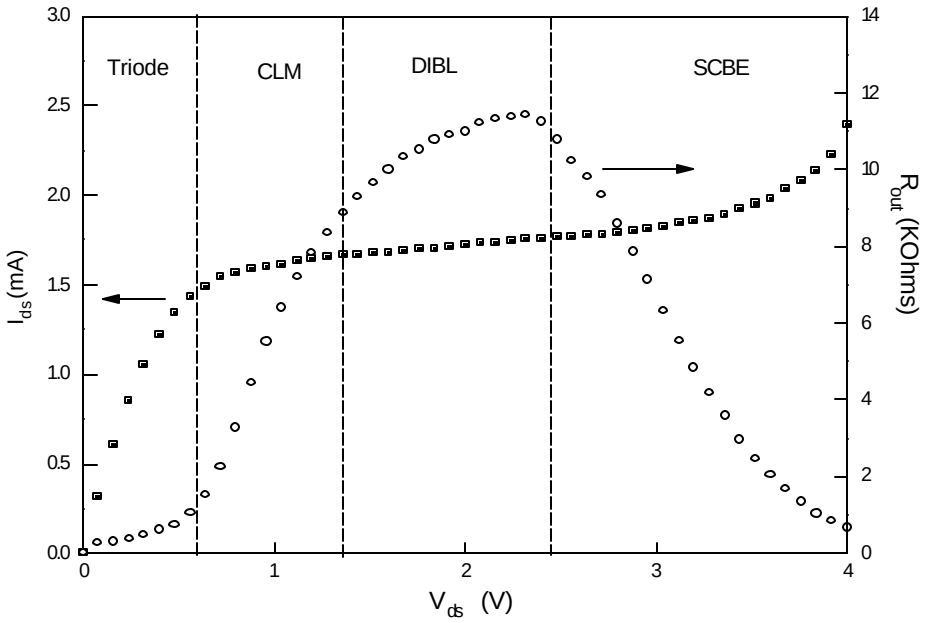

Figure 2-6. General behavior of MOSFET output resistance.

Generally, drain current is a function of the gate voltage and the drain voltage. But the drain current depends on the drain voltage very weakly in the saturation region. A Taylor series can be used to expand the drain current in the saturation region [3].

$$I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{gs}, V_{dsat}) + \frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{ds}}(V_{ds} - V_{dsat}) \equiv I_{dsat}(1 + \frac{V_{ds} - V_{dsat}}{V_A}) \tag{2.6.1}$$

where

$$I_{dsat} = I_{ds}(V_{gs,} V_{dsat}) = W v_{sat} C_{ox}(V_{gst} - A_{bulk} V_{dsat}) \tag{2.6.2}$$

and

$$V_A = I_{dsat}(\frac{\partial I_{ds}}{\partial V_{ds}})^{-1} \tag{2.6.3}$$

The parameter V_A is called the Early voltage and is introduced for the analysis of the output resistance in the saturation region. Only the first order term is kept in the Taylor series. We also assume that the contributions to the Early voltage from all three mechanisms are independent and can be calculated separately.

2.6.1 Channel Length Modulation (CLM)

If channel length modulation is the only physical mechanism to be taken into account, then according to Eq. (2.6.3), the Early voltage can be calculated by

$$V_{ACLM} = I_{dsat}(\frac{\P I_{ds}}{\P L}\frac{\P L}{\P V_{ds}})^{-1} = \frac{A_{bulk}E_{sat}L + V_{gst}}{A_{bulk}E_{sat}}(\frac{\P DL}{\P V_{ds}})^{-1} \tag{2.6.4}$$

where ΔL is the length of the velocity saturation region; the effective channel length is L-ΔL. Based on the quasi-two dimensional approximation, V_{ACLM} can be derived as the following

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L + V_{gst}}{A_{bulk}E_{sat}l}(V_{ds} - V_{dsat}) \tag{2.6.5}$$

where V_{ACLM} is the Early Voltage due to channel length modulation alone.

The parameter P_{clm} is introduced into the V_{ACLM} expression not only to compensate for the error caused by the Taylor expansion in the Early voltage model, but also to compensate for the error in X_J since $l \propto \sqrt{X_J}$

and the junction depth X_J can not generally be determined very accurately. Thus, the V_{ACLM} became

$$V_{ACLM} = \frac{1}{P_{clm}}\frac{A_{bulk}E_{sat}L + V_{gst}}{A_{bulk}E_{sat}l}(V_{ds} - V_{dsat}) \tag{2.6.6}$$

2.6.2 Drain-Induced Barrier Lowering (*DIBL*)

As discussed above, threshold voltage can be approximated as a linear function of the drain voltage. According to Eq. (2.6.3), the Early voltage due to the *DIBL* effect can be calculated as:

(2.6.7)

$$V_{ADIBLC} = I_{dsat}\left(\frac{\partial I_{ds}}{\partial V_{th}}\frac{\partial V_{th}}{\partial V_{ds}}\right)^{-1}$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{q_{rout}(1 + P_{DIBLCB}V_{bseff})}\left(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat} + V_{gsteff} + 2v_t}\right)$$

During the derivation of Eq. (2.6.7), the parasitic resistance is assumed to be equal to 0. As expected, V_{ADIBLC} is a strong function of L as shown in Eq. (2.6.7). As channel length decreases, V_{ADIBLC} decreases very quickly. The combination of the *CLM* and *DIBL* effects determines the output resistance in the third region, as was shown in Figure 2-6.

Despite the formulation of these two effects, accurate modeling of the output resistance in the saturation region requires that the coefficient $\theta_{th}(L)$ be replaced by $\theta_{rout}(L)$. Both $\theta_{th}(L)$ and $\theta_{rout}(L)$ have the same channel length dependencies but different coefficients. The expression for $\theta_{rout}(L)$ is

(2.6.8)

$$q_{rout}(L) = P_{diblc1}[\exp(-D_{rout}L / 2l_t) + 2\exp(-D_{rout}L / l_t)] + P_{diblc2}$$

Parameters P_{diblc1}, P_{diblc2}, P_{diblcb} and D_{rout} are introduced to correct for *DIBL* effect in the strong inversion region. The reason why D_{vt0} is not

equal to P_{diblc1} and D_{vt1} is not equal to D_{rout} is because the gate voltage modulates the *DIBL* effect. When the threshold voltage is determined, the gate voltage is equal to the threshold voltage. But in the saturation region where the output resistance is modeled, the gate voltage is much larger than the threshold voltage. Drain induced barrier lowering may not be the same at different gate bias. P_{diblc2} is usually very small (may be as small as 8.0E-3). If P_{diblc2} is placed into the threshold voltage model, it will not cause any significant change. However it is an important parameter in V_{ADIBL} for long channel devices, because P_{diblc2} will be dominant in Eq. (2.6.8) if the channel is long.

2.6.3 Current Expression without Substrate Current Induced Body Effect

In order to have a continuous drain current and output resistance expression at the transition point between linear and saturation region, the V_{Asat} parameter is introduced into the Early voltage expression. V_{Asat} is the Early Voltage at $V_{ds} = V_{dsat}$ and is as follows:

$$V_{Asat} = \frac{E_{sat}L + V_{dsat} + 2R_{ds}v_{sat}C_{ox}W(V_{gst} - A_{bulk}V_{ds}/2)}{1 + A_{bulk}R_{ds}v_{sat}C_{ox}W} \tag{2.6.9}$$

Total Early voltage, V_A, can be written as

$$V_A = V_{Asat} + \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}}\right)^{-1} \tag{2.6.10}$$

The complete (with no impact ionization at high drain voltages) current expression in the saturation region is given by

$$I_{dso} = Wv_{sat} C_{ox} (V_{gst} - A_{bulk} V_{dsat})(1 + \frac{V_{ds} - V_{dsat}}{V_A}) \tag{2.6.11}$$

Furthermore, another parameter, P_{vag}, is introduced in V_A to account for the gate bias dependence of V_A more accurately. The final expression for Early voltage becomes

$$V_A = V_{Asat} + (1 + \frac{P_{vag} V_{gs}}{E_{sat} L_{eff}})(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}})^{-1} \tag{2.6.12}$$

2.6.4 Current Expression with Substrate Current Induced Body Effect

When the electrical field near the drain is very large (> 0.1MV/cm), some electrons coming from the source will be energetic (hot) enough to cause impact ionization. This creates electron-hole pairs when they collide with silicon atoms. The substrate current I_{sub} thus created during impact ionization will increase exponentially with the drain voltage. A well known I_{sub} model [20] is given as:

$$I_{sub} = \frac{A_i}{B_i} I_{ds} (V_{ds} - V_{dsat}) \exp\left(- \frac{B_i l}{V_{ds} - V_{dsat}} \right) \tag{2.6.13}$$

The parameters A_i and B_i are determined from extraction. I_{sub} will affect the drain current in two ways. The total drain current will change because it is the sum of the channel current from the source as well as the substrate current. The total drain current can now be expressed [21] as follows

$$I_{ds} = I_{dso} + I_{sub} = I_{dso}\left[1 + \frac{(V_{ds} - V_{dsat})}{\frac{B_i}{A_i}\exp(\frac{B_i l}{V_{ds} - V_{dsat}})}\right] \tag{2.6.14}$$

The total drain current, including *CLM*, *DIBL* and *SCBE*, can be written as

$$I_{ds} = Wv_{sat}C_{ox}(V_{gst} - A_{bulk}V_{dsat})(1 + \frac{V_{ds} - V_{dsat}}{V_A})(1 + \frac{V_{ds} - V_{dsat}}{V_{ASCBE}}) \tag{2.6.15}$$

where V_{ASCBE} can also be called as the Early voltage due to the substrate current induced body effect. Its expression is the following

$$V_{ASCBE} = \frac{B_i}{A_i}\exp(\frac{B_i l}{V_{ds} - V_{dsat}}) \tag{2.6.16}$$

From Eq. (2.6.16), we can see that V_{ASCBE} is a strong function of V_{ds}. In addition, we also observe that V_{ASCBE} is small only when V_{ds} is large. This is why *SCBE* is important for devices with high drain voltage bias. The channel length and gate oxide dependence of V_{ASCBE} comes from V_{dsat} and *l.* We replace *Bi* with *PSCBE*2 and *Ai/Bi* with *PSCBE*1*/L* to yield the following expression for V_{ASCBE}

(2.6.17)

$$\frac{1}{V_{ASCBE}} = \frac{P_{SCBE2}}{L}\exp(-\frac{P_{SCBE1}l}{V_{ds}-V_{dsat}})$$

The variables P_{scbe1} and P_{scbe2} are determined experimentally.

2.7 Subthreshold Drain Current

The drain current equation in the subthreshold region can be expressed as [2, 3]

(2.7.1)

$$I_{ds} = I_{s0}(1-\exp(-\frac{V_{ds}}{v_t}))\exp(\frac{V_{gs}-V_{th}-V_{off}}{nv_t})$$

(2.7.2)

$$I_{s0} = m_0\frac{W}{L}\sqrt{\frac{qe_{si}N_{ch}}{2f_s}}v_t^2$$

Here the parameter v_t is the thermal voltage and is given by K_BT/q. V_{off} is the offset voltage, as discussed in Jeng's dissertation [18]. V_{off} is an important parameter which determines the drain current at V_{gs} = 0. In Eq. (2.7.1), the parameter *n* is the subthreshold swing parameter. Experimental data shows that the subthreshold swing is a function of channel length and the interface state density. These two mechanisms are modeled by the following

(2.7.3)

$$n = 1+N_{factor}\frac{C_d}{C_{ox}}+\frac{(C_{dsc}+C_{dscd}V_{ds}+C_{dscb}V_{bseff})\left(\exp(-D_{VT1}\frac{L_{eff}}{2l_t})+2\exp(-D_{VT1}\frac{L_{eff}}{l_t})\right)}{C_{ox}}+\frac{C_{it}}{C_{ox}}$$

where the term

$$(C_{dsc} + C_{dscd}V_{ds} + C_{dscb}V_{bseff})\left(\exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + 2\exp(-D_{VT1}\frac{L_{eff}}{l_t})\right)$$

represents the coupling capacitance between the drain or source to the channel. The parameters C_{dsc}, C_{dscd} and C_{dscb} are extracted. The parameter C_{it} in Eq. (2.7.3) is the capacitance due to interface states. From Eq. (2.7.3), it can be seen that subthreshold swing shares the same exponential dependence on channel length as the *DIBL* effect. The parameter *Nfactor* is introduced to compensate for errors in the depletion width capacitance calculation. *Nfactor* is determined experimentally and is usually very close to 1.

2.8 Effective Channel Length and Width

The effective channel length and width used in all model expressions is given below

$$L_{eff} = L_{drawn} - 2dL \tag{2.8.1}$$

$$W_{eff} = W_{drawn} - 2dW \tag{2.8.2a}$$

$$W_{eff}' = W_{drawn} - 2dW' \tag{2.8.2b}$$

The only difference between Eq. (2.8.2a) and (2.8.2b) is that the former includes bias dependencies. The parameters *dW* and *dL* are modeled by the following

(2.8.3)

$$dW = dW' + dW_g V_{gsteff} + dW_b \left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s} \right)$$
$$dW' = W_{\text{int}} + \frac{W_l}{L^{W\ln}} + \frac{W_w}{W^{Wwn}} + \frac{W_{wl}}{L^{W\ln} W^{Wwn}}$$

(2.8.4)

$$dL = L_{\text{int}} + \frac{L_l}{L^{L\ln}} + \frac{L_w}{W^{Lwn}} + \frac{L_{wl}}{L^{L\ln} W^{Lwn}}$$

These complicated formulations require some explanation. From Eq. (2.8.3), the variable W_{int} models represents the tradition manner from which "delta W" is extracted (from the *int*ercepts of straights lines on a $1/R_{ds}$ vs. W_{drawn} plot). The parameters dW_g and dW_b have been added to account for the contribution of both front gate and back side (substrate) biasing effects. For dL, the parameter L_{int} represents the traditional manner from which "delta L" is extracted (mainly from the *int*ercepts of lines from a R_{ds} vs. L_{drawn} plot).

The remaining terms in both dW and dL are included for the convenience of the user. They are meant to allow the user to model each parameter as a function of W_{drawn}, L_{drawn} and their associated product terms. In addition, the freedom to model these dependencies as other than just simple inverse functions of W and L is also provided for the user. For dW, they are Wln and Wwn. For dL they are Lln and Lwn.

By default all of the above *geometrical* dependencies for both dW and dL are turned off. Again, these equations are provided for the convenience of the user. As such, it is up to the user to adopt the correct extraction strategy to ensure proper use.

2.9 Poly Gate Depletion Effect

When a gate voltage is applied to a heavily doped poly-silicon gate, e.g. NMOS with n^+ poly-silicon gate, a thin depletion layer will be formed at the interface between the poly-silicon and gate oxide. Although this depletion layer is very thin due to the high doping concentration of the poly-Si gate, its effect cannot be ignored in the 0.1μm regime since the gate oxide thickness will also be very small, possibly 50Å or thinner.

Figure 2-7 shows an NMOSFET with a depletion region in the n^+ poly-silicon gate. The doping concentration in the n^+ poly-silicon gate is N_{gate} and the doping concentration in the substrate is N_{sub}. The gate oxide thickness is T_{ox}. The depletion width in the poly gate is X_p. The depletion width in the substrate is X_d. If we assume the doping concentration in the gate is infinite, then no depletion region will exist in the gate, and there would be one sheet of positive charge whose thickness is zero at the interface between the poly-silicon gate and gate oxide.

In reality, the doping concentration is, of course, finite. The positive charge near the interface of the poly-silicon gate and the gate oxide is distributed over a finite depletion region with thickness X_p. In the presence of the depletion region, the voltage drop across the gate oxide and the substrate will be reduced, because part of the gate voltage will be dropped across the depletion region in the gate. That means the effective gate voltage will be reduced.

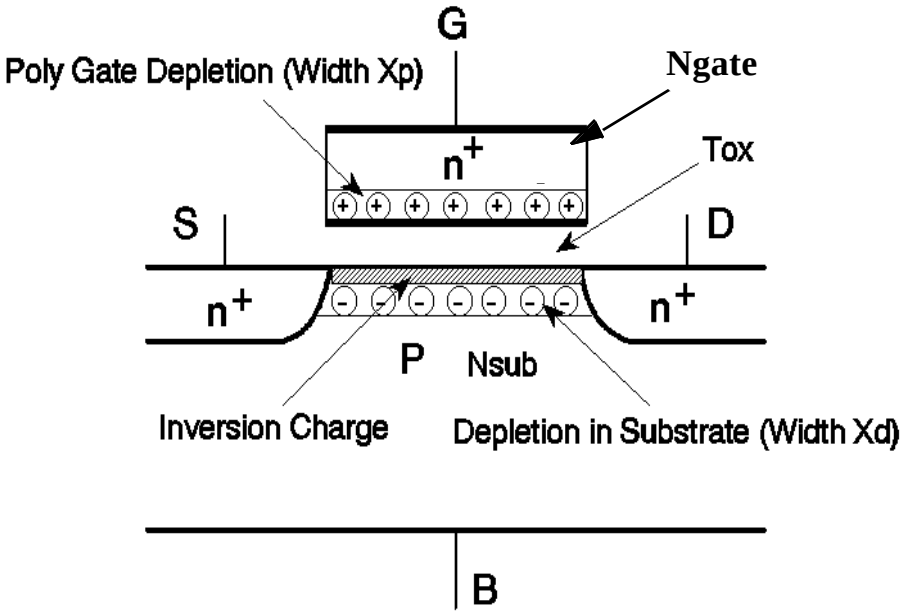

Figure 2-7. Charge distribution in a MOSFET with the poly gate depletion effect. The device is in the strong inversion region.

The effective gate voltage can be calculated in the following manner. Assume the doping concentration in the poly gate is uniform. The voltage drop in the poly gate (V_{poly}) can be calculated as

$$V_{poly} = \frac{1}{2} X_{poly} E_{poly} = \frac{qN_{gate} X_{poly}^2}{2e_{si}} \tag{2.9.1}$$

where E_{poly} is the maximum electrical field in the poly gate. The boundary condition at the interface of poly gate and the gate oxide is

$$e_{ox} E_{ox} = e_{si} E_{poly} = \sqrt{2qe_{si} N_{gate} V_{poly}} \tag{2.9.2}$$

where E_{ox} is the electrical field in the gate oxide. The gate voltage satisfies

$$V_{gs} - V_{FB} - \Phi_s = V_{poly} + V_{ox} \tag{2.9.3}$$

where V_{ox} is the voltage drop across the gate oxide and satisfies $V_{ox} = E_{ox}T_{ox}$.

According to the equations (2.9.1) to (2.9.3), we obtain the following

$$a\left(V_{gs} - V_{FB} - \Phi_s - V_{poly}\right)^2 - V_{poly} = 0 \tag{2.9.4}$$

where (2.9.5)

$$a = \frac{e_{ox}^{\ 2}}{2qe_{si}N_{gate}T_{ox}^{\ 2}}$$

By solving the equation (2.9.4), we get the effective gate voltage (V_{gs_eff}) which is equal to:

$$V_{gs\_eff} = V_{FB} + \Phi_s + \frac{qe_{si}N_{gate}T_{ox}^{\ 2}}{e_{ox}^{\ 2}}\left(\sqrt{1 + \frac{2e_{ox}^{\ 2}\left(V_{gs} - V_{FB} - \Phi_s\right)}{qe_{si}N_{gate}T_{ox}^{\ 2}}} - 1\right) \tag{2.9.6}$$

Figure 2-8 shows V_{gs_eff} / V_{gs} versus the gate voltage. The threshold voltage is assumed to be 0.4V. If T_{ox} = 40 Å, the effective gate voltage can be reduced by 6% due to the poly gate depletion effect as the applied gate voltage is equal to 3.5V.

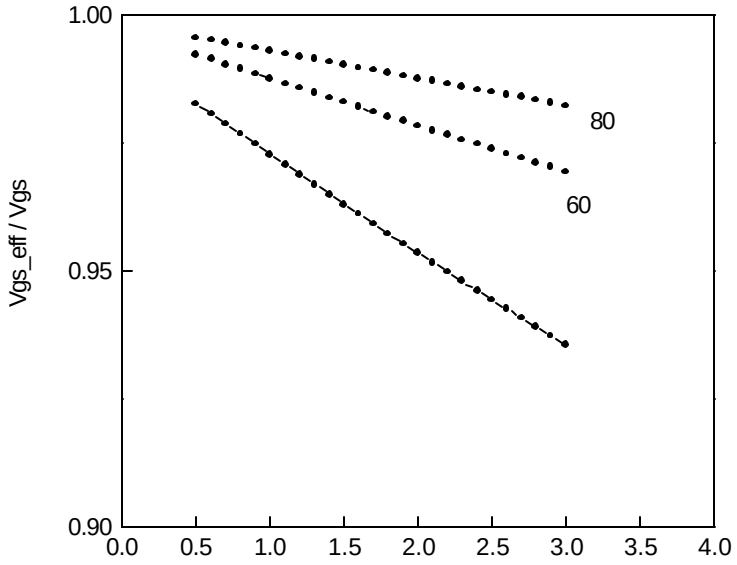

Figure 2-8. The effective gate voltage versus applied gate voltage at different gate oxide thickness.

The drain current reduction in the linear region as a function of the gate voltage can now be determined. Assume the drain voltage is very small, e.g. *50mV*. Then the linear drain current is proportional to $C_{ox}(V_{gs} - V_{th})$. The ratio of the linear drain current with and without poly gate depletion is equal to:

(2.9.7)

Figure 2-9 shows $I_{ds}(V_{gs\_eff})$ / $I_{ds}(V_{gs})$ versus the gate voltage using Eq. (2.9.7). The drain current can be reduced by several percent due to gate depletion.

CHAPTER 3: Unified I-V Model

The development of separate model expressions for such device operation regimes as subthreshold and strong inversion were discussed in Chapter 2. Although these expressions can accurately describe device behavior within their own respective region of operation, problems are likely to occur between two well-described regions or within transition regions. In order to circumvent this issue, a unified model should be synthesized to not only preserve region-specific expressions but also to ensure the continuities of current and conductance *and* their derivatives in *all* transition regions as well. Such high standards are kept in BSIM3v3.2.1 . As a result, convergence and simulation efficiency are much improved.

This chapter will describe the unified I-V model equations. While most of the parameter symbols in this chapter are explained in the following text, a complete description of all I-V model parameters can be found in Appendix A.

3.1 Unified Channel Charge Density Expression

Separate expressions for channel charge density are shown below for subthreshold (Eq. (3.1.1a) and (3.1.1b)) and strong inversion (Eq. (3.1.2)). Both expressions are valid for small V_{ds}.

(3.1.1a)

$$Q_{chsubs0} = Q_0 \exp(\frac{V_{gs} - V_{th}}{n v_t})$$

where Q_0 is

(3.1.1b)

$$Q_0 = \sqrt{\frac{q e_{si} N_{ch}}{2 f_s}} v_t \exp(-\frac{V_{off}}{n v_t})$$

(3.1.2)

$$Q_{chs0} = C_{ox}(V_{gs} - V_{th})$$

In both Eqs. (3.1.1a) and (3.1.2), the parameters $Q_{chsubs0}$ and Q_{chs0} are the channel charge densities at the source for very small Vds. To form a unified expression, an effective (V_{gs}-V_{th}) function named V_{gsteff} is introduced to describe the channel charge characteristics from subthreshold to strong inversion

(3.1.3)

$$V_{gsteff} = \frac{2\, n\, v_t \ln\left[1 + \exp(\frac{V_{gs} - V_{th}}{2\, n\, v_t})\right]}{1 + 2\, n\ \ C_{OX}\sqrt{\frac{2\Phi_s}{q e_{si} N_{ch}}} \exp(-\frac{V_{gs} - V_{th} - 2V_{off}}{2\, n\, v_t})}$$

The unified channel charge density at the source end for both subthreshold and inversion region can therefore be written as

(3.1.4)

$$Q_{chs0} = C_{ox} V_{gsteff}$$

Figures 3-1 and 3-2 show the smoothness of Eq. (3.1.4) from subthreshold to strong inversion regions. The V_{gsteff} expression will be used again in subsequent sections of this chapter to model the drain current.

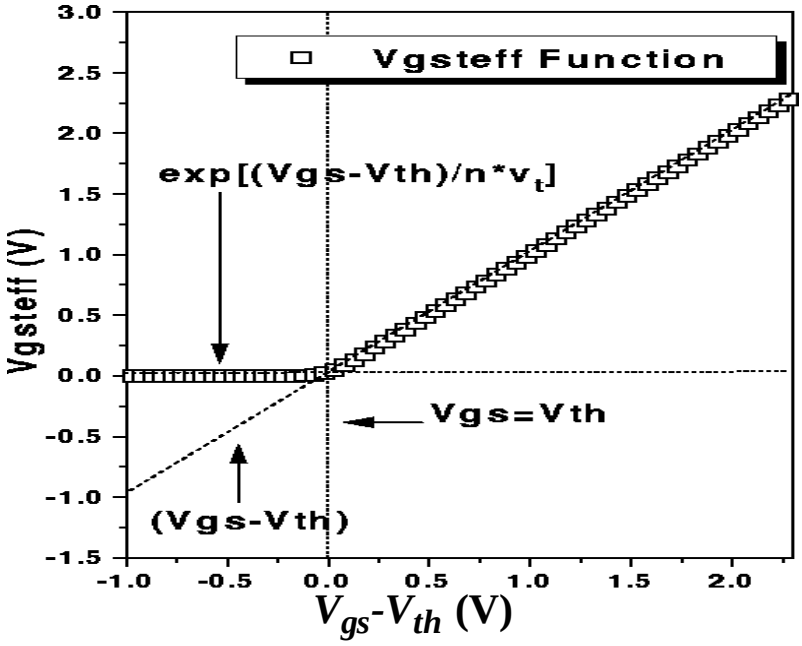

Figure 3-1. The V_{gsteff} function vs. (V_{gs}-V_{th}) in linear scale.

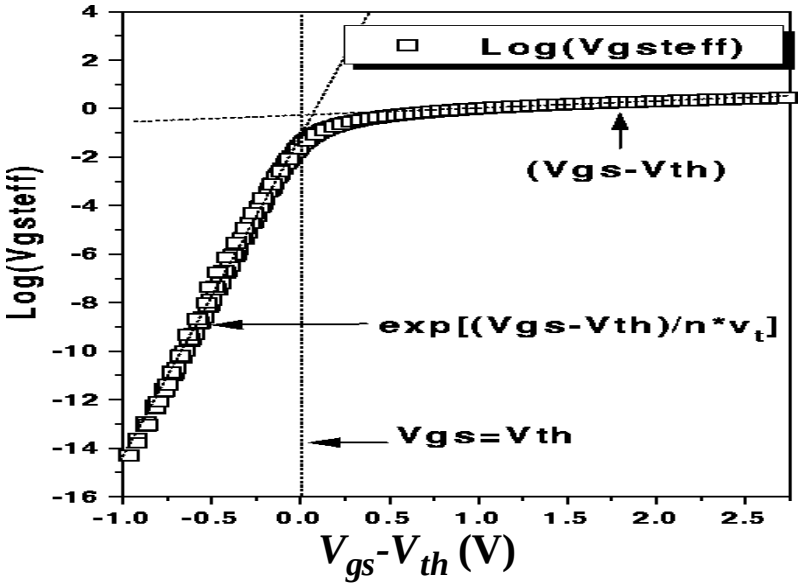

Figure 3-2. V_{gsteff} function vs. (V_{gs}-V_{th}) in log scale.

Eq. (3.1.4) serves as the cornerstone of the unified channel charge expression at the source for small V_{ds}. To account for the influence of V_{ds}, the V_{gsteff} function must keep track of the change in channel potential from the source to the drain. In other words, Eq. (3.1.4) will have to include a y dependence. To initiate this formulation, consider first the re-formulation of channel charge density for the case of **strong inversion**

$$Q_{chs(y)} = C_{ox}(V_{gs} - V_{th} - A_{bulk}V_{F(y)}) \tag{3.1.5}$$

The parameter $V_F(y)$ stands for the quasi-Fermi potential at any given point y, along the channel with respect to the source. This equation can also be written as

$$Q_{chs(y)} = Q_{chs0} + \Delta Q_{chs(y)} \tag{3.1.6}$$

The term $\Delta Q_{chs}(y)$ is the incremental channel charge density induced by the drain voltage at point y. It can be expressed as

$$\Delta Q_{chs(y)} = -CoxA_{bulk}V_{F(y)} \tag{3.1.7}$$

For the **subthreshold region** (V_{gs}<<V_{th}), the channel charge density along the channel from source to drain can be written as

$$\begin{aligned} Q_{chsubs(y)} &= Q_0 \exp\left(\frac{V_{gs} - V_{th} - A_{bulk}V_{F(y)}}{nv_t}\right) \\ &= Q_{chsubs0} \exp\left(-\frac{A_{bulk}V_{F(y)}}{nv_t}\right) \end{aligned} \tag{3.1.8}$$

A Taylor series expansion of the right-hand side of Eq. (3.1.8) yields the following (keeping only the first two terms)

$$Q_{chsubs(y)} = Q_{chsubs0}\left(1 - \frac{A_{bulk}V_{F(y)}}{nv_t}\right) \tag{3.1.9}$$

Analogous to Eq. (3.1.6), Eq. (3.1.9) can also be written as

$$Q_{chsubs(y)} = Q_{chsubs0} + \Delta Q_{chsubs(y)} \tag{3.1.10}$$

The parameter $\Delta Q_{chsubs}(y)$ is the incremental channel charge density induced by the drain voltage in the subthreshold region. It can be written as

$$\Delta Q_{chsubs(y)} = -\frac{A_{bulk}V_{F(y)}}{nv_t} Q_{chsubs0} \tag{3.1.11}$$

Note that Eq. (3.1.9) is valid only when $V_F(y)$ is very small, which is maintained fortunately, due to the fact that Eq. (3.1.9) is only used in the linear regime (i.e. $V_{ds} \leq 2v_t$).

Eqs. (3.1.6) and (3.1.10) both have drain voltage dependencies. However, they are decupled and a unified expression for $Q_{ch}(y)$ is needed. To obtain a unified expression along the channel, we first assume

$$\Delta Q_{ch(y)} = \frac{\Delta Q_{chs(y)}\Delta Q_{chsubs(y)}}{\Delta Q_{chs(y)} + \Delta Q_{chsubs(y)}} \tag{3.1.12}$$

Here, $\Delta Q_{ch}(y)$ is the incremental channel charge density induced by the drain voltage. Substituting Eq. (3.1.7) and (3.1.11) into Eq. (3.1.12), we obtain

(3.1.13)

$$\Delta Q_{ch(y)} = \frac{V_{F(y)}}{Vb} Q_{chs0}$$

where $V_b = (V_{gsteff} + n*v_t)/A_{bulk}$. In order to remove any association between the variable n and bias dependencies (V_{gsteff}) as well as to ensure more precise modeling of Eq. (3.1.8) for linear regimes (under subthreshold conditions), n is replaced by 2. The expression for V_b now becomes

(3.1.14)

$$V_b = \frac{V_{gsteff} + 2v_t}{A_{bulk}}$$

A unified expression for $Q_{ch}(y)$ from subthreshold to strong inversion regimes is now at hand

(3.1.15)

$$Q_{ch(y)} = Q_{chs0}(1 - \frac{V_{F(y)}}{V_b})$$

The variable Q_{chs0} is given by Eq. (3.1.4).

3.2 Unified Mobility Expression

Unified mobility model based on the V_{gsteff} expression of Eq. 3.1.3 is described in the following.

(mobMod = 1) (3.2.1)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})\left(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}\right) + U_b\left(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}\right)^2}$$

To account for depletion mode devices, another mobility model option is given by the following

(mobMod = 2) (3.2.2)

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})\left(\frac{V_{gsteff}}{T_{OX}}\right) + U_b\left(\frac{V_{gsteff}}{T_{OX}}\right)^2}$$

To consider the body bias dependence of Eq. 3.2.1 further, we have introduced the following expression

(For mobMod = 3) (3.2.3)

$$\mu_{eff} = \frac{\mu_o}{1 + \left[U_a\left(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}\right) + U_b\left(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}\right)^2\right](1 + U_c V_{bseff})}$$

3.3 Unified Linear Current Expression

3.3.1 Intrinsic case (R_{ds}=0)

Generally, the following expression [2] is used to account for both drift and diffusion current

$$I_{d(y)} = WQ_{ch(y)}\mu_{ne(y)}\frac{dV_{F(y)}}{dy} \tag{3.3.1}$$

where the parameter $u_{ne}(y)$ can be written as

$$\mu_{ne(y)} = \frac{\mu_{eff}}{1+\frac{E_y}{E_{sat}}} \tag{3.3.2}$$

Substituting Eq. (3.3.2) in Eq. (3.3.1) we get

$$I_{d(y)} = WQ_{chso}\left(1-\frac{V_{F(y)}}{V_b}\right)\frac{\mu_{eff}}{1+\frac{E_y}{E_{sat}}}\frac{dV_{F(y)}}{dy} \tag{3.3.3}$$

Eq. (3.3.3) resembles the equation used to model drain current in the strong inversion regime. However, it can now be used to describe the current characteristics in the subthreshold regime when V_{ds} is very small (V_{ds}<2v_t). Eq. (3.3.3) can now be integrated from the source to drain to get the expression for linear drain current in the channel. This expression is valid from the subthreshold regime to the strong inversion regime

$$I_{ds0} = \frac{W\mu_{eff}Q_{chs0}V_{ds}\left(1-\frac{V_{ds}}{2V_b}\right)}{L\left(1+\frac{V_{ds}}{E_{sat}L}\right)} \tag{3.3.4}$$

3.3.2 Extrinsic Case (R_{ds} > 0)

The current expression when R_{ds} > 0 can be obtained based on Eq. (2.5.9) and Eq. (3.3.4). The expression for linear drain current from subthreshold to strong inversion is:

$$I_{ds} = \frac{I_{dso}}{1 + \frac{R_{ds} I_{dso}}{V_{ds}}} \tag{3.3.5}$$

3.4 Unified V_{dsat} Expression

3.4.1 Intrinsic case (R_{ds}=0)

To get an expression for the electric field as a function of *y* along the channel, we integrate Eq. (3.3.1) from 0 to an arbitrary point *y*. The result is as follows

$$E_y = \frac{I_{dso}}{\sqrt{(WQ_{chs0}\mu_{eff} - \frac{I_{dso}}{E_{sat}})^2 - \frac{2 I_{ds0} W Q_{chs0} \mu_{eff} y}{V_b}}} \tag{3.4.1}$$

If we assume that drift velocity saturates when *Ey=Esat*, we get the following expression for I_{dsat}

$$I_{dsat} = \frac{W \mu_{eff} Q_{chs0} E_{sat} L V_b}{2L(E_{sat} L + V_b)} \tag{3.4.2}$$

Let V_{ds}=V_{dsat} in Eq. (3.3.4) and set this equal to Eq. (3.4.2), we get the following expression for V_{dsat}

$$V_{dsat} = \frac{E_{sat}L(V_{gsteff} + 2v_t)}{A_{bulk}E_{sat}L + V_{gsteff} + 2v_t} \tag{3.4.3}$$

3.4.2 Extrinsic Case (R_{ds}>0)

The V_{dsat} expression for the extrinsic case is formulated from Eq. (3.4.3) and Eq. (2.5.10) to be the following

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \tag{3.4.4a}$$

where

$$a = A_{bulk}{}^2 W_{eff} n_{sat} C_{ox} R_{DS} + (\frac{1}{l} - 1) A_{bulk} \tag{3.4.4b}$$

$$b = -\left((V_{gsteff} + 2v_t)(\frac{2}{l} - 1) + A_{bulk}E_{sat}L_{eff} + 3A_{bulk}(V_{gsteff} + 2v_t) W_{eff} n_{sat} C_{ox} R_{DS} \right) \tag{3.4.4c}$$

$$c = (V_{gsteff} + 2v_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff} n_{sat} C_{ox} R_{DS} \tag{3.4.4d}$$

$$l = A_1 V_{gsteff} + A_2 \tag{3.4.4e}$$

The parameter λ is introduced to account for non-saturation effects. Parameters A_1 and A_2 can be extracted.

3.5 Unified Saturation Current Expression

A unified expression for the saturation current from the subthreshold to the strong inversion regime can be formulated by introducing the V_{gsteff} function into Eq. (2.6.15). The resulting equations are the following

$$I_{ds} = \frac{I_{dso(Vdsat)}}{1+\frac{R_{ds}I_{dso(Vdsat)}}{V_{dsat}}}\left(1+\frac{V_{ds}-V_{dsat}}{V_A}\right)\left(1+\frac{V_{ds}-V_{dsat}}{V_{ASCBE}}\right) \tag{3.5.1}$$

where

$$V_A = V_{Asat} + (1+\frac{P_{vag}V_{gsteff}}{E_{sat}L_{eff}})(\frac{1}{V_{ACLM}}+\frac{1}{V_{ADIBLC}})^{-1} \tag{3.5.2}$$

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{DS}n_{sat}C_{ox}W_{eff}V_{gsteff}[1-\frac{A_{bulk}V_{dsat}}{2(V_{gsteff}+2v_t)}]}{2/l - 1 + R_{DS}n_{sat}C_{ox}W_{eff}A_{bulk}} \tag{3.5.3}$$

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{P_{CLM}A_{bulk}E_{sat}\,litl}(V_{ds}-V_{dsat}) \tag{3.5.4}$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{q_{rout}(1 + P_{DIBLCB}V_{bseff})}\left(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat} + V_{gsteff} + 2v_t}\right) \tag{3.5.5}$$

$$q_{rout} = P_{DIBLC1}\left[\exp(-D_{ROUT}\frac{L_{eff}}{2l_{t0}}) + 2\exp(-D_{ROUT}\frac{L_{eff}}{l_{t0}})\right] + P_{DIBLC2} \tag{3.5.6}$$

$$\frac{1}{V_{ASCBE}} = \frac{P_{scbe2}}{L_{eff}}\exp\left(\frac{-P_{scbe1}\,litl}{V_{ds} - V_{dsat}}\right) \tag{3.5.7}$$

3.6 Single Current Expression for All Operating Regimes of V_{gs} and V_{ds}

The V_{gsteff} function introduced in Chapter 2 gave a unified expression for the linear drain current from subthreshold to strong inversion as well as for the saturation drain current from subthreshold to strong inversion, *separately*. In order to link the continuous linear current with that of the continuous saturation current, a smooth function for V_{ds} is introduced. In the past, several smoothing functions have been proposed for MOSFET modeling [22-24]. The smoothing function used in BSIM3 is similar to that proposed in [24]. The final current equation for both linear and saturation current now becomes

$$I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds}I_{dso(Vdseff)}}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right) \tag{3.6.1}$$

Most of the previous equations which contain V_{ds} and V_{dsat} dependencies are now substituted with the V_{dseff} function. For example, Eq. (3.5.4) now becomes

(3.6.2)

$$V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{P_{CLM} A_{bulk} E_{sat}\, litl} (V_{ds} - V_{dseff})$$

Similarly, Eq. (3.5.7) now becomes

(3.6.3)

$$\frac{1}{V_{ASCBE}} = \frac{P_{scbe2}}{L_{eff}} \exp\left(\frac{-P_{scbe1}\, litl}{V_{ds} - V_{dseff}}\right)$$

The V_{dseff} expression is written as

(3.6.4)

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - d + \sqrt{(V_{dsat} - V_{ds} - d)^2 + 4dV_{dsat}}\right)$$

The expression for V_{dsat} is that given under Section 3.4. The parameter δ in the unit of volts can be extracted. The dependence of V_{dseff} on V_{ds} is given in Figure 3-3. The V_{dseff} function follows V_{ds} in the linear region and tends to V_{dsat} in the saturation region. Figure 3-4 shows the effect of δ on the transition region between linear and saturation regimes.

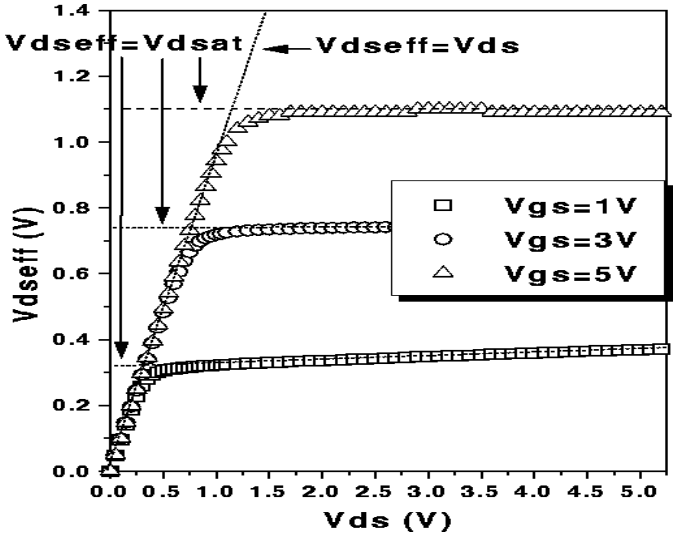

Figure 3-3. V_{dseff} **vs.** V_{ds} **for** δ**=0.01 and different** V_{gs}**.**

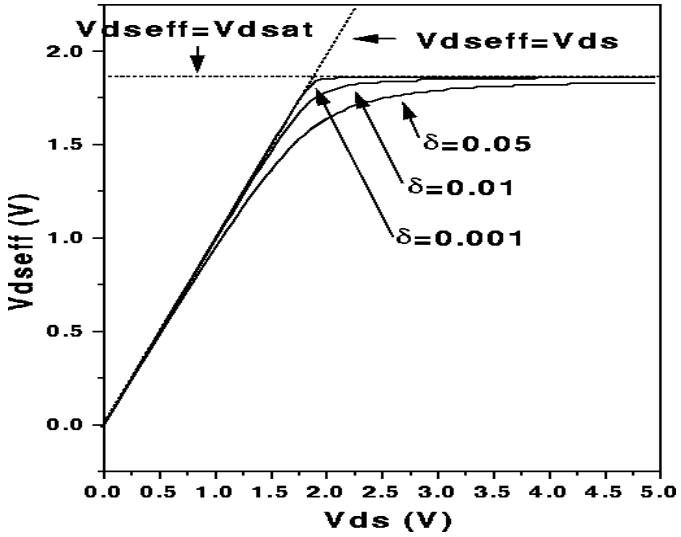

Figure 3-4. V_{dseff} **vs.** V_{ds} **for** V_{gs}**=3V and different** δ **values.**

3.7 Substrate Current

The substrate current in BSIM3v3.2.1 is modeled by

$$I_{sub} = \frac{a_0 + a_1 \cdot L_{eff}}{L_{eff}} \left(V_{ds} - V_{dseff}\right) \exp\left(- \frac{b_0}{V_{ds} - V_{dseff}} \right) \frac{I_{ds0}}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A} \right) \tag{3.7.1}$$

where parameters a_0 and b_0 are impact ionization coefficients; parameter a_1 improves the I_{sub} scalability.

3.8 A Note on V_{bs}

All V_{bs} terms have been substituted with a V_{bseff} expression as shown in Eq. (3.8.1). This is done in order to set an upper bound for the body bias value during simulations. Unreasonable values can occur if this expression is not introduced.

$$V_{bseff} = V_{bc} + 0.5[V_{bs} - V_{bc} - d_1 + \sqrt{(V_{bs} - V_{bc} - d_1)^2 - 4 d_1 V_{bc}}\ ] \tag{3.8.1}$$

where d_1=0.001V.

Parameter V_{bc} is the maximum allowable V_{bs} value and is obtained based on the condition of $dV_{th}/dV_{bs} = 0$ for the V_{th} expression of 2.1.4.

CHAPTER 4: Capacitance Modeling

Accurate modeling of MOSFET capacitance plays equally important role as that of the DC model. This chapter describes the methodology and device physics considered in both intrinsic and extrinsic capacitance modeling in BSIM3v3.3. Detailed model equations are given in Appendix B. One of the important features of BSIM3v3.2 is introduction of a new intrinsic capacitance model (capMod=3 as the default model), considering the finite charge thickness determined by quantum effect, which becomes more important for thinner T_{ox} CMOS technologies. This model is smooth, continuous and accurate throughout all operating regions.

4.1 General Description of Capacitance Modeling

BSIM3v3.3 models capacitance with the following general features:

- Separate effective channel length and width are used for capacitance models.
- The intrinsic capacitance models, capMod=0 and 1, use piece-wise equations. capMod=2 and 3 are smooth and single equation models; therefore both charge and capacitance are continous and smooth over all regions.
- Threshold voltage is consistent with DC part except for capMod=0, where a long-channel V_{th} is used. Therefore, those effects such as body bias, short/narrow channel and DIBL effects are explicitly considered in capMod=1, 2, and 3.
- Overlap capacitance comprises two parts: (1) a bias-independent component which models the effective overlap capacitance between the gate and the heavily doped source/drain; (2) a gate-bias dependent component between the gate and the lightly doped source/drain region.

- Bias-independent fringing capacitances are added between the gate and source as well as the gate and drain.

Name	Function	Default	Unit
capMod	Flag for capacitance models	3	(True)
vfbcv	the flat-band voltage for capMod = 0	-1.0	(V)
acde	Exponential coefficient for X_{DC} for accumulation and depletion regions	1	(m/V)
moin	Coefficient for the surface potential	15	($V^{0.5}$)
cgso	Non-LDD region G/S overlap C per channel length	Calculated	F/m
cgdo	Non-LDD region G/D overlap C per channel length	Calculated	F/m
CGS1	Lightly-doped source to gate overlap capacitance	0	(F/m)
CGD1	Lightly-doped drain to gate overlap capacitance	0	(F/m)
CKAPPA	Coefficient for lightly-doped overlap capacitance	0.6	
CF	Fringing field capacitance	equation (4.5.1)	(F/m)
CLC	Constant term for short channel model	0.1	µm
CLE	Exponential term for short channel model	0.6	
DWC	Long channel gate capacitance width offset	Wint	µm
DLC	Long channel gate capacitance length offset	Lint	µm

Table 4-1. Model parameters in capacitance models.

4.2 Geometry Definition for C-V Modeling

For capacitance modeling, MOSFET's can be divided into two regions: intrinsic and extrinsic. The intrinsic capacitance is associated with the region between the metallurgical source and drain junction, which is defined by the effective length

(L_{active}) and width (W_{active}) when the gate to S/D region is at flat band voltage. L_{active} and W_{active} are defined by Eqs. (4.2.1) through (4.2.4).

$$L_{active} = L_{drawn} - 2dL_{eff} \tag{4.2.1}$$

$$W_{active} = W_{drawn} - 2dW_{eff} \tag{4.2.2}$$

$$dL_{eff} = DLC + \frac{Llc}{L^{L\ln}} + \frac{Lwc}{W^{Lwn}} + \frac{Lwlc}{L^{L\ln}W^{Lwn}} \tag{4.2.3}$$

$$dW_{eff} = DWC + \frac{Wlc}{L^{W\ln}} + \frac{Wwc}{W^{Wwn}} + \frac{Wwlc}{L^{W\ln}W^{Wwn}} \tag{4.2.4}$$

The meanings of *DWC* and *DLC* are different from those of *Wint* and *Lint* in the I-V model. L_{active} and W_{active} are the effective length and width of the intrinsic device for capacitance calculations. Unlike the case with I-V, we assumed that these dimensions have no voltage bias dependence. The parameter dL_{eff} is equal to the source/drain to gate overlap length plus the difference between drawn and actual POLY CD due to processing (gate printing, etching and oxidation) on one side. Overall, a distinction should be made between the effective channel length extracted from the capacitance measurement and from the I-V measurement.

Traditionally, the L_{eff} extracted during I-V model characterization is used to gauge a technology. However this L_{eff} does not necessarily carry a physical meaning. It is just a parameter used in the I-V formulation. This L_{eff} is therefore very sensitive to the I-V equations used and also to the conduction characteristics of the LDD

region relative to the channel region. A device with a large L_{eff} and a small parasitic resistance can have a similar current drive as another with a smaller L_{eff} but larger R_{ds}. In some cases L_{eff} can be larger than the polysilicon gate length giving L_{eff} a dubious physical meaning.

The L_{active} parameter extracted from the capacitance method is a closer representation of the metallurgical junction length (physical length). Due to the graded source/ drain junction profile the source to drain length can have a very strong bias dependence. We therefore define L_{active} to be that measured at gate to source/drain flat band voltage. If *DWC*, *DLC* and the newly-introduced length/ width dependence parameters (*Llc*, *Lwc*, *Lwlc*, *Wlc*, *Wwc* and *Wwlc*) are not specified in technology files, BSIM3v3.3 assumes that the DC bias-independent L_{eff} and W_{eff} (Eqs. (2.8.1) - (2.8.4)) will be used for C-V modeling, and *DWC*, *DLC*,*Llc*, *Lwc*, *Lwlc*, *Wlc*, *Wwc* and *Wwlc* will be set equal to the values of their DC counterparts (default values).

4.3 Methodology for Intrinsic Capacitance Modeling

4.3.1 Basic Formulation

To ensure charge conservation, terminal charges instead of the terminal voltages are used as state variables. The terminal charges Q_g, Q_b, Q_s, and Q_d are the charges associated with the gate, bulk, source, and drain termianls, respectively. The gate charge is comprised of mirror charges from these components: the channel inversion charge (Q_{inv}), accumulation charge (Q_{acc}) and the substrate depletion charge (Q_{sub}).

The accumulation charge and the substrate charge are associated with the substrate while the channel charge comes from the source and drain terminals

(4.3.1)

$$\begin{cases} Q_g = -\left(Q_{sub} + Q_{inv} + Q_{acc}\right) \\ Q_b = Q_{acc} + Q_{sub} \\ Q_{inv} = Q_s + Q_d \end{cases}$$

The substrate charge can be divided into two components - the substrate charge at zero source-drain bias (Q_{sub0}), which is a function of gate to substrate bias, and the additional non-uniform substrate charge in the presence of a drain bias (dQ_{sub}). Q_g now becomes

(4.3.2)

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + dQ_{sub}\right)$$

The total charge is computed by integrating the charge along the channel. The threshold voltage along the channel is modified due to the non-uniform substrate charge by

(4.3.3)

$$V_{th}(y) = V_{th}(0) + \left(A_{bulk} - 1\right)V_y$$

(4.3.4)

$$\begin{cases} Q_c = W_{active}\int_0^{L_{active}} q_c dy = -W_{active}C_{ox}\int_0^{L_{active}}\left(V_{gt} - A_{bulk}V_y\right)dy \\ Q_g = W_{active}\int_0^{L_{active}} q_g dy = W_{active}C_{ox}\int_0^{L_{active}}\left(V_{gt} + V_{th} - V_{FB} - \Phi_s - V_y\right)dy \\ Q_b = W_{active}\int_0^{L_{active}} q_b dy = -W_{active}C_{ox}\int_0^{L_{active}}\left(V_{th} - V_{FB} - \Phi_s + \left(A_{bulk} - 1\right)V_y\right)dy \end{cases}$$

Substituting the following

$$dy = \frac{dV_y}{e_y}$$

and

$$I_{ds} = \frac{W_{active}\mu_{eff}C_{ox}}{L_{active}}\left(V_{gt} - \frac{A_{bulk}}{2}V_{ds}\right)V_{ds} = W_{active}\mu_{eff}C_{ox}\left(V_{gt} - A_{bulk}V_y\right)E_y \tag{4.3.5}$$

into Eq. (4.3.4), we have the following upon integration

$$\begin{cases} Q_c = -W_{active}L_{active}C_{ox}\left(V_{gt} - \dfrac{A_{bulk}}{2}V_{ds} + \dfrac{A_{bulk}{}^2V_{ds}{}^2}{12\left(V_{gt} - \dfrac{A_{bulk}}{2}V_{ds}\right)}\right) \\ Q_g = -Q_{sub\,0} + W_{active}L_{active}C_{ox}\left(V_{gt} - \dfrac{V_{ds}}{2} + \dfrac{A_{bulk}V_{ds}{}^2}{12\left(V_{gt} - \dfrac{A_{bulk}}{2}V_{ds}\right)}\right) \\ Q_b = -Q_g - Q_c = Q_{sub} + Q_{sub\,0} + Q_{acc} \end{cases} \tag{4.3.6}$$

where

(4.3.7)

$$\begin{cases} Q_{sub\,0} = -W_{active} L_{active} \sqrt{2 e_{si} q N_{sub} (2\Phi_B - V_{bs})} \\ dQ_{sub} = W_{active} L_{active} C_{ox} \left(\dfrac{1 - A_{bulk}}{2} V_{ds} + \dfrac{A_{bulk} (A_{bulk} - 1) V_{ds}^{\ 2}}{12 \left(V_{gt} - \dfrac{A_{bulk}}{2} V_{ds} \right)} \right) \end{cases}$$

The inversion charges are supplied from the source and drain electrodes such that $Q_{inv} = Q_s + Q_d$. The ratio of Q_d and Q_s is the charge partitioning ratio. Existing charge partitioning schemes are 0/100, 50/50 and 40/60 (*XPART* = 0, 0.5 and 1) which are the ratios of Q_d to Q_s in the saturation region. We will revisit charge partitioning in Section 4.3.4.

All capacitances are derived from the charges to ensure charge conservation. Since there are four terminals, there are altogether 16 components. For each component

(4.3.8)

$$C_{ij} = \frac{\P Q_i}{\P V_j}$$

where *i* and *j* denote the transistor terminals. In addition

$$\sum_i C_{ij} = \sum_j C_{ij} = 0$$

4.3.2 Short Channel Model

In deriving the long channel charge model, mobility is assumed to be constant with no velocity saturation. Therefore in saturation region ($V_{ds} \geq V_{dsat}$), the carrier density at the drain end is zero. Since no channel length modulation is assumed, the channel charge will remain a constant throughout the saturation region. In essence, the channel charge in the

saturation region is assumed to be zero. This is a good approximation for long channel devices but fails when $L_{eff} < 2$ μm. If we define a drain bias, $V_{dsat,cv}$, in which the channel charge becomes a constant, we will find that $V_{dsat,cv}$ in general is larger than V_{dsat} but smaller than the long channel V_{dsat}, given by V_{gt}/A_{bulk}. However, in old long channel charge models, $V_{dsat,cv}$ is set to V_{gt}/A_{bulk} independent of channel length. Consequently, C_{ij}/L_{eff} has no channel length dependence (Eqs. (4.3.6), (4.37)). A pseudo short channel modification from the long channel has been used in the past. It involved the parameter A_{bulk} in the capacitance model which was redefined to be equal to V_{gt}/V_{dsat}, thereby equating $V_{dsat,cv}$ and V_{dsat}. This overestimated the effect of velocity saturation and resulted in a smaller channel capacitance.

The difficulty in developing a short channel model lies in calculating the charge in the saturation region. Although current continuity stipulates that the charge density in the saturation region is almost constant, it is difficult to calculate accurately the length of the saturation region. Moreover, due to the exponentially increasing lateral electric field, most of the charge in the saturation region are not controlled by the gate electrode. However, one would expect that the total charge in the channel will exponentially decrease with drain bias. Experimentally,

$$V_{dsat,iv} < V_{dsat,cv} < V_{dsat,iv}\Big|_{L_{active}\to\infty} = \frac{V_{gsteff,cv}}{A_{bulk}} \tag{4.3.9}$$

and $V_{dsat,cv}$ is modeled by the following

(4.3.10a)

$$V_{dsat,cv} = \frac{V_{gsteff,cv}}{A_{bulk}\left(1+\left(\frac{CLC}{L_{active}}\right)^{CLE}\right)}$$

(4.3.10b)

$$V_{gsteff,cv} = noff \cdot nv_t \ln\left(1+\exp\left(\frac{V_{gs}-V_{th}-voffcv}{noff \cdot nv_t}\right)\right)$$

Parameters *noff* and *voffcv* are introduced to better fit measured data above subthreshold regions. The parameter A_{bulk} is substituted A_{bulk0} in the long channel equation by

(4.3.11)

$$A_{bulk}' = A_{bulk0}\left(1+\left(\frac{\mathrm{CLC}}{L_{active}}\right)^{\mathrm{CLE}}\right)$$

(4.3.11a)

$$A_{bulk} = \left(1+\frac{K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}}\left(\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{X_J X_{dep}}}+\frac{B_0}{W_{eff}'+B_1}\right)\right)\cdot\frac{1}{1+Keta V_{bseff}}$$

In (4.3.11), parameters *CLC* and *CLE* are introduced to consider channel-length modulation.

4.3.3 Single Equation Formulation

Traditional MOSFET SPICE capacitance models use piece-wise equations. This can result in discontinuities and non-smoothness at transition regions. The following describes single-equation formulation for charge, capacitance and voltage modeling in capMod=2 and 3.

(a) Transition from depletion to inversion region

The biggest discontinuity is the inversion capacitance at threshold voltage. Conventional models use step functions and the inversion capacitance changes abruptly from 0 to C_{ox}. Concurrently, since the substrate charge is a constant, the substrate capacitance drops abruptly to 0 at threshold voltage. Both of these effects can cause oscillation during circuit simulation. Experimentally, capacitance starts to increase almost quadratically at ~0.2V below threshold voltage and levels off at ~0.3V above threshold voltage. For analog and low power circuits, an accurate capacitance model around the threshold voltage is very important.

The non-abrupt channel inversion capacitance and substrate capacitance model is developed from the I-V model which uses a single equation to formulate the subthreshold, transition and inversion regions. The new channel inversion charge model can be modified to any charge model by substituting V_{gt} with $V_{gsteff,cv}$ as in the following

$$Q\left(_{Vgt}\right) = Q\left(V_{gsteff,CV}\right) \tag{4.3.12}$$

Capacitance now becomes

(4.3.13)

$$C(V_{gt}) = C(V_{gsteffCV})\frac{\partial V_{gsteffCV}}{V_{gs,ds,bs}}$$

The "inversion" charge is always non-zero, even in the accumulation region. However, it decreases exponentially with gate bias in the subthreshold region.

(b) Transition from accumulation to depletion region

An effective flatband voltage V_{FBeff} is used to smooth out the transition between accumulation and depletion regions. It affects the accumulation and depletion charges

(4.3.14)

$$V_{FBeff} = vfb - 0.5\left\{V_3 + \sqrt{V_3^2 + 4d_3 vfb}\right\} \quad where\, V_3 = vfb - V_{gs} + V_{bseff} - d_3;\ d_3 = 0.02V$$

(4.3.15)

$$vfb = V_{th} - \Phi_s - K_{1ox}\sqrt{\Phi_s - V_{bseff}}$$

In BSIM3v3.3, a bias-independent V_{th} is used to calculate *vfb* for capMod = 1, 2 and 3. For capMod = 0, *Vfbcv* is used instead (refer to the appendices).

(4.3.16)

$$Q_{acc} = -W_{active}L_{active}C_{ox}\left(V_{FBeff} - vfb\right)$$

(4.3.17)

$$Q_{sub0} = -W_{active}L_{active}C_{ox}\cdot\frac{K_{1ox}^{\ 2}}{2}\left(-1+\sqrt{1+\frac{4\left(V_{gs}-V_{FBeff}-V_{gsteffCV}-V_{bseff}\right)}{K_{1ox}^{\ 2}}}\right)$$

(c) Transition from linear to saturation region

An effective V_{ds}, V_{cveff}, is used to smooth out the transition between linear and saturation regions. It affects the inversion charge.

(4.3.18)

$$V_{cveff} = V_{dsat,cv} - 0.5\left\{V_4 + \sqrt{V_4^2 + 4d_4 V_{dsat,cv}}\right\} \quad where V_4 = V_{dsat,cv} - V_{ds} - d_4; d_4 = 0.02V$$

(4.3.19)

$$Q_{inv} = -W_{active} L_{active} C_{ox} \left(\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right) + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

(4.3.20)

$$dQ_{sub} = W_{active} L_{active} C_{ox} \left(\frac{1 - A_{bulk}'}{2} V_{cveff} - \frac{\left(1 - A_{bulk}'\right) A_{bulk}' V_{cveff}^2}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

Below is a list of all the three partitioning schemes for the inversion charge:

(i) The 50/50 charge partition

This is the simplest of all partitioning schemes in which the inversion charges are assumed to be contributed equally from the source and drain nodes.

(4.3.21)

$$Q_s = Q_d = 0.5Q_{inv} = -\frac{W_{active}L_{active}C_{ox}}{2}\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2}V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2}V_{cveff}\right)}\right)$$

(ii) The 40/60 channel-charge partition

This is the most physical model of the three partitioning schemes in which the channel charges are allocated to the source and drain terminals by assuming a linear dependence on the position *y*.

(4.3.22)

$$\begin{cases} Q_s = W_{active}\int_0^{L_{active}} q_c\left(1 - \frac{y}{L_{active}}\right)dy \\ Q_d = W_{active}\int_0^{L_{active}} q_c\frac{y}{L_{active}}dy \end{cases}$$

(4.3.23)

$$Qs = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffCV} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffCV}^3 - \frac{4}{3}V_{gsteffCV}^2 A_{bulk}'V_{cveff} + \frac{2}{3}V_{gsteffCV}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

(4.3.24)

$$Q_d = \frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffcv}^3 - \frac{5}{3}V_{gsteffcv}^2\left(A_{bulk}'V_{cveff}\right) + V_{gsteffcv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

(iii) The 0/100 Charge Partition

In fast transient simulations, the use of a quasi-static model may result in a large unrealistic drain current spike. This partitioning scheme is developed to artificially suppress the drain current spike by assigning all inversion

charges in the saturation region to the source electrode. Notice that this charge partitioning scheme will still give drain current spikes in the linear region and aggravate the source current spike problem.

(4.3.25)

$$Q_s = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteff,c}}{2} + \frac{A_{bulk}' V_{cveff}}{4} - \frac{\left(A_{bulk}' V_{cveff}\right)^2}{24\left(V_{gsteff,c} - \frac{A_{bulk}'}{2} V_{cveff}\right)} \right)$$

(4.3.26)

$$Q_d = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteff,c}}{2} - \frac{3A_{bulk}' V_{cveff}}{4} + \frac{\left(A_{bulk}' V_{cveff}\right)^2}{8\left(V_{gsteff,c} - \frac{A_{bulk}'}{2} V_{cveff}\right)} \right)$$

(d) Bias-dependent threshold voltage effects on capacitance

Consistent Vth between DC and CV is important for acurate circuit simulation. capMod=1, 2 and 3 use the same Vth as in the DC model. Therefore, those effects, such as body bias, DIBL and short-channel effects are all explicitly considered in capacitance modeling. In deriving the capacitances additional differentiations are needed to account for the dependence of threshold voltage on drain and substrate biases.

4.4 Charge-Thickness Capacitance Model

Current MOSFET models in SPICE generally overestimate the intrinsic capacitance and usually are not smooth at V_{fb} and V_{th}. The discrepancy is more

pronounced in thinner T_{ox} devices due to the assumption of inversion and accumulation charge being located at the interface. The charge sheet model or the band-gap(E_g)-reduction model of quantum effect [31] improves the Φ_B and thus the V_{th} modeling but is inadequate for CV because they assume zero charge thickness. Numerical quantum simulation results in Figure 4-1 indicate the significant charge thickness in all regions of the CV curves [32].

This section describes the concepts used in the charge-thichness model (CTM). Appendix B lists all charge equations. A full report and anaylsis of the CTM model can be found in [32].

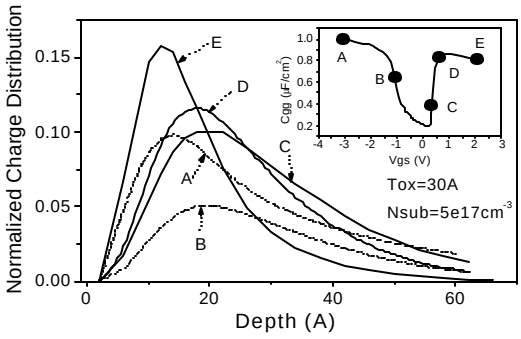

Figure 4-1. Charge distribution from numerical quantum simulations show significant charge thickness at various bias conditions shown in the inset.

CTM is a charge-based model and therefore starts with the DC charge thicknss, X_{DC}. The charge thicknss introduces a capacitance in series with C_{ox} as illustrated in Figure 4-2, resulting in an effective C_{ox}, C_{oxeff}. Based on numerical self-consistent solution of Shrodinger, Poisson and Fermi-Dirac equations, universal and analytical X_{DC} models have been developed. C_{oxeff} can be expressed as

(4.4.1)

$$C_{oxeff} = \frac{C_{ox}C_{cen}}{C_{ox} + C_{cen}}$$

where

$$C_{cen} = {e_{si}}/{X_{DC}}$$

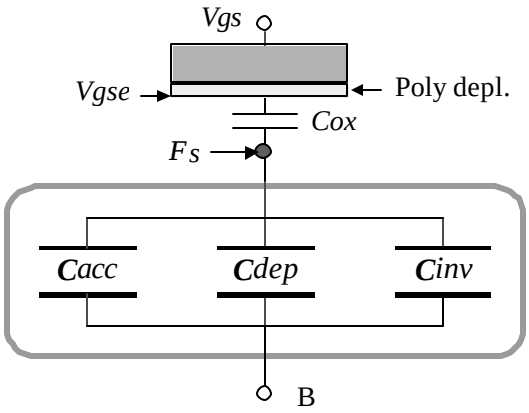

Figure 4-2. Charge-thickness capacitance concept in CTM. V_{gse} accounts for the poly depletion effect.

(i) X_{DC} for accumulation and depletion

The DC charge thickness in the accumulation and depletion regions can be expressed by [32]

(4.4.2)

$$X_{DC} = \frac{1}{3}L_{debye}\exp\left[acde\cdot\left(\frac{N_{sub}}{2\times10^{16}}\right)^{-0.25}\cdot\frac{V_{gs}-V_{bs}-V_{fb}}{T_{ox}}\right]$$

where X_{DC} is in the unit of cm and (V_{gs} - V_{bs} - *vfb*) / T_{ox} has a unit of MV/cm. The model parameter *acde* is introduced for better fitting with a default value of 1. For numerical statbility, (4.4.2) is replaced by (4.4.3)

$$X_{DC} = X_{\max} - \frac{1}{2}\left(X_0 + \sqrt{X_0^2 + 4d_x X_{\max}}\right) \tag{4.4.3}$$

where

$$X_0 = X_{\max} - X_{DC} - d_x$$

and $X_{max}=L_{debye}/3$; $\delta_x = 10^{-3} T_{ox}$.

(ii) X_{DC} of inversion charge

The inversion charge layer thichness [32] can be formulated as

$$X_{DC} = \frac{1.9\times10^{-7}}{1+\left(\frac{V_{gsteff}+4(V_{th}-vfb-2\Phi_B)}{2T_{ox}}\right)^{0.7}} \quad [cm] \tag{4.4.4}$$

Through *vfb* in (4.3.30), this equation is found to be applicable to N^+ or P^+ poly-Si gates as well as other future gate materials. Figure 4-3 illustrates the universality of (4.3.30) as verified by the numerical quantum simulations, where the *x*-axe

represents the boundary conditions (the average of the electric fields at the top and the bottom of the charge layers) of the Schrodinger and the Poisson equations.

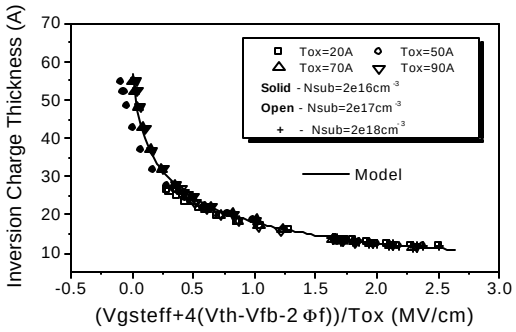

Figure 4-3. For all T_{ox} and N_{sub}, modeled inversion charge thickness agrees with numerical quantum simulations.

(iii) Body charge thichness in inversion

In inversion region, the body charge thickness effect is accurately modeled by including the deviation of the surface potential Φ_s from $2\Phi_B$ [32]

$$\Phi_d = \Phi_s - 2\Phi_B = n_t \ln\left(\frac{V_{gsteffcv}\cdot\left(V_{gsteffcv} + 2K_{1ox}\sqrt{2\Phi_B}\right)}{moin\,K_{1ox}n_t^2} + 1\right) \tag{4.4.5}$$

where the model parameter *moin* (defaulting to 15) is introduced for better fit to different technologies. The inversion channel charge density is therefore derived as

$$q_{inv} = -C_{oxeff}\cdot\left(V_{gsteffcv} - \Phi_d\right) \tag{4.4.6}$$

Figure 4-4 illustrates the universality of CTM model by compariing C_{gg} of a SiON/ Ta_2O_5/TiN gate stack structure with an equivalent T_{ox} of 1.8nm between data, numerical quantum simulation and modeling [32].

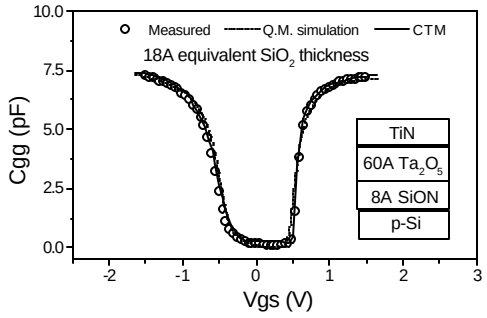

Figure 4-4. Universality of CTM is demonstrated by modeling the C_{gg} of 1.8nm equivalent T_{ox} NMOSFET with SiON/Ta_2O_5/TiN gate stack.

4.5 Extrinsic Capacitance

4.5.1 Fringing Capacitance

The fringing capacitance consists of a bias independent outer fringing capacitance and a bias dependent inner fringing capacitance. Only the bias independent outer fringing capacitance is implemented. Experimentally, it is virtually impossible to separate this capacitance with the overlap capacitance. Nonetheless, the outer fringing capacitance can be theoretically calculated by

(4.5.1)

$$CF = \frac{2e_{ox}}{p}\ln\left(1+\frac{t_{poly}}{T_{ox}}\right)$$

where t_{poly} is equal to 4×10^{-7} m. *CF* is a model parameter.

4.5.2 Overlap Capacitance

An accurate model for the overlap capacitance is essential. This is especially true for the drain side where the effect of the capacitance is amplified by the transistor gain. In old capacitance models this capacitance is assumed to be bias independent. However, experimental data show that the overlap capacitance changes with gate to source and gate to drain biases. In a single drain structure or the heavily doped S/D to gate overlap region in a LDD structure the bias dependence is the result of depleting the surface of the source and drain regions. Since the modulation is expected to be very small, we can model this region with a constant capacitance. However in LDD MOSFETs a substantial portion of the LDD region can be depleted, both in the vertical and lateral directions. This can lead to a large reduction of overlap capacitance. This LDD region can be in accumulation or depletion. We use a single equation for both regions by using such smoothing parameters as $V_{gs,overlap}$ and $V_{gd,overlap}$ for the source and drain side, respectively. Unlike the case with the intrinsic capacitance, the overlap capacitances are reciprocal. In other words, $C_{gs,overlap}$ = $C_{sg,overlap}$ and $C_{gd,overlap} = C_{dg,overlap}$.

(i) Source Overlap Charge

(4.5.2)

$$\frac{Q_{overlap,s}}{W_{active}} = CGS0 \cdot V_{gs} + CGS1\left(V_{gs} - V_{gs,overlap} - \frac{CKAPPA}{2}\left(-1 + \sqrt{1 - \frac{4V_{gs,overlap}}{CKAPPA}}\right)\right)$$

(4.5.3)

$$V_{gs,overlap} = \frac{1}{2}\left(V_{gs} + d_1 - \sqrt{(V_{gs} + d_1)^2 + 4d_1}\right), \quad d_1 = 0.02V$$

where *CKAPPA* is a model parameter. *CKAPPA* is related to the average doping of LDD region by

$$CKAPPA = \frac{2\varepsilon_{si} q N_{LDD}}{C_{ox}^{\ 2}}$$

The typical value for N_{LDD} is 5×10^{17} cm^{-3}.

(ii) Drain Overlap Charge

(4.5.4)

$$\frac{Q_{overlap,d}}{W_{active}} = CGD0 \cdot V_{gd} + CGD1\left(V_{gd} - V_{gd,overlap} - \frac{CKAPPA}{2}\left(-1 + \sqrt{1 - \frac{4V_{gd,overlap}}{CKAPPA}}\right)\right)$$

(4.5.5)

$$V_{gd,overlap} = \frac{1}{2}\left(V_{gd} + d_1 - \sqrt{(V_{gd} + d_1)^2 + 4d_1}\right), \quad d_1 = 0.02V$$

(iii) Gate Overlap Charge

(4.5.6)

$$Q_{overlap,g} = -\left(Q_{overlap,d} + Q_{overlap,s} + (CGB0 \cdot L_{active}) \cdot V_{gb}\right)$$

In the above expressions, if *CGS*0 and *CGD*0 (the overlap capacitances between the gate and the heavily doped source/drain regions, respectively) are not given, they are calculated according to the following

*CGS*0 = (*DLC***C*$_{ox}$*)* - *CGS*1 (if *DLC* is given and *DLC* > *0*)

*CGS*0 = 0 (if the previously calculated *CGS*0 is less than 0)

*CGS*0 = 0.6 $Xj*C_{ox}$ (otherwise)

*CGD*0 = ($DLC*C_{ox}$) - *CGD*1 (if *DLC* is given and *DLC* > *CGD*1/*Cox*)

*CGD*0 = 0 (if previously calculated *CDG*0 is less than 0)

*CGD*0 = 0.6 $Xj*C_{ox}$ (otherwise).

*CGB*0 in Eqn. (4.5.6) is a model parameter, which represents the gate-to-body overlap capacitance per unit channel length.

CHAPTER 5: Non-Quasi Static Model

5.1 Background Information

As MOSFET's become more performance-driven, the need for accurate prediction of circuit performance near cut-off frequency or under very rapid transient operation becomes more essential. However, most SPICE MOSFET models are based on Quasi-Static (QS) assumptions. In other words, the finite charging time for the inversion layer is ignored. When these models are used with 40/60 charge partitioning, unrealistically drain current spikes frequently occur [33]. In addition, the inability of these models to accurately simulate channel charge re-distribution causes problems in fast switched-capacitor type circuits. Many Non-Quasi-Static (NQS) models have been published, but these models (1) assume, unrealistically, no velocity saturation and (2) are complex in their formulations with considerable simulation time.

5.2 The NQS Model

The NQS model has been re-implemented in BSIM3v3.2 to improve the simulation performance and accuracy. This model is based on the channel charge relaxation time approach. A new charge partitioning scheme is used, which is physically consistent with quasi-static CV model.

5.3 Model Formulation

The channel of a MOSFET is analogous to a bias dependent RC distributed transmission line (Figure 5-1a). In the Quasi-Static (QS) approach, the gate capacitor node is lumped with both the external source and drain nodes (Figure 5-1b). This ignores the finite time for the channel charge to build-up. One Non-Quasi-Static (NQS) solution is to represent the channel as *n* transistors in series (Figure 5-1c). This model, although accurate, comes at the expense of simulation time. The NQS model in BSIM3v3.2.2 was based on the circuit of Figure 5-1d. This Elmore equivalent circuit models channel charge build-up accurately because it retains the lowest frequency pole of the original RC network (Figure 5-1a). The NQS model has two parameters as follows. The model flag, nqsMod, is now only an element (instance) parameter, no longer a model parameter. To turn on the NQS model, set nqsMod=1 in the instance statement. nqsMod defaults to zero with this model off.

Name	Function	Default	Unit
nqsMod	Instance flag for the NQS model	0	none
elm	Elmore constant	5	none

Table 5-1. NQS model and instance parameters.

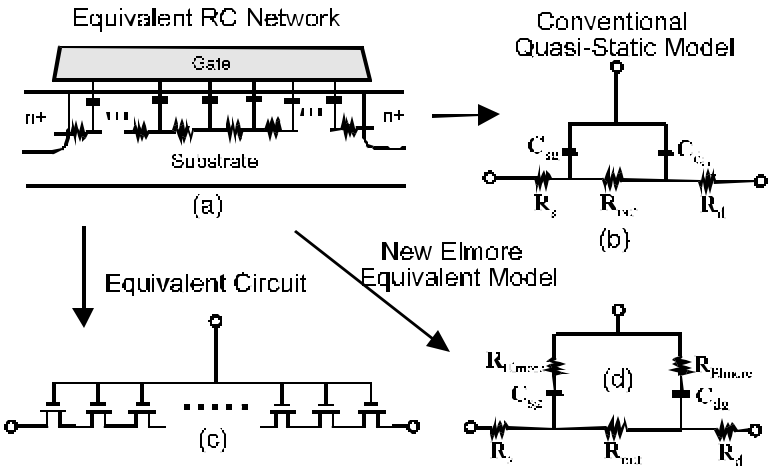

Figure 5-1. Quasi-Static and Non-Quasi-Static models for SPICE analysis.

5.3.1 SPICE sub-circuit for NQS model

Figure 5-2 gives the RC-subcircuit of NQS model for SPICE implementation. An additional node, $Q_{def}(t)$, is created to keep track of the amount of deficit/surplus channel charge necessary to reach the equilibrium based on the relaxation time approach. The bias-dependent resistance $\boldsymbol{R}$ ($1/R=G_{tau}$) can be determined from the RC time constant (τ). The current source $i_{cheq}(t)$ results from the equilibrium channel charge, $Q_{cheq}(t)$. The capacitor $\boldsymbol{C}$ is multiplied by a scaling factor C_{fact} (with a typical value of 1×10^{-9}) to improve simulation accuracy. Q_{def} now becomes

$$Q_{def}(t)=V_{def}\times(1\cdot C_{fact}) \tag{5.3.1}$$

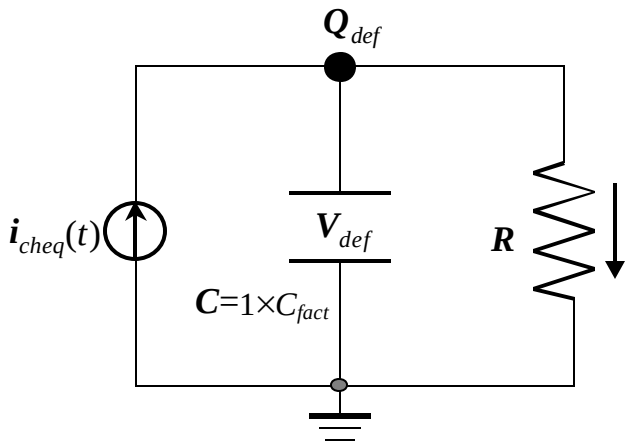

Figure 5-2. NQS sub-circuit for SPICE implementation.

5.3.2 Relaxation time

The relaxation time τ is modeled as two components: τ_{drift} and τ_{diff}. In strong inversion region, τ is determined by τ_{drift}, which, in turn, is determined by the Elmore resistance R_{elm}; in subthreshold region, τ_{diff} dominates. τ is expressed by

$$\frac{1}{t} = \frac{1}{t_{diff}} + \frac{1}{t_{drift}} \tag{5.3.2}$$

R_{elm} in strong inversoin is calculated from the channel resistance as

$$R_{elm} = \frac{L_{eff}^{\ 2}}{elm \cdot m_0 Q_{ch}} \approx \frac{L_{eff}^{\ 2}}{elm \cdot m_0 Q_{cheq}} \tag{5.3.3}$$

where *elm* is the Elmore constant of the RC channel network with a theorectical value of 5. The quasi-static (or equilibrium) channel charge $Q_{cheq}(t)$, equal to Q_{inv} of capMod=0, 1, 2 and 3, is used to approximate the actual channel charge $Q_{ch}(t)$. τ_{drift} is formulated as

(5.3.4)

$$t_{drift} \approx R_{elm} \cdot C_{ox} W_{eff} L_{eff} \approx \frac{C_{ox} W_{eff} L_{eff}^{3}}{elm \cdot m_0 Q_{cheq}}$$

τ_{diff} has the form of

(5.3.5)

$$t_{diff} = \frac{q L_{eff}^{2}}{16 \cdot m_0 kT}$$

5.3.3 Terminal charging current and charge partitioning

Considering both the transport and charging component, the total current related to the terminals D, G and S can be written as

(5.3.6)

$$i_{D,G,S}(t) = I_{D,G,S}(\mathrm{DC}) + \frac{\partial Q_{d,g,s}(t)}{\partial t}$$

Based on the relaxation time approach, the terminal charge and corresponding charging current can be formulated by

(5.3.7)

$$Q_{def}(t) = Q_{cheq}(t) - Q_{ch}(t)$$

and

(5.3.8a)

$$\frac{\partial Q_{def}(t)}{\partial t} = \frac{\partial Q_{cheq}(t)}{\partial t} - \frac{Q_{def}(t)}{t}$$

(5.3.8b)

$$\frac{\partial Q_{d,g,s}(t)}{\partial t} = D, G, S_{xpart} \frac{Q_{def}(t)}{t}$$

where D,G,S_{xpart} are the NQS channel charge partitioning number for terminals D, G and S, respectively; $D_{xpart} + S_{xpart} = 1$ and $G_{xpart} = -1$. It is important for D_{xpart} and S_{xpart} to be consistent with the quasi-static charge partitioning number *XPART* and to be equal ($D_{xpart} = S_{xpart}$) at V_{ds}=0 (which is not the case in the previous version), where the transistor operation mode changes (between forward and reverse modes). Based on this consideration, D_{xpart} is now formulated as

(5.3.9)

$$D_{xpart} = \frac{Q_d}{Q_d + Q_s} = \frac{Q_d}{Q_{cheq}}$$

which is now bias dependent. For example, the derivities of D_{xpart} can be easily obtained based on the quasi-static results:

(5.3.10)

$$\frac{dD_{xpart}}{dV_i} = \frac{1}{Q_{cheq}} \left(S_{xpart} \cdot C_{di} - D_{xpart} \cdot C_{si} \right)$$

where i represents the four terminals and C_{di} and C_{si} are the intrinsic capacitances calculated from the quasi-static analysis. The corresponding values for S_{xpart} can be derived from the fact that $D_{xpart} + S_{xpart} = 1$.

In the accumulation and depletion regions, Eq. (5.3.9) is simplified as

If $XPART < 0.5$, $D_{xpart} = 0.4$;
Else if $XPART > 0.5$, $D_{xpart} = 0.0$;
Else $D_{xpart} = 0.5$;

5.3.4 Derivation of nodal conductances

This section gives some examples of how to derive the nodal conductances related to NQS for transient analysis. By noting that $\tau = \boldsymbol{RC}$, G_{tau} can be derived as

(5.3.11)

$$G_{tau} = \frac{C_{fact}}{t}$$

τ is given by Eq. (5.3.2). Based on Eq. (5.3.8b), the self-conductance due to NQS at the transistor node D can be derived as

(5.3.12)

$$\frac{dD_{xpart}}{dV_d} \cdot \left(G_{tau} \cdot V_{def}\right) + D_{xpart} \cdot V_{def} \cdot \frac{dG_{tau}}{dV_d}$$

The trans-conductance due to NQS on the node D relative to the node of Q_{def} can be derived as

(5.3.13)

$$D_{xpart} \cdot G_{tau}$$

Other conductances can also be obtained in a similar way.

5.3.5 The AC Model

Similarly, the small-signal AC charge-deficit NQS model can be turned on by setting ***acnqsMod*** = 1 and off by setting ***acnqsMod*** = 0.

For small signals, by substituting (5.3.7) into (5.3.8b), it is easy to show that in the frequency domain, $Q_{ch}(t)$ can be transformed into

(5.3.14)

$$\Delta Q_{ch}(t) = \frac{\Delta Q_{cheq}(t)}{1 + jwt}$$

where w is the angular frequency. Based on (5.3.14), it can be shown that the transcapacitances C_{gi}, C_{si}, and C_{di} (i stands for any of the G, D, S and B terminals of the device) and the channel transconductances G_m, G_{ds}, and G_{mbs} all become complex quantities. For example, now G_m have the form of

(5.3.15)

$$G_m = \frac{G_{m0}}{1 + w^2 t^2} + j\left(-\frac{G_{m0} \cdot wt}{1 + w^2 t^2}\right)$$

and

(5.3.16)

$$C_{dg} = \frac{C_{dg0}}{1 + w^2 t^2} + j\left(-\frac{C_{dg0} \cdot wt}{1 + w^2 t^2}\right)$$

Those quantities with sub “0” in the above two equations are known from OP (operating point) analysis.

CHAPTER 6: Parameter Extraction

Parameter extraction is an important part of model development. Many different extraction methods have been developed [23, 24]. The appropriate methodology depends on the model and on the way the model is used. A combination of a local optimization and the group device extraction strategy is adopted for parameter extraction.

6.1 Optimization strategy

There are two main, different optimization strategies: global optimization and local optimization. Global optimization relies on the explicit use of a computer to find one set of model parameters which will best fit the available experimental (measured) data. This methodology may give the minimum average error between measured and simulated (calculated) data points, but it also treats each parameter as a "fitting" parameter. Physical parameters extracted in such a manner might yield values that are not consistent with their physical intent.

In local optimization, many parameters are extracted independently of one another. Parameters are extracted from device bias conditions which correspond to dominant physical mechanisms. Parameters which are extracted in this manner might not fit experimental data in all the bias conditions. Nonetheless, these extraction methodologies are developed specifically with respect to a given parameter’s physical meaning. If properly executed, it should, overall, predict

device performance quite well. Values extracted in this manner will now have some physical relevance.

6.2 Extraction Strategies

Two different strategies are available for extracting parameters: the single device extraction strategy and group device extraction strategy. In single device extraction strategy, experimental data from a single device is used to extract a complete set of model parameters. This strategy will fit one device very well but will not fit other devices with different geometries. Furthermore, single device extraction strategy can not guarantee that the extracted parameters are physical. If only one set of channel length and width is used, parameters related to channel length and channel width dependencies can not be determined.

BSIM3v3 uses group device extraction strategy. This requires measured data from devices with different geometries. All devices are measured under the same bias conditions. The resulting fit might not be absolutely perfect for any single device but will be better for the group of devices under consideration.

6.3 Extraction Procedure

6.3.1 Parameter Extraction Requirements

One large size device and two sets of smaller-sized devices are needed to extract parameters, as shown in Figure 6-1.

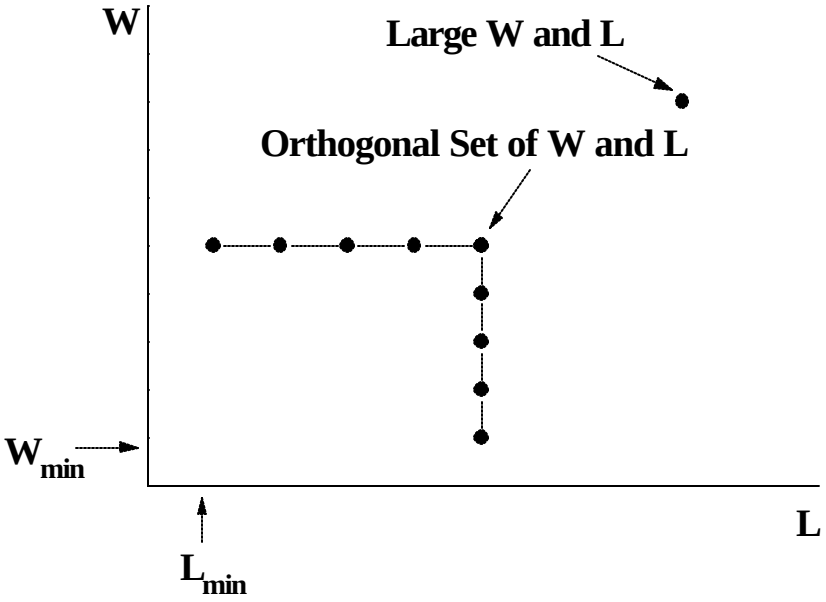

Figure 6-1. Device geometries used for parameter extraction

The large-sized device (W ≥ 10μm, L ≥ 10μm) is used to extract parameters which are independent of short/narrow channel effects and parasitic resistance. Specifically, these are: mobility, the large-sized device threshold voltage V_{Tideal}, and the body effect coefficients K_1 and K_2 which depend on the vertical doping concentration distribution. The set of devices with a fixed large channel width but different channel lengths are used to extract parameters which are related to the short channel effects. Similarly, the set of devices with a fixed, long channel length but different channel widths are used to extract parameters which are related to narrow width

effects. Regardless of device geometry, each device will have to be measured under four, distinct bias conditions.

(1) I_{ds} vs. V_{gs} @ $V_{ds} = 0.05V$ with different V_{bs}.

(2) I_{ds} vs. V_{ds} @ $V_{bs} = 0V$ with different V_{gs}.

(3) I_{ds} vs. V_{gs} @ $V_{ds} = V_{dd}$ with different V_{bs}. (V_{dd} is the maximum drain voltage).

(4) I_{ds} vs. V_{ds} @ $V_{bs} = V_{bb}$ with different V_{gs}. ($|V_{bb}|$ is the maximum body bias).

6.3.2 Optimization

The optimization process recommended is a combination of Newton-Raphson's iteration and linear-squares fit of either one, two, or three variables. This methodology was discussed by M. C. Jeng [18]. A flow chart of this optimization process is shown in Figure 6-2. The model equation is first arranged in a form suitable for Newton-Raphson's iteration as shown in Eq. (6.3.1):

(6.3.1)

$$f_{\exp}(P_{10},P_{20},P_{30}) - f_{sim}(P_1^{(m)},P_2^{(m)},P_3^{(m)}) = \frac{\partial f_{sim}}{\partial P_1}\Delta P_1^m + \frac{\partial f_{sim}}{\partial P_2}\Delta P_2^m + \frac{\partial f_{sim}}{\partial P_3}\Delta P_3^m$$

The variable $f_{sim}()$ is the objective function to be optimized. The variable $f_{exp}()$ stands for the experimental data. P_{10}, P_{20}, and P_{30} represent the desired extracted parameter values. $P_1^{(m)}$, $P_2^{(m)}$ and $P_3^{(m)}$ represent parameter values after the mth iteration.

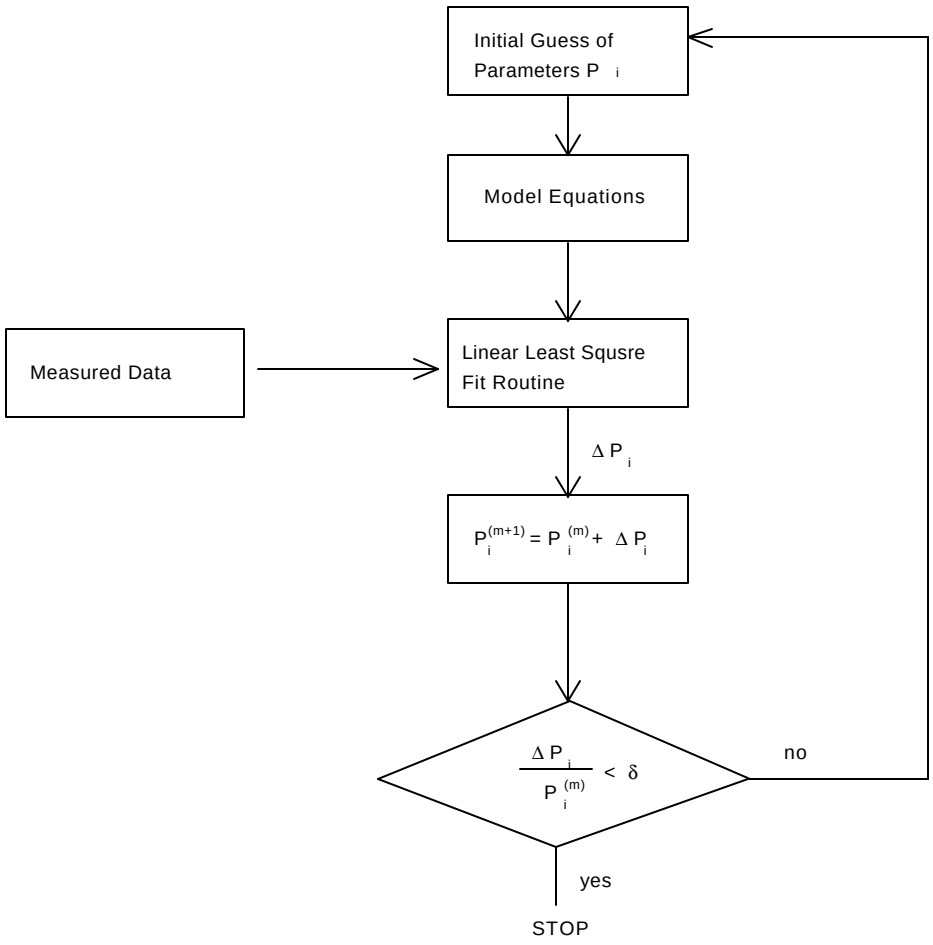

Figure 6-2. Optimization flow.

To change Eq. (6.3.1) into a form that a linear least-squares fit routine can be used (i.e. in a form of $y = a + bx_1 + cx_2$), both sides of the Eq. (6.3.1) are divided by $\partial f_{sim} / \partial P_1$. This gives the change in P_1, $\Delta P_1^{(m)}$, for the next iteration such that:

$$P_i^{(m+1)} = P_i^{(m)} + DP_i^{(m)} \tag{6.3.2}$$

where i=1, 2, 3 for this example. The (m+1) parameter values for P_2 and P_3 are obtained in an identical fashion. This process is repeated until the incremental parameter change in parameter values $\Delta P_i^{(m)}$ are smaller than a pre-determined value. At this point, the parameters P_1, P_2, and P_3 have been extracted.

6.3.3 Extraction Routine

Before any model parameters can be extracted, some process parameters have to be provided. They are listed below in Table 6-1:

Input Parameters Names	Physical Meaning
T_{ox}	Gate oxide thickness
N_{ch}	Doping concentration in the channel
T	Temperature at which the data is taken
L_{drawn}	Mask level channel length
W_{drawn}	Mask level channel width
X_j	Junction depth

Table 6-1. Prerequisite input parameters prior to extraction process.

The parameters are extracted in the following procedure. These procedures are based on a physical understanding of the model and based on local

optimization. (Note: *Fitting Target Data* refers to measurement data used for model extraction.)

Step 1

Extracted Parameters & Fitting Target Data	Device & Experimental Data
V_{th0}, K_1, K_2 Fitting Target Exp. Data: $V_{th}(V_{bs})$	Large Size Device (Large W & L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs} Extracted Experimental Data $V_{th}(V_{bs})$

Step 2

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
μ_0, U_a, U_b, U_c Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	Large Size Device (Large W & L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 3

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
Lint, $R_{ds}(R_{dsw}, W, V_{bs})$ Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 4

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
$Wint$, $R_{ds}(R_{dsw}, W, V_{bs})$ Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed L & Different W). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 5

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
R_{dsw},$Prwb$, Wr Fitting Target Exp. Data: $R_{ds}(R_{dsw}, W, V_{bs})$	$R_{ds}(R_{dsw}, W, V_{bs})$

Step 6

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
D_{vt0}, D_{vt1}, D_{vt2}, Nlx Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed W & Different L). $V_{th}(V_{bs}, L, W)$

Step 7

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
D_{vt0w}, D_{vt1w}, D_{vt2w} Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed L & Different W). $V_{th}(V_{bs}, L, W)$

Step 8

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
K_3, K_{3b}, W_0 Fitting Target Exp. Data: $V_{th}(V_{bs}, L, W)$	One Set of Devices (Large and Fixed L & Different W). $V_{th}(V_{bs}, L, W)$

Step 9

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
V_{off}, $Nfactor$, C_{dsc}, C_{dscb} Fitting Target Exp. Data: Subthreshold region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 10

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

C_{dscd} Fitting Target Exp. Data: Subthreshold region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ $V_{bs} = V_{bb}$ at Different V_{ds}

Step 11

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
dWb Fitting Target Exp. Data: Strong Inversion region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ V_{ds} = 0.05V at Different V_{bs}

Step 12

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
v_{sat}, A_0, A_{gs} Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$ A_1, A_2 (PMOS Only) Fitting Target Exp. Data $V_{asat}(V_{gs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 13

Extracted Parameters & Fitting Target Data	Devices & Experimental Data

$B0$, $B1$ Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed L & Different W). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 14

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
dWg Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed L & Different W). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 15

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
P_{scbe1}, P_{scbe2} Fitting Target Exp. Data: $R_{out}(V_{gs}, V_{ds})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 16

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
P_{clm}, $\theta(D_{rout}, P_{diblc1}, P_{diblc2}, L)$, $Pavg$ Fitting Target Exp. Data: $R_{out}(V_{gs}, V_{ds})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{ds} @ V_{bs} = 0V at Different V_{gs}

Step 17

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
D_{rout}, P_{dibl1c}, P_{diblc2} Fitting Target Exp. Data: $\theta(D_{rout}, P_{diblc1}, P_{diblc2}, L)$	One Set of Devices (Large and Fixed W & Different L). $\theta(D_{rout}, P_{diblc1}, P_{diblc2}, L)$

Step 18

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
$P_{dibl1cb}$ Fitting Target Exp. Data: $\theta(D_{rout}, P_{diblc1}, P_{diblc2}, L, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ fixed V_{gs} at Different V_{bs}

Step 19

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
$\theta_{dibl}(Eta0, Etab, Dsub, L)$ Fitting Target Exp. Data: Subthreshold region $I_{ds}(V_{gs}, V_{bs})$	One Set of Devices (Large and Fixed W & Different L). I_{ds} vs. V_{gs} @ $V_{ds} = V_{dd}$ at Different V_{bs}

Step 20

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
*Eta*0, *Etab*, *Dsub* Fitting Target Exp. Data: θ_{dibl}(*Eta*0, *Etab*, *L*)	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{gs} @ $V_{ds} = V_{dd}$ at Different V_{bs}

Step 21

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
Keta Fitting Target Exp. Data: $I_{sat}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{ds} @ $V_{bs} = V_{bb}$ at Different V_{gs}

Step 22

Extracted Parameters & Fitting Target Data	Devices & Experimental Data
α_0, α_1, β_0 Fitting Target Exp. Data: $I_{sub}(V_{gs}, V_{bs})/W$	One Set of Devices (Large and Fixed *W* & Different *L*). I_{ds} vs. V_{ds} @ $V_{bs} = V_{bb}$ at Different V_{ds}

6.4 Notes on Parameter Extraction

6.4.1 Parameters with Special Notes

Below is a list of model parameters which have special notes for parameter extraction.

Symbols used in SPICE	Description	Default Value	Unit	Notes
Vth0	Threshold voltage for large W and L device @ Vbs=0V	0.7 (NMOS) -0.7 (PMOS)	V	nI-1
K1	First order body effect coefficient	0.5	$V^{1/2}$	nI-2
K2	Second order body effect coefficient	0	none	nI-2
Vbm	Maximum applied body bias	-3	V	nI-2
Nch	Channel doping concentration	1.7E17	$1/cm^3$	nI-3
gamma1	Body-effect coefficient near interface	calculated	$V^{1/2}$	nI-4
gamma2	Body-effect coefficient in the bulk	calculated	$V^{1/2}$	nI-5
Vbx	Vbs at which the depletion width equals xt	calculated	V	nI-6
Cgso	Non-LDD source-gate overlap capacitance per channel length	calculated	F/m	nC-1
Cgdo	Non-Ldd drain-gate overlap capacitance per channel length	calculated	F/m	nC-2
CF	Fringing field capacitance	calculated	F/m	nC-3

Table 6-2. Parameters with notes for extraction.

6.4.2 Explanation of Notes

nI-1. If V_{th0} is not specified, it is calculated by

$$V_{th0} = V_{FB} + \Phi_s + K_1\sqrt{\Phi_s}$$

where the model parameter V_{FB}=-1.0. If V_{th0} is specified, V_{FB} defaults to

$$V_{FB} = V_{th0} - \Phi_s - K_1\sqrt{\Phi_s}$$

nI-2. If K_1 and K_2 are not given, they are calculated based on

$$K_1 = g_2 - 2K_2\sqrt{\Phi_s - V_{bm}}$$

$$K_2 = \frac{(g_1 - g_2)\left(\sqrt{\Phi_s - V_{bx}} - \sqrt{\Phi_s}\right)}{2\sqrt{\Phi_s}\left(\sqrt{\Phi_s - V_{bm}} - \sqrt{\Phi_s}\right) + V_{bm}}$$

where Φ_s is calculated by

$$\Phi_s = 2V_{tm0}\ln\left(\frac{N_{ch}}{n_i}\right)$$

$$V_{tm0} = \frac{k_B T_{nom}}{q}$$

$$n_i = 1.45\times10^{10}\left(\frac{T_{nom}}{300.15}\right)^{1.5}\exp\left(21.5565981-\frac{E_{g0}}{2V_{tm0}}\right)$$

$$E_{g0} = 1.16-\frac{7.02\times10^{-4}T_{nom}^{\ 2}}{T_{nom}+1108}$$

where E_{g0} is the energy bandgap at temperature T_{nom}.

nI-3. If N_{ch} is not given and γ_1 is given, N_{ch} is calculated from

$$N_{ch} = \frac{g_1^{\ 2}C_{ox}^{\ 2}}{2qe_{si}}$$

If both γ_1 and N_{ch} are not given, N_{ch} defaults to 1.7e23 m^{-3} and γ_1 is calculated from N_{ch}.

nI-4. If γ_1 is not given, it is calculated by

$$g_1 = \frac{\sqrt{2qe_{si}N_{ch}}}{C_{ox}}$$

nI-5. If γ_2 is not given, it is calculated by

$$g_2 = \frac{\sqrt{2qe_{si}N_{sub}}}{C_{ox}}$$

nI-6. If V_{bx} is not given, it is calculated by

$$\frac{qN_{ch}X_t^{\ 2}}{2e_{si}} = \Phi_s - V_{bx}$$

nC-1. If *Cgso* is not given, it is calculated by

if (*dlc* is given and is greater 0),
    Cgso = *dlc* * *Cox* - *Cgs*1
    if (*Cgso* < 0)
    Cgso = 0
else *Cgso* = 0.6 *Xj* * *Cox*

nC-2. If *Cgdo* is not given, it is calculated by

if (*dlc* is given and is greater than 0),
    Cgdo = *dlc* * *Cox* - *Cgd*1
    if (*Cgdo* < 0)
    Cgdo = 0
else *Cgdo* = 0.6 *Xj* * *Cox*

nC-3. If *CF* is not given then it is calculated usin by

$$CF = \frac{2\varepsilon_{ox}}{\pi}\ln\left(1+\frac{4\times10^{-7}}{Tox}\right)$$

CHAPTER 7: Benchmark Test Results

A series of benchmark tests [26] have been performed to check the model robustness, accuracy and performance. Although not all the benchmark test results are included in this chapter, the most important ones are demonstrated.

7.1 Benchmark Test Types

Table 7-1 lists the various benchmark test conditions and associated figure number included in this section. Notice that for each plot, smooth transitions are apparent for current, transconductance, and source to drain resistance for all transition regions regardless of bias conditions.

Device Size	Bias Conditions	Notes	Figure Number
W/L=20/5	Ids vs. Vgs @ Vbs=0V; Vds=0.05, 3.3V	Log scale	7-1
W/L=20/5	Ids vs. Vgs @ Vbs=0V; Vds=0.05, 3.3V	Linear scale	7-2
W/L=20/0.5	Ids vs. Vgs @ Vbs=0V; Vds=0.05, 3.3V	Log scale	7-3
W/L=20/0.5	Ids vs. Vgs @ Vbs=0V; Vds=0.05, 3.3V	Linear scale	7-4
W/L=20/5	Ids vs. Vgs @ Vds=0.05V; Vbs=0 to -3.3V	Log scale	7-5
W/L=20/5	Ids vs. Vgs @ Vds=0.05V; Vbs=0 to -3.3V; W/L=20/5	Linear scale	7-6
W/L=20/0.5	Ids vs. Vgs @ Vds=0.05V; Vbs=0 to -3.3V	Log scale	7-7
W/L=20/0.5	Ids vs. Vgs @ Vds=0.05V; Vbs=0 to -3.3V	Linear scale	7-8
W/L=20/5	Gm/Ids vs. Vgs @ Vds=0.05V, 3-3V; Vbs=0V	Linear scale	7-9

Device Size	Bias Conditions	Notes	Figure Number
W/L=20/0.5	Gm/Ids vs. Vgs @ Vds=0.05V, 3-3V; Vbs=0V	Linear scale	7-10
W/L=20/5	Gm/Ids vs. Vgs @ Vds=0.05V; Vbs=0V to -3.3V	Linear scale	7-11
W/L=20/0.5	Gm/Ids vs. Vgs @ Vds=0.05V; Vbs=0V to -3.3V	Linear scale	7-12
W/L=20/0.5	Ids vs. Vds @Vbs=0V; Vgs=0.5V, 0.55V, 0.6V	Linear scale	7-13
W/L=20/5	Ids vs. Vds @Vbs=0V; Vgs=1.15V to 3.3V	Linear scale	7-14
W/L=20/0.5	Ids vs. Vds @Vbs=0V; Vgs=1.084V to 3.3V	Linear scale	7-15
W/L=20/0.5	Rout vs. Vds @ Vbs=0V; Vgs=1.084V to 3.3V	Linear scale	7-16

Table 7-1. Benchmark test information.

7.2 Benchmark Test Results

All of the figures listed in Table 7-1 are shown below. Unless otherwise indicated, symbols represent measurement data and lines represent the results of the model. All of these plots serve to demonstrate the robustness and continuous behavior of the unified model expression for not only I_{ds} but G_m, G_m/I_{ds}, and R_{out} as well.

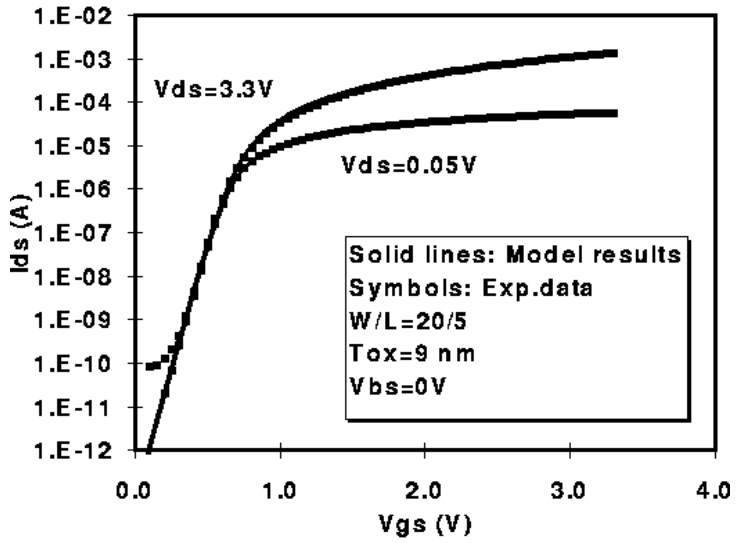

Figure 7-1. Continuity from subthreshold to strong inversion (log scale).

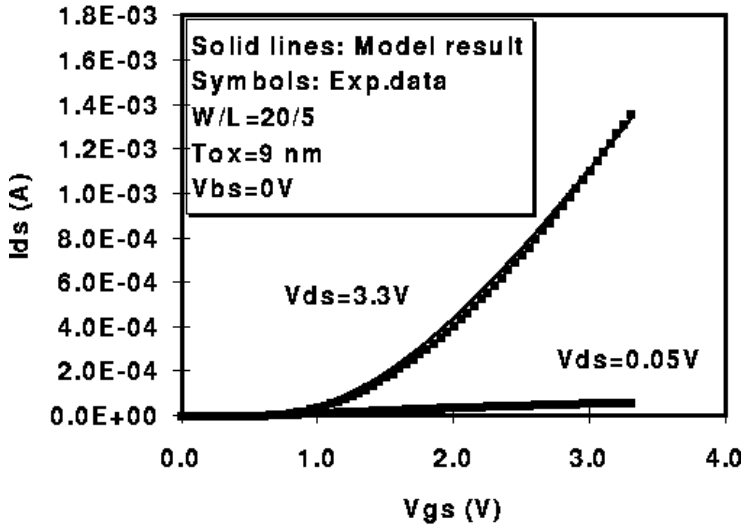

Figure 7-2. Continuity from subthreshold to strong inversion (linear scale).

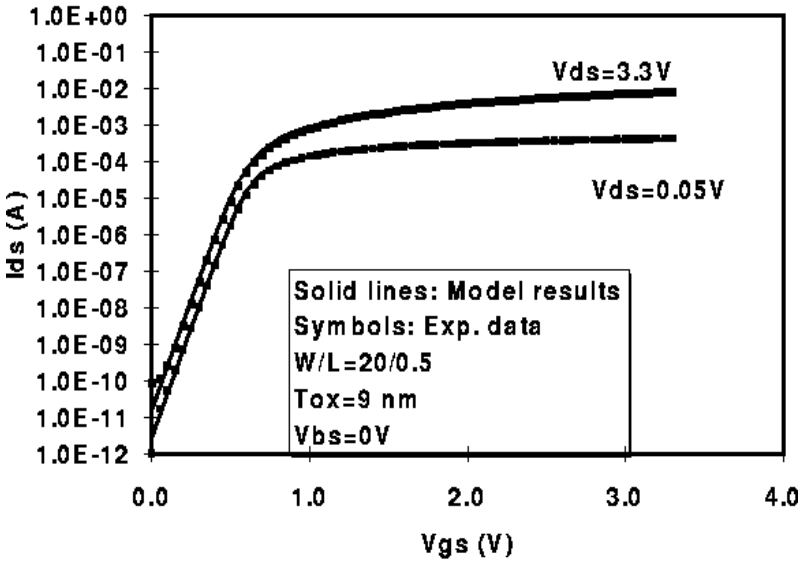

Figure 7-3. Same as Figure 7-1 but for a short channel device.

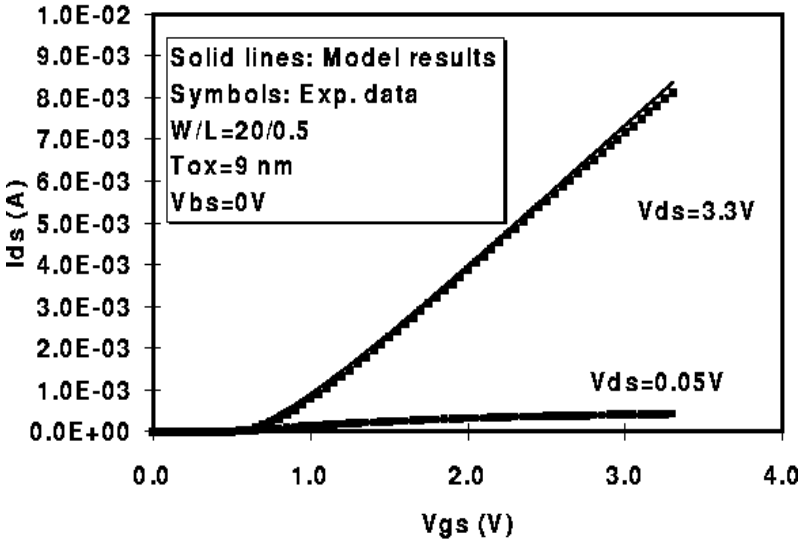

Figure 7-4. Same as Figure 7-2 but for a short channel device.

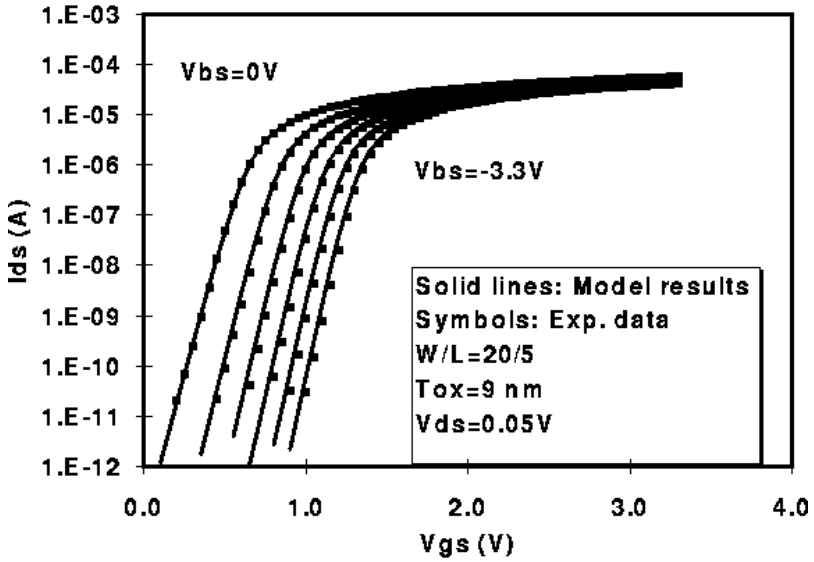

Figure 7-5. Subthreshold to strong inversion continuity as a function of V_{bs}.

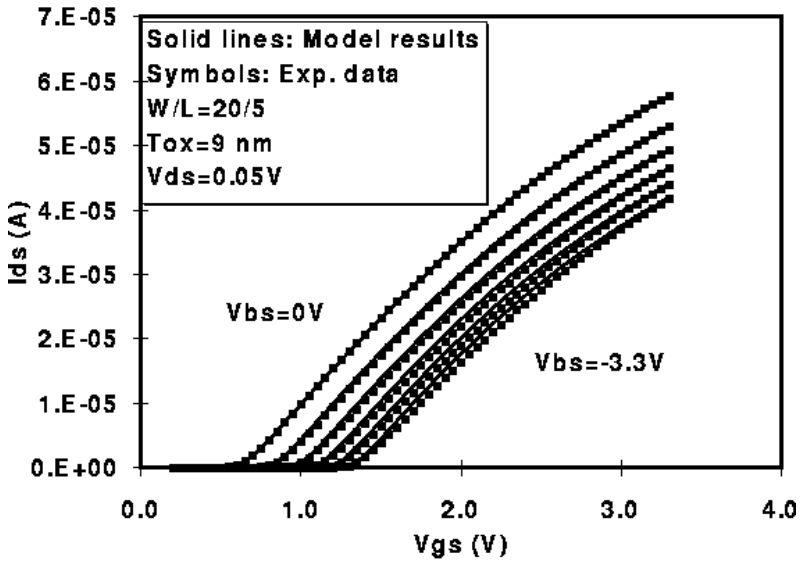

Figure 7-6. Subthreshold to strong inversion continuity as a function of V_{bs}.

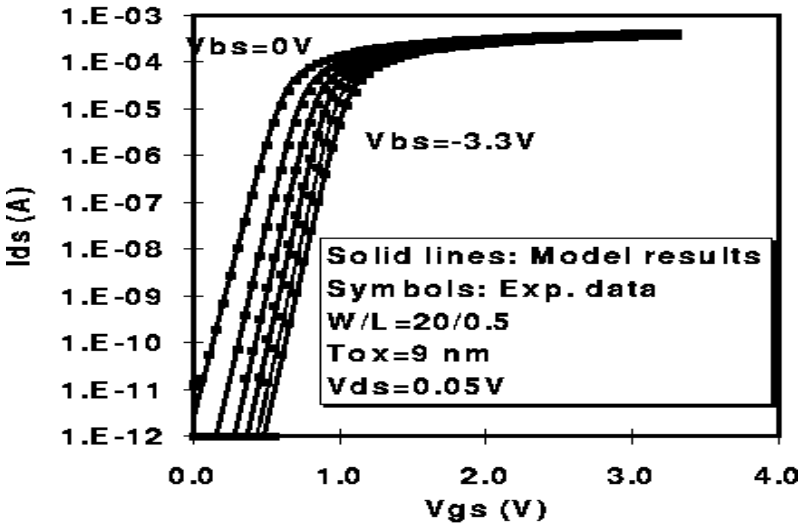

Figure 7-7. Same as Figure 7-5 but for a short channel device.

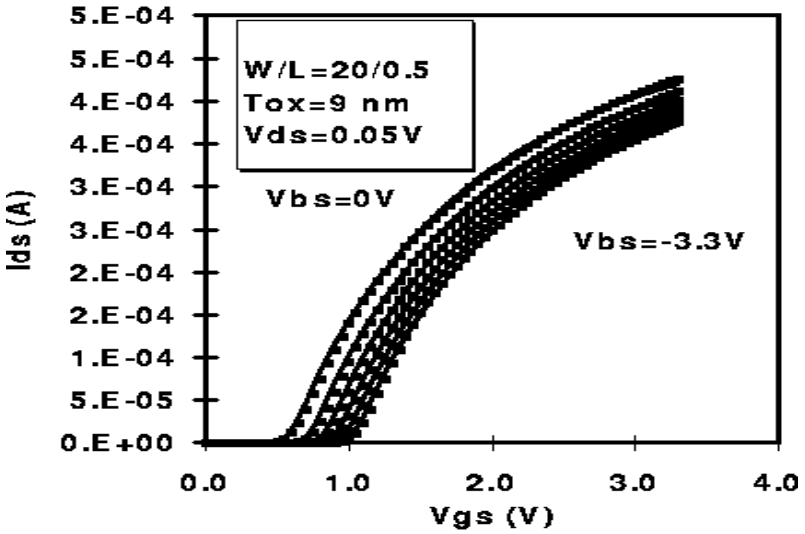

Figure 7-8. Same as Figure 7-6 but for a short channel device.

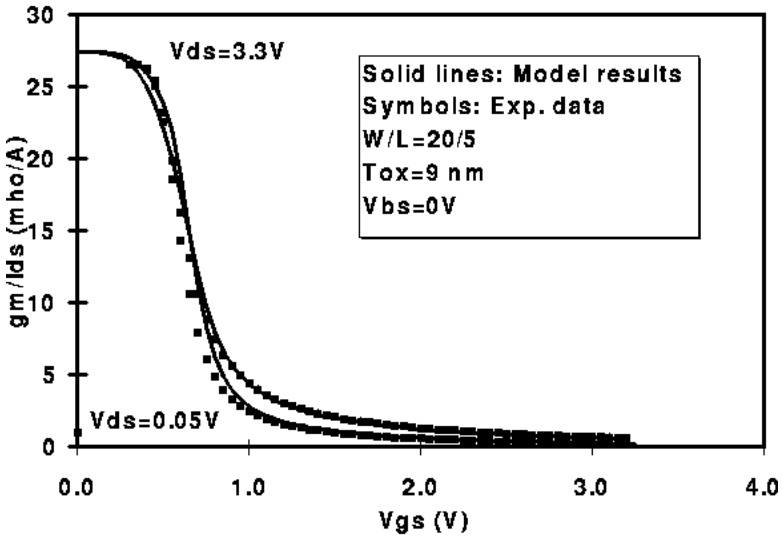

Figure 7-9. G_m/I_{ds} continuity from subthreshold to strong inversion regions.

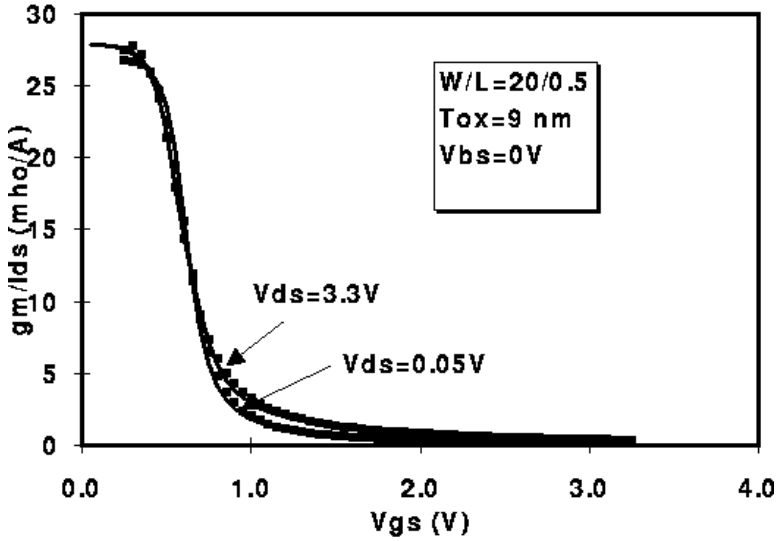

Figure 7-10. Same as Figure 7-9 but for a short channel device.

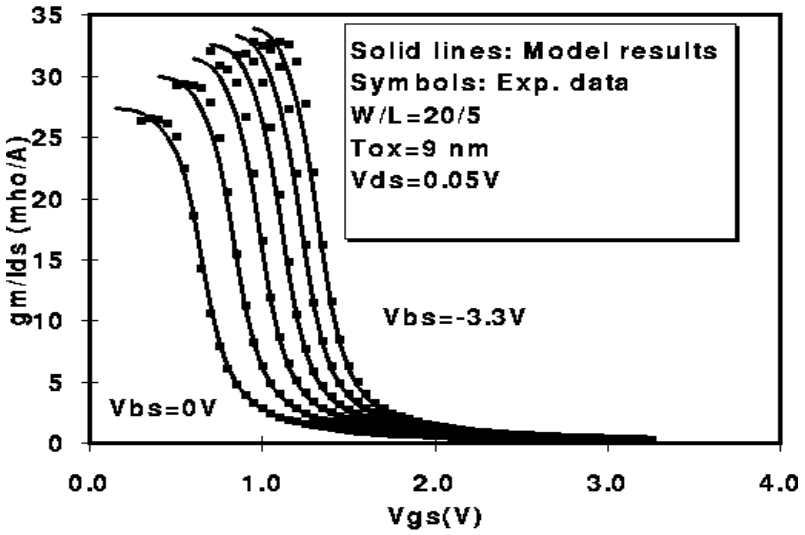

Figure 7-11. G_m/I_{ds} continuity as a function of V_{bs}.

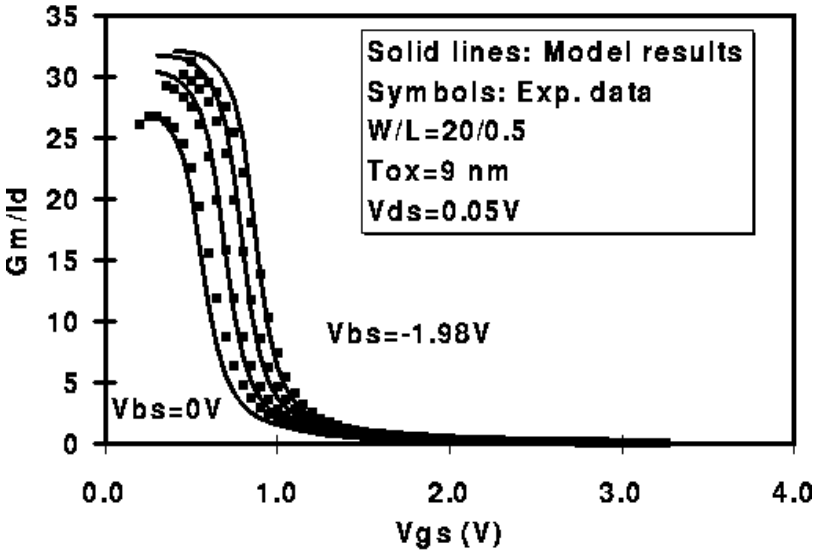

Figure 7-12. Same as Figure 7-11 but for a short channel device.

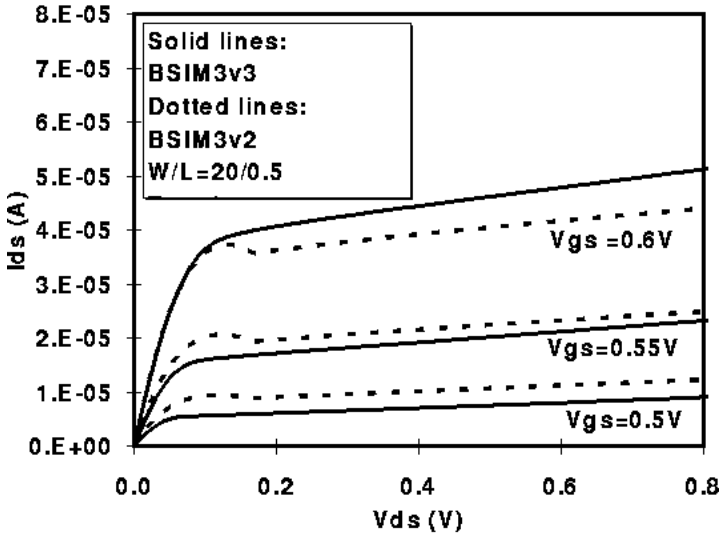

Figure 7-13. Comparison of G_{ds} with BSIM3v2.

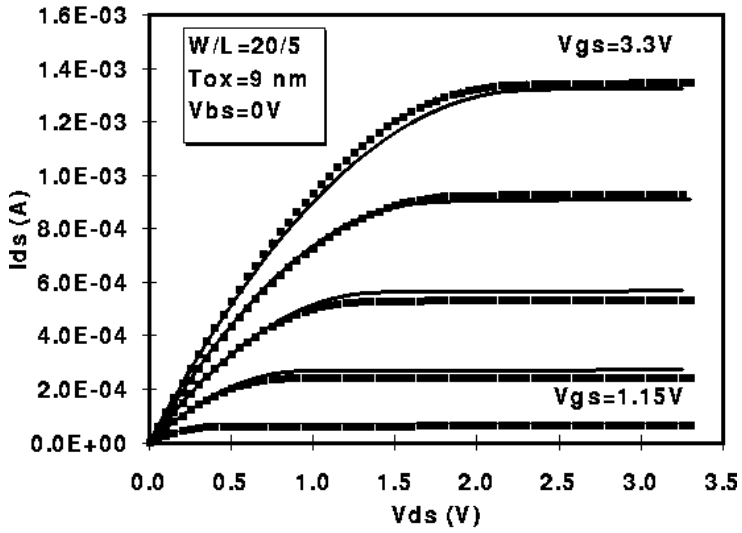

Figure 7-14. Smooth transitions from linear to saturation regimes.

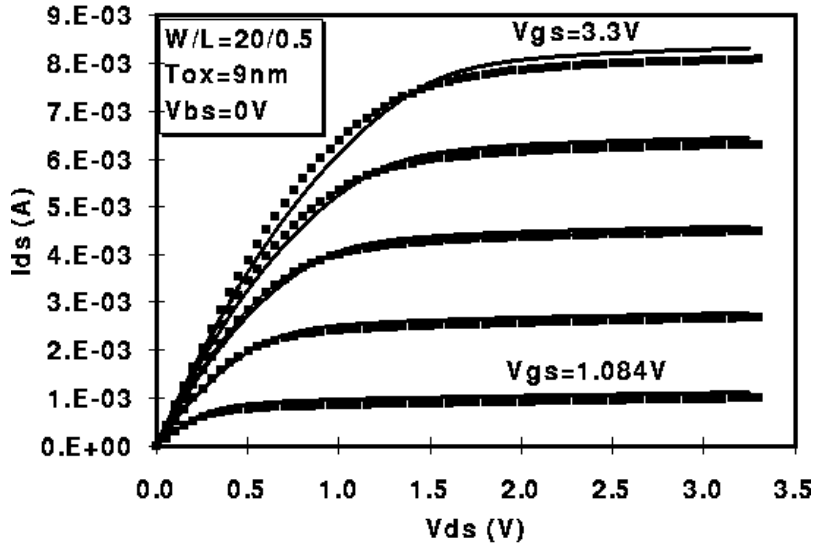

Figure 7-15. Same as Figure 7-14 but for a short channel device.

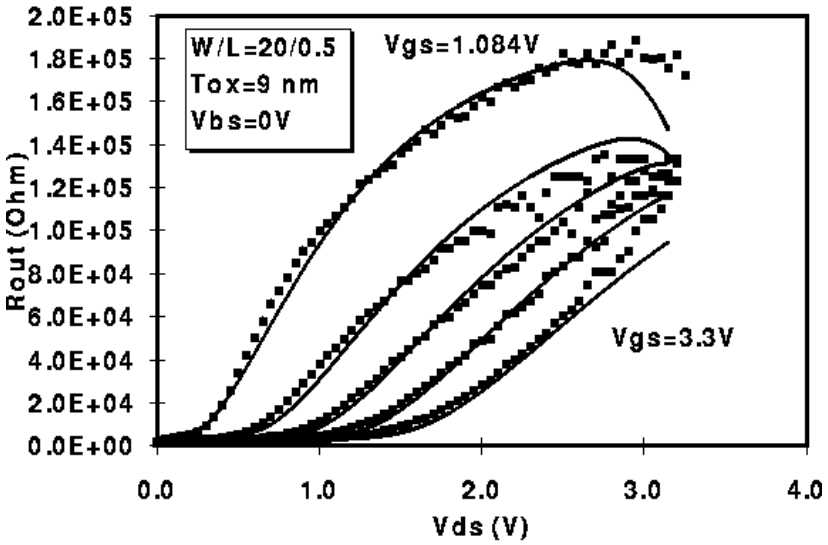

Figure 7-16. Continuous and non-negative R_{out} behavior.

CHAPTER 8: Noise Modeling

8.1 Flicker Noise

8.1.1 Parameters

There exist two models for flicker noise modeling. One is called SPICE2 flicker noise model; the other is BSIM3 flicker noise model [35-36]. The flicker noise model parameters are listed in Table 8-1.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Noia	noia	Noise parameter A	(NMOS) 1e20 (PMOS) 9.9e18	none
Noib	noib	Noise parameter B	(NMOS) 5e4 (PMOS) 2.4e3	none
Noic	noic	Noise parameter C	(NMOS) -1.4e-12 (PMOS) 1.4e-12	none
Em	em	Saturation field	4.1e7	V/m
Af	af	Flick noise exponent	1	none
Ef	ef	Flicker noise frequency exponent	1	none
Kf	kf	Flicker noise coefficient	0	none
LINTNOI	lintnoi	Length Reduction Parameter Off-set	0.0	m

Table 8-1. Flicker noise model parameters.

8.1.2 Formulations

1. For SPICE2 model

(8.1)

$$Noisedensity = \frac{K_f I_{ds}^{af}}{C_{ox} L_{eff}^{2} f^{ef}}$$

where f is the frequency.

2. For BSIM3 model

If $V_{gs} > V_{th} + 0.1$

(8.2)

$$S_{id,inv}(f) = \frac{k_B T q^2 m_{eff} I_{ds}}{C_{oxe}(L_{eff} - 2 \times LINTNOI)^2 A_{bulk} f^{ef} \times 10^8} \left(NOIA \log\left(\frac{N_0 + 2 \times 10^{14}}{N_l + 2 \times 10^{14}} \right) + NOIB (N_0 - N_l) + \frac{NOIC}{2} (N_0^2 - N_l^2) \right)$$
$$+ \frac{k_B T I_{ds}^2 D L_{clm}}{W_{eff} \times (L_{eff} - 2 \times LINTNOI)^2 f^{ef} \times 10^8} \times \frac{NOIA + NOIB\, N_l + NOIC \times N_l^2}{(N_l + N^*)^2}$$

where V_{tm} is the thermal voltage, m_{eff} is the effective mobiity at the given bias condition, and L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source side given by

(8.3)

$$N_0 = \frac{C_{ox}(V_{gs} - V_{th})}{q}$$

The parameter N_l is the charge density at the drain end given by

(8.4)

$$N_l = \frac{C_{ox}\left(V_{gs} - V_{th} - \min\left(V_{ds}, V_{dsat}\right)\right)}{q}$$

DL_{clm} is the channel length reduction due to channel length modulation and given by

(8.5)

$$\Delta L_{\text{clm}} = \begin{cases} Litl \cdot \log\left(\dfrac{\dfrac{V_{ds} - V_{dsat}}{Litl} + E_m}{E_{sat}}\right) & \left(\text{for } V_{ds} > V_{dsat}\right) \\ 0 \quad \left(\text{otherwise}\right) \end{cases}$$

$$E_{sat} = \frac{2 \times v_{sat}}{m_{eff}}$$

where

$$Litl = \sqrt{3X_j T_{ox}}$$

Otherwise

(8.6)

$$Noisedensity = \frac{S_{\text{limit}} \times S_{\text{wi}}}{S_{\text{limit}} + S_{\text{wi}}}$$

Where, S_{limit} is the flicker noise calculated at $V_{gs} = V_{th} + 0.1$ and S_{wi} is given by

(8.7)

$$S_{\mathrm{wi}} = \frac{Noia \cdot V_{tm} \cdot I_{ds}^{\ 2}}{W_{eff} L_{eff} \cdot f^{ef} \cdot 4 \times 10^{36}}$$

8.2 Channel Thermal Noise

There also exist two models for channel thermal noise modeling. One is called SPICE2 thermal noise model. The other is BSIM3v3 thermal noise model. Each of these can be toggled through the model flag, **noiMod**.

1. For SPICE2 thermal noise model

(8.8)

$$\frac{8 k_B T}{3}\left(G_m + G_{mbs} + G_{ds}\right)$$

where G_m, G_{mbs} and G_{ds} are the transconductances.

2. For BSIM3v3 thermal noise model [37]

(8.9)

$$\frac{4 k_B T \Delta f \mu_{eff}}{\mu_{eff} \left|Q_{inv}\right| R_{ds}(V) + L_{eff}^{\ 2}} \left|Q_{inv}\right|$$

Q_{inv} is the inversion channel charge computed from the capacitance models (**capMod** = 0, 1, 2 or 3).

3. New SPICE2 thermal noise model

(8.10)

$$\frac{8}{3} kT\left(g_m + g_{ds} + g_{mbs}\right)\left[\frac{3}{2} - \frac{\min(Vds, Vdsat)}{2Vdsat}\right]$$

8.3 Noise Model Flag

A model flag, **noiMod**, is used to select different combination of flicker and thermal noise models discussed above with possible optoins described in Table 8-2.

noimod flag	Flicker noise model	Thermal noise model
1	SPICE2	SPICE2
2	BSIM3v3	BSIM3v3
3	BSIM3v3	SPICE2
4	SPICE2	BSIM3v3
5	SPICE2	SPICE2new
6	BSIM3v3	SPICE2new

Table 8-2. noiMod flag for differnet noise models.

CHAPTER 9: MOS Diode Modeling

9.1 Diode IV Model

The diode IV modeling now supports a resistance-free diode model and a current-limiting feature by introducing a new model parameter *ijth* (defaulting to 0.1A). If *ijth* is explicitly specified to be zero, a resistance-free diode model will be triggered; otherwise two critical junction votages *Vjsm* for S/B diode and *Vjdm* for D/B diode will be computed from the value of *ijth.*

9.1.1 Modeling the S/B Diode

If the S/B saturation current I_{sbs} is larger than zero, the following equations is used to calculate the S/B diode current I_{bs}.

Case 1 - *ijth* is equal to zero: A resistance-free diode.

$$I_{bs} = I_{sbs}\left(\exp\left(\frac{V_{bs}}{NV_{tm}}\right)-1\right)+G_{\min}V_{bs} \tag{9.1}$$

where $NV_{tm} = NJ \cdot (KbT)/q$; *NJ* is a model parameter, known as the junction emission coefficient.

Case 2 - *ijth* is non-zero: Current limiting feature.

If $V_{bs} < Vjsm$

$$I_{bs} = I_{sbs}\left(\exp\left(\frac{V_{bs}}{NV_{tm}}\right)-1\right)+G_{\min}V_{bs} \tag{9.2}$$

otherwise

$$I_{bs} = ijth+\frac{ijth+I_{sbs}}{NV_{tm}}\left(V_{bs}-Vjsm\right)+G_{\min}V_{bs} \tag{9.3}$$

with *Vjsm* computed by

$$Vjsm = NV_{tm}\ln\left(\frac{ijth}{I_{sbs}}+1\right)$$

The saturation current I_{sbs} is given by

$$I_{sbs} = A_s J_s + P_s J_{ssw} \tag{9.4}$$

where J_s is the junction saturation current density, A_S is the source junction area, J_{ssw} is the sidewall junction saturation current density, P_s is the perimeter of the source junction. J_s and J_{ssw} are functions of temperature and can be written as

$$J_s = J_{s0}\exp\left(\frac{\frac{E_{g0}}{V_{tm0}}-\frac{E_g}{V_{tm}}+XTI\ln\left(\frac{T}{T_{nom}}\right)}{NJ}\right) \tag{9.5}$$

(9.6)

$$J_{ssw} = J_{s0sw} \exp\left(\frac{\frac{E_{g0}}{V_{tm0}} - \frac{E_g}{V_{tm}} + XTI \ln\left(\frac{T}{T_{nom}}\right)}{NJ} \right)$$

The energy band-gap E_{g0} and E_g at the nominal and operating temperatures are expressed by (9.7a) and (9.7b), repectively:

(9.7a)

$$E_{g0} = 1.16 - \frac{7.02 \times 10^{-4} T_{nom}^{\ 2}}{T_{nom} + 1108}$$

(9.7b)

$$E_g = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

In the above derivatoins, J_{s0} is the saturation current density at T_{nom}. If J_{s0} is not given, $J_{s0} = 1 \times 10^{-4}$ A/m^2. J_{s0sw} is the sidewall saturation current density at T_{nom}, with a default value of zero.

If I_{sbs} is not positive, I_{bs} is calculated by

(9.8)

$$I_{bs} = G_{\min} \cdot V_{bs}$$

9.1.2 Modeling the D/B Diode

If the D/B saturation current I_{sbd} is larger than zero, the following equations is used to calculate the D/B diode current I_{bd}.

Case 1 - *ijth* is equal to zero: A resistance-free diode.

(9.9)

$$I_{bd} = I_{sbd}\left(\exp\left(\frac{V_{bd}}{NV_{tm}}\right)-1\right)+G_{\min}V_{bd}$$

Case 2 - *ijth* is non-zero: Current limiting feature.

If $V_{bd} < Vjdm$

(9.10)

$$I_{bd} = I_{sbd}\left(\exp\left(\frac{V_{bd}}{NV_{tm}}\right)-1\right)+G_{\min}V_{bd}$$

otherwise

(9.11)

$$I_{bd} = ijth+\frac{ijth+I_{sbd}}{NV_{tm}}\left(V_{bd}-Vjdm\right)+G_{\min}V_{bd}$$

with *Vjdm* computed by

$$Vjdm = NV_{tm}\ln\left(\frac{ijth}{I_{sbd}}+1\right)$$

The saturation current I_{sbd} is given by

(9.12)

$$I_{sbd} = A_d J_s + P_d J_{ssw}$$

where A_d is the drain junction area and P_d is the perimeter of the drain junction. If I_{sbd} is not positive, I_{bd} is calculated by

(9.13)

$$I_{bd} = G_{\min}\cdot V_{bd}$$

9.1.3 Model Parameter Lists

The diode DC model parameters are listed in Table 9-1.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Js0	js	Saturation current density	1e-4	A/m^2
Js0sw	jssw	Side wall saturation current density	0	A/m
NJ	nj	Emission coefficient	1	none
XTI	xti	Junction current temperature exponent coefficient	3.0	none
ijth	ijth	Limiting current	0.1	A

Table 9-1. MOS diode model parameters.

9.2 MOS Diode Capacitance Model

Source and drain junction capacitance can be divided into two components: the junction bottom area capacitance C_{jb} and the junction periphery capacitance C_{jp}. The formula for both the capacitances is similar, but with different model parameters. The equation of C_{jb} includes the parameters such as C_j, M_j, and P_b. The equation of C_{jp} includes the parameters such as C_{jsw}, M_{jsw}, P_{bsw}, C_{jswg}, M_{jswg}, and P_{bswg}.

9.2.1 S/B Junction Capacitance

The S/B junction capacitance can be calculated by

If $P_s > W_{eff}$

$$Capbs = A_s C_{jbs} + \left(P_s - W_{eff}\right) C_{jbssw} + W_{eff} C_{jbsswg} \tag{9.14}$$

Otherwise

$$Capbs = A_s C_{jbs} + P_s C_{jbsswg} \tag{9.15}$$

where C_{jbs} is the unit bottom area capacitance of the S/B junction, C_{jbssw} is the periphery capacitance of the S/B junction along the field oxide side, and C_{jbsswg} is the periphery capacitance of the S/B junction along the gate oxide side.

If C_j is larger than zero, C_{jbs} is calculated by

if $V_{bs} < 0$

$$C_{jbs} = C_j \left(1 - \frac{V_{bs}}{P_b}\right)^{-M_j} \tag{9.16}$$

otherwise

$$C_{jbs} = C_j \left(1 + M_j \frac{V_{bs}}{P_b}\right) \tag{9.17}$$

If C_{jsw} is large than zero, C_{jbssw} is calculated by

if $V_{bs} < 0$

(9.18)

$$C_{jbssw} = C_{jsw}\left(1 - \frac{V_{bs}}{P_{bsw}}\right)^{-M_{jsw}}$$

otherwise

(9.19)

$$C_{jbssw} = C_{jsw}\left(1 + M_{jsw}\frac{V_{bs}}{P_{bsw}}\right)$$

If C_{jswg} is larger than zero, C_{jbsswg} is calculated by

if $V_{bs} < 0$

(9.20)

$$C_{jbsswg} = C_{jswg}\left(1 - \frac{V_{bs}}{P_{bswg}}\right)^{-M_{jswg}}$$

otherwise

(9.21)

$$C_{jbsswg} = C_{jswg}\left(1 + M_{jswg}\frac{V_{bs}}{P_{bswg}}\right)$$

9.2.2 D/B Junction Capacitance

The D/B junction capacitance can be calculated by

If $P_d > W_{eff}$

$$Capbd = A_d C_{jbd} + (P_d - W_{eff}) C_{jbdsw} + W_{eff} C_{jbdswg} \tag{9.22}$$

Otherwise

$$Capbd = A_d C_{jbd} + P_d C_{jbdswg} \tag{9.23}$$

where C_{jbd} is the unit bottom area capacitance of the D/B junction, C_{jbdsw} is the periphery capacitance of the D/B junction along the field oxide side, and C_{jbdswg} is the periphery capacitance of the D/B junction along the gate oxide side.

If C_j is larger than zero, C_{jbd} is calculated by

if $V_{bd} < 0$

$$C_{jbd} = C_j \left(1 - \frac{V_{bd}}{P_b}\right)^{-M_j} \tag{9.24}$$

otherwise

$$C_{jbd} = C_j \left(1 + M_j \frac{V_{bd}}{P_b}\right) \tag{9.25}$$

If C_{jsw} is large than zero, C_{jbdsw} is calculated by

if $V_{bd} < 0$

(9.26)

$$C_{jbdsw} = C_{jsw}\left(1-\frac{V_{bd}}{P_{bsw}}\right)^{-M_{jsw}}$$

otherwise

(9.27)

$$C_{jbdsw} = C_{jsw}\left(1+M_{jsw}\frac{V_{bd}}{P_{bsw}}\right)$$

If C_{jswg} is larger than zero, C_{jbdswg} is calculated by

if $V_{bd} < 0$

(9.28)

$$C_{jbdswg} = C_{jswg}\left(1-\frac{V_{bd}}{P_{bswg}}\right)^{-M_{jswg}}$$

otherwise

(9.29)

$$C_{jbdswg} = C_{jswg}\left(1+M_{jswg}\frac{V_{bd}}{P_{bswg}}\right)$$

9.2.3 Temperature Dependence of Junction Capacitance

The temperature dependence of the junction capacitance is modeled. Both zero-bias unit-area junction capacitance (C_j, C_{jsw} and C_{jswg}) and built-in potential of the junction (P_b, P_{bsw} and P_{bswg}) are temperature dependent and modeled in the following.

For zero-bias junction capacitance:

$$C_j(T) = C_j(T_{nom}) \cdot (1 + tcj \cdot \Delta T) \tag{9.30a}$$

$$C_{jsw}(T) = C_{jsw}(T_{nom}) \cdot (1 + tcjsw \cdot \Delta T) \tag{9.30b}$$

$$C_{jswg}(T) = C_{jswg}(T_{nom}) \cdot (1 + tcjswg \cdot \Delta T) \tag{9.30c}$$

For the built-in potential:

$$P_b(T) = P_b(T_{nom}) - tpb \cdot \Delta T \tag{9.31a}$$

$$P_{bsw}(T) = P_{bsw}(T_{nom}) - tpbsw \Delta T \tag{9.31b}$$

$$P_{bswg}(T) = P_{bswg}(T_{nom}) - tpbswg \Delta T \tag{9.31c}$$

In Eqs. (9.30) and (9.31), the temperature difference is defined as

(9.32)

$$\Delta T = T - T_{nom}$$

The six new model parameters in the above equations are described in Table 9-2.

9.2.4 Junction Capacitance Parameters

The following table give a full description of those model parameters used in the diode junction capacitance modeling.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Cj	cj	Bottom junction capacitance per unit area at zero bias	5e-4	F/m^2
Mj	mj	Bottom junction capacitance grading coefficient	0.5	none
Pb	pb	Bottom junction built-in potential	1.0	V
Cjsw	cjsw	Source/drain sidewall junction capacitance per unit length at zero bias	5e-10	F/m
Mjsw	mjsw	Source/drain sidewall junction capacitance grading coefficient	0.33	none
Pbsw	pbsw	Source/drain side wall junction built-in potential	1.0	V
Cjswg	cjswg	Source/drain gate side wall junction capacitance per unit length at zero bias	Cjsw	F/m
Mjswg	mjswg	Source/drain gate side wall junction capacitance grading coefficient	Mjsw	none
Pbswg	pbswg	Source/drain gate side wall junction built-in potential	Pbsw	V
tpb	tpb	Temperature coefficient of Pb	0.0	V/K
tpbsw	tpbsw	Temperature coefficient of Pbsw	0.0	V/K

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
tpbswg	tpbswg	Temperature coefficient of Pbswg	0.0	V/K
tcj	tcj	Temperature coefficient of Cj	0.0	1/K
tcjsw	tcjsw	Temperature coefficient of Cjsw	0.0	1/K
tcjswg	tcjswg	Temperature coefficient of Cjswg	0.0	1/K

Table 9-2. MOS Junction Capacitance Model Parameters.

APPENDIX A: Parameter List

A.1 Model Control Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
None	level	The model selector	8	none	
None	version	Model version selector	3.3	none	
None	binUnit	Bining unit selector	1	none	
None	paramChk	Parameter value check	False	none	
mobMod	mobMod	Mobility model selector	1	none	
capMod	capMod	Flag for capacitance models	3	none	
nqsMod[a]	nqsMod	Flag for NQS model	0	none	
acnqsMod	acnqsMod	Flag for AC NQS model Both instance/model parameter	0	none	
noiMod	noiMod	Flag for noise models	1	none	

a. nqsMod is now an element (instance) parameter, no longer a model parameter.

A.2 DC Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Vth0	vth0	Threshold voltage @Vbs=0 for Large L.	0.7 (NMOS) -0.7 (PMOS)	V	nI-1
VFB	vfb	Flat-band voltage	Calculated	V	nI-1
K1	k1	First order body effect coefficient	0.5	$V^{1/2}$	nI-2
K2	k2	Second order body effect coefficient	0.0	none	nI-2
K3	k3	Narrow width coefficient	80.0	none	
K3b	k3b	Body effect coefficient of k3	0.0	1/V	
W0	w0	Narrow width parameter	2.5e-6	m	
Nlx	nlx	Lateral non-uniform doping parameter	1.74e-7	m	
Vbm	vbm	Maximum applied body bias in Vth calculation	-3.0	V	
Dvt0	dvt0	first coefficient of short-channel effect on Vth	2.2	none	
Dvt1	dvt1	Second coefficient of short-channel effect on Vth	0.53	none	
Dvt2	dvt2	Body-bias coefficient of short-channel effect on Vth	-0.032	1/V	
Dvt0w	dvt0w	First coefficient of narrow width effect on Vth for small channel length	0	1/m	
Dvt1w	dvtw1	Second coefficient of narrow width effect on Vth for small channel length	5.3e6	1/m	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Dvt2w	dvt2w	Body-bias coefficient of narrow width effect for small channel length	-0.032	1/V	
μ0	u0	Mobility at Temp = Tnom NMOSFET PMOSFET	 670.0 250.0	cm^2/Vs	
Ua	ua	First-order mobility degradation coefficient	2.25E-9	m/V	
Ub	ub	Second-order mobility degradation coefficient	5.87E-19	$(m/V)^2$	
Uc	uc	Body-effect of mobility degradation coefficient	mobMod =1, 2: -4.65e-11 mobMod =3: -0.046	m/V^2 1/V	
νsat	vsat	Saturation velocity at Temp = Tnom	8.0E4	m/sec	
A0	a0	Bulk charge effect coefficient for channel length	1.0	none	
Ags	ags	gate bias coefficient of Abulk	0.0	1/V	
B0	b0	Bulk charge effect coefficient for channel width	0.0	m	
B1	b1	Bulk charge effect width offset	0.0	m	
Keta	keta	Body-bias coefficient of bulk charge effect	-0.047	1/V	
A1	a1	First non-saturation effect parameter	0.0	1/V	
A2	a2	Second non-saturation factor	1.0	none	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Rdsw	rdsw	Parasitic resistance per unit width	0.0	Ω-μm^{Wr}	
Prwb	prwb	Body effect coefficient of Rdsw	0	$V^{-1/2}$	
Prwg	prwg	Gate bias effect coefficient of Rdsw	0	1/V	
Wr	wr	Width Offset from Weff for Rds calculation	1.0	none	
Wint	wint	Width offset fitting parameter from I-V without bias	0.0	m	
Lint	lint	Length offset fitting parameter from I-V without bias	0.0	m	
dWg	dwg	Coefficient of Weff's gate dependence	0.0	m/V	
dWb	dwb	Coefficient of Weff's substrate body bias dependence	0.0	$m/V^{1/2}$	
Voff	voff	Offset voltage in the subthreshold region at large W and L	-0.08	V	
Nfactor	nfactor	Subthreshold swing factor	1.0	none	
Eta0	eta0	DIBL coefficient in subthreshold region	0.08	none	
Etab	etab	Body-bias coefficient for the subthreshold DIBL effect	-0.07	1/V	
Dsub	dsub	DIBL coefficient exponent in subthreshold region	drout	none	
Cit	cit	Interface trap capacitance	0.0	F/m^2	
Cdsc	cdsc	Drain/Source to channel coupling capacitance	2.4E-4	F/m^2	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Cdscb	cdscb	Body-bias sensitivity of Cdsc	0.0	F/Vm^2	
Cdscd	cdscd	Drain-bias sensitivity of Cdsc	0.0	F/Vm^2	
Pclm	pclm	Channel length modulation parameter	1.3	none	
Pdiblc1	pdiblc1	First output resistance DIBL effect correction parameter	0.39	none	
Pdiblc2	pdiblc2	Second output resistance DIBL effect correction parameter	0.0086	none	
Pdiblcb	pdiblcb	Body effect coefficient of DIBL correction parameters	0	1/V	
Drout	drout	L dependence coefficient of the DIBL correction parameter in Rout	0.56	none	
Pscbe1	pscbe1	First substrate current body-effect parameter	4.24E8	V/m	
Pscbe2	pscbe2	Second substrate current body-effect parameter	1.0E-5	m/V	nI-3
Pvag	pvag	Gate dependence of Early voltage	0.0	none	
δ	delta	Effective Vds parameter	0.01	V	
Ngate	ngate	poly gate doping concentration	0	cm^{-3}	
$\alpha 0$	alpha0	The first parameter of impact ionization current	0	m/V	
$\alpha 1$	alpha1	Isub parameter for length scaling	0.0	1/V	
$\beta 0$	beta0	The second parameter of impact ionization current	30	V	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Rsh	rsh	Source drain sheet resistance in ohm per square	0.0	Ω/ square	
Js0sw	jssw	Side wall saturation current density	0.0	A/m	
Js0	js	Source drain junction saturation current per unit area	1.0E-4	A/m^2	
ijth	ijth	Diode limiting current	0.1	A	nI-3

A.3 C-V Model Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Xpart	xpart	Charge partitioning flag	0.0	none	
CGS0	cgso	Non LDD region source-gate overlap capacitance per channel length	calculated	F/m	nC-1
CGD0	cgdo	Non LDD region drain-gate overlap capacitance per channel length	calculated	F/m	nC-2
CGB0	cgbo	Gate bulk overlap capaci-tance per unit channel length	0.0	F/m	
Cj	cj	Bottom junction capacitance per unit area at zero bias	5.0e-4	F/m^2	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Mj	mj	Bottom junction capacitance grating coefficient	0.5		
Mjsw	mjsw	Source/Drain side wall junction capacitance grading coefficient	0.33	none	
Cjsw	cjsw	Source/Drain side wall junction capacitance per unit area	5.E-10	F/m	
Cjswg	cjswg	Source/drain gate side wall junction capacitance grading coefficient	Cjsw	F/m	
Mjswg	mjswg	Source/drain gate side wall junction capacitance grading coefficient	Mjsw	none	
Pbsw	pbsw	Source/drain side wall junction built-in potential	1.0	V	
Pb	pb	Bottom built-in potential	1.0	V	
Pbswg	pbswg	Source/Drain gate side wall junction built-in potential	Pbsw	V	
CGS1	cgs1	Light doped source-gate region overlap capacitance	0.0	F/m	
CGD1	cgd1	Light doped drain-gate region overlap capacitance	0.0	F/m	
CKAPPA	ckappa	Coefficient for lightly doped region overlap capacitance Fringing field capacitance	0.6	V	
Cf	cf	fringing field capacitance	calculated	F/m	nC-3
CLC	clc	Constant term for the short channel model	0.1E-6	m	
CLE	cle	Exponential term for the short channel model	0.6	none	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
DLC	dlc	Length offset fitting parameter from C-V	lint	m	
DWC	dwc	Width offset fitting parameter from C-V	wint	m	
Vfbcv	vfbcv	Flat-band voltage parameter (for capMod=0 only)	-1	V	
noff	noff	CV parameter in Vgsteff,CV for weak to strong inversion	1.0	none	nC-4
voffcv	voffcv	CV parameter in Vgsteff,CV for week to strong inversion	0.0	V	nC-4
acde	acde	Exponential coefficient for charge thickness in capMod=3 for accumulation and depletion regions	1.0	m/V	nC-4
moin	moin	Coefficient for the gate-bias dependent surface potential	15.0	none	nC-4

A.4 NQS Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Elm	elm	Elmore constant of the channel	5	none	

A.5 dW and dL Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Wl	wl	Coefficient of length dependence for width offset	0.0	m^{Wln}	
Wln	wln	Power of length dependence of width offset	1.0	none	
Ww	ww	Coefficient of width dependence for width offset	0.0	m^{Wwn}	
Wwn	wwn	Power of width dependence of width offset	1.0	none	
Wwl	wwl	Coefficient of length and width cross term for width offset	0.0	$m^{Wwn+Wln}$	
Ll	ll	Coefficient of length dependence for length offset	0.0	m^{Lln}	
Lln	lln	Power of length dependence for length offset	1.0	none	
Lw	lw	Coefficient of width dependence for length offset	0.0	m^{Lwn}	
Lwn	lwn	Power of width dependence for length offset	1.0	none	
Lwl	lwl	Coefficient of length and width cross term for length offset	0.0	$m^{Lwn+Lln}$	
Llc	Llc	Coefficient of length dependence for CV channel length offset	Ll	m^{Lln}	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Lwc	Lwc	Coefficient of width dependence for CV channel length offset	Lw	m^{Lwn}	
Lwlc	Lwlc	Coefficient of length and width-dependence for CV channel length offset	Lwl	$m^{Lwn+Lln}$	
Wlc	Wlc	Coefficient of length dependence for CV channel width offset	Wl	m^{Wln}	
Wwc	Wwc	Coefficient of widthdependence for CV channel width offset	Ww	m^{Wwn}	
Wwlc	Wwlc	Coefficient of length and width-dependence for CV channel width offset	Wwl	$m^{Wln+Wwn}$	

A.6 Temperature Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Tnom	tnom	Temperature at which parameters are extracted	27	^{o}C	
μte	ute	Mobility temperature exponent	-1.5	none	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Kt1	kt1	Temperature coefficient for threshold voltage	-0.11	V	
Kt1l	kt1l	Channel length dependence of the temperature coefficient for threshold voltage	0.0	Vm	
Kt2	kt2	Body-bias coefficient of Vth temperature effect	0.022	none	
Ua1	ua1	Temperature coefficient for Ua	4.31E-9	m/V	
Ub1	ub1	Temperature coefficient for Ub	-7.61E-18	$(m/V)^2$	
Uc1	uc1	Temperature coefficient for Uc	mobMod=1, 2: -5.6E-11 mobMod=3: -0.056	m/V^2 1/V	
At	at	Temperature coefficient for saturation velocity	3.3E4	m/sec	
Prt	prt	Temperature coefficient for Rdsw	0.0	Ω-μm	
At	at	Temperature coefficient for saturation velocity	3.3E4	m/sec	
nj	nj	Emission coefficient of junction	1.0	none	
XTI	xti	Junction current temperature exponent coefficient	3.0	none	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
tpb	tpb	Temperature coefficient of Pb	0.0	V/K	
tpbsw	tpbsw	Temperature coefficient of Pbsw	0.0	V/K	
tpbswg	tpbswg	Temperature coefficient of Pbswg	0.0	V/K	
tcj	tcj	Temperature coefficient of Cj	0.0	1/K	
tcjsw	tcjsw	Temperature coefficient of Cjsw	0.0	1/K	
tcjswg	tcjswg	Temperature coefficient of Cjswg	0.0	1/K	

A.7 Flicker Noise Model Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Noia	noia	Noise parameter A	(NMOS) 1e20 (PMOS) 9.9e18	none	
Noib	noib	Noise parameter B	(NMOS) 5e4 (PMOS) 2.4e3	none	
Noic	noic	Noise parameter C	(NMOS) -1.4e-12 (PMOS) 1.4e-12	none	
Em	em	Saturation field	4.1e7	V/m	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Af	af	Flicker noise exponent	1	none	
Ef	ef	Flicker noise frequency exponent	1	none	
Kf	kf	Flicker noise coefficient	0	none	
LINTNOI	lintnoi	Length Reduction Parameter Offset	0.0	m	

A.8 Process Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Tox	tox	Gate oxide thickness	1.5e-8	m	
Toxm	toxm	Tox at which parameters are extracted	Tox	m	nI-3
Xj	xj	Junction Depth	1.5e-7	m	
$\gamma 1$	gamma1	Body-effect coefficient near the surface	calculated	$V^{1/2}$	nI-5
$\gamma 2$	gamma2	Body-effect coefficient in the bulk	calculated	$V^{1/2}$	nI-6
Nch	nch	Channel doping concentration	1.7e17	$1/cm^3$	nI-4
Nsub	nsub	Substrate doping concentration	6e16	$1/cm^3$	
Vbx	vbx	Vbs at which the depletion region width equals xt	calculated	V	nI-7
Xt	xt	Doping depth	1.55e-7	m	

A.9 Geometry Range Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Lmin	lmin	Minimum channel length	0.0	m	
Lmax	lmax	Maximum channel length	1.0	m	
Wmin	wmin	Minimum channel width	0.0	m	
Wmax	wmax	Maximum channel width	1.0	m	
binUnit	binunit	Bin unit scale selector	1.0	none	

A.10Model Parameter Notes

nI-1. If V_{th0} is not specified, it is calculated by

$$V_{th0} = V_{FB} + \Phi_s + K_1\sqrt{\Phi_s}$$

where the model parameter V_{FB}=-1.0. If V_{th0} is specified, V_{FB} defaults to

$$V_{FB} = V_{th0} - \Phi_s - K_1\sqrt{\Phi_s}$$

nI-2. If K_1 and K_2 are not given, they are calculated based on

$$K_1 = \gamma_2 - 2K_2\sqrt{\Phi_s - V_{bm}}$$

$$K_2 = \frac{(\gamma_1 - \gamma_2)\left(\sqrt{\Phi_s - V_{bx}} - \sqrt{\Phi_s}\right)}{2\sqrt{\Phi_s}\left(\sqrt{\Phi_s - V_{bm}} - \sqrt{\Phi_s}\right) + V_{bm}}$$

where Φ_s is calculated by

$$\Phi_s = 2V_{tm0}\ln\left(\frac{N_{ch}}{n_i}\right)$$

$$V_{tm0} = \frac{k_B T_{nom}}{q}$$

$$n_i = 1.45\times10^{10}\left(\frac{T_{nom}}{300.15}\right)^{1.5}\exp\left(21.5565981 - \frac{E_{g0}}{2V_{tm0}}\right)$$

$$E_{g0} = 1.16 - \frac{7.02\times10^{-4}T_{nom}{}^2}{T_{nom} + 1108}$$

where E_{g0} is the energy bandgap at temperature T_{nom}.

nI-3.

If *pscbe*2 <= 0.0, a warning message will be given.
If *ijth* < 0.0, a fatal error message will occur.

If *Toxm* < = 0.0, a fatal error message will occur.

nI-4. If N_{ch} is not given and γ_1 is given, N_{ch} is calculated from

$$N_{ch} = \frac{\gamma_1^{\,2} C_{ox}^{\,2}}{2q\varepsilon_{si}}$$

If both γ_1 and N_{ch} are not given, N_{ch} defaults to 1.7e23 m^{-3} and γ_1 is calculated from N_{ch}.

nI-5. If γ_1 is not given, it is calculated by

$$\gamma_1 = \frac{\sqrt{2q\varepsilon_{si}N_{ch}}}{C_{ox}}$$

nI-6. If γ_2 is not given, it is calculated by

$$\gamma_2 = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C_{ox}}$$

nI-7. If V_{bx} is not given, it is calculated by

$$\frac{qN_{ch}X_t^{\,2}}{2\varepsilon_{si}} = \Phi_s - V_{bx}$$

nC-1. If *Cgso* is not given, it is calculated by

if (*dlc* is given and is greater 0),
    Cgso = *dlc* * *Cox* - *Cgs*1
    if (*Cgso* < 0)
    Cgso = 0
else *Cgso* = 0.6 *Xj* * *Cox*

nC-2. If *Cgdo* is not given, it is calculated by

if (*dlc* is given and is greater than 0),
Cgdo = *dlc* * *Cox* - *Cgd*1
if (*Cgdo* < 0)
Cgdo = 0
else *Cgdo* = 0.6 *Xj* * *Cox*

nC-3. If *CF* is not given then it is calculated usin by

$$CF = \frac{2\varepsilon_{ox}}{\pi}\ln\left(1+\frac{4\times10^{-7}}{Tox}\right)$$

nC-4.

If (*acde* < 0.4) or (*acde* > 1.6), a warning message will be given.
If (*moin* < 5.0) or (*moin* > 25.0), a warning message will be given.
If (*noff* < 0.1) or (*noff* > 4.0), a warning message will be given.
If (*voffcv* < -0.5) or (*voffcv* > 0.5), a warning message will be given.

APPENDIX B: Equation List

B.1 I-V Model

B.1.1 Threshold Voltage

$$
\begin{aligned}
V_{th} &= V_{th0ox} + K_{1ox}\cdot\sqrt{\Phi_s - V_{bseff}} - K_{2ox}V_{bseff} \\
&\quad + K_{1ox}\left(\sqrt{1+\frac{Nlx}{L_{eff}}}-1\right)\sqrt{\Phi_s} + \left(K_3 + K_{3b}V_{bseff}\right)\frac{T_{ox}}{W_{eff}'+W_0}\Phi_s \\
&\quad - D_{VT0w}\left(\exp\left(-D_{VT1w}\frac{W_{eff}'L_{eff}}{2l_{tw}}\right)+2\exp\left(-D_{VT1w}\frac{W_{eff}'L_{eff}}{l_{tw}}\right)\right)\left(V_{bi}-\Phi_s\right) \\
&\quad - D_{VT0}\left(\exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right)+2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)\left(V_{bi}-\Phi_s\right) \\
&\quad - \left(\exp\left(-D_{sub}\frac{L_{eff}}{2l_{to}}\right)+2\exp\left(-D_{sub}\frac{L_{eff}}{l_{to}}\right)\right)\left(E_{tao}+E_{tab}V_{bseff}\right)V_{ds}
\end{aligned}
$$

$$
V_{th0ox} = V_{th0} - K_1\cdot\sqrt{\Phi_s}
$$

$$
K_{1ox} = K_1\cdot\frac{T_{ox}}{T_{oxm}}
$$

$$
K_{2ox} = K_2\cdot\frac{T_{ox}}{T_{oxm}}
$$

$$l_t = \sqrt{e_{si} X_{dep} / C_{ox}}(1 + D_{VT2} V_{bseff})$$

$$l_{tw} = \sqrt{e_{si} X_{dep} / C_{ox}}(1 + D_{VT2w} V_{bseff})$$

$$l_{to} = \sqrt{e_{si} X_{dep0} / C_{ox}}$$

$$X_{dep} = \sqrt{\frac{2e_{si}(\Phi_s - V_{bseff})}{qN_{ch}}}$$

$$X_{dep0} = \sqrt{\frac{2e_{si}\Phi_s}{qN_{ch}}}$$

($\delta 1$=0.001)

$$V_{bseff} = V_{bc} + 0.5[V_{bs} - V_{bc} - d_1 + \sqrt{(V_{bs} - V_{bc} - d_1)^2 - 4d_1 V_{bc}}\ ]$$

$$V_{bc} = 0.9\left(\Phi_s - \frac{K_1^{\ 2}}{4K_2^{\ 2}}\right)$$

$$V_{bi} = v_t \ln(\frac{N_{ch} N_{DS}}{n_i^{\ 2}})$$

B.1.2 Effective (V_{gs}-V_{th})

$$V_{gsteff} = \frac{2\, n\, v_t \ln\left[1 + \exp(\frac{V_{gs} - V_{th}}{2\, n\, v_t})\right]}{1 + 2\, n\ \ C_{OX}\sqrt{\frac{2\Phi_s}{qe_{si}N_{ch}}}\exp(-\frac{V_{gs} - V_{th\,-}\, 2V_{off}}{2\, n\, v_t})}$$

$$n = 1 + N_{factor}\frac{C_d}{C_{ox}} + \frac{(C_{dsc} + C_{dscd}V_{ds} + C_{dscb}V_{bseff})\left(\exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + 2\exp(-D_{VT1}\frac{L_{eff}}{l_t})\right)}{C_{ox}} + \frac{C_{it}}{C_{ox}}$$

$$C_d = \frac{e_{si}}{X_{dep}}$$

B.1.3 Mobility

For mobMod=1

$$m_{eff} = \frac{m_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{OX}})^2}$$

For mobMod=2

$$m_{eff} = \frac{m_o}{1 + (U_{a+} U_c V_{bseff})(\frac{V_{gsteff}}{T_{OX}}) + U_b(\frac{V_{gsteff}}{T_{OX}})^2}$$

For mobMod=3

$$m_{eff} = \frac{m_o}{1 + [U_a(\frac{V_{gsteff} + 2V_{th}}{T_{OX}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{OX}})^2](1 + U_c V_{bseff})}$$

B.1.4 Drain Saturation Voltage

For $R_{ds} > 0$ or $\lambda \neq 1$:

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{bulk}{}^2 W_{eff} n_{sat} C_{ox} R_{DS} + (\frac{1}{l} - 1) A_{bulk}$$

$$b = -\left((V_{gsteff} + 2v_t)(\frac{2}{l} - 1) + A_{bulk} E_{sat} L_{eff} + 3A_{bulk}(V_{gsteff} + 2v_t) W_{eff} n_{sat} C_{ox} R_{DS} \right)$$

$$c = (V_{gsteff} + 2v_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff} n_{sat} C_{ox} R_{DS}$$

$$l = A_1 V_{gsteff} + A_2$$

For $R_{ds} = 0$ and $\lambda = 1$:

$$V_{dsat} = \frac{E_{sat}\ L_{eff}\ (V_{gsteff} + 2v_t)}{A_{bulk}\ E_{sat}\ \ L_{eff} + (V_{gsteff} + 2v_t)}$$

$$A_{bulk} = \left(1 + \frac{K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}} \left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}} \left(1 - A_{gs} V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}} \right)^2 \right) + \frac{B_0}{W_{eff}' + B_1} \right) \right) \frac{1}{1 + Keta V_{bseff}}$$

$$E_{sat} = \frac{2\nu_{sat}}{\mu_{eff}}$$

B.1.5 Effective V_{ds}

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right)$$

B.1.6 Drain Current Expression

$$I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds} I_{dso(Vdseff)}}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

$$I_{dso} = \frac{W_{eff}\mu_{eff}C_{ox}V_{gsteff}\left(1 - A_{bulk}\frac{V_{dseff}}{2(V_{gsteff} + 2\nu_t)}\right)V_{dseff}}{L_{eff}\left[1 + V_{dseff} / (E_{sat}L_{eff})\right]}$$

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag}V_{gsteff}}{E_{sat}L_{eff}}\right)\left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1}$$

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{P_{CLM}A_{bulk}E_{sat}\,litl}(V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{q_{rout}(1 + P_{DIBLCB}V_{bseff})}\left(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat} + V_{gsteff} + 2v_t}\right)$$

$$q_{rout} = P_{DIBLC1}\left[\exp(-D_{ROUT}\frac{L_{eff}}{2l_{t0}}) + 2\exp(-D_{ROUT}\frac{L_{eff}}{l_{t0}})\right] + P_{DIBLC2}$$

$$\frac{1}{V_{ASCBE}} = \frac{P_{scbe2}}{L_{eff}}\exp\left(\frac{-P_{scbe1}\,litl}{V_{ds} - V_{dseff}}\right)$$

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{DS}n_{sat}C_{ox}W_{eff}V_{gsteff}[1 - \frac{A_{bulk}V_{dsat}}{2(V_{gsteff} + 2v_t)}]}{2/l - 1 + R_{DS}n_{sat}C_{ox}W_{eff}A_{bulk}}$$

$$litl = \sqrt{\frac{e_{si}T_{ox}X_j}{e_{ox}}}$$

B.1.7 Substrate Current

$$I_{sub} = \frac{a_0 + a_1 \cdot L_{eff}}{L_{eff}}(V_{ds} - V_{dseff})\exp\left(-\frac{b_0}{V_{ds} - V_{dseff}}\right)\frac{I_{ds0}}{1 + \frac{R_{ds}I_{ds0}}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)$$

B.1.8 Polysilicon Depletion Effect

$$V_{poly} = \frac{1}{2} X_{poly} E_{poly} = \frac{qN_{gate} X_{poly}^2}{2e_{si}}$$

$$e_{ox} E_{ox} = e_{si} E_{poly} = \sqrt{2qe_{si} N_{gate} V_{poly}}$$

$$V_{gs} - V_{FB} - \Phi_s = V_{poly} + V_{ox}$$

$$a\left(V_{gs} - V_{FB} - \Phi_s - V_{poly}\right)^2 - V_{poly} = 0$$

$$a = \frac{e_{ox}^2}{2qe_{si} N_{gate} T_{ox}^2}$$

$$V_{gs\_eff} = V_{FB} + \Phi_s + \frac{qe_{si} N_{gate} T_{ox}^2}{e_{ox}^2} \left(\sqrt{1 + \frac{2e_{ox}^2 \left(V_{gs} - V_{FB} - \Phi_s\right)}{qe_{si} N_{gate} T_{ox}^2}} - 1 \right)$$

B.1.9 Effective Channel Length and Width

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - 2dW$$

$$W_{eff}' = W_{drawn} - 2dW'$$

$$dW = dW' + dW_g V_{gsteff} + dW_b\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right)$$
$$dW' = W_{\text{int}} + \frac{W_l}{L^{W\ln}} + \frac{W_w}{W^{Wwn}} + \frac{W_{wl}}{L^{W\ln}W^{Wwn}}$$

$$dL = L_{\text{int}} + \frac{L_l}{L^{L\ln}} + \frac{L_w}{W^{Lwn}} + \frac{L_{wl}}{L^{L\ln}W^{Lwn}}$$

B.1.10 Source/Drain Resistance

$$R_{ds} = \frac{R_{dsw}\left(1 + P_{rwg}V_{gsteff} + P_{rwb}\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right)\right)}{\left(10^6 W_{eff}'\right)^{W_r}}$$

B.1.11 Temperature Effects

$$V_{th(T)} = V_{th(Tnorm)} + (K_{T1} + K_{t1l}/L_{eff} + K_{T2}V_{bseff})(T/T_{norm} - 1)$$

$$m_{o(T)} = m_{o(Tnorm)}\left(\frac{T}{T_{norm}}\right)^{m_e}$$

$$v_{sat(T)} = v_{sat(Tnorm)} - A_T(T/T_{norm} - 1)$$

$$R_{dsw(T)} = R_{dsw(}T_{norm)} + \mathrm{P}_{r\,t}(\frac{T}{T_{norm}} - 1)$$

$$U_{a(T)} = U_{a(Tnorm)} + U_{a1}(T / T_{norm} - 1)$$

$$U_{b(T)} = U_{b(Tnorm)} + U_{b1}(T / T_{norm} - 1)$$

$$U_{c(T)} = U_{c(Tnorm)} + U_{c1}(T / T_{norm} - 1)$$

B.2 Capacitance Model Equations

B.2.1 Dimension Dependence

$$\mathrm{L}_{\mathrm{active}} = \mathrm{L}_{\mathrm{drawn}} - 2\delta\mathrm{L}_{\mathrm{eff}}$$

$$\mathrm{W}_{\mathrm{active}} = \mathrm{W}_{\mathrm{drawn}} - 2\delta\mathrm{W}_{\mathrm{eff}}$$

$$dL_{eff} = DLC + \frac{Llc}{L^{L\ln}} + \frac{Lwc}{W^{Lwn}} + \frac{Lwlc}{L^{L\ln}W^{Lwn}}$$

$$dW_{eff} = DWC + \frac{Wlc}{L^{W\ln}} + \frac{Wwc}{W^{Wwn}} + \frac{Wwlc}{L^{W\ln}W^{Wwn}}$$

B.2.2 Overlap Capacitance

B.2.2.1 Source Overlap Capacitance

(1) for capMod = 0

$$\frac{Q_{overlap,s}}{W_{active}} = \mathrm{CGS0}V_{gs}$$

(2) for capMod = 1

If $V_{gs} < 0$

$$\frac{Q_{overlap,s}}{W_{active}} = CGS0 \cdot V_{gs} + \frac{CKAPPA \cdot CGS1}{2}\left(-1+\sqrt{1-\frac{4V_{gs}}{CKAPPA}}\right)$$

Else

$$\frac{Q_{overlap,s}}{W_{active}} = \left(CGS0 + CKAPPA \cdot CGS1\right) \cdot V_{gs}$$

(3) for capMod = 2

$$\frac{Q_{overlap,s}}{W_{active}} = CGS0 \cdot V_{gs} + CGS1\left(V_{gs} - V_{gs,overlap} - \frac{CKAPPA}{2}\left(-1+\sqrt{1-\frac{4V_{gs,overlap}}{CKAPPA}}\right)\right)$$

$$V_{gs,overlap} = \frac{1}{2}\left(V_{gs} + d_1 - \sqrt{\left(V_{gs}+d_1\right)^2 + 4d_1}\right), \quad d_1 = 0.02$$

B.2.2.2 Drain Overlap Capacitance

(1) for capMod = 0

$$\frac{Q_{overlap,d}}{W_{active}} = \text{CGD0}V_{gd}$$

(2) for capMod = 1

If $V_{gd} < 0$

$$\frac{Q_{overlap,d}}{W_{active}} = CGD0 \cdot V_{gs} + \frac{CKAPPA \cdot CGD1}{2}\left(-1+\sqrt{1-\frac{4V_{gd}}{CKAPPA}}\right)$$

Else

$$\frac{Q_{overlap,d}}{W_{active}} = \left(CGD0 + CKAPPA \cdot CGD1\right) \cdot V_{gd}$$

(3) for capMod = 2

$$\frac{Q_{overlap,d}}{W_{active}} = CGD0 \cdot V_{gd} + CGD1\left(V_{gd} - V_{gd,overlap} - \frac{CKAPPA}{2}\left(-1+\sqrt{1-\frac{4V_{gd,overlap}}{CKAPPA}}\right)\right)$$

$$V_{gd,overlap} = \frac{1}{2}\left(V_{gd} + d_1 - \sqrt{\left(V_{gd} + d_1\right)^2 + 4d_1}\right) \quad d_1 = 0.02$$

B.2.2.3 Gate Overlap Charge

$$Q_{overlap,g} = -\left(Q_{overlap,s} + Q_{overlap,d}\right)$$

B.2.3 Instrinsic Charges

(1) **capMod = 0**

a. Accumulation region ($V_{gs} < V_{fbcv} + V_{bs}$)

$$Q_g = W_{active} L_{active} C_{ox} \left(V_{gs} - V_{bs} - V_{fbcv}\right)$$

$$Q_{sub} = -Q_g$$

$$Q_{inv} = 0$$

b. Subthreshold region ($V_{gs} < V_{th}$)

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \cdot \frac{K_{1ox}^{\ 2}}{2}\left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{fbcv} - V_{bs}\right)}{K_{1ox}^{\ 2}}}\right)$$

$$Q_g = -Q_b$$

$$Q_{inv} = 0$$

c. Strong inversion ($V_{gs} > V_{th}$)

$$V_{dsat,cv} = \frac{V_{gs} - V_{th}}{A_{bulk}'}$$

$$A_{bulk}' = A_{bulk0}\left(1 + \left(\frac{CLC}{Leff}\right)^{CLE}\right)$$

$$A_{bulk0} = \left(1 + \frac{K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}}\left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}} + \frac{B_0}{W_{eff}' + B_1}\right)\right)\cdot\frac{1}{1 + Keta V_{bseff}}$$

$$V_{th} = V_{fbcv} + \Phi_s + K_{1ox}\sqrt{\Phi_s - V_{bseff}}$$

(i) 50/50 Charge partition

If $V_{ds} < V_{dsat}$

$$Q_g = C_{ox} W_{active} L_{active}\left(V_{gs} - V_{fbcv} - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2}\right)}\right)$$

$$Q_{inv} = -W_{active} L_{active} C_{ox} [V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_b = W_{active} L_{active} C_{ox} [V_{fb} - V_{th} + F_s + \frac{(1 - A_{bulk}') V_{ds}}{2} - \frac{(1 - A_{bulk}') A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_s = Q_d = 0.5 Q_{inv} = -W_{active} L_{active} C_{ox} [V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

otherwise

$$Q_g = W_{active} L_{active} C_{ox} (V_{gs} - V_{fb} - F_s - \frac{V_{dsat}}{3})$$

$$Q_s = Q_d = -\frac{1}{3} W_{active} L_{active} C_{ox} (V_{gs} - V_{th})$$

$$Q_b = -W_{active} L_{active} C_{ox} (V_{fb} + F_s - V_{th} + \frac{(1 - A_{bulk}') V_{dsat}}{3})$$

(ii) 40/60 channel-charge Partition

if ($V_{ds} < V_{dsat}$)

$$Q_g = C_{ox} W_{active} L_{active} [V_{gs} - V_{fb} - F_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2})}]$$

$$Q_{inv} = -W_{active} L_{active} C_{ox} [V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_b = W_{active} L_{active} C_{ox} [V_{fb} - V_{th} + F_s + \frac{(1 - A_{bulk}') V_{ds}}{2} - \frac{(1 - A_{bulk}') A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_d = -W_{active} L_{active} C_{ox}$$
$$\left[\frac{V_{gs} - V_{th}}{2} - \frac{A_{bulk}'}{2} V_{ds} + \frac{A_{bulk}' V_{ds} [\frac{(V_{gs} - V_{th})^2}{6} - \frac{A_{bulk}' V_{ds} (V_{gs} - V_{th})}{8} + \frac{(A_{bulk}' V_{ds})^2}{40}}{(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})^2} \right]$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

otherwise

$$Q_g = W_{active} L_{active} C_{ox} (V_{gs} - V_{fb} - F_s - \frac{V_{dsat}}{3})$$

$$Q_d = -\frac{4}{15} W_{active} L_{active} C_{ox} (V_{gs} - V_{th})$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

$$Q_b = -W_{active} L_{active} C_{ox} (V_{fb} + F_s - V_{th} + \frac{(1 - A_{bulk}')V_{dsat}}{3})$$

(iii) 0/100 Channel-charge Partition

if $V_{ds} < V_{dsat}$

$$Q_g = C_{ox} W_{active} L_{active} [V_{gs} - V_{fb} - F_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2})}]$$

$$Q_{inv} = -W_{active} L_{active} C_{ox} [V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_b = W_{active} L_{active} C_{ox} [V_{fb} - V_{th} + F_s + \frac{(1 - A_{bulk}')V_{ds}}{2} - \frac{(1 - A_{bulk}')A_{bulk}' V_{ds}^2}{12(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})}]$$

$$Q_d = -W_{active} L_{active} C_{ox} \left[\frac{V_{gs} - V_{th}}{2} + \frac{A_{bulk}'}{4} V_{ds} - \frac{(A_{bulk}' V_{ds})^2}{24(V_{gs} - V_{th} - \frac{A_{bulk}'}{2} V_{ds})} \right]$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

otherwise

$$Q_g = W_{active} L_{active} C_{ox} (V_{gs} - V_{fb} - F_s - \frac{V_{dsat}}{3})$$

$$Q_b = -W_{active} L_{active} C_{ox} (V_{fb} + F_s - V_{th} + \frac{(1 - A_{bulk}')V_{dsat}}{3})$$

$$Q_d = 0$$

$$Qs = -\left(Q_g + Q_b\right)$$

(2) **capMod = 1**

The flat-band voltage V_{fb} is calculated from

$$V_{fb} = V_{th} - \Phi_s - K_{1ox} \sqrt{\Phi_s - V_{bseff}}$$

where the bias dependences of V_{th} given in Section B.1.1 are not considered in calculating V_{fb} for capMod = 1.

if ($V_{gs} < V_{fb} + V_{bs} + V_{gsteffcv}$)

$$Q_{gl} = W_{active} L_{active} C_{ox} \left(V_{gs} - V_{fb} - V_{bs} - V_{gsteffcv} \right)$$

else

$$Q_{g1} = W_{active} L_{active} C_{ox} \cdot \frac{K_{1ox}^{\ 2}}{2} \left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{fb} - V_{gsteff,CV} - V_{bseff}\right)}{K_{1ox}^{\ 2}}} \right)$$

$$Q_{b1} = -Q_{g1}$$

$$V_{dsat,cv} = \frac{V_{gsteffcv}}{A_{bulk}'}$$

$$\mathrm{A_{bulk}}' = \mathrm{A_{bulk0}} \left(1 + \left(\frac{CLC}{\mathrm{L_{eff}}} \right)^{CLE} \right)$$

$$A_{bulk0} = \left(1 + \frac{K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}} \left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}} + \frac{B_0}{W_{eff}' + B_1} \right) \right) \cdot \frac{1}{1 + Keta V_{bseff}}$$

$$V_{gsteff,cv} = noff \cdot nv_t \ln\left(1+\exp\left(\frac{V_{gs}-V_{th}-voffcv}{noff \cdot nv_t}\right)\right)$$

if ($V_{ds} <= V_{dsat}$)

$$Q_g = Q_{g1} + W_{active} L_{active} C_{ox}\left(V_{gsteff\,cv} - \frac{V_{ds}}{2} + \frac{A_{bulk}{}' V_{ds}{}^2}{12\left(V_{gsteff\,cv} - \frac{A_{bulk}{}'}{2} V_{ds}\right)}\right)$$

$$Q_b = Q_{b1} + W_{active} L_{active} C_{ox}\left(\frac{1-A_{bulk}{}'}{2} V_{ds} - \frac{(1-A_{bulk}{}')A_{bulk}{}' V_{ds}{}^2}{12\left(V_{gsteffcv} - \frac{A_{bulk}{}'}{2} V_{ds}\right)}\right)$$

(i) 50/50 Channel-charge Partition

$$Q_s = Q_d = -\frac{W_{active} L_{active} C_{ox}}{2}\left(V_{gsteff\,cv} - \frac{A_{bulk}{}'}{2} V_{ds} + \frac{A_{bulk}{}'^2 V_{ds}{}^2}{12\left(V_{gsteffcv} - \frac{A_{bulk}{}'}{2} V_{ds}\right)}\right)$$

(ii) 40/60 Channel-charge partition

$$Q_s = -\frac{W_{active} L_{active} C_{ox}}{2\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2} V_{ds}\right)^2}$$
$$\left(V_{gsteffcv}{}^3 - \frac{4}{3} V_{gstefcvf}{}^2 \left(A_{bulk}' V_{ds}\right) + \frac{2}{3} V_{gsteffcv} \left(A_{bulk}' V_{ds}\right)^2 - \frac{2}{15} \left(A_{bulk}' V_{ds}\right)^3\right)$$

$$Q_d = -(Q_g + Q_b + Q_s)$$

(iii) 0/100 Channel-charge Partition

$$Q_s = -W_{active} L_{active} C_{ox} \left(\frac{V_{gstefcv}}{2} + \frac{A_{bulk}' V_{ds}}{4} - \frac{\left(A_{bulk}' V_{ds}\right)^2}{24\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{ds}\right)} \right)$$

$$Q_d = -(Q_g + Q_b + Q_s)$$

if ($V_{ds} > V_{dsat}$)

$$Q_g = Q_{g1} + W_{active} L_{active} C_{ox} \left(V_{gsteff\,cv} - \frac{V_{dsat}}{3} \right)$$

$$Q_b = Q_{b1} - W_{active} L_{active} C_{ox} \frac{\left(V_{gsteffcv} - V_{dsat}\right)}{3}$$

(i) 50/50 Channel-charge Partition

$$Q_s = Q_d = -\frac{W_{active} L_{active} C_{ox}}{3} V_{gsteff}{}^{cv}$$

(ii) 40/60 Channel-charge Partition

$$Q_s = -\frac{2W_{active} L_{active} C_{ox}}{5} V_{gsteffcv}$$

$$Q_d = -(Q_g + Q_b + Q_s)$$

(iii) 0/100 Channel-charge Partition

$$Q_s = -W_{active} L_{active} C_{ox} \frac{2V_{gstefcv}}{3}$$

$$Q_d = -(Q_g + Q_b + Q_s)$$

(3) **capMod = 2**

The flat-band voltage V_{fb} is calculated from

$$vfb = V_{th} - \Phi_s - K_{1ox}\sqrt{\Phi_s - V_{bseff}}$$

where the bias dependences of V_{th} given in Section B.1.1 are not considered in calculating V_{fb} for capMod = 2.

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub}\right)$$

$$Q_b = Q_{acc} + Q_{sub\,0} + \delta Q_{sub}$$

$$Q_{inv} = Q_s + Q_d$$

$$V_{FBeff} = vfb - 0.5\left\{V_3 + \sqrt{V_3^{\,2} + 4d_3 vfb}\right\} \quad where \quad V_3 = vfb - V_{gb} - d_3; \;\; d_3 = 0.02$$

$$Q_{acc} = -W_{active} L_{active} C_{ox}\left(V_{FBeff} - vfb\right)$$

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \cdot \frac{K_{1ox}^{\,2}}{2}\left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{FBeff} - V_{gsteff,CV} - V_{bseff}\right)}{K_{1ox}^{\,2}}}\right)$$

$$V_{dsat,cv} = \frac{V_{gsteff,cv}}{A_{bulk}'}$$

$$A_{bulk}' = A_{bulk\,0}\left(1 + \left(\frac{\mathrm{CLC}}{L_{active}}\right)^{\mathrm{CLE}}\right.$$

$$A_{bulk0} = \left(1 + \frac{K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}}\left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}} + \frac{B_0}{W_{eff}' + B_1}\right)\right) \cdot \frac{1}{1 + Keta V_{bseff}}$$

$$V_{gsteff,cv} = noff \cdot nv_t \ln\left(1 + \exp\left(\frac{V_{gs} - V_{th} - voffcv}{noff \cdot nv_t}\right)\right)$$

$$V_{cveff} = V_{dsat,cv} - 0.5\left\{V_4 + \sqrt{V_4^2 + 4d_4 V_{dsat,cv}}\right\} \quad where \quad V_4 = V_{dsat,cv} - V_{ds} - d_4; \quad d_4 = 0.02$$

$$Q_{inv} = -W_{active} L_{active} C_{ox}\left(\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2} V_{cveff}\right) + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2} V_{cveff}\right)}\right)$$

$$dQ_{sub} = W_{active} L_{active} C_{ox}\left(\frac{1 - A_{bulk}'}{2} V_{cveff} - \frac{(1 - A_{bulk}')A_{bulk}' V_{cveff}^2}{12\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff}\right)}\right)$$

B.2.3.1 50/50 Charge partition

$$Q_s = Q_d = 0.5 Q_{inv} = -\frac{W_{active} L_{active} C_{ox}}{2} \left(V_{gsteff^{cv}} - \frac{A_{bulk}'}{2} V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteffcv} - \frac{A_{bulk}}{2} V_{cveff} \right)} \right)$$

B.2.3.2 40/60 Channel-charge Partition

$$Q_s = -\frac{W_{active} L_{active} C_{ox}}{2\left(V_{gsteff^{cv}} - \frac{A_{bulk}'}{2} V_{cveff} \right)^2} \left(V_{gsteffcv}^3 - \frac{4}{3} V_{gsteffc}^2 \left(A_{bulk}' V_{cveff} \right) + \frac{2}{3} V_{gsteff} \left(A_{bulk}' V_{cveff} \right)^2 - \frac{2}{15} \left(A_{bulk}' V_{cveff} \right)^3 \right)$$

$$Q_d = -\frac{W_{active} L_{active} C_{ox}}{2\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} \right)^2} \left(V_{gsteffcv}^3 - \frac{5}{3} V_{gsteffc}^2 \left(A_{bulk}' V_{cveff} \right) + V_{gsteff^{cv}} \left(A_{bulk}' V_{cveff} \right)^2 - \frac{1}{5} \left(A_{bulk}' V_{cveff} \right)^3 \right)$$

B.2.3.3 0/100 Charge Partition

$$Q_s = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteffcv}}{2} + \frac{A_{bulk}' V_{cveff}}{4} - \frac{\left(A_{bulk}' V_{cveff} \right)^2}{24\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

$$Q_d = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteffcv}}{2} - \frac{3A_{bulk}' V_{cveff}}{4} + \frac{\left(A_{bulk}' V_{cveff} \right)^2}{8\left(V_{gsteffcv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

(3) **capMod = 3 (Charge-Thickness Model)**

capMod = 3 also uses the bias-independent V_{th} to calculate V_{fb} as in capMod = 1 and 2.

$$vfb = V_{th} - \Phi_s - K_{1ox}\sqrt{\Phi_s - V_{bseff}}$$

For the finite charge thickness (X_{DC}) formulations, refer to Chapter 4.

$$Q_{acc} = WLC_{oxeff} \cdot V_{gbacc}$$

$$V_{gbacc} = \frac{1}{2} \cdot \left[V_0 + \sqrt{V_0^2 + 4d_3 V_{fb}} \right]$$

$$V_0 = V_{fb} + V_{bseff} - V_{gs} - d_3$$

$$V_{FBeff} = vfb - 0.5\left\{ V_3 + \sqrt{V_3^2 + 4d_3 vfb} \right\} \quad where \quad V_3 = vfb - V_{gb} - d_3; \quad d_3 = 0.02$$

$$C_{oxeff} = \frac{C_{ox} C_{cen}}{C_{ox} + C_{cen}}$$

$$C_{cen} = \varepsilon_{si} / X_{DC}$$

$$\Phi_d = \Phi_s - 2\Phi_B = n_t \ln\left(\frac{V_{gsteffCV}\cdot(V_{gsteffCV} + 2K_{1ox}\sqrt{2\Phi_B}}{moin\cdot K_{1ox}{}^2 n_t}\right)$$

$$Q_{sub0} = -WLC_{oxeff}\cdot\frac{K_{1ox}{}^2}{2}\cdot\left[-1+\sqrt{1+\frac{4(V_{gs}-V_{FBeff}-V_{bseffs}-V_{gsteffcv})}{K_{1ox}{}^2}}\right]$$

$$V_{cveff} = V_{dsat} - \frac{1}{2}\cdot\left(V_1 + \sqrt{V_1^2 + 4d_3 V_{dsat}}\right)$$

$$V_1 = V_{dsat} - V_{ds} - d_3$$

$$V_{dsat} = \frac{V_{gsteff,cv} - j_d}{A_{bulk}'}$$

$$Q_{inv} = -WLC_{oxeff}\cdot\left[V_{gsteffcv} - j_d - \frac{1}{2}A_{bulk}'V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{12\cdot\left(V_{gsteffcv} - j_d - A_{bulk}'V_{cveff}/2\right)}\right]$$

$$dQ_{sub} = WLC_{oxeff} \cdot \left[\frac{1 - A_{bulk}'}{2} V_{cveff} - \frac{(1 - A_{bulk}') \cdot A_{bulk}' V_{cveff}^2}{12 \cdot \left(V_{gsteff,cv} - j_d - A_{bulk}' V_{cveff} / 2 \right)} \right]$$

(i) 50/50 Charge Partition

$$Q_S = Q_D = \frac{1}{2} Q_{inv} = -\frac{WLC_{oxeff}}{2} \left[V_{gsteff,cv} - j_d - \frac{1}{2} A_{bulk}' V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{12 \cdot \left(V_{gsteff,cv} - j_d - A_{bulk}' V_{cveff} / 2 \right)} \right]$$

(ii) 40/60 Charge Partition

$$Q_S = -\frac{WLC_{oxeff}}{2\left(V_{gsteff,cv} - j_d - A_{bulk}' V_{cveff} / 2 \right)^2} \left[(V_{gsteff,cv} - j_d)^3 - \frac{4}{3}(V_{gsteff,cv} - j_d)^2 A_{bulk}' V_{cveff} + \frac{2}{3}(V_{gsteff,cv} - j_d)(A_{bulk}' V_{cveff})^2 - \frac{2}{15}(A_{bulk}' V_{cveff})^3 \right]$$

$$Q_D = -\frac{WLC_{oxeff}}{2\left(V_{gsteff,cv} - j_d - A_{bulk}' V_{cveff} / 2 \right)^2} \left[(V_{gsteff,cv} - j_d)^3 - \frac{5}{3}(V_{gsteff,cv} - j_d)^2 A_{bulk}' V_{cveff} + (V_{gsteff,cv} - j_d)(A_{bulk}' V_{cveff})^2 - \frac{1}{5}(A_{bulk}' V_{cveff})^3 \right]$$

(iii) 0/100 Charge Partition

$$Q_S = -\frac{WLC_{oxeff}}{2} \cdot \left[V_{gsteff,cv} - j_d + \frac{1}{2} A_{bulk}' V_{cveff} - \frac{A_{bulk}'^2 V_{cveff}^2}{12 \cdot \left(V_{gsteff,cv} - j_d - A_{bulk}' V_{cveff} / 2 \right)} \right]$$

$$Q_D = -\frac{WLC_{oxeff}}{2}\cdot\left[V_{gsteff,cv} - j_d - \frac{3}{2}A_{bulk}'V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{4\cdot\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{dveff}/2\right)}\right]$$

APPENDIX C: References

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APPENDIX D: Model Parameter Binning

Below is the information on parameter binning regarding which model parameters can or cannot be binned. All those parameters which can be binned follow this implementation:

$$P = P_0 + \frac{P_L}{L_{eff}} + \frac{P_W}{W_{eff}} + \frac{P_P}{L_{eff} \times W_{eff}}$$

For example, for the parameter k1: P_0 = k1, P_L = lk1, P_W = wk1, P_P = pk1. binUnit is a bining unit selector. If binUnit = 1, the units of L_{eff} and W_{eff} used in the binning equation above have the units of microns; therwise in meters.

For example, for a device with L_{eff} = 0.5μm and W_{eff} = 10μm. If binUnit = 1, the parameter values for *vsat* are 1e5, 1e4, 2e4, and 3e4 for *vsat*, *lvsat*, *wvsat*, and *pvsat*, respectively. Therefore, the effective value of *vsat* for this device is

vsat = 1e5 + 1e4/0.5 + 2e4/10 + 3e4/(0.5*10) = 1.28e5

To get the same effective value of *vsat* for binUnit = 0, the values of *vsat*, *lvsat*, *wvsat*, and *pvsat* would be 1e5, 1e-2, 2e-2, 3e-8, respectively. Thus,

vsat = 1e5 + 1e-2/0.5e6 + 2e-2/10e-6 + 3e-8/(0.5e-6 * 10e-6) = 1.28e5

D.1 Model Control Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
None	level	The model selector	NO
None	version	Model version selector	NO
None	binUnit	Bining unit selector	NO
None	param-Chk	Parameter value check	NO
mobMod	mobMod	Mobility model selector	NO
capMod	capMod	Flag for the short channel capacitance model	NO
nqsMod	nqsMod	Flag for NQS model	NO
noiMod	noiMod	Flag for Noise model	NO

D.2 DC Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Vth0	vth0	Threshold voltage @V_{bs}=0 for Large L.	YES
VFB	vfb	Flat band voltage	YES
K1	k1	First order body effect coeffi-cient	YES
K2	k2	Second order body effect coef-ficient	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
K3	k3	Narrow width coefficient	YES
K3b	k3b	Body effect coefficient of k3	YES
W0	w0	Narrow width parameter	YES
Nlx	nlx	Lateral non-uniform doping parameter	YES
Dvt0	dvt0	first coefficient of short-channel effect on Vth	YES
Dvt1	dvt1	Second coefficient of short-channel effect on Vth	YES
Dvt2	dvt2	Body-bias coefficient of short-channel effect on Vth	YES
Dvt0w	dvt0w	First coefficient of narrow width effect on Vth for small channel length	YES
Dvt1w	dvtw1	Second coefficient of narrow width effect on Vth for small channel length	YES
Dvt2w	dvt2w	Body-bias coefficient of narrow width effect for small channel length	YES
$\mu 0$	u0	Mobility at Temp = Tnom NMOSFET PMOSFET	YES
Ua	ua	First-order mobility degradation coefficient	YES
Ub	ub	Second-order mobility degradation coefficient	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Uc	uc	Body-effect of mobility degradation coefficient	YES
vsat	vsat	Saturation velocity at Temp = Tnom	YES
A0	a0	Bulk charge effect coefficient for channel length	YES
Ags	ags	gate bias coefficient of Abulk	YES
B0	b0	Bulk charge effect coefficient for channel width	YES
B1	b1	Bulk charge effect width offset	YES
Keta	keta	Body-bias coefficient of bulk charge effect	YES
A1	a1	First non0saturation effect parameter	YES
A2	a2	Second non-saturation factor	YES
Rdsw	rdsw	Parasitic resistance per unit width	YES
Prwb	prwb	Body effect coefficient of Rdsw	YES
Prwg	prwg	Gate bias effect coefficient of Rdsw	YES
Wr	wr	Width Offset from Weff for Rds calculation	YES
Wint	wint	Width offset fitting parameter from I-V without bias	NO
Lint	lint	Length offset fitting parameter from I-V without bias	NO

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
dWg	dwg	Coefficient of Weff's gate dependence	YES
dWb	dwb	Coefficient of Weff's substrate body bias dependence	YES
Voff	voff	Offset voltage in the subthreshold region for large W and L	YES
Nfactor	nfactor	Subthreshold swing factor	YES
Eta0	eta0	DIBL coefficient in subthreshold region	YES
Etab	etab	Body-bias coefficient for the subthreshold DIBL effect	YES
Dsub	dsub	DIBL coefficient exponent in subthreshold region	YES
Cit	cit	Interface trap capacitance	YES
Cdsc	cdsc	Drain/Source to channel coupling capacitance	YES
Cdscb	cdscb	Body-bias sensitivity of Cdsc	YES
Cdscd	cdscd	Drain-bias sensitivity of Cdsc	YES
Pclm	pclm	Channel length modulation parameter	YES
Pdiblc1	pdiblc1	First output resistance DIBL effect correction parameter	YES
Pdiblc2	pdiblc2	Second output resistance DIBL effect correction parameter	YES
Pdiblcb	pdiblcb	Body effect coefficient of DIBL correction parameters	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Drout	drout	L dependence coefficient of the DIBL correction parameter in Rout	YES
Pscbe1	pscbe1	First substrate current body-effect parameter	YES
Pscbe2	pscbe2	Second substrate current body-effect parameter	YES
Pvag	pvag	Gate dependence of Early voltage	YES
δ	delta	Effective Vds parameter	YES
Ngate	ngate	poly gate doping concentration	YES
$\alpha 0$	alpha0	The first parameter of impact ionization current	YES
$\alpha 1$	alpha1	Isub parameter for length scaling	YES
$\beta 0$	beta0	The second parameter of impact ionization current	YES
Rsh	rsh	Source drain sheet resistance in ohm per square	NO
Js0	js	Source drain junction saturation current per unit area	NO
ijth	ijth	Diode limiting current	NO

D.3 AC and Capacitance Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Xpart	xpart	Charge partitioning rate flag	NO
CGS0	cgso	Non LDD region source-gate overlap capacitance per channel length	NO
CGD0	cgdo	Non LDD region drain-gate overlap capacitance per channel length	NO
CGB0	cgbo	Gate bulk overlap capaci-tance per unit channel length	NO
Cj	cj	Bottom junction per unit area	NO
Mj	mj	Bottom junction capacitance grating coefficient	NO
Mjsw	mjsw	Source/Drain side junction capacitance grading coeffi-cient	NO
Cjsw	cjsw	Source/Drain side junction capacitance per unit area	NO
Pb	pb	Bottom built-in potential	NO
Pbsw	pbsw	Source/Drain side junction built-in potential	NO
CGS1	cgs1	Light doped source-gate region overlap capacitance	YES
CGD1	cgd1	Light doped drain-gate region overlap capacitance	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
CKAPPA	ckappa	Coefficient for lightly doped region overlap capacitance Fringing field capacitance	YES
Cf	cf	fringing field capacitance	YES
CLC	clc	Constant term for the short channel model	YES
CLE	cle	Exponential term for the short channel model	YES
DLC	dlc	Length offset fitting parame-ter from C-V	YES
DWC	dwc	Width offset fitting parameter from C-V	YES
Vfbcv	vfbcv	Flat-band voltage parameter (for capMod = 0 only)	YES
noff	noff	CV parameter in Vgsteff,CV for weak to strong inversion	YES
voffcv	voffcv	CV parameter in Vgsteff,CV for weak to strong inversion	YES
acde	acde	Exponential coefficient for charge thickness in capMod=3 for accumulation and deple-tion regions	YES
moin	moin	Coefficient for the gate-bias dependent surface potential	YES

D.4 NQS Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Elm	elm	Elmore constant of the channel	YES

D.5 dW and dL Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Wl	wl	Coefficient of length dependence for width offset	NO
Wln	wln	Power of length dependence of width offset	NO
Ww	ww	Coefficient of width dependence for width offset	NO
Wwn	wwn	Power of width dependence of width offset	NO
Wwl	wwl	Coefficient of length and width cross term for width offset	NO
Ll	ll	Coefficient of length dependence for length offset	NO
Lln	lln	Power of length dependence for length offset	NO

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Lw	lw	Coefficient of width dependence for length offset	NO
Lwn	lwn	Power of width dependence for length offset	NO
Lwl	lwl	Coefficient of length and width cross term for length offset	NO
Llc	Llc	Coefficient of length dependence for CV channel length offset	NO
Lwc	Lwc	Coefficient of width dependence for CV channel length offset	NO
Lwlc	Lwlc	Coefficient of length and width-dependence for CV channel length offset	NO
Wlc	Wlc	Coefficient of length dependence for CV channel width offset	NO
Wwc	Wwc	Coefficient of widthdependence for CV channel width offset	NO
Wwlc	Wwlc	Coefficient of length and width-dependence for CV channel width offset	NO

D.6 Temperature Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Tnom	tnom	Temperature at which parameters are extracted	NO
μte	ute	Mobility temperature exponent	YES
Kt1	kt1	Temperature coefficient for threshold voltage	YES
Kt1l	kt1l	Channel length dependence of the temperature coefficient for threshold voltage	YES
Kt2	kt2	Body-bias coefficient of Vth temperature effect	YES
Ua1	ua1	Temperature coefficient for Ua	YES
Ub1	ub1	Temperature coefficient for Ub	YES
Uc1	uc1	Temperature coefficient for Uc	YES
At	at	Temperature coefficient for saturation velocity	YES
Prt	prt	Temperature coefficient for Rdsw	YES
nj	nj	Emission coefficient	YES
XTI	xti	Junction current temperature exponent coefficient	YES

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
tpb	tpb	Temperature coefficient of Pb	NO
tpbsw	tpbsw	Temperature coefficient of Pbsw	NO
tpbswg	tpbswg	Temperature coefficient of Pbswg	NO
tcj	tcj	Temperature coefficient of Cj	NO
tcjsw	tcjsw	Temperature coefficient of Cjsw	NO
tcjswg	tcjswg	Temperature coefficient of Cjswg	NO

D.7 Flicker Noise Model Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Noia	noia	Noise parameter A	NO
Noib	noib	Noise parameter B	NO
Noic	noic	Noise parameter C	NO
Em	em	Saturation field	NO
Af	af	Flicker noise exponent	NO

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Ef	ef	Flicker noise frequency exponent	NO
Kf	kf	Flicker noise parameter	NO

D.8 Process Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Tox	tox	Gate oxide thickness	NO
Toxm	toxm	Tox at which parameters are extracted	NO
Xj	xj	Junction Depth	YES
$\gamma 1$	gamma1	Body-effect coefficient near the surface	YES
$\gamma 2$	gamma2	Body-effect coefficient in the bulk	YES
Nch	nch	Channel doping concentration	YES
Nsub	nsub	Substrate doping concentration	YES
Vbx	vbx	Vbs at which the depletion region width equals xt	YES
Vbm	vbm	Maximum applied body bias in Vth calculation	YES
Xt	xt	Doping depth	YES

D.9 Geometry Range Parameters

Symbols used in equation	Symbols used in SPICE	Description	Can Be Binned?
Lmin	lmin	Minimum channel length	NO
Lmax	lmax	Maximum channel length	NO
Wmin	wmin	Minimum channel width	NO
Wmax	wmax	Maximum channel width	NO
binUnit	binUnit	Binning unit selector	NO