OLABISI ONABANJO UNIVERSITY, AGO-IWOYE
FACULTY OF SCIENCE
DEPARTMENT OF MATHEMATICAL SCIENCES
B.Sc. COMPUTER SCIENCE DEGREE EXAMINATIONS (400 LEVEL)
2018/2019 HARMATTAN SEMESTER EXAMINATIONS

COURSE CODE/TITLE: CMP 421: COMPUTER ARCHITECTURE II
INSTRUCTIONS: ATTEMPT ANY FOUR (4) QUESTIONS
TIMEALLOWED: 2.00 HOURS

1a. The memory system of a typical computer system is an organized hierarchy of storage devices. Discuss. Use relevant diagram for your illustration. (13 marks)

b. Determine the Average Memory Access Time (t_{av}) of a memory hierarchy that consists of three levels. Define the parameters involved. (4 ½ marks)

2a. Show the memory organization (1024 bytes) of a computer with four 128 x 8 RAM Chips and 512 x8 ROM Chips. (6 marks)

b. How many address lines and data limes are required to access memory of question of 4a? (4 marks)

c. Why page-table is required in a virtual memory system. Explain different ways of organizing a page-table. (7 ½)

3a. What is the average access time of a system having three levels of memory, a cache memory, a semiconductor main memory, and a magnetic disk secondary memory, if the access times of the memories are 20 ns, 100 ns, and 1 ms, respectively. The cache hit ratio is 90% and the main memory hit ratio is 95%. (5 ½ marks)

b. A computer system has an MM consisting of 16 MB 32-bit words. It also has an 8 KB cache. Assume that the computer uses a byte-addressable mechanism. Determine the number of bits in each field of the address in each of the following organizations:
(i). Direct mapping with block size of one word
(ii). Direct mapping with a block size of eight words
(iii). Associative mapping with a block size of eight words
(iv). Set-associative mapping with a set size of four block and a block size of one word. (12 marks)

4a. Briefly explain the term "cache memory". (5 ½ marks)

b. Consider the case of a main memory consisting of 4K blocks, a cache memory consisting of 128 blocks, and a block size of 16 words. According to the direct-mapping technique the MMU interprets the address issued by the processor by dividing the address into three fields: Word field, Block field, and Tag field.
(i). Draw a diagram to show the Direct Mapping of main memory blocks to cache blocks.
(ii). Give the formula for deriving the lengths, in bits, of each of the fields (Word, Block, Tag) and the number of bits in the main memory address.
(iii). Compute the four parameters derived in 2b(ii). (12 marks)

5. Explain how data transfer from disk to memory is conducted under each of the following I/O schemes: (i). DMA, (ii). Shared I/O, and (iii). Memory-mapped I/O. Show the steps taken in each case. Also use relevant diagram for your illustration. (17 ½ marks)

6a. Explain the following: (i). The use of time out mechanism in handshaking data transfer scheme. (ii). Synchronous buses (iii). Asynchronous buses (10 marks)

b. A virtual memory system has an address space of 8k words, memory space of 4k words and page and block size of 1k words. The following page reference changes occur during a given time interval. 4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7. Determine the four pages that are resident in main memory after each Page Reference change if the replacement algorithm used is (i) FIFO (ii) LRU (7 ½ marks)