PWM controller

23.1 Function overview

PWM is a method of digitally encoding the level of an analog signal. Through the use of a high-resolution counter, the duty cycle of the square wave is modulated to encode the level of a specific analog signal. The PWM signal is still digital because at any given moment, the full-scale direct DC power supply is either fully present (ON) or completely absent (OFF). A voltage or current source is a repetitive pulse of on (ON) or off (OFF).

The impulse sequence is added to the simulated load. When it is on, it means that the DC power supply is added to the load, and when it is off, it means that the power supply is disconnected. Any analog value can be encoded using PWM as long as the bandwidth is sufficient.

23.2 Main Features

- Support 2-channel input signal capture function (CH0 and CH4 channels)
- The input signal capture function supports interrupt interactive mode and DMA transfer mode; DMA mode supports word-by-word operation
- Support 5-channel PWM signal generation
- 5-channel PWM signal generation supports one-shot generation mode and auto-load mode
- Support 5-channel braking function
- PWM output frequency range: 3Hz~160kHz
- Maximum accuracy of duty cycle: 1/256, width of counter inserted into dead zone: 8bit
- Support channel 0 and channel 1 two channels synchronization, also channel 2 and channel 3
- Support complementary and non-complementary modes of pairs of channel 0 and channel 1, also of channel 2 and channel 3
- Support 5-channel synchronization function

23.3 Functional Description

23.3.1 Input Signal Capture

The PWM controller supports the signal capture function of two channels, and the capture of channel 0 can be activated by setting Bit24 of the PWM_CR register function, the capture function of channel 4 can be activated by setting Bit1 of the PWM_CH4CAPDAT register. The level of the captured signal can also be set whether to flip the function. After the channel captures the corresponding signal, the capture number is updated to the corresponding capture register PWM_CAPDAT (for CH0) and PWM_ CH4CAPDAT (CH4 capture number).

23.3.2 DMA Transfer Capture Number

After the capture function is enabled on channel 0 or channel 4, the count of the capture register can be quickly transferred to the memory through the DMA channel, speeding up user process.

23.3.3 Support for one-shot and automount modes

Each of the five output channels of the PWM controller supports one-shot output mode and auto-reload mode. In single load mode, the channel outputs a specified cycle. After the specified period of waveforms, the PWM wave will no longer be output; in the automatic loading mode, after the channel outputs the specified period of waveforms, it will automatically reload the period number, thereby continuing to generate PWM waves.

23.3.4 Multiple Output Modes

The PWM controller supports independent output mode, that is, each channel outputs independently without interfering with each other; it supports dual-channel synchronous mode, that is, one channel's output is exactly the same as the output of another channel; supports five-channel synchronous mode, the output of channel 1 to channel 4 is exactly the same as the output of channel 0; support dual-channel complementary output, that is, the waveform output by one channel is completely opposite to the waveform output by the other channel; support complementary mode commonly used dead zone settings, the dead zone length can be set up to 256 clock cycles; support brake mode, when the brake port detects the specified voltage after leveling, the output channel will output the brake level that has been set. A variety of output modes are flexible and configurable to meet various application scenarios related to PWM by users.

23.4 Register Description

23.4.1 PWM Register List

Table 185 PWM register list

Offset	Name	Short name	Access	Info
0X0000	Clock frequency division register_01	PWM_CLKDIV01	RW	Set the clock frequency divider of channel 0 and channel 1
0X0004	Clock frequency division register_23	PWM_CLKDIV23	RW	Set the clock frequency divider of channel 2 and channel 3
0X0008	Control register	PWM_CR	RW	Configure or control some configurable items

0X000C	Period register	PWM_PERIOD	RW	Set the period of channel 0 to channel 4
0X0010	Cycle count register	PWM_PNUM	RW	Set number of cycles of channel 0 to channel 4
0X0014	Compare register	PWM_CMPDAT	RW	Set the comparison value of channel 0 to channel 4
0X0018	Deadband control register	PWM_DTCR	RW	Used to configure or control the dead zone related configurable
0X001C	Interrupt control register	PWM_IE	RW	Used to control related interrupts
0X0020	Interrupt status register	PWM_IF	RW	Used to query the status of related interrupts
0X0024	Ch0 Capture register	PWM_CH0CAPDAT	RW	Used to store CH0 counter for capture edge and falling edge
0X0028	Brake control register	PWM_BKCR	RW	Used to control the brake mode
0X002C	Clock frequency division register_4	PWM_CH4CR1	RW	Set the clock frequency divider of channel 4
0X0030	Ch4 Control register_2	PWM_CH4CR2	RW	Set the relevant configuration items of channel 4
0X0034	Ch4 capture register	PWM_CH4CAPDAT	RO	Used to capture and count to channel 4
0X0038	Ch4 Control register_3	PWM_CH4CR3	RW	Set the relevant configuration items of channel 4

(Note : some register names are changed to correspond to its HAL names by dde)

23.4.2 Clock Divider Register_01

Table 186 PWM clock frequency division register_01

bit	access	Instructions	reset value
[31:16]	RW	CLKDIV1 CH1 frequency division counter The frequency division number is determined by the counter value Note: The frequency division range is (0~65535), if no frequency division is required, enter 0 or 1.	0
[15:0]	RW	CLKDIV0 CH0 frequency division counter Same as CH1	0

23.4.3 Clock frequency division register_23

Table 187 PWM clock frequency division register_23

bit	access	Instructions	reset value
[31:16]	RW	CLKDIV3 CH3 frequency division counter Same as CH1	0
[15:0]	RW	CLKDIV2 CH2 frequency division counter Same as CH1	0

23.4.4 Control Register

Table 188 PWM Control Register

bit	access	Instructions	reset value
[31:27]	RW	CNTEN Counter count enable 0: stop counting 1: start counting Note: Each bit controls each channel separately, CH4-CH0 are controlled sequentially from high to low	5'b0
[26]	–	reserve	1'b0
[25]	RW	CAPINV Capture reverse enable flag 0: capture mode input signal reverse disabled 1: The reverse of the input signal in capture mode is enabled and the input signal is reversed	1'b0
[24]	RW	CPEN Capture function enable flag 0: The capture function of CH0 is disabled, and the values of RCAPDAT and FCAPDAT will not be updated;	1'b0

		1: CH0 capture function is enabled, capture and latch the PWM counter, respectively stored in RCAPDAT (rising latch on edge) and FCAPDAT (latch on falling edge)	
[23:22]	RW	CNTTYPE3 CH3 counter counting method 2’b00: Edge-aligned mode (the counter is incremented, only for capture mode) 2’b01: Edge-aligned mode (the counter is decrementing, only for PWM mode) 2’b10: Center-aligned mode (for PWM mode only) Note: In PWM mode, when the counter is set to edge-aligned mode, it is necessary to set the counting mode as decrement	2'b0
[21:20]	RW	CNTTYPE2 CH2 counter counting mode Same as CH3	2'b0
[19:18]	RW	CNTTYPE1 CH1 counter counting mode Same as CH3	2'b0
[17:16]	RW	CNTTYPE0 CH0 counter counting mode Same as CH3	2'b0
[15:14]	RW	TWOSYNCEN 2-channel synchronous mode enable signal 0: 2-channel synchronization not allowed 1: allow 2-channel synchronization, PWM_CH0 and PWM_CH1 have the same phase, and the phase is determined by PWM_CH0; PWM_CH2 has the same phase as PWM_CH3, and the phase is determined by PWM_CH2 15th bit control CH3 and CH2, 14th bit control CH1 and CH0	2'b0
[13]	–	reserve	1'b0
[12]	RW		1'b0

		POEN PWM pin output enable bit 0: PWM pin is set to output state 1: PWM pin are tri-stated Note: only for CH0	
[11:8]	RW	CNT MODE PWM Generation Cycle Mode 0: one-shot mode 1: Autoload mode Note: During the change of CNTMODE, PWM_CMPDAT is reset to zero; Each bit controls each channel separately, from high to low to control CH3-CH0	4'h0
[7]	–	reserve	1'b0
[6]	RW	ALLSYNCEN All channel synchronous mode enable signal 0: Synchronization of all channels is disabled 1: Allow synchronization of all channels, PWM_CH0, PWM_CH1, PWM_CH2 and PWM_CH3 have the same phase, and the phase is determined by PWM_CH0	1'b0
[5:2]	RW	PINV PWM output signal polarity enable 0: PWM output polarity inversion disabled 1: PWM output polarity inversion enable Note: Each bit controls each channel separately, from high to low to control CH3-CH0	4'h0
[1:0]	RW	OUTMODE output mode 0: Every two channels non-complementary mode 1: Every two channels form a complementary pattern BIT1 controls CH2 and CH3 BIT0 controls CH0 and CH1	2’b0

23.4.5 Period Register

Table 189 PWM Period Register

bit	access	Instructions	reset value
[31:24]	RW	PERIOD3 CH3 period register value (note: period cannot be greater than 255) “Edge-aligned mode” (counter counting method is decrementing): ➢PERIOD register value, the period value is (PERIOD + 1) ➢Duty cycle=(CMP+1)/(PERIOD+1) ➢CMP>=PERIOD: PWM output is fixed at high ➢CMP<PERIOD: PWM low level width is (PERIOD-CMP), high level width is (CMP+1) ➢CMP=0: PWM low level width is PERIOD, high level width is 1; "Middle Alignment Mode": ➢PERIOD register value: period is 2*(PERIOD+1) ➢Duty cycle=(2*CMP+1)/(2*(PERIOD+1)) ➢CMP>PERIOD: PWM keeps high ➢CMP<=PERIOD: PWM low level=2*(PERIOD-CMP)+1, High level = (2*CMP) +1 ➢CMP=0: PWM low level width is 2*PERIOD+1, high level width is 1. Note: In "middle-aligned mode", the number of cycles should not be 255. No matter which alignment mode is selected, the channel period is determined by the frequency divider (N) and the number of periods (P). That is: the input clock is 40MHz, the clock frequency f_div after frequency division is: f_div = 40MHz/N, where N is frequency divider (16bit). The output frequency f_output is: f_output = f_div / P, where P is the number of cycles. Note: In PWM mode, when the counter is set to edge-aligned mode, it is necessary to set the counting mode as decrement way.	8'h0
[23:16]	RW	PERIOD2 Same as PERIOD3	8’h0
[15:8]	RW	PERIOD1 Same as PERIOD3	8’h0
[7:0]	RW	PERIOD0	8’h0

		Same as PERIOD3	

23.4.6 Cycle Count Register

Table 190 PWM Cycle Number Register

bit	access	Instructions	reset value
[31:24]	RW	PNUM3 PWM3 generation cycle number Set the number of PWM3 cycles PNUM3, when the PWM generates PNUM3 PWM signals, stop generating output, trigger the interrupt and set the interrupt status word at the same time	8'h0
[23:16]	RW	PNUM2 Same as PNUM3	8’h0
[15:8]	RW	PNUM1 Same as PNUM3	8’h0
[7:0]	RW	PNUM0 Same as PNUM3	8’h0

23.4.7 Compare Register

Table 191 PWM Compare Register

bit	access	Instructions	reset value
[31:24]	RW	CMP3 PWM3 compare register value “Edge-aligned mode” (counter counting method is decrementing): ➢PERIOD register value, the period value is (PERIOD + 1) ➢Duty cycle=(CMP+1)/(PERIOD+1) ➢CMP>=PERIOD: PWM output is fixed at high ➢CMP<PERIOD: PWM low level width is (PERIOD-CMP), high level width is (CMP+1) ➢CMP=0: PWM low level width is PERIOD, high level width is 1; "Middle Alignment Mode": ➢PERIOD register value: period is 2*(PERIOD+1) ➢Duty cycle=(2*CMP+1)/(2*(PERIOD+1)) ➢CMP>PERIOD: PWM keeps high	8'h0

		➢CMP<=PERIOD: PWM low level=2*(PERIOD-CMP)+1, High level = (2*CMP) +1 ➢CMP=0: PWM low level width is 2*PERIOD+1, high level width is 1. Note: In "middle-aligned mode", the number of cycles should not be 255. No matter which alignment mode is selected, the channel period is determined by the frequency divider (N) and the number of periods (P). That is: the input clock is 40MHz, the clock frequency f_div after frequency division is: f_div = 40MHz/N, where N is frequency divider (16bit). The output frequency f_output is: f_output = f_div / P, where P is the number of cycles. Note: In PWM mode, when the counter is set to edge-aligned mode, it is necessary to set the counting mode as decrement way.	
[23:16]	RW	CMP2 Same as CMP3	8'h0
[15:8]	RW	CMP1 Same as CMP3	8'h0
[7:0]	RW	CMP0 Same as CMP3	8'h0

23.4.8 Dead-time control register

Table 192 PWM dead-band control register

bit	access	Instructions
[31:22]	--	reserved
[21]	RW	DTEN23 Channel 2 and channel 3 the dead zone insertion enable flag. The effective signal of dead zone insertion is valid only after the complementary mode of the channels is turned on. 0: Insertion of dead zone disabled 1: Insertion of dead zone enabled
[20]	RW	DTEN01 Channel 0 and channel 1 the dead zone insertion enable flag. Same as DTEN23
[19:18]	--	reserved
[17:16]	RW	

		DTDIV Dead-band clock frequency division control 2’b00: dead zone clock is equal to reference clock (40MHz) 2’b01: The dead zone clock is equal to the reference clock (40MHz) divided by two 2’b10: The dead zone clock is equal to the reference clock (40MHz) divided by four 2’b11: The dead zone clock is equal to the reference clock (40MHz) divided by eight
[15:8]	RW	DTCNT23 Dead-band interval for channel 3 and channel 2 8bit determines the dead zone interval value, and the dead zone clock is determined by DTDIV
[7:0]	RW	DTCNT01 Dead-band interval for channel 1 and channel 0 8bit determines the dead zone interval value, and the dead zone clock is determined by DTDIV

23.4.9 Interrupt Control Register

Table 193 PWM Interrupt Control Register

bit	access	Instructions	reset value
[31:8]	–	reserved	24'h0
[7]	RW	DMA_request_EN DMA_request enable 0: DMA_request disabled 1: DMA_request enabled	1'b0
[6]	RW	FLIEN Falling edge buffer interrupt enable bit 0: Falling edge buffer interrupt is disabled 1: Falling edge buffer interrupt is enabled Note: For CH0	1'b0
[5]	RW	RLIEN Rising edge buffer interrupt enable bit 0: rising buffer interrupt is disabled 1: Rising edge buffer interrupt is enabled NOTE: For CH0	1'b0

[4:0]	RW	PIEN PWM Period Interrupt Enable Bit 0: Periodic interrupt is disabled 1: Periodic interrupt is enabled Note: When the counter counts to 0 and the number of PWM cycles meets PWM_PNUM, an interrupt is triggered.	5'b0

23.4.10 Interrupt Status Register

Table 194 PWM Interrupt Status Register

bit	access	Instructions	reset value
[31:10]	–	reserved	22'h0
[9]	RW	OVERFL counter overflow flag 1’b0: capture mode, the counter does not overflow during the counter counting process 1’b1: capture mode, counter overflow during counter counting Note: When the user clears CFLIF or CRLIF, this bit will also be cleared at the same time	1'b0
[8]	RW	FLIFOV Falling edge delay interrupt flag overrun status 1’b0: When CFILF is 1, no falling edge delay interrupt will be generated 1’b1: When CFILF is 1, another falling edge delayed interrupt occurred Note: When the user clears CFILF, this bit is also cleared at the same time	1'b0
[7]	RW	RLIFOV Rising edge delay interrupt flags overrun status 1’b0: When CRILF is 1, no rising edge delay interrupt will be generated 1’b1: When CRILF is 1, another rising edge delay interrupt occurred Note: When the user clears CRILF, this bit is also cleared at the same time	1'b0
[6]	RW	CFLIF Capture falling edge interrupt flag 1’b0: No falling edge captured	1'b0

		1’b1: When a falling edge is captured, this bit is set to 1 Note: By writing 1, clear this flag; NOTE: For CH0	
[5]	RW	CRLIF Capture rising edge interrupt flag 1’b0: rising edge not captured 1’b1: When a rising edge is captured, this bit is set to 1 Note: By writing 1, clear this flag; NOTE: For CH0	1'b0
[4:0]	RW	PIF PWM Period Interrupt Flag When the PWM generates a PWM signal with a specified period, the flag is set to 1; write 1 by software to clear the flag Note: Each bit identifies each channel separately, and controls CH4-CH0 in sequence from high to low	5'b0

23.4.11 Channel 0 Capture Register

Table 195 PWM channel 0 capture register

bit	access	Instructions	reset value
[31:16]	RO	PWM_FCAPDAT CH0 capture falling edge register When there is a falling edge on the input signal, store the current counter value	16'h0
[15:0]	RO	PWM_RCAPDAT CH0 capture rising edge register When there is a rising edge on the input signal, store the current counter value	16'h0

23.4.12 Brake Control Register

Table 196 PWM brake control register

bit	access	Instructions	reset value
[31:16]	–	reserved	16'h0
[15:11]	RW		5'b0

		BRKCTL brake mode enable 0: brake mode disabled 1: brake mode active bits correspond to CH4, CH3, CH2, CH1 and CH0 respectively	
[10:8]	–	reserved	3'h0
[7:3]	RW	BKOD Brake Output Control Register 0: When the brake mode is triggered, the PWM output is low 1: When the brake mode is triggered, the PWM output is high Bits correspond to CH4, CH3, CH2, CH1 and CH0 respectively	5'b0
[2:0]	–	reserved	3'h0

23.4.13 Clock Divider Register_4

Table 197 PWM clock frequency division register_4

bit	access	Instructions	reset value
[31:16]	RW	CLKDIV4 CH4 frequency divider Note: The frequency division range is (0~65535), if no frequency division is required, enter 0 or 1.	16'h0
[15:8]	RW	PERIOD4 CH4 period register value (note: period cannot be greater than 255) "Edge-aligned mode (counter counting method is decrementing)": ➢PERIOD register value, the period value is (PERIOD + 1) ➢Duty cycle=(CMP+1)/(PERIOD+1) ➢CMP>=PERIOD: PWM output fixed bit high ➢CMP<PERIOD: PWM low level width is (PERIOD-CMP), high level width is (CMP+1) ➢CMP=0: PWM low level width is PERIOD, high level width is 1; "Middle Alignment Mode": ➢PERIOD register value: the period is 2*(PERIOD+1) ➢Duty cycle=(2*CMP+1)/(2*(PERIOD+1)) ➢CMP>PERIOD: PWM keeps high ➢CMP<=PERIOD: PWM low level=2*(PERIOD-CMP)+1, high level=(2*CMP)+1	8'h0

		➢CMP=0: PWM low level width is 2*PERIOD+1, high level width is 1. Note: In "middle-aligned mode", the number of cycles should not be 255. No matter which alignment mode is selected, the channel period is determined by the frequency division number (N) and the number of periods (P), That is: the input clock is 40MHz, the clock frequency f_div after frequency division is: f_div = 40MHz/N, where N is frequency divider (16bit). The output frequency f_output is: f_output = f_div / P, where P is the number of cycles. Note: In PWM mode, when the counter is set to edge-aligned mode, it is necessary to set the counting mode as decrement way.	
[7:0]	RW	PNUM4 CH4 generation cycle number Set the number of PWM4 cycles to PNUM4. When the PWM generates PNUM4 PWM signals, stop generating outputs, triggering an interrupt and setting the interrupt status word.	8'h0

23.4.14 Channel 4 Control Register_2

Table 198 PWM Channel 4 Control Register_2

bit	access	Instructions	reset value
[31:16]	–	reserved	16'h0
[15:8]	RW	CMP4 CH4 compare register value "Edge-aligned mode (counter counting method is decrementing)": ➢PERIOD register value, the period value is (PERIOD + 1) ➢Duty cycle=(CMP+1)/(PERIOD+1) ➢CMP>=PERIOD: PWM output fixed bit high ➢CMP<PERIOD: PWM low level width is (PERIOD-CMP), high level width is (CMP+1) ➢CMP=0: PWM low level width is PERIOD, high level width is 1; "Middle Alignment Mode": ➢PERIOD register value: the period is 2*(PERIOD+1) ➢Duty cycle=(2*CMP+1)/2*(PERIOD+1) ➢CMP>PERIOD: PWM keeps high ➢CMP<=PERIOD: PWM low level=2*(PERIOD-CMP)+1, high	8 'h0

		level=(2*CMP)+1 ➢CMP=0: PWM low level width is 2*PERIOD+1, high level width is 1. No matter which alignment mode is selected, the channel period is determined by the frequency division number (N) and the period number (P), namely: The input clock is 40MHz, the clock frequency f_div after frequency division is: f_div = 40MHz/N, where N is the frequency divider (16bit). The output frequency f_output is: f_output = f_div / P, where P is the number of cycles. Note: In PWM mode, when the counter is set to edge-aligned mode, it is necessary to set the counting mode as decrement way.	
[7:5]	–	reserved	3'h0
[4:3]	RW	 CNTTYPE4 CH4 counter counting mode 2’b00: Edge-aligned mode (the counter counting method is incremented, only for capture mode) 2’b01: Edge-aligned mode (the counter is decrementing, only for PWM mode) 2’b10: Center-aligned mode (for PWM mode only) Note: In PWM mode, when the counter is set to edge-aligned mode, it is necessary to set the counting mode as decrement way.	2'h0
[2]	–	reserved	1'h0
[1]	RW	 CNTMODE4 CH4 generation cycle mode 0: one-shot mode 1: Autoload mode Note: During the change of CNTMODE, PWM_CMPDAT is reset to zero	1'h0
[0]	RW	 PINV4 CH4 output signal polarity enable 0: PWM output polarity inversion disabled 1: PWM output polarity inversion enabled	1'h0

23.4.15 Channel 4 Capture Register

Table 199 PWM channel 4 capture register

bit	access	Instructions	reset value

[31:16]	RO	PWM_FCAP2DAT capture falling edge register When there is a falling edge on the input signal, store the current counter value	16'h0
[15:0]	RO	PWM_RCAP2DAT capture rising edge register When there is a rising edge on the input signal, store the current counter value	16'h0

23.4.16 Channel 4 Control Register_3

Table 200 PWM Channel 4 Control Register_3

bit	access	Instructions	reset value
[31:11]	–	reserved	21'h0
[10]	RW	DMA_request2_mask DMA_request2 enable 0: DMA_request2 disabled 1: DMA_request2 enabled Note: only for CH4	1'b0
[9]	RW	FLIEN2 Falling edge buffer interrupt enable bit 0: Falling edge buffer interrupt is disabled 1: Falling edge buffer interrupt is enabled Note: only for CH4	1'b0
[8]	RW	RLIEN2 Rising edge buffer interrupt enable bit 0: rising buffer interrupt is disabled 1: Rising edge buffer interrupt is enabled Note: only for CH4	1'b0
[7]	RW	OVERFL2 counter overflow flag 0: capture mode, the counter does not overflow during the counter counting process 1: capture mode, counter overflow during counter counting Note: When the user clears CFLIF or CRLIF, this bit will also be cleared at the same time Note: only for CH4	1'b0

[6]	RW	FLIFOV2 Falling edge delay interrupt flags overrun status 0: When CFILF is 1, no falling edge delay interrupt will be generated 1: When CFILF is 1, another falling edge delayed interrupt occurred Note: When the user clears CFILF, this bit is also cleared at the same time Note: only for CH4	1'b0
[5]	RW	RLIFOV2 Rising edge delay interrupt flags overrun status 0: When CRILF is 1, no rising edge delay interrupt will be generated 1: When CRILF is 1, another rising edge delay interrupt occurred Note: When the user clears CRILF, this bit is also cleared at the same time Note: only for CH4	1'b0
[4]	RW	CFLIF2 Capture falling edge interrupt flag 1’b0: No falling edge captured 1’b1: When a falling edge is captured, this bit is set to 1 Note: By writing 1, clear this flag Note: only for CH4	1'b0
[3]	RW	CRLIF2 Capture rising edge interrupt flag 0: rising edge not captured 1: When a rising edge is captured, this bit is set to 1 Note: By writing 1, this flag is cleared Note: only for CH4	1'b0
[2]	RW	POEN2 PWM pin output enable bit 0: PWM pin is set to output state 1: PWM pins are tri-stated Note: only for CH4	1'b0
[1]	RW	CPEN2 Capture function enable flag 0: The capture function of CH4 is disabled, and the values of RCAPDAT and FCAPDAT will not be updated; 1: The capture function of CH4 is enabled, capture and latch	1'b0

		the PWM counter, and store them in RCAPDAT (rising latch on edge) and FCAPDAT (latch on falling edge) Note: only for CH4	
[0]	RW	 CAPINV2 Capture reverse enable flag 0: capture mode input signal reverse disabled 1: The reverse of the input signal in capture mode is enabled, and the input signal is reversed Note: only for CH4	1'b0