Series Connection of Insulated Gate Bipolar Transistors (IGBTs)

Ruchira Withanage and Noel Shammas

***Abstract*—High-voltage switches required in present power electronics applications are realized by connecting existing devices in series. Unequal sharing of voltage across series-connected devices can be minimized by using active gate control techniques, snubber circuits, and active clamping circuits. The primary objectives of this paper are to discuss existing voltage-balancing techniques, to present a novel hybrid voltage-balancing technique, and to optimize the number of insulated gate bipolar transistors (IGBTs) in a series string in terms of power losses. The novel voltage-balancing technique can achieve good voltage balancing with a minimum number of components and minimum total losses (i.e., IGBT losses and balancing circuit losses). This technique was validated by both simulation and experimental work. The power loss of a high-voltage switch depends on the voltage-balancing circuit and the number of IGBTs in series and switching frequency. For a given application, the optimum number of IGBTs, in terms of power losses, depends on device characteristics and switching frequency.**

***Index Terms*—Active gate control, insulated gate bipolar transistors, optimum capacitance, voltage balancing.**

I. Introduction

ADVANCES in power semiconductor devices, power converter circuit topologies, and control techniques have resulted in the rapid growth of power electronics applications. High-power electronic applications require solid state switches that can handle high currents and high voltages. By connecting power semiconductor devices in parallel and/or series, high-power solid-state switches can be realized.

For high-voltage applications where the system operating voltage is higher than that for a single available device, several devices can be connected in series to provide the higher voltage rating required. In an example of such applications, the series-connected devices can be used in a two-level topology or multilevel topologies. Although high dv/dt of a series-connected two-level topology can cause insulation failures and common-mode voltages in motor drive applications [1], a two-level topology costs less, requires less circuit design and has less control complexity compared to multilevel circuit topologies [2]. The main problem with series connection of semiconductor devices is the unequal voltage distribution between them in both transient and steady-state operations. The unequal voltage sharing is mainly due to the spread of device dynamic and static parameters, gate-drive delays, and external circuit parameters. This voltage unbalance may exceed the individual device voltage rating and the subsequent failure of a device causes final failure of the entire series string of devices.

There are several methods for minimizing the voltage difference across individual devices in series string of IGBTs. Since the voltage difference is mainly due to device parameter spread and gate-drive delays, careful selection of power semiconductor devices which have low parameter spread and synchronizing gate-drive signals will minimize the voltage unbalance. In addition to this, passive snubber circuits, active gate control circuits, and voltage clamping circuits are also used to minimize voltage unbalance.

A. Passive Snubber Circuits

The use of a passive snubber is a widely used technique in series operation of power devices. A resistor–capacitor (*RC*) or resistor–capacitor-diode (RCD) circuit is used in parallel with the series element for transient sharing. Passive snubbers are simple to implement; they reduce the switching losses and can be used in robust applications. The use of large snubber capacitors minimizes the voltage unbalance but increases both snubber power loss and commutation time of the device. In addition, these components are large in size and costly. The switching characteristics of devices are slowed down, and therefore, their operating frequency has to be kept low. Chen *et al.* [3] used RCD snubbers for voltage balancing in series-connected IGBTs and described the design criteria for the RCD snubber in conjunction with the snubber inductance. The results show good voltage balancing and large commutation time.

B. Active Gate Control Circuits

In the active gate control techniques, gate charge is controlled by a control circuit according to the voltage unbalance, and ultimately, it will increase or decrease the rate of change of collector–emitter voltage. Consoli *et al.* [4] produced a method to balance the collector–emitter voltages in transient state. In this method, a positive gate pulse is injected by connecting a precharged capacitor to the fastest device to switch OFF. The main advantage of this method is the avoidance of using passive components but voltage balancing cannot always be guaranteed. In the method proposed by Gerster [5], a gate signal is adjusted to control the transient and steady-state voltage unbalances of

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series-connected IGBTs. The control circuit is complex in this method although devices switching times and power losses are not increased significantly. Raciti *et al.* [6] investigated a method where one device was kept as the reference (Master device) and the collector–emitter voltage of the others (slave devices) are controlled by referring to the master device voltage. This technique does not increase power losses significantly, and connections of more than two devices in series make voltage sensing circuit very complex and costly. In the method proposed by Palmer [7], all the devices connected in series are controlled according to the common reference during the transient state. The reference waveform is a designer choice and it does not depend on the device. The voltage sensing and control is not as complex as in [6] and the power loss of the devices depends on the rate of rise of the reference voltage. Weiwei *et al.* [8] used this technique to optimize the diode recovery at IGBT turn ON. In the method proposed by Hong *et al.* [9], collector–emitter voltage is controlled by applying a positive gate charge to the gate terminal if it is greater than the reference voltage. The gate control circuit is relatively simple compared to other active gate control methods mentioned earlier. The main problems with this technique are high-power loss and higher *dv/dt* during transient stage of the first device to switch OFF. A similar method was proposed by Kon *et al.* [10]. In order to avoid complex gate side circuits, Baek *et al.* [11] investigated a new simple voltage-balancing circuit, which mainly consists of a diode, resistors, and capacitors. Later this topology was optimized and extended for high-power devices by Abbate *et al.* [12]. This method is simple, but switching losses are high because of the clamping action.

In general, the active gate control techniques do not increase switching losses and commutation time significantly. The control circuits add more complexity to gate-driver circuit and require high-speed and high-sensitive devices. As the component count of the gate-drive circuit increases, the reliability of the control method is decreased. Active gate control techniques do not need bulky snubber circuits, but they do require small passive snubber to balance voltage during the IGBT current tail time.

C. Voltage Clamping Circuits

Active voltage clamping techniques clamp the collector–emitter voltage at a reference voltage level. These circuits are simple and easy to implement compared to the techniques mentioned earlier and no complex analog/digital circuits are needed. In the method proposed by Bruckmann *et al.* [13], the IGBT collector–emitter voltage is clamped by zener diode over voltage protection circuit. Saiz *et al.* [14] improved the zener diode clamping method [13], by introducing a capacitor and resistors.

The main drawback of this method is that it increases power loss in the first device to be clamped since it experiences both high current and high voltage until other devices switch OFF; therefore, efficiency of the application is reduced.

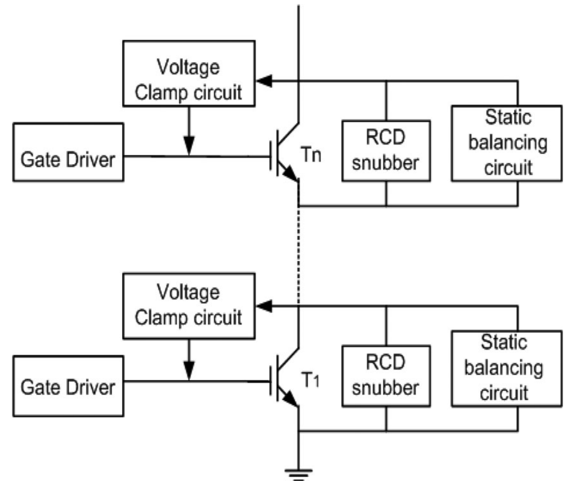

Fig. 1. Block diagram of active voltage clamping and passive snubber technique.

A reliable and robust voltage-balancing technique should have a minimum number of components, simple gate control circuit and it should minimize the IGBT switching losses and the losses associated with it. The current voltage-balancing techniques discussed previously are unable to achieve all the aforementioned goals simultaneously without significant compromises [15]. Therefore, a novel hybrid voltage-balancing technique is proposed in this paper to achieve good voltage balancing with minimum number of components and minimum total losses (i.e., IGBT losses and balancing circuit losses). This technique can be implemented in two different ways. One way is to use a simple active gate control technique with optimized snubber (in terms of losses) [16] and the other way is to use an active voltage clamp circuit with optimized snubber. In this paper, both simulation and experimental studies of the novel hybrid voltage-balancing technique implemented with active voltage clamp circuit with optimized snubber are presented.

II. Novel Hybrid Voltage-Balancing Technique

A. Simulation Studies

The circuit block diagram of the proposed hybrid voltage-balancing technique is shown in Fig. 1. The active voltage clamping circuit consists of few transient voltage suppressors (TVS) in series, a diode, and a clamping resistor. The circuit diagram of the active voltage clamping circuit is shown in Fig. 2. TVS have to be connected in series to get the desired clamping voltage ($V_{\rm CL}$). A *pn* diode ($D1$) is used to avoid a low-impedance path between gate and collector of the IGBT when the IGBT is ON. The clamping resistor is used to limit the current through TVS in order to keep them within safe power ratings. Also, it helps to damp any oscillations in gate voltage due to stray inductance in the circuit. The required clamping voltage is set by

$$V_{\rm CL} = I_{\rm CL} R_{\rm CL} + nV_{\rm BR} + V_{\rm GE} \quad (1)$$

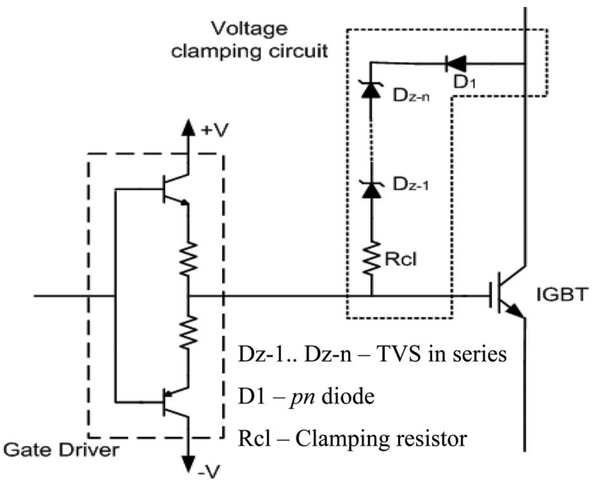

Fig. 2. Active voltage clamping circuit.

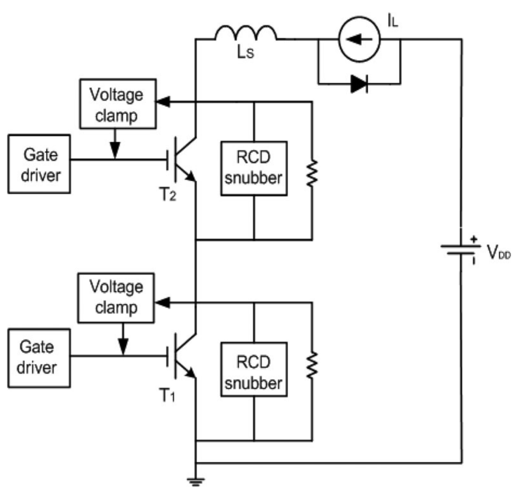

Fig. 3. Simulated circuit for hybrid technique with active voltage clamp.

where I_{CL} is the current through the clamp resistor, n is the number of TVS in series, V_{BR} is the breakdown voltage of a TVS, and V_{GE} is the IGBT gate–emitter voltage. When the IGBT collector–emitter voltage is higher than nV_{BR}, I_{CL} starts to flow through TVS, the diode ($D1$), and the clamp resistor by eventually clamping the IGBT collector–emitter voltage at V_{CL}.

The active voltage clamping circuits in series-connected IGBTs increase switching losses of IGBTs. To minimize the switching losses, a small RCD snubber can be connected across each IGBT collector–emitter terminal. The optimum value of the snubber capacitor is determined to ensure minimum total losses, considering both switching and snubber losses. The combined active voltage clamping and optimized snubber circuit clamps the IGBT collector–emitter voltage to a desired safe value, while minimizing the total switching losses. The optimum value of the capacitor can be found by simple theoretical calculation and simulations.

The hybrid voltage-balancing technique was simulated using Pspice Orcad for a chopper circuit shown in Fig. 3. The load current I_L of the chopper circuit was set to 20 A and dc-link voltage V_{DD} was set to 1 kV. The Toshiba 1 kV/50 A MG50N2YS1 IGBT model was used in the simulation studies. The IGBT model in the Pspice model editor is based on the Hefner model [17]. Pspice automatic parameter extraction program was used to generate the required parameters from data sheet for Hefner IGBT model. The freewheeling diode model used in chopper circuit was the fast recovery soft-switching 1200 V/30 A IDP30E120 diode from Infineon Technologies and the TVS model used was 1.5KE170A. The Pspice models for freewheeling diode and TVS (zener diode) were obtained from the Pspice standard model library. Three TVS were connected in series to achieve the desired breakdown voltage as shown in Fig. 2. The basic gate-drive circuit used is also shown in Fig. 2. The Fairchild 45 V/3 A BDP947 n-p-n bipolar transistor and Fairchild 80 V/3 A BDP956 p-n-p bipolar transistor models were used in the simulations. Those models were obtained from the manufacture. In this hybrid technique, voltage across the series IGBTs can be balanced by the active voltage clamp circuit even without the optimized snubber. In order to introduce voltage unbalance to illustrate a practical situation, a gate delay of 200 ns was applied to the lower IGBT T1 in the chopper circuit arrangement shown in Fig. 3. The voltage unbalance which occurred without any balancing technique is shown in Fig. 4. The initial turn-OFF transient voltage of the T2 reached 880 V and steadied at 560 V while voltage of T1 settled at 440 V. At turn-ON, the voltage of T1 reached 1 kV.

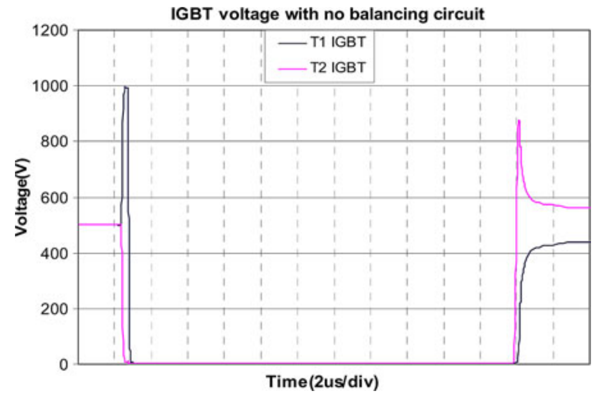

Fig. 4. IGBT voltages with no balancing technique.

Then, the chopper circuit was simulated with only active voltage clamp (no snubbers) as the balancing technique and the waveforms of the two series-connected IGBTs are shown in Fig. 5. At the initial turn-ON and OFF, voltages reached around 540 and 530 V, respectively but OFF-state voltage was steadied at 500 V. Initial voltage overshoots can be expected since the clamping voltage is increased due to the voltage drop across the series resistor in active voltage clamp. Since there are no control stages in the voltage clamp circuit (unlike in a gate control technique), active voltage clamp responds very rapidly to any over voltage across the IGBT. As mentioned earlier, the optimum snubber capacitance can be approximated by a simple calculation and more accurately by simulation. Theoretical calculation of the optimum capacitance is explained in [18]. It is found that

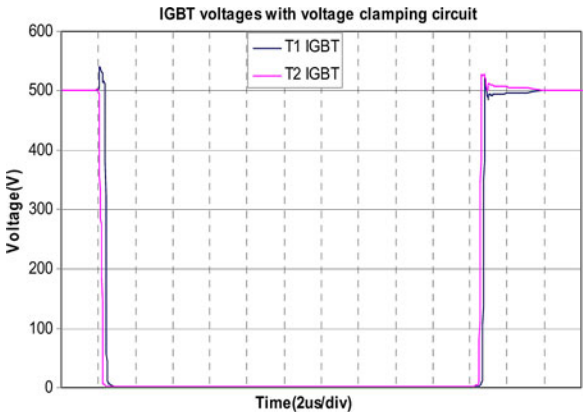

Fig. 5. IGBT voltage waveforms with active voltage clamping circuit.

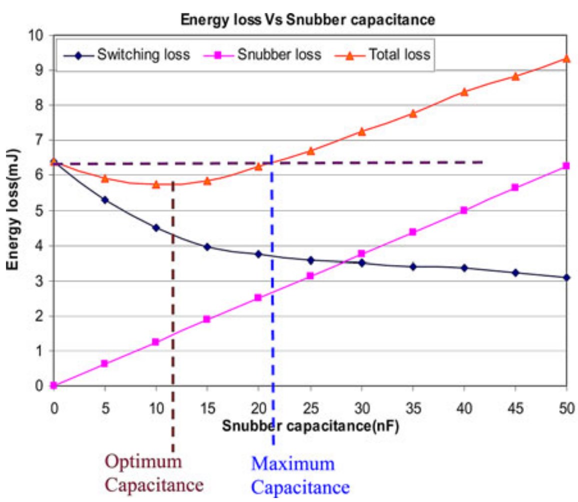

Fig. 6. Switching losses, snubber loss, and total losses.

for minimum total loss snubber capacitance is [18]

$$C = \frac{1}{\sqrt{6}} \cdot \frac{I_L \cdot t_f}{V_{\mathrm{DC}}}. \quad (2)$$

For Toshiba 1-kV/50-A MG50N2YS1 IGBT operating at $V_{\mathrm{DC}} =$ 500 V and $I_L = 20$ A (operating conditions in the simulation), optimum snubber capacitance value at minimum total loss is 10 nF.

To find the optimum snubber capacitance by simulation, the chopper circuit shown in Fig. 3 was simulated and energy losses in the IGBTs were calculated. Snubber loss was calculated as $(0.5).C.V_{\mathrm{DC}}^2$. Both IGBT switching losses and snubber losses were obtained for snubber capacitances varying from 0 (snubberless) to 50 nF. The switching losses, snubber losses, and the total losses were plotted in the same graph, which is shown in Fig. 6. The optimum capacitance value is around 12 nF compared to 10 nF in theoretical calculations. The minimum total loss is 5.75 mJ which consists of snubber loss of 1.5 mJ and switching loss of 4.28 mJ. The snubber-less total loss (i.e., only switching loss) is 6.41 mJ. Therefore, the energy saving of using an optimum snubber is 0.66 mJ which is 10.3% of the snubber-less energy loss. The maximum capacitance at which energy can be saved compared to snubber-less energy as shown in Fig. 6, is 22 nF.

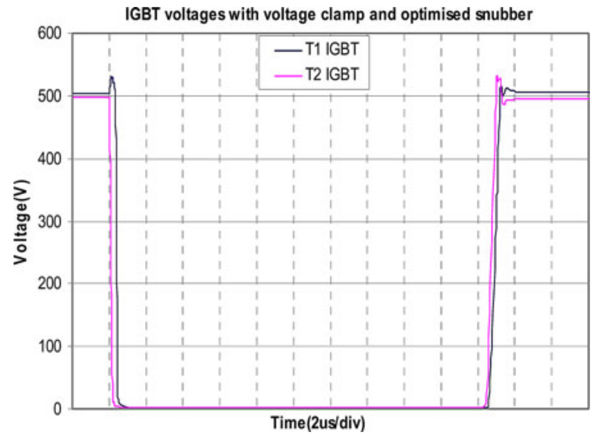

Fig. 7. IGBT voltage waveforms with active voltage clamp and optimum snubber.

The chopper circuit (in Fig. 3) was simulated with the active voltage clamp circuit and the optimum snubber in which snubber capacitance was chosen to be 15 nF. The IGBT voltage waveforms of the two series-connected IGBTs in the chopper circuit are shown in Fig. 7. It shows good voltage balancing with the voltage clamp and optimized snubber. Initial turn-ON and OFF voltages reached around 525 V but OFF-state voltage was steadied around 500 V. Initial voltage overshoots are due to the voltage drop across the series resistor in the voltage clamp circuit. The T2 IGBT voltage was clamped a few volts below the snubber-less clamped voltage which is shown in Fig. 6, since the snubber capacitance reduces the rate of rise of voltage.

B. Experimental Studies of the Novel Hybrid Voltage-Balancing Technique

In order to validate the hybrid voltage-balancing technique experimentally, three 3.3-kV/1200-A Mitsubishi IGBT modules (model CM1200HB-66H) were connected in series and used in a clamped inductive load circuit operating at 4.2 kV. The test circuit arrangement was similar to that shown in Fig. 3. A photograph of the experimental setup is shown in Fig. 8.

All three IGBTs were obtained from the same batch to minimize device parameter spread. The clamping voltage of the voltage clamp circuit was set around 1.8 kV for each IGBT. The active voltage clamp circuit was built into the gate-driver board which was placed on top of each IGBT to minimize stray inductance. The voltage and current waveforms with no voltage balancing (neither active voltage clamp nor snubber) are shown in Fig. 9. The peak voltage of T1 IGBT reached around 2100 V and the peak voltages of T2 and T3 IGBTs reached around 1800 V, due to the inductive overshoot. The turn-OFF voltage and current waveforms of IGBTs in series with active voltage clamp circuit (no snubbers) are shown in Fig. 10. Initially voltages of T1 and T2 IGBTs rose to 1880 and 1800 V, respectively, while the voltage of T3 IGBT reached 1650 V due to the inductive overshoot. Voltage unbalance with the active clamp circuit was reduced compared to Fig. 9.

Fig. 8. Experimental setup.

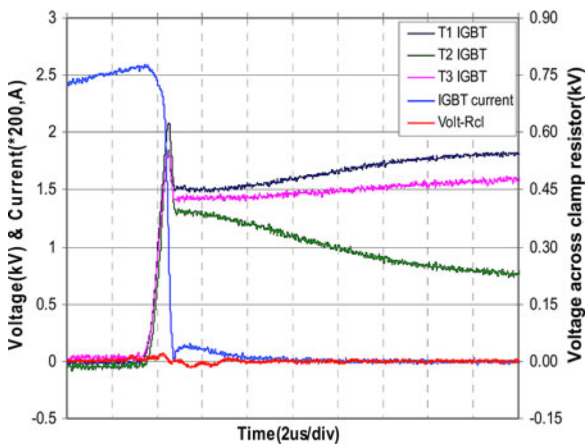

Fig. 9. IGBT turn-OFF voltage and current waveforms at 4200 V/520 A.

In order to find the optimum snubber capacitance values, tests were carried out at different load current levels for different snubber capacitances in RCD snubbers. The turn-OFF voltage/current waveforms of three series-connected IGBTs with snubber capacitances of 0.2 μF at load current of 520 A are shown in Fig. 11. The initial peak voltage of T1 was limited to around 1860 V and T2 and T3 IGBT voltages reached around 1760 and 1740 V, respectively. Oscillations seen in all IGBT voltage waveforms are due to the ringing between the stray inductance of the circuit (including snubber loop) and snubber capacitances. These oscillations can be minimized by minimizing the circuit loop inductance in the power circuit design stage (e.g., by using laminated bus bars). The voltage balancing could have been improved more as compared to the waveforms in Fig. 10 due to lower dv/dt achievable with 0.2 μF snubber capacitor, if there were no oscillations.

By comparing waveforms in Figs. 9–11, it can be seen that the hybrid voltage-balancing technique is quite effective. The other important aspect of hybrid voltage-balancing technique is to find out the optimum capacitance where total losses are minimized. To find the optimum capacitance, three IGBTs in series were tested for load currents varying from 270 to 780 A.

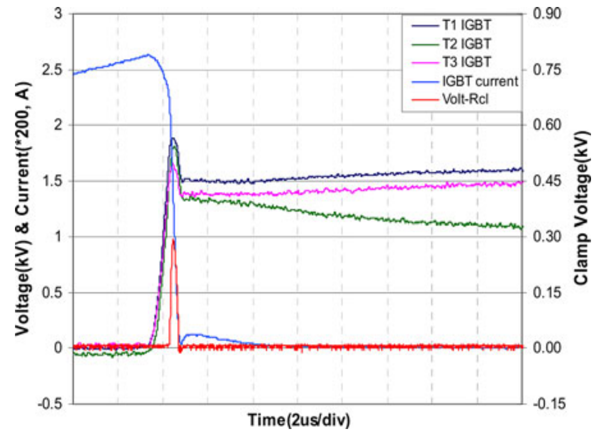

Fig. 10. IGBT turn-OFF voltage/current waveform with active voltage clamp at 4200 V/520 A.

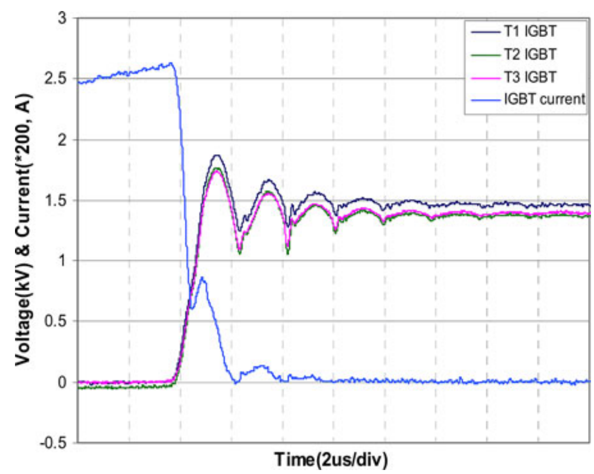

Fig. 11. IGBT turn-OFF voltages with hybrid voltage-balancing technique (snub. cap $= 0.2$ μF).

The IGBT switching loss, snubber capacitor and diode losses (snubber loss), and total loss for T1 IGBT were calculated at each current level and they are plotted in Fig. 12 for the load current of 520 A. To find out the optimum capacitance at different load currents, total loss was plotted against snubber capacitance for different load currents, as shown in Fig. 13. It can be seen that in Fig. 13, the optimum capacitance increases with load current. When the IGBT current is high, switching loss reduction dominates over snubber loss increase at low snubber capacitances and the converse is true for high snubber capacitances. At low current levels, snubber loss always dominates over switching loss reduction. This is because snubber loss does not greatly depend on load current (diode loss is increased with load current slightly) but switching loss heavily depends on load current for a given voltage level. Therefore, by analyzing the results in Fig. 13, it can be concluded that effectiveness of hybrid voltage-balancing technique depends on the load current and it becomes more effective at high current levels.

Energy savings achieved due to passive snubber compared to snubber-less loss is shown in Fig. 14 on a percentage basis.

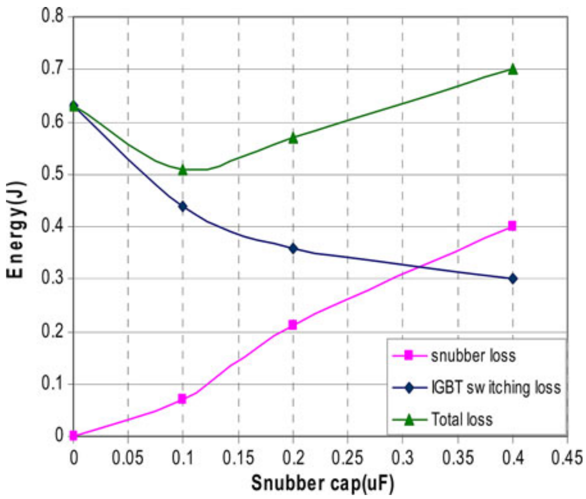

Fig. 12. IGBT switching loss, snubber loss, and total loss versus snub capacitor (load current 520 A).

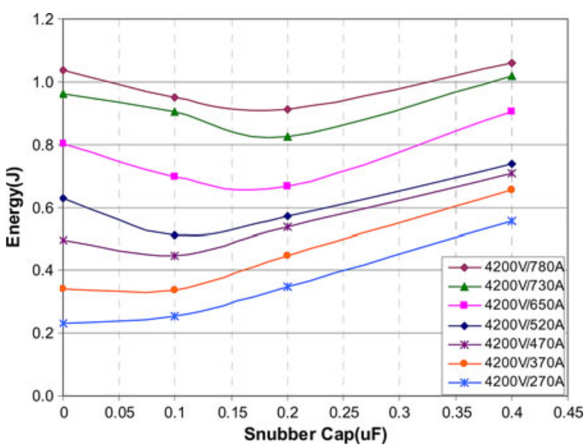

Fig. 13. Total loss at different load currents and snubber capacitances.

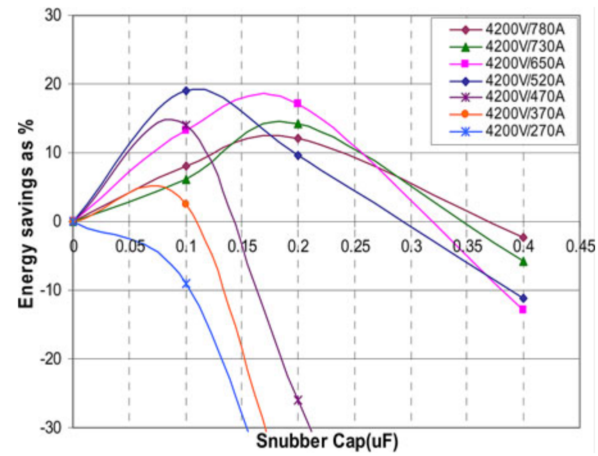

Fig. 14. Percentage of energy savings by using a passive snubber.

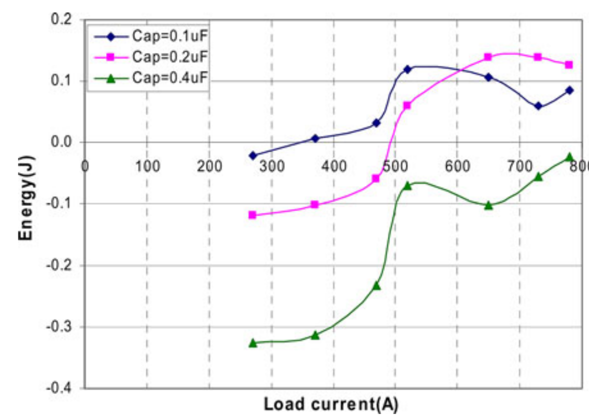

Fig. 15. Actual energy savings at different load currents.

As load current is increased, the reduction in IGBT switching loss with the snubber decreases compared to snubber-less switching loss. This is due to the increase in rate of rise of IGBT voltage (as current increases, dv/dt increases in the snubber) effects the IGBT switching loss reduction. Also at low currents, snubber loss dominates over switching loss reduction. These are the reasons to have a particular current level in Fig. 14 where maximum percentage of energy saving can be achieved as load current is increased for a given snubber capacitor. Maximum percentage of energy savings are achieved at 520 and 650 A for 0.1- and 0.2-μF snubber capacitances, respectively. The overall maximum percentage of energy saving is obtained at 520 A with 0.1-μF snubber capacitance. The actual energy savings with passive snubbers compared to snubber-less energy loss at different load currents are shown in Fig. 15. If the load current is lower than 350 A, a passive snubber would increase the total loss compared to snubber-less loss. If the load current is greater than 490 A, both 0.1- and 0.2-μF snubber capacitance would reduce the losses compared to snubber-less loss. If the load current is between 350 and 490 A, 0.1-μF snubber capacitance will reduce the losses, whereas 0.2-μF snubber capacitance will increase the losses, compared to the snubberless loss. The 0.4-μF snubber capacitance always increases the total losses irrespective of load current, but the loss increase is higher at low load currents. Therefore, 0.1-μF snubber capacitance is more effective in energy saving in 4200-V/800-A chopper application.

Average energy savings for different load current ranges are shown in Table I. If a 0.1-μF snubber capacitor is used, there is always a positive average energy saving. It can be seen that average energy saving is negative if the load current varies between 270 and 780 A for 0.2 μF. This is due to the dominance of high energy losses (negative saving) at low current levels over the energy savings at high current levels. The average energy saving is increased as load current is increased but it is reduced at high currents (in this case a current of 730–780 A). At high current levels, energy saving is increased with an increase of snubber capacitance.

III. Discussion on Optimization of the Number of IGBTs in a Series String

In high-power electronics applications where series connection of IGBTs are used (e.g., high-voltage direct current

TABLE I
AVERAGE ENERGY SAVINGS FOR DIFFERENT LOAD LEVELS

Load current range (A)	Average energy saving (%)	
	0.1 μF	0.2 μF
270 – 780	7.68	-9.82
370 – 780	10.47	-2.91
470 – 780	12.1	5.42
520 – 780	11.63	13.27
650 – 780	9.16	14.52
730 – 780	7.14	13.21

converters), voltage balancing and power losses are the most important factors to be considered. Power losses depend both on voltage-balancing technique and number of IGBTs in a series string. Therefore, a voltage-balancing circuit should have low losses and the novel hybrid voltage-balancing technique described in this paper is well suited for the high-power applications. The number of devices in a series string of IGBTs depends on the operating voltage of an application and the individual device voltage rating. For a given application, the use of higher voltage-rated IGBTs leads to a fewer number of devices. However, lower rated IGBTs have lower ON-state voltage drops due to shorter base region thickness and shorter switching times due to the lower stored charge compared to the higher rated IGBTs. When the devices are connected in series, the total power loss depends on the number of devices and the individual device power loss.

A. Analysis of IGBT Power Losses in a Series String

In this section, individual IGBT power losses (both switching and conduction) and total power loss in the series strings of 1.2-, 1.7-, 3.3-, and 6.5-kV IGBTs are analyzed. ISE TCAD software is used to design and simulate different rated IGBTs. For the design of 1.2-, 1.7-, and 3.3-kV IGBTs, nonpunch through base structure and planar gate structure were considered. For 6.5-kV IGBT, nonpunch through structure is not practical and hence soft-punch through structure [19] was simulated.

The ISE TCAD simulation was carried out for a chopper circuit (shown in Fig. 16) operating at 4.5 kV/100 A. The power switch T_1 in the chopper circuit represents a series string of IGBTs. Four different series combinations, that is, series connection of six 1.2-kV IGBTs, four 1.7-kV IGBTs, two 3.3-kV IGBTs, and single 6.5-kV IGBT are simulated to represent the power switch in the chopper circuit. The number of devices in the string for a particular rated IGBT is decided by considering a derating factor.

When the IGBTs are connected in series, the total power loss (both conduction and switching loss) is equal to the sum of the power losses of the individual devices in the string. Series-connected IGBT strings can be operated at different duty cycles depending on the application. Turn-ON and OFF losses do not depend on duty cycle, while conduction loss increases with the increase in duty cycle. The total power loss for the series strings of six 1.2-kV IGBTs, four 1.7-kV IGBTs, two 3.3-kV IGBTs, and single 6.5-kV IGBT for 20% and 80% duty cycles are presented in Figs. 17 and 18, respectively. The total power loss increases with the increase in operating frequency and the level of increase in power loss depends on device characteristics. At low frequencies, conduction loss contribution is more significant than switching loss contribution to the total power loss.

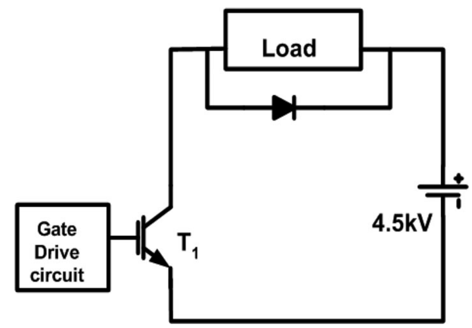

Fig. 16. 4.5-kV/100-A chopper circuit.

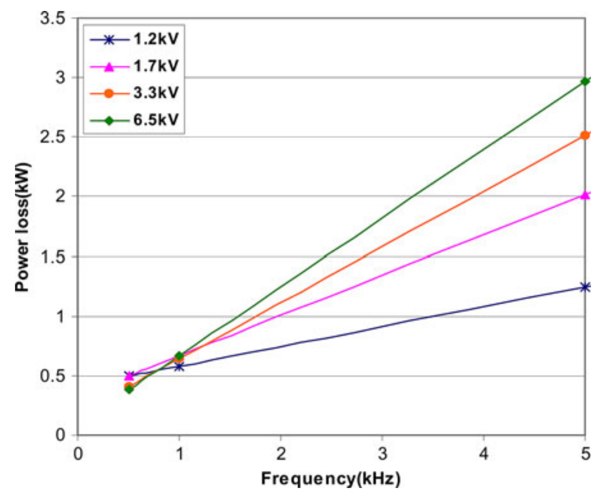

Fig. 17. Total power loss versus frequency for $D = 20\%$.

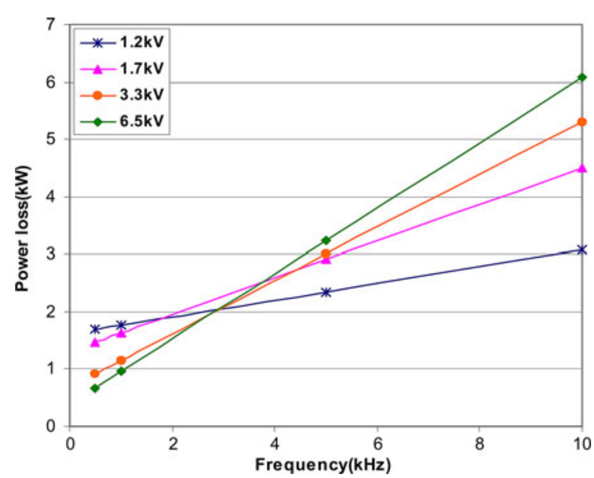

Fig. 18. Power loss versus frequency for $D = 80\%$.

B. Main Factors in Optimizing Number of Devices in a Series IGBT String

In general, at low frequencies, series string with higher rated IGBTs (fewer devices in series) results in significant power savings. The power savings over the life of the converter should be capitalized to see the economies of converters. The other issue related to the operating frequencies is the filters required in converter circuits. If the switching frequency is low, filter units are bulky and expensive.

In series connection of IGBTs, voltage across each device is equalized by using external voltage-balancing (both transient and steady state) circuits. If the number of devices is increased in an IGBT string, the number of voltage-balancing circuits must also be increased. Therefore, capital cost involved in voltage-balancing circuits is increased as the number of IGBTs per string is increased. The number of devices required can be minimized by using higher rated IGBTs, but those IGBTs are more expensive than lower rated IGBTs. Therefore, the cost of devices for few higher rated devices may be similar to the higher number of lower rated devices. To ensure continuous operation of the IGBT string in case of a device(s) failure, few additional IGBTs (and snubbers if used) are connected in a series string. This addition of devices may make IGBT string with higher rated devices more expensive than lower rated IGBTs. The voltage-balancing circuit (Snubber components, zener diodes, etc.) used with a higher rated IGBT should also be higher rated and are expensive compared to the voltage-balancing circuit used with lower rated IGBTs. The other important issue is the reliability of the series IGBT string. If the number of components in the series strings is high, the reliability will be low, since each component has a finite probability of failure. Therefore, series IGBT strings with lower rated IGBTs are less reliable than series strings with higher rated IGBTs. The maintenance cost of lower rated IGBTs can be greater than higher rated IGBTs since more time and resources are needed for higher number of devices.

In the literature, Githiari [20] has optimized the number of device in series considering only ON-state voltage drop which represents conduction loss. The optimum number of devices cannot be solely decided on power losses, but the other main factors described earlier have to be considered. Therefore, in deciding on the optimum number of devices, all issues mentioned earlier should be considered from an economic point of view.

IV. Conclusion

In series connection of IGBTs, the gate control circuits ensure better voltage balancing compared to active clamping and passive snubbers in terms of switching losses and commutation time. Most of the active gate control circuits are very complex; hence, they are less reliable compared to other voltage-balancing techniques. The active clamping and passive snubber circuits are used because they are simple and easy to implement compared to complex active gate control techniques. The proposed hybrid voltage-balancing technique showed good voltage balancing and has low power losses and circuit complexity. Simulation and experimental results confirmed the possibility of finding an optimum capacitance. The number of IGBTs in a series string was optimized in terms of power losses. Significant power savings can be achieved by using lower rated IGBTs at higher frequencies and higher rated IGBTs at low frequencies. The optimum number of devices in an IGBT string should not be decided solely on the basis of power loss savings, but other factors such as capital cost of the devices and voltage-balancing circuits, reliability, and maintenance costs have to be considered.

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