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The measurement of the relative phase of two sinusoidal electrical signals is a frequently encountered task in heterodyne interferometry, but also occurs in many other applications. Especially in interferometry, multi-radian detectors are often required, which also count integer multiples of 2π. While a large variety of solutions to this problem is already known, we present an alternative approach, which pre-processes the signals with simple analog circuitry and digitizes two resulting voltages with an analog-to-digital converter (ADC), whose sampling frequency can be far below the frequency of the sinusoidal signals. Phase reconstruction is finally carried out by software. The main advantage of this approach is its simplicity, using only few low-cost hardware components and a standard 2-channel ADC with low performance requirements. We present an application on the two-color interferometer of the ASDEX Upgrade tokamak, where the relative phase of 40 MHz sinusoids is measured.

I. INTRODUCTION

In interferometry, the phase of an electromagnetic wave after passing through a sample is measured, often relatively to an external reference, like a second electromagnetic wave which propagates through vacuum or air. This phase measurement can be performed by combining probe and reference beam to generate, depending on phase, constructive of destructive interference. Alternatively, a heterodyne phase detection scheme can be applied, in which the two waves which are brought to interference have slightly different frequency. Their interference results in a beat signal, whose envelope function is carrying the desired phase information. The beat frequency is determined by the frequency difference $\Delta\omega$ of the two waves, which can be set to values in the kilohertz to megahertz range to make the signal well accessible for measurement with the available detectors. The heterodyne phase detection concept can be applied to microwaves, throughout the terahertz range, and in the infrared and visible range and is sometimes referred to as "down-mixing" of the involved frequencies. For the generation of two waves with frequency difference $\Delta\omega$, different methods exist. One of them is to use two sources whose relative emission frequency is feedback-controlled, like two laser cavities[1]. Another method is to use only one source, split the beam in two and shift the frequency of one component. Frequency shifting is usually achieved via the Doppler effect and can be implemented e.g. with rotating optical gratings[2] in the terahertz range, or with acousto-optic modulators (AOMs) in the visible and infrared range. On the two-color interferometer used for plasma density measurement on the ASDEX Upgrade tokamak, whose optical layout we have discussed in ref. [3], AOMs are used to generate a frequency shift of 40 MHz. Accordingly, the readout electronics of the interferometer has to detect the relative phase of two 40 MHz sinusoids, counting also integer multiples of 2π. There is a large variety of electronic circuits and data acquisition systems which fulfill this task, based on different operating principles. Just to name few of them, there are hard-wired phase counters which use an internal phase-locked loop and account for phase changes by increasing or decreasing the reading of a binary counter[4]. Another approach is to digitize the sinusoidal signal with an ADC whose sampling frequency is exactly 4/3 of the signal frequency, resulting in intentional aliasing, and subsequent phase analysis by digital signal processing[5]. In earlier work[3], we have shown that digitization of probe and reference signal with a sufficient oversampling factor allows for carrying out the entire phase analysis by software, but requires fast ADCs and much memory if the beat frequency is high. The drawback of most of these methods is that they require either fast ADCs, with sampling frequencies of the order of the beat frequency, or even far above, which can be challenging when the beat frequency is in the upper MHz range, or they require sophisticated electronic circuits which have to be built specifically for the individual application. Our recent approach, on the contrary, uses a simple circuit of low-cost components and a standard ADC.

II. ELECTRONIC CIRCUIT

The key component of our phase detector is the integrated circuit AD8302, which has two inputs ("INPA" and "INPB") for sinusoidal signals, and a phase output ("VPHS") which (ideally) delivers 1.8 V when the input signals are in phase, and 0 V when the input signals have a phase shift of 180 degrees. This output voltage will be referred to as U1 in the further discussion. The actual response of the AD8302 circuit has been found to be non-linear, as will be discussed below. Obviously, the output of a single AD8302 chip does not allow for unambiguous phase detection, as e.g. a voltage increase from 0 to 1.8 V could mean that phase has increased from 180 to 360 degrees, but could also mean that it has decreased from 180 to 0 degrees. To resolve this ambiguity, both sinusoidal input signals are split and fed into a second AD8302 chip, where the phase of one of the signals is shifted by 90 degrees, as illustrated in figure 1 and already briefly summarized in earlier work[6]. For signal splitting, MiniCircuits PSC-2-1 power splitters are used, and for phase shifting, the MiniCircuits PSCQ-2-50 is used. That way, an output voltage of the second
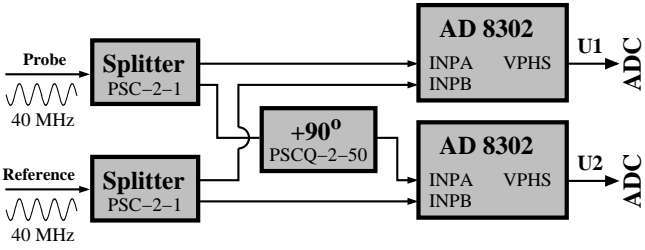
FIG. 1. Schematic block diagram of the phase counter circuit.

chip is obtained which is 0 V if the phase shift is 90 degrees and 1.8 V if it is 270 degrees. This voltage will be referred to as U2. The output of the two AD8302 chips, i.e. U1 and U2, is fed into a 2-channel simultaneous sampling ADC. In our application on the ASDEX Upgrade interferometer, the input frequency is 40 MHz and the ADC sampling rate is 500 kSamples per second. We use a 14-bit ADC with an input voltage range of -10V to +10V, which is more than actually needed for the 0-1.8 V signals, but was a convenient choice, as a multipurpose ADC could be taken off-the-shelf. The choice of the ADC speed does not depend on the frequency of the sinusoidal input signals. Rather than this, it has to be matched to the time scale on which phase variations of the input signals occur.

III. ANALYSIS ALGORITHM

When analyzing the data recorded by the ADC, it was found that the AD8302 circuits exhibit imperfections. They do not accurately deliver 0 V when the input signals have 180 degrees phase shift, and not exactly 1.8 V when they are in phase. In the latter case, the output voltage was found to be close to 2 V. Moreover, their response is not linear over the full range, i.e. when the phase shift of the input signals increases linearly in time, the output voltage does not linearly increase from its minimum to its maximum value. Whereas good linearity is observed in an interval of about 15° to 165°, clear deviation from linearity occurs close to 0 and 180 degrees. To characterize the AD8302 response, we therefore connected two frequency generators to the inputs of the phase detector, whose internal clock oscillators were synchronized and whose output frequency was set to 40 and 40.0005 MHz, respectively, to generate a continuous phase drift. Ideally, the AD8302 should deliver a linear ramp up and down from 0 to 1.8 V and back under these conditions. The actual result for the two outputs (U1 and U2) of the phase counter unit is shown in figure 2. We built in total four phase counter units from eight AD8302 chips, which were found to show different response, as the second plot panel of figure 2 illustrates (grey dashed lines). From the data obtained with the two frequency generators, a calibration curve has been derived for each phase detector. The time axis was split equidistantly into 360 segments which correspond to a relative phase of 0, 1, 2, ... degrees. This was repeated for all oscillation periods in the calibration data set. Finally, the average voltages U1 and U2 for each integer angle (in degrees) were cal-
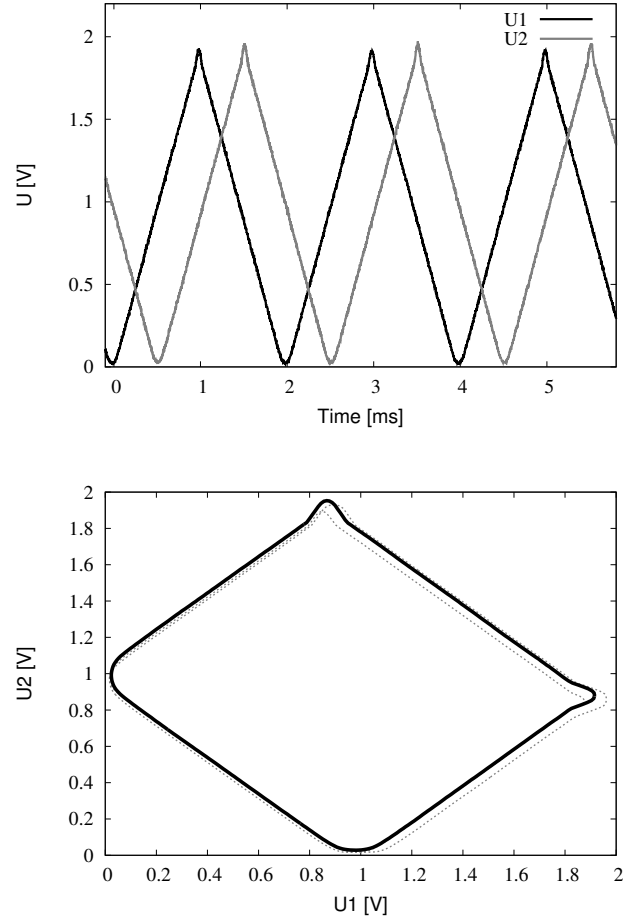

FIG. 2. Result of feeding two sinusoidal input signals of 40 and 40.0005 MHz into the phase counting circuit. Top: Time traces of the output voltages U1 and U2. It can be seen that the upper reversal point is actually close to 2 V, and slightly differs for U1 and U2. Bottom: Phase diagram, where U1 and U2 have been plotted versus each other. The bold black curve corresponds to the same phase counter shown in the upper plot panel. The dashed grey curves correspond to two other circuits that were built, illustrating the spread within a delivery batch of chips.

culated, resulting in a calibration curve defined by 360 data points, which we label $(U1_i \mid U2_i)$, $i \in \{0, ..., 359\}$, in the further discussion.

To perform phase measurements, the voltages U1 and U2 are recorded with the ADC. For each point in time, the phase φ is then calculated with a computer algorithm, which works as follows: For the measured pair of voltages $(U1 \mid U2)$, the point i on the calibration curve is determined which is closest, i.e. which minimizes $d_i = \sqrt{(U1 - U1_i)^2 + (U2 - U2_i)^2}$. After this, the distance d_j to the second-closest point j is calculated, and linear interpolation is performed between the angles corresponding to those two points, using the ratio d_i/d_j. This is illustrated in figure 3. The method described up to this point has a clear weakness at the reversal points (corresponding to the corners of the calibration curve, roughly at 0, 90, 180 and 270 degrees), as the evolution of one of the two voltages U1 and U2 is rather flat there (U1 flat at 0° and 180°, U2 flat at 90° and 270°). This means
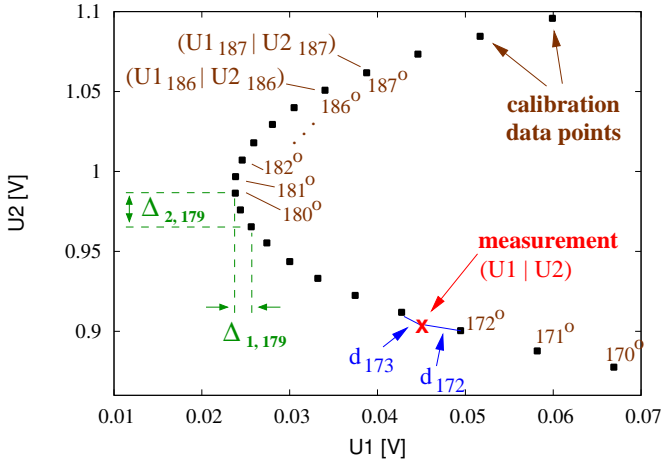
FIG. 3. Illustration of the analysis algorithm: The phase diagram shows a part of the calibration curve, which consists of 360 data points - one per degree. To calculate the phase corresponding to a measured data point (U1 | U2), the closest and second-closest point on the calibration curve is determined - in the example, this is 173° and 172°, respectively. The corresponding distances in the U1-U2 plane are labeled d_{173} and d_{172}. To calculate the coordinate-weighted distances d'_i (which are not shown in the figure), the voltage variations $\Delta_{1,i}$ and $\Delta_{2,i}$ in the vicinity of the ith calibration point are used, which are illustrated for one representative case (i=179). In the example, the resulting angle is approximately 172.7^o.

that a variation in the phase angle results only in a clear variation of one of the voltages, whereas the other one is rather constant and does therefore not carry much phase information. Having identified the closest point i on the calibration curve, the algorithm therefore calculates the variation of U1 and U2 in the vicinity of this point as $\Delta_{1,i} = |U1_{i-1} - U1_{i+1}|$ and $\Delta_{2,i} = |U2_{i-1} - U2_{i+1}|$ (also illustrated in figure 3), uses the coordinate-weighted distance $d'_i = \sqrt{(\Delta_{1,i} \cdot (U1 - U1_i))^2 + (\Delta_{2,i} \cdot (U2 - U2_i))^2}$ to detect the second-closest point j and performs linear interpolation based on the ratio d'_i / d'_j:

$$\varphi = i + (j - i) \frac{d'_i}{d'_i + d'_j}$$

In case of input signal perturbation, which we sometimes encountered as a result of electric cross-talk, the signals might no longer have proper sinusoidal shape, which often leads to data points $(U1 | U2)$ which are far off the calibration curve. In such cases, an outlier rejection algorithm was found to be helpful, which flags the result as invalid if d_i exceeds an empirical threshold.

The approach described so far allows the determination of the phase shift as a fraction of 2π. Many applications require multi-radian phase detectors, which are capable of tracking phase shifts greater than 2π. This has been accomplished by introducing a variable for the integer multiples of 2π in the analysis algorithm which is incremented by one when the reconstructed phase jumps from 360 to 0 degrees, and which is decremented by one when there is a transition from 0 to 360 degrees. This requires the ADC sampling frequency to be chosen large enough to ensure that phase changes in between two samples will

be much less than 180 degrees under all experimental conditions, as stated at the end of section II.

IV. RESULTS

The two-color interferometer on the ASDEX Upgrade tokamak sends two laser beams from a helium-neon ($\lambda_{HeNe} = 633nm$) and a carbon dioxide ($\lambda_{CO2} = 10.6\mu m$) laser through a plasma along the same path[3]. The total optical path that the laser beams travel from the AOMs to the detectors is more than 10 meters. Although the interferometer frame rests on an independent support structure on the concrete floor of the experiment hall, the presence of vacuum pumps and other devices with moving parts inside causes a certain level of vibration in the optical setup. The two-color setup measures two phase shifts experienced by two different laser wavelengths, which allows one to compensate for vibrations and to get an unbiased measurement of the line-integrated electron density in the plasma. First, for simplicity, we discuss only results from the HeNe branch of the two-color interferometer. Phase changes experienced by the HeNe beam are dominantly caused by vibrations, whereas the plasma density has only little influence. As discussed above, the interferometer uses heterodyne detection, where an acousto-optic modulator shifts the frequency of one beam component by 40 MHz. The resulting interference signal is a 40 MHz beat signal, which is registered by a fast photo diode. The phase counting electronics compares the phase of this detector signal to the phase of the modulator driver signal, which is a 40 MHz sinusoid as well. Figure 4 shows the temporal evolution of the phase counter output voltages U1 and U2, as well as the phase evolution reconstructed by the algorithm described in the previous section. The maximum phase variation in this example is about 8x 2π peak-to-peak, corresponding to an optical path change of about 5 micrometers. Figure 5 finally shows an example of a plasma density measurement carried out with the new phase counting electronics. Two of the phase counters have been installed on the central interferometer chord to record both, the phase evolution of the HeNe and the CO_2 branch of the interferometer. The figure shows the corresponding time traces over a time period of 3 seconds. It can be seen that the two traces look very similar, representing mainly the optical path changes in the interferometer due to vibrations. In accordance with the ratio of the wavelengths, the HeNe branch registers phase changes of more than 70x 2π, whereas the phase in the CO_2 branch varies by only about 4x 2π (not considering the negative-going spike at t=2.3s, which is not caused by vibration, but by a high plasma density event, as will become apparent in the further discussion). Density information is recovered from the two phases measured via equation (2) in ref. [3], which implies that basically the HeNe phase is multiplied by the wavelength ratio and subtracted from the CO_2 phase. With the appropriate pre-factor and sign, this yields the time trace of the line-integrated density, which is also shown in figure 5. The corresponding plasma discharge was shut down by massive gas injection at t=2.3s, which is a common method
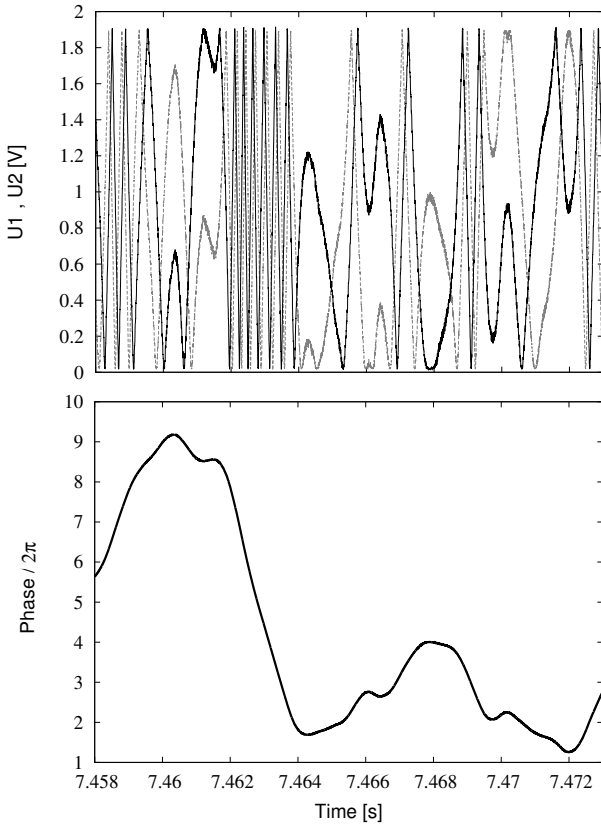
FIG. 4. Temporal evolution of the voltages U1 (black) and U2 (gray, upper plot panel) and the reconstructed phase evolution (lower plot panel) for the helium-neon branch of the central interferometer channel in ASDEX Upgrade discharge #32214. The diagram shows a short time window of about 15 ms out of an 8-second plasma discharge.
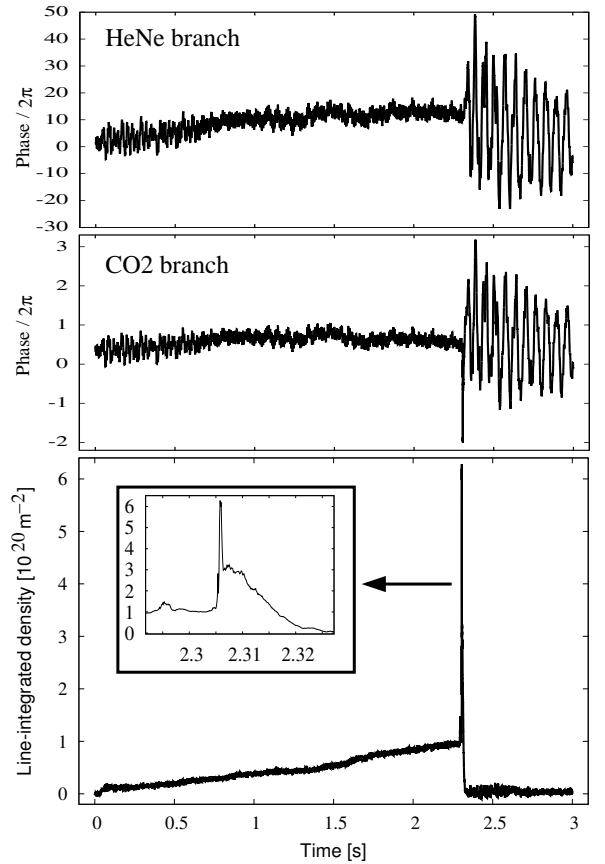

FIG. 5. Temporal evolution of the phase in the HeNe branch (top) and the CO_2 branch (center) during ASDEX Upgrade discharge #33242, which was shut down by massive gas injection at t=2.3s. The line-integrated density calculated from those two phase signals is shown in the lower plot panel.

of rapidly terminating a tokamak plasma. This technique was developed for unstable discharges, where the forced shutdown of the discharge reduces both, thermal loads to the plasma-facing components and electromagnetic forces on the plasma vessel, as compared to the uncontrolled collapse of the discharge, which otherwise would occur shortly after. The massive gas injection induces a sudden and steep rise of the density up to a value of about $6.3 \ 10^{20} \ m^{-2}$ within roughly a millisecond, followed by a decay down to zero within the next 15-20 ms, after which there is no plasma any more. Even under these conditions, the multiples of 2π have been correctly tracked by the phase counter, such that the time trace returns to zero at the end. The sudden disruption of the toroidal plasma current caused by the gas injection results in substantial currents induced in the vacuum vessel structure, which cause electromagnetic forces acting on the tokamak. Although mechanically coupled only via the massive concrete floor, vibrations are also excited in the interferometer structure, which explains the strong oscillation of both phase signals after t=2.3s. The density trace remains unaffected, as the two-color interferometer successfully compensates the vibrations.

Over several years of operation, the phase counters have been found to be reliable and stable in their calibration curves. Failure of the tracking of multiples of 2π is only observed when the input signals have too little amplitude or no longer proper sinusoidal shape. The former may happen in case of optics misalignment, or temporary beam refraction on the CO_2 branch when large quantities of gas are injected to shut down the discharge, like in the example presented in ref. [3]. The latter is regularly observed when ion cyclotron resonance heating at a frequency of 36.5 MHz is applied on ASDEX Upgrade, which electrically cross-talks into the 40 MHz interferometer signals despite of shielding efforts. The installation of band-pass filters to reject the 36.5 MHz helped to clearly mitigate this problem.

V. SUMMARY

In this article, we have presented a rather simple phase detection circuit, which requires only few commercially available electronic components and an ADC with moderate speed and resolution, allowing for fast implementation at low cost. It is applicable to a wide range of frequencies, with an upper limit of 2.7 GHz set by the capabilities of the AD8302 chip. The signal splitter and 90° phase shifter have to be appropriately chosen for the frequency range of interest, with the choice given in section II yielding good results at the 40 MHz beat frequency

of the ASDEX Upgrade interferometer. Since the integrated circuits used for phase detection show non-linear response, with the exact characteristic varying from chip to chip, an initial calibration measurement needs to be carried out to obtain a calibration curve for each single phase detector unit. We have used the calibration data set over years and have not observed any noticeable drift in time. An algorithm has been presented which calculates the phase information from the digitized output signals of the phase detector units. In our application, data analysis is performed offline. At the sampling frequency of 500 kSamples per second, however, the algorithm is less than a factor of 3 too slow for real-time application on a standard CPU, where it takes roughly 25 seconds to process the data of a 10-second plasma discharge. By further optimization of the algorithm for speed, e.g. by using lookup tables rather than performing calculations, or implementation on a programmable logic device, real-time capability appears achievable.

Due to the simplicity of the involved hardware, this phase counter could be an interesting option for many applications in and beyond interferometry, and for scientific research applications was well as for academic education purposes. Implementing the hardware part is simple, cheap and straight-forward. With the initial knowledge that phase counter response is non-linear and the recording of a calibration data set is required, also the implementation on the software side can be accomplished with moderate effort.

[1] K. Kawahata, A. Ejiri, K. Tanaka et al., Fusion Engineering and Design **34-35**, 393-397 (1997).
[2] D. Veron, Optics Communications **10**, 95-98 (1974).
[3] A. Mlynek, G. Pautasso, M. Maraschek et al., Fusion Science and Technology **61**, 290-300 (2012).
[4] H. R. Koslowski, Measurement Science and Technology **5**, 307 (1994).
[5] M. A. Van Zeeland, R. L. Boivin, T. N. Carlstrom et al., Review of Scientific Instruments **79**, 10E719 (2008).
[6] A. Mlynek, L. Casali, H. Eixenberger et al., 40th EPS conference on plasma physics, Espoo, Finland, Europhysics Conference Abstracts **37D**, P6.012 (2013) http://ocs.ciemat.es/EPS2013PAP/pdf/P6.012.pdf.