DRF1510

Application Note

Class-D Full-Bridge RF Generator with Internal Cooling System

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Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document.

1.2 Revision 1.1

In Revision 1.1 of this document, contact information was updated and select part numbers in Appendix III were changed. For more information, see Appendix III: Parts List.

Contents

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2 Introduction

This application note describes an evaluation of the DRF1510 Class-D Full-Bridge (FB) Hybrid Module with internal cooling system. The design circuit operates in a high-frequency (HF) band from 3 MHz to 30 MHz, and generates 4.5 kWpk RF power with >90% efficiency. The DRF1510 Class-D FB reference design is available from Microsemi as a kit. This hardware allows designers to readily verify the design principles and the circuit operation at 4.5 kW. The reference design also teaches the critical design circuit of high-power RF FB topologies.

The DRF1510 device is a MOSFET FB hybrid device that has been optimized for efficiency and reduced system cost. It is targeted at HF industrial, scientific, and medical (ISM) markets. The DRF1510 device contains four gate drivers and four power MOSFETs, and it can generate several kilowatt levels of RF power output at frequencies approaching 30 MHz. Higher power levels can be achieved by combining multiple modules. Please contact Gui Choi at gchoi@microsemi.com if you have any technical questions.

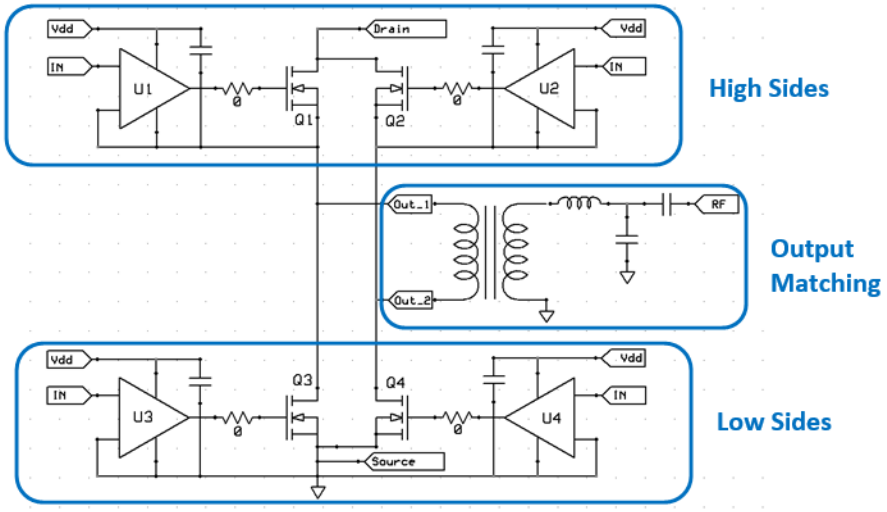
2.1 Theory of Operation

The DRF1510 Class-D FB circuit includes high-side drivers, high-side MOSFETs, low-side drivers, low-side MOSFETs, an output transformer, and an output matching circuit.

Class-D FB topology uses two pulse signals which are 180° out of phase with each other and can provide RF output power of 4.5 kWpk at 13.56 MHz with maximum efficiency of 93%.

The following illustration shows a simplified representation of the full-bridge circuit of the DRF1510 device.

Figure 1 Simplified Full-Bridge Circuit



As shown in the previous drawing, the input pulse signal provides gate drive power to MOSFETs Q1/Q4 simultaneously, and another input pulse signal provides gate drive power to MOSFETs Q2/Q3. These two MOSFET pairs are driven 180° out of phase. When Q1/Q4 are on, Q2/Q3 are off; when Q1/Q4 are off, Q2/Q3 are on. The square-wave transition starts at 0 V and quickly rises to the +HV, remains at +HV for one half cycle, and then quickly returns to 0 V.

Because the two MOSFETs are on and off simultaneously, the timing-related parameters, such as Time Delay and Rise/Fall Time, are very important and use the same length cables for connecting to PCBs.

The output matching circuit consists of a transformer (T1), a series inductor (L1), a shunt capacitor (C1), and a series capacitor (C2). This network provides a sinusoidal RF signal into the 50 Ω load. The output matching circuit (T1, L1, C1, and C2) is optimized to provide a sine wave at the 50 Ω Load.

In Class-D FB topology, the control and stability of the high-side switches (Q1/Q2) is a critical point. At nodes Out_1 and Out_2, there will be a high-voltage square wave which will have fast leading edges. These abrupt transitions can induce enough image current through the stray capacitance of the input circuits to cause Q1/Q2 to conduct too soon or too late. This can cause cross conduction of Q1/Q4 and Q2/Q3.

To make clean input signals by reducing the stray capacitance, input transformers should be made with the smallest multi-apertures possible. For more information, see the parts list in Appendix III.

3 Circuit Description

High-definition images of the circuit description for this product are available in the attached Adobe Acrobat files. To view or print the information, double-click the attachment icons to the left of the figure titles.

The following illustration shows the circuit layout of the DRF1510. It consists of the following sections: the pulse generation with pre-drive amplifier, input circuit containing the high- and low-side isolation, high-voltage circuit, the RF output matching circuit, and a cooling system with metal case.

Figure 2 Reference Design Circuit Diagram

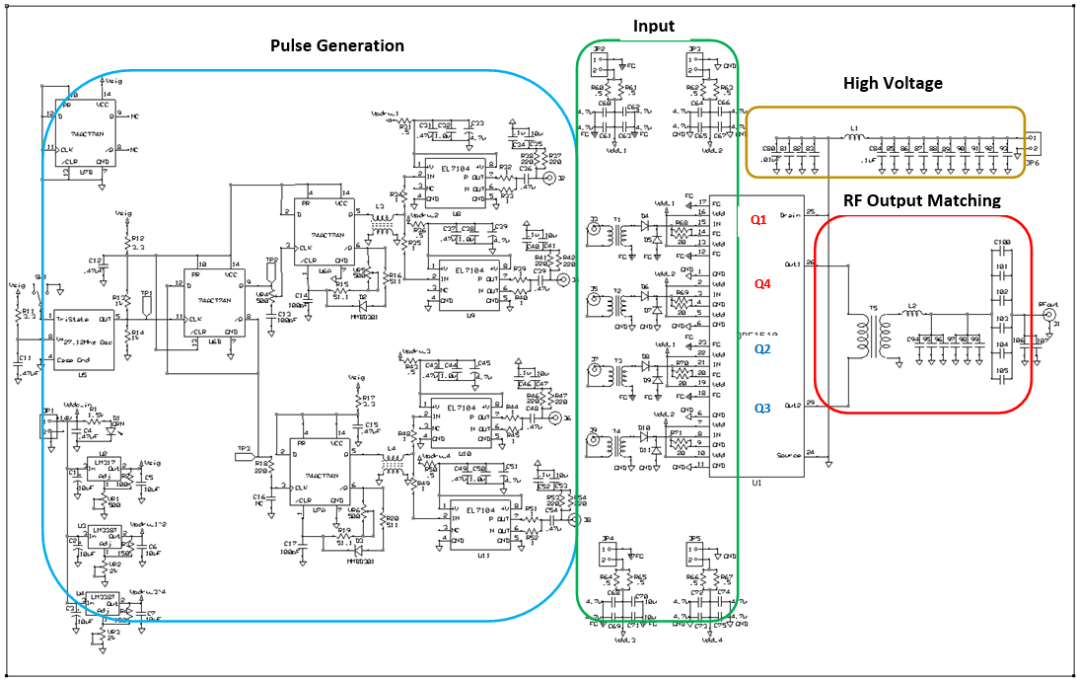
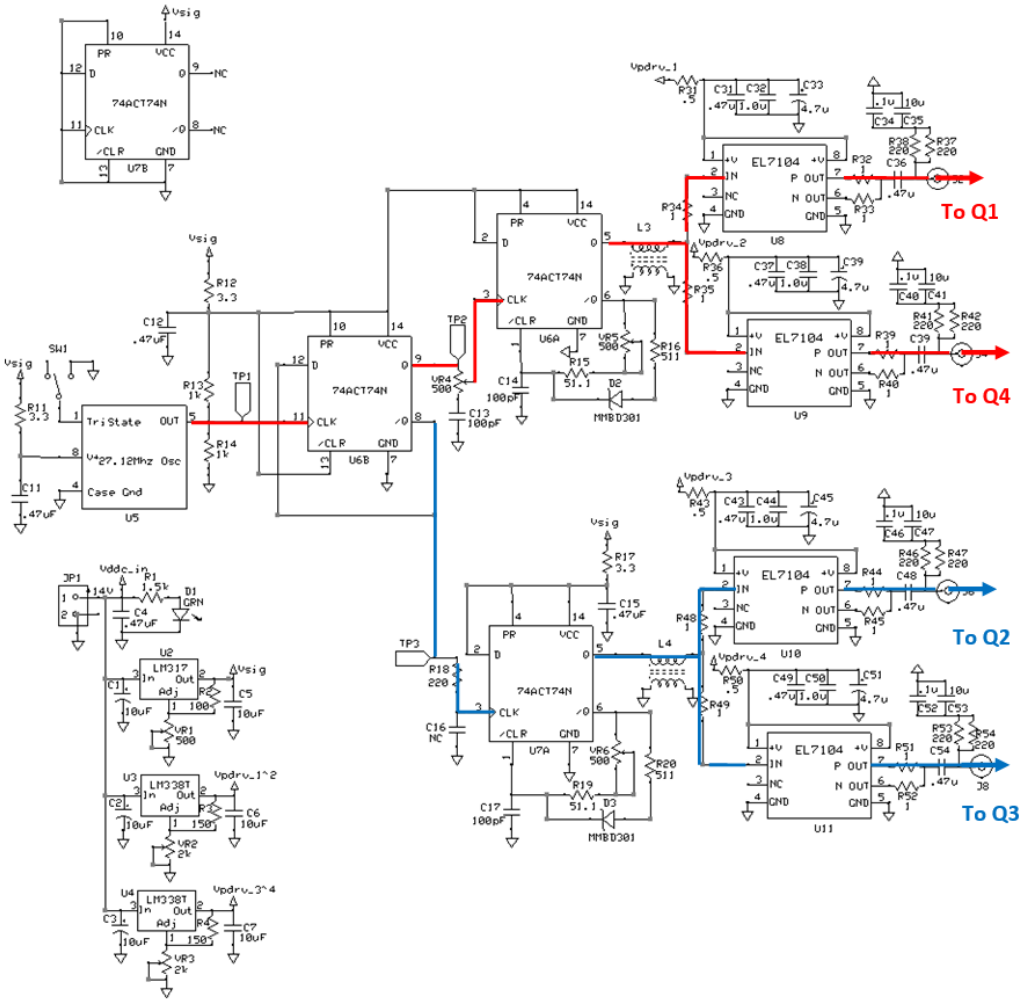
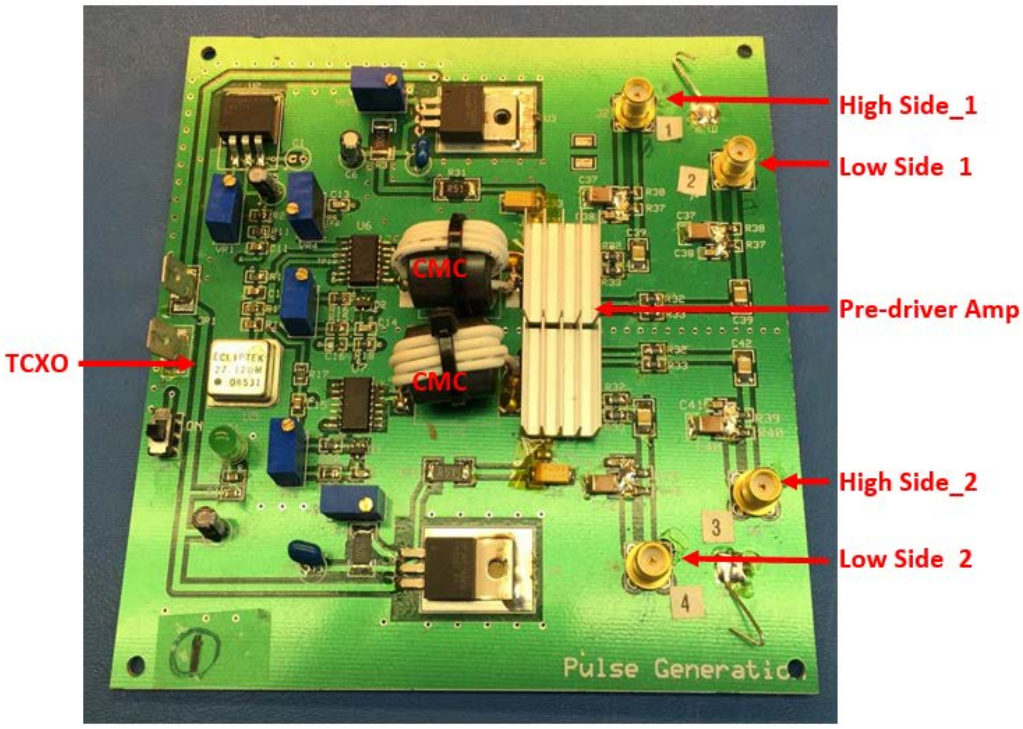


Figure 3 Pulse Generation with Pre-Drive Amplifier



The following image shows the pulse generation and pre-driver amplifiers of the DRF1510 reference design (the blue section of the full schematic of Figure 3). This pulse generation circuit generates two pairs of input signals that are 180° out of phase to the input of the DRF1510 FB module, using a 27.12 MHz crystal oscillator (TCXO (U5)) is used.

Figure 4 Pulse Generation with Pre-Drive Amplifier Circuit



This integrated circuit generates a 27.12 MHz, 50% duty-cycle signal that is applied to U6B pin 11. The flip-flop U6B is configured as a divide-by-two circuit. This provides a 13.56 MHz square wave at Pins 9 and 8. These two signals are exactly 180° out of phase. The precision of this relationship is critical for the proper operation of the full-bridge topology. U6B pin 9 applies one phase to the high-side pulse-width generator and a similar path for the low-side pulse-width generator. U6B pin 9 is an RC network (VR4 and C13). This network is used to ensure that the high-side and low-side drives are 180° out of phase.

Given that these two circuit paths perform exactly the same, we will only follow the circuit path for the high-side pre-driver. U6A of the high-side pulse-width generator is a flip-flop circuit configured to produce a pulse with time duration less than the one-half cycle time of the 13.56 MHz clock signal. For the DRF1510 FB at 13.56 MHz, the pulse widths occupy an approximate range of 20 nS to 35 nS. These pulses are then applied to U8 and U9, and the input transformers are set (red path); U10 and U11 are set to another input transformer (blue path).

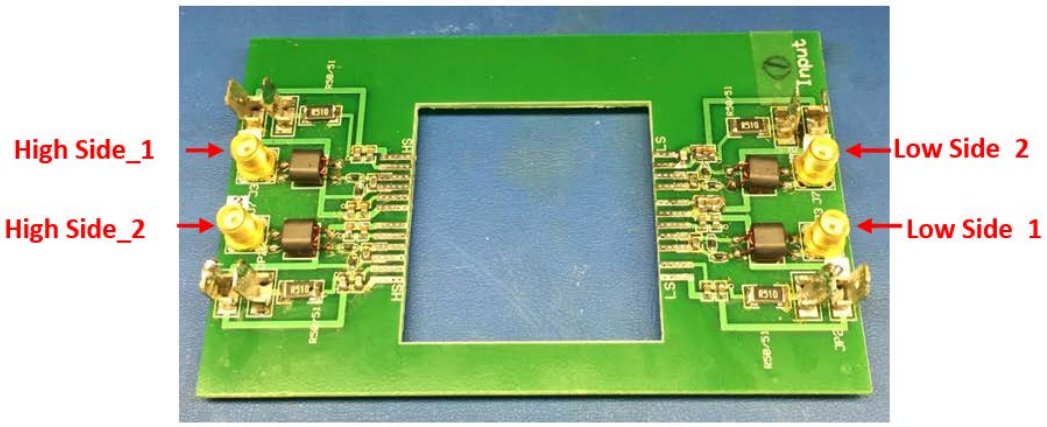
As shown in the previous image, the pulse generation circuit consists of a 27.12 MHz signal (TCXO(U5)). It has a frequency-down conversion to 13.56 MHz and is split into two 180° out-of-phase signals and applied to one-shot circuit of IC (U6A, and U7A). The phase can be adjusted to a 180° out-of-phase setting by using VR4. The pulse widths are set to 20 nS–35 nS using a potentiometer (VR5 and VR6, respectively). Common Mode Choke (CMC) L3 and L4 are necessary to eliminate EMI and RFI. These two CMCs are made of 43 core material and 50 Ω coaxial cable (alternatively, they can use SMD-type CMC). The output signal at L3/L4 is split into two signals, and each signal goes to the respective pre-drive amp (U8, U9, U10, U11). EL7104s is from Intersil, and

these pulse signals are connected to the output connectors (J2, J4, J6, J8) through snubber circuits with resistors and capacitors. The TCXO voltage is 4 VDC–4.5 VDC supplied from the DC regulation circuit using a regulator (U2), and the pre-drive amp voltage is 11 V–12 V from the regulator. This voltage is supplied from the adjustable regulator (U3 and U4). It is highly recommended to use an EMI shielding box covering the entire PCB and the low-level control circuits to avoid any interference from the output section.

3.1 Input PCB

In the following image, there are four RF connectors for four pulse signals from the pulse generation PCB: two pulse signals are for the high side (yellow and blue) and two are for the low side (pink and green). These pulse signals are applied to the input transformers, which are used for floating the ground for the high side; the signals are then applied to the Schottky diodes and input load resistors. This provides an improved rise-and-fall time of the control pulses. The operating voltage for the four drivers is set at 10 VDC–12 VDC. The waveform captured at the output of the pulse generation is shown in Figure 6.

Figure 5 Input PCB with Input Transformers



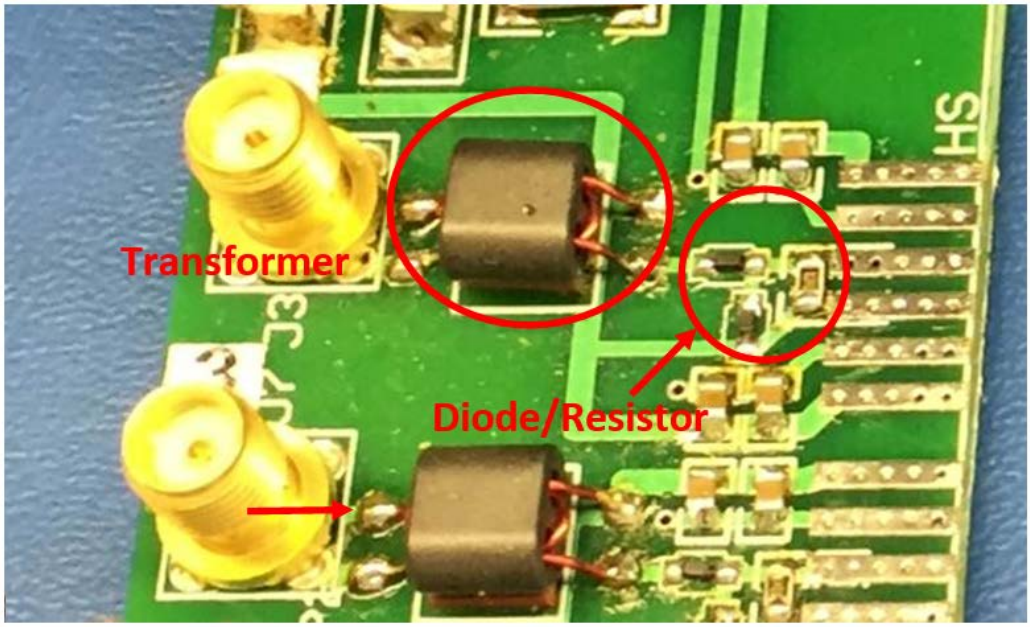
The signals travel through approximately 10 inches of 50 Ω coaxial cable with EMI wrap and are then applied to the primary of T1, T2, T3, and T4 in Figure 5.

Figure 6 Waveform at Inputs of the Input PCB

3.2 Input Circuit

The following image shows the input circuit with the input transformers.

Figure 7 Input Transformer

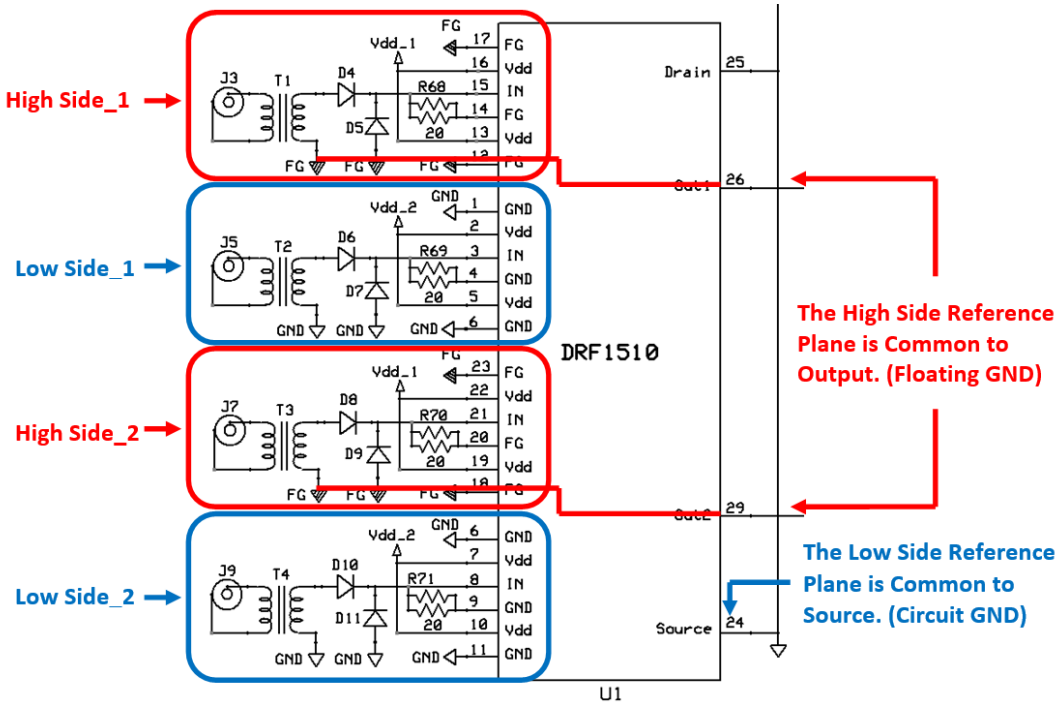


It is highly recommended that the turns ratio of the primary and secondary is 1:1 for less loss and distortion, and the input transformers are constructed with ferrite core material 43 and 24 or 26 enameled-coil wire. This is a critical and electrically sensitive component. The size of the ferrite core is approximately 0.275 inches by 0.250 inches with a multi-aperture-cores shape.

It is essential that the construction of the transformers minimizes both the stray capacitance and the leakage inductance. The peak positive voltage at the output is approximately 4 V, and the pulse width is approximately 20 nS–35 nS. This is a critical component; special care must be taken during design and construction in order to ensure low leakage inductance and low stray capacitance. Schottky diodes and input load resistors are used for clamping the overshooting and undershooting at the input ports.

The two isolation transformers on the high side are illustrated in the image above. As previously described, the high-side reference plane (F_Gnd) is not at ground DC or AC.

Figure 8 High-Side and Low-Side Reference Planes



As illustrated in DRF1400 Half Bridge Application Note (AN1817), the single most important and critical circuit detail is that the floating GND (FG) is not a common ground. It is floating at the output of the full-bridge pins 26 and 29 of the DRF1510 device. Also note that the DRF1510 device high-side input pins are all referenced to FG and out pins. In addition, all circuit components contained within the red rectangles in the illustration above are also at this potential and must be isolated from the circuit ground.

The input pre-driver for the high side and the low side are shown in Figure 10. T1 and T2 couple the pre-driver signals for the high side and the low side to the input of the DRF1510 device while isolating the F_Gnd from the system ground. With a high drive-voltage signal at T1, high-side switch pins 16 and 17 are in a saturated switch condition. At the same time, the low-side drive is at a 0 V state and the low-side switch is in an off condition (pins 16 and 15). This alternating pattern of drive signals generates a square wave high-power signal at pin 16.

3.3 RF Output Matching

The image below shows the DRF1510 device's RF output matching circuit for 13.56 MHz 4.5 kW at 400 V with a 50 Ω load. To increase DC-to-RF efficiency, first reflect the optimum output impedance 10+j9 into the MOSFET drains and provide a match to the 50 Ω load. The circuit must also be resonant at 13.56 MHz. This circuit is illustrated in the red block of Figure 10.

Figure 9 Output Matching with Power Transformer

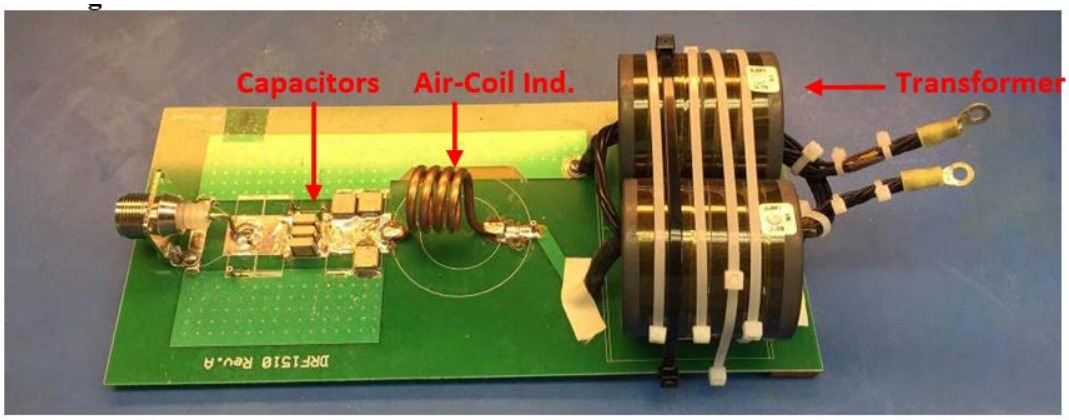
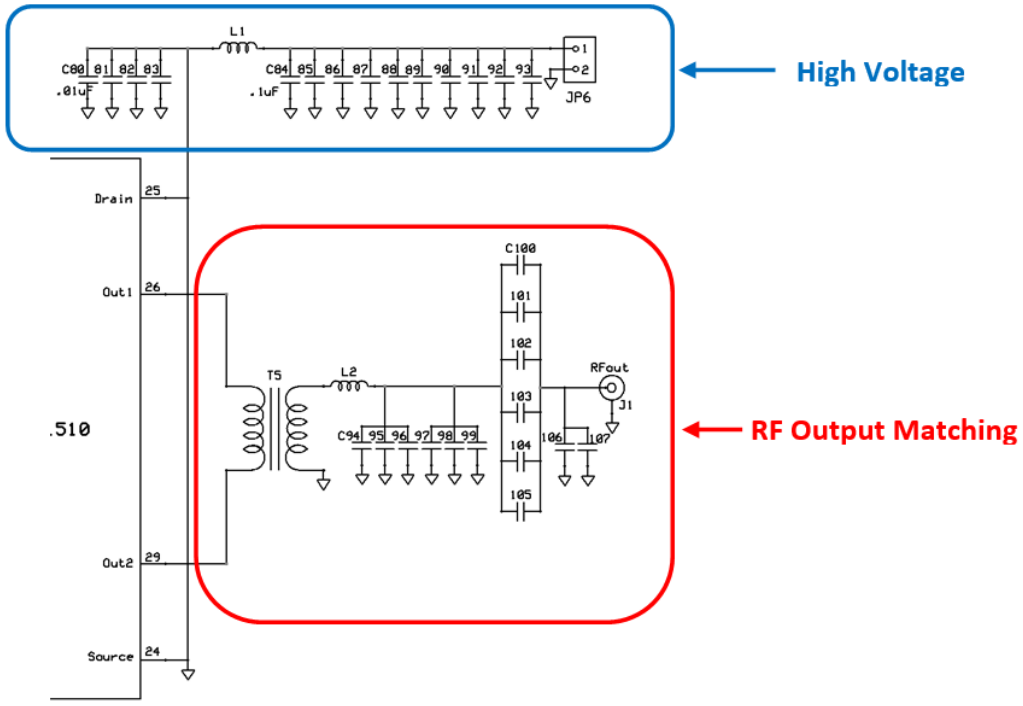


Figure 10 RF Output Matching Circuit and High-Voltage Circuit



The matching circuit consists of a power transformer for combining two outputs, serial air coil inductor L2, shunt capacitors C94 through C99, series capacitors C100 through C105, and shunt capacitors C106 through C107.

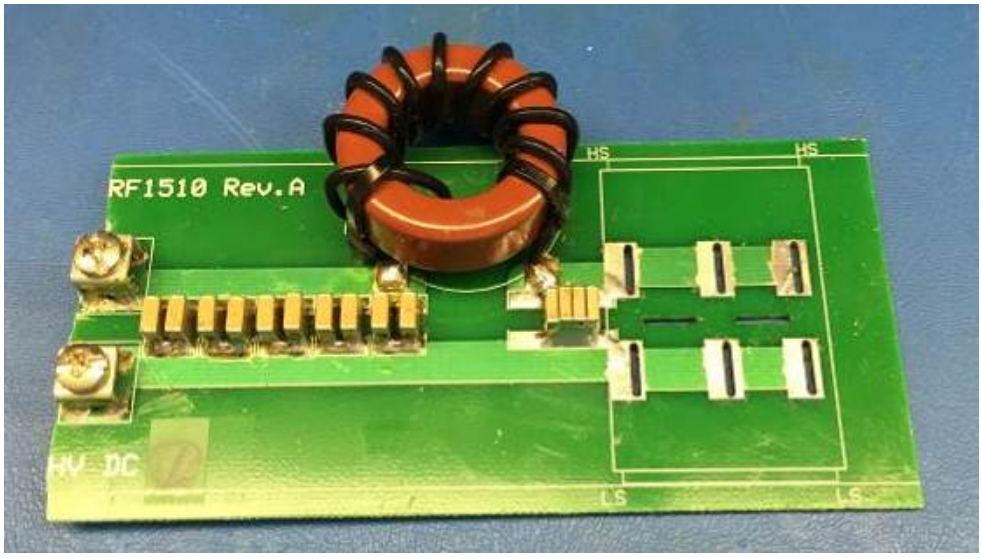
The power transformer (T5) is constructed with 12 pieces of toroid ferrite cores material 67, and the wire is six pieces of 14 AWG (10 inches long for the primary and 14 inches long for the secondary section).

The air-coil inductor has four turns; it is constructed with 6 AWG solid bare copper and the ID is 0.8 inches. For the RF output matching, it is highly recommended to use high-RF-power multilayer capacitors (100E series from ATC).

3.4 High Voltage

The following image shows the high-voltage circuit of the DRF1510 device. It illustrates the high-voltage circuit that supplies DC voltage to the MOSFETs with four capacitors (0.01 µF/1 kV) in parallel (C80 to C83), located between the device's drain and source.

Figure 11 High-Voltage Circuit



This circuit is illustrated in the blue block in Figure 10 (it is also in the PCB layout). These capacitors provide a very low-inductance, high-capacitance bypass component and also minimize overshoots on the drain waveform. It is mounted vertically on the drain and source pads of the PCB. All RF circuit components must support voltages over 1000 V and power levels of several kilowatts.

The capacitors are critical circuit elements for ensuring overall system performance and minimizing the peak-ring voltage at the common pin 16.

The green block of Figure 13 illustrates both the more conventional RF bypassing network and the DC bypass components.

The RF choke is a critical component in the high-voltage circuit, and it eliminates EMI interference on the high-voltage DC line. The RF choke is constructed with metal powder mix #2 and 10 turns of AWG 14 wire.

3.5 Test Setup

The following three images show the DRF1510 reference design's bench set up. The 11 VDC high-side power supplies (Vdd_1/Vdd_2) and the 11 VDC low-side power supplies are on the front panel. The panel has one 14 VDC power supply for the pulse generation and one 13.5 VDC power supply for

the pump and fans. In order to eliminate all EMI signals, use ferrite core material #73 along with all DC wires, which are absolutely essential for stable FB operation. There is also CMC on this power feed.

The HV RF probe is in the lower right. There are two important points to note with respect to the probe attachment: (1) the location of the electrical attachment of the probe tip and the ground, and (2) that a CMC is installed on the probe cable. Failure to connect the HV RF probe in the proper manner will result in excessive high-frequency noise on the signal and will corrupt the accuracy of measurements.

Figure 12 DRF1510 Reference Design Kit

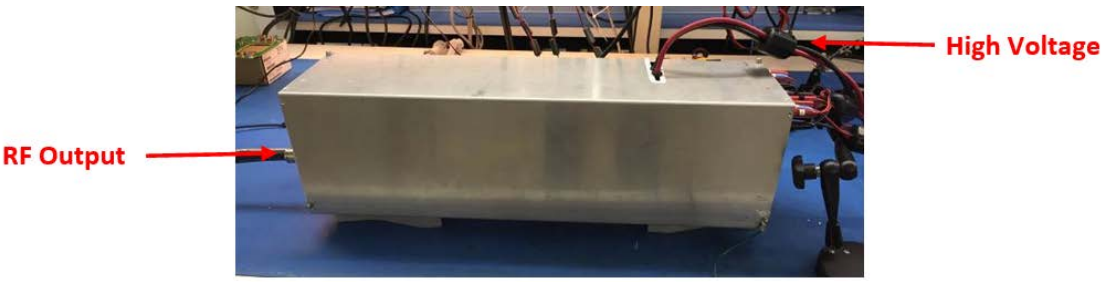


Figure 13 Inside of the DRF1510 Reference Design Kit

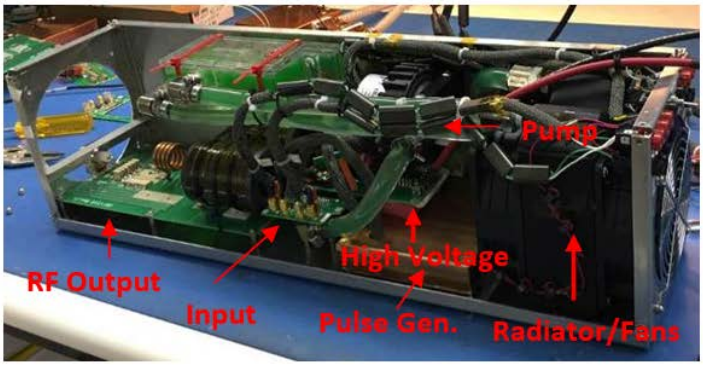


Figure 14 DC voltage and RF Out

3.6 DC Supply

There are power supply circuits for two high-side and two low-side drivers. These supplies are electrically isolated. The high-side ground is floating (F_GND in the schematic), while the low-side is a common ground. The gate driver voltage is set at 11.0 V. It is critical that all DC connections use a CMC set made from Fair-Rite's multi-apertures (ferrite material #73) in order to eliminate conductive noise at the operating frequency. The HV supply circuit consists of an RF choke (L1) and 22 bypass capacitors (C71 through C92). The RFC is made from a T130-2 with 10 turns of 16 AWG, which has approximately 1000 Ω inductive reactance. All capacitors must support over 1 kV, such as AVX 2225 X7R (min. 10% tolerance). It is critical that a CMC (ferrite material #73) along with HV wire are on the high-voltage supply lines in order to eliminate all conductive noise elements.

Primary cooling for the DRF1510 device is provided through a water-cooled heat sink and is constructed with two 184CFM fans, one pump (14 psi max.), and a radiator. The cooling capacity is approximately 500 W, and the heat sink temperature is approximately 40 °C at full power of 4.5 kW. Additional air cooling is provided for PCB components by the AC fan in the upper right.

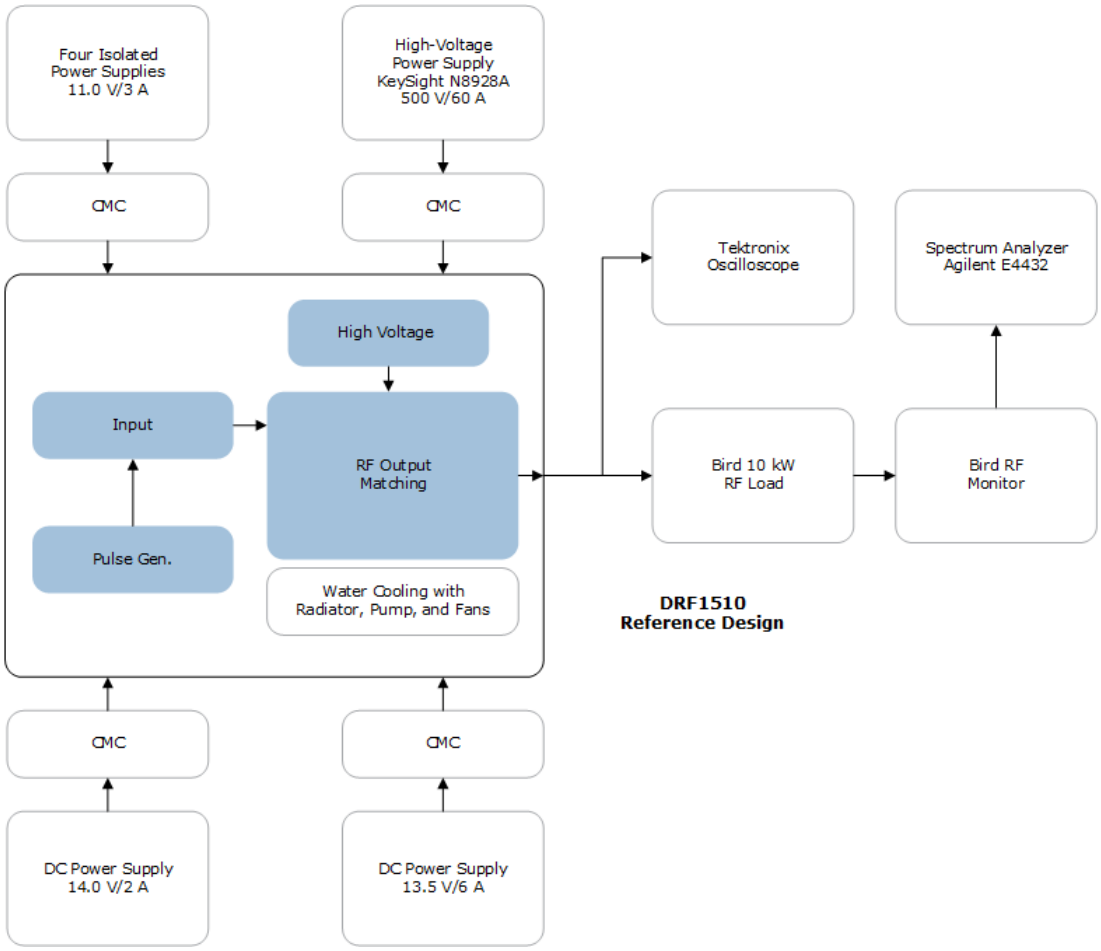
4 Test Result (Data Summary)

This section describes the test result information of the DRF1510 device.

4.1 Test Setup

The following illustration shows the test setup specifications for the DRF1510 device.

Figure 15 Test Setup Diagram



4.2 Test Requirements

All the test results presented in this application note were collected using the equipment configuration illustrated in Figure 15. For the high-side, the DC power supplies should be isolated for the floating ground. The high-voltage supply is varied from 0 V to 500 V in the course of compiling the data.

Note: All power supplies have a CMC (ferrite material #73) on the output leads. All adjustments on the DRF1510 device have been made and checked prior to applying HV power.

Turn on the power supplies, set an HV of 40 V, and allow the device to warm up for at least 30 minutes. Ramp up the HV gradually while monitoring the RF power and waveform at output port U1, ensuring that all functions are normal before increasing the HV supply. If the RF power and/or drain waveform becomes unstable, shut down all power supplies and identify the error before resuming testing.

4.3 Test Results

The following table shows the test results of the RF output/efficiency versus V_{DD}, including the DC voltage supply, MOSFET drain current, and power out with efficiency.

Table 1 Typical Performance Data

HV (V)	I_{HV} (A)	RF P_{OUT} (W)	Efficiency (%)
50	1.95	73	77.9
100	3.1	280	90.3
150	4.51	631	93.3
200	6.02	1127	93.6
250	7.60	1778	93.6
300	9.20	2558	92.7
350	10.82	3548	93.7
395	12.25	4518	93.4

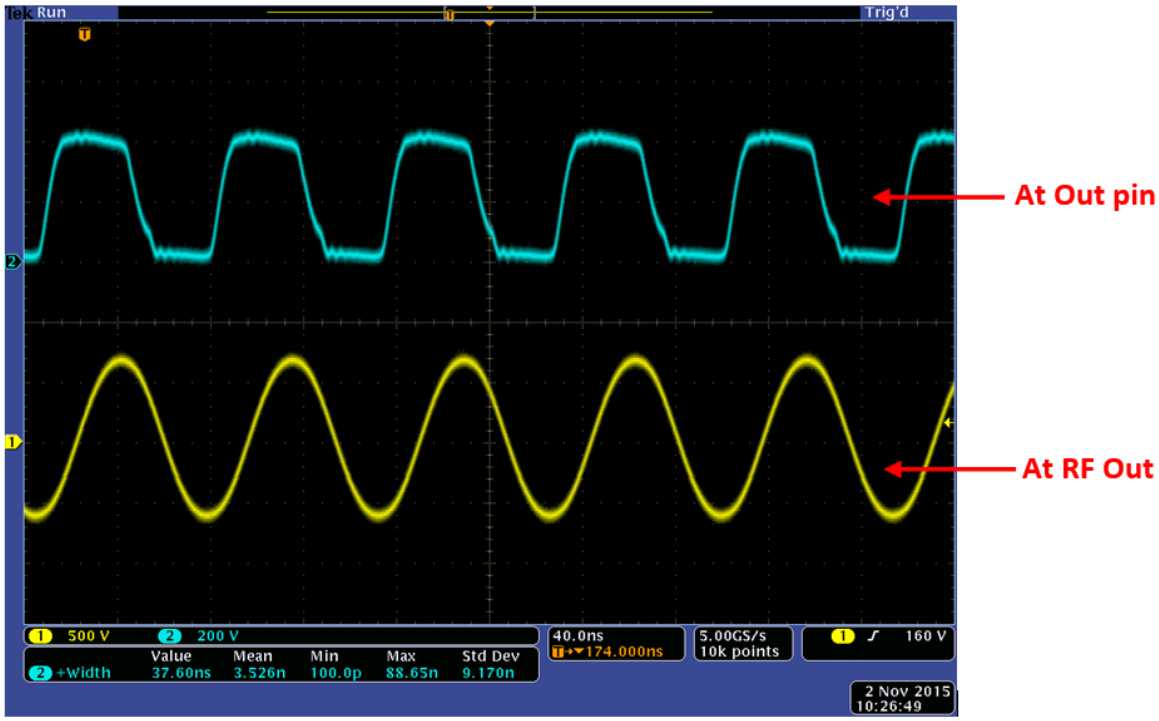
This step-by-step process should be observed from low power levels to a maximum of 4.5 kW. The variation of efficiency and P_{OUT} over 10 minutes is charted in Figure 18 and the drain HV (V_{DD}) versus P_{OUT} is charted in Figure 17. Efficiency is calculated using the RF power output and DC input power of the power MOSFET. The efficiency is valued at 13.56 MHz. The drain efficiency (η) of the reference design is typically 93 % at 4.5 kW. More RF power can be achieved by further tuning and optimizing the output circuit and improving the cooling capacity.

4.4 Performance Charts

The following graphs show the performance of the DRF1510 device.

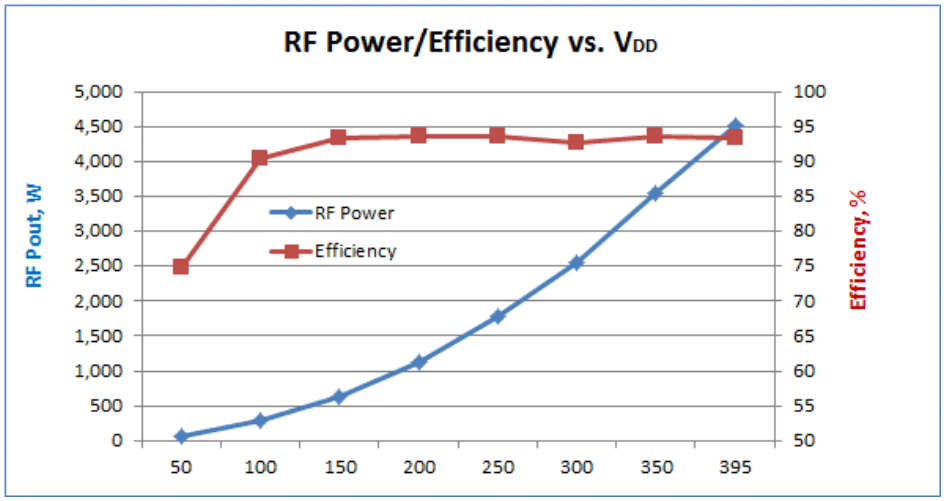
The image below shows the drain waveform and sinusoidal signal at RF Out.

Figure 16 Drain Waveform and Sinusoidal at RF Out



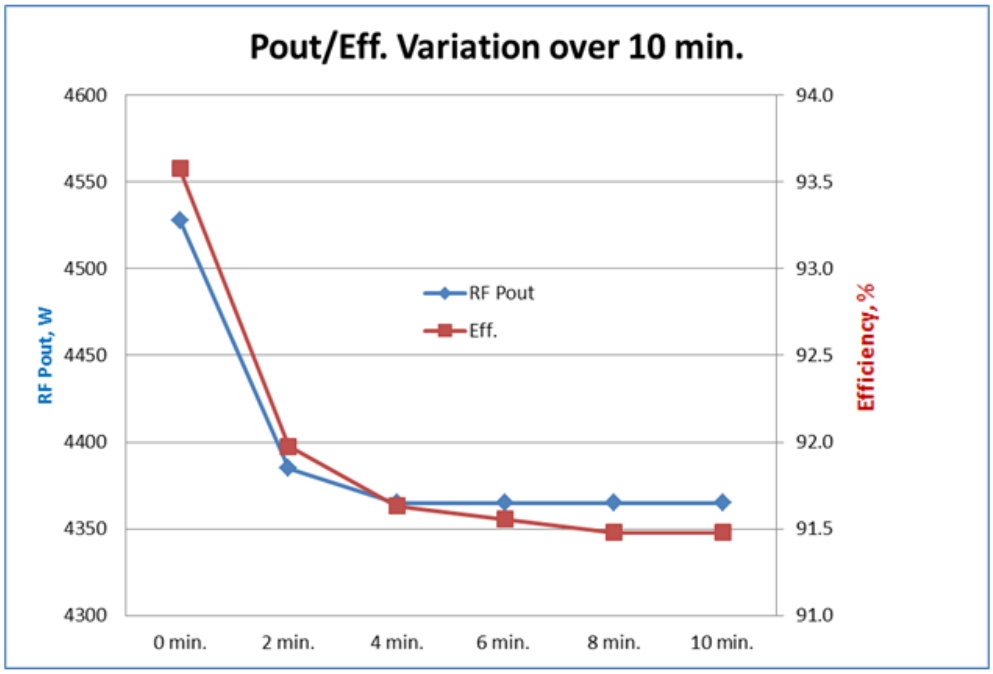
The graph below illustrates the RF P_{OUT}/efficiency variation for 10 minutes to check the system's stability. Measurements were taken up to 4.5 kW (HV from 50 V to 400 V) and the reference design kit was run for 10 minutes.

Figure 17 RF P_{OUT}/Efficiency vs. V_{DD}



The following graph shows the power out versus efficiency variation over 10 minutes of the DRF1510 device.

Figure 18 RF P_{OUT}/Efficiency Variation



5 Conclusion

This application note provides technical information for designing a 4.5 kW Class-D Full-Bridge RF Generator operating in 13.56 MHz without an external cooling system (such as a water chiller). Critical aspects of circuit design are also included. Among these critical aspects are the isolation of high-side and low-side drivers, the suppression of conductive noise, and the bypassing of capacitors on the drain HV and inside the cooling channel with radiator/pump and fans. The power transformer in the RF output board is a critical component for full-bridge operation in combining two output ports. A Microsemi DRF1510 Hybrid was used to overcome layout parasitic, simplifying the design and providing a single low-cost, high-efficiency RF generator. Transformer design can be further optimized to eliminate peaking as shown in the V_{DS} waveforms. The reference design minimizes design time by allowing an engineer to evaluate the performance into a 50 Ω load. Please contact Gui Choi at gchoi@microsemi.com if you have any technical questions.

6 Appendix I: PCB Layout

PCB size:

- RF output: 5.0” W * 10.0” L
- Pulse generation: 4.7” W * 5.0” L
- Input: 3.2” W * 5.0” L
- High voltage: 2.0” W * 4.9” L

PCB: FR-4, 65 mil T

Figure 19 RF Output Diagram

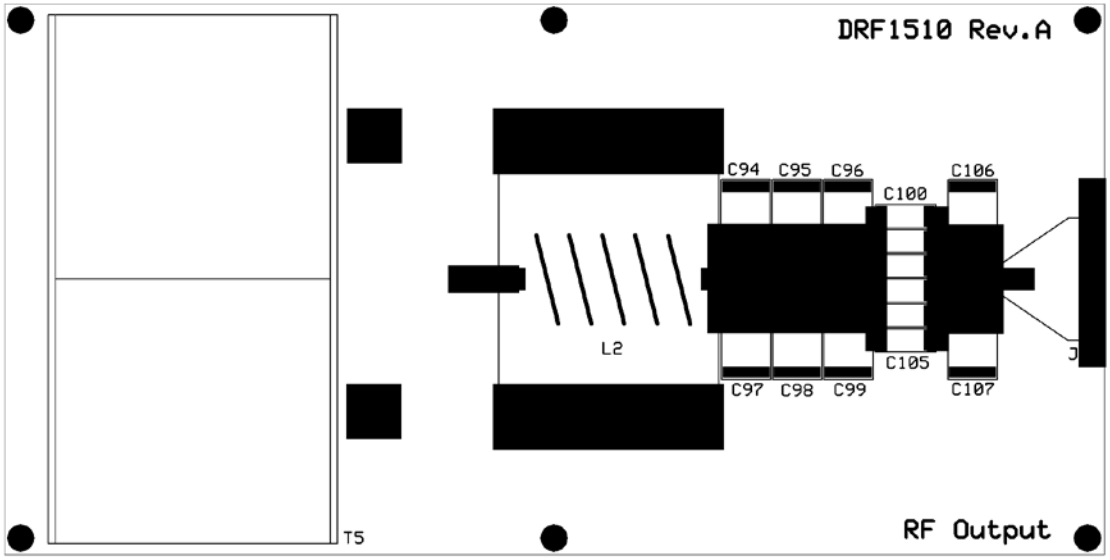
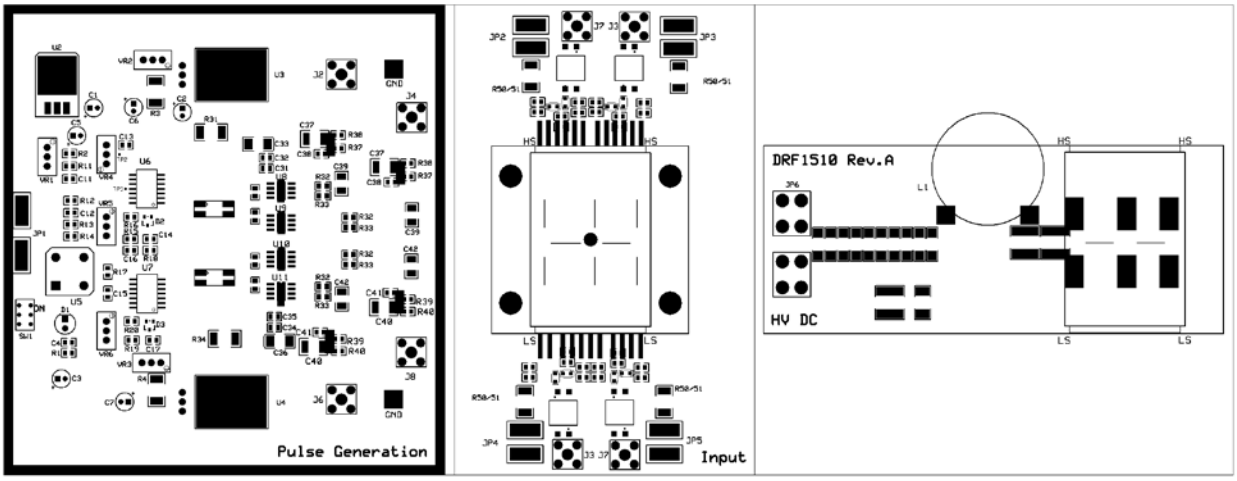


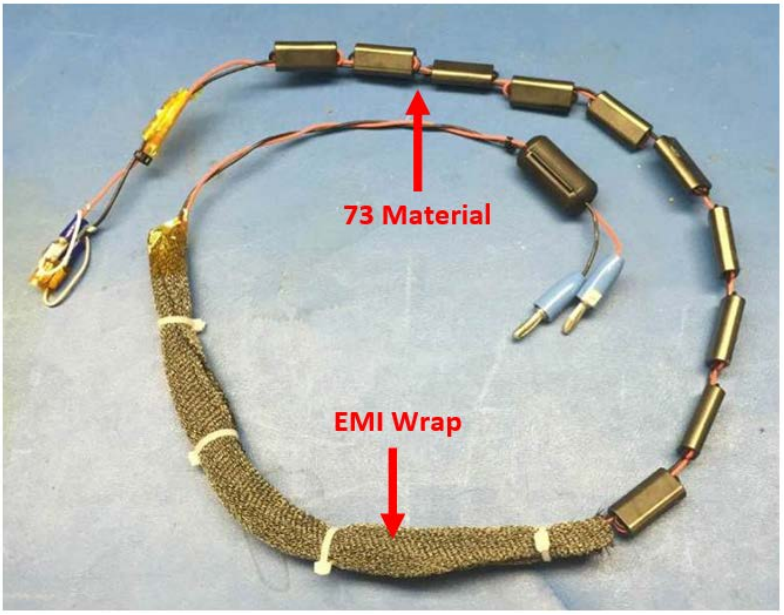
Figure 20 Pulse Generation, Input, and High-Voltage Diagrams



7 Appenix II: DC Bias for High-Side and Low-Side Driver

The following image shows the ferrite material and the EMI wrap of the DRF1510 device.

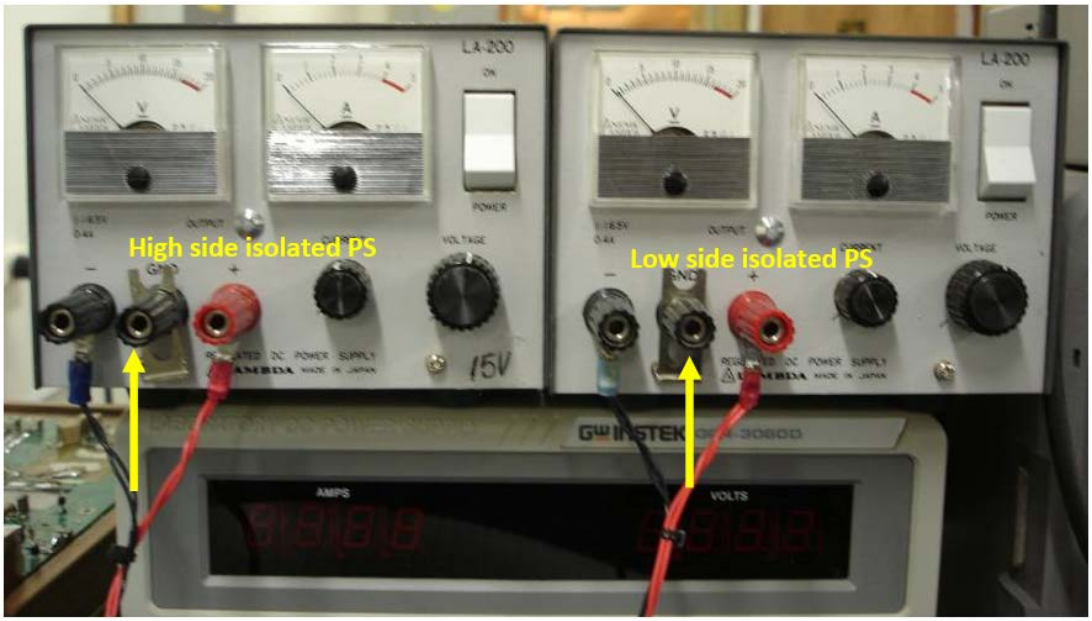
Figure 21 Ferrite Material and EMI Wrap



The following image shows the connected high-side and low-side PS.

Note: Do not connect GND to negative terminals for high- and low-side driver to make an isolated PS.

Figure 22 High-Side and Low-Side Isolated PS



8 Appendix III: Parts List

The following table shows the parts list of the DRF1510.

Table 2 Parts List

Part ID	Description	Size	Manufacturer	Manufacturer's Part Number
U1	DRF1510		Microsemi	DRF1510
C1–3, 5–7	10 µF/50 V (elec. cap)	5*11		
C60–75	4.7 µF/50 V (elec. cap)	0805		
C34, 40, 46, 52	0.1 µF/25 V (cer. cap)	0805	AVX	0805C104KAT2A
C4, 11, 12, 15, 31, 37, 43, 49	0.47 µF/50 V (cer. cap)	0805	AVX	08055C474K4T2A
C36, 39, 48, 54	0.47 µF/50 V (cer. cap)	1210	AVX	12105C474KAT2A
C13, 14, 17	100 pF/50 V (cer. cap)	0805	Murata	GRM2165C1H101JA01D
C33, 39, 45, 51	4.7 µF/35 V (tant. cap)	6032-28	AVX	TAJC475K035R
C32, 38, 44, 50	1.0 µF/50 V (cer. cap)	0805	Taiyo Yuden	GMK212BJ105KG-T
C80–83	0.01 µF/2 kV	2225	AVX	2225GC103KAT1A
C84–93	0.1 µF/1 kV	2225	AVX	2225AC104KAZ1A
C94	47 pF	3838	ATC	100E470KT
C95	47 pF	3838	ATC	100E470KT
C96	22 pF	3838	ATC	100E220KT
C97	20 pF	3838	ATC	100E200KT
C98	10 pF–27 pF	3838	ATC	Tuning with 100E series
C99	10 pF–27 pF	3838	ATC	Tuning with 100E series
C100	47 pF	3838	ATC	100E470KT
C101	47 pF	3838	ATC	100E470KT
C102	47 pF	3838	ATC	100E470KT
C103	82 pF	3838	ATC	100E820KT
C104	22 pF	3838	ATC	100E220KT
C105	10 pF–27 pF	3838	ATC	Tuning with 100E series
C106	0 pF–10 pF	3838	ATC	Tuning with 100E series
C107	0 pF–10 pF	3838	ATC	Tuning with 100E series
R1	1500 Ω	0805	ROHM	MCR10EZHF1501
R2	100 Ω	0805	VISHAY	CRCW0805100RJNEA
R3–4	150 Ω	2512	VISHAY	CRCW2512150RJNEG
R11, 12, 17	3.3 Ω	0805	SUSUMU	RL1220S-3R3-F
R13, 14	1000 Ω	0805	ROHM	MCR10EZHF1001
R15, 19	51.1 Ω	0805	Panasonic	ERJ-6ENF51R1V
R16, 20	511 Ω	0805	ROHM	MCR10EZHF5110
R31, 36, 43, 60–67	0.5 Ω	2512	Panasonic	ERJ1TRQFR51U

Part ID	Description	Size	Manufacturer	Manufacturer's Part Number
R32–35, 44, 45, 48, 49, 51, 52	1 Ω	2512	Vishay	CRCW25121R00FNEG
R18, 37, 38, 41, 42, 46, 47, 53, 54	220 Ω	0805	ROHM	MCR10EZHF2200
R68–71	20 Ω	0805	Vishay	
VR1, 4–6	POT 500 Ω, 1 W	3/8" sq	Vishay	T93YA501KT20
VR2, 3	POT 2000 Ω, 1 W	3/8" sq	Vishay	T93YA202KT20
D1	LED, green	5 mm	Panasonic	LN31GPH
D2	30 V/200 mW (Schottky diode)	SOT23	ON Semiconductor	MMBD301LT1G
D3	30 V/200 mW (Schottky diode)	SOT23	ON Semiconductor	MMBD301LT1G
D4–11	Schottky diode	SOD323F	NXP	PMEG4002EJ
L1	RF choke		Micrometals Belden	T130-2 8073(10TURNS)
L2	4T air coil			6 AWG, 4TURNS
L3, 4	CM choke		Fairchild Belden	2643375102 83265(4TURNS)
T1–4	Input transformer (1:1)		Fair-Rite Alpha	2843002302 20 AWG
T5	Output transformer (1:1)		Fair-Rite Alpha	5967003801 8073
U2	LM317	14SOP		LM317
U3, 4	LM338T	TO-220	National	LM338T/NOPB
U5	27.12M TCXO		Ecliptek Co.	EP1100HSTSC-27.120M
U6, 7	Dual flip flop	14SOP	TI	SN74ACT74NSR
U8–11	EL7104	8LDSOIC	Intersil	EL7104CSZ
SW1	Slide switch SPDT		E-Switch	EG1271A
J1	RFout port	HN female		
J2–9	SMA, PCB mount	Straight		
JP1–5	DC terminal		Keystone	4902
JP6	DC terminal		Keystone	8191
Pump	RP-1250		Koolance	
Fan	12038HBK-184	184CFM	Koolance	
Radiator	HX-120XC		Koolance	

9 Appendix IV: Test Equipment Required

The required equipment for testing the reference design kit is described in the following table.

Table 3 Required Test Equipment

Equipment	Spec	Quantity	Remark
HV PS	0 V–500 V, 15 A	1	Keysight N8928A or equivalent
Driver PS	0 V–15 V, 4 A	4	Keysight E3642 or equivalent
Pulse PS	0 V–15 V, 2 A	1	GWInstek 3060D or equivalent
Fan/pump	0 V–15 V, 6 A	1	GWInstek 6030 or equivalent
DC wire for HV	AWG8	1 pair	"Y" terminal and wire with CMC
DC wire for driver	AWG20	4 pairs	"Snap" terminal and wire with ferrite material #73
DC wire for pulse generation	AWG20	1 pair	"Snap" terminal and wire with ferrite material #73
DC wire for fan/pump	AWG20	1 pair	
Spec analyzer	E4411 or equivalent		
RF power meter/load	10 kW	1	Birds SCC711300041/4421 or equivalent
RF coax cable	LMR400	1	5 feet long with HN_male connector
Oscilloscope		1	Tektronix or equivalent
HV probe	2 kV	1	P5100A
STD probe	300 V	4	