AM / FM - PLL

Description

The U4280BM is an integrated circuit in BICMOS technology for frequency synthesizer. It performs all the functions of a PLL radio tuning system and is controlled by I^2C bus. The device is designed for all frequency synthesizer applications of radio receivers, as well as RDS (**R**adio **D**ata **S**ystem) applications.

Features

- Frequency range up to 150 MHz
- Pre-amplifier for AM and FM
- Fine tuning steps: AM ≧ 1kHz
  FM ≧ 2 kHz
- Two programmable 16-bit divider, adjustable from 2 to 65535
- Reference oscillator up to 15 MHz
- 5 programmable switching outputs, 4 are open drain outputs up to 15 V
- Phase detector with separate outputs for AM and FM
- Controlled via I^2C bus

Ordering Information

Extended Type Number	Package	Remarks
U4280BM-B	DIP20	
U4280BM-BFL	SO20	

Block Diagram

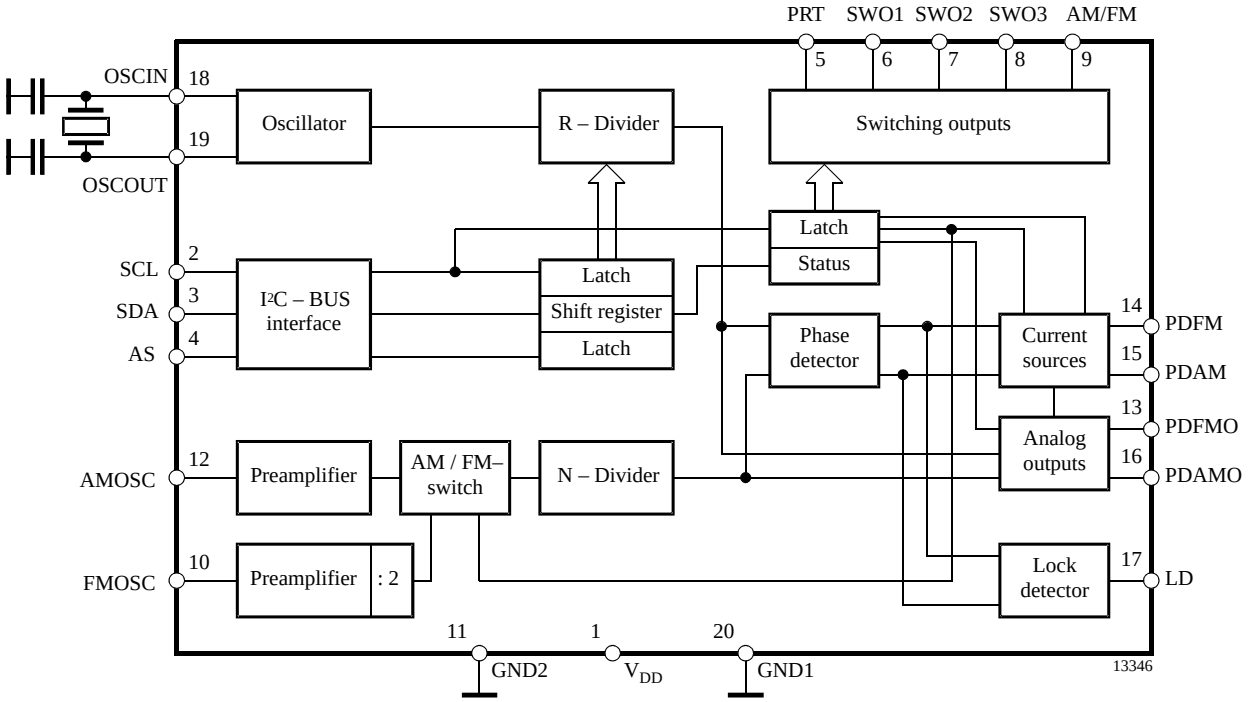


Figure 1. Block diagram

Pin Description

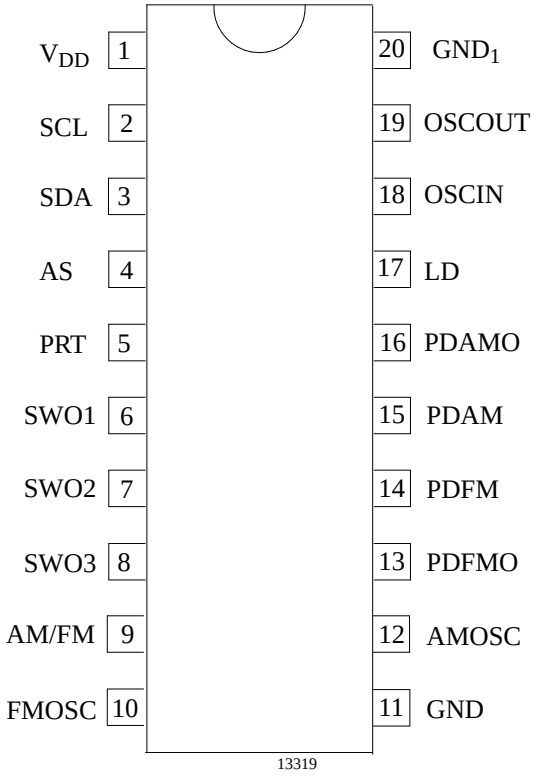


Figure 2. Pinning

Pin	Symbol	Function
1	V_{DD}	Supply voltage
2	SCL	I^2C bus clock
3	SDA	I^2C bus data
4	AS	Address selection
5	PRT	Switching port
6	SWO1	Switching output 1
7	SWO2	Switching output 2
8	SWO3	Switching output 3
9	AM/FM	Switching output AM/FM
10	FMOSC	FM oscillator input
11	GND2	Ground 2 (analog)
12	AMOSC	AM oscillator input
13	PDFMO	FM analog output
14	PDFM	FM current output
15	PDAM	AM current output
16	PDAMO	AM analog output
17	LD	Lock detect
18	OSCIN	Oscillator input
19	OSCOUT	Oscillator output
20	GND1	Ground 1 (digital)

Functional Description

The U4280BM is controlled via the 2-wire I^2C bus. For programming there are one module address byte, two subaddress bytes and five data bytes.

The module address contains a programmable address bit A 1 which with address select input AS (Pin 4) makes it possible to operate two U4280BM-B in one system. If bit A 1 is identical with the status of the address select input AS, the chip is selected.

The subaddress determines which one of the data bytes is transmitted first. If subaddress of R-divider is transmitted, the sequence of the next data bytes is DB 0 (Status), DB 1 and DB 2.

If subaddress of N-divider is transmitted, the sequence of the next data bytes is DB 3 and DB 4. The bit organisation of the module address, subaddress and 5 data bytes are shown in figure 2

Each transmission on the I^2C bus begins with the “START”-condition and has to be ended by the “STOP”-condition (see figure 3).

The integrated circuit U 4283 BM has two separate inputs for AM and FM oscillator. Pre-amplified AM signal is directed to the 16 bit N-divider via AM/FM switch, whereas (pre-amplified) FM signal is first divided by a fixed prescaler (:2). AM/FM switch is controlled by software. Tuning steps can be selected by 16 bit R-divider. Further there is a digital memory phase detector. There are two separate current sources for AM and FM amplifier (charge pump) as given in electrical characteristics. It allows independent adjustment of gain, whereby providing high current for high speed tuning and low current for stable tuning.

Bit Organization

	MSB							LSB
Module address	1	1	0	0	1	0	0/1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Subaddress (R-divider)	X	X	X	X	0	1	X	X

Subaddress (N-divider)	X	X	X	X	1	1	X	X

	MSB							LSB
Data byte 0 (Status)	PRT	SWO1	SWO2	SWO3	AM/ FM	PD ANA	PD POL	PD CUR
	D7	D6	D5	D4	D3	D2	D1	D0

Data byte 1	2^{15}	R-divider	2^{8}

Data byte 2	2^{7}	R-divider	2^{0}

Data byte 3	2^{15}	N-divider	2^{8}

Data byte 4	2^{7}	N-divider	2^{0}

	LOW	HIGH
AM/FM	FM-operation	AM-operation
PD - ANA	PD analog	TEST
PD - POL	Negative polarity	Positive polarity
PD - CUR	Output current 2	Output current 1

Figure 3.

Transmission Protocol

	MSB LSB										
S	Address A7 A0	A	Subaddress R-divider	A	Data 0	A	Data 1	A	Data 2	A	P

	MSB LSB								
S	Address A7 A0	A	Subaddress N-divider	A	Data 3	A	Data 4 A	A	P

S = Start P = Stop A = Acknowledge

Figure 4.

Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pin 1	V_{DD}	–0.3 to +6	V
Input voltages	Pins 2, 3, 4, 10, 12, 18 and 19	V_I	–0.3 to V_{DD} + 0.3	V
Output currents	Pins 3, 5, 6, 7, 8 and 9	I_O	–1 to +5	mA
Output drain voltage	Pins 6, 7, 8 and 9	V_{OD}	20	V
Ambient temperature range		T_{amb}	–25 to +85	°C
Storage temperature range		T_{stg}	–40 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	160	K/W

Electrical Characteristics

V_{DD} = 5 V, T_{amb} = 25°C, otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 1	V_{DD}	4.5	5.0	5.5	V
Quiescent supply voltage	Pin 1	I_{DD}		6.0	11.6	mA
FM input sensitivity	R_G = 50 Ω Pin 10					
	f_i = 30 to 60 MHz	V_I	50			mV
	f_i = 70 to 120 MHz	V_i	25			mV
	f_i = 120 to 130 MHz	V_i	50			mV
AM input sensitivity	R_G = 50 Ω Pin 12					
	f_i = 0.4 to 35 MHz	V_i	25			mV
Oscillator input sensitivity	R_G = 50 Ω Pin 18					
	f_i = 0.1 to 15 MHz	V_i	100			mV
Adjustable divider [1]			2		65535	
Switching output, PRT	Pin 5					
	I_H = 1 mA	V_{OH}	V_{DD} – 0.4			V
	I_L = 1 mA	V_{OL}			0.4	V
	I_L = 0.1 mA	V_{OL}			0.1	V
SWO1 to SWO3, AM/FM (open drain outputs)	Pins 6 to 9					
	I_L = 1 mA	V_{OL}			0.4	V
	I_L = 0.1 mA	V_{OL}			0.1	V
LD (open drain)	Pin 17					
	I_L = 1 mA	V_{OL}			0.4	V
Phase detector						
PDFM	Pin 14					
	Output current 1	I_{O1}	±400	±500	±600	µA
	Output current 2	I_{O2}	±100	±125	±150	µA
PDAM	Pin 15					
	Output current 1	I_{O1}	±75	±100	±100	µA
	Output current 2	I_{O2}	±20	±25	±30	µA
Analog output	Pins 14 and 15 to V_{DD}	$I_{13,16}$		–1	–2	mA
	Pins 14 and 15 to GND	$I_{13,16}$	0.1	0.5		mA
I^2bus inputs SCL, SDA	H input voltage, Pins 2 and 3	V_{IH}	3		V_{DD}	V
	L input voltage, Pins 2 and 3	V_{IL}	0		1.5	V
Output voltage	I_{SDAH} = 3 mA	V_O			0.4	V
Clock frequency	Pin 2	f_{SCL}	0		110	kHz
Bus timing						
Rise time SCL, SDA		t_r			1	µs
Fall time SCL, SDA		t_f			300	ns
“H” phase SCL		t_H	4			µs
“L” phase SCL		t_L	4.7			µs
Waiting time START		t_{wSTA}	4			µs
Set up time START		t_{hSTA}	4			µs
Set up time STOP		t_{sSTA}	4.7			µs
Set up time DATA		t_{sDAT}	250			ns
Hold time DATA		t_{hDAT}	0			µs

[1] FM input frequency is additionally divided by two (Pin 10).

Bus Timing

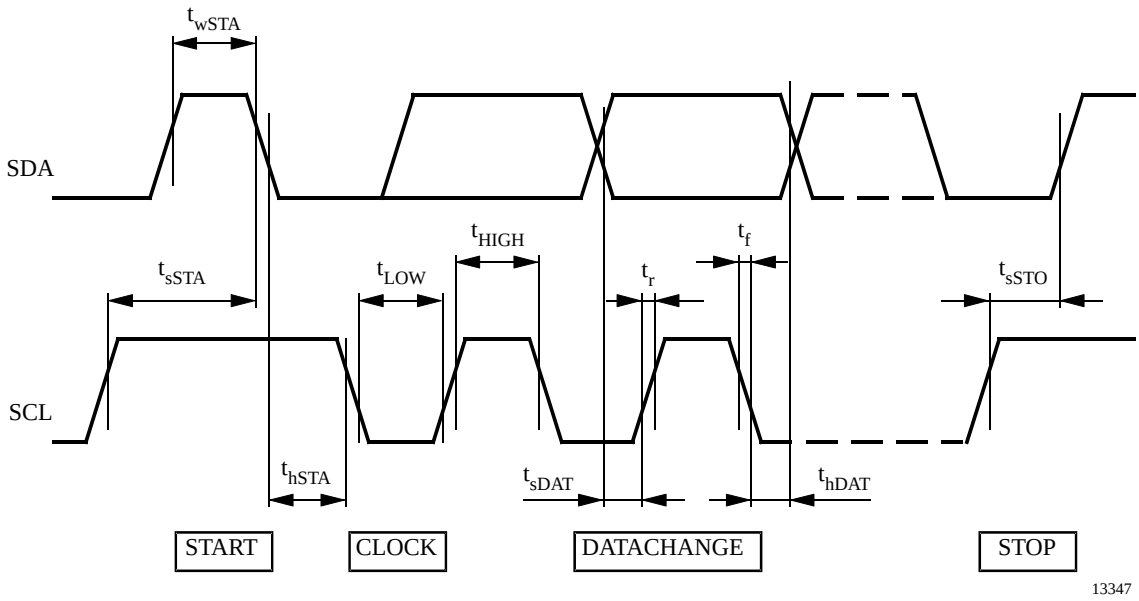


Figure 5. Bus timing

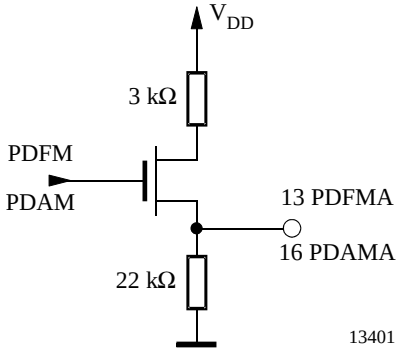


Figure 6. Analog outputs PDFMA, PDAMA

Application Circuit

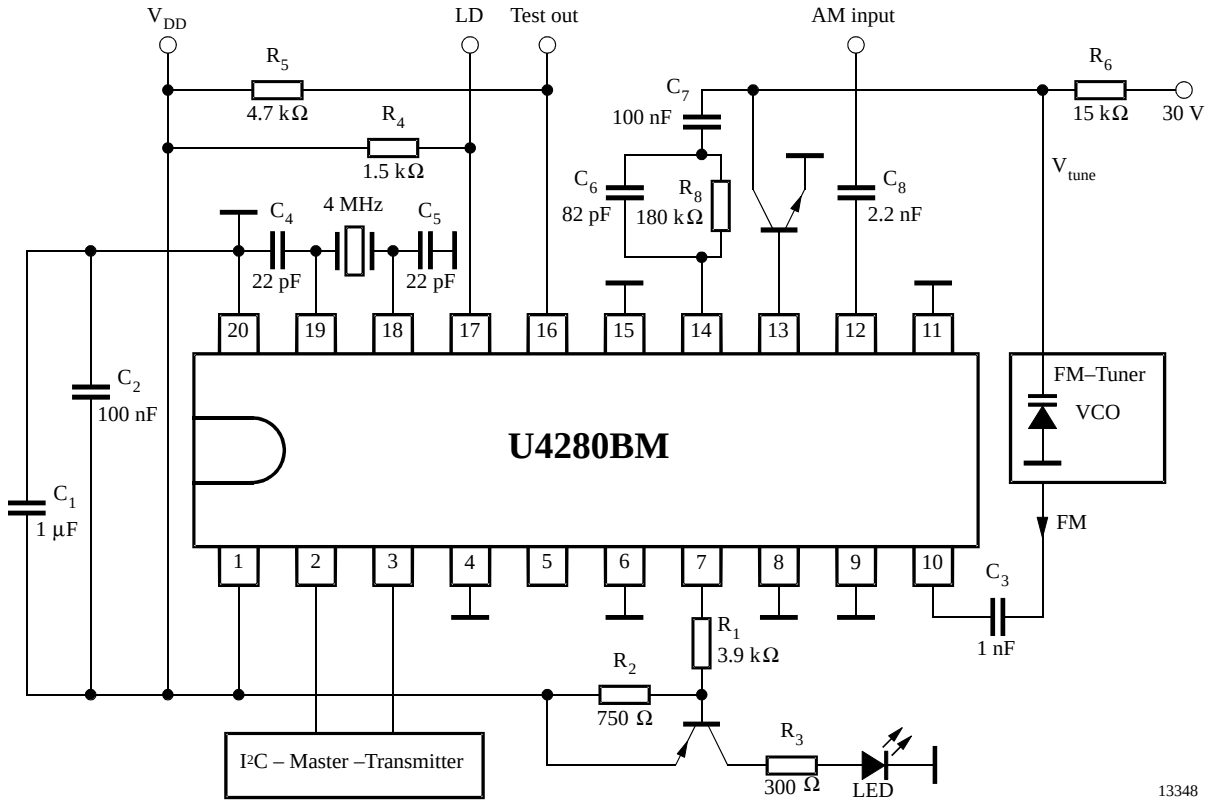
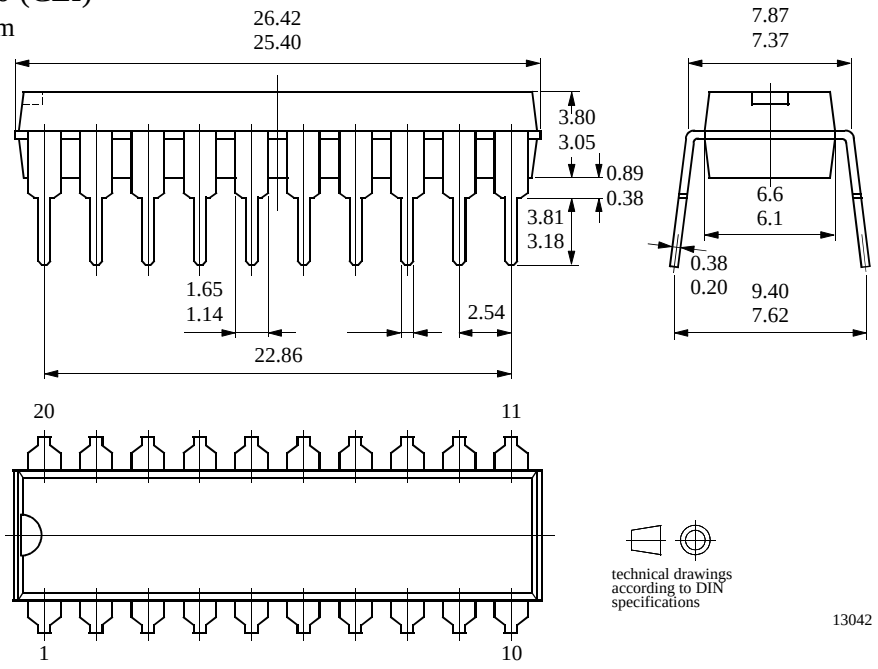


Figure 7. Application circuit

Package Information

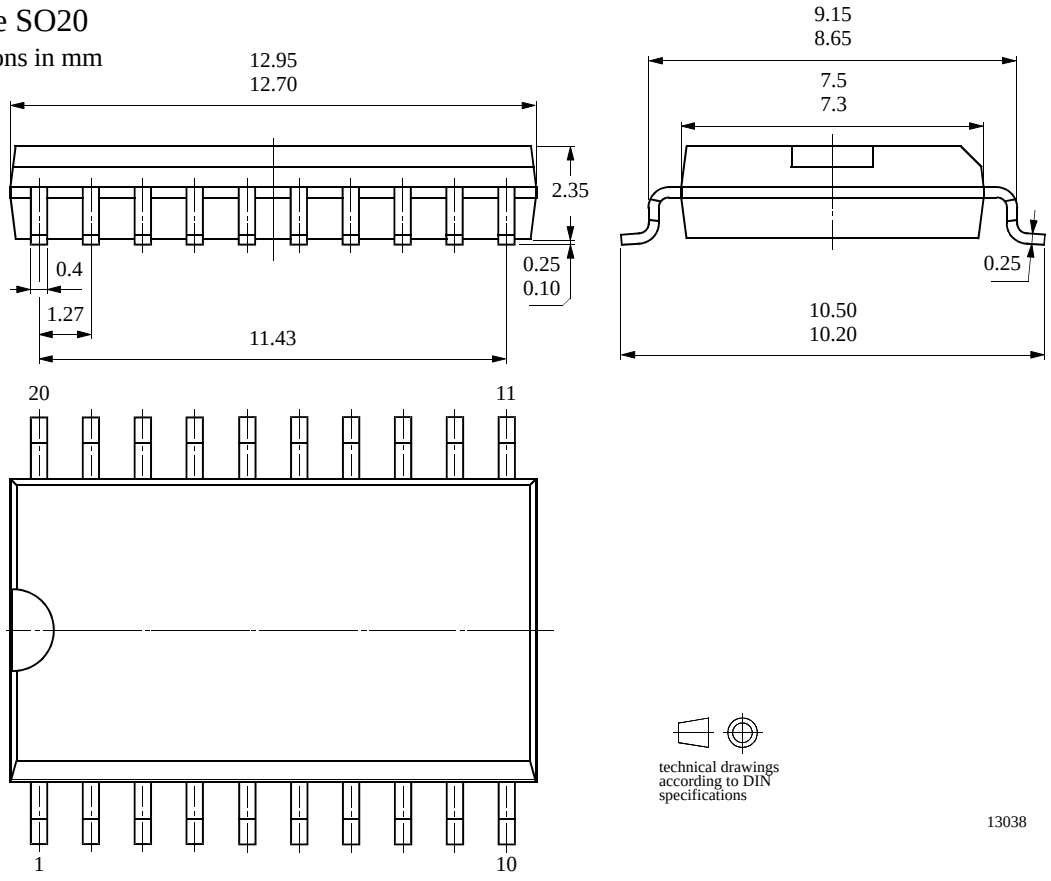
Package DIP20 (CEI)

Dimensions in mm



Package SO20

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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