Third harmonic filtered 13.56 MHz Push-Pull Class-E Power Amplifier

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***Abstract*—A novel energy efficient power amplifier designed to drive an inductive load is presented in this paper. In this power amplifier the standard Class-E topology is extended towards a Push-Pull configuration with frequency tripling. By tuning the load network to the third harmonic of the switching frequency, gate driving losses have been decreased. Opportunities and restrictions related to the fundamental change in operation of the amplifier are clarified. Calculations and simulation results are shown as well as experimental results. Furthermore a circuit is presented to further reduce the required power of the gate drive circuit.**

I. Introduction

EFFICIENCY improvement is of vital importance to be prepared for a sustainable future. In this context important issues are the increasing awareness of environmental issues and the higher cost of and demand for energy. An option to meet this efficiency increase requirement is the use of resonant power converters. The Class-E type is a resonant converter that becomes increasingly valuable as a high frequency solid state power converter in both the dc-to-ac (inverter), as the dc-to-dc (voltage converter) configuration. This is due to its simple design and potentially high efficiency. In this framework a Class-E Power Amplifier (PA) in a Push-Pull (PP) configuration is designed, which is aimed to provide 300 Watts of output power (P_{out}) with a high efficiency ($\eta = 90\%$). The load for which the converter is designed consists of a 11 Ω resistor (R_{load}) in series with a 2.2 μH inductor (L_{load}).

The Class-E switching mode tuned PA was first introduced by the Sokals in [1], and offered a new way of highly efficient power amplification. The idea behind this class of power amplifiers is that it should operate without switching losses. This demand can only be satisfied if the voltage across the switching device returns to zero prior to the turn on, and the current through the drain source capacitor has returned to zero before the turn on instant. The converter works under so-called nominal operation if these two conditions are met. Presuming these conditions, together with an infinite Quality factor (Q) in the load circuit, rejecting all unwanted harmonics and by the use of ideal components, a 100% efficiency can be reached.

The first paper analytically describing the Class-E operation was written by Raab [2]. He defines the Class-E principle as "A tuned power amplifier composed of a single pole switch and a load network". From this definition it becomes clear that the load network should be tuned to the required output frequency. Further analytical design methods were developed [3], [4] to determine the behavior of the amplifier with a finite feed inductor instead of an ideal current source. In the case of an ideal current source all the Radio Frequency (RF) content is rejected, the input inductor is therefore called Radio Frequency Choke (RFC).

The PP configuration of the Class-E PA was mentioned in [2]. A variation on this design was presented by Chen *et al.* [5] to reduce the higher harmonic content in the load compared to the conventional Class-E. Chen proposes to use a symmetrical arrangement of one inductor and one capacitor in the load network, thereby further reducing the total number of used components.

Previously implemented Class-E PA, of comparable output power and with the same output frequency of 13.56 MHz (f_o), can be found in [6], [7] and [8]. In [6] a 400 Watt PA is presented which has an efficiency (η) of 84% and a peak voltage across the MOSFET ($\hat{v}_{ds}$) of 362 Volt. For this design an input power of 12 Watts is needed to drive the gate of the MOSFET. In [7] and [8], a 1 KW PA is implemented with an efficiency of 85 and 86% respectively. When delivering 300 Watts of power they have an efficiency of 85 and 95% respectively. The remark that needs to be made here is that all three amplifiers were designed for a 50 Ω load impedance, which is substantially higher than the 11 Ω of the PA presented here, resulting in lower currents and therefore a higher efficiency. Choi [8] however makes the mistake to exclude the required power to drive the gate in the efficiency calculation, thereby resulting in a very high efficiency (95%) at low power levels. In [7] the required gate driving power is 45 Watts. This high number is due to the combination of a large gate capacitance, 15 V gate voltage and the high switching frequency (f_{sw}). To avoid losses of this magnitude in the gate driver, this paper proposes a combination of two solutions i.e. third harmonic filtering and resonant gate driving.

Intentionally filtering out one higher harmonic of the switching frequency in the load network has not yet been tried in a conventional Class-E PA. Looking at the design assumptions stated in [1], this is because the RFC input inductor is chosen sufficiently large to act as a source of substantially constant current. In the Class-D topology this principle has been used before [9]; but no power loss reduction in comparison to base harmonic operation is stated.

A lot of resonant gate driving circuits have been presented in the last decades [10]–[13]. All these circuits aim to retrieve as much energy as possible out of the input capacitance (C_{iss}) when turning the MOSFET off. Ideally it is possible to operate

the resonant gate driver circuit without losses i.e. with a balanced energy exchange mechanism between the gate of the MOSFET and a passive circuit. Main differences between the mentioned topologies are the number of active components, their switching sequences, and the way in which the retrieved energy is stored.

The PA delivers a 13.56 MHz (f_o) High Frequency (HF) voltage to the load and it does this with the switches operated at one-third of the resonant frequency, i.e. 4.52 MHz (f_{sw}), to reduce the switching losses. An extra feature to further reduce the power consumption of the amplifier is the charge exchange mechanism with which the gates of the MOSFETs are driven. The opportunities and restrictions in comparison with conventional Class-E amplifiers will be explained and experimental results are presented.

This paper is organized as follows. Firstly, the final design of the proposed amplifier together with the idealized waveforms is presented in section II. Next, the model analysis and simulation results are shown in section III. Then in section IV different types of gate driving circuitry are explored and the most suitable type for this application is chosen. In section V the design procedure for the required inductors is pointed out. The experimental results will be shown and analyzed in section VI. Finally the conclusions and recommendations are stated in section VII and VIII respectively.

II. Converter Design

In order to find the optimal converter for this specific application, other resonant converter topologies (Class-D [14], F [15], and E/F [16]) were also investigated. To be able to determine which topology is most suitable, the filtering capability of the load itself must be clarified first. The filtering capability or Quality factor (Q) is defined as the ratio between the stored and the dissipated power of a combination of passive components. For the given combination of L_{load} and R_{load}, Q can be calculated with:

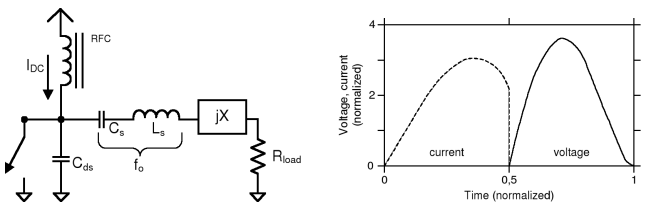
$$Q = \frac{P_{stored}}{P_{dissipated}} = \frac{I^2X}{I^2R} = \frac{2\pi f_o L_{load}}{R_{load}} = 17. \qquad (1)$$

From (1) the conclusion can be drawn that this load circuit has excellent filtering properties.

The first alternative which is investigated is the Class-D converter. The basic principle of the Class-D converter is that complementary switches (Half Bridge, HB) are activated alternately. At the mid-point of these switches a resonant circuit is connected, which is tuned to the switching frequency and ideally filters out all the higher harmonics. This results in a purely sinusoidal signal delivered to the load. The main reason for not using the Class-D concept is that the upper HB MOSFET must be driven using a transformer, causing extra losses, or with a level shifter, causing additional problems due to the relatively high switching frequency. The Class-F and E/F topologies have also been studied, but are unsuitable. Due to the high Q of the load (1), extra filtering (Class-F) is unnecessary, and other harmonics than 13.56 MHz will be rejected (Class-E/F). The Class-E configuration is thought to be the best solution for the given load specification. The motivations for this choice will be explained in the following.

A. Class-E Basic Topology

The Class-E tuning approach has been designed as a time-domain technique with the active device treated as an ideal switch: assume an open circuit during the off state and a perfect short during the on state. The basic Single Stage (SS) Class-E topology and its optimal waveforms are depicted in Fig. 1. To make a time-domain analysis of the circuit possible,



(a) Topology (b) Optimal waveforms [16]

Fig. 1. Class-E amplifier.

restrictions on the waveforms have to be made according to [1]:

1) The rise of the voltage across the MOSFET at turn-off should be delayed until after the drain current has gone to zero.
2) The drain voltage should be brought back to zero at the time of the MOSFET turn-on, Zero Voltage Switching (ZVS).
3) The slope of the drain voltage should be zero at the time of turn-on, Zero Derivative Switching (ZDS).

An amplifier with a switch and a resonant load network which meets these criteria is called *Optimum Class-E*. The criteria can be translated to a set of equations:

$$v_{ds}(t) \mid_{t=kT} = 0, \qquad (2)$$

$$\frac{dv_{ds}(t)}{dt} \mid_{t=kT} = 0. \qquad (3)$$

Where $T = 1/f_{sw}$ is the duration of one period, k is the number of completed cycles and $v_{ds}(t)$ is the drain to source voltage across the switch. The second term (3) ensures that the drain current ($i_d(t)$) is equal to zero at switch on since the drain source capacitance (C_{ds} 1) has been fully discharged by then. To simplify the theoretical analysis of the waveforms the components in the circuit can be considered ideal:

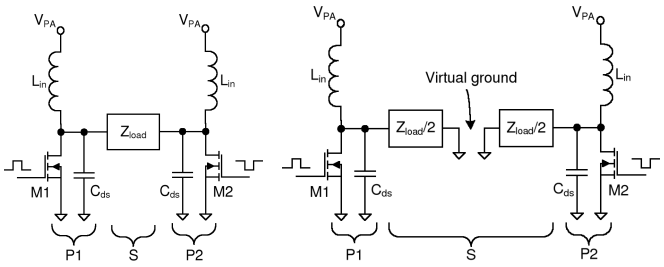
4) The MOSFET has zero saturation voltage, zero saturation resistance, infinite off-resistance and its switching action is instantaneous and lossless.
5) Total shunt capacitance is independent of the drain voltage and is assumed linear.
6) The RFC allows only a constant dc current and has no resistance.
7) There are no losses in the circuit except in R_{load}.
8) The quality factor of the resonant circuit is high enough so that the output current can be considered sinusoidal.

Analysis of the Class-E PA based on this set of assumptions is done in many papers, e.g., [2]–[4], [17] and has been expanded for analysis without constraint 6, i.e. for a finite input inductor [18], [19]. Main problem using these design procedures is that

they are only valid for base harmonic tuning because of (3). If for example the optimum Class-E PA of [18] is switched at 1/3 of the designated frequency, the voltage across the ideal switch starts to resonate at f_o (Fig. 1) depending on the combination of components in the load circuit. This leads to negative voltages across the switch, which is not possible when a MOSFET is used. As a result of this, the PA cannot operate in optimal mode (criteria 1-3) and is therefore called *Suboptimal Class-E*.

B. The Push-Pull Configuration

The PP configuration (Fig. 2a) is chosen for this application for multiple reasons from which filtering is the most important one. By switching the legs of the PA alternating with a duty-ratio $D = 0.5$ and a phase difference between the two legs (ϕ) of π, all the even harmonics of (f_{sw}) generated by P1 will be canceled out by the same signal generated in P2 due to its anti-phase. MOSFET conduction loss, and the resulting thermal stress problems are the second reason to choose for PP. The desired output power of 300 W in combination with an aimed efficiency around 90% means 33 W of loss in total. Given a passive cooling mechanism, distributing losses over more than one switch is desirable.



(a) Push Pull circuit (b) Effect at odd harmonics

Fig. 2. Class-E topologies with resonance circuits S, P1 and P2.

To extend the SS Class-E amplifier towards the PP configuration, the superposition principle is used. For the odd harmonics applies that the ground point at the load network side of the SS equals the midpoint of the PP stage. Two SS Class-E amplifiers with half the impedance of the PP and the load side ground point connected to each other consequently are the equivalent of a PP stage. For the even harmonics this midpoint can be seen as a open circuit, and therefore they will be canceled out. An illustration of this circuit combining principle can be found in Fig. 2b.

In the PP circuit there are three resonant circuits that determine the behavior of the circuit, namely the parallel resonances in the two legs (P1 and P2) and the series load resonance (S), as indicated in Fig. 2a. An extra difficulty is the nonlinear output capacitance of the MOSFETs in P1 and P2. Therefore the total C_{ds} is first determined for an ideal switch, in further simulations it will be replaced with a real MOSFET and additional capacitors.

C. Filtering the third Harmonic

To make third harmonic tuning possible, a few changes to the general Class-E have to be made. The first change is that the input inductors (L_{in}, Fig. 2) must allow the current from the DC-supply to contain the base harmonic and especially the third harmonic of f_{sw}. Another parameter that needs to be accurately determined is the shunt capacitor (C_{ds}), which has to resonate with L_{in} and the load network at f_o during the off state. The last change is an extra buffer capacitor (C_{PA}) to reduce the ripple on the input voltage (V_{PA}) which is a result of the high frequency input current (i_{in}). This capacitor must be a low Equivalent Series Resistance (ESR) type up to f_o to minimize its losses.

D. Series and Parallel Resonant Circuits

To moderate the calculations on the required values of the resonating components, one half of the PP configuration with a virtual ground is used (Fig. 2b). The resulting load impedance for a SS equivalent circuit (3) consists of a resistor ($R_{ss} = R_{load}/2 = 5.5\Omega$) in series with an inductor ($L_{ss} = L_{load}/2 = 1.1\mu H$) and a capacitor ($C_{ss} = 2 \cdot C_s$) which will be determined in section III-A.

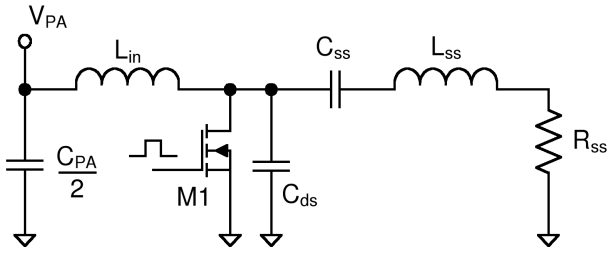


Fig. 3. Total SS Class-E amplifier.

When observing a SS Class-E circuit, two resonance loops can be identified; namely the series resonance of the load network (L_{ss} and C_{ss}), and the parallel resonance of L_{in}, C_{ds} and the rest inductance (L_x) of the load network, essential for subresonant operation (Fig. 1). In order to guarantee subresonant operation, L_x should represent a substantial part of L_{ss}. At the same time a suitable value for C_{ds} and L_{in} is required to maximize the third harmonic content, to reduce the peak voltage, and to minimize the nonlinear effect of the output capacitance of the MOSFET. In the following simulations an optimum for these arguments is found and the final PP amplifier is tested.

III. Model Analysis and Simulations

To determine the optimal component combination, simulations are carried out with the software package LTspice (Linear Technology). First an ideal switch with a fixed capacitance in parallel and a diode anti-parallel to it are used. In section III-B this will be extended to a fixed value in parallel to the nonlinear output capacitance of the MOSFET.

A. Single Stage with Ideal Switch

The ideal switch is a useful component to verify the behavior of a circuit. In the simulations a switch and a diode with an on resistance (R_{on}) of 125 $m\Omega$ [20] are used to

simulate the MOSFET device losses. Various combinations of L_{in}, C_{ds} and L_x are used, to see what combination results in the maximum efficiency.

Because of the already high Q of the load network (1), the series capacitance (C_{ss}) is increased and the inductance ($L_{ss} = L_s + L_x$ Fig. 1) is kept constant. This gives the same result as using an additional inductor L_x, i.e. a subresonant load network.

During the simulations a variable supply voltage (V_{pa}) is used, and the SS output power ($P_{out(ss)}$) is fixed to 150 W. To ensure an sufficiently high lifetime of the MOSFET, the maximum allowed peak voltage across the switch is set to 75% of the maximum voltage across the MOSFET ($\hat{v}_{ds} = 450V$ section III-B). The best combinations of L_{in}, C_{ds} and C_{ss} when using an ideal switch are depicted in table I, the gate drive losses determined in section IV-B (3.4 W in total) are taken into account here. Simulations using higher values for L_{in} are also carried out to reduce the RMS input current but this resulted in too high values for $\hat{v}_{ds}$.

TABLE I
EFFICIENCY AS FUNCTION OF BEST COMPONENT COMBINATIONS

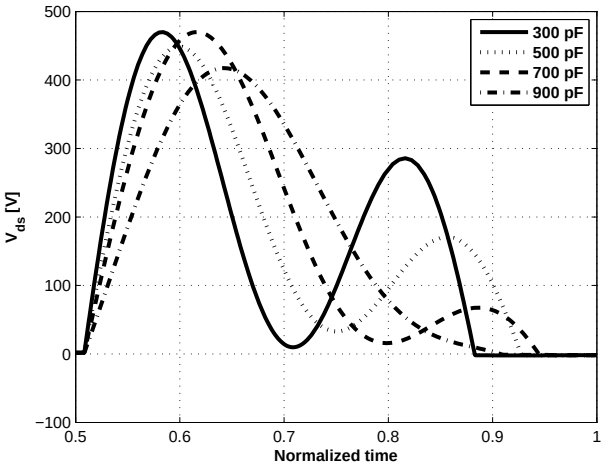
L_{in}[nH]	C_{ds}[pF]	C_{ss}[pF]	V_{pa}[V]	$\hat{V}_{ds}$[V]	η[%]
550	500	130	90	443	96
550	700	130	99	450	96.3
550	500	136	80	440	96.3
550	700	136	74	430	**97**

In figure 4, V_{pa} is fixed to 80 V to illustrate the difference in response and peak voltage. From Fig. 4a it becomes clear that only for a high C_{ds} the derivative of the voltage goes to zero, which is an optimal Class-E demand. A disadvantage is that the third harmonic of the switching frequency is relatively small in this situation, resulting in a lower efficiency as a waveform which does not satisfy the demand. From this it can be concluded that this requirement is inappropriate when tuning for frequency tripling. The high Q of the load network is clearly visible in figure 4b, a small difference in C_{ss} results in a totally different response.

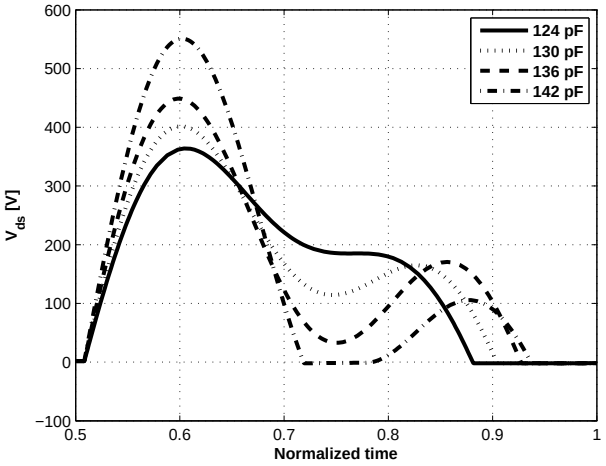
From table I it can be concluded that for this situation the combination of $L_{in} = 550$ nH $C_{ds} = 700$ pF and $C_{ss} = 136$ pF, is the most efficient. The required supply voltage for this combination however is the lowest, resulting in higher currents. The RMS input current (I_{in}) is 6.7 A in this setup, this value is used to determine the loss of L_{in} in section V. With these high currents, the efficiency will be lower if all loss components are taken into account. In section III-C, the final combination of components is determined.

B. MOSFET

A MOSFET is often treated as an ideal switching device with two states, i.e. "on" and "off". In a real-life application however, this is far from true. A MOSFET has parasitic capacitors between each combination of pins, includes an anti parallel diode from source to drain, has conduction losses in its channel resistance ($R_{ds(on)}$), and the gate includes an internal resistance (R_g). The parasitic pin to pin capacitors C_{gs},C_{ds} and C_{gd} all vary nonlinearly depending on the voltage across the device (V_{ds}).



(a) $L_{in} = 550$ nH and $C_{ss} = 136$ pF, C_{ds} as indicated

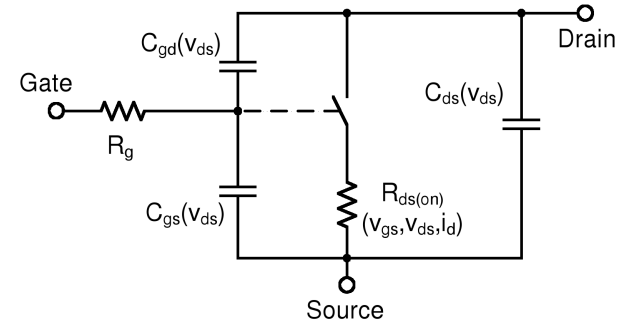


(b) $L_{in} = 550$ nH and $C_{ds} = 500$ pF, C_{ss} as indicated

Fig. 4. Waveforms of v_{ds} for indicated values of L_{in}, C_{ds} and C_{ss}.

Choosing a suitable MOSFET for a specific application depends on a lot of device parameters. A direct relation exists between the channel resistance ($R_{ds(on)}$), and the gate charge (Q_g). A low $R_{ds(on)}$ results in a large channel surface and with that a large C_{iss} and therefore Q_g. To find a MOSFET with low switching and low conduction losses the product of $R_{ds(on)} \cdot Q_g$ is a useful parameter. In search of the best MOSFET for this application the first choice is to limit the maximum voltage across the device (V_{dss}) to 600 V. For even higher values of V_{dss}, the product $R_{ds(on)} \cdot Q_g$ again increases due to the required larger channel length and with that larger Q_g, assuming a constant $R_{ds(on)}$. Due to the large current through the switch the 26NM60 MOSFET of ST [20] is chosen for its low $R_{ds(on)}$. The gate charge of the device is relatively high but the product $R_{ds(on)} \cdot Q_g$ is still low compared to similar devices.

Many different MOSFET models have been presented by their manufacturers and in the literature [11]. Main differences in these models is the number of passive components and what they are dependent on. Another difference is if extrinsic components are taken into account, such as bond wire inductance and the parasitic capacitance caused by the casing of the die. In this research a first order intrinsic model with nonlinear capacitors [21] is used as can be seen in Fig. 5a. The VDmos tool [21] is used to model different suitable types of MOSFETs for LTspice. This tool calculates the first order model values of all components, linear and nonlinear, based upon their data sheet. The two most important graphs to describe the MOSFETs dynamic behavior can be found in Fig. 5b and c.



(a) Model

(b) Capacitance variations

(c) Gate charge vs V_{gs}

Fig. 5. Dynamic MOSFET characteristics.

The relation between the parasitic capacitances that can be measured (data sheet) and the pin to pin capacitances is given by:

$$C_{ds} = C_{oss} - \frac{C_{rss}(C_{iss} - C_{rss})}{C_{iss}}, \tag{4}$$

for the drain to source capacitance. The gate to source capacitance can be determined using:

$$C_{gs} = C_{iss} - C_{rss}, \tag{5}$$

and finally the gate to drain is equal to the miller capacitance:

$$C_{gd} = C_{rss}. \tag{6}$$

A model of the 26NM60 is made, and from this it can be found that the C_{oss} of the device is approximately 165 pF for $\bar{V}_{ds} = V_{pa}/(1-D) = 160$ V during the off state. With an optimal total C_{ds} of 500 to 700 pF, the additional fixed capacitance ($C_{ds(fix)}$) is 335 to 535 pF. Now that all the passive components are set and a suitable MOSFET has been chosen, the behavior of the circuit can be compared to the ideal switch situation.

C. Push Pull PA with MOSFET model

The total setup of the PP amplifier is tested to verify if the circuit works as intended. A model with all the loss mechanisms is made to see which combination has the best overall efficiency. An overview off all the added ESR values can be found in table II. The value of of the series capacitance in the PP configuration (C_s) is half that of the SS (C_{ss}).

TABLE II
COMPONENT ESR OVERVIEW

Component	Value [pF / nH]	ESR[mΩ]	V_{pa}[V]
C_s	272/4	4 x 35	
$C_{ds(fix)1,2}$	345,339	30	84
	445,439	24	82
	545,539	19	84
L_{in1}	538	141	
L_{in2}	545	139	

The capacitors used are the ERB 500 V types of Murata, and multiple devices in parallel are used to obtain the required value. Due to the high peak to peak voltage (v_{pp}) across L_{load} and C_s, this capacitance is spread over four capacitors in series of each 272 pF. To spread the current and reduce the ESR, each of these four capacitors is build up out of 6 capacitors in parallel.

The small variations in $C_{ds(fix)1,2}$ (table II) are used to compensate the variations in the inductors L_{in1} and L_{in2}. Efficiency calculations are carried out to determine the final component combinations, the results can be found in table III. In the simulations the supply voltage is adapted to match P_{out}. The total of the conduction and switching loss for both devices is indicated in table III. The total schematic with all components and their ESRs is depicted in Fig. 6. From this it can be concluded that the most efficient combination is with $C_{ds(fix)1} = 445$ and $C_{ds(fix)2} = 439$ pF. The accompanying waveforms are shown in Fig. 7. The voltage across (v_{ds}), and the current through (i_d) MOSFET M_1 can be found in Fig. 7a. There it can be seen that due to C_{oss}, the current through M_1 does not drop instantly resulting in switching losses. The switching loss in the MOSFETs is 4 W or 44 %, and the conduction loss is 5.2 W or 56 % each. Together with the ESRs this causes the decrease in efficiency between the ideal switch and the MOSFET circuit. The current through L_{in1}

TABLE III
POWER LOSS AND EFFICIENCY OVERVIEW

$C_{ds(fix)1,2}$ [pF]	MOSFET loss [W]	ESR loss [W]	η [%]
345,339	24.9	19.5	87.2
445,439	18.3	18.7	**89.1**
545,539	17	20.8	88.6

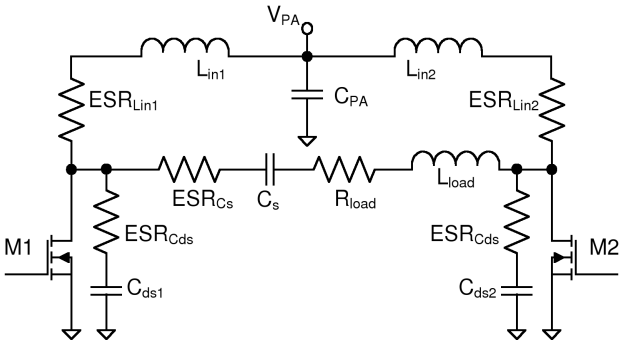
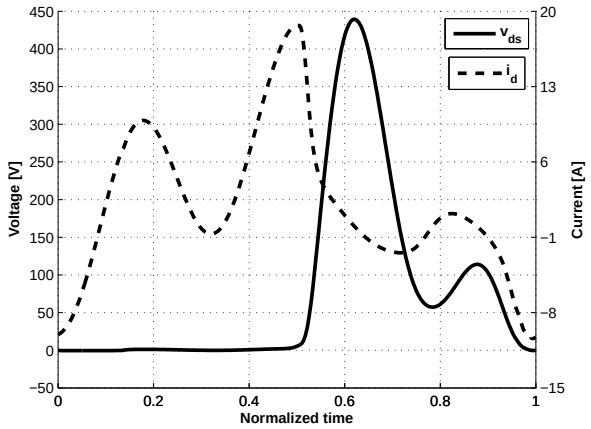
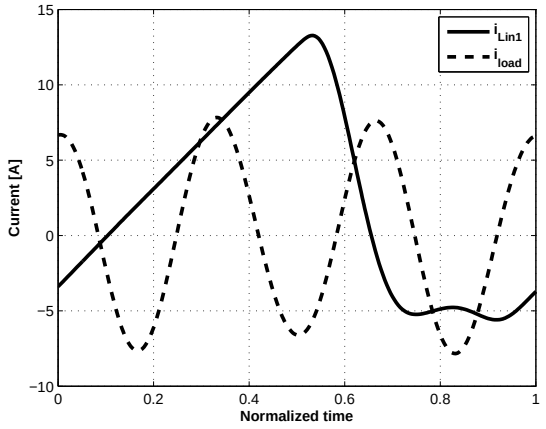


Fig. 6. Total PP Class-E PA with ESR of passive components.

(i_{Lin1}) and the current through the load (i_{load}) are depicted in Fig. 7b.



(a) Waveforms of v_{ds} across and i_d through M_1.



(b) Waveforms of i_{Lin1} and i_{load}

Fig. 7. Significant voltage and current waveforms in PP PA.

Finally, C_{PA} is determined using:

$$C_{PA} \geq \frac{2P_{in}}{(V_{PA(max)} - V_{PA(min)})f_o} \geq 101nF. \quad (7)$$

Where $V_{PA(max)}$ and $V_{PA(min)}$ are derived from $V_{PA} = 80$ V with a maximum peak to peak voltage of 3 V. In the build amplifier, C_{PA} consists of six 18 nF multilayer ceramic capacitors of Murata with a combined ESR of 10 $m\Omega$ at f_o.

IV. Resonant Gate Driver

In order to reach the maximum efficiency in a PA, every part of the circuit has to be designed for this purpose. The power loss generated by the gate drivers can be a significant part of the overall power losses in a PA [7], especially at high frequencies and in case of high currents, as in this application. The Voltage Source Driver (VSD) circuit [7] is popular for its simplicity and low cost. Downside of the circuit is that it is hard switched and that the energy stored in the input capacitance of the MOSFET (C_{iss}) is lost when the device is switched off (gate losses). The loss mechanisms present in a VSD can be divided in three parts [11], namely the hard switching losses of the HB consisting of M_1 and M_2 (Fig. 8), the losses in the gates of switches M_1 and M_2 and the largest part, the main MOSFET gate losses. Losses in the gates of M_1 and M_2 cannot be avoided, but only reduced by minimizing the number of switches. Main challenges therefore are to make the circuit operate under ZVS conditions and to preserve most of the energy needed to charge C_{iss} (5), (6).

The power loss in the gate the main MOSFET when using a VSD is equal to the product of the gate charge, the gate-drive voltage and the switching frequency as given by

$$P_{gate} = Q_g V_{dc} f_{sw} = C_{iss} V_{dc}^2 f_{sw}. \quad (8)$$

This results in a loss of 3.3 W per MOSFET, using a 26NM50 from ST [20] with a drive voltage (V_{dc}) of 10 V and a gate charge of 73nC (Fig. 5).

The additional power loss due to hard switching is caused by the dissipation of the energy stored in the output capacitances (C_{oss}) of the HB. These losses can be determined using:

$$P_{C_{oss}HB} = 2C_{oss} V_{dc}^2 f_{sw}. \quad (9)$$

The third loss component is caused by the conduction losses through the HB MOSFETs. These losses can be calculated with:

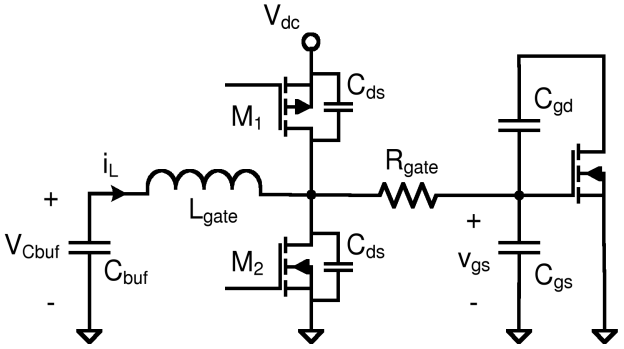
$$P_{R_{ds(on)}HB} = R_{ds(on)M1} I_{dM1}^2 + R_{ds(on)M2} I_{dM2}^2. \quad (10)$$

Resonant gate drivers are a efficient alternative to a conventional VSD to drive power MOSFETs, if properly operated. These drivers are called resonant gate drivers because there is an energy exchange between either the supply voltage or an additional capacitor and C_{iss} of the power MOSFET, via an inductor. Different types of resonant gate driver topologies have been analyzed to come up with a design that fits the requirements of this PA best.

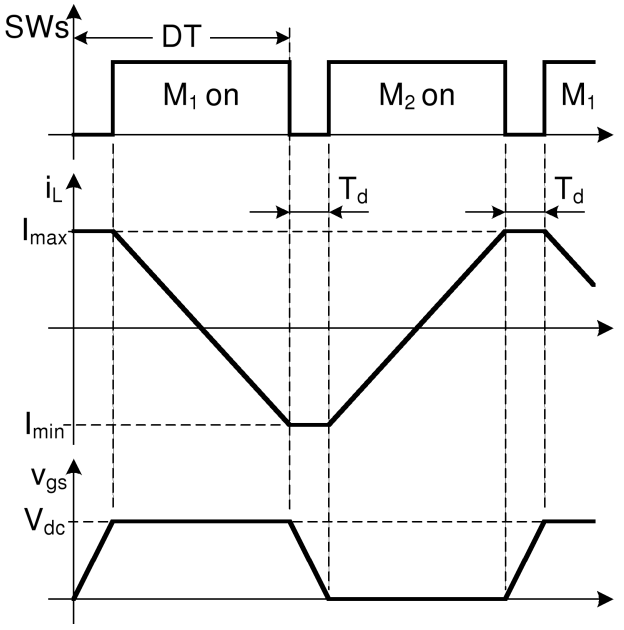
A. Topologies

In [10] the first effort was made to come up with a so called Resonant Transitions (RT) circuit and in [11] an extensive analysis of the same circuit was performed. The circuit consists of a current source with a HB (Fig. 8a) to switch the direction of the current. The resonant circuit L_{gate}, C_{iss}, is formed only during transitions i.e. when both M_1 and M_2 are off, clarifying the name of the circuit. When the gate is fully

charged to V_{dc}, M_1 is turned on to provide a low impedance path from the gate to V_{dc}. Provided that C_{buf} is large enough, the steady state voltage across $V_{C_{buf}} \approx DV_{dc}$ with an ac ripple depending on the value of C_{buf} and the power drawn per cycle. A disadvantage of this topology is that during $T - 2T_d$ one



(a) Gate driver circuit



(b) Waveforms

Fig. 8. Resonant transition gate driver [10].

of the HB MOSFETs is conducting, decreasing the efficiency. The required inductance to drive the main MOSFET (table IV) can be determined with:

$$L_{gateRT} = \frac{D(1-D)T_d}{2C_{iss}f_{sw}} = 316nH, \tag{11}$$

where the dead time (T_d) has been set to 15% of T to avoid cross conduction through the HB. The maximum current through the inductor (I_{max}) can subsequently be determined using:

$$I_{max} = \frac{D(1-D)V_{dc}T_d}{2L_{gateRT}} = 873mA. \tag{12}$$

For simulations, the value of C_{buf} is set to 200 nF, in series with 40 mΩ. This value will be later adapted to the final value of L_{gateRT} or $L_{gatePCR}$.

In [12] a Passive Clamping Resonant (PCR) gate driving configuration is introduced. The circuit consists of HB, an inductor as resonant element, and a set of free running anti-parallel diodes as can be seen in Fig. 9. Main difference with the RT circuit is that here the MOSFETs are only turned on for a short period of time to change v_{gs}. The diodes provide a return path for the current i_L when C_{iss} is charged by clamping v_{gs} to V_{dc} or ground to make sure no voltage peaks occur. Downside of the topology is that the value of the resonant inductance depends on the required rise time for v_{gs} and the gate capacitance of the upper MOSFET (M_1). This results in a low inductance for this application due to the high value of f_{sw}, and with that high RMS losses. The required

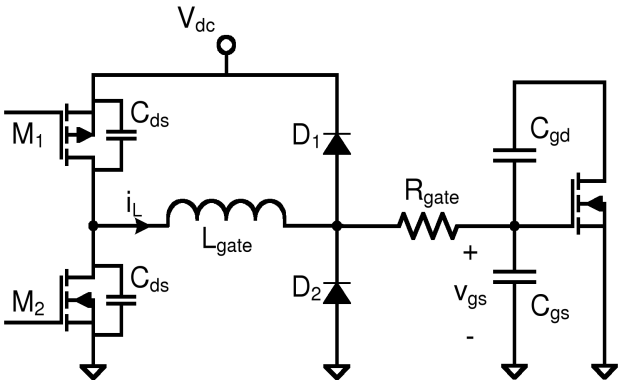


Fig. 9. Passive clamped resonant gate driver.

resonant inductance $L_{gatePRC}$ can be calculated as:

$$L_{gatePRC} = \left(\frac{2T_d}{\pi}\right)^2 \frac{1}{C_{iss}} = 154nH. \tag{13}$$

In [13] a Full Bridge (FB) Active Clamping Resonant (ACR) gate driving circuit is presented. The circuit is comparable with the previous configuration, but here two extra MOSFETs replace the diodes (Fig. 9) and actively clamp v_{gs} to V_{dc} or ground. By turning M_4 (replacing D2 in Fig. 9) off after turning M_1 on, the inductor is charged before charging the input capacitance of the power MOSFET. Switching details can be found in [13]. This circuit is not suitable for this application because the MOSFET it needs to drive has a gate resistance (R_{gate}) of 1.6 Ω, resulting in a lower efficiency than a conventional VSD.

To verify the behavior of the circuits working on f_{sw}, simulations have been carried out. Based on the simulation results a topology is chosen for this application.

B. Simulations

Simulations on the RT and PRC gate driving topology are carried out to determine the most suitable topology. To make a fair comparison between the various circuits, the same driving and main MOSFETs have been used in all simulations. The key parameters of the components can be found in table IV. The RT gate driver circuit with a 330 nH inductor has high Hard Switching (HS) losses due to the slow transitions between V_{dc} and ground. Simulations with

TABLE IV
COMPONENT KEY PARAMETERS

Component	Type nr.	Key parameters
Main MOSFET	ST26NM60	$R_{gate} = 1.6\Omega, R_{ds(on)} = 125m\Omega$, Q_g(figure5c)
P-MOS M_1	Si4532DY-P	$C_{oss} = 180pF, R_{ds(on)} = 62m\Omega$
N-MOS M_2	Si4532DY-N	$C_{oss} = 110pF, R_{ds(on)} = 44m\Omega$
$D_{1,2}$	PMEG2020A	$V_F = 380mV@1Apk$
L_{gateRT}	3615uH33-K	$R_{dc} = 50m\Omega, L = 330nH \pm 10\%$
$L_{gatePRC}$	3615uH15-K	$R_{dc} = 30m\Omega, L = 150nH \pm 10\%$

lower inductance values for L_{gateRT}, are carried out to find an optimum combination of the lowest RMS and HS losses. The results of this simulation sequence can be found in table V, where also the losses of a VSD are added for comparison. Based on these results a 150 nH inductor should be chosen, but the slope of its waveform has a discontinuity around the threshold level of the main MOSFET, which could result in duty cycle variation. The 100 nH inductor is chosen as the best solution because of its waveform (Fig. 10) and the small difference in loss. The total loss of the driver circuit is 1.7 W, during the simulations the supply voltage V_{dc} is kept constant at 10 V. The drive losses could be further reduced if V_{dc} would decrease, this however would result in an increase of $R_{ds(on)}$ of the main MOSFET, and with that the loss of the PA. The resulting efficiency improvement opposing the VSD is 50%. The resistance R_{dc} in table V represents the ESR of that specific inductor. The waveforms of v_{gs} for different inductance values can be found in Fig. 10. The rise (t_{rise}) and fall time (t_{fall}) of v_{gs} with the 100 nH inductor RT gate driver is approximately 16 ns.

TABLE V
RT GATE DRIVER LOSSES

Inductance [nH]	I_{max} [A]	R_{dc}[mΩ]	P_{loss} [W]
VSD	4.4	0	3.4
50	6.1	14	4.1
80	3.6	20	2.4
100	2.7	27	1.7
150	1.7	30	**1.4**
220	1.1	35	1.7
330	0.8	50	2.1

Simulations on the PCR gate driving circuit have also been carried out. Main conclusion is that the calculated induction value (13) is again much too high to get a good v_{gs} waveform. In order to get the same t_{rise} and t_{fall} as the RT gate driver circuit, an inductor of 35 nH is needed. The resulting loss in the circuit is 3.8 W, which is even higher than with a VSD. The RT circuit is therefore chosen as the gate driver for this application.

The value of C_{buf} depends on the maximum allowed voltage ripple, and the required power per switching cycle. With the voltage ripple being set to 1 v_{pp} around 5 V and the required power being 3.9 W calculated via (12) and R_{gate}, the resulting minimal capacitance value is 172 nF.

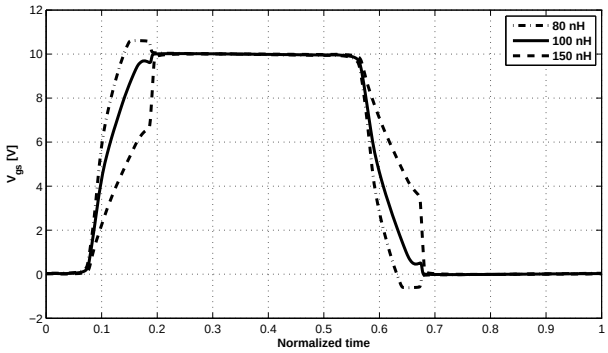


Fig. 10. Waveforms of v_{gs} for L_{gateRT} is 80, 100, 150 nH respectively.

V. INDUCTOR DESIGN

With efficiency being the most important application requirement, an input inductor has to be developed that contributes to this goal. As can be seen in the simulation results, the RMS current flowing through the inductor (I_{in}) is 6.7 A, and has a main frequency component of f_{sw}. Therefore a coil needs to be designed with a low ESR at this frequency. Important choices that have to be made is the type of conductor, wether magnetic material will be used and the shape of the coil and coil-former. The main problems faced when developing a low loss HF inductor are the skin and the proximity-effect.

A. theoretical analysis

As can be concluded from the previous, an input inductor must be designed which meets the following demands, sorted by importance for this application:

1) The inductance must be 550nH with a tolerance of maximum 5%.
2) The overall loss of the coil must be as low as possible.
3) The ESR must be as low as possible.
4) The coil should fit on the PCB.
5) The inductor should have a minimum external magnetic field.

In order to minimize the skin effect, copper strip of 35μm thick and 6.35 mm wide is used. An other option is to use stranded (Litz) wire, but its variable winding pattern could result in a non-homogenous field distribution and thereby an unpredictable inductance per length of wire. Especially low inductance coils, consisting of relatively short wire, are sensitive to this effect. Downside of copper strip is that its very wide so a clever way of winding it must be found in order to fit on the PCB. The possibility of multiple layers of copper strip to reduce the resistance is also considered. Due to the large surface of the strip and the short distance between the layers this would result in a high coupling capacitance, reducing the resonant frequency and Q.

The second choice that has to be made is that of the coil shape; solenoid vs toroid. As can be found in [22], a solenoid uses the least space for a coil with a given inductance. But a solenoid does not encapsulate the magnetic field it generates, thus it would have to be placed further away from the rest of

the circuit, resulting in extra effective space for the inductor. Another disadvantage is that the two inductors would interfere with each other causing a change in their inductance. To be able to comply with the given demands 1, 4 and 5, a toroid shape is chosen for this application.

Once the shape of the coil is known, the size of the required inductor core should be determined. The basic idea is to comply with demand 4, which means that the maximum outer diameter (d_o) of the coil is 50 mm. The minimum inner diameter (d_i) is set to be 20 mm, to maximize the enclosed surface. The value of d_i is limited by the width of the copper strip in combination with the number of windings (N). The number of windings is set to 7. For a higher number of windings d_i should be increased to prevent additional proximity losses. The resulting decrease of the encapsulated surface can only be compensated by increasing the height of the core. For a lower number of windings the required height increases rapidly, and the magnetic field generated would not be encapsulated as well as with 7 windings. For this combination, the pitch between the windings is 9 mm, and with that the distance between two windings 2.7 mm. The proximity effect is therefore neglected in the calculated loss comparison, in section V-B, this will be verified.

The required height for the core can be determined according to [23] with :

$$h = \frac{\pi}{N^2 \ln\left(\frac{d_o}{d_i}\right)}\left[\frac{2L}{\mu_0} - \frac{(d_i+d_o)}{2}\left[\ln\left(8\frac{d_o+d_i}{d_o-d_i}\right)-2\right]\right] = 59mm \tag{14}$$

where μ_0 is the permeability of free space, and L the required inductance. Two test inductors were first build to verify (14), and from this a compensation factor of 0.712 is calculated. The resulting height of the inductor is 42mm.

The strip length (l_{strip}) resulting from the calculated parameters is 794 mm. The skin depth in copper at f_{sw} is equal to 31 μm, therefore the skin effect can be neglected in this 35 μm thick conductor. The calculated ESR of the strip ($R_{strip/m}$) is equal to 77 $m\Omega/m$, the resulting (R_{strip}) for the given l_{strip} should therefore be 61 $m\Omega$. The measured ESR of a straight piece of copper strip (1 meter) is equal to 173 $m\Omega$. The large difference can be a result of impurities in the copper, increasing its electrical resistivity. The measured value of R_{strip} is used in the loss comparison of table VI.

The last question that needs to be considered is wether to use a magnetic core material. It would have the advantage of better preserving the external magnetic field inside the toroid. In this application two inductors are needed, and they should preferably be mounted close to each other to minimize the magnetic radiation to the rest of the circuit. Furthermore, the large external field of air core inductors causes electromagnetic interference (EMI) and consequently electromagnetic compatibility (EMC) problems. Possible disadvantages would be saturation due to the large I_{in}, nonlinearity, and permeability variations with time and temperature which cause the inductance to fluctuate. Since demand 1 can be satisfied in both configurations, a theoretical comparison is made between an air core inductor and two configurations of magnetic material. The aim was to verify which suits demand 2 best and wether the decrease in wire length is sufficient to compensate for the core loss. The magnetic cores used are the T175-2, and T157-6 (Micrometals). The peak AC flux density is denoted by $\hat{B}_{ac}$ and l_{strip} is the length of strip needed to wind the core N times. From table VI it can be concluded that for this combination of parameters an air core coil is the most efficient solution. In the next section the measurement results of the fabricated inductors will be presented.

TABLE VI
INDUCTOR LOSS COMPARISON

Core type	L [nH]	N [#]	$\hat{B}_{ac}$ [mT]	P_{core} [W]	l_{strip} [mm]	P_{Cu} [W]	P_{total} [W]
Air	550	7	0.6	-	794	6.2	**6.2**
T175-2	540	6	6.4	4.6	293	2.3	6.9
T157-6	564	7	7.2	4.3	307	2.4	6.7

B. Experimental Verification

To verify the presented theory in practice the inductors are build. To minimize the radiated magnetic field of the inductors one is wound CW and the other CCW. The material used for the toroid coil-former is Delrin, a polymer grade which can withstand temperatures up to 200 $^\circ C$. A comparison between the theory and the two actually manufactured inductors can be found in table VII. The tested frequency range (Δf) used is that from 3 MHz till 15 MHz. From table VII it can be concluded that the theoretically determined height (14) results in two inductors with an inductance well within the 5% tolerance stated in demand 1 if the compensation factor is used. The actual ESR is also satisfactory predicted, being maximally $2m\Omega$ higher than for a straight piece of strip. The proximity effect can therefore be neglected.

TABLE VII
INDUCTOR IN THEORY AND PRACTICE

Inductor	L [nH]	ESR [mΩ]	Q	ΔL [%]	ΔESR [%]	$\frac{\Delta L}{\Delta f}$ $\left[\frac{pH}{MHz}\right]$	$\frac{\Delta ESR}{\Delta f}$ $\left[\frac{m\Omega}{MHz}\right]$
Theory	550	139	112				
Inductor I	538	141	108	-2.2	1.4	-125	5.1
Inductor II	545	139	111	-0.9	0	-75	5

VI. EXPERIMENTAL RESULTS

The 13.56 MHz Class-E Push-Pull amplifier is build, Fig. 11 shows the implemented amplifier. The PCB that has been designed is clearly visible as is the passive cooling element on which it is mounted. To be able to adequately cool the main MOSFETs, a window is milled out of the PCB for each of them. The crystal oscillator and dead time control circuitry

are placed on the lower left side of the PCB, the PA part including the input inductors designed in section V-B can be found in the upper right corner.

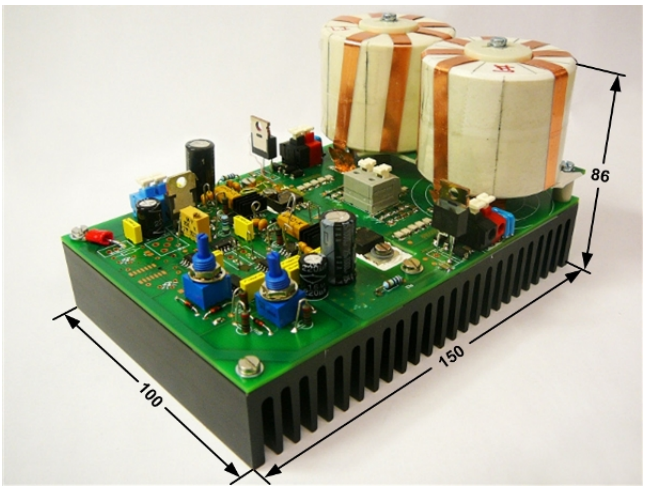
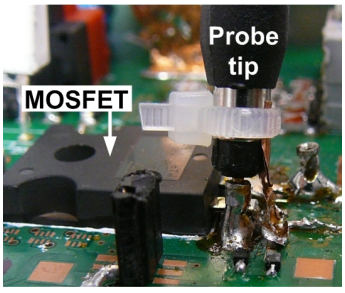


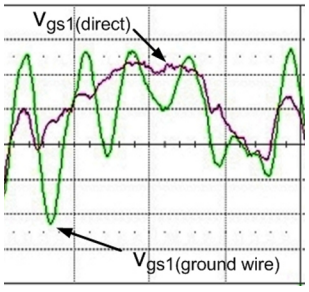
Fig. 11. Implemented power amplifier, dimensions in mm.

A. Direct Measuring

The ground wire with which a conventional voltage probe is equipped is an additional inductance which influences the measurement. This inductance causes a resonating circuit with C_{oss} of M_1 or M_2 of the HB, depending on which of the MOSFETs is in off state. To minimize the influence by the parasitic resonant circuit this inductance should be minimized, a direct measurement technique is practised to do this (Fig. 12a). A piece of copper strip is used to make a short connection from the source of the main MOSFETs to ground. A zoomed-in plot of the difference between a direct and a ground wire measurement is depicted in Fig. 12b. From Fig. 12, it can



(a) Detail of measurement technique.



(b) Difference in waveforms, t = 20 ns/div, v = 2 V/div.

Fig. 12. Direct measurement to minimize external influences.

be concluded that the direct and ground wire measurement have the same average shape. The peaks on the ground wire measurements however differ up to 5 V in comparison to the direct measurement. Measuring v_{gs} of the main MOSFETs is therefore carried out with a direct connection throughout this project to increase the measurement accuracy.

B. Resonant Transitions Gate Driver

To verify wether the gate driver operates as intended in section IV-B, measurements are carried out. A picture of v_{gs} of both the RT gate driver waveforms of M_1 (v_{gsM1}) and M_2 (v_{gsM2}) can be found in Fig. 13. When comparing these waveforms to the simulations it can be concluded that t_{rise}) and t_{fall} are approximately 20 ns each, being slightly higher than the predicted value. The voltage however, is not clamped to the supply voltage (V_{dc}) or ground level, this is due to the small inductance formed by the piece of PCB track from the HB to the gate of the main MOSFET. The duty cycle of v_{gsM1} and v_{gsM2} is 46%, being slightly less than was intended. To

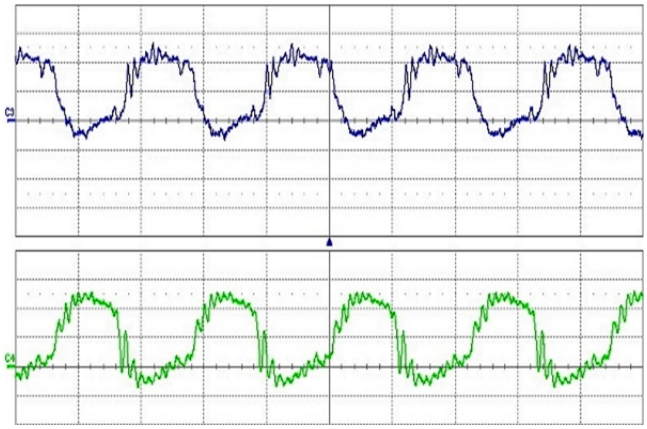


Fig. 13. v_{gsM1} (upper) and v_{gsM2} (lower), t = 100ns/div, V = 5 V/div.

verify if the proposed circuit reaches the calculated power loss reduction of 50%, additional measurements are carried out. The power loss of the RT gate driver is measured over a long period of time (30 min.) to ensure thermal stability. The resulting power needed to drive the main MOSFET is 2.6 W, which is significantly higher than the calculated 1.7 W. To clarify the large difference, the frequency response of the 100nH inductor was measured to verify the data stated in its data sheet. The measured inductance and ESR of the inductor at f_{sw} are 90 nH and 90 $m\Omega$ respectively. The decrease in inductance as well as the larger ESR results in higher RMS losses in the circuit. With these values an additional simulation was done which resulted in 2.3 W of loss. The additional difference is due to small variations in the gate drive signals of M_1 and M_2 (Fig. 8a). The loss of the VSD is also measured for comparison, with 3.4 W this was the same as the calculated value. The final reduction in power required to drive the ST26NM60, is 24% with the circuit presented here.

C. Power Amplifier

Measurements on the PP PA are carried out. To avoid breakdown of the main MOSFETs during the measurements, a supply voltage (V_{pa}) of 50 V was used during the first measurements. The resulting optimal $C_{ds(fix)1} = 370$ and $C_{ds(fix)2} = 364$ pF were used. The resulting waveforms of the drain source voltage of M_1 (v_{dsM1}) and M_2 (v_{dsM2}) are

depicted in Fig. 14 , the current through the load network is also shown here. The RMS value of the load current (I_{load}) is 2.6 A.

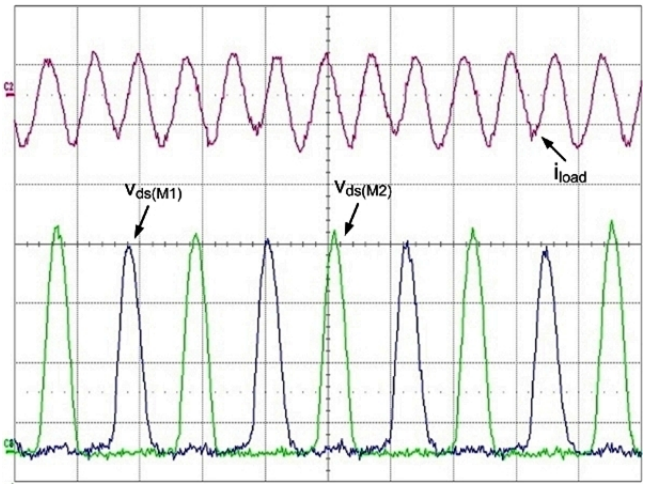
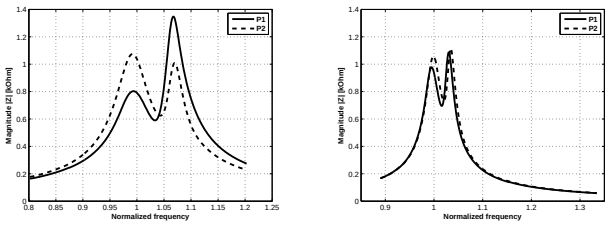


Fig. 14. i_{load}, v_{dsM1} and v_{dsM2}, t = 100ns/div, I = 5 A/div, V = 100V/div.

From Fig. 14 it can be concluded that v_{dsM1} and v_{dsM2} do not have the required shape. The simulated peak voltage across the MOSFET ($\hat{v}_{ds}$) should be approximately 280 V in this configuration. In order to get the required power into the load network, the waveforms should have a lower $\hat{v}_{ds}$ with a constant average voltage across the switch i.e. the second peak should be present. Several possible solutions to this problem have been examined. The first idea was to vary $C_{ds(fix)1,2}$, but this did not result in a waveform with a second peak. The second idea was to use a different type of MOSFET, the ST26NM60 has a high C_{oss} at low v_{ds} values. The final idea was to measure and compare the impedance of the two parallel resonance loops (P1 and P2). The impedance of the loops was tuned by making small changes in the fixed capacitor values ($C_{ds(fix)1,2}$) and repositioning the input inductors ($L_{in(1,2)}$). The difference in measured frequency sweep impedance response between P1 and P2 before and after the tuning can be found in Fig. 15a and b respectively. The normalized frequency in Fig. 15 is determined by measuring the total parallel impedance response of P1 and P2 together. The frequency corresponding to the maximum impedance point was chosen as the unity frequency.



(a) Impedance before tuning (b) Corrected impedance

Fig. 15. Impedance of P1 and P2 dependent of the frequency.

The final measurements were carried out using a new type of MOSFET and the improved parallel resonance loops. The MOSFETs used in the final setup were two ST20NM50 devices with a very low C_{oss}, especially at low v_{ds} values ($C_{oss} \approx 3$ nF at $v_{ds} = 0$ V). These devices have a V_{dss} of 500 V and are therefore only suitable for testing purposes. The used values for $C_{ds(fix)1,2}$ in this setup were 395 and 370 pF respectively, and $V_{pa} = 50$ V. The resulting waveform of v_{dsM2} has the intended shape and $\hat{v}_{ds}$, but v_{dsM1} does not (Fig. 16). This is due to a small phase angle error between v_{gs1} and v_{gs2} causing an unbalanced energy distribution in the circuit. No total efficiency measurement was done because the PA did not function as intended.

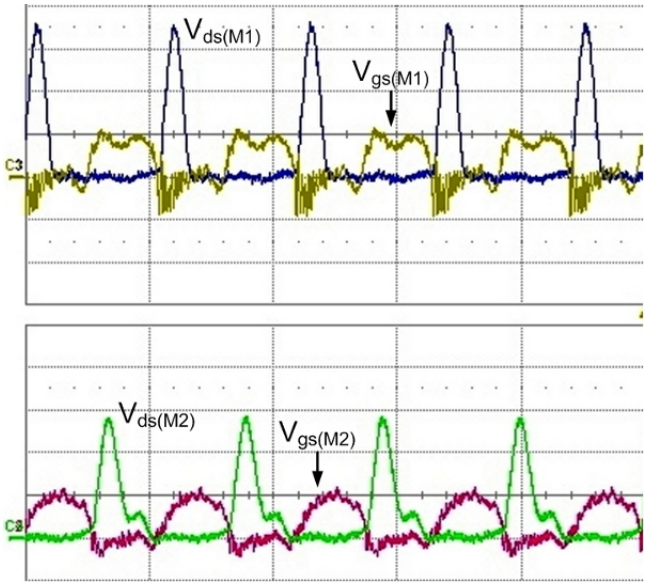


Fig. 16. Waveforms of v_{ds} and v_{gs} of M_1 and M_2, t = 200ns/div, v_{gs} = 10 V/div, v_{ds} = 100V/div.

VII. Conclusions

In this paper a novel approach for driving a Class-E PA is presented. Simulations on the proposed circuit were performed, and showed that an efficient energy conversion to a high frequency load network is possible. The measurements on the build PA however, show that there are a lot of essential parameters that need to be very accurate and stable. Tolerance in capacitors should be eliminated by using multiple components in parallel. The maximum efficiency bottlenecks in this circuit are mainly the ESR of the air core inductors and C_s. The most critical parameter of the MOSFET is the output capacitance, which is limited by the ideal total drain source capacitor value. The simulated maximum efficiency of 89% is an evident improvement opposing [6]–[8].

An efficient gate drive circuit is presented. The measured losses are somewhat higher than simulated, but still a significant improvement is shown when compared to [6], [7].

A trustworthy method is presented to design inductors for the low inductance range, aimed to have an as low as possible overall loss.

VIII. Recommendations

Further measurements on the PP PA should be performed to optimize the operation and to verify the simulated efficiency.

A MOSFET type with a very low C_{oss} should be used to minimize the nonlinearity effects and cancel out variations between different devices. Variations in the input inductors and the output capacitance of the MOSFET should be compensated by the value of the fixed drain to source capacitors. An accurate and stable capacitor type should be used for C_s.

Thicker copper strip should be used to reduce the ESR of the input inductors. The ESR of the copper strip was significantly higher than expected, resulting in 37 % of the overall losses.

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