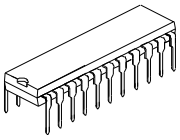
PLL FOR DIGITAL TUNING SYSTEM(DTS)

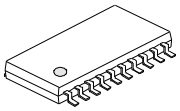
DESCRIPTION

The SC72131 is phase-locked loop (PLL) LSI for digital turning systems (DTS).

The LSI is use to configure high-performance digital tuning systems,such as radio/cassette players. They allow high-performance AM/FM tuners to be implemented easily.



SDIP-22-300-1.778



SOP-20-300-1.27

FEATURES

* Built-in prescalers. Operate at input frequency ranging from 10~160MHz during FMIN input and at 0.5~40MHz during AMIN input.
* 12 possible reference frequencies (with 4.5 or 7.2 MHz crystal) 1, 3, 5, 9, 10, 3.125, 6.25, 12.5, 15, 25, 50 and 100 kHz
* Built-in 20bit general-purpose counter for such as measuring intermediate frequency (IF), IF input frequency ranging from 0.4M~12MHz.
* Has an unlock detector circuit，an dead zone control circuit and an deadlock clear circuit
* Built-in MOS transistor for forming an active low-pass filter
* 4 N-channel open-drain output ports (OFF withstanding Voltage: 13V) and 2 input or output ports.
* Serial data I/O
  — All functions controlled through 4 serial bus lines
* Operating ranges
  — Supply voltage.....5.0 ± 0.5 V
  — Operating temperature.....–40 to +85° C
* Packages
  —SDIP-22-300-1.78
  —SOP-20-300-1.27

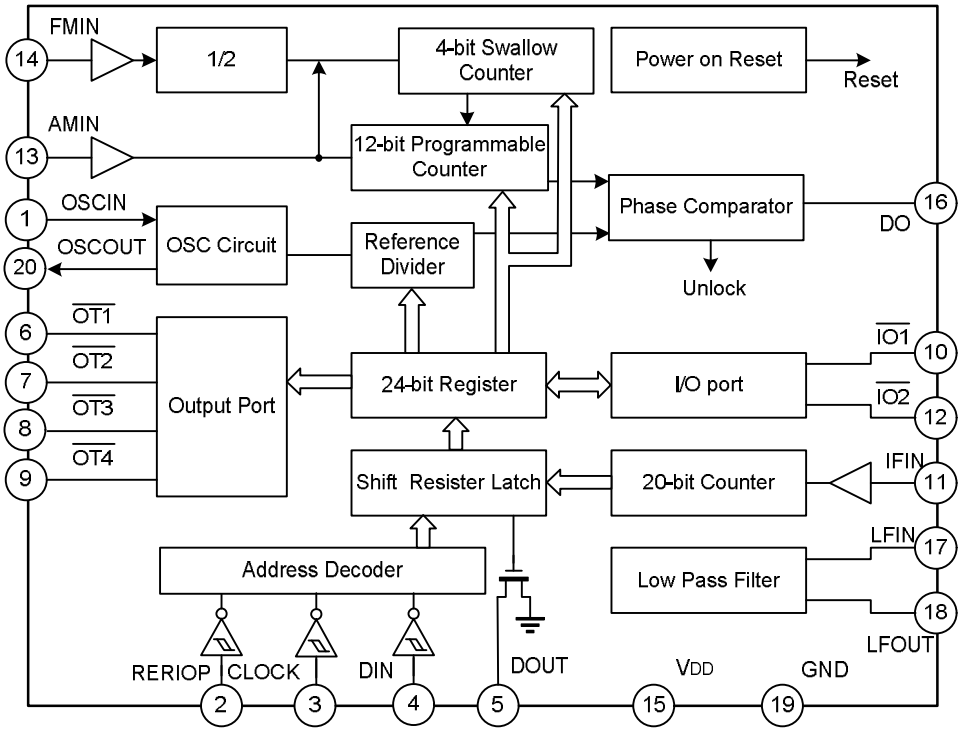
ORDERING INFORMATION

Part No.	Package
SC72131	SDIP-22-300-1.778
SC72131S	SOP-20-300-1.27

APPLICATIONS

* Digital Tuning Systems

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C, VSS=0V)

Characteristics	Symbol	Ratings	Unit
Supply Voltage	V_{DDmax}	-0.3 to 7.0	V
Allowable Power Dissipation	P_{dmax}	350	mW
N-ch Open-Drain OFF Withstanding Voltage	V_{OFF}	13	V
Operating Temperature	T_{opr}	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (Tamb=-40 to 85°C, VSS=0V)

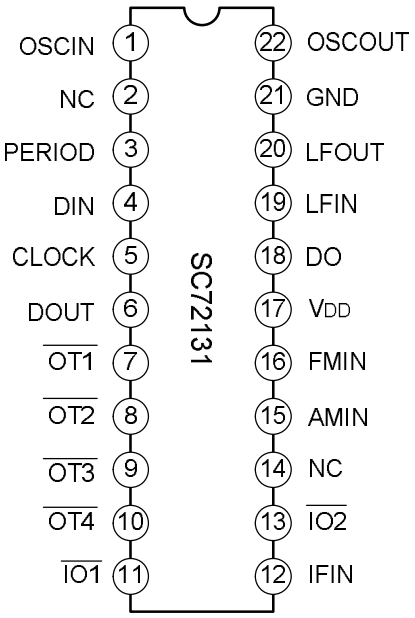
Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Built-in Feedback Resistance	R_{f1}			1.0		MΩ
	R_{f2}			500		kΩ
	R_{f3}			500		kΩ
	R_{f4}			250		kΩ
Built-in Pull-down Resistor	R_{pd1}			200		kΩ
	R_{pd2}			200		kΩ
Hysteresis	V_{HIS}			0.1V_{DD}		V
Output High Level Voltage	V_{OH1}	I_O=-1mA	V_{DD}-1.0			V

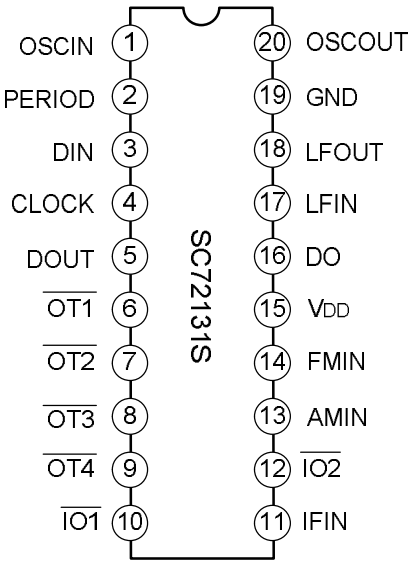
(To be continued)

(Continued)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Low Level Voltage	V_{OL1}	I_O=1mA			1.0	V
	V_{OL2}	I_O=0.5mA			0.5	V
		I_O=1mA			1.0	V
	V_{OL3}	I_O=1mA			0.2	V
		I_O=5mA			1.0	V
	V_{OL4}	I_O=1mA			0.2	V
		I_O=5mA			1.0	V
		I_O=8mA			1.6	V
	V_{OL5}	I_O=1mA, A_{IN}=1.3V			0.5	V
Input High Level Current	I_{IH1}	V_I=6.5V			5.0	μA
	I_{IH2}	V_I=13V			5.0	μA
	I_{IH3}	V_I=V_{DD}	2.0		11	μA
	I_{IH4}	V_I=V_{DD}	4.0		22	μA
	I_{IH5}	V_I=V_{DD}	8.0		44	μA
	I_{IH6}	V_I=6.5V			200	nA
Input Low Level Current	I_{IL1}	V_I=0			5.0	μA
	I_{IL2}	V_I=0			5.0	μA
Input Low Level Current	I_{IL3}	V_I=0	2.0		11	μA
	I_{IL4}	V_I=0	4.0		22	μA
	I_{IL5}	V_I=0	8.0		44	μA
	I_{IL6}	V_I=0			200	μA
Output Off Leakage Current	I_{OFF1}	V_O=13			5.0	μA
	I_{OFF2}	V_O=6.5V			5.0	μA
High Level Three-state Off Leakage Current	I_{OFFH}	V_O=V_{DD}		0.01	200	nA
Low Level Three-state Off Leakage Current	I_{OFFL}	V_O=0V		0.01	200	nA
Input Capacitance	C_{IN}			6		pF
Current Drain	I_{DD1}	X_{tal}=7.2MHz, f_{IN2}=130MHz, V_{IN2}=40mVrms		5	10	mA
	I_{DD2}	PLL block stopped (PLL INHIBIT), Xtal oscillator operating (X_{tal}=7.2MHz)		0.5		mA
	I_{DD3}	PLL block stopped, Xtal oscillator stopped			10	μA

PIN CONFIGURATION (SDIP22, SOP20)





PIN DESCRIPTION

Pin NO.		Pin Name	Description
SDIP-22	SOP-20		
1	1	OSCIN	Connects 4.5M or 7.2M crystal oscillator to supply reference frequency and internal clock.
22	20	OSCOUT	
2		NC	--
3	2	PERIOD	Serial I/O ports, These pins transfer data to and from the controller to set divisors and dividing modes, and to control the general-purpose counter and general-purpose I/O ports.
4	3	DIN	
5	4	CLOCK	
6	5	DOUT	
7	6	$\overline{OT1}$	• N channel open drain port pins. • The output states are determined by $\overline{OT1}$ to $\overline{OT4}$ bits in the serial data. • If the serial data TBC bit is set to 1, a time base signal (8Hz) can be output from the $\overline{OT1}$ pin. • These pins are set to the OFF state when power is turn on.
8	7	$\overline{OT2}$	
9	8	$\overline{OT3}$	
10	9	$\overline{OT4}$	
11	10	$\overline{IO1}$	• CMOS structure allows free use of these ports for input or output. • Ports are set for input when the power is turned on.
13	12	$\overline{IO2}$	
12	11	IFIN	• Input pin for measure general-purpose counter frequencies. The frequency measurement function has such uses as measuring intermediate frequencies (IF) • These pin feature built-in amps, Data are input by capacitor coupling.

(To be continued)

(Continued)

Pin NO.		Pin Name	Description
SDIP-22	SOP-20		
14		NC	--
15	13	AMIN	• These pins input AM and FM band local oscillator signals by capacitor coupling. • These pins feature built-in amps.
16	14	FMIN	
17	15	V_{DD}	• power supply pin (Applies 5.0V ± 10%)
18	16	DO	• This pin is for phase comparator tristate output.
19	17	LFIN	• These pins for low-pass filter input pin and output pin.
20	18	LFOUT	
21	19	GND	• The SC72131 ground.

FUNCTION DESCRIPTION

Serial Data I/O Methods

The SC72131 inputs and outputs data using the 4 serial bus lines, the serial data I/O methods are selected by an 8bit address

Register assignments

Address = 82H(IN)

P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	MODE	FM	CTE	OSC	R0	R1	R2	R3

Address = 92H(IN)

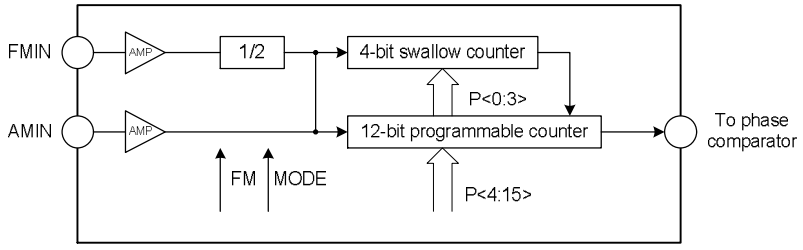
IO C1	IO C2	$\overline{IO1}$	$\overline{IO2}$	$\overline{OT1}$	$\overline{OT2}$	$\overline{OT3}$	$\overline{OT4}$	*	DO C0	DO C1	DO C2	UL 0	UL 1	DZ 0	DZ 1	G0	G1	TO	DOC	IFS	T0	T1	T2

Address = A2H (OUT)

I1	I2	*	UL	IF19	IF18	IF17	IF16	IF15	IF14	IF13	IF12	IF11	IF10	IF9	IF8	IF7	IF6	IF5	IF4	IF3	IF2	IF1	IF0

Programmable divider structure

Swallow counter and programmable counter circuit configuration

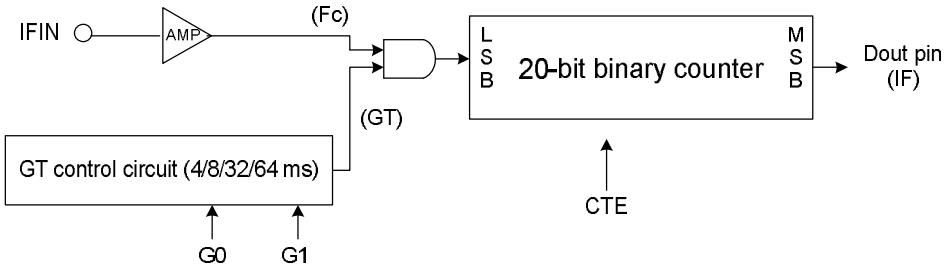


FM	MODE	Input pin	Set divisor	Actual divisor: N	Input frequency range (MHz)
1	*	FMIN	272 to 65535	Twice the set value	10 to 160
0	1	AMIN	272 to 65535	The set value	2 to 40
0	0	AMIN	4 to 4095	The set value	0.5 to 10

Note: * Don't care.

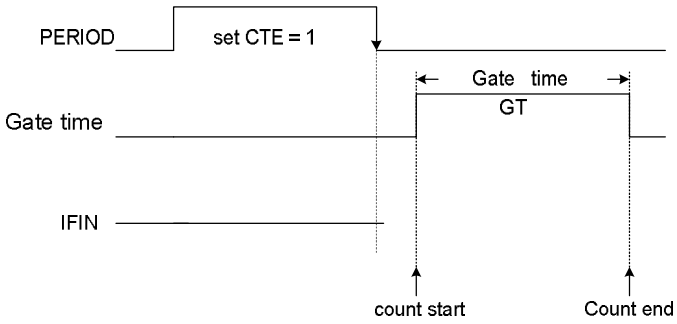
1.IF Counter Structure

The SC72131 IF counter section consists of input amp, a gate time control circuit and a 20bit binary counter. The result, i.e., the counter's msb, can be read serially from the Dout pin.



G1	G0	Gate time (GT) (ms)	Wait time (ms)
0	0	4	3 ~ 4
0	1	8	3 ~ 4
1	0	32	7 ~ 8
1	1	64	7 ~ 8

2. IF Counter Operation



Note: 1. IFIN input have built-in amp. Data are input by capacitor coupling.

2. Before starting the IF count, the IF counter must be reset in advance by setting CTE in the serial data to 0.

3. The IF count is started by changing the CTE bit in the serial data from 0 to 1. The serial data is latched by the SC72131 when the CE pin is dropped from high to low.

4.The IF signal must be supplied to the IFIN pin in the period between the point the CE pin goes low and the end of the wait time at the latest.

5. The value of the IF counter at the end of the Gate-Time must be read out during the period that CTE is 1. This is because the IF counter is reset when CTE is set to 0.

6. When operating the IF counter, the control microprocessor must first check the state of the IF-IC SD (station detect) signal and only after determining that the SD signal is present turn on IF buffer output

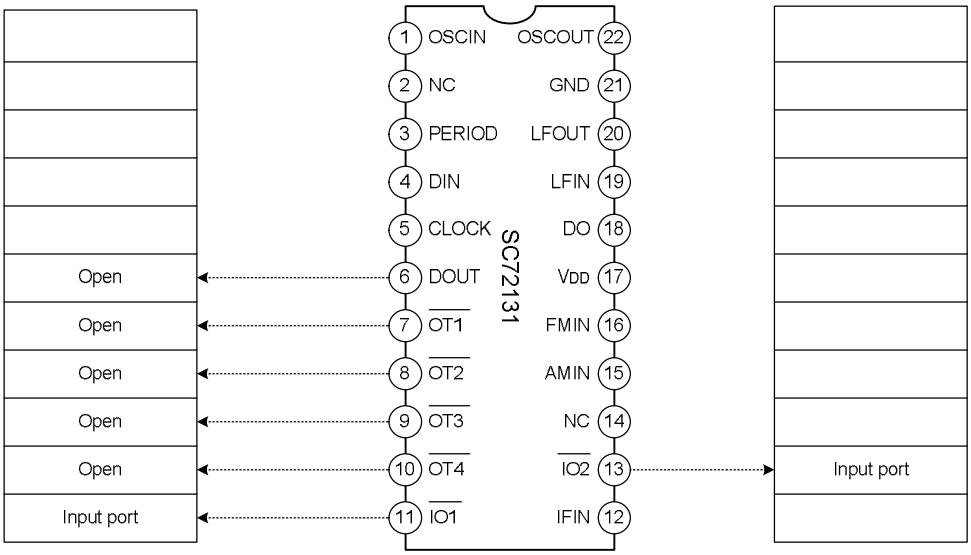
and execute an IF count operation. Auto search techniques that use only the IF counter are not recommended, since it is possible for IF buffer leakage output to cause incorrect stops at points where there is no station.

3. Power Supply Pins

A capacitor of at least 2000 pF must be inserted between the power supply VDD and GND pins for noise exclusion. This capacitor must be placed as close as possible to the VDD and GND pins.

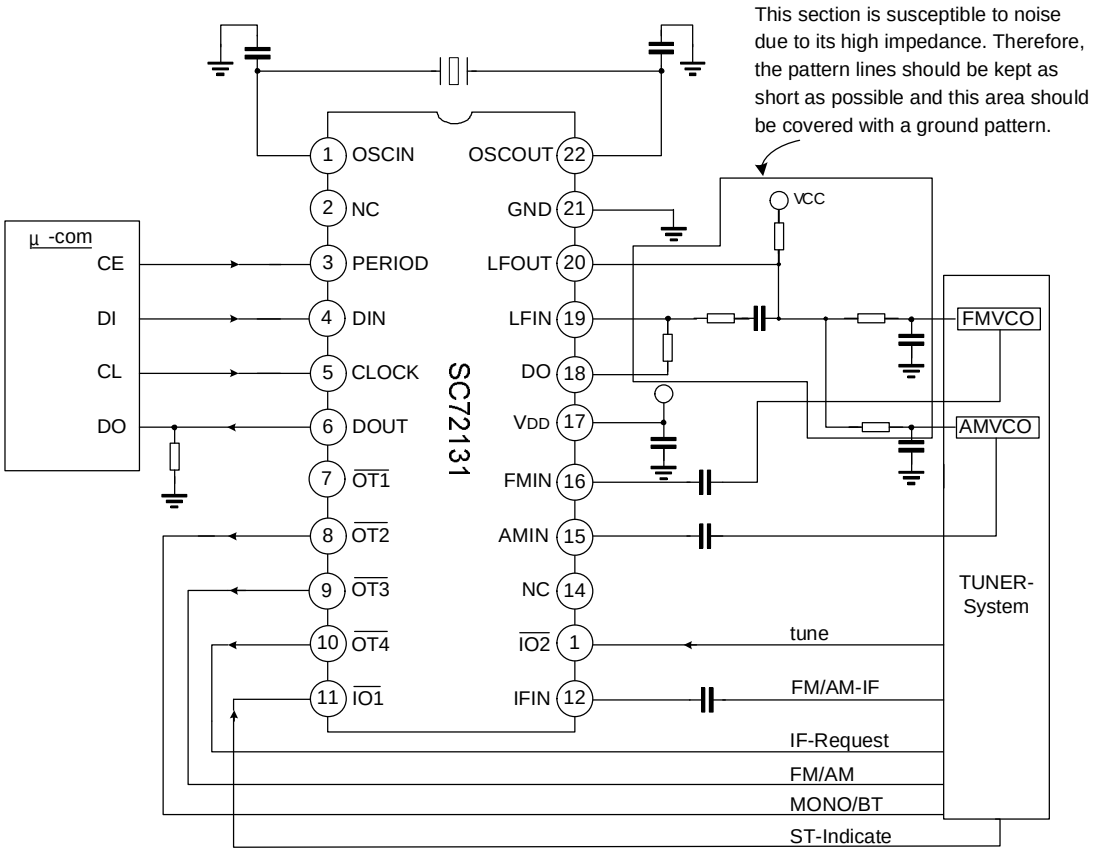
PIN STATES AFTER THE POWER ON RESET

After power-on reset, the pins (DOUT $\overline{OT1}$ $\overline{OT2}$ $\overline{OT3}$ $\overline{OT4}$) are set to OPEN state and the pins ($\overline{IO1}$, $\overline{IO2}$) set to INPUT state.



Note: this circuit according to SDIP-22 package, and the circuit of SOP-20 removed two NC pins, and others are the same as the above circuit.

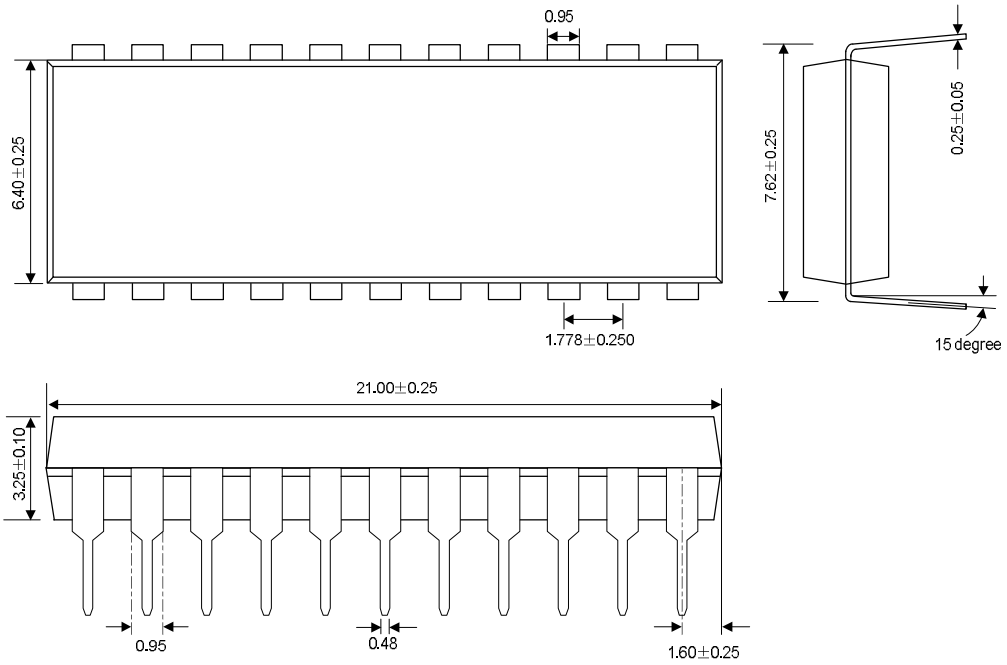
TYPICAL APPLICATION CIRCUIT



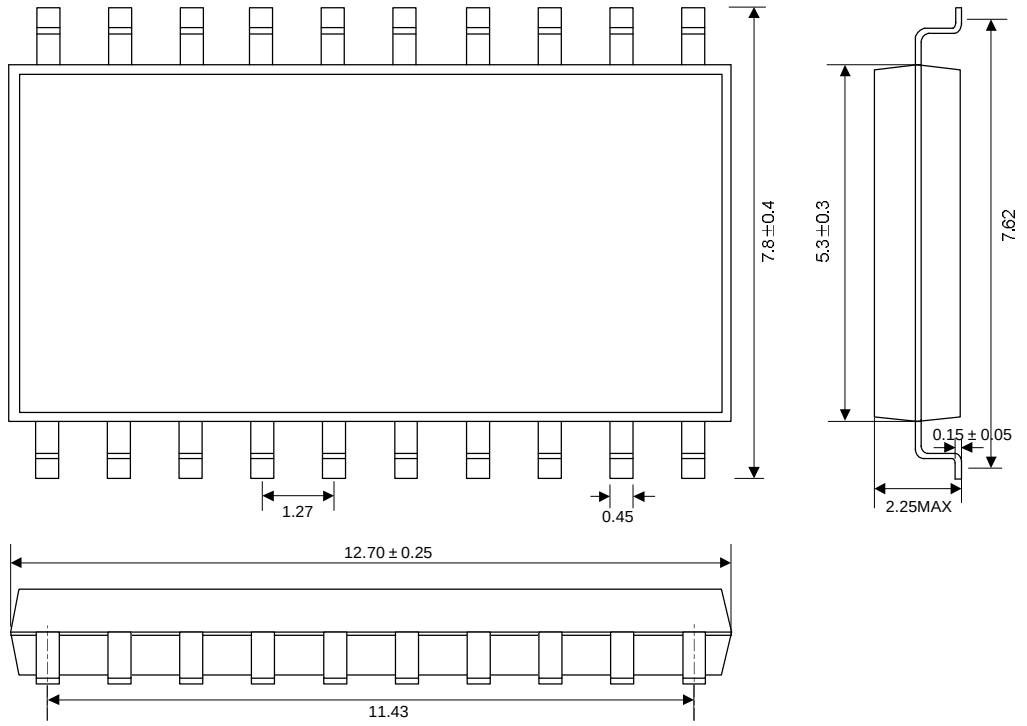
Note: this circuit according to SDIP-22 package, and the circuit of SOP-20 removed two NC pins, and others are the same as the above circuit.

PACKAGE OUTLINE

SDIP-22-300-1.778 UNIT: mm



SOP-20-300-1.27 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.