MICRON TECHNOLOGY, INC.

4 MEG x 4 EDO DRAM

DRAM

MT4LC4M4E8, MT4C4M4E8
MT4LC4M4E9, MT4C4M4E9

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- State-of-the-art, high-performance, low-power CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or +5V ±10%)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, HIDDEN and CAS#-BEFORE-RAS# (CBR)
- Optional Self Refresh (S) for low-power data retention
- 11 row, 11 column addresses (2K refresh) or 12 row, 10 column addresses (4K refresh)
- Extended Data-Out (EDO) PAGE MODE access cycle
- 5V-tolerant inputs and I/Os on 3.3V devices

OPTIONS — MARKING

- Voltages
  - 3.3V — LC
  - 5V — C
- Refresh Addressing
  - 2,048 (i.e. 2K) Rows — E8
  - 4,096 (i.e. 4K) Rows — E9
- Packages
  - Plastic SOJ (300 mil) — DJ
  - Plastic TSOP (300 mil) — TG
- Timing
  - 50ns access — -5
  - 60ns access — -6
- Refresh Rates
  - Standard Refresh — None
  - Self Refresh (128ms period) — S
- Part Number Example: MT4LC4M4E8DJ-6

Note: *The 4 Meg x 4 EDO DRAM base number differentiates the offerings in two places -* MT4LC4M4E8. *The third field distinguishes the low voltage offering: LC designates V_{CC} = 3.3V and C designates V_{CC} = 5V. The fifth field distinguishes various options: E8 designates a 2K refresh and E9 designates a 4K refresh for EDO DRAMs.*

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ (DA-2)

V_{CC}	1	26	V_{SS}
DQ1	2	25	DQ4
DQ2	3	24	DQ3
WE#	4	23	CAS#
RAS#	5	22	OE#
*NC/A11	6	21	A9
A10	8	19	A8
A0	9	18	A7
A1	10	17	A6
A2	11	16	A5
A3	12	15	A4
V_{CC}	13	14	V_{SS}

24/26-Pin TSOP (DB-2)

V_{CC}	1	26	V_{SS}
DQ1	2	25	DQ4
DQ2	3	24	DQ3
WE#	4	23	CAS#
RAS#	5	22	OE#
*NC/A11	6	21	A9
A10	8	19	A8
A0	9	18	A7
A1	10	17	A6
A2	11	16	A5
A3	12	15	A4
V_{CC}	13	14	V_{SS}

* NC on 2K refresh and A11 on 4K refresh options.

Note: The "#" symbol indicates signal is active LOW.

4 MEG x 4 EDO DRAM PART NUMBERS

PART NUMBER	Vcc	REFRESH	PACKAGE	REFRESH
MT4LC4M4E8DJ	3.3V	2K	SOJ	Standard
MT4LC4M4E8DJS	3.3V	2K	SOJ	Self
MT4LC4M4E8TG	3.3V	2K	TSOP	Standard
MT4LC4M4E8TGS	3.3V	2K	TSOP	Self
MT4LC4M4E9DJ	3.3V	4K	SOJ	Standard
MT4LC4M4E9DJS	3.3V	4K	SOJ	Self
MT4LC4M4E9TG	3.3V	4K	TSOP	Standard
MT4LC4M4E9TGS	3.3V	4K	TSOP	Self
MT4C4M4E8DJ	5V	2K	SOJ	Standard
MT4C4M4E8DJS	5V	2K	SOJ	Self
MT4C4M4E8TG	5V	2K	TSOP	Standard
MT4C4M4E8TGS	5V	2K	TSOP	Self
MT4C4M4E9DJ	5V	4K	SOJ	Standard
MT4C4M4E9DJS	5V	4K	SOJ	Self
MT4C4M4E9TG	5V	4K	TSOP	Standard
MT4C4M4E9TGS	5V	4K	TSOP	Self

GENERAL DESCRIPTION

The 4 Meg x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 configuration. RAS# is used to latch the row address (first 11 bits for 2K and first 12 bits for 4K). Once the page has been opened by RAS#, CAS# is used to latch the column address

GENERAL DESCRIPTION (continued)

(the latter 11 bits for 2K and the latter 10 bits for 4K, address pins A10 and A11 are "don't care"). READ and WRITE cycles are selected with the WE# input.

A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE# and OE#.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address-defined page boundary. The PAGE cycle is always initiated with a row address strobed-in by RAS#, followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the PAGE MODE of operation, i.e., closes the page.

EDO PAGE MODE

The 4 Meg x 4 EDO DRAM provides EDO PAGE MODE, which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# returns HIGH. EDO allows CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control allows pipeline READs.

FAST PAGE MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO PAGE MODE DRAMs operate like FAST PAGE MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z (refer to

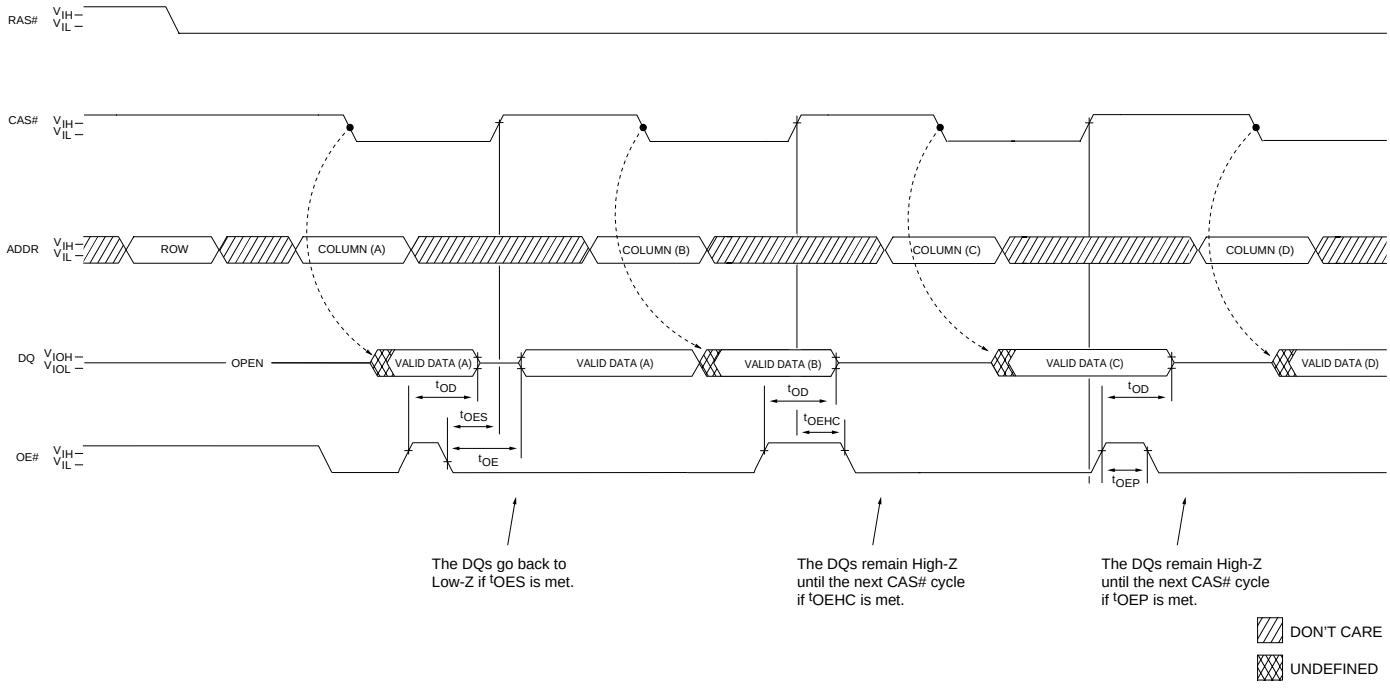


Figure 1
OE# CONTROL OF DQs

Figure 1). WE# can also perform the function of disabling the output devices under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# high time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last.

REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (2,048 for 2K and 4,096 for 4K) are executed within ^{t}REF (MAX), regardless of sequence. The CBR and Self Refresh cycles will invoke the internal refresh counter for automatic RAS# addressing.

An optional Self Refresh mode is also available on the S version. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms. The optional Self Refresh feature is initiated by performing a CBR Refresh cycle and holding RAS# LOW for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh period of 128ms, or 31.25µs per row for a 4K refresh and 62.5µs per row for a 2K refresh if using distributed CBR Refresh. This refresh rate can be applied during normal operation, as well as during a standby or BATTERY BACKUP mode.

The Self Refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting Self Refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

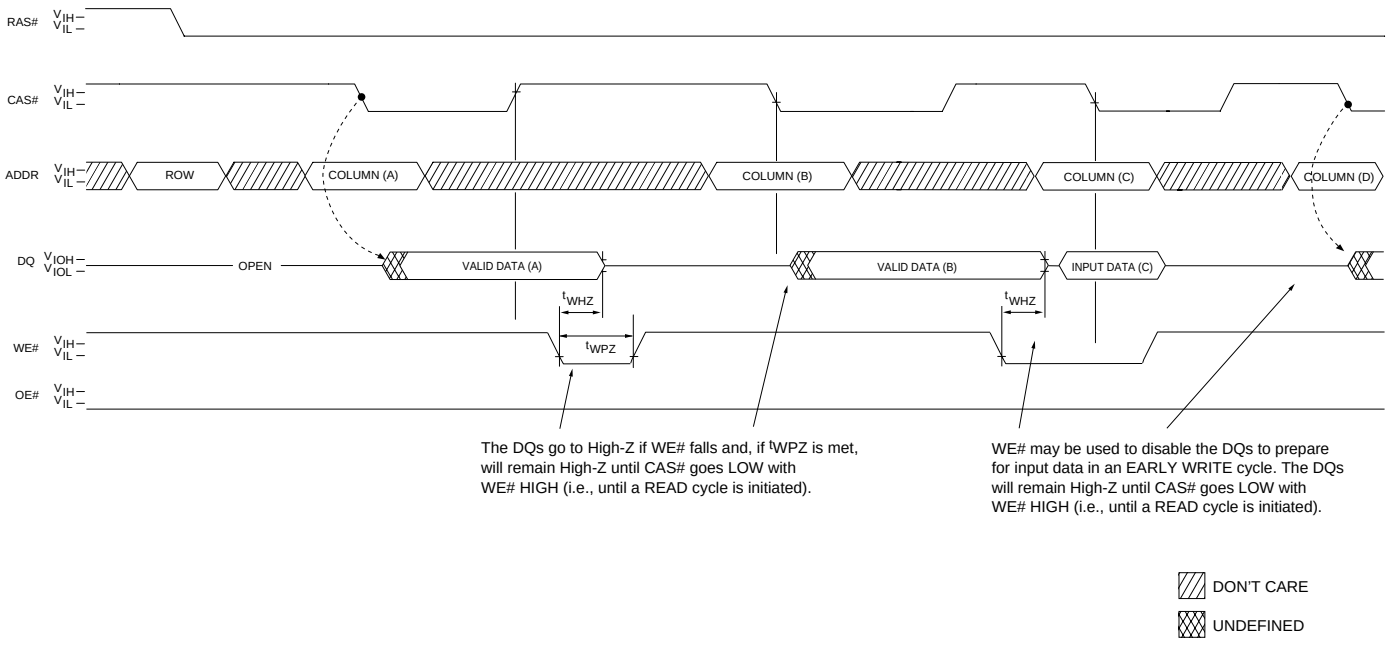
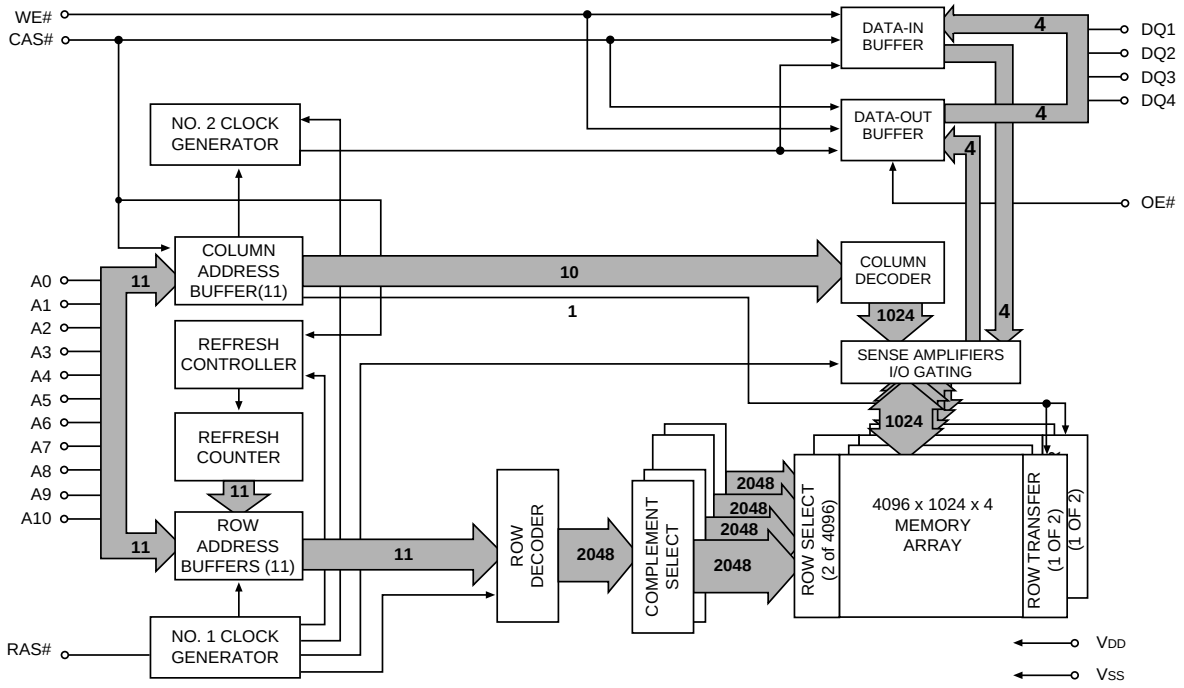
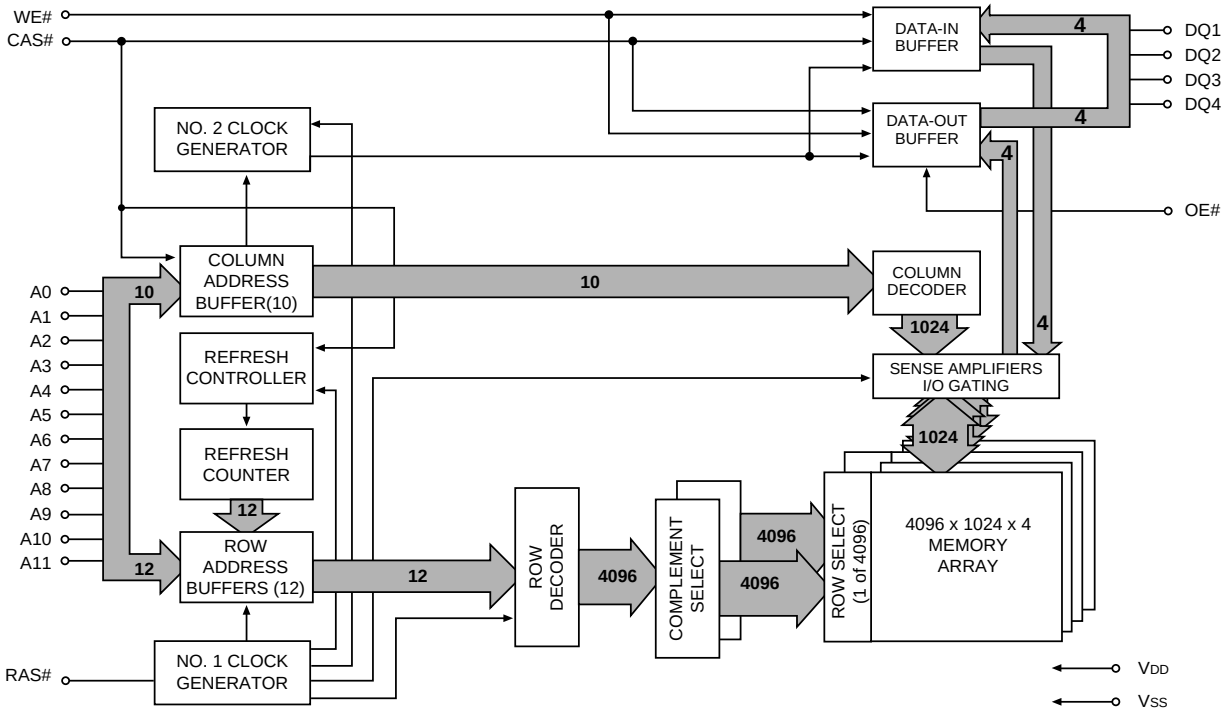


Figure 2
WE# CONTROL OF DQs

FUNCTIONAL BLOCK DIAGRAM - 2K REFRESH



FUNCTIONAL BLOCK DIAGRAM - 4K REFRESH



TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	OE#	ADDRESSES		DATA-IN/OUT
						^tR	^tC	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
EARLY WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
	Any Cycle	L	L→H	H	L	n/a	n/a	Data-Out
EDO-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
RAS#-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS}:
- 3.3V ..... -1V to +4.6V
- 5V ..... -1V to +7V

Voltage on NC, Inputs or I/O Pins Relative to V_{SS}:
- 3.3V ..... -1V to +5.5V
- 5V ..... -1V to +7V

Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1)

PARAMETER/CONDITION	SYMBOL	3.3V		5V		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Supply Voltage	V_{CC}	3.0	3.6	4.5	5.5	V	
Input High Voltage: Valid Logic 1; all inputs, I/Os and any NC	V_{IH}	2.0	5.5	2.4	V_{CC} +1	V	
Input Low Voltage: Valid Logic 0; all inputs, I/Os and any NC	V_{IL}	-1.0	0.8	-0.5	0.8	V	
Input Leakage Current: Any input at V_{IN} ($0V \le V_{IN} \le V_{IH}$ [MAX]); all other pins not under test = 0V	I_I	-2	2	-2	2	µA	4
Output High Voltage: I_{OUT} = -2mA (3.3V), -5mA (5V)	V_{OH}	2.4	-	2.4	-	V	
Output Low Voltage: I_{OUT} = 2mA (3.3V), 4.2mA (5V)	V_{OL}	-	0.4	-	0.4	V	
Output Leakage Current: Any output at V_{OUT} ($0V \le V_{OUT} \le 5.5V$); DQ is disabled and in High-Z state	I_{OZ}	-5	5	-5	5	µA	

Icc OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3)

PARAMETER/CONDITION	SYM	SPEED	3.3V		5V		UNITS	NOTES
			2K Refresh	4K Refresh	2K Refresh	4K Refresh		
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	ALL	1	1	1	1	mA	
STANDBY CURRENT: CMOS (non-S version only) (RAS# = CAS# = other inputs = V_{CC} -0.2V)	I_{CC2}	ALL	500	500	500	500	µA	
STANDBY CURRENT: CMOS (S version only) (RAS# = CAS# = other inputs = V_{CC} -0.2V)	I_{CC2}	ALL	150	150	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	-5 -6	110 100	90 80	140 130	120 110	mA	5, 6
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	-5 -6	110 100	100 90	110 100	100 90	mA	5, 6
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	-5 -6	110 100	90 80	140 130	120 110	mA	5, 6
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	-5 -6	110 100	90 80	140 130	120 110	mA	5, 7
REFRESH CURRENT: Extended (S version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = ^tRAS (MIN); WE# = V_{CC} -0.2V; A0-A11,OE# and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC7}	ALL	300	300	300	300	µA	5, 7
		^tRC	62.5	31.25	62.5	31.25	µs	25
REFRESH CURRENT: Self (S version only) Average power supply current: CBR with RAS# ≥ ^tRASS (MIN) and CAS# held LOW; WE# = V_{CC} -0.2V; A0-A11, OE# and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	ALL	300	300	300	300	µA	5, 7

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	8
Input Capacitance: RAS#, CAS#, WE#, OE#	C_{I2}	7	pF	8
Input/Output Capacitance: DQ	C_{IO}	7	pF	8

AC ELECTRICAL CHARACTERISTICS

(Notes: 2, 3, 9, 10, 11, 12, 17) (V_{CC} [MIN] ≤ V_{CC} ≤ V_{CC} [MAX])

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column address setup to CAS# precharge	^tACH	12		15		ns	
Column address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column address setup time	^tASC	0		0		ns	
Row address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	42		49		ns	13
Access time from CAS#	^tCAC		13		15	ns	14
Column address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# LOW to “don’t care” during Self Refresh	^tCHD	15		15		ns	
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	7
CAS# to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after next CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	15
Access time from CAS# precharge	^tCPA		28		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	38		45		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	
CAS# to WE# delay time	^tCWD	28		35		ns	13
Write command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	8		10		ns	16
Data-in setup time	^tDS	0		0		ns	16
Output disable	^tOD	0	12	0	15	ns	
Output Enable	^tOE		12		15	ns	17
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	18
OE# HIGH hold from CAS# HIGH	^tOEHC	5		10		ns	18
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	20

AC ELECTRICAL CHARACTERISTICS

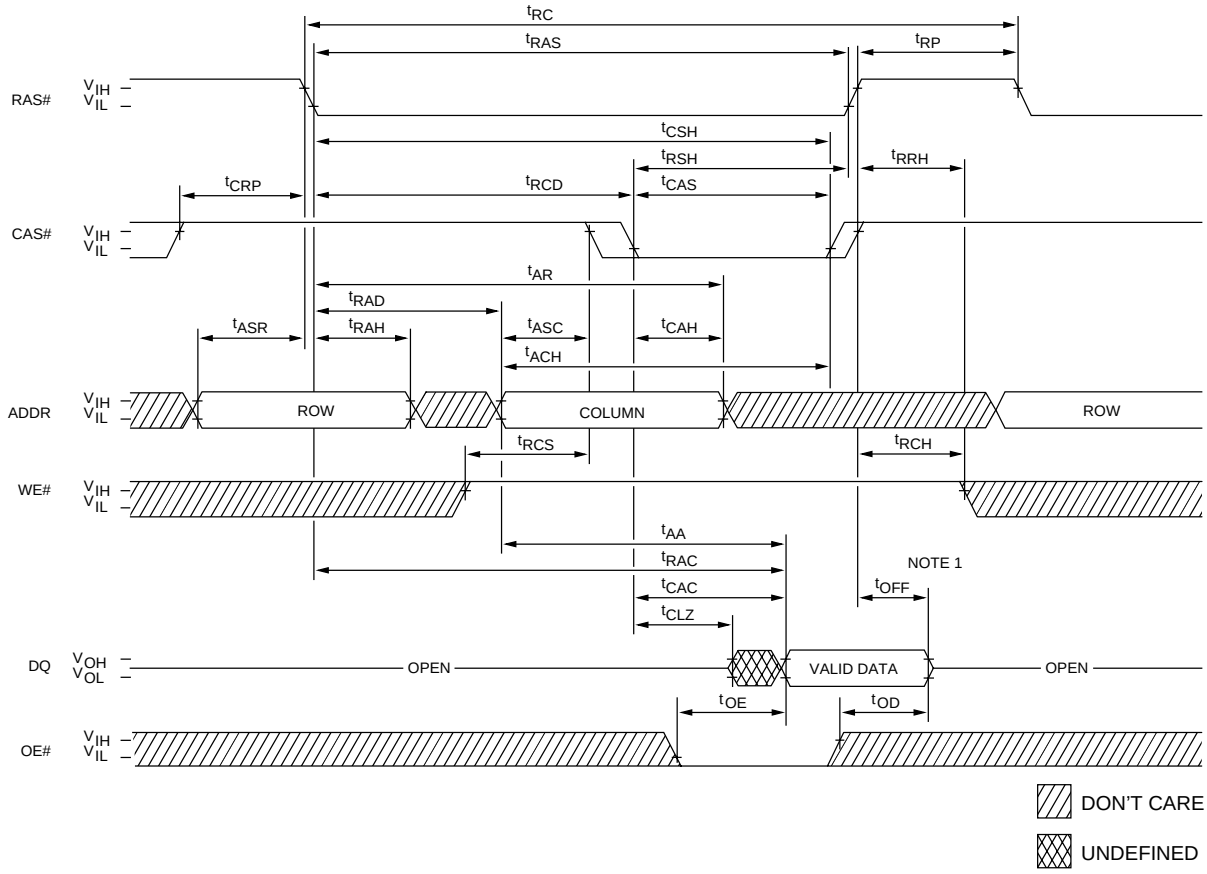
(Notes: 2, 3, 9, 10, 11, 12, 17) (V_{CC} [MIN] ≤ V_{CC} ≤ V_{CC} [MAX])

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	47		56		ns	
Access time from RAS#	^{t}RAC		50		60	ns	19
RAS# to column address delay time	^{t}RAD	9		12		ns	21
Row address hold time	^{t}RAH	9		10		ns	
RAS# pulse width	^{t}RAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^{t}RASP	50	125,000	60	125,000	ns	
RAS# pulse width during Self Refresh	^{t}RASS	100		100		µs	
Random READ or WRITE cycle time	^{t}RC	84		104		ns	
RAS# to CAS# delay time	^{t}RCD	11		14		ns	22
Read command hold time (referenced to CAS#)	^{t}RCH	0		0		ns	23
Read command setup time	^{t}RCS	0		0		ns	
Refresh period (2,048 cycles)	^{t}REF		32		32	ms	
Refresh period (4,096 cycles)	^{t}REF		64		64	ms	
Refresh period S version	^{t}REF		128		128	ms	
RAS# precharge time	^{t}RP	30		40		ns	
RAS# to CAS# precharge time	^{t}RPC	5		5		ns	
RAS# precharge time exiting Self Refresh	^{t}RPS	90		105		ns	
Read command hold time (referenced to RAS#)	^{t}RRH	0		0		ns	23
RAS# hold time	^{t}RSH	13		15		ns	
READ WRITE cycle time	^{t}RWC	116		140		ns	
RAS# to WE# delay time	^{t}RWD	67		79		ns	13
Write command to RAS# lead time	^{t}RWL	13		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
Write command hold time	^{t}WCH	8		10		ns	
Write command hold time (referenced to RAS#)	^{t}WCR	38		45		ns	
WE# command setup time	^{t}WCS	0		0		ns	13
Output disable delay from WE#	^{t}WHZ	0	12	0	15	ns	
Write command pulse width	^{t}WP	5		5		ns	
WE# pulse to disable at CAS# HIGH	^{t}WPZ	10		10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	8		10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	8		10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \le T_A \le 70^{\circ}C$) is ensured.
3. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. NC pins are assumed to be left floating and are not tested for leakage.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. Column address changed once each cycle.
7. Enables on-chip refresh and address counters.
8. This parameter is sampled. $V_{CC} = V_{CC_{MIN}}$; f = 1 MHz.
9. AC characteristics assume ^{t}T = 2.5ns.
10. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
11. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
12. Measured with a load equivalent to two TTL gates and 100pF; and V_{OL} = 0.8V and V_{OH} = 2V.
13. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \ge {}^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}WCS < {}^{t}WCS$ (MIN) and $^{t}RWD \ge {}^{t}RWD$ (MIN), $^{t}AWD \ge {}^{t}AWD$ (MIN) and $^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
14. Requires that ^{t}AA and ^{t}RAC are not violated.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
16. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
17. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^{t}OEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
19. Requires that ^{t}AA and ^{t}CAC are not violated.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of RAS# or CAS#, whichever occurs last.
21. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
22. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD limit, ^{t}AA and ^{t}CAC must always be met.
23. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.
25. The refresh period is extended from 32ms (2K refresh) or 64ms (4K refresh) to 128ms (both 2K and 4K refreshes). For 4K refresh, ^{t}RC = 31.25µs (128ms / 4,096 rows = 31.25µs) and for 2K refresh, ^{t}RC = 62.5µs (128ms / 2,048 rows = 62.5µs).

READ CYCLE



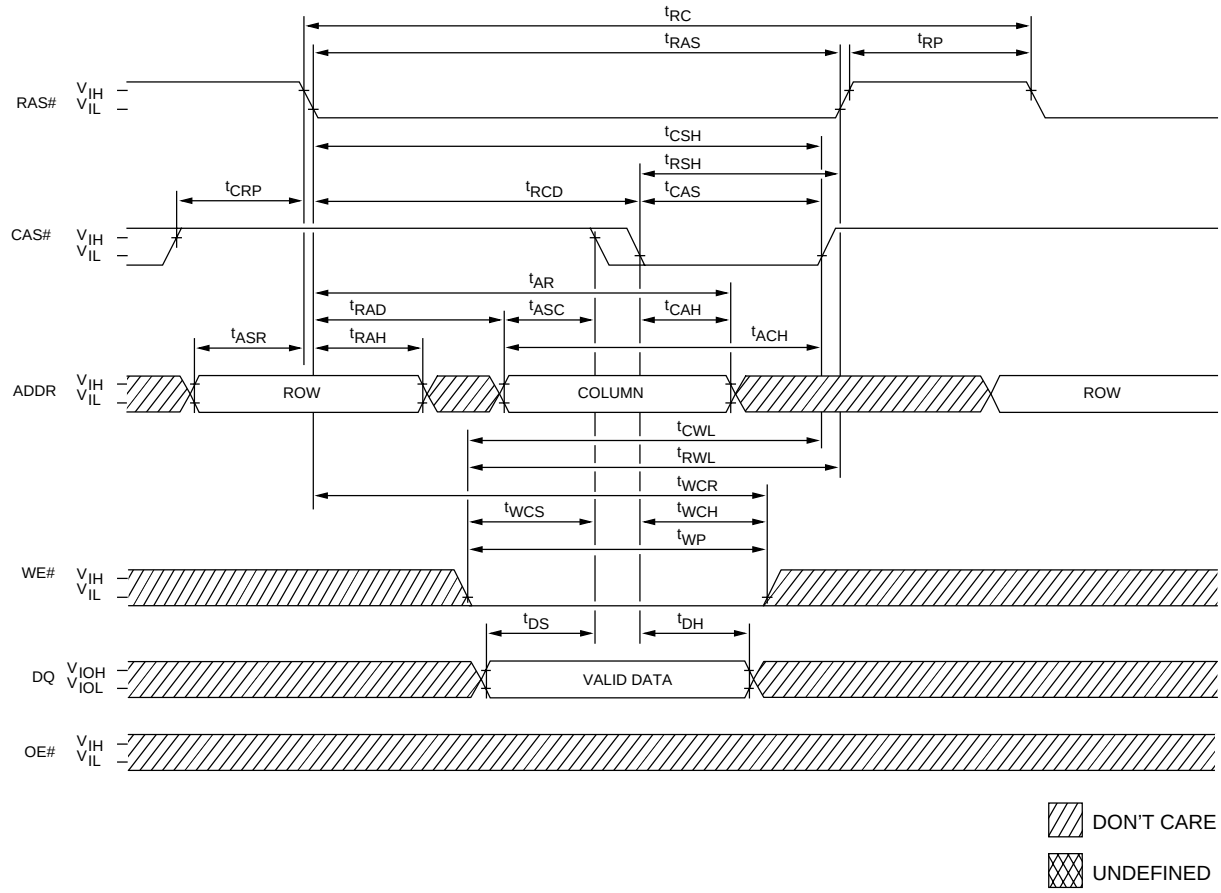
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	0	12	0	15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

NOTE: 1. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE

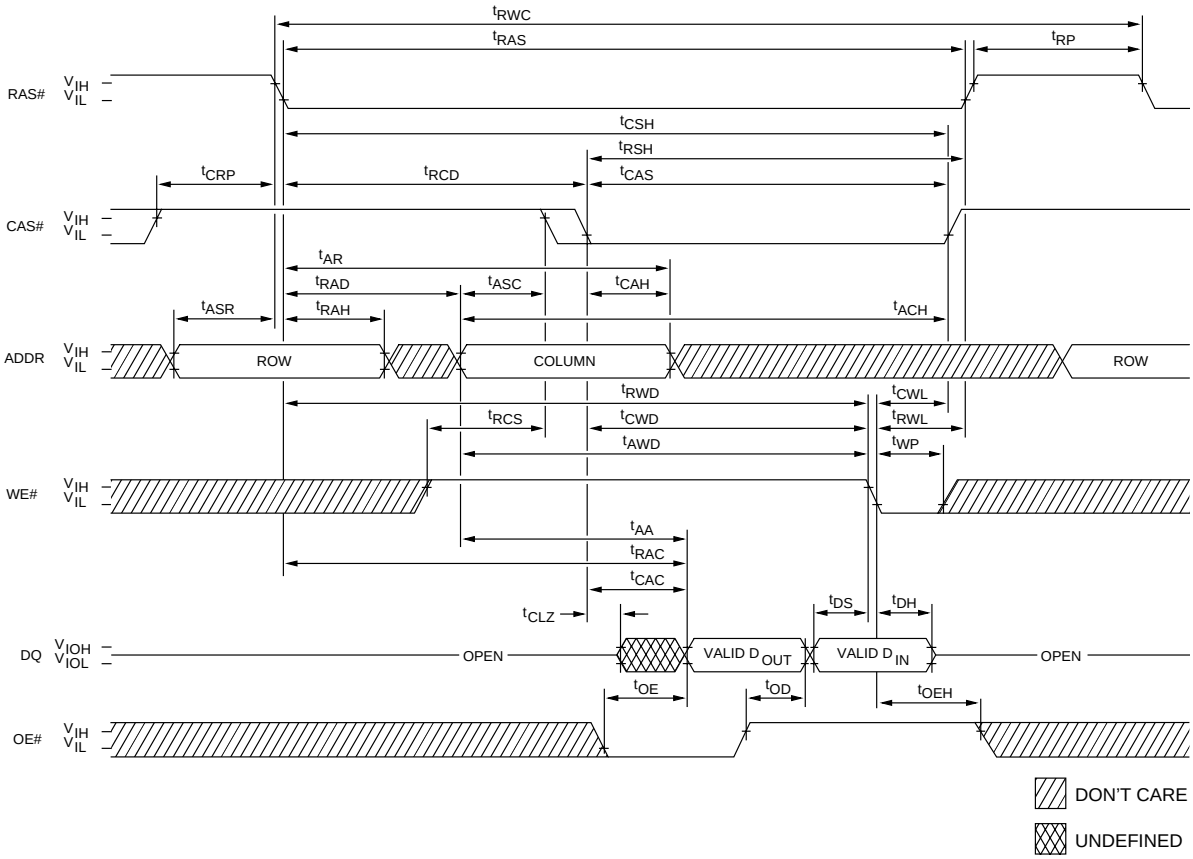


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD	9		12		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

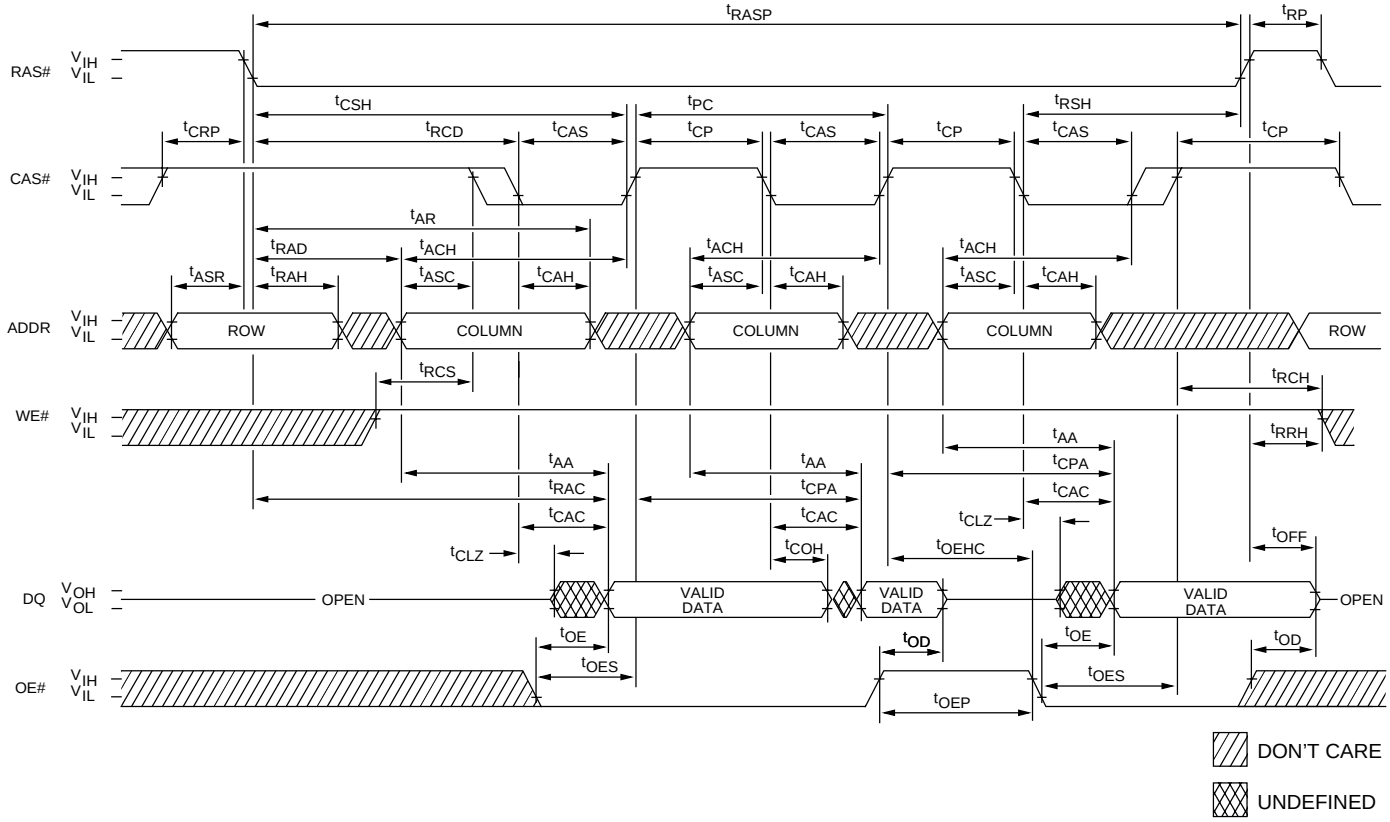


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tAWD	42		49		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC	116		140		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

EDO-PAGE-MODE READ CYCLE

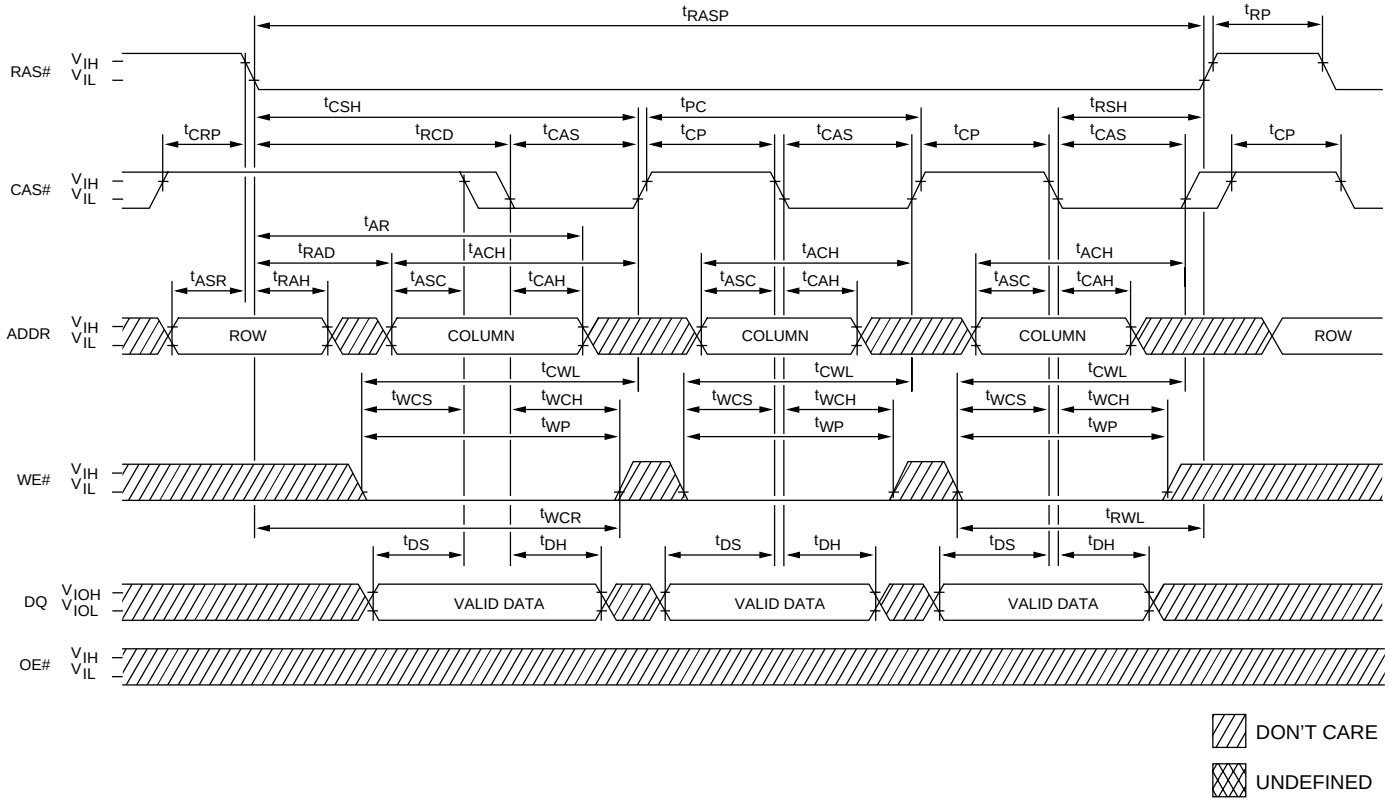


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

EDO-PAGE-MODE EARLY WRITE CYCLE

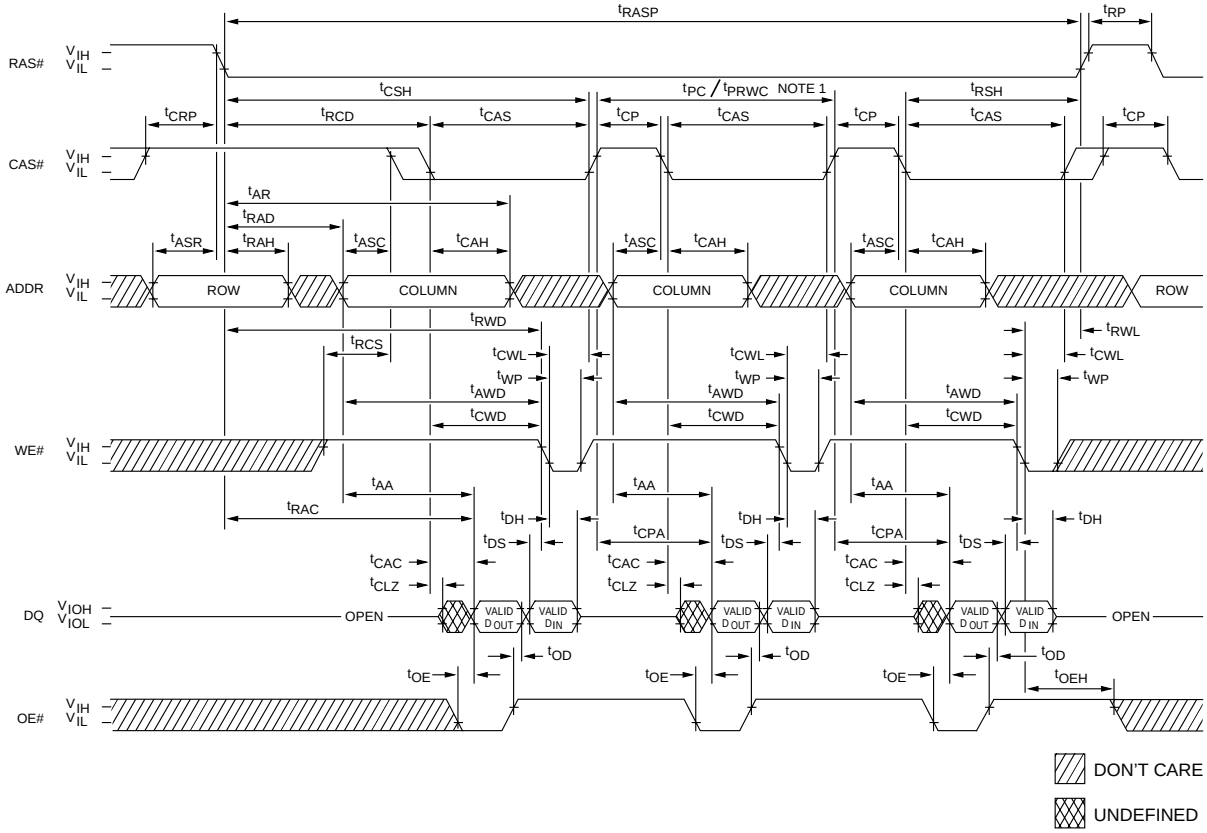


TIMING PARAMETERS

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tPC	20		25		ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



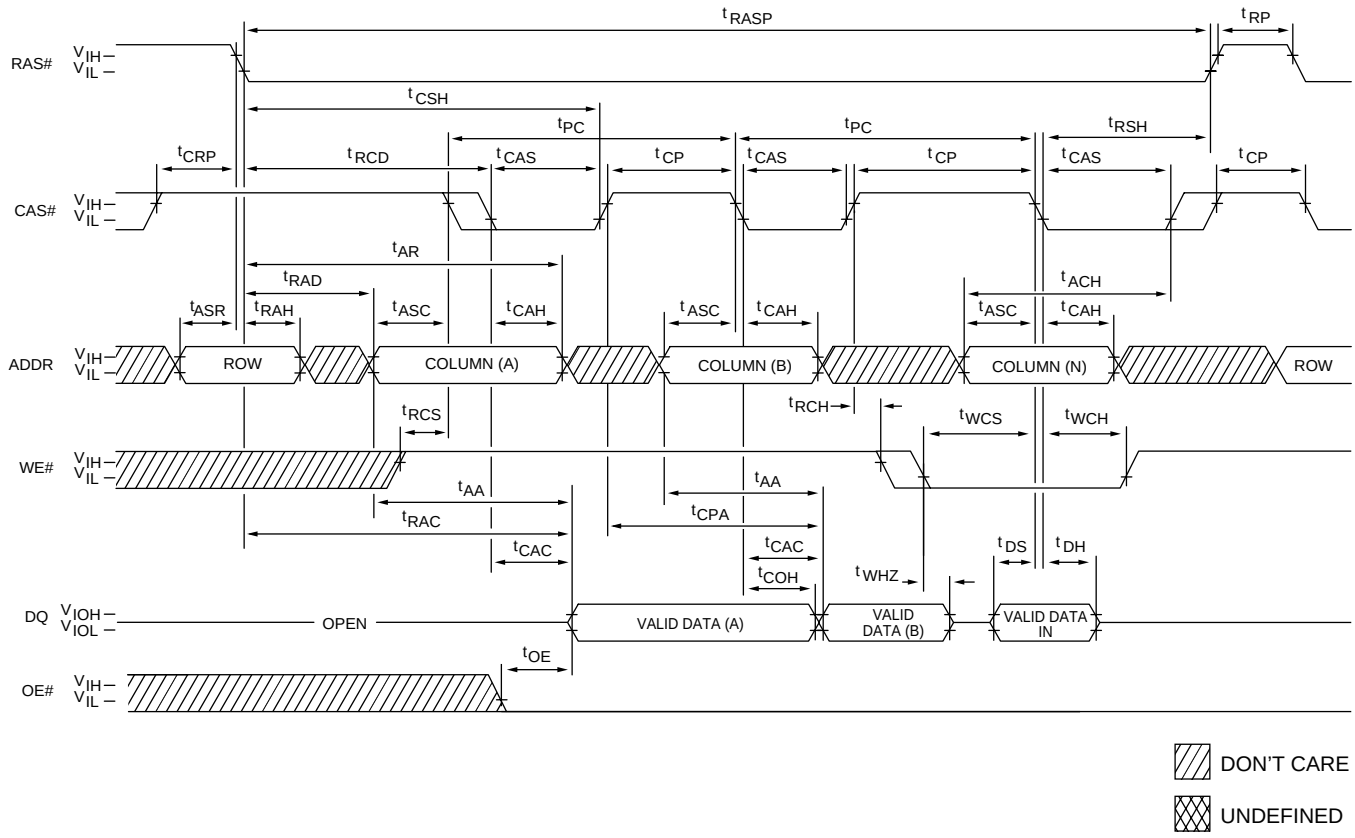
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tPC	20		25		ns
tPRWC	47		56		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

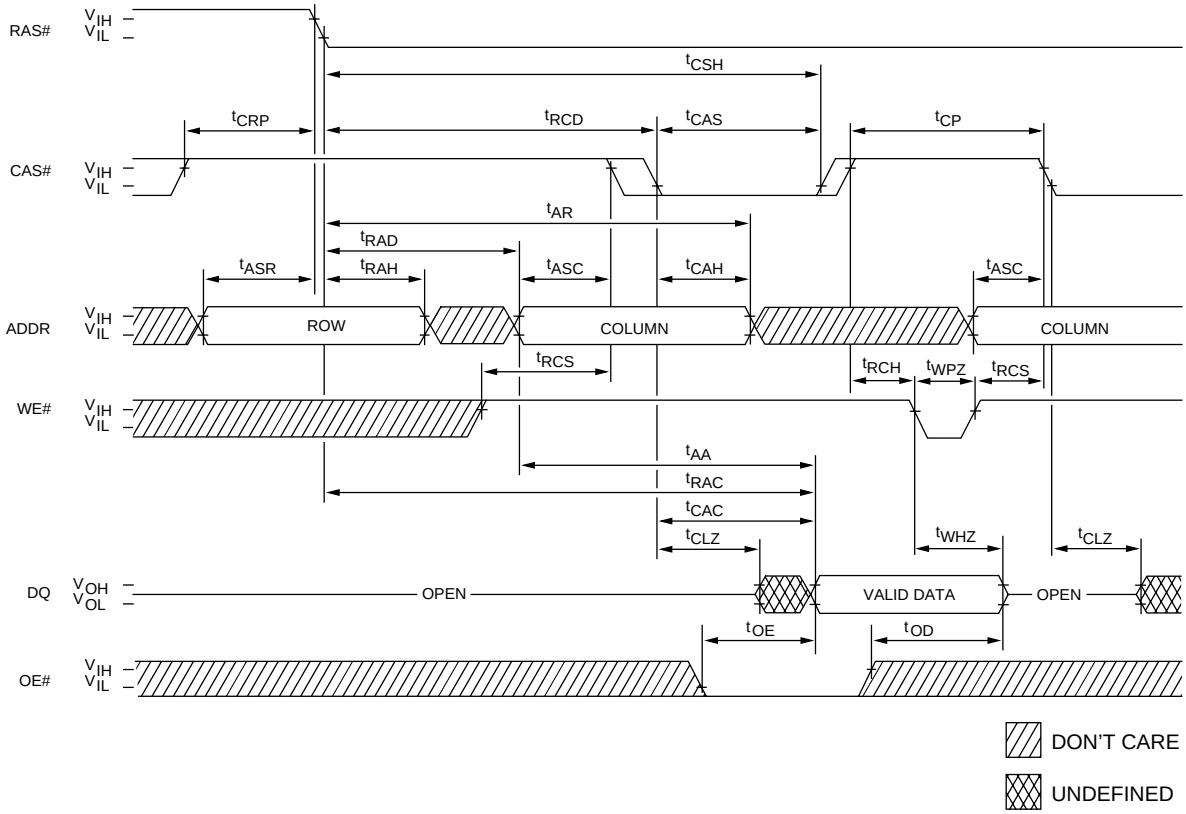


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns

READ CYCLE
(With WE#-controlled disable)



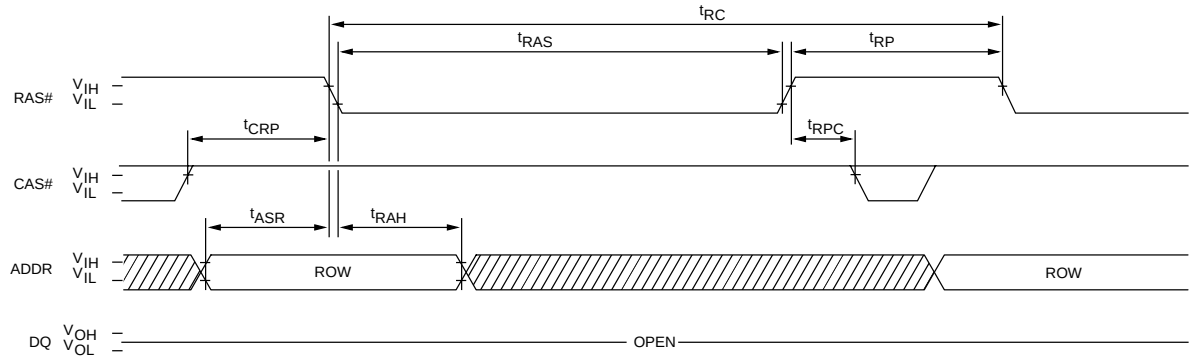
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ	0	12	0	15	ns
tWPZ	10		10		ns

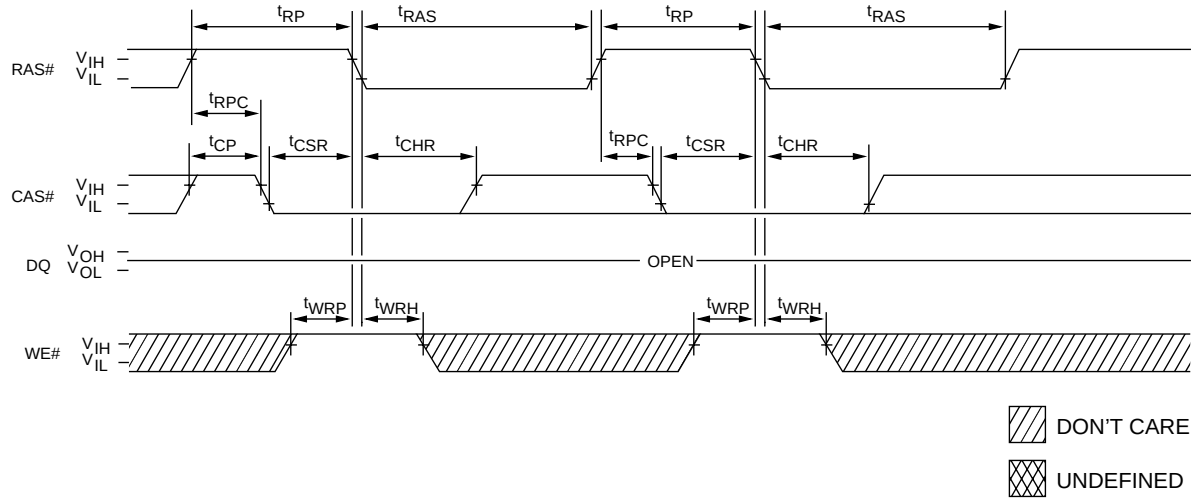
RAS#-ONLY REFRESH CYCLE

(OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE

(Addresses and OE# = DON'T CARE)

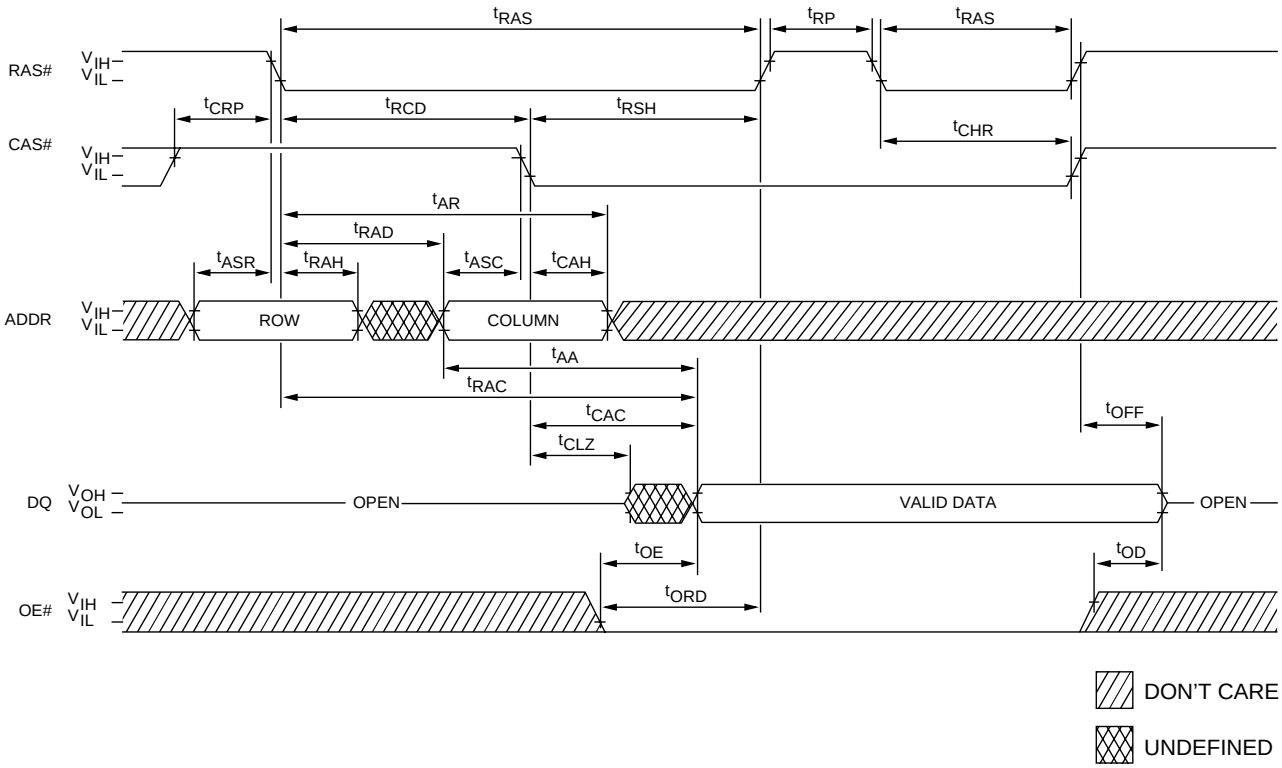


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCHR	8		10		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	9		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	8		10		ns
tWRP	8		10		ns

HIDDEN REFRESH CYCLE [24]
(WE# = HIGH; OE# = LOW)

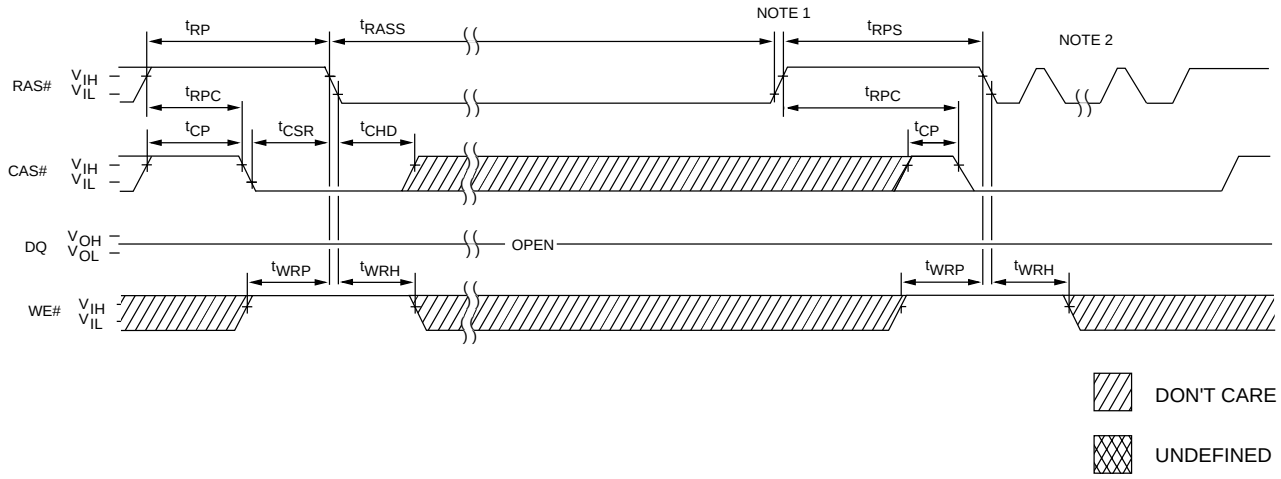


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR	8		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



TIMING PARAMETERS

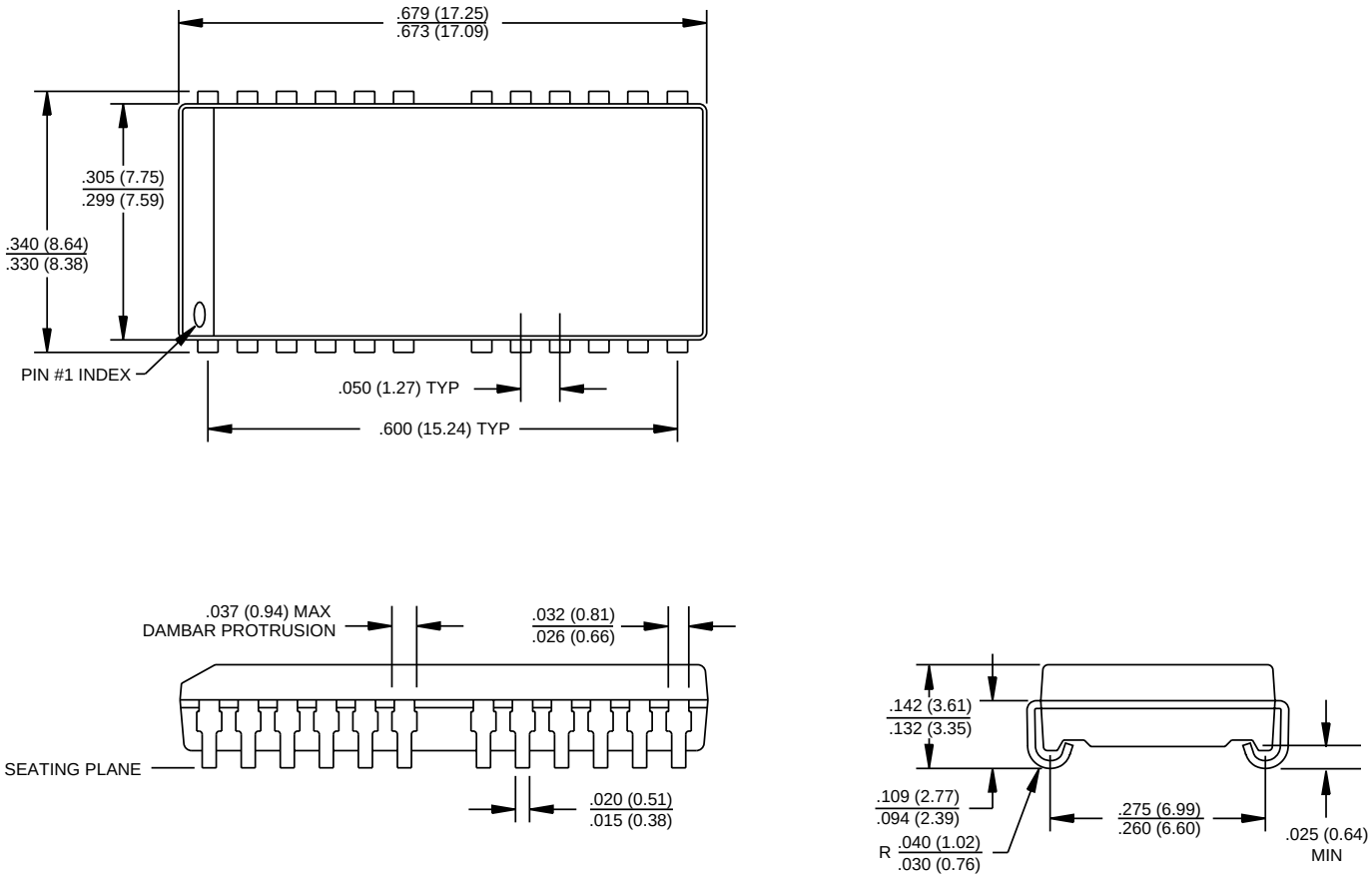
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCHD	15		15		ns
tCP	8		10		ns
tCSR	5		5		ns
tRASS	100		100		µs
tRP	30		40		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRPC	5		5		ns
tRPS	90		105		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTE: 1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter Self Refresh mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

24/26-PIN PLASTIC SOJ (300 mil)

DA-2

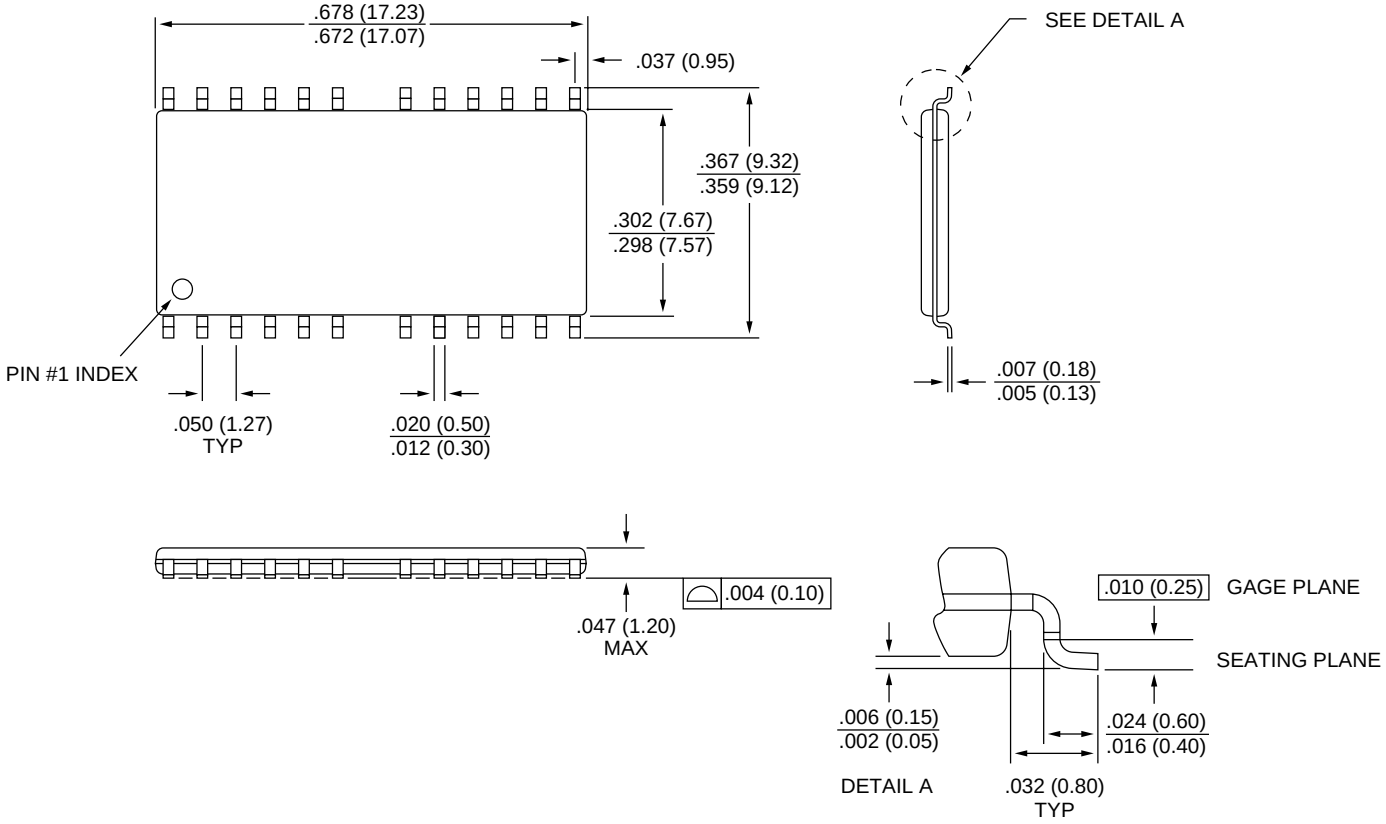


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24/26-PIN PLASTIC TSOP (300 mil)

DB-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

Technology that works for you.

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