INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4001B gates Quadruple 2-input NOR gate

Product specification
File under Integrated Circuits, IC04

January 1995





Quadruple 2-input NOR gate

HEF4001B gates

DESCRIPTION

The HEF4001B provides the positive quadruple 2-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

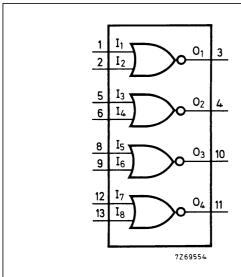
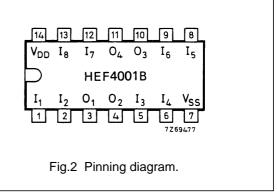


Fig.1 Functional diagram.



HEF4001BP(N): 14-lead DIL; plastic

(SOT27-1)

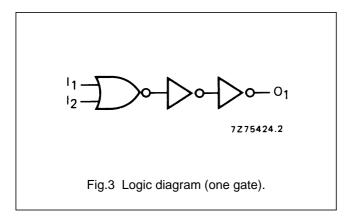
HEF4001BD(F): 14-lead DIL; ceramic (cerdip)

(SOT73)

HEF4001BT(D): 14-lead SO; plastic

(SOT108-1)

(): Package Designator North America



FAMILY DATA, IDD LIMITS category GATES

See Family Specifications

Philips Semiconductors Product specification

Quadruple 2-input NOR gate

HEF4001B gates

AC CHARACTERISTICS

 V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times \leq 20 ns

	V _{DD}	SYMBOL	TYP	MAX		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \rightarrow O_n$	5		60	120	ns	33 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C _L
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L
	5		50	100	ns	23 ns + (0,55 ns/pF) C _L
LOW to HIGH	10	t _{PLH}	25	45	ns	14 ns + (0,23 ns/pF) C _L
	15		20	35	ns	12 ns + (0,16 ns/pF) C _L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C _L
HIGH to LOW	10	t _{THL}	30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
	5		60	120	ns	10 ns + (1,0 ns/pF) C _L
LOW to HIGH	10	t _{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V _{DD}	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	1100 $f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	5000 $f_i + \sum (f_o C_L) \times V_{DD}^2$	f _i = input freq. (MHz)
package (P)	15	14 200 $f_i + \sum (f_o C_L) \times V_{DD}^2$	f _o = output freq. (MHz)
			C _L = load capacitance (pF)
			$\sum (f_o C_L) = \text{sum of outputs}$
			V _{DD} = supply voltage (V)