Computer Organization

COMP2120

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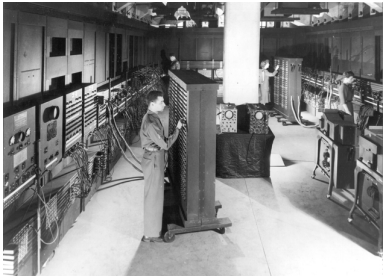
Evolution of Computers

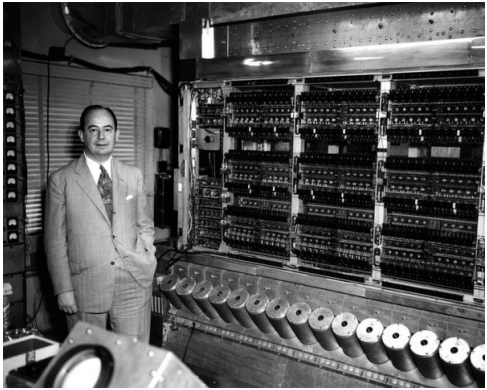
The 1st generation — vacuum tubes (1946-1957)

- the 1st computer — ENIAC (Electronic Numerical Integrator And Computer), 18,000 vacuum tubes and 1500 square feet, 30 tons, and use 140kW of power.
- World War II, Artillery firing table, nuclear weapon, University of Pennsylvania
- Manual programming



The First Modern Computer — the IAS Machine

- Developed by von Neumann, Institute of Advanced Studies (IAS) at Princeton University.
- First General Purpose Computer designed (i.e. programmable).
- Using the concept of stored program. Much easier to re-program.



The IAS Computer

- Main memory, store data and programs (instruction)
- Arithmetic and logic unit (ALU)
- Control unit
- I/O

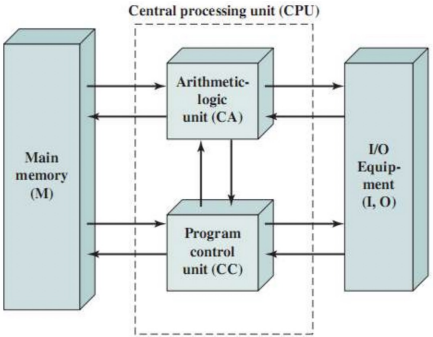


Figure 2.1 Structure of the IAS Computer

Milestones in Computer Architecture

- The 1st generation — vacuum tubes
- The 2nd generation — transistors
- The 3rd generation — Integrated Circuits (IC)
- The 4th generation — Very Large Scale Integration IC (VLSI)

Performance Evolution

Table 1.2 Computer Generations

Generation	Approximate Dates	Technology	Typical Speed (operations per second)
1	1946–1957	Vacuum tube	40,000
2	1957–1964	Transistor	200,000
3	1965–1971	Small- and medium-scale integration	1,000,000
4	1972–1977	Large scale integration	10,000,000
5	1978–1991	Very large scale integration	100,000,000
6	1991–	Ultra large scale integration	>1,000,000,000

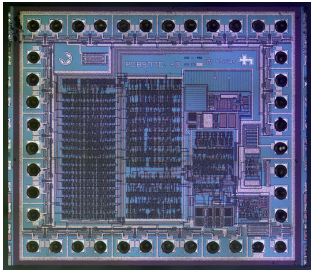
The 2nd generation-transistors (1958-1964)

- transistor was invented in 1948, one of the greatest inventions of the 20th century, 1956 Nobel Prize in Physics

- Smaller, faster, cheaper, more reliable
- Examples: TX-0 (1956), PDP-8, IBM 1401, CDC 1604
- Magnetic cores as primary memory
- Each component manufactured separately
- Disadvantages: Very costly for commercial use, required frequent maintenance, frequent cooling also required.

The 3rd generation — Integrated Circuits (1965-1977)

- IC was first invented by Kilby at Texas Instrument. 2000 Nobel Prize in physics



- punch card $\Longrightarrow$ mouse and keyboard
- high-level programming languages
- Concepts of Computer Families — Computers that execute the same program, but varies in performance, e.g. IBM S/360 and later S/370.

The 4th generation — Very Large Scale Integration (VLSI)

- personal computer (PC) revolution
- microprocessor was developed — Intel 4004, 4040, 8080, 8086, ...
- operating system for micros — CP/M, MSDOS, Windows, ...
- high performance workstations to replace mainframe computers.

Moore's Law

- Number of transistors in a chip doubles every 18 months.
- Transistor Count: i9-12900K, 2.95 billion transistors; M3 Max, 92 billion transistors

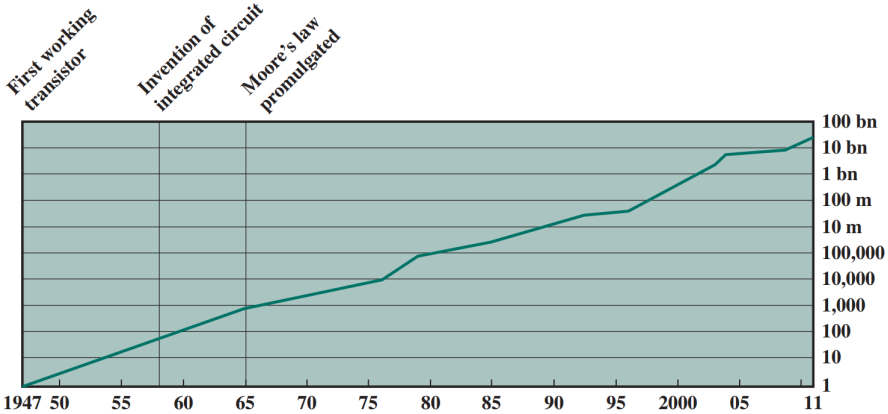


Figure 1.12 Growth in Transistor Count on Integrated Circuits

Evolution of Intel Processors

Table 1.3 Evolution of Intel Microprocessors (page 1 of 2)

(a) 1970s Processors

	4004	8008	8080	8086	8088
Introduced	1971	1972	1974	1978	1979
Clock speeds	108 kHz	108 kHz	2 MHz	5 MHz, 8 MHz, 10 MHz	5 MHz, 8 MHz
Bus width	4 bits	8 bits	8 bits	16 bits	8 bits
Number of transistors	2,300	3,500	6,000	29,000	29,000
Feature size (μm)	10	8	6	3	6
Addressable memory	640 bytes	16 KB	64 KB	1 MB	1 MB

(b) 1980s Processors

	80286	386TM DX	386TM SX	486TM DX CPU
Introduced	1982	1985	1988	1989
Clock speeds	6–12.5 MHz	16–33 MHz	16–33 MHz	25–50 MHz
Bus width	16 bits	32 bits	16 bits	32 bits
Number of transistors	134,000	275,000	275,000	1.2 million
Feature size (μm)	1.5	1	1	0.8–1
Addressable memory	16 MB	4 GB	16 MB	4 GB
Virtual memory	1 GB	64 TB	64 TB	64 TB
Cache	—	—	—	8 kB

Evolution of Intel Processors

(c) 1990s Processors

	486TM SX	Pentium	Pentium Pro	Pentium II
Introduced	1991	1993	1995	1997
Clock speeds	16–33 MHz	60–166 MHz,	150–200 MHz	200–300 MHz
Bus width	32 bits	32 bits	64 bits	64 bits
Number of transistors	1.185 million	3.1 million	5.5 million	7.5 million
Feature size (μm)	1	0.8	0.6	0.35
Addressable memory	4 GB	4 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB	64 TB
Cache	8 kB	8 kB	512 kB L1 and 1 MB L2	512 kB L2

(d) Recent Processors

	Pentium III	Pentium 4	Core 2 Duo	Core i7 EE 4960X
Introduced	1999	2000	2006	2013
Clock speeds	450–660 MHz	1.3–1.8 GHz	1.06–1.2 GHz	4 GHz
Bus width	64 bits	64 bits	64 bits	64 bits
Number of transistors	9.5 million	42 million	167 million	1.86 billion
Feature size (nm)	250	180	65	22
Addressable memory	64 GB	64 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB	64 TB
Cache	512 kB L2	256 kB L2	2 MB L2	1.5 MB L2/15 MB L3
Number of cores	1	1	2	6

Processors Trend

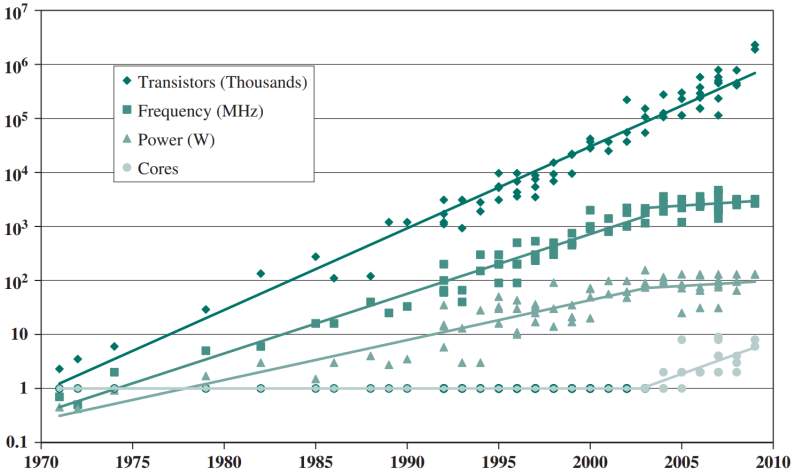
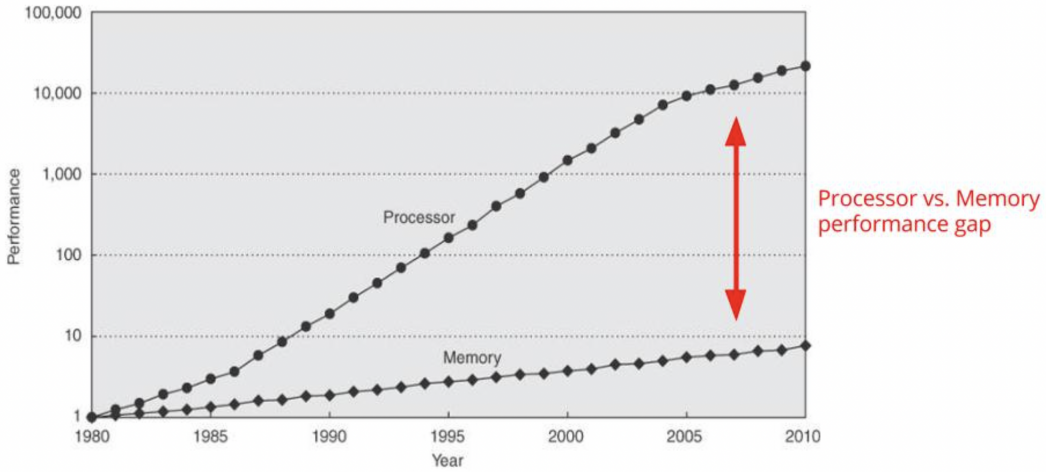


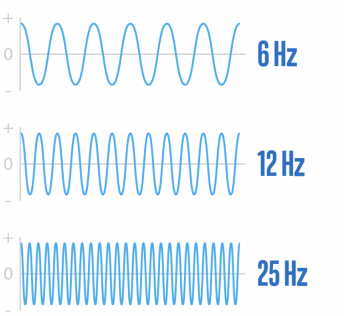
Figure 2.2 Processor Trends

Performance of Logic vs Memory



Benchmark performance

- Clock Speed: the pulse frequency produced by the clock, measured in cycles per second, or Hertz (Hz). Also known as clock rate, clock speed
- A “cycle” is technically a synchronized pulse
- 1 GHz processor: receive 1 billion pulses per second



Benchmark performance

- A program: a lot of instructions, each instruction has several cycles.
- Example: A classic RISC pipeline, with the following five cycles:
  - Instruction fetch cycle (IF).
  - Instruction decode/Register fetch cycle (ID).
  - Execution/Effective address cycle (EX).
  - Memory access (MEM).
  - Write-back cycle (WB)
- Load (5 cycles), Store (4 cycles), Branch (3 cycles), Jump (3 cycles).
- Average cycles per instruction (CPI):

$$CPI = \frac{\sum_i CPI_i \times I_i}{I_c}, \quad I_c = \sum_i I_i$$

processor time T

$$T = \frac{I_c \times CPI}{f}$$

Benchmark performance

- If a program has: 50% load instructions, 25% store instructions, 15% R-type instructions, 8% branch instructions, 2% jump instructions, then, the CPI is:

$$CPI = \frac{5 \times 50 + 4 \times 25 + 4 \times 15 + 3 \times 8 + 3 \times 2}{100} = 4.4$$

- MIPS — Million Instruction per Second

$$MIPS = \frac{f}{CPI \times 10^6}$$

- MFLOPS — Million FLoating point Operations per Second.

Benchmark performance

- MIPS and MFLOPS may not accurately reflect the performance of a computer. Why not ??

EXAMPLE 2.8 Consider this high-level language statement:

```
A = B + C   /* assume all quantities in main memory */
```

With a traditional instruction set architecture, referred to as a complex instruction set computer (CISC), this instruction can be compiled into one processor instruction:

```
add   mem(B), mem(C), mem (A)
```

On a typical RISC machine, the compilation would look something like this:

```
load  mem(B), reg(1);
load  mem(C), reg(2);
add   reg(1), reg(2), reg(3);
store reg(3), mem (A)
```

- Better to actually measure the time required to do some real jobs — SPEC marks. (Standard Performance Evaluation Corporation)