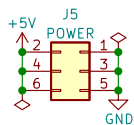
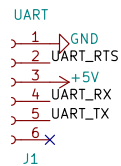
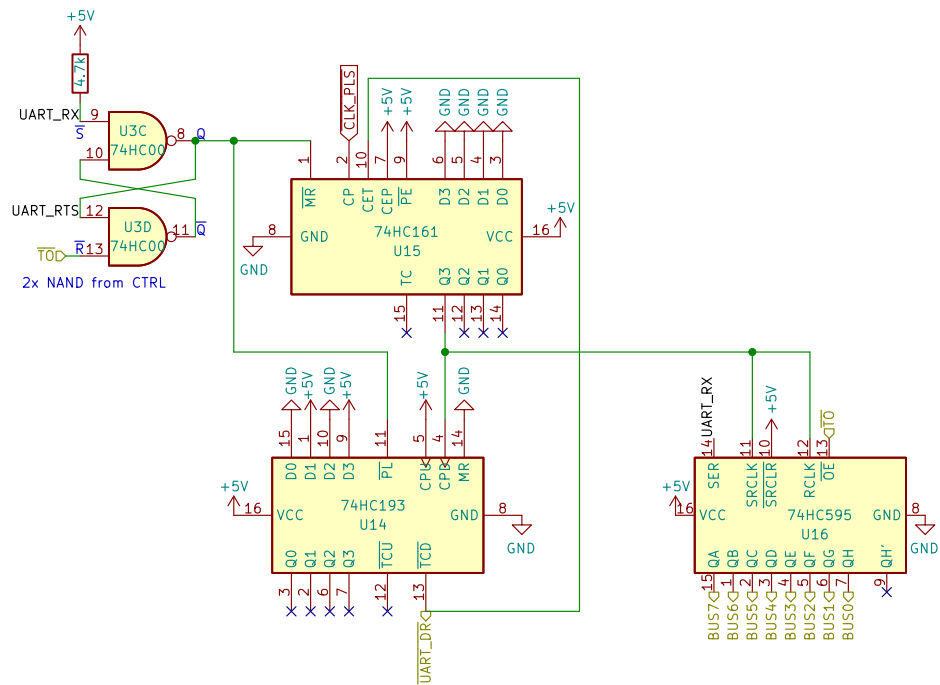


UART bitrate 500kbps, 1 start bit, 8 data bits,  
2 stop bits, new line LF, transmit line delay 10ms.



When using a USB-to-serial converter featuring CH340G (not FT232, CP2102) you may use RTS/CTS flow control and omit the line delay for faster data transmission.

Just connect the RTS output ("I am ready to receive") to the CTS input ("You are clear to send" input) of your receiver.



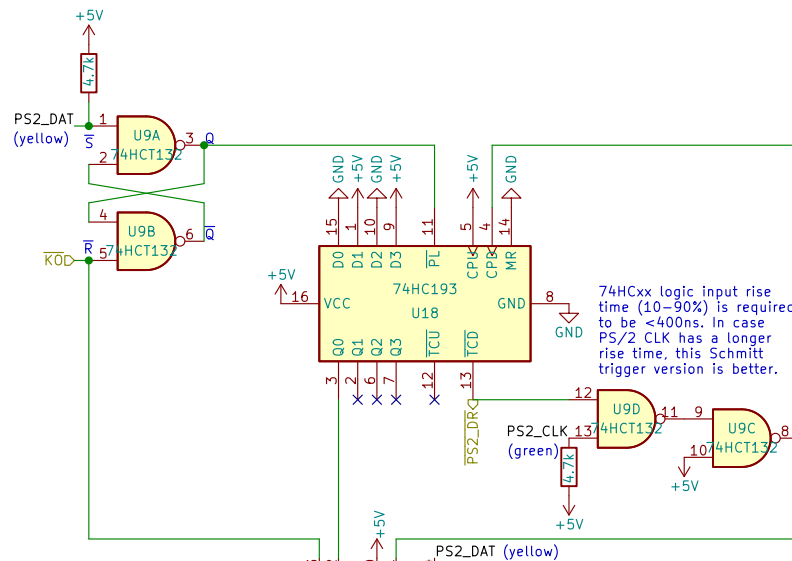
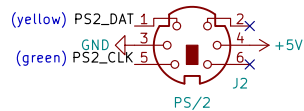
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Sheet: /UART/  
File: UART\_RX.kicad\_sch

### Title: UART Section

Size: A4 Date: 2023-12-11  
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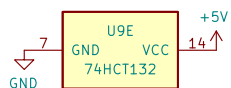


TCD goes LOW at the falling edge of CPD at the beginning of the high stop bit ensuring that a full transmission has been read. Since the last processed bit is the P bit and since the output register is always one clock behind, the output contains the 8 data bits.

The order of the bits is intentionally reversed.

74HCxx logic input rise time (10–90%) is required to be <400ns. In case PS/2 CLK has a longer rise time, this Schmitt trigger version is better.

I am using a 74HC132 (NAND with Schmitt-trigger inputs) rather than the standard 74HC00 here, since PS/2 signals can have rather large rise and fall time. For PS/2 devices with lower (3.3V) output use 74HCT132.



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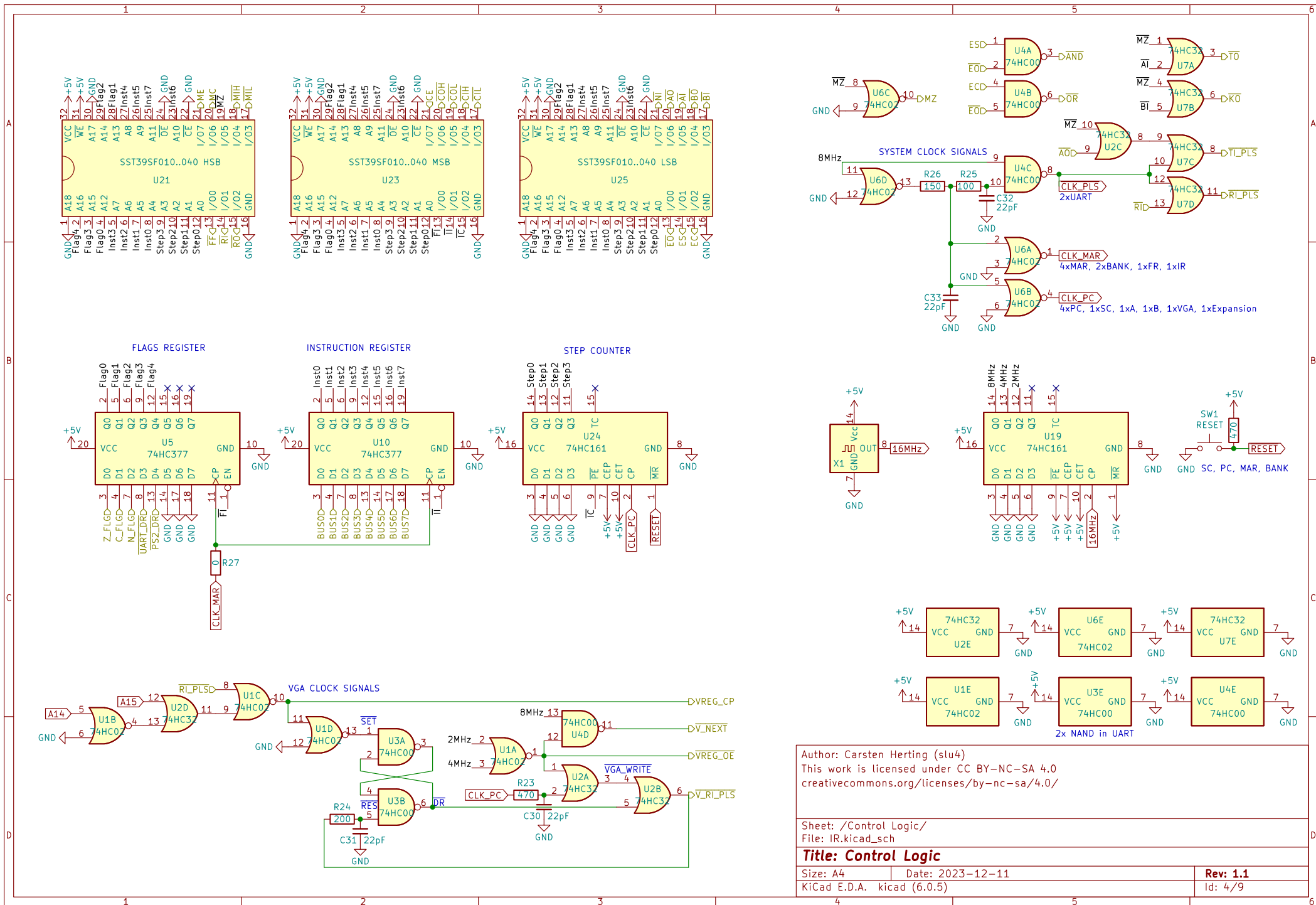
**Title: PS/2 Receiver**

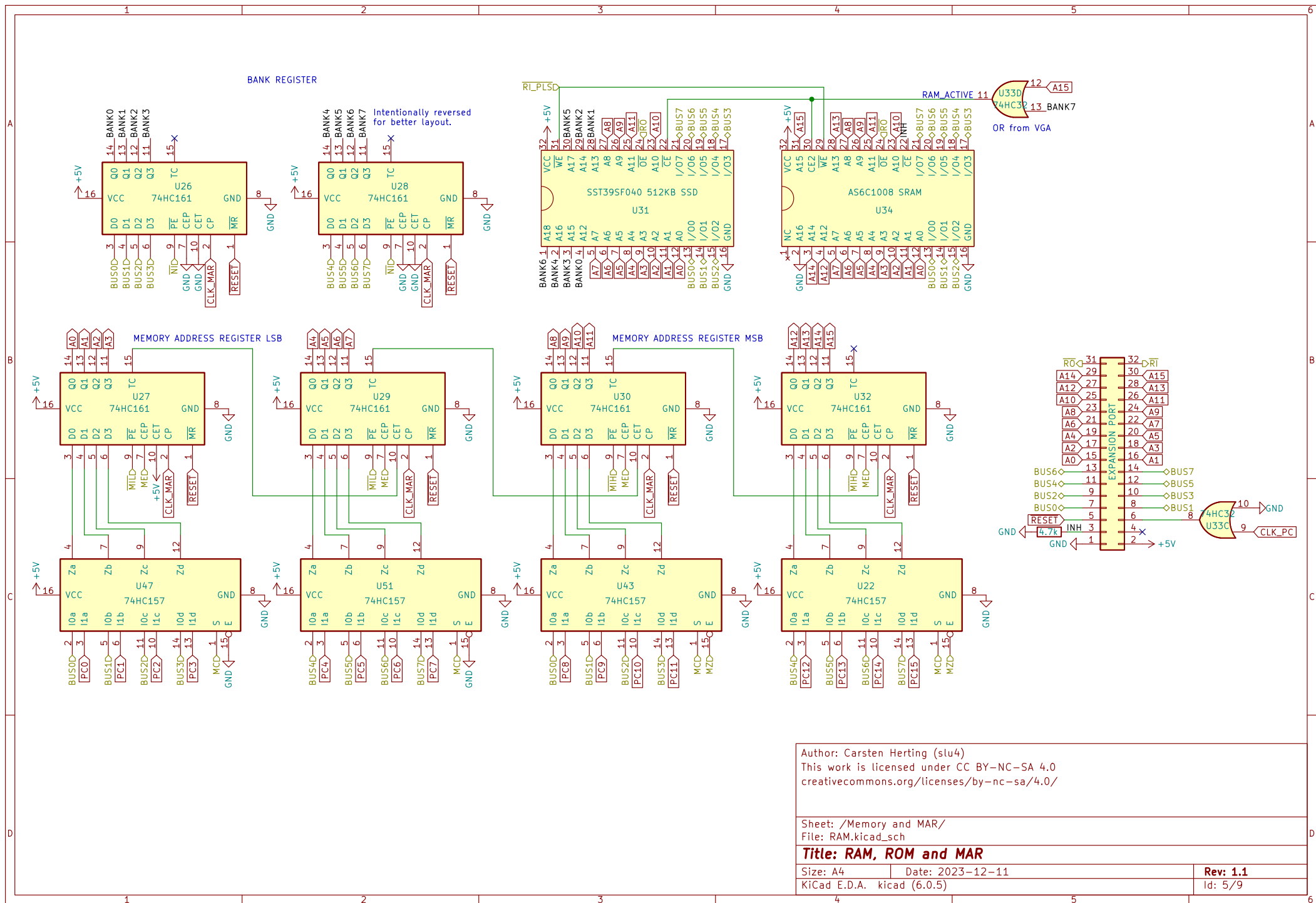
Size: A4 Date: 2023-12-11

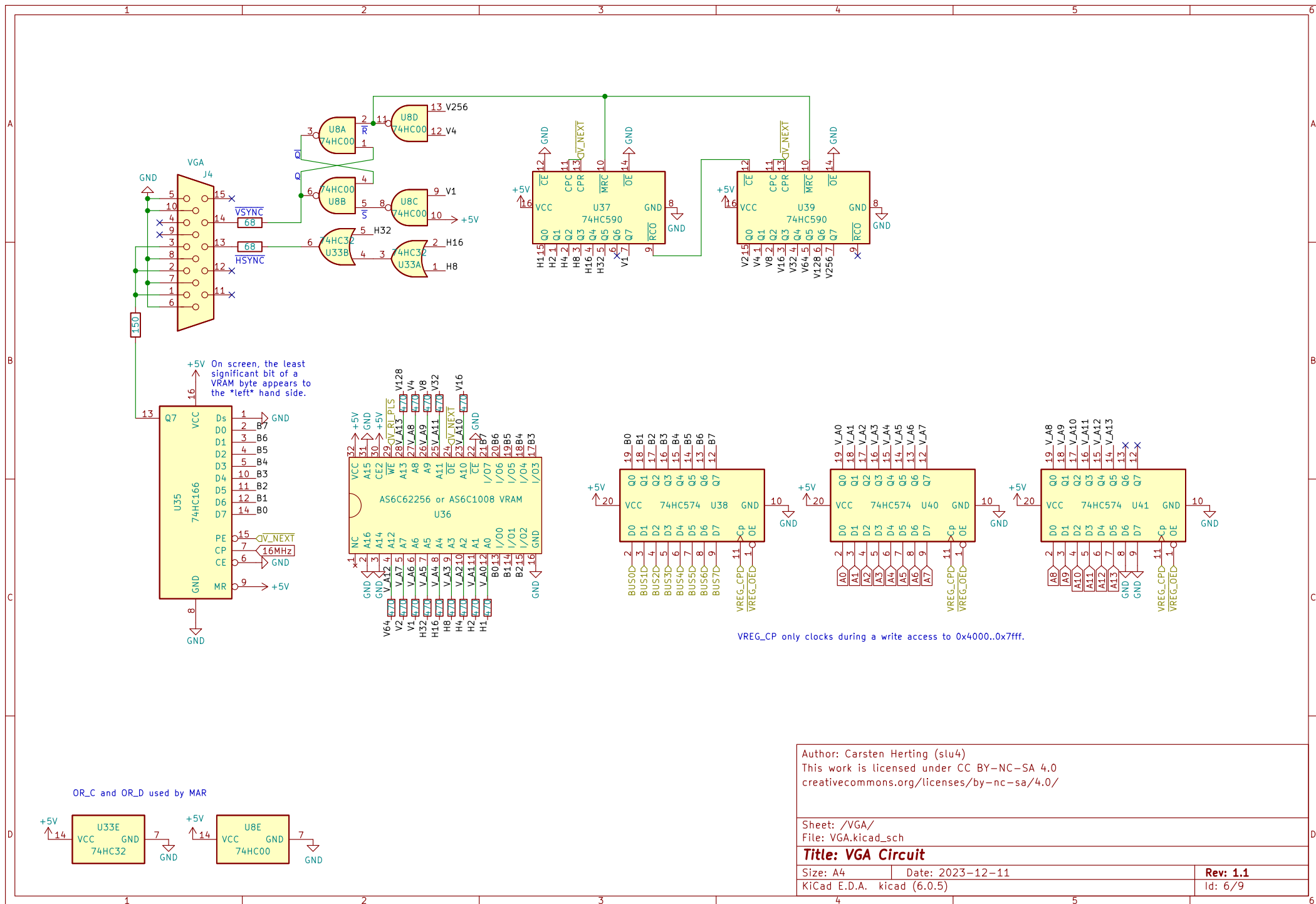
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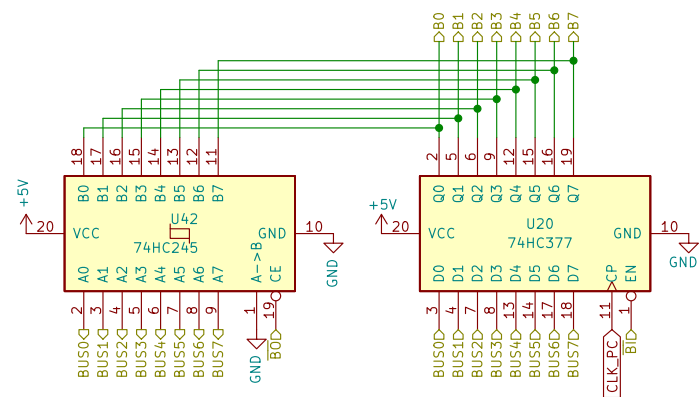
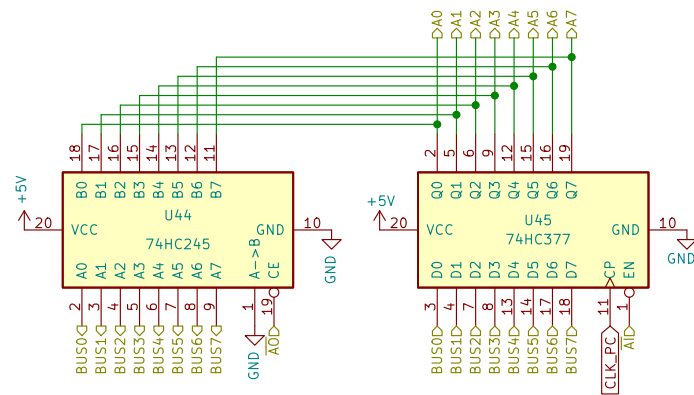
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Sheet: /VGA/  
 File: VGA.kicad\_sch

### Title: VGA Circuit

Size: A4 Date: 2023-12-11  
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Sheet: /Registers/  
File: RegB.kicad\_sch

**Title: B Register**

Size: A4	Date: 2023-12-11
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Size: A4	Date: 20
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