

Chisel and IC Projects Structuring

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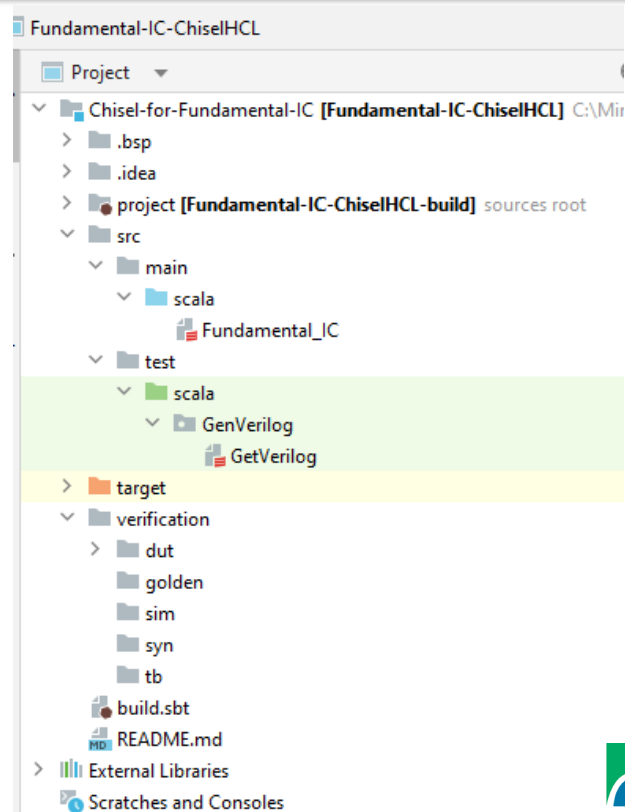
1. Project directory

1.1 Chisel related

src-main: all the Chisel designs are located in main-scala

src-test: the Chisel generation is located in test-scala-GenVerilog

verification-dut: all the generated Verilog is located in verification-dut



1. Project directory

1.2. Verilog design and simulation

In verification folder, it shows the design and verification env

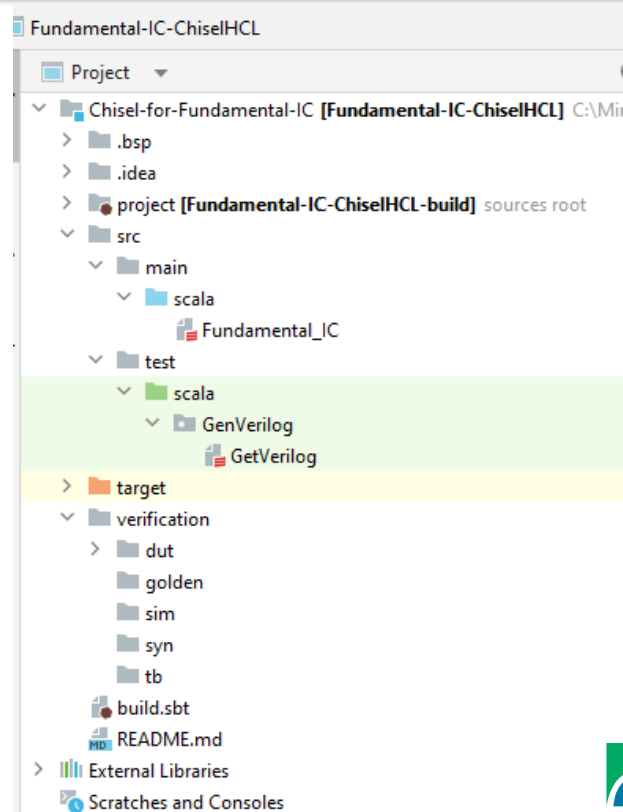
dut: design-under-test (Verilog/SystemVerilog designs)

golden: randomized input and golden output files

sim: run script for ModelSim simulator

syn: synthesis & implementation results for Vivado

tb: testbench



2. Project organization

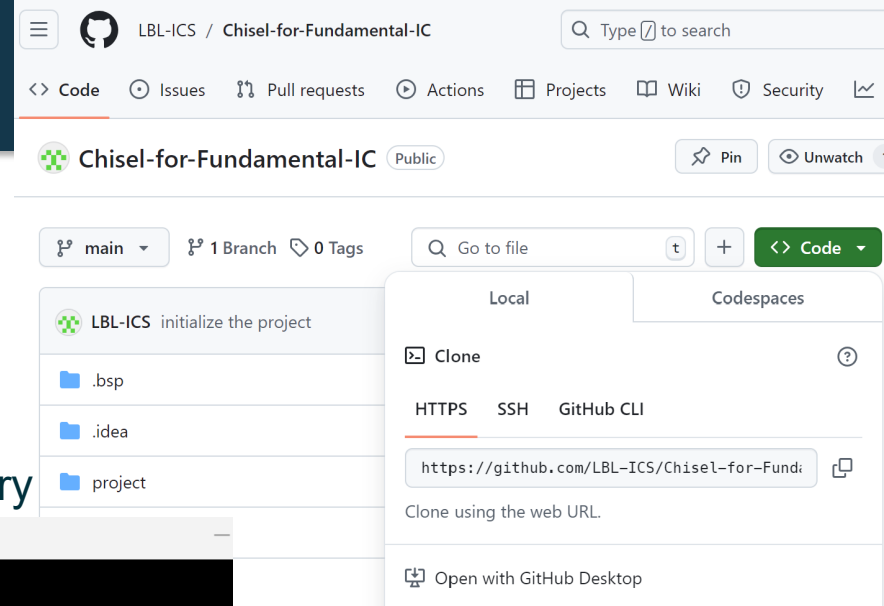
Git repository for project

- Create a git repository
- Locate to your local directory and open Gitbash

Clone the git repository to your local project directory

```
MINGW64:/c/Mirror/GitProject
-Environment/
DFT-Design-Verification-with-Verilog-HDL/
DFT-Design-with-Chisel-HCL/
FP-Modules-ChiselHCL-VerilogHDL/
Fundamental-IC-in-Chisel/
IC-Design/
IC-Design-Instructor/
TSQR-Factorization-Design-with-Chisel-HCL/
Trig-Design-with-Chisel-HCL/
chisel-book/
chisel-template/
chisel-tutorial/
fftdesigns_chiselgenerators/
test/

bobbi@Thinkpad-X1-NN MINGW64 /c/Mirror/GitProject
$ git clone https://github.com/LBL-ICS/Chisel-for-Fundamental-IC.git
Cloning into 'Chisel-for-Fundamental-IC'...
remote: Enumerating objects: 3, done.
remote: Counting objects: 100% (3/3), done.
remote: Compressing objects: 100% (2/2), done.
remote: Total 3 (delta 0), reused 0 (delta 0), pack-reused 0 (from 0)
Receiving objects: 100% (3/3), done.
```



2. Project organization

c. Update your project

Locate to the terminal in IntelliJ, then

- `git add .`
- `git commit -m "your commit"`
- `git push -u origin main`

Note: we use Git repository as the version control tool to maintain and organize projects. whenever you want to release your project, update to Git!

```
Terminal: C:\WINDOW...rshell.exe x + v
Windows PowerShell
Copyright (C) Microsoft Corporation. All rights reserved.

Install the latest PowerShell for new features and improvements! https://aka.ms/PSWindows

PS C:\Mirror\GitProject\Chisel-for-Fundamental-IC> git add .
Enumerating objects: 62, done.
Counting objects: 100% (62/62), done.
Delta compression using up to 20 threads
Compressing objects: 100% (29/29), done.
Writing objects: 100% (37/37), 10.91 KiB | 2.18 MiB/s, done.
Total 37 (delta 10), reused 0 (delta 0), pack-reused 0
remote: Resolving deltas: 100% (10/10), completed with 7 local objects.
To https://github.com/LBL-ICS/Chisel-for-Fundamental-IC.git
 e0608dc..ccb9ee4  main -> main

Git  TODO  Problems  Terminal  Services  Build  sbt shell  Dependencies
```

```
Terminal: C:\WINDOW...rshell.exe x + v
PS C:\Mirror\GitProject\Chisel-for-Fundamental-IC> git commit -m "add some chisel designs"
[main 483b011] add some chisel designs
4 files changed, 81 insertions(+), 1 deletion(-)
create mode 100644 verification/dut/parallel_adder.sv
PS C:\Mirror\GitProject\Chisel-for-Fundamental-IC> git push origin main
Enumerating objects: 32, done.
Counting objects: 100% (32/32), done.
Delta compression using up to 20 threads
Compressing objects: 100% (13/13), done.
Writing objects: 100% (17/17), 2.30 KiB | 2.30 MiB/s, done.
Total 17 (delta 4), reused 0 (delta 0), pack-reused 0
remote: Resolving deltas: 100% (4/4), completed with 4 local objects.
To https://github.com/LBL-ICS/Chisel-for-Fundamental-IC.git
 ccb9ee4..483b011  main -> main
PS C:\Mirror\GitProject\Chisel-for-Fundamental-IC>
```

References

1. Chisel Design – XY. Pdf
2. Chisel Env Setup – XY. pdf
3. Chisel Designs for Fundamental IC, Git repository: <https://github.com/LBL-ICS/Chisel-for-Fundamental-IC.git>
4. Xiaokun Yang, “Integrated Circuit Design: IC Design Flow and Project-Based Learning”, CRC Press -Taylor & Francis Group, ISBN: 978-1-032-03079-1 (ebook ISBN: 978-1-003-18708-0), First edition
5. Chisel Bootcamp
6. Chisel3 Cheat sheet
7. Chisel textbook, version 5