

IntelliJ IDEA Setup for Chisel

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1. Install IntelliJ

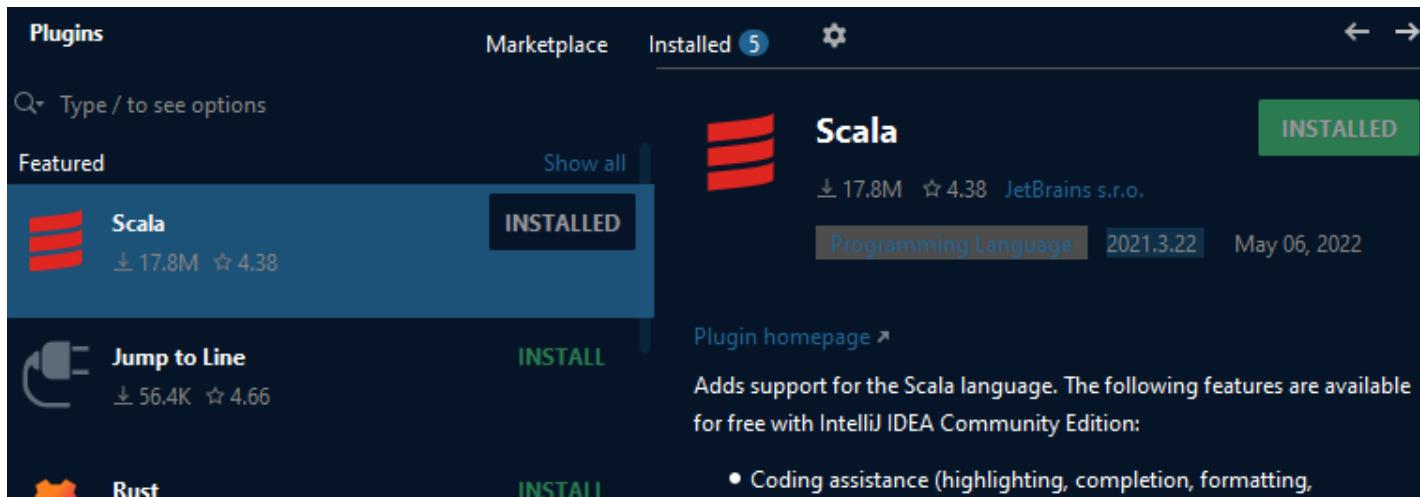
Please download and install IntelliJ
Community edition is free-licensed version
Or apply for student license which is also free



2. Install Scala Plugin

Chisel is based on **Scala**, so you'll need to install the **Scala plugin** in **IntelliJ** to work with Chisel code.

File -> setting -> plugin -> **Marketplace**



3 JDK (Java Development Kit) for SBT (Scala Build Tool)

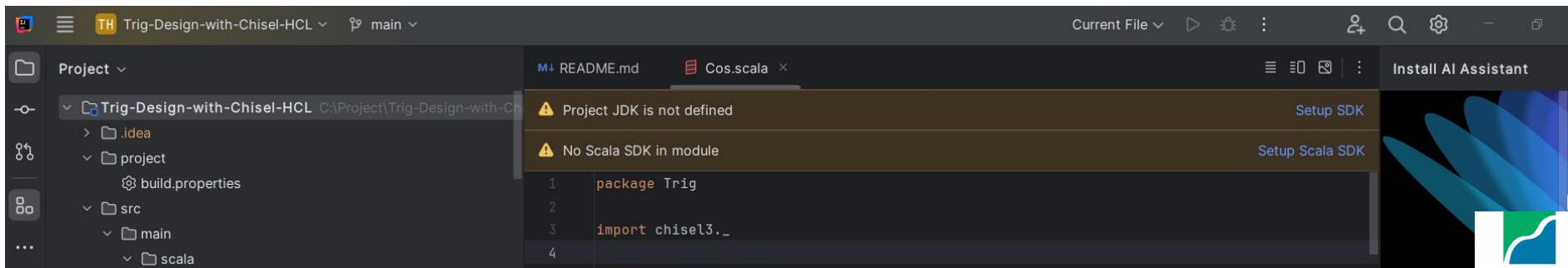
3.1 Install JDK (Java Development Kit)

To set up Chisel in **IntelliJ**, we use **sbt (Scala Build Tool)**, and sbt requires the **JDK** to function correctly. Chisel is based on Scala, and Scala, in turn, runs on the **Java Virtual Machine (JVM)**.

3.2 Configure IntelliJ:

After installing the **JDK**, you'll need to configure it in **IntelliJ** by going to:

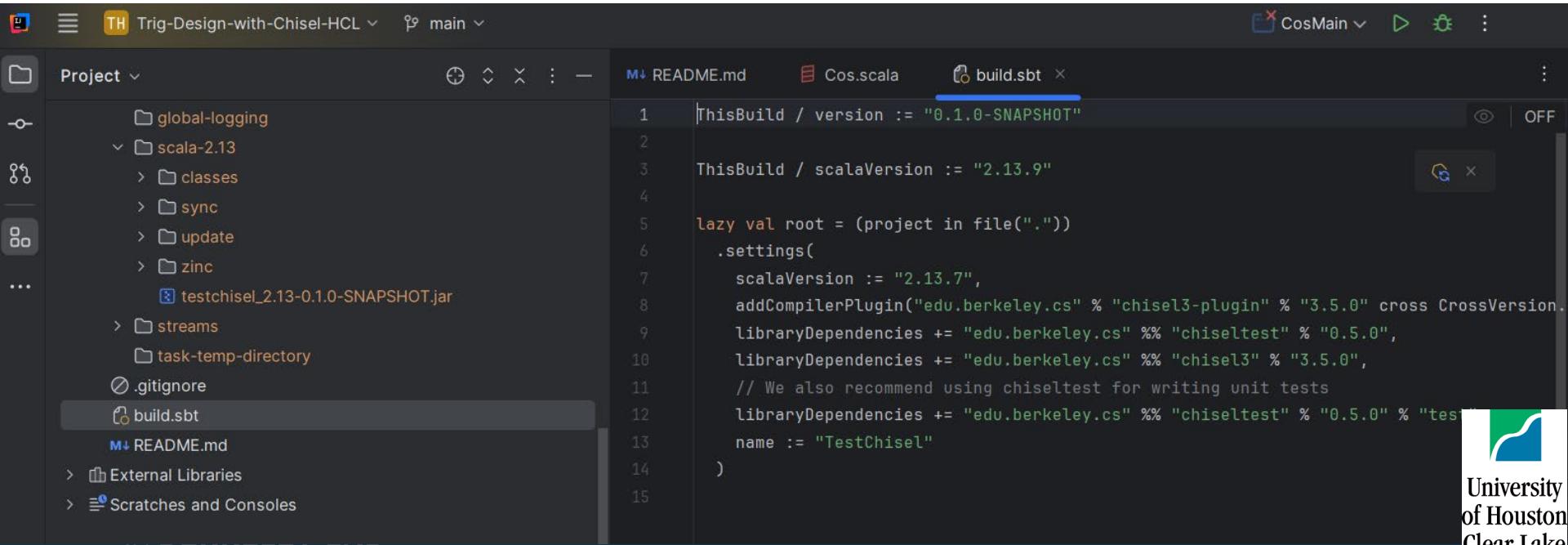
- File -> Project Structure -> Project Settings -> Project -> Select the JDK under "Project SDK."



4. SBT (Scala Build Tool)

Chisel projects are typically managed using **sbt**, which simplifies building Scala (and Chisel) projects.

Before running sbt, please create/check the Chisel dependencies in your **build.sbt** file which is shown in the screenshot. You can skip this step by clone the Git Repository in step 5.



The screenshot shows a code editor interface with a dark theme. On the left is a project navigation sidebar showing files like README.md, build.sbt, and External Libraries. The main area displays the contents of the build.sbt file:

```
1 ThisBuild / version := "0.1.0-SNAPSHOT"
2
3 ThisBuild / scalaVersion := "2.13.9"
4
5 lazy val root = (project in file("."))
6   .settings(
7     scalaVersion := "2.13.7",
8     addCompilerPlugin("edu.berkeley.cs" %% "chisel3-plugin" % "3.5.0" cross CrossVersion.Both),
9     libraryDependencies += "edu.berkeley.cs" %% "chiseltest" % "0.5.0",
10    libraryDependencies += "edu.berkeley.cs" %% "chisel3" % "3.5.0",
11    // We also recommend using chiseltest for writing unit tests
12    libraryDependencies += "edu.berkeley.cs" %% "chiseltest" % "0.5.0" % "test"
13    name := "TestChisel"
14  )
```

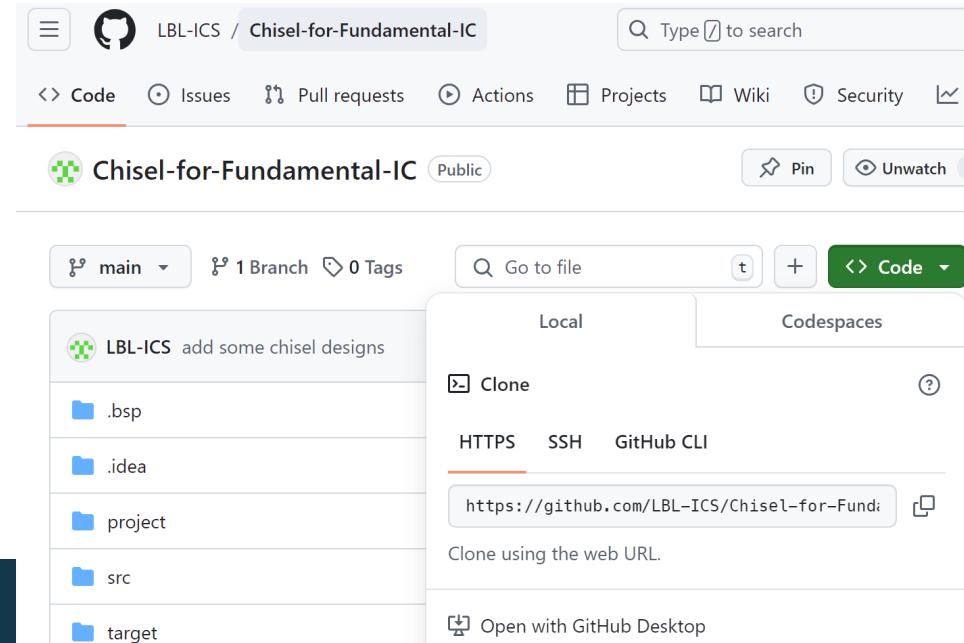
The build.sbt tab is highlighted in blue at the top of the editor. The University of Houston Clear Lake logo is visible in the bottom right corner.

5. Clone Git Repository for Chisel Env and Project

Please clone the Git repository: <https://github.com/LBL-ICS/Chisel-for-Fundamental-IC.git>

- 1) Locate to your local directory and open Gitbash
- 2) Typing: git clone <https://github.com/LBL-ICS/Chisel-for-Fundamental-IC.git>

```
bobbi@Thinkpad-X1-NN MINGW64 /c/Mirror/GitProject
$ git clone https://github.com/LBL-ICS/test.git
Cloning into 'test'...
remote: Enumerating objects: 41, done.
remote: Counting objects: 100% (41/41), done.
remote: Compressing objects: 100% (29/29), done.
remote: Total 41 (delta 4), reused 40 (delta 3), pack-reused 0
Receiving objects: 100% (41/41), 32.89 KiB | 673.00 KiB/s, done.
Resolving deltas: 100% (4/4), done.
```



6. Run Chisel Project

After setting up sbt, you can compile and run your Chisel project by clicking the green triangle!
When successfully run the sbt, you will find the generated Verilog code in verification/dut

The screenshot shows a file explorer on the left and a code editor on the right. The file explorer displays a project structure:

- Chisel-for-Fundamental-IC [Fundamental-IC-ChiselHCL] C:\Mirror\GitProject\Chisel-for-Fundamental-IC
- .bsp
- .idea
- project [Fundamental-IC-ChiselHCL-build] sources root
- src
 - main
 - scala
 - Fundamental_IC
 - test
 - scala
 - GenVerilog
 - GetVerilog
- target
- verification
 - dut
 - golden
 - sim
 - syn
 - tb
- build.sbt
- README.md

The code editor shows a file named `main.scala` with the following content:

```
1 import chisel3._  
2 import chiseltest._  
3 import org.scalatest.flatspec.AnyFlatSpec  
4 import chiseltest.VerilatorBackendAnnotation  
5 import chisel3.stage.ChiselGeneratorAnnotation  
6 import circt.stage.{ChiselStage, FirtoolOption}  
7  
8 import Fundamental_IC._  
9  
10 object main extends App {  
11     (new ChiselStage).execute(  
12         Array("--target", "systemverilog", "--target-dir", "verification/dut"),  
13         Seq(ChiselGeneratorAnnotation(() => new parallel_adder(4, bw = 32)),  
14             FirtoolOption("--disable-all-randomization"),  
15             FirtoolOption("-strip-debug-info")  
16     )  
17 }  
18 }
```

A red circle highlights the green play button icon at the start of the `main` object definition in line 10.



References

1. Chisel Design – XY. Pdf
2. Chisel and IC Projects Structuring – XY. pdf
3. Chisel Bootcamp
4. Chisel3 Cheat sheet
5. Chisel textbook, version 5
6. Chisel Designs for Fundamental IC, Git repository: <https://github.com/LBL-ICS/Chisel-for-Fundamental-IC.git>
7. Xiaokun Yang, “Integrated Circuit Design: IC Design Flow and Project-Based Learning”, CRC Press -Taylor & Francis Group, ISBN: 978-1-032-03079-1 (ebook ISBN: 978-1-003-18708-0), First edition
8. Project Structuring for IC Design and Simulation, Git repository: <https://github.com/LBL-ICS/IC-Design.git>

