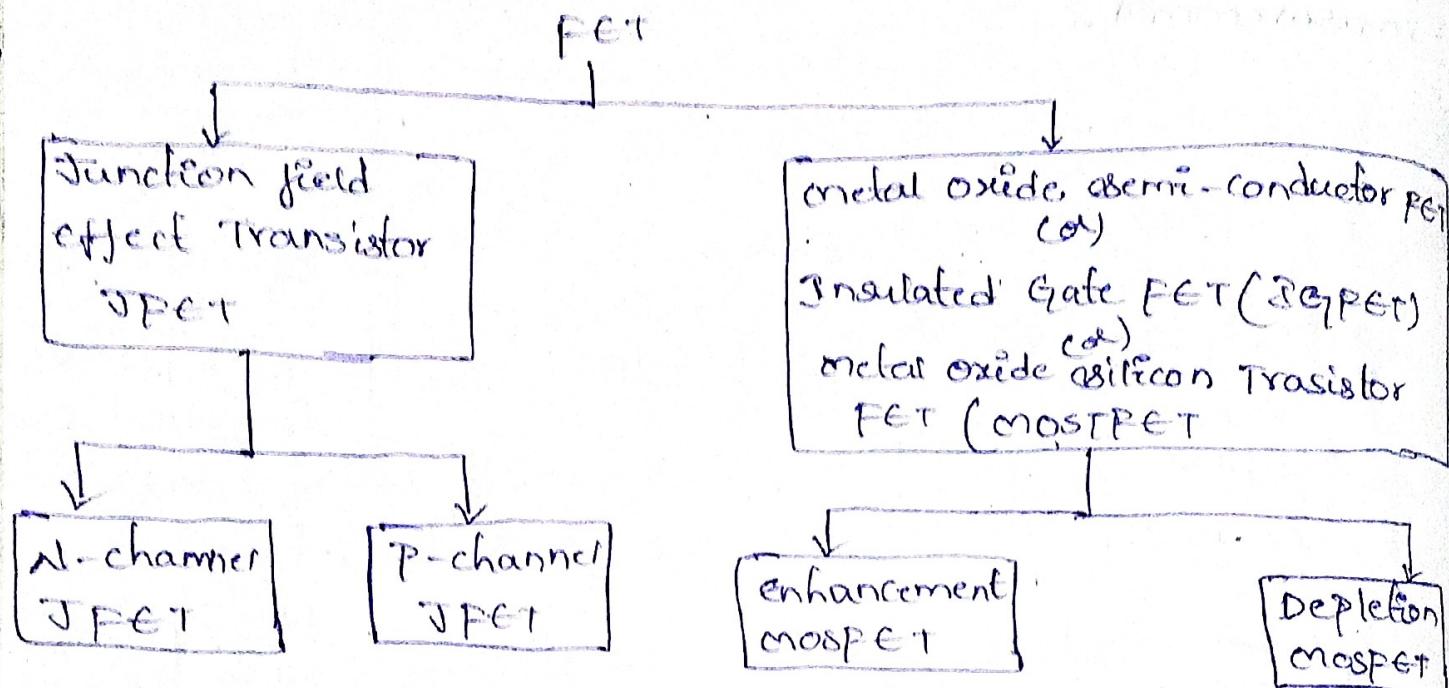


UNIT IV

Field Effect Transistor (FET)

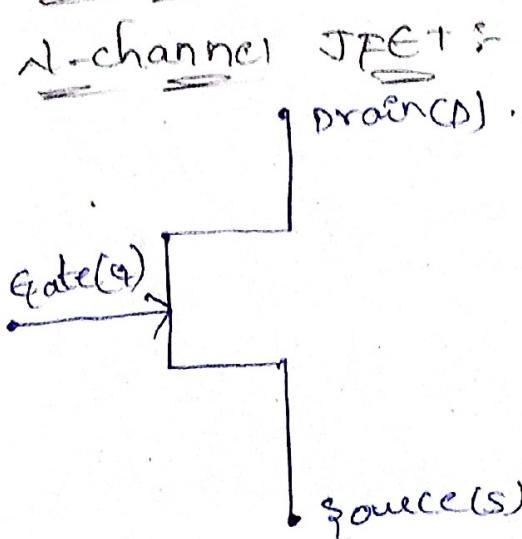
- * FET is also called as Unipolar Junction Transistor.
- * FET has only majority carriers.
- * FET is divided into two types.



* The FET contains 3 terminals

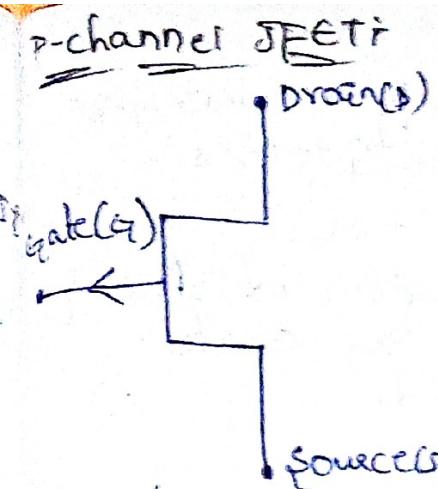
- 1) Gate
- 2) Source
- 3) Drain.

Circuit symbol of JFET



* The direction of the current is Ensdic.

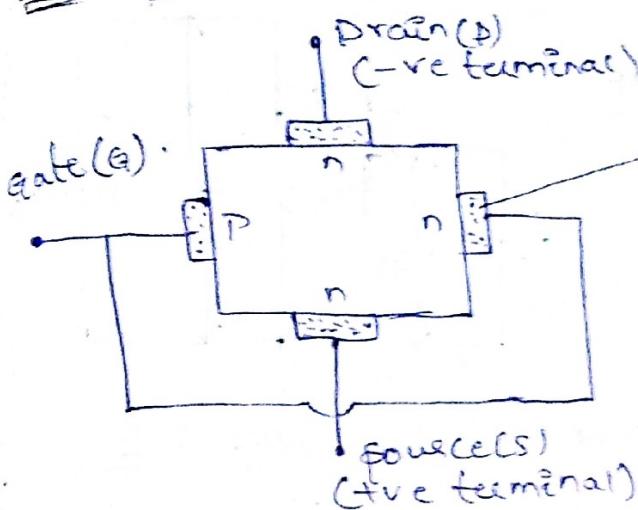
- * Electrons are the majority carriers.
- * Electrons enter through source and leave out from the drain.
- * We are using the reverse bias of p-n junction diode to N-channel.



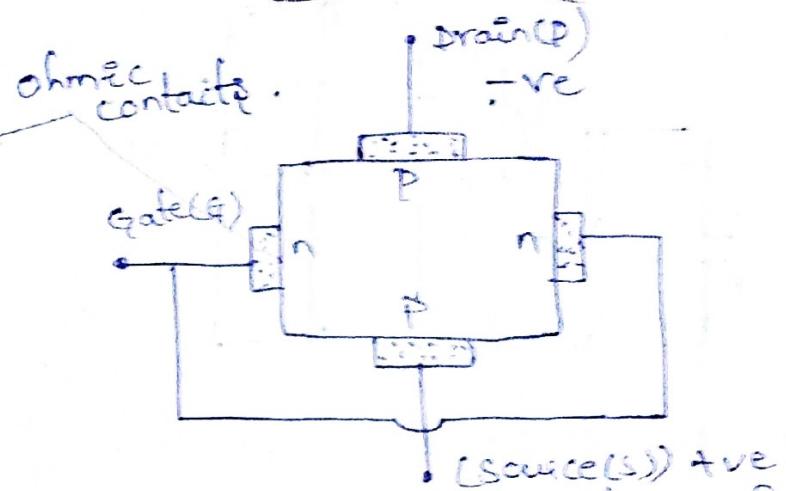
- * The current direction is produced at outside.
- * Holes are the majority carriers.
- * Holes enter through the source and leave out from the drain.
- * We are using the forward bias of P-N junction diode to p-channel.

structure of JFET

n-channel JFET



p-channel JFET



* flow of charge that is current is produced through electro static field. Hence, the name FET.

* FET is mainly divided into two types

1) JFET

2) mosFET:

* JFET is divided into two types

1) n-channel JFET

2) p-channel JFET.

* Here the source, gate, drain etc.

source:

* Source is the terminal in which only majority carriers from n-type to p-type is entered into the process.

Drain

* Drain is a terminal in which only majority carriers from both n-type and p-type leave from the process.

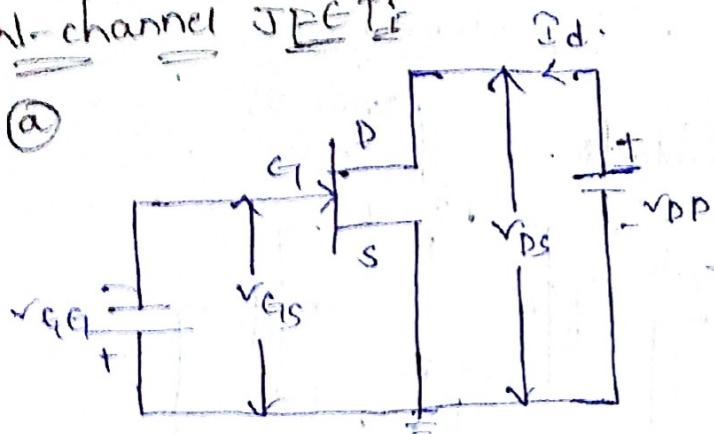
Gate

on both sides of n-type and p-type a region which is produced in the middle portion is called as gate.

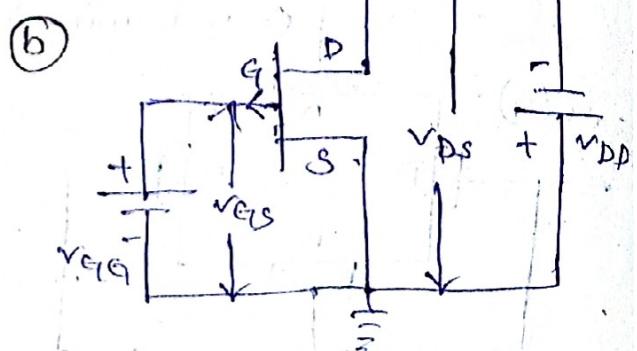
* In the gate terminal channel is produced.

Working of JFET

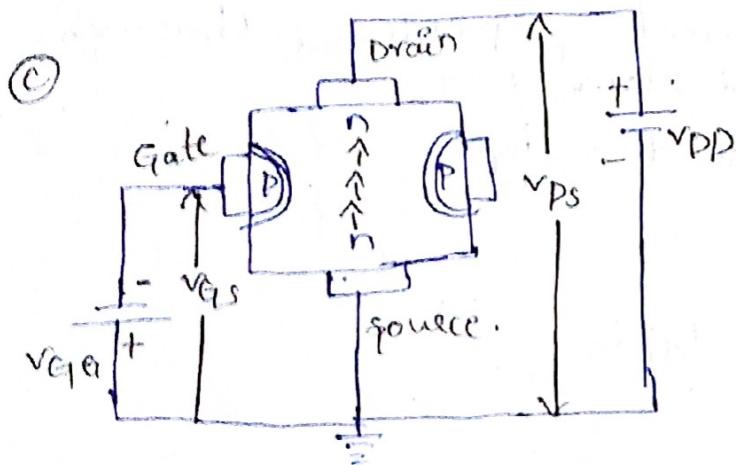
n-channel JFET



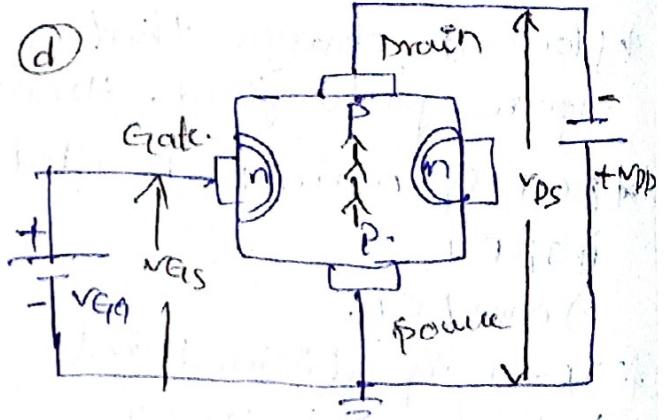
p-channel JFET



Biasing of n-channel JFET



Biasing of p-channel JFET



- * As shown in fig 'a' in current direction towards gate is produced inside the process.
- * Here, input is taken as gate which is called as gate voltage (V_{GA}) and o/p is taken as drain voltage (V_{DD}).
- * The current which is produced at the output is called as Drain current (I_D).

- * As shown in the figure the input voltage gate V_g produced is negative by connecting p-n junction diode under reverse bias conditions.
- * At the output drain voltage V_d is considered as $+V_c$ in which ammeter is connected from $+V_c$ to $+V_c$.
- * At the input gate to source voltage (V_{GS}) is produced and at the output drain to source voltage (V_{DS}) is produced.
- * Similarly with respect to p-channel J-FET the polarities for both V_g & O/P gets reversed.
- * As shown in fig 'b' the current direction towards gate is produced outside the process.
- * Here the input is taken as gate voltage (V_{GG}) & O/P is taken as drain voltage (V_{DD})
- * The current which is produced at the O/P is called as drain current (I_D)
- * As shown in the fig the input voltage gate is produced as $+V_c$ by connecting p-n junction Diode under forward bias conditions.
- * At the output drain voltage V_d is considered as $-V_c$ in which ammeter is connected from $+V_c$ to $-V_c$.
- * As shown in fig ② & ④ three types of conditions are formed-
 - 1) when both $V_{GS} = 0V$ and $V_{DS} = 0V$
under this condition on when no voltage is applied both regions are produced in a constant and linear manner.
 - 2) when $V_{DS} = 0V$ and V_{GS} is increased from 0V.
under this condition reverse bias voltage increases the thickness of depletion region also increases

under this condition

$$I = \frac{V}{R} \quad [\because \text{General formula of current}]$$

$R = \frac{\rho L}{A}$ ρ = Resistivity of the channel

L = length of the channel

A = area cross section of the channel.

$$\text{Drain current, } I_D = \frac{V_{DS}}{R}$$

$$I_D = \frac{V_{DS} A}{\rho L}$$

- 3) When $V_{GS} = 0V$ & V_{GS} is increased from 0V
* under this condition when V_{DS} is increased for both
n-channel JFET and p-channel JFET, a double layer
is formed which produces in wedge shape.

fig @ & fig @

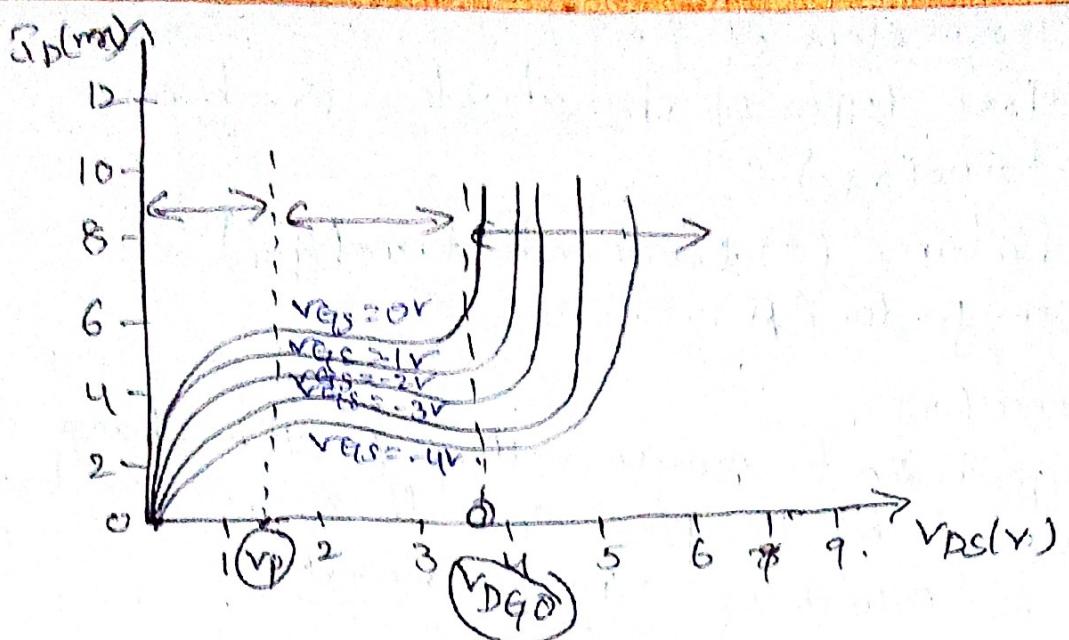
- * In the fig c & d
* In n-channel JFET a double layer is formed
which produces in wedge shape.
* In p-channel JFET a double layer is formed
which produces in wedge shape.
* In p-channel JFET a double layer is formed
which produces in wedge shape [when we apply the more bias to both
wedge shape when we apply the more bias to both
p-type and n-type then it produces two layers]

* Brasing means furtherly increasing.

Drain characteristics of P-JFET

- * As show in the fig drain characteristics is produced
by taking gate to source voltage (V_{GS}) is at
constant and there by varying both Drain Current
(I_D) and drain to source voltage (V_{DS})

- * If we increase the V_{GS} values it shows the -ve values



* Here there are three types of regions

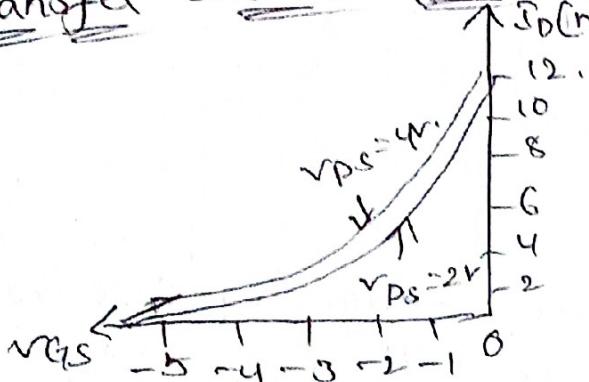
1) Ohmic Region:

* When $V_{DS} \geq 0$ or $V_{DS} = V_p$ [Pinch off voltage] then region formed is called as "Ohmic Region"

2) Pinch off Region:

* Under this region when V_{GS} produces both +ve & -ve voltages for constant & linear values, the region formed is called as Pinch off region.

Transfer characteristics of FET:



* As shown in the fig transfer characteristics produced by keeping drain to source voltage (V_{DS}) constant and thereby varying both drain current (I_D) and gate to source voltage (V_{GS})

* The transfer characteristics are produced under reverse bias condition with gate to source voltage as -ve value

Characteristic Parameters of FET

* It contains three types of characteristics such as

- 1) Drain resistance (r_d)
- 2) Mutual conductance (μ) transconductance (g_m)
- 3) Amplification factor (μ)

1) Drain resistance (r_d):

* change in o/p drain to source voltage to the change in o/p drain current by keeping Gate to source voltage at constant is called as "Drain Resistance"

$$\therefore r_d = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} \text{ constant}$$

units of r_d is ohm's (Ω)

2) Transconductance (g_m):

* change in o/p drain current to the change in input (i_p) by keeping drain to source voltage (V_{DS}) by keeping drain to source voltage (V_{DS}) at constant is called as "Transconductance" (g_m).

$$\therefore g_m = \frac{\Delta V_{GS}}{\Delta V_{ID}}, V_{DS} \text{ constant}$$

* units of g_m is (A) mho's.

3) Amplification factor (μ):

* change in o/p drain to source voltage (V_{DS}) to the change in i/p Gate to source voltage (V_{GS}) by keeping drain current constant is called as "Amplification factor"

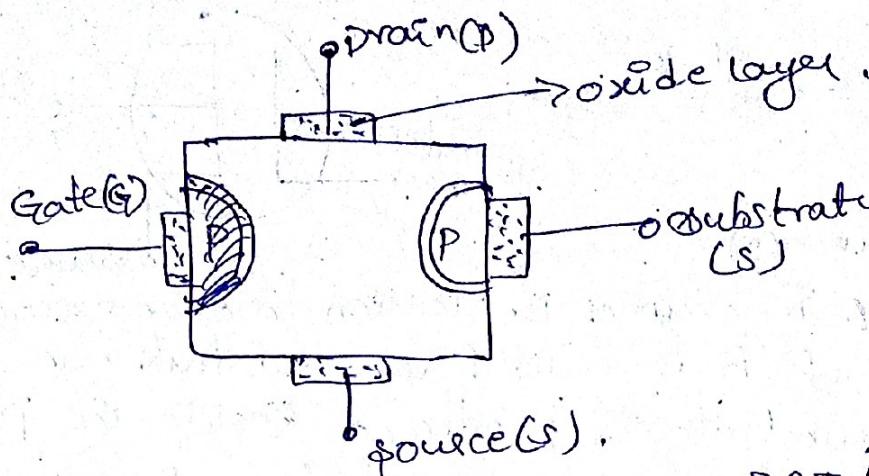
$$\therefore \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}, I_D \text{ constant}$$

* units \Rightarrow there is no units for amplification factor.

2) MOSFET:

* MOSFET [metal oxide semi-conductor field effect transistor]

Fig. 1 Construction diagram of mosfet

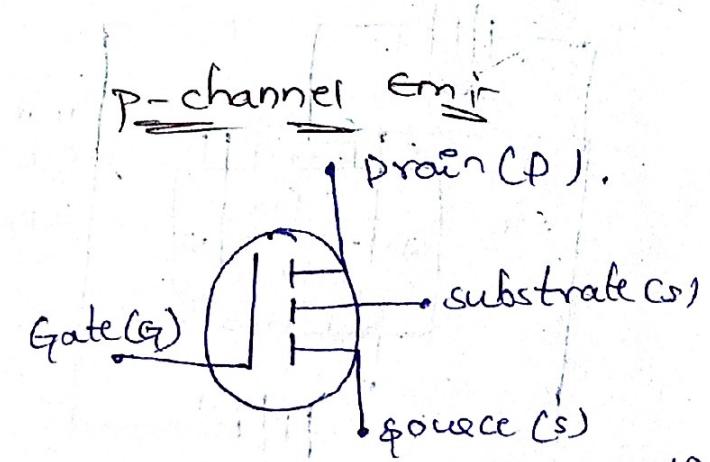
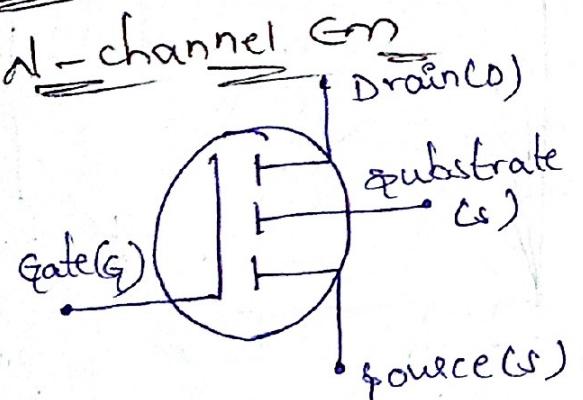


* This is also called as special mosfet / dual node mosfet.

* The mosfet is divided into two types:

- 1) enhancement mosfet
- 2) depletion mosfet.

enhancement mosfet:

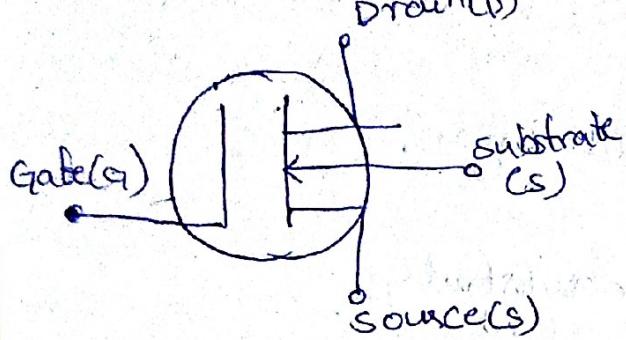


* In N-channel and P-channel enhancement mosfet another terminal is produced which is called as substrate. In N-channel E-mosfet substrate is produced inside the process whereas in P-channel E-mosfet substrate is produced outside the process.

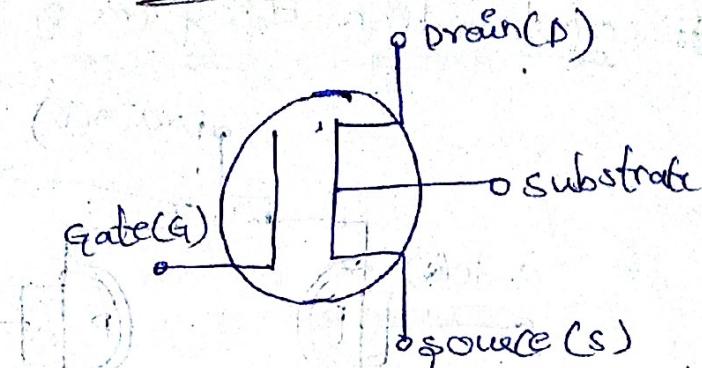
* In N-channel E-mosfet and P-channel E-mosfet source drain & substrate all are separated with each other.

2) Depletion mosFET

N-channel DMos



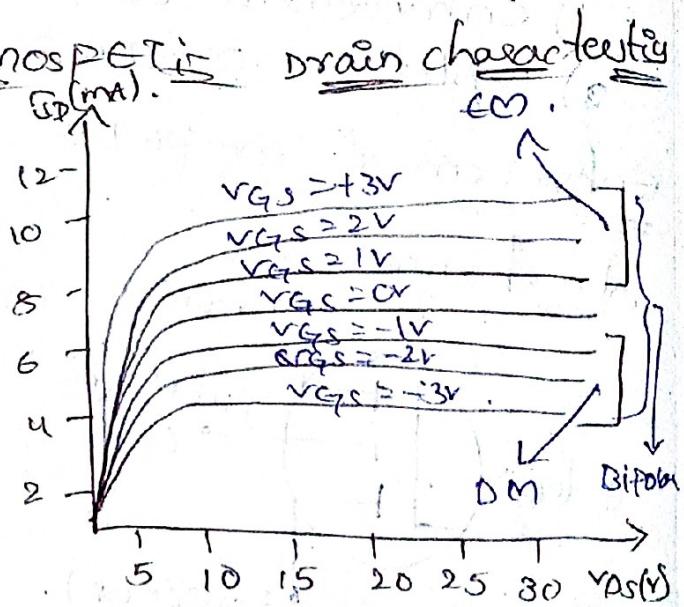
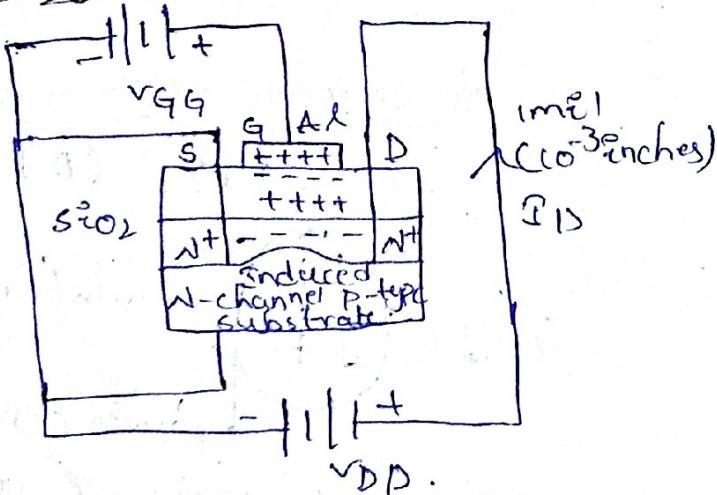
P-channel DMos



* In N-channel & P-channel Depletion mosFET another terminal is produced which is called as substrate. In N-channel DMosFET substrate is produced inside the process where P-channel DMosFET substrate is produced outside of the process.

* In N-channel DMosFET and P-channel DMosFET source, drain and substrate all are combined with each other.

Working of enhancement mosFET is drain characteristic



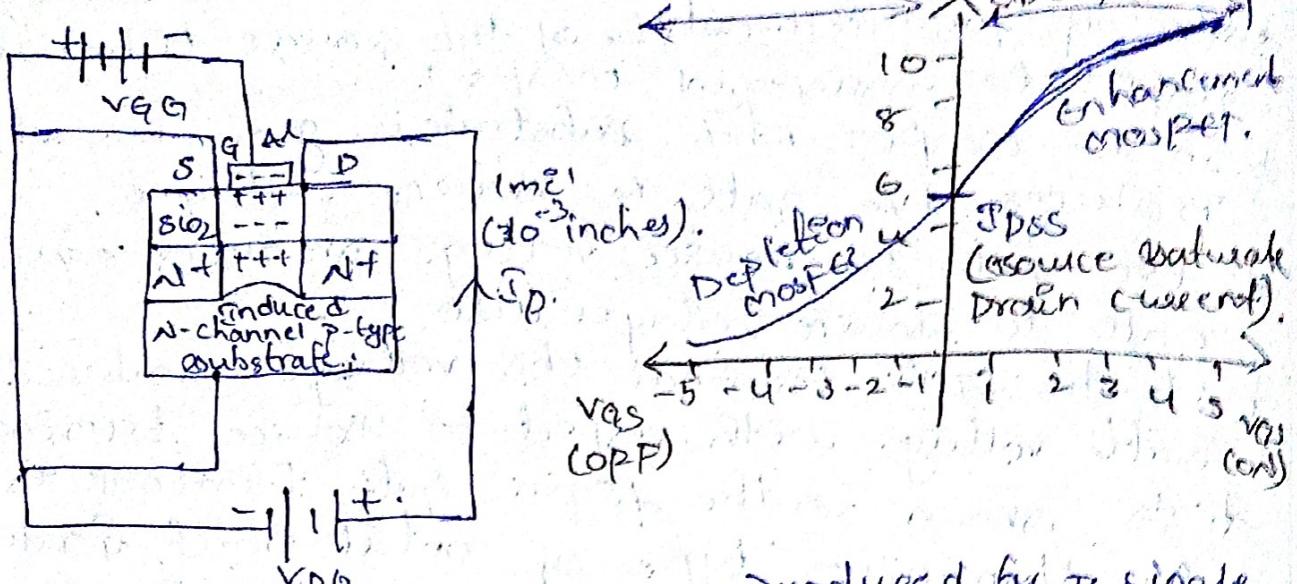
* Two heavily doped N+ regions are produced by a single lightly doped p-type silicon material, which is called as gate (G).

* One N+ terminal is called as source(S) and other N+ terminal is called as drain(D).

* Both source and drain(D) terminals are separated by one mil (10^{-3} inches).

- * As a result of the source terminal an insulating layer which is formed is called as SiO_2 (Silicon Oxide)
- * SiO_2 is produced outside of the source terminal with respect to enhancement mosFET.
- * In E-mosFET when substrate is grounded with produces +ve gate to source voltage.
- * +ve gate to source voltage produces equally -ve gate to source voltages also.
- * At the gate terminal the voltage produced is +ve gate voltage with respect to source terminal.
- * At the figure gate terminal is produced by Aluminium type of metal which induces inversion layer in the form of negative to positive.
- * In the E-mosFET drain characteristics are produced by keeping gate to source voltage constant and there by varying drain current (i_{D}) and V_{DS} .
- * +ve gate to source voltage is produced by E-mosFET and -ve gate to source voltage is produced by D-mosFET.
- * As a result both mosFETs are produced by a single mosFET in which bipolar signals are produced.
- * When bipolar signals are produced, it is also called as "Dual mode mosFET".
- * Drain voltage does not gets effected if gate is produced in either +ve or -ve voltages.

Working of Depletion mosFET & Transfer characteristics



- * Two heavily doped N^+ regions are produced by a single lightly doped p-type silicon material called as Gate(G).
- * One N^+ terminal is called as Source(S) and other N^+ terminal is called as Drain(D).
- * Both Source(S) and Drain(D) terminals are separated by one mil (10^{-3} inches).
- * As a result at the source terminal an insulating material called as SiO_2 is formed.
- * As shown in the fig here SiO_2 is produced inside the source terminal.
- * As a result negative gate voltage is supplied in which inversion layer is produced in the form of +ve to -ve.
- * Here, the substrate is connected to supply voltage in which it produces equally +ve and -ve gate to source voltages.
- * In depletion mosFET characteristics are formed by keeping drain current constant & varying both V_{GS} and V_{DS} .

- * when V_{GS} is ON the voltage is produced which is given in the form of C-MOSFET.
- * when V_{GS} is OFF it produces -ve voltage in which D-MOSFET is produced.
- * As a result both bipolar signals are produced, therefore it is also called as ~~D~~ Dual mode mosfet.
- * As shown in the fig both +ve and -ve gate to source voltage are produced at center point called as I_{DSS} (source saturation drain current).
- * Here, also drain voltage is not affected with the help of any -ve & -ve gate to source voltage.

Advantages of FET

- 1) contains high Z/P impedance
- 2) produces thermal stability
- 3) produces offset voltages better than BJT
- 4) used as unipolar device
- 5) only majority carriers are produced.
- 6) current is controlled by electric field.

Disadvantages of FET

- 1) it contains low gain Band width product.

$$B.W = F_H - F_L$$

Relation b/w FET Parameters

$$I_D = f(V_{DS}, V_{GS}) \rightarrow ①$$

I_D is produced by function of V_{DS} & V_{GS} change
so I_D is given by

$$\Delta I_D = \left(\frac{\Delta I_D}{\Delta V_{DS}} \right) V_{GS} \Delta V_{DS} + \left(\frac{\Delta I_D}{\Delta V_{GS}} \right) V_{DS} \Delta V_{GS} \rightarrow ②$$

dividing both sides w.r.t v_{GS} we get

$$\frac{\Delta I_D}{\Delta v_{GS}} = \left(\frac{\Delta I_D}{\Delta v_{DS}} \right)_{v_{GS}} \frac{\Delta v_{DS}}{\Delta v_{GS}} + \left(\frac{\Delta I_D}{\Delta v_{GS}} \right)_{v_{DS}} \frac{\Delta v_{DS}}{\Delta v_{GS}}$$

$$\frac{\Delta I_D}{\Delta v_{GS}} = \left(\frac{\Delta I_D}{\Delta v_{DS}} \right)_{v_{GS}} \frac{\Delta v_{DS}}{\Delta v_{GS}} + \left(\frac{\Delta I_D}{\Delta v_{DS}} \right)_{v_{GS}} v_{DS}.$$

If I_D is constant, then $\frac{\Delta I_D}{\Delta v_{GS}} = 0$.

$$\left(\frac{\Delta I_D}{\Delta v_{DS}} \right)_{v_{GS}} \frac{\Delta v_{DS}}{\Delta v_{GS}} + \left(\frac{\Delta I_D}{\Delta v_{DS}} \right)_{v_{DS}} v_{DS} = 0.$$

$$\left(\frac{\Delta I_D}{\Delta v_{DS}} \right)_{v_{GS}} \left(\frac{\Delta v_{DS}}{\Delta v_{GS}} \right)_{ID} + \left(\frac{\Delta I_D}{\Delta v_{DS}} \right)_{v_{DS}} v_{DS} = 0$$

$$\frac{1}{r_d} (-\mu) + g_m = 0$$

$$\boxed{\mu = r_d g_m}$$