Table (8) illustrates FPGA pin assignment for the FMC_A (J3) connector located at the front panel side:

FMC_A Signal Name	Signal Description	FPGA Pin#
FMC_A_CLK[0]_M2C_N	Mezzanine Card to Carrier Card Clock	G19
FMC_A_CLK[0]_M2C_P	Mezzanine Card to Carrier Card Clock	H19
FMC_A_CLK[1]_M2C_N	Mezzanine Card to Carrier Card Clock	G15
FMC_A_CLK[1]_M2C_P	Mezzanine Card to Carrier Card Clock	G16
FMC_A_DP[0]_C2M_N	Serial I/O: Carrier to Mezzanine	AF5
FMC_A_DP[0]_C2M_P	Serial I/O: Carrier to Mezzanine	AF6
FMC_A_DP[0]_M2C_N	Serial I/O: Mezzanine to Carrier	AF1
FMC_A_DP[0]_M2C_P	Serial I/O: Mezzanine to Carrier	AF2
FMC_A_DP[1]_C2M_N	Serial I/O: Carrier to Mezzanine	AD5
FMC_A_DP[1]_C2M_P	Serial I/O: Carrier to Mezzanine	AD6
FMC_A_DP[1]_M2C_N	Serial I/O: Mezzanine to Carrier	AC3
FMC_A_DP[1]_M2C_P	Serial I/O: Mezzanine to Carrier	AC4
FMC_A_DP[2]_C2M_N	Serial I/O: Carrier to Mezzanine	AE3
FMC_A_DP[2]_C2M_P	Serial I/O: Carrier to Mezzanine	AE4
FMC_A_DP[2]_M2C_N	Serial I/O: Mezzanine to Carrier	AD1
FMC_A_DP[2]_M2C_P	Serial I/O: Mezzanine to Carrier	AD2
FMC_A_DP[3]_C2M_N	Serial I/O: Carrier to Mezzanine	AG7
FMC_A_DP[3]_C2M_P	Serial I/O: Carrier to Mezzanine	AG8
FMC_A_DP[3]_M2C_N	Serial I/O: Mezzanine to Carrier	AG3
FMC_A_DP[3]_M2C_P	Serial I/O: Mezzanine to Carrier	AG4
FMC_A_DP[4]_C2M_N	Serial I/O: Carrier to Mezzanine	AJ7
FMC_A_DP[4]_C2M_P	Serial I/O: Carrier to Mezzanine	AJ8
FMC_A_DP[4]_M2C_N	Serial I/O: Mezzanine to Carrier	AJ3
FMC_A_DP[4]_M2C_P	Serial I/O: Mezzanine to Carrier	AJ4
FMC_A_DP[5]_C2M_N	Serial I/O: Carrier to Mezzanine	AL7
FMC_A_DP[5]_C2M_P	Serial I/O: Carrier to Mezzanine	AL8
FMC_A_DP[5]_M2C_N	Serial I/O: Mezzanine to Carrier	AL3
FMC_A_DP[5]_M2C_P	Serial I/O: Mezzanine to Carrier	AL4
FMC_A_DP[6]_C2M_N	Serial I/O: Carrier to Mezzanine	AK5
FMC_A_DP[6]_C2M_P	Serial I/O: Carrier to Mezzanine	AK6
FMC_A_DP[6]_M2C_N	Serial I/O: Mezzanine to Carrier	AK1
FMC_A_DP[6]_M2C_P	Serial I/O: Mezzanine to Carrier	AK2
FMC_A_DP[7]_C2M_N	Serial I/O: Carrier to Mezzanine	AH5
FMC_A_DP[7]_C2M_P	Serial I/O: Carrier to Mezzanine	AH6
FMC_A_DP[7]_M2C_N	Serial I/O: Mezzanine to Carrier	AH1
FMC_A_DP[7]_M2C_P	Serial I/O: Mezzanine to Carrier	AH2
FMC_A_DP[8]_C2M_N	Serial I/O: Carrier to Mezzanine	AA3
FMC_A_DP[8]_C2M_P	Serial I/O: Carrier to Mezzanine	AA4

FMC_A_DP[8]_M2C_N	Serial I/O: Mezzanine to Carrier	Y1
FMC_A_DP[8]_M2C_P	Serial I/O: Mezzanine to Carrier	Y2
FMC_A_DP[9]_C2M_N	Serial I/O: Carrier to Mezzanine	AB5
FMC_A_DP[9]_C2M_P	Serial I/O: Carrier to Mezzanine	AB6
FMC_A_DP[9]_M2C_N	Serial I/O: Mezzanine to Carrier	AB1
FMC_A_DP[9]_M2C_P	Serial I/O: Mezzanine to Carrier	AB2
FMC_A_GBTCLK[0]_M2C_	Serial I/O Clock: Mezzanine to Carrier	AC7
FMC_A_GBTCLK[0]_M2C_	Serial I/O Clock: Mezzanine to Carrier	AC8
FMC_A_GBTCLK[1]_M2C_	Serial I/O Clock: Mezzanine to Carrier	AA7
FMC_A_GBTCLK[1]_M2C_	Serial I/O Clock: Mezzanine to Carrier	AA8
FMC_A_HA[0]_CC_N	User Defined I/O (clock capable)	K23
FMC_A_HA[0]_CC_P	User Defined I/O (clock capable)	K22
FMC_A_HA[1]_CC_N	User Defined I/O (clock capable)	J24
FMC_A_HA[1]_CC_P	User Defined I/O (clock capable)	J23
FMC_A_HA[2]_N	User Defined I/O	C24
FMC_A_HA[2]_P	User Defined I/O	D24
FMC_A_HA[3]_N	User Defined I/O	F24
FMC_A_HA[3]_P	User Defined I/O	G24
FMC_A_HA[4]_N	User Defined I/O	E22
FMC_A_HA[4]_P	User Defined I/O	E21
FMC_A_HA[5]_N	User Defined I/O	E23
FMC_A_HA[5]_P	User Defined I/O	F23
FMC_A_HA[6]_N	User Defined I/O	J21
FMC_A_HA[6]_P	User Defined I/O	K21
FMC_A_HA[7]_N	User Defined I/O	B22
FMC_A_HA[7]_P	User Defined I/O	C22
FMC_A_HA[8]_N	User Defined I/O	A22
FMC_A_HA[8]_P	User Defined I/O	B21
FMC_A_HA[9]_N	User Defined I/O	A24
FMC_A_HA[9]_P	User Defined I/O	B24
FMC_A_HA[10]_N	User Defined I/O	P20
FMC_A_HA[10]_P	User Defined I/O	R20
FMC_A_HA[11]_N	User Defined I/O	N22
FMC_A_HA[11]_P	User Defined I/O	N21
FMC_A_HA[12]_N	User Defined I/O	L24
FMC_A_HA[12]_P	User Defined I/O	L23
FMC_A_HA[13]_N	User Defined I/O	C21
FMC_A_HA[13]_P	User Defined I/O	D21
FMC_A_HA[14]_N	User Defined I/O	P21
FMC_A_HA[14]_P	User Defined I/O	R21
FMC_A_HA[15]_N	User Defined I/O	M21

FMC_A_HA[15]_P	User Defined I/O	M20
FMC_A_HA[16]_N	User Defined I/O	K20
FMC_A_HA[16]_P	User Defined I/O	L20
FMC_A_HA[17]_CC_N	User Defined I/O (clock capable)	H24
FMC_A_HA[17]_CC_P	User Defined I/O (clock capable)	H23
FMC_A_HA[18]_CC_N	User Defined I/O (clock capable)	H22
FMC_A_HA[18]_CC_P	User Defined I/O (clock capable)	H21
FMC_A_HA[19]_N	User Defined I/O	G22
FMC_A_HA[19]_P	User Defined I/O	G21
FMC_A_HA[20]_N	User Defined I/O	R23
FMC_A_HA[20]_P	User Defined I/O	T23
FMC_A_HA[21]_N	User Defined I/O	C23
FMC_A_HA[21]_P	User Defined I/O	D23
FMC_A_HA[22]_N	User Defined I/O	N23
FMC_A_HA[22]_P	User Defined I/O	P23
FMC_A_HA[23]_N	User Defined I/O	R22
FMC_A_HA[23]_P	User Defined I/O	T22
FMC_A_HB[0]_CC_N	User Defined I/O (clock capable)	AN19
FMC_A_HB[0]_CC_P	User Defined I/O (clock capable)	AM19
FMC_A_HB[1]_N	User Defined I/O	AV17
FMC_A_HB[1]_P	User Defined I/O	AV18
FMC_A_HB[2]_N	User Defined I/O	AW18
FMC_A_HB[2]_P	User Defined I/O	AV19
FMC_A_HB[3]_N	User Defined I/O	AT20
FMC_A_HB[3]_P	User Defined I/O	AR20
FMC_A_HB[4]_N	User Defined I/O	AL18
FMC_A_HB[4]_P	User Defined I/O	AL19
FMC_A_HB[5]_N	User Defined I/O	AU19
FMC_A_HB[5]_P	User Defined I/O	AT19
FMC_A_HB[6]_CC_N	User Defined I/O (clock capable)	AM17
FMC_A_HB[6]_CC_P	User Defined I/O (clock capable)	AL17
FMC_A_HB[7]_N	User Defined I/O	AT17
FMC_A_HB[7]_P	User Defined I/O	AT18
FMC_A_HB[8]_N	User Defined I/O	AH18
FMC_A_HB[8]_P	User Defined I/O	AH19
FMC_A_HB[9]_N	User Defined I/O	AP18
FMC_A_HB[9]_P	User Defined I/O	AP19
FMC_A_HB[10]_N	User Defined I/O	AR17
FMC_A_HB[10]_P	User Defined I/O	AR18
FMC_A_HB[11]_N	User Defined I/O	AR16
FMC_A_HB[11]_P	User Defined I/O	AP16

FMC_A_HB[12]_N	User Defined I/O	AG19
FMC_A_HB[12]_P	User Defined I/O	AF19
FMC_A_HB[13]_N	User Defined I/O	AJ18
FMC_A_HB[13]_P	User Defined I/O	AJ19
FMC_A_HB[14]_N	User Defined I/O	AH16
FMC_A_HB[14]_P	User Defined I/O	AH17
FMC_A_HB[15]_N	User Defined I/O	AK16
FMC_A_HB[15]_P	User Defined I/O	AJ16
FMC_A_HB[16]_N	User Defined I/O	AK17
FMC_A_HB[16]_P	User Defined I/O	AK18
FMC_A_HB[17]_CC_N	User Defined I/O (clock capable)	AN17
FMC_A_HB[17]_CC_P	User Defined I/O (clock capable)	AN18
FMC_A_HB[18]_N	User Defined I/O	AE16
FMC_A_HB[18]_P	User Defined I/O	AD16
FMC_A_HB[19]_N	User Defined I/O	AF18
FMC_A_HB[19]_P	User Defined I/O	AE18
FMC_A_HB[20]_N	User Defined I/O	AG16
FMC_A_HB[20]_P	User Defined I/O	AG17
FMC_A_HB[21]_N	User Defined I/O	AF17
FMC_A_HB[21]_P	User Defined I/O	AE17
FMC_A_LA[0]_CC_N	User Defined I/O (clock capable)	J19
FMC_A_LA[0]_CC_P	User Defined I/O (clock capable)	J20
FMC_A_LA[1]_CC_N	User Defined I/O (clock capable)	J18
FMC_A_LA[1]_CC_P	User Defined I/O (clock capable)	K18
FMC_A_LA[2]_N	User Defined I/O	E20
FMC_A_LA[2]_P	User Defined I/O	F20
FMC_A_LA[3]_N	User Defined I/O	A20
FMC_A_LA[3]_P	User Defined I/O	B20
FMC_A_LA[4]_N	User Defined I/O	C19
FMC_A_LA[4]_P	User Defined I/O	D19
FMC_A_LA[5]_N	User Defined I/O	A17
FMC_A_LA[5]_P	User Defined I/O	A18
FMC_A_LA[6]_N	User Defined I/O	A19
FMC_A_LA[6]_P	User Defined I/O	B19
FMC_A_LA[7]_N	User Defined I/O	C18
FMC_A_LA[7]_P	User Defined I/O	D18
FMC_A_LA[8]_N	User Defined I/O	B17
FMC_A_LA[8]_P	User Defined I/O	C17
FMC_A_LA[9]_N	User Defined I/O	E17
FMC_A_LA[9]_P	User Defined I/O	F17
FMC_A_LA[10]_N	User Defined I/O	E18

FMC_A_LA[11]_P User Defined I/O P19 FMC_A_LA[12]_N User Defined I/O N18 FMC_A_LA[12]_P User Defined I/O N19 FMC_A_LA[13]_N User Defined I/O J16 FMC_A_LA[13]_P User Defined I/O K16 FMC_A_LA[14]_N User Defined I/O K17 FMC_A_LA[14]_P User Defined I/O N16 FMC_A_LA[15]_N User Defined I/O N16 FMC_A_LA[15]_P User Defined I/O M17 FMC_A_LA[16]_N User Defined I/O M17 FMC_A_LA[16]_P User Defined I/O M17 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[19]_N User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[20]_N User Defined I/O D13 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[10]_P	User Defined I/O	F18
FMC_A_LA[12]_N User Defined I/O N18 FMC_A_LA[12]_P User Defined I/O N19 FMC_A_LA[13]_N User Defined I/O J16 FMC_A_LA[13]_P User Defined I/O K16 FMC_A_LA[14]_N User Defined I/O K17 FMC_A_LA[14]_P User Defined I/O N16 FMC_A_LA[15]_N User Defined I/O N16 FMC_A_LA[15]_P User Defined I/O M16 FMC_A_LA[16]_N User Defined I/O M16 FMC_A_LA[16]_P User Defined I/O M17 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[20]_N User Defined I/O D13 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[11]_N	User Defined I/O	P18
FMC_A_LA[12]_P User Defined I/O N19 FMC_A_LA[13]_N User Defined I/O J16 FMC_A_LA[13]_P User Defined I/O K16 FMC_A_LA[14]_N User Defined I/O K17 FMC_A_LA[14]_P User Defined I/O L17 FMC_A_LA[15]_N User Defined I/O N16 FMC_A_LA[15]_P User Defined I/O M17 FMC_A_LA[16]_N User Defined I/O M17 FMC_A_LA[16]_P User Defined I/O M17 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[11]_P	User Defined I/O	P19
FMC_A_LA[13]_N User Defined I/O J16 FMC_A_LA[13]_P User Defined I/O K16 FMC_A_LA[14]_N User Defined I/O K17 FMC_A_LA[14]_P User Defined I/O L17 FMC_A_LA[15]_N User Defined I/O N16 FMC_A_LA[15]_P User Defined I/O M17 FMC_A_LA[16]_N User Defined I/O M17 FMC_A_LA[16]_P User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[20]_N User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[12]_N	User Defined I/O	N18
FMC_A_LA[13]_P User Defined I/O K16 FMC_A_LA[14]_N User Defined I/O K17 FMC_A_LA[14]_P User Defined I/O L17 FMC_A_LA[15]_N User Defined I/O N16 FMC_A_LA[15]_P User Defined I/O N17 FMC_A_LA[16]_N User Defined I/O M16 FMC_A_LA[16]_P User Defined I/O M17 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[12]_P	User Defined I/O	N19
FMC_A_LA[14]_N User Defined I/O K17 FMC_A_LA[14]_P User Defined I/O L17 FMC_A_LA[15]_N User Defined I/O N16 FMC_A_LA[15]_P User Defined I/O N17 FMC_A_LA[16]_N User Defined I/O M16 FMC_A_LA[16]_P User Defined I/O M17 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[13]_N	User Defined I/O	J16
FMC_A_LA[14]_P User Defined I/O L17 FMC_A_LA[15]_N User Defined I/O N16 FMC_A_LA[15]_P User Defined I/O N17 FMC_A_LA[16]_N User Defined I/O M16 FMC_A_LA[16]_P User Defined I/O M17 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O B12 FMC_A_LA[20]_N User Defined I/O C12	IC_A_LA[13]_P	User Defined I/O	K16
FMC_A_LA[15]_N User Defined I/O N16 FMC_A_LA[15]_P User Defined I/O N17 FMC_A_LA[16]_N User Defined I/O M16 FMC_A_LA[16]_P User Defined I/O M17 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[14]_N	User Defined I/O	K17
FMC_A_LA[15]_P User Defined I/O N17 FMC_A_LA[16]_N User Defined I/O M16 FMC_A_LA[16]_P User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) F15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[14]_P	User Defined I/O	L17
FMC_A_LA[16]_N User Defined I/O M16 FMC_A_LA[16]_P User Defined I/O (clock capable) FMC_A_LA[17]_CC_N User Defined I/O (clock capable) FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[15]_N	User Defined I/O	N16
FMC_A_LA[16]_P User Defined I/O M17 FMC_A_LA[17]_CC_N User Defined I/O (clock capable) E15 FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[15]_P	User Defined I/O	N17
FMC_A_LA[17]_CC_N User Defined I/O (clock capable) FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[16]_N	User Defined I/O	M16
FMC_A_LA[17]_CC_P User Defined I/O (clock capable) F15 FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[16]_P	User Defined I/O	M17
FMC_A_LA[18]_CC_N User Defined I/O (clock capable) H14 FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	_A_LA[17]_CC_N	User Defined I/O (clock capable)	E15
FMC_A_LA[18]_CC_P User Defined I/O (clock capable) J14 FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	_A_LA[17]_CC_P	User Defined I/O (clock capable)	F15
FMC_A_LA[19]_N User Defined I/O C13 FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	_A_LA[18]_CC_N	User Defined I/O (clock capable)	H14
FMC_A_LA[19]_P User Defined I/O D13 FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	_A_LA[18]_CC_P	User Defined I/O (clock capable)	J14
FMC_A_LA[20]_N User Defined I/O B12 FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[19]_N	User Defined I/O	C13
FMC_A_LA[20]_P User Defined I/O C12	IC_A_LA[19]_P	User Defined I/O	D13
	IC_A_LA[20]_N	User Defined I/O	B12
FMC_A_LA[21]_N User Defined I/O J15	IC_A_LA[20]_P	User Defined I/O	C12
	IC_A_LA[21]_N	User Defined I/O	J15
FMC_A_LA[21]_P User Defined I/O K15	IC_A_LA[21]_P	User Defined I/O	K15
FMC_A_LA[22]_N User Defined I/O F14	IC_A_LA[22]_N	User Defined I/O	F14
FMC_A_LA[22]_P User Defined I/O G14	IC_A_LA[22]_P	User Defined I/O	G14
FMC_A_LA[23]_N User Defined I/O A12	IC_A_LA[23]_N	User Defined I/O	A12
FMC_A_LA[23]_P User Defined I/O A13	IC_A_LA[23]_P	User Defined I/O	A13
FMC_A_LA[24]_N User Defined I/O L15	IC_A_LA[24]_N	User Defined I/O	L15
FMC_A_LA[24]_P User Defined I/O M15	IC_A_LA[24]_P	User Defined I/O	M15
FMC_A_LA[25]_N User Defined I/O H13	IC_A_LA[25]_N	User Defined I/O	H13
FMC_A_LA[25]_P User Defined I/O J13	IC_A_LA[25]_P	User Defined I/O	J13
FMC_A_LA[26]_N User Defined I/O F12	IC_A_LA[26]_N	User Defined I/O	F12
FMC_A_LA[26]_P User Defined I/O F13	IC_A_LA[26]_P	User Defined I/O	F13
FMC_A_LA[27]_N User Defined I/O E12	IC_A_LA[27]_N	User Defined I/O	E12
FMC_A_LA[27]_P User Defined I/O E13	IC_A_LA[27]_P	User Defined I/O	E13
FMC_A_LA[28]_N User Defined I/O M14	IC_A_LA[28]_N	User Defined I/O	M14
FMC_A_LA[28]_P User Defined I/O N14	IC_A_LA[28]_P	User Defined I/O	N14
FMC_A_LA[29]_N User Defined I/O L12	IC_A_LA[29]_N	User Defined I/O	L12
FMC_A_LA[29]_P User Defined I/O L13	IC_A_LA[29]_P	User Defined I/O	L13
FMC_A_LA[30]_N User Defined I/O N13	IC_A_LA[30]_N	User Defined I/O	N13
FMC_A_LA[30]_P User Defined I/O P13	IC_A_LA[30]_P	User Defined I/O	P13

FMC_A_LA[31]_N	User Defined I/O	M12
FMC_A_LA[31]_P	User Defined I/O	N12
FMC_A_LA[32]_N	User Defined I/O	R12
FMC_A_LA[32]_P	User Defined I/O	R13
FMC_A_LA[33]_N	User Defined I/O	P14
FMC_A_LA[33]_P	User Defined I/O	P15
FPGA_GC_FMC_A_N		H17
FPGA_GC_FMC_A_P		H18
FMC_A_PG_M2C_F		A14
FMC_A_PRSNT_M2C_L_F		B16
CLK_GTH_FMC_A_N		AE7
CLK_GTH_FMC_A_P		AE8

Table (8): FMC_A Mezzanine Connector FPGA Pin Assignment

Table (9) illustrates FPGA pin assignment for the FMC_B (J4) connector located at the upper right side of the platform.

FMC_B Signal Name	Signal Description	FPGA Pin#
FMC_B_CLK[0]_M2C_N	Mezzanine Card to Carrier Card Clock	AT37
FMC_B_CLK[0]_M2C_P	Mezzanine Card to Carrier Card Clock	AR37
FMC_B_CLK[1]_M2C_N	Mezzanine Card to Carrier Card Clock	AN32
FMC_B_CLK[1]_M2C_P	Mezzanine Card to Carrier Card Clock	AM32
FMC_B_DP[0]_C2M_N	Serial I/O: Carrier to Mezzanine	Y37
FMC_B_DP[0]_C2M_P	Serial I/O: Carrier to Mezzanine	Y36
FMC_B_DP[0]_M2C_N	Serial I/O: Mezzanine to Carrier	W39
FMC_B_DP[0]_M2C_P	Serial I/O: Mezzanine to Carrier	W38
FMC_B_DP[1]_C2M_N	Serial I/O: Carrier to Mezzanine	AC35
FMC_B_DP[1]_C2M_P	Serial I/O: Carrier to Mezzanine	AC34
FMC_B_DP[1]_M2C_N	Serial I/O: Mezzanine to Carrier	AB37
FMC_B_DP[1]_M2C_P	Serial I/O: Mezzanine to Carrier	AB36
FMC_B_DP[2]_C2M_N	Serial I/O: Carrier to Mezzanine	AA35
FMC_B_DP[2]_C2M_P	Serial I/O: Carrier to Mezzanine	AA34
FMC_B_DP[2]_M2C_N	Serial I/O: Mezzanine to Carrier	AA39
FMC_B_DP[2]_M2C_P	Serial I/O: Mezzanine to Carrier	AA38
FMC_B_DP[3]_C2M_N	Serial I/O: Carrier to Mezzanine	W35
FMC_B_DP[3]_C2M_P	Serial I/O: Carrier to Mezzanine	W34
FMC_B_DP[3]_M2C_N	Serial I/O: Mezzanine to Carrier	V37
FMC_B_DP[3]_M2C_P	Serial I/O: Mezzanine to Carrier	V36
FMC_B_DP[4]_C2M_N	Serial I/O: Carrier to Mezzanine	T37
FMC_B_DP[4]_C2M_P	Serial I/O: Carrier to Mezzanine	T36
FMC_B_DP[4]_M2C_N	Serial I/O: Mezzanine to Carrier	R39
FMC_B_DP[4]_M2C_P	Serial I/O: Mezzanine to Carrier	R38