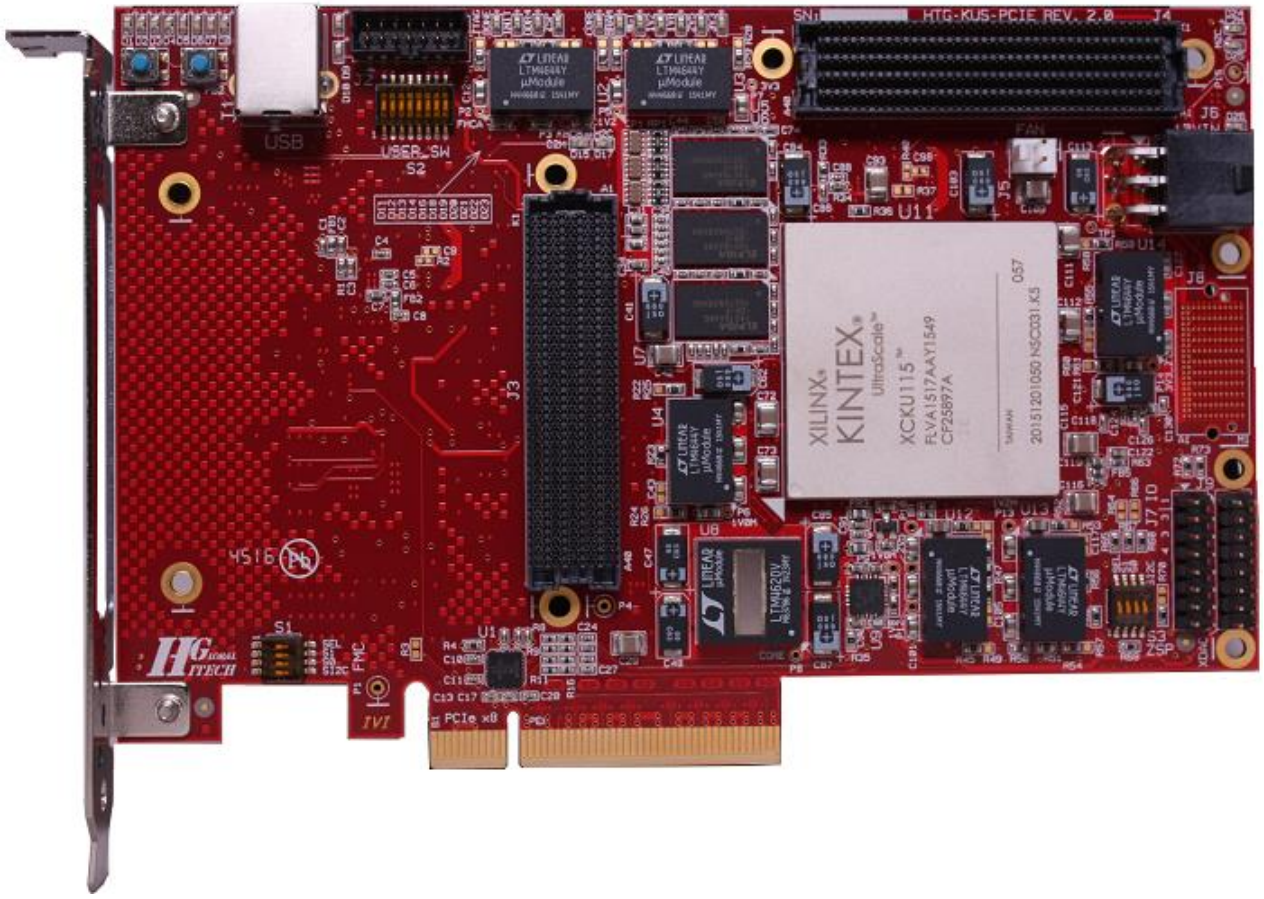
HiTech Global Kintex® UltraScale™ PCI Express Development Platform

HTG-K800 User Manual

Version 1.0 July 2015



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Revision History

Date	Version	Notes
7/15/2015	1.0	

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Chapter 1: Introduction to Xilinx Kintex UltraScale FPGAs

1.1) Overview

Kintex® UltraScale™ devices deliver ASIC-class system-level performance, clock management and power management for next generation price-performance-per-watt. These second generation devices expand the mid-range by delivering the highest throughput with lowest latency for medium-to-high volume applications that include 100G networking, wireless infrastructure, and other DSP-intensive applications. Based on the ASIC-class advantage of the UltraScale architecture, Kintex UltraScale devices are co-optimized with the Vivado® Design Suite and leverage the UltraFAST™ design methodology to accelerate time to market.

The family incorporates:

- ASIC-like clocking for scalability, performance and lower dynamic power
- Next generation routing for rapid timing closure
- Enhanced logic infrastructure for maximum performance and device utilization

Value	Deliverables
Programmable System Integration	• Up to 1.2M logic cells leveraging 2nd generation 3D IC • Multi-chip integration for DSP-intensive applications • Multiple integrated PCI-Express Gen3 cores
Increased System Performance	• 8.2 TeraMACs of DSP compute performance • Up to two speed-grade improvement with high utilization • 16G backplane-capable transceivers, up to 64 per device • 2,400 Mb/s DDR4 for robust operation over varying PVT
BOM Cost Reduction	• System integration reduces application BOM cost by up to 60% • 12.5 Gb/s transceivers in slowest speed grade • 2,400 Mb/s DDR4 in a mid-speed grade • VCXO integration reduces clocking component cost
Total Power Reduction	• Up to 40% lower power vs. previous generation • Fine granular clock gating with UltraScale ASIC-like clocking • Enhanced logic cell packing reduces dynamic power
Accelerated Design Productivity	• Footprint compatibility with Virtex UltraScale for scalability • Co-optimized with Vivado Design Suite for rapid design closure

Table (1) illustrates key features of the Kintex UltraScale devices supported by the HTG-K800 platform.

	Device Name	KU060	KU085	KU115
Logic Resources	Effective LEs (K)	696	1,044	1,393
	Logic Cells (K)	580	871	1,161
	CLB Flip-Flops	663,360	995, 040	1,326,720
	CLB LUTs	331,680	497,520	663,360
Memory Resources	Maximum Distributed RAM (Kb)	9,180	13,770	18,360
	Block RAM/FIFO w/ECC (36Kb each)	1,080	1,620	2,160
	Block RAM/FIFO (18Kb each)	2,160	3,240	4,320
	Total Block RAM (Mb)	38	56.9	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	10	18	24
	I/O DLL	40	56	64
I/O Resources	Maximum Single-Ended HP I/Os	520	520	520
	Maximum Differential HP I/O Pairs	240	240	240
	Maximum Single-Ended HR I/Os	104	104	104
	Maximum Differential HR I/O Pairs	48	56	72
Integrated IP Resources	DSP Slices	2,760	4,100	5,520
	System Monitor	1	2	2
	PCIe® Gen1/2/3	3	3	6
	Interlaken	0	0	0
	100G Ethernet	0	0	0
	16.3Gb/s Transceivers (GTH)	32	48	48

Table (1) Summary of Kintex UltraScale FPGA Features

Chapter 2: HTG-K800 Development Platform Introduction

2.1) Introduction

Supported by Xilinx Kintex UltraScale XCKU-60, 085, or 115 FPGA and wide variety of expansion modules, the HTG-K800 platform is ideal for all applications requiring high performance Xilinx FPGA programmability.

Modular architecture of the HTG-K800 Kintex UltraScale platform provides great level of versatility through two industry standard Vita57.1 FPGA Mezzanine Connectors (FMC) and one Z-RAY High-Speed Bus using Samtec Z-Ray connector (ZSP). Two High-Pin-Count (HPC) FMC connectors provide access to 320 single-ended I/Os and 20 high-speed GTH Serial Transceivers of the onboard Kintex UltraScale FPGA. The Z-RAY High-Speed Serial Bus provides access to 16 GTH Serial Transceivers, single-ended I/O pins for control functions, programmable clock and adjustable power supplies for daughter cards such as Hybrid Memory Cube (HMC), QSFP+, SFP+, SMA breakout, and re-timer/gearbox interfaces (CFP4, QSFP28, etc.)

HiTech Global also offers 100Gig Ethernet MAC and PCS (10x10 and 4x28) IP core for high-speed networking applications.

2.2) Features

The key features of the HTG-K800 platforms include:

► Xilinx Kintex UltraScale (060, 085, or 115) FPGA
► x8 PCI Express Gen3 end point
► x2 FPGA Mezzanine Connector (FMC) High Pin Count (HPC) each with 160 single-ended I/Os (total of 320) and 10 GTH (total of 20) GTH Serial Transceivers
► Z-RAY High-Speed Serial Bus with 16 GTH Serial Transceivers, control I/Os, and 12.V and 3.3V power pins (available for the 085 and 115 models)
- Available Modules:
Hybrid Memory Cube (HMC), SFP+, QSFP+, 100G Gearbox (QSFP28, CFP4, CFP2), SMA breakout, Samtec FireFly
► 72-bit DDR4 Components (2.5GB, DDR4)
► Configuration SPI Flash
► USB/UART
► Programmable Clocks (with default frequencies and programmable through I2C bus)
► XADC Headers
► GPIO Headers
► JTAG Header
► User LEDs, Push Buttons , & Switch
► PCI Express or Standalone operational modes (powered by 6-pin PCIe power connector)
► 6.6" x 4.25"

High-level block diagram and mechanical dimensions of the HTG-K800 platforms are illustrated by figure (1) and (2).

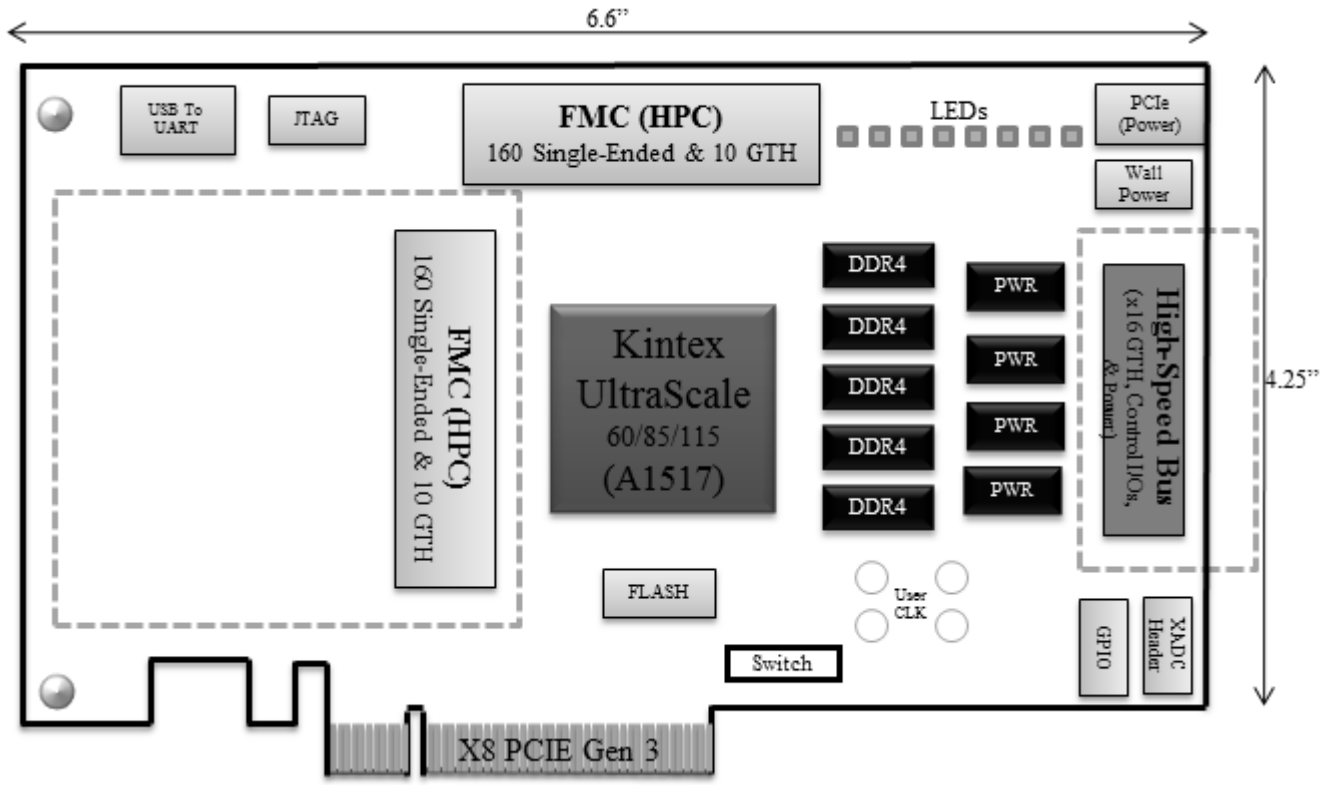


Figure (1): Block Diagram

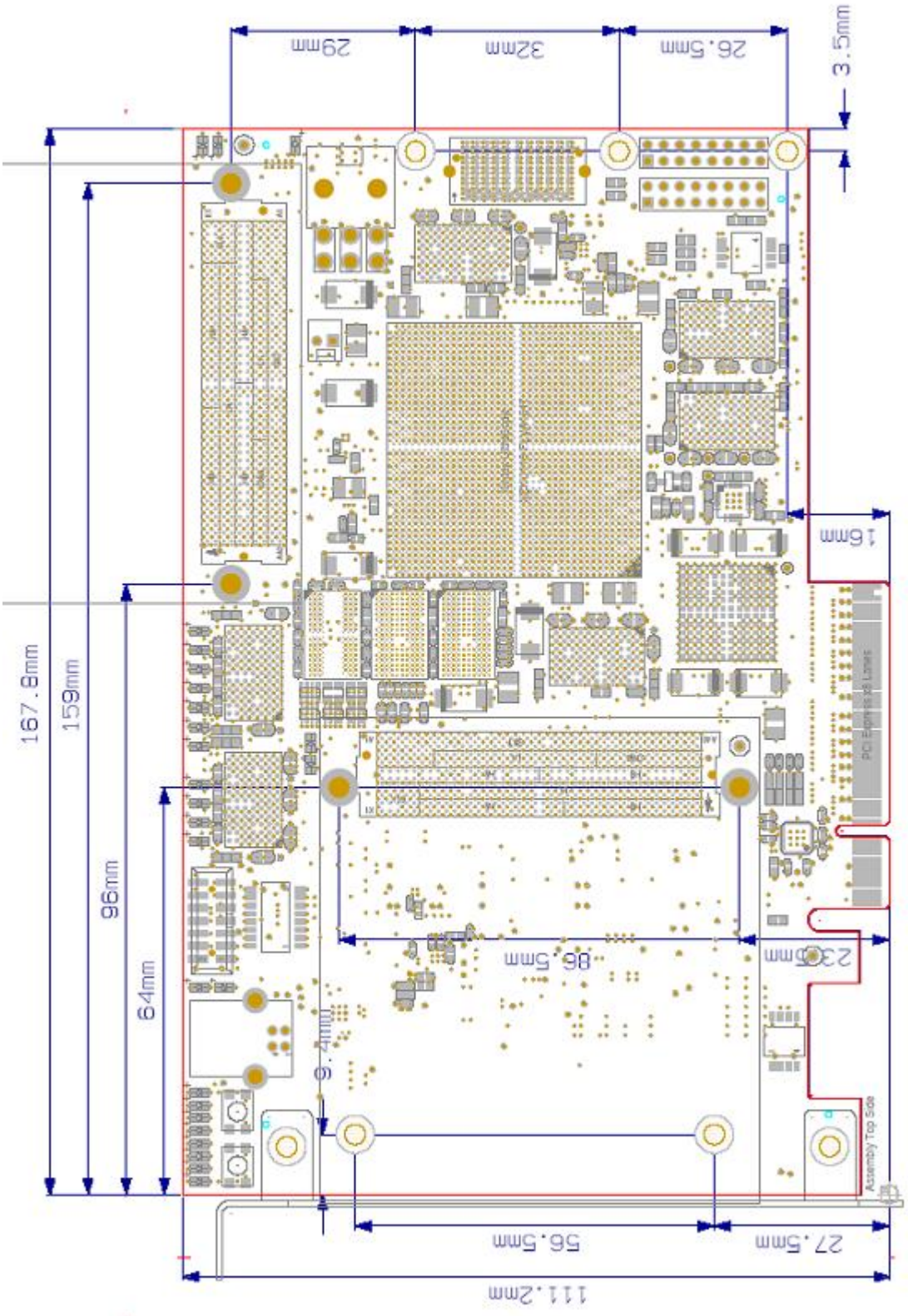


Figure (2): Mechanical Dimensions

Common footprint of the 060, 085, and 115 FPGAs in A1517 package allows usage of one PCB for all 3 devices. FPGA bank assignment for each interface is illustrated by figure (3).

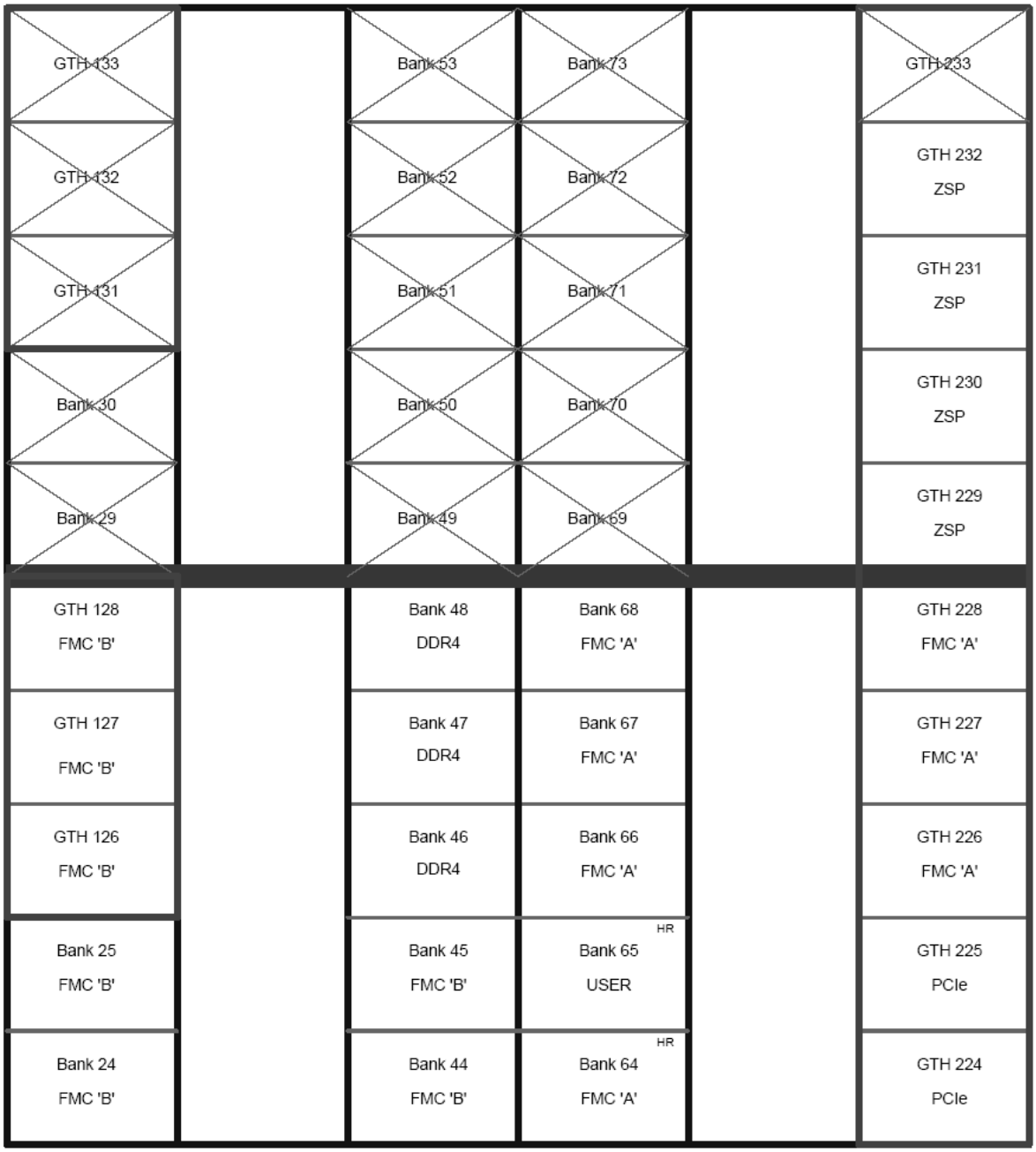


Figure (3): Kintex UltraScale FPGA Bank Assignment

****Note: GTH 229-232 are not available in KU060 FPGA**

2.3) Clock Distribution

For effective utilization of the FPGA resources, the HTG-K800 platforms are supported by different low-jitter / high-performance crystal oscillators. Figure (4) and table (2) illustrate the platform's clock diagram.

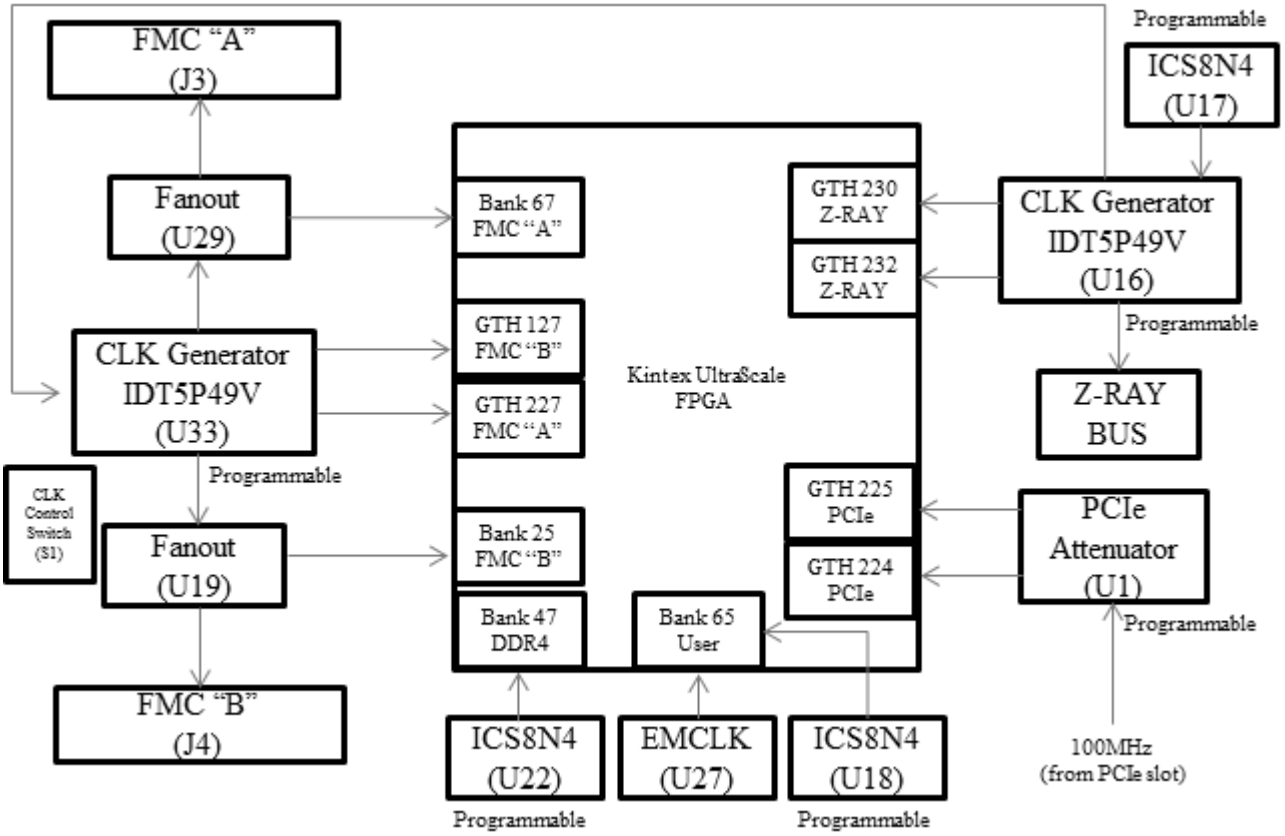


Figure (4): Clock Diagram

Reference Designator	Oscillator Part Number	Oscillator Description
U27	SIT8008AC-82-18E-80.000625	80.000625MHz EMCLK
U17	8N4Q001LG-0055CDI	Z-RAY Bus /FMC I2C Programmable XO with default value of 156.25MHz
U18	8N4Q001LG-0139CDI	FPGA Reference I2C Programmable XO with default value of 200MHz
U22	8N4Q001LG-0139CDI	DDR4 I2C Programmable XO with default value of 200MHz
U16	5P49V5901AdddNLGI	Z-RAY Bus Clock Generator, 5MHz-350MHz, 4 Outputs
U33	5P49V5901AdddNLGI	FMC Clock Generator, 5MHz-350MHz, 4 Outputs

Table (2): Clock Summary

2.4) PCI Express

Xilinx Kintex UltraScale FPGAs support Integrated Root Port and Endpoint for PCI Express solution. The unified architecture of the blocks, along with the AXI4 user interfaces, provides easy migration and design reuse across all supported devices.

The HTG-K800 provides 8 lanes of PCI Express Gen3 (with hard macro controller inside the FPGA) interface through eight GTH serial transceivers.

Table (3) illustrates FPGA pins assignment for PCI Express signals.

Signal Name	FPGA Pin #
PCIE_CLK0_MGT_N	AK9
PCIE_CLK0_MGT_P	AK10
PCIE_CLK1_MGT_N	AT9
PCIE_CLK1_MGT_P	AT10
PCIE_PERST_N_F	AE15
PCIE_RX[0]_N	AM1
PCIE_RX[0]_P	AM2
PCIE_RX[1]_N	AN3
PCIE_RX[1]_P	AN4
PCIE_RX[2]_N	AP1
PCIE_RX[2]_P	AP2
PCIE_RX[3]_N	AR3
PCIE_RX[3]_P	AR4
PCIE_RX[4]_N	AT1
PCIE_RX[4]_P	AT2
PCIE_RX[5]_N	AU3
PCIE_RX[5]_P	AU4
PCIE_RX[6]_N	AV1
PCIE_RX[6]_P	AV2
PCIE_RX[7]_N	AW3
PCIE_RX[7]_P	AW4
PCIE_TX[0]_N	AM5
PCIE_TX[0]_P	AM6
PCIE_TX[1]_N	AN7
PCIE_TX[1]_P	AN8
PCIE_TX[2]_N	AP5
PCIE_TX[2]_P	AP6
PCIE_TX[3]_N	AR7
PCIE_TX[3]_P	AR8
PCIE_TX[4]_N	AT5

PCIE_TX[4]_P	AT6
PCIE_TX[5]_N	AU7
PCIE_TX[5]_P	AU8
PCIE_TX[6]_N	AV5
PCIE_TX[6]_P	AV6
PCIE_TX[7]_N	AW7
PCIE_TX[7]_P	AW8
PCIE_WAKE_N_F	B14

Table (3): PCI Express FPGA Pin Assignments

2.4.1) PCI Express Clock

To provide a clean clock with the lowest possible jitter for the PCI Express interface, the HTG-K800 platform is supported by IDT PCI Express Jitter Attenuator chip (ICS871S1022EKLF). The chip (U1) provides cleaned / jitter-reduced 100MHz or 250MHz clocks for the PCI Express interface. Figure (5) illustrates clock circuit of the PCI Express components.

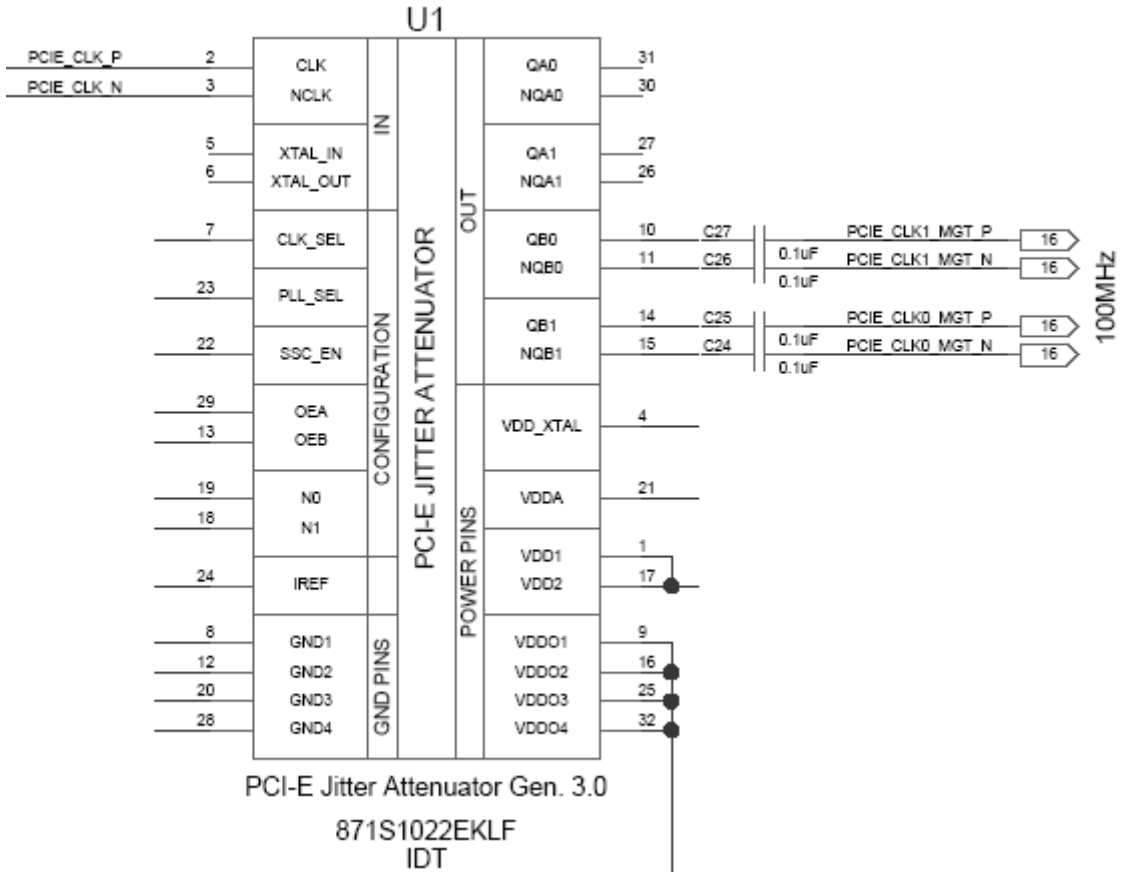


Figure (5): PCI Express Clock Circuit

Output of the PCI Express Jitter Attenuator (U1) is controlled by logic state of the N0 and N1 as shown by table (4) and figure (6)

Inputs			Outputs
In (MHz)	N1:N0	N Divider	
100	00	5	100MHz
100	01	4	125MHz
100	10	2	250MHz
100	11	1	500MHz

Table (4): Jitter Attenuator Mode Selection

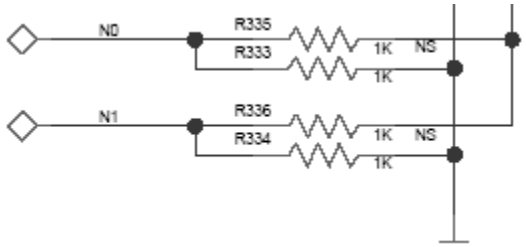


Figure (6): Jitter Attenuator Mode Select Resistor Setting

2.5) DDR-4 Memory Interface

The HTG-K800 platform is populated with five 256 Mb x 16 DDR4 components (Micron EDY4016AABG-DR-F) providing total memory density of 2.5GB. The memory components are connected to the FPGA's banks 46-48.

Table (5) illustrates the FPGA bank assignment for the DDR4 interface.

DDR4 Signal Name	FPGA Pin #
DDR4_A[0]	A30
DDR4_A[1]	D31
DDR4_A[2]	B30
DDR4_A[3]	C29
DDR4_A[4]	C31
DDR4_A[5]	F29
DDR4_A[6]	A32
DDR4_A[7]	J30
DDR4_A[8]	H33
DDR4_A[9]	G29
DDR4_A[10]	E31
DDR4_A[11]	J33
DDR4_A[12]	A28
DDR4_A[13]	H29
DDR4_A[14]	E32
DDR4_A[15]	D29

DDR4_A[16]	D30
DDR4_ACT_N	B32
DDR4_ALERT_N	G30
DDR4_BA[0]	G32
DDR4_BA[1]	E30
DDR4_BG[0]	F32
DDR4_CK_C	K32
DDR4_CK_T	K31
DDR4_CKE	C33
DDR4_CS_N	A29
DDR4_DM_DBI_N[0]	H27
DDR4_DM_DBI_N[1]	M25
DDR4_DM_DBI_N[2]	D28
DDR4_DM_DBI_N[3]	P28
DDR4_DM_DBI_N[4]	F38
DDR4_DM_DBI_N[5]	K36
DDR4_DM_DBI_N[6]	E36
DDR4_DM_DBI_N[7]	G35
DDR4_DM_DBI_N[8]	M31
DDR4_DQ[0]	E28
DDR4_DQ[1]	G26
DDR4_DQ[2]	G27
DDR4_DQ[3]	E27
DDR4_DQ[4]	J26
DDR4_DQ[5]	H26
DDR4_DQ[6]	F28
DDR4_DQ[7]	F27
DDR4_DQ[8]	K26
DDR4_DQ[9]	M27
DDR4_DQ[10]	K28
DDR4_DQ[11]	K27
DDR4_DQ[12]	J28
DDR4_DQ[13]	N24
DDR4_DQ[14]	L27
DDR4_DQ[15]	M24
DDR4_DQ[16]	B26
DDR4_DQ[17]	E26
DDR4_DQ[18]	B25
DDR4_DQ[19]	B27
DDR4_DQ[20]	E25
DDR4_DQ[21]	C27

DDR4_DQ[22]	A25
DDR4_DQ[23]	C26
DDR4_DQ[24]	N26
DDR4_DQ[25]	R27
DDR4_DQ[26]	R28
DDR4_DQ[27]	R26
DDR4_DQ[28]	P26
DDR4_DQ[29]	T28
DDR4_DQ[30]	R25
DDR4_DQ[31]	T25
DDR4_DQ[32]	A38
DDR4_DQ[33]	C37
DDR4_DQ[34]	B37
DDR4_DQ[35]	C39
DDR4_DQ[36]	A37
DDR4_DQ[37]	E37
DDR4_DQ[38]	D39
DDR4_DQ[39]	D38
DDR4_DQ[40]	K35
DDR4_DQ[41]	J39
DDR4_DQ[42]	L35
DDR4_DQ[43]	K37
DDR4_DQ[44]	J35
DDR4_DQ[45]	L37
DDR4_DQ[46]	J34
DDR4_DQ[47]	J38
DDR4_DQ[48]	C36
DDR4_DQ[49]	B34
DDR4_DQ[50]	D35
DDR4_DQ[51]	C34
DDR4_DQ[52]	E35
DDR4_DQ[53]	A34
DDR4_DQ[54]	B36
DDR4_DQ[55]	D34
DDR4_DQ[56]	G39
DDR4_DQ[57]	G36
DDR4_DQ[58]	H36
DDR4_DQ[59]	F37
DDR4_DQ[60]	H39
DDR4_DQ[61]	G34
DDR4_DQ[62]	G37

DDR4_DQ[63]	H34
DDR4_DQ[64]	R30
DDR4_DQ[65]	M29
DDR4_DQ[66]	L33
DDR4_DQ[67]	M30
DDR4_DQ[68]	P30
DDR4_DQ[69]	L30
DDR4_DQ[70]	L29
DDR4_DQ[71]	L32
DDR4_DQS_C[0]	F25
DDR4_DQS_C[1]	K25
DDR4_DQS_C[2]	D26
DDR4_DQS_C[3]	P25
DDR4_DQS_C[4]	B39
DDR4_DQS_C[5]	K38
DDR4_DQS_C[6]	A35
DDR4_DQS_C[7]	H38
DDR4_DQS_C[8]	N29
DDR4_DQS_T[0]	G25
DDR4_DQS_T[1]	L25
DDR4_DQS_T[2]	D25
DDR4_DQS_T[3]	P24
DDR4_DQS_T[4]	C38
DDR4_DQS_T[5]	L38
DDR4_DQS_T[6]	B35
DDR4_DQS_T[7]	H37
DDR4_DQS_T[8]	P29
DDR4_ODT	B31
DDR4_PAR	C32
DDR4_RST_N	H32
DDR4_TEN	F30
SYS_CLK_DDR4_N	E33
SYS_CLK_DDR4_P	F33

Table (5): DDR4 Memory FPGA Pin Assignment

2.5.1) DDR4 Clock

As illustrated by figure (7), clock for the DDR4 interface is generated by the high-performance low-jitter IDT 8N4Q001LG-0139CDI programmable crystal (U22). This oscillator holds up to four factory pre- programmed frequencies that are selectable through resistor settings of the FSEL [1:0] pins as shown by table (6). The default frequency of the U22 is set to 200MHz. The oscillator can also be programmed with different frequencies through its I2C bus.

FSEL [1:0] =00 (R157 & R156)	FSEL [1:0] =01 (R157 & R156)	FSEL [1:0] =10 (R157 & R156)	FSEL [1:0] =11 (R157 & R156)
1st Frequency	**2nd Frequency**	**3rd Frequency**	**4th Frequency**
170	200 (default)	220	250

Table (6): DDR4 Pre-Programmed Frequency Selection

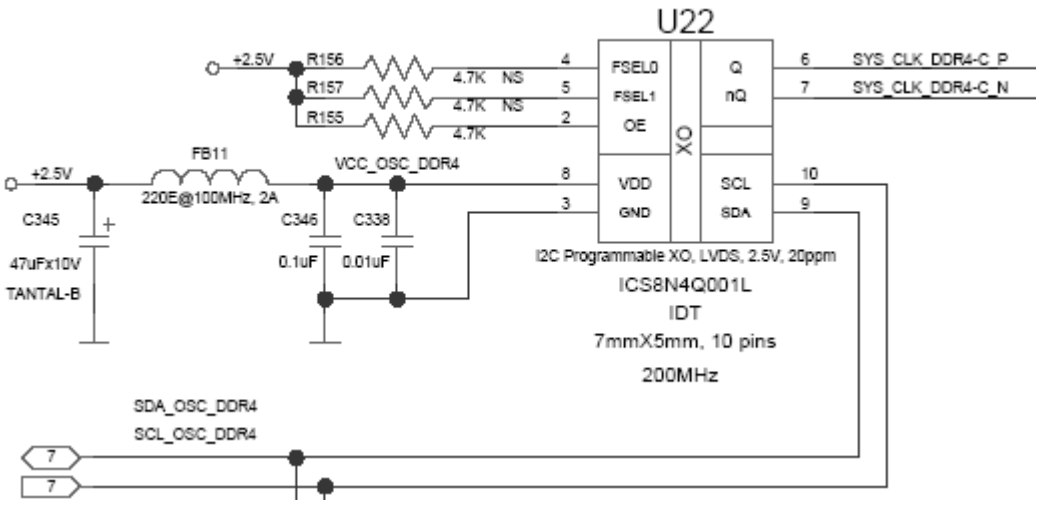


Figure (7): DDR4 Clock Circuit

The ICS8N4Q001 is a Quad-Frequency Programmable Clock Oscillator with very flexible frequency programming and delivers excellent phase noise performance at <0.5 ps rms 1kHz - 20MHz. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance, combined with high power supply noise rejection. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 10-lead ceramic 5mm x 7mm x 1.55mm package. Besides the 4 default power-up frequencies set by the FSEL0 and FSEL1 pins, the ICS8N4Q001 can be programmed via the I2C interface to output clock frequencies between 15.476 to 866.67MHz and from 975 to 1,300MHz to a very high degree of precision with a frequency step size of 435.9Hz ÷ N (N: PLL post divider). Since the FSEL0 and FSEL1 pins are mapped to 4 independent PLL M and N divider registers (P, MINT, MFRAC and N), reprogramming those registers to other frequencies under control of FSEL0 and FSEL1 is supported.

Additional product information is available at http://www.idt.com/document/dst/idt8n4q001-datasheet

2.6) FPGA Mezzanine Card Interfaces

The HTG-K800 platform is populated with **two** 400-pin Samtec connectors (J3 & J4) for High Pin Count (HPC) implementation of Vita 57.1 FPGA Mezzanine Card (FMC) interface. The Vita57.1 calls for fixed location of I/Os, Power, Clocks, and Jtag signals so any compliant module can easily be pluggable into any compliant carrier card.

Each HPC FMC connector provides access to **160** singled ended HR (High Range) I/Os with supporting voltage ranges from 1.2V to 1.8V, **10** GTH (16 Gbps) Serial Transceivers , JTAG signals, Voltage adjustable supplies, I2C signals, and multiple differential clocks.

J3 is located at the front panel side and J4 at the upper right corner of the platform.

HiTech Global provides the following add-on FMC modules with CX4, SFP, SFP+, QSFP+, USB 3.0, SATA, SMA, RJ45, PCI Express Root, AD/DA, and high-end processor.

- **x2 QSFP+ FMC Module** (Part #: HTG-FMC-X2QSFP)
- **x4 SFP/x4 SATA FMC Module** (Part #: HTG-FMC-X4SFP-X4SATA)
- **x4 SFP+ FMC Module** (Part #: HTG-FMC-X4SFP)
- **x10 SFP+ FMC Module** (Part #: HTG-FMC-X10SFP)
- **x8 SMA FMC Module** Part #: HTG-FMC-X8SMA)
- **x8 SMA/x33 LVDS FMC Module** Part #: HTG-FMC-SMA-LVDS)
- **x2 SFP+ FMC Module** (Part #: HTG-FMC-SFP-PLUS)
- **x1 PCIE Root FMC Module** (Part #: HTG-FMC-PCIE-RC)
- **x4 RJ45 FMC Module** (Part #: HTG-FMC-R45-SGMII)
- **x2 CX4 FMC Module** (Part #: HTG-FMC-2CX4)
- **x1 QSFP+/x2 SFP+ FMC Module** (Part #: HTG-FMC-SFP-OC)
- **16-bit AD/DA FMC Module** (serial) connectors (Part #: HTG-FMC-ADDA)

Additional information for the HiTech Global's FMC modules is available at:

http://www.hitechglobal.com/Accessories/FMC_Modules.htm

Figure (8) illustrates FPGA Carrier Card connector (Samtec Part # **ASP-134486-01)** grid labeling (used on the HTG-K800 platform)

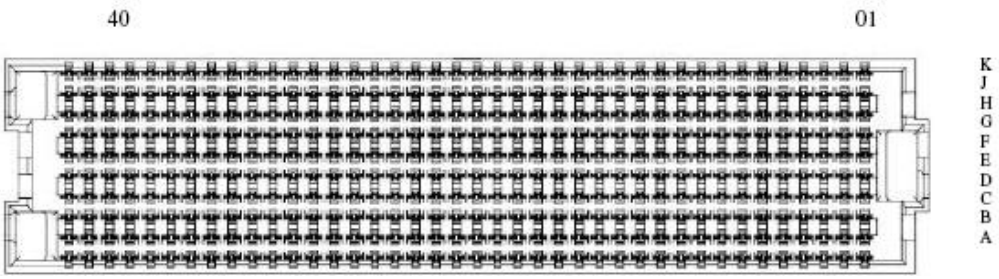


Figure (8): Carrier Card Connector Grid Labeling

Figure (9) illustrates FMC Module connector (Samtec Part # **ASP-134488-01**) grid labeling (used on the HTG-FMC-xxx modules)

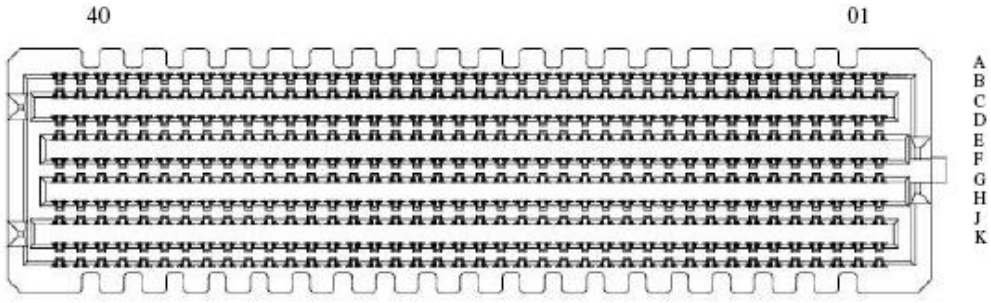


Figure (9): FMC Module Connector Grid Labeling

The ASP-134488-01 connectors are available for purchase at:

https://hitechglobal.us/index.php?route=product/product&path=25&product_id=59

FMC to FMC cables are also available for connecting the HTG-K800 platforms to each other or similar Vita57.1 compliant carrier boards or modules. The FMC to FMC cables are available with lengths of 5" and 9".

Additional information is available at http://hitechglobal.com/FMCModules/FMC_Cable.htm

Image (1) illustrates approximate bend radius for a 9" FMC to FMC cable.

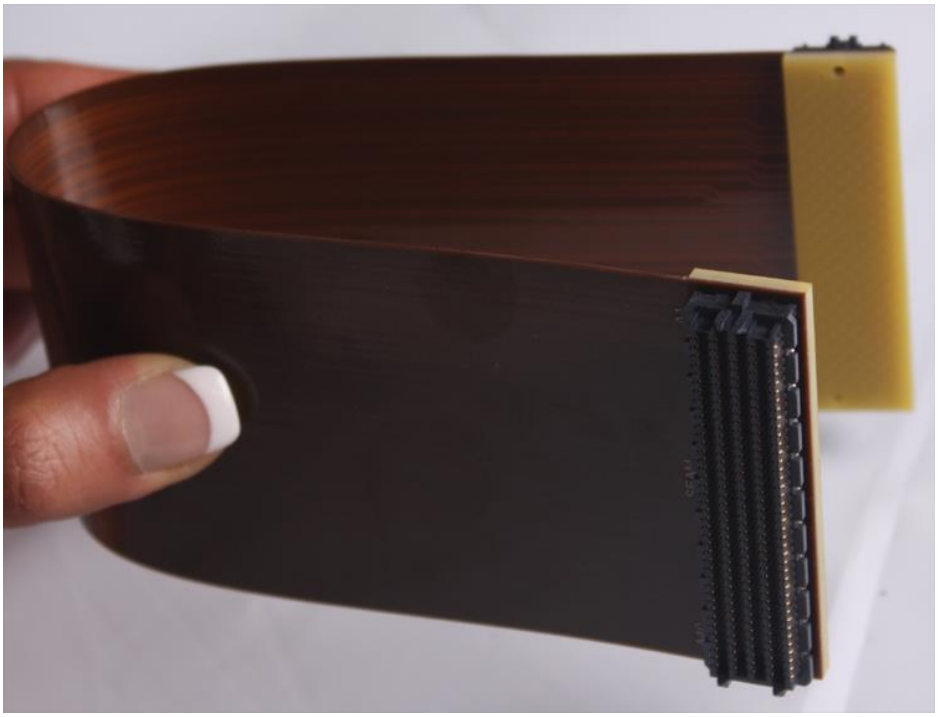


Image (1): FMC To FMC Cable

Table (7) illustrates the exact location of the fixed functional pins on a High Pin Count (HPC) FMC connector.

K	J	H	G	F	E	D	C	B	A
VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
		LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table (7): Vita57.1 FMC Pin Assignment

Table (8) illustrates FPGA pin assignment for the FMC_A (J3) connector located at the front panel side:

FMC_A Signal Name	Signal Description	FPGA Pin #
FMC_A_CLK[0]_M2C_N	Mezzanine Card to Carrier Card Clock	G19
FMC_A_CLK[0]_M2C_P	Mezzanine Card to Carrier Card Clock	H19
FMC_A_CLK[1]_M2C_N	Mezzanine Card to Carrier Card Clock	G15
FMC_A_CLK[1]_M2C_P	Mezzanine Card to Carrier Card Clock	G16
FMC_A_DP[0]_C2M_N	Serial I/O: Carrier to Mezzanine	AF5
FMC_A_DP[0]_C2M_P	Serial I/O: Carrier to Mezzanine	AF6
FMC_A_DP[0]_M2C_N	Serial I/O: Mezzanine to Carrier	AF1
FMC_A_DP[0]_M2C_P	Serial I/O: Mezzanine to Carrier	AF2
FMC_A_DP[1]_C2M_N	Serial I/O: Carrier to Mezzanine	AD5
FMC_A_DP[1]_C2M_P	Serial I/O: Carrier to Mezzanine	AD6
FMC_A_DP[1]_M2C_N	Serial I/O: Mezzanine to Carrier	AC3
FMC_A_DP[1]_M2C_P	Serial I/O: Mezzanine to Carrier	AC4
FMC_A_DP[2]_C2M_N	Serial I/O: Carrier to Mezzanine	AE3
FMC_A_DP[2]_C2M_P	Serial I/O: Carrier to Mezzanine	AE4
FMC_A_DP[2]_M2C_N	Serial I/O: Mezzanine to Carrier	AD1
FMC_A_DP[2]_M2C_P	Serial I/O: Mezzanine to Carrier	AD2
FMC_A_DP[3]_C2M_N	Serial I/O: Carrier to Mezzanine	AG7
FMC_A_DP[3]_C2M_P	Serial I/O: Carrier to Mezzanine	AG8
FMC_A_DP[3]_M2C_N	Serial I/O: Mezzanine to Carrier	AG3
FMC_A_DP[3]_M2C_P	Serial I/O: Mezzanine to Carrier	AG4
FMC_A_DP[4]_C2M_N	Serial I/O: Carrier to Mezzanine	AJ7
FMC_A_DP[4]_C2M_P	Serial I/O: Carrier to Mezzanine	AJ8
FMC_A_DP[4]_M2C_N	Serial I/O: Mezzanine to Carrier	AJ3
FMC_A_DP[4]_M2C_P	Serial I/O: Mezzanine to Carrier	AJ4
FMC_A_DP[5]_C2M_N	Serial I/O: Carrier to Mezzanine	AL7
FMC_A_DP[5]_C2M_P	Serial I/O: Carrier to Mezzanine	AL8
FMC_A_DP[5]_M2C_N	Serial I/O: Mezzanine to Carrier	AL3
FMC_A_DP[5]_M2C_P	Serial I/O: Mezzanine to Carrier	AL4
FMC_A_DP[6]_C2M_N	Serial I/O: Carrier to Mezzanine	AK5
FMC_A_DP[6]_C2M_P	Serial I/O: Carrier to Mezzanine	AK6
FMC_A_DP[6]_M2C_N	Serial I/O: Mezzanine to Carrier	AK1
FMC_A_DP[6]_M2C_P	Serial I/O: Mezzanine to Carrier	AK2
FMC_A_DP[7]_C2M_N	Serial I/O: Carrier to Mezzanine	AH5
FMC_A_DP[7]_C2M_P	Serial I/O: Carrier to Mezzanine	AH6
FMC_A_DP[7]_M2C_N	Serial I/O: Mezzanine to Carrier	AH1
FMC_A_DP[7]_M2C_P	Serial I/O: Mezzanine to Carrier	AH2
FMC_A_DP[8]_C2M_N	Serial I/O: Carrier to Mezzanine	AA3
FMC_A_DP[8]_C2M_P	Serial I/O: Carrier to Mezzanine	AA4

FMC_A_DP[8]_M2C_N	Serial I/O: Mezzanine to Carrier	Y1
FMC_A_DP[8]_M2C_P	Serial I/O: Mezzanine to Carrier	Y2
FMC_A_DP[9]_C2M_N	Serial I/O: Carrier to Mezzanine	AB5
FMC_A_DP[9]_C2M_P	Serial I/O: Carrier to Mezzanine	AB6
FMC_A_DP[9]_M2C_N	Serial I/O: Mezzanine to Carrier	AB1
FMC_A_DP[9]_M2C_P	Serial I/O: Mezzanine to Carrier	AB2
FMC_A_GBTCLK[0]_M2C_	Serial I/O Clock: Mezzanine to Carrier	AC7
FMC_A_GBTCLK[0]_M2C_	Serial I/O Clock: Mezzanine to Carrier	AC8
FMC_A_GBTCLK[1]_M2C_	Serial I/O Clock: Mezzanine to Carrier	AA7
FMC_A_GBTCLK[1]_M2C_	Serial I/O Clock: Mezzanine to Carrier	AA8
FMC_A_HA[0]_CC_N	User Defined I/O (clock capable)	K23
FMC_A_HA[0]_CC_P	User Defined I/O (clock capable)	K22
FMC_A_HA[1]_CC_N	User Defined I/O (clock capable)	J24
FMC_A_HA[1]_CC_P	User Defined I/O (clock capable)	J23
FMC_A_HA[2]_N	User Defined I/O	C24
FMC_A_HA[2]_P	User Defined I/O	D24
FMC_A_HA[3]_N	User Defined I/O	F24
FMC_A_HA[3]_P	User Defined I/O	G24
FMC_A_HA[4]_N	User Defined I/O	E22
FMC_A_HA[4]_P	User Defined I/O	E21
FMC_A_HA[5]_N	User Defined I/O	E23
FMC_A_HA[5]_P	User Defined I/O	F23
FMC_A_HA[6]_N	User Defined I/O	J21
FMC_A_HA[6]_P	User Defined I/O	K21
FMC_A_HA[7]_N	User Defined I/O	B22
FMC_A_HA[7]_P	User Defined I/O	C22
FMC_A_HA[8]_N	User Defined I/O	A22
FMC_A_HA[8]_P	User Defined I/O	B21
FMC_A_HA[9]_N	User Defined I/O	A24
FMC_A_HA[9]_P	User Defined I/O	B24
FMC_A_HA[10]_N	User Defined I/O	P20
FMC_A_HA[10]_P	User Defined I/O	R20
FMC_A_HA[11]_N	User Defined I/O	N22
FMC_A_HA[11]_P	User Defined I/O	N21
FMC_A_HA[12]_N	User Defined I/O	L24
FMC_A_HA[12]_P	User Defined I/O	L23
FMC_A_HA[13]_N	User Defined I/O	C21
FMC_A_HA[13]_P	User Defined I/O	D21
FMC_A_HA[14]_N	User Defined I/O	P21
FMC_A_HA[14]_P	User Defined I/O	R21
FMC_A_HA[15]_N	User Defined I/O	M21

FMC_A_HA[15]_P	User Defined I/O	M20
FMC_A_HA[16]_N	User Defined I/O	K20
FMC_A_HA[16]_P	User Defined I/O	L20
FMC_A_HA[17]_CC_N	User Defined I/O (clock capable)	H24
FMC_A_HA[17]_CC_P	User Defined I/O (clock capable)	H23
FMC_A_HA[18]_CC_N	User Defined I/O (clock capable)	H22
FMC_A_HA[18]_CC_P	User Defined I/O (clock capable)	H21
FMC_A_HA[19]_N	User Defined I/O	G22
FMC_A_HA[19]_P	User Defined I/O	G21
FMC_A_HA[20]_N	User Defined I/O	R23
FMC_A_HA[20]_P	User Defined I/O	T23
FMC_A_HA[21]_N	User Defined I/O	C23
FMC_A_HA[21]_P	User Defined I/O	D23
FMC_A_HA[22]_N	User Defined I/O	N23
FMC_A_HA[22]_P	User Defined I/O	P23
FMC_A_HA[23]_N	User Defined I/O	R22
FMC_A_HA[23]_P	User Defined I/O	T22
FMC_A_HB[0]_CC_N	User Defined I/O (clock capable)	AN19
FMC_A_HB[0]_CC_P	User Defined I/O (clock capable)	AM19
FMC_A_HB[1]_N	User Defined I/O	AV17
FMC_A_HB[1]_P	User Defined I/O	AV18
FMC_A_HB[2]_N	User Defined I/O	AW18
FMC_A_HB[2]_P	User Defined I/O	AV19
FMC_A_HB[3]_N	User Defined I/O	AT20
FMC_A_HB[3]_P	User Defined I/O	AR20
FMC_A_HB[4]_N	User Defined I/O	AL18
FMC_A_HB[4]_P	User Defined I/O	AL19
FMC_A_HB[5]_N	User Defined I/O	AU19
FMC_A_HB[5]_P	User Defined I/O	AT19
FMC_A_HB[6]_CC_N	User Defined I/O (clock capable)	AM17
FMC_A_HB[6]_CC_P	User Defined I/O (clock capable)	AL17
FMC_A_HB[7]_N	User Defined I/O	AT17
FMC_A_HB[7]_P	User Defined I/O	AT18
FMC_A_HB[8]_N	User Defined I/O	AH18
FMC_A_HB[8]_P	User Defined I/O	AH19
FMC_A_HB[9]_N	User Defined I/O	AP18
FMC_A_HB[9]_P	User Defined I/O	AP19
FMC_A_HB[10]_N	User Defined I/O	AR17
FMC_A_HB[10]_P	User Defined I/O	AR18
FMC_A_HB[11]_N	User Defined I/O	AR16
FMC_A_HB[11]_P	User Defined I/O	AP16

FMC_A_HB[12]_N	User Defined I/O	AG19
FMC_A_HB[12]_P	User Defined I/O	AF19
FMC_A_HB[13]_N	User Defined I/O	AJ18
FMC_A_HB[13]_P	User Defined I/O	AJ19
FMC_A_HB[14]_N	User Defined I/O	AH16
FMC_A_HB[14]_P	User Defined I/O	AH17
FMC_A_HB[15]_N	User Defined I/O	AK16
FMC_A_HB[15]_P	User Defined I/O	AJ16
FMC_A_HB[16]_N	User Defined I/O	AK17
FMC_A_HB[16]_P	User Defined I/O	AK18
FMC_A_HB[17]_CC_N	User Defined I/O (clock capable)	AN17
FMC_A_HB[17]_CC_P	User Defined I/O (clock capable)	AN18
FMC_A_HB[18]_N	User Defined I/O	AE16
FMC_A_HB[18]_P	User Defined I/O	AD16
FMC_A_HB[19]_N	User Defined I/O	AF18
FMC_A_HB[19]_P	User Defined I/O	AE18
FMC_A_HB[20]_N	User Defined I/O	AG16
FMC_A_HB[20]_P	User Defined I/O	AG17
FMC_A_HB[21]_N	User Defined I/O	AF17
FMC_A_HB[21]_P	User Defined I/O	AE17
FMC_A_LA[0]_CC_N	User Defined I/O (clock capable)	J19
FMC_A_LA[0]_CC_P	User Defined I/O (clock capable)	J20
FMC_A_LA[1]_CC_N	User Defined I/O (clock capable)	J18
FMC_A_LA[1]_CC_P	User Defined I/O (clock capable)	K18
FMC_A_LA[2]_N	User Defined I/O	E20
FMC_A_LA[2]_P	User Defined I/O	F20
FMC_A_LA[3]_N	User Defined I/O	A20
FMC_A_LA[3]_P	User Defined I/O	B20
FMC_A_LA[4]_N	User Defined I/O	C19
FMC_A_LA[4]_P	User Defined I/O	D19
FMC_A_LA[5]_N	User Defined I/O	A17
FMC_A_LA[5]_P	User Defined I/O	A18
FMC_A_LA[6]_N	User Defined I/O	A19
FMC_A_LA[6]_P	User Defined I/O	B19
FMC_A_LA[7]_N	User Defined I/O	C18
FMC_A_LA[7]_P	User Defined I/O	D18
FMC_A_LA[8]_N	User Defined I/O	B17
FMC_A_LA[8]_P	User Defined I/O	C17
FMC_A_LA[9]_N	User Defined I/O	E17
FMC_A_LA[9]_P	User Defined I/O	F17
FMC_A_LA[10]_N	User Defined I/O	E18

FMC_A_LA[10]_P	User Defined I/O	F18
FMC_A_LA[11]_N	User Defined I/O	P18
FMC_A_LA[11]_P	User Defined I/O	P19
FMC_A_LA[12]_N	User Defined I/O	N18
FMC_A_LA[12]_P	User Defined I/O	N19
FMC_A_LA[13]_N	User Defined I/O	J16
FMC_A_LA[13]_P	User Defined I/O	K16
FMC_A_LA[14]_N	User Defined I/O	K17
FMC_A_LA[14]_P	User Defined I/O	L17
FMC_A_LA[15]_N	User Defined I/O	N16
FMC_A_LA[15]_P	User Defined I/O	N17
FMC_A_LA[16]_N	User Defined I/O	M16
FMC_A_LA[16]_P	User Defined I/O	M17
FMC_A_LA[17]_CC_N	User Defined I/O (clock capable)	E15
FMC_A_LA[17]_CC_P	User Defined I/O (clock capable)	F15
FMC_A_LA[18]_CC_N	User Defined I/O (clock capable)	H14
FMC_A_LA[18]_CC_P	User Defined I/O (clock capable)	J14
FMC_A_LA[19]_N	User Defined I/O	C13
FMC_A_LA[19]_P	User Defined I/O	D13
FMC_A_LA[20]_N	User Defined I/O	B12
FMC_A_LA[20]_P	User Defined I/O	C12
FMC_A_LA[21]_N	User Defined I/O	J15
FMC_A_LA[21]_P	User Defined I/O	K15
FMC_A_LA[22]_N	User Defined I/O	F14
FMC_A_LA[22]_P	User Defined I/O	G14
FMC_A_LA[23]_N	User Defined I/O	A12
FMC_A_LA[23]_P	User Defined I/O	A13
FMC_A_LA[24]_N	User Defined I/O	L15
FMC_A_LA[24]_P	User Defined I/O	M15
FMC_A_LA[25]_N	User Defined I/O	H13
FMC_A_LA[25]_P	User Defined I/O	J13
FMC_A_LA[26]_N	User Defined I/O	F12
FMC_A_LA[26]_P	User Defined I/O	F13
FMC_A_LA[27]_N	User Defined I/O	E12
FMC_A_LA[27]_P	User Defined I/O	E13
FMC_A_LA[28]_N	User Defined I/O	M14
FMC_A_LA[28]_P	User Defined I/O	N14
FMC_A_LA[29]_N	User Defined I/O	L12
FMC_A_LA[29]_P	User Defined I/O	L13
FMC_A_LA[30]_N	User Defined I/O	N13
FMC_A_LA[30]_P	User Defined I/O	P13

FMC_A_LA[31]_N	User Defined I/O	M12
FMC_A_LA[31]_P	User Defined I/O	N12
FMC_A_LA[32]_N	User Defined I/O	R12
FMC_A_LA[32]_P	User Defined I/O	R13
FMC_A_LA[33]_N	User Defined I/O	P14
FMC_A_LA[33]_P	User Defined I/O	P15
FPGA_GC_FMC_A_N		H17
FPGA_GC_FMC_A_P		H18
FMC_A_PG_M2C_F		A14
FMC_A_PRSNT_M2C_L_F		B16
CLK_GTH_FMC_A_N		AE7
CLK_GTH_FMC_A_P		AE8

Table (8): FMC_A Mezzanine Connector FPGA Pin Assignment

Table (9) illustrates FPGA pin assignment for the FMC_B (J4) connector located at the upper right side of the platform.

FMC_B Signal Name	Signal Description	FPGA Pin #
FMC_B_CLK[0]_M2C_N	Mezzanine Card to Carrier Card Clock	AT37
FMC_B_CLK[0]_M2C_P	Mezzanine Card to Carrier Card Clock	AR37
FMC_B_CLK[1]_M2C_N	Mezzanine Card to Carrier Card Clock	AN32
FMC_B_CLK[1]_M2C_P	Mezzanine Card to Carrier Card Clock	AM32
FMC_B_DP[0]_C2M_N	Serial I/O: Carrier to Mezzanine	Y37
FMC_B_DP[0]_C2M_P	Serial I/O: Carrier to Mezzanine	Y36
FMC_B_DP[0]_M2C_N	Serial I/O: Mezzanine to Carrier	W39
FMC_B_DP[0]_M2C_P	Serial I/O: Mezzanine to Carrier	W38
FMC_B_DP[1]_C2M_N	Serial I/O: Carrier to Mezzanine	AC35
FMC_B_DP[1]_C2M_P	Serial I/O: Carrier to Mezzanine	AC34
FMC_B_DP[1]_M2C_N	Serial I/O: Mezzanine to Carrier	AB37
FMC_B_DP[1]_M2C_P	Serial I/O: Mezzanine to Carrier	AB36
FMC_B_DP[2]_C2M_N	Serial I/O: Carrier to Mezzanine	AA35
FMC_B_DP[2]_C2M_P	Serial I/O: Carrier to Mezzanine	AA34
FMC_B_DP[2]_M2C_N	Serial I/O: Mezzanine to Carrier	AA39
FMC_B_DP[2]_M2C_P	Serial I/O: Mezzanine to Carrier	AA38
FMC_B_DP[3]_C2M_N	Serial I/O: Carrier to Mezzanine	W35
FMC_B_DP[3]_C2M_P	Serial I/O: Carrier to Mezzanine	W34
FMC_B_DP[3]_M2C_N	Serial I/O: Mezzanine to Carrier	V37
FMC_B_DP[3]_M2C_P	Serial I/O: Mezzanine to Carrier	V36
FMC_B_DP[4]_C2M_N	Serial I/O: Carrier to Mezzanine	T37
FMC_B_DP[4]_C2M_P	Serial I/O: Carrier to Mezzanine	T36
FMC_B_DP[4]_M2C_N	Serial I/O: Mezzanine to Carrier	R39
FMC_B_DP[4]_M2C_P	Serial I/O: Mezzanine to Carrier	R38

FMC_B_DP[5]_C2M_N	Serial I/O: Carrier to Mezzanine	N35
FMC_B_DP[5]_C2M_P	Serial I/O: Carrier to Mezzanine	N34
FMC_B_DP[5]_M2C_N	Serial I/O: Mezzanine to Carrier	N39
FMC_B_DP[5]_M2C_P	Serial I/O: Mezzanine to Carrier	N38
FMC_B_DP[6]_C2M_N	Serial I/O: Carrier to Mezzanine	R35
FMC_B_DP[6]_C2M_P	Serial I/O: Carrier to Mezzanine	R34
FMC_B_DP[6]_M2C_N	Serial I/O: Mezzanine to Carrier	P37
FMC_B_DP[6]_M2C_P	Serial I/O: Mezzanine to Carrier	P36
FMC_B_DP[7]_C2M_N	Serial I/O: Carrier to Mezzanine	U35
FMC_B_DP[7]_C2M_P	Serial I/O: Carrier to Mezzanine	U34
FMC_B_DP[7]_M2C_N	Serial I/O: Mezzanine to Carrier	U39
FMC_B_DP[7]_M2C_P	Serial I/O: Mezzanine to Carrier	U38
FMC_B_DP[8]_C2M_N	Serial I/O: Carrier to Mezzanine	AE35
FMC_B_DP[8]_C2M_P	Serial I/O: Carrier to Mezzanine	AE34
FMC_B_DP[8]_M2C_N	Serial I/O: Mezzanine to Carrier	AE39
FMC_B_DP[8]_M2C_P	Serial I/O: Mezzanine to Carrier	AE38
FMC_B_DP[9]_C2M_N	Serial I/O: Carrier to Mezzanine	AD37
FMC_B_DP[9]_C2M_P	Serial I/O: Carrier to Mezzanine	AD36
FMC_B_DP[9]_M2C_N	Serial I/O: Mezzanine to Carrier	AC39
FMC_B_DP[9]_M2C_P	Serial I/O: Mezzanine to Carrier	AC38
FMC_B_GBTCLK[0]_M2C_	Serial I/O Clock: Mezzanine to Carrier	Y33
FMC_B_GBTCLK[0]_M2C_	Serial I/O Clock: Mezzanine to Carrier	Y32
FMC_B_GBTCLK[1]_M2C_	Serial I/O Clock: Mezzanine to Carrier	T33
FMC_B_GBTCLK[1]_M2C_	Serial I/O Clock: Mezzanine to Carrier	T32
FMC_B_HA[0]_CC_N	User Defined I/O (clock capable)	AL28
FMC_B_HA[0]_CC_P	User Defined I/O (clock capable)	AL27
FMC_B_HA[1]_CC_N	User Defined I/O (clock capable)	AN27
FMC_B_HA[1]_CC_P	User Defined I/O (clock capable)	AM27
FMC_B_HA[2]_N	User Defined I/O	AE26
FMC_B_HA[2]_P	User Defined I/O	AD26
FMC_B_HA[3]_N	User Defined I/O	AE25
FMC_B_HA[3]_P	User Defined I/O	AD25
FMC_B_HA[4]_N	User Defined I/O	AR25
FMC_B_HA[4]_P	User Defined I/O	AP25
FMC_B_HA[5]_N	User Defined I/O	AW28
FMC_B_HA[5]_P	User Defined I/O	AV28
FMC_B_HA[6]_N	User Defined I/O	AF27
FMC_B_HA[6]_P	User Defined I/O	AE27
FMC_B_HA[7]_N	User Defined I/O	AG27
FMC_B_HA[7]_P	User Defined I/O	AG26
FMC_B_HA[8]_N	User Defined I/O	AM25

FMC_B_HA[8]_P	User Defined I/O	AM24
FMC_B_HA[9]_N	User Defined I/O	AR27
FMC_B_HA[9]_P	User Defined I/O	AR26
FMC_B_HA[10]_N	User Defined I/O	AG25
FMC_B_HA[10]_P	User Defined I/O	AF25
FMC_B_HA[11]_N	User Defined I/O	AV27
FMC_B_HA[11]_P	User Defined I/O	AV26
FMC_B_HA[12]_N	User Defined I/O	AP28
FMC_B_HA[12]_P	User Defined I/O	AN28
FMC_B_HA[13]_N	User Defined I/O	AJ24
FMC_B_HA[13]_P	User Defined I/O	AH24
FMC_B_HA[14]_N	User Defined I/O	AJ26
FMC_B_HA[14]_P	User Defined I/O	AH26
FMC_B_HA[15]_N	User Defined I/O	AG24
FMC_B_HA[15]_P	User Defined I/O	AF24
FMC_B_HA[16]_N	User Defined I/O	AK25
FMC_B_HA[16]_P	User Defined I/O	AJ25
FMC_B_HA[17]_CC_N	User Defined I/O (clock capable)	AK28
FMC_B_HA[17]_CC_P	User Defined I/O (clock capable)	AK27
FMC_B_HA[18]_CC_N	User Defined I/O (clock capable)	AN26
FMC_B_HA[18]_CC_P	User Defined I/O (clock capable)	AM26
FMC_B_HA[19]_N	User Defined I/O	AU26
FMC_B_HA[19]_P	User Defined I/O	AU25
FMC_B_HA[20]_N	User Defined I/O	AU27
FMC_B_HA[20]_P	User Defined I/O	AT27
FMC_B_HA[21]_N	User Defined I/O	AL25
FMC_B_HA[21]_P	User Defined I/O	AL24
FMC_B_HA[22]_N	User Defined I/O	AT28
FMC_B_HA[22]_P	User Defined I/O	AR28
FMC_B_HA[23]_N	User Defined I/O	AW26
FMC_B_HA[23]_P	User Defined I/O	AW25
FMC_B_HB[0]_CC_N	User Defined I/O (clock capable)	AN21
FMC_B_HB[0]_CC_P	User Defined I/O (clock capable)	AM21
FMC_B_HB[1]_N	User Defined I/O	AG22
FMC_B_HB[1]_P	User Defined I/O	AG21
FMC_B_HB[2]_N	User Defined I/O	AH23
FMC_B_HB[2]_P	User Defined I/O	AH22
FMC_B_HB[3]_N	User Defined I/O	AF23
FMC_B_HB[3]_P	User Defined I/O	AE23
FMC_B_HB[4]_N	User Defined I/O	AK21
FMC_B_HB[4]_P	User Defined I/O	AK20

FMC_B_HB[5]_N	User Defined I/O	AJ21
FMC_B_HB[5]_P	User Defined I/O	AJ20
FMC_B_HB[6]_CC_N	User Defined I/O (clock capable)	AN22
FMC_B_HB[6]_CC_P	User Defined I/O (clock capable)	AM22
FMC_B_HB[7]_N	User Defined I/O	AT24
FMC_B_HB[7]_P	User Defined I/O	AT23
FMC_B_HB[8]_N	User Defined I/O	AL22
FMC_B_HB[8]_P	User Defined I/O	AK22
FMC_B_HB[9]_N	User Defined I/O	AM20
FMC_B_HB[9]_P	User Defined I/O	AL20
FMC_B_HB[10]_N	User Defined I/O	AV22
FMC_B_HB[10]_P	User Defined I/O	AU21
FMC_B_HB[11]_N	User Defined I/O	AU22
FMC_B_HB[11]_P	User Defined I/O	AT22
FMC_B_HB[12]_N	User Defined I/O	AR21
FMC_B_HB[12]_P	User Defined I/O	AP21
FMC_B_HB[13]_N	User Defined I/O	AP24
FMC_B_HB[13]_P	User Defined I/O	AN24
FMC_B_HB[14]_N	User Defined I/O	AW23
FMC_B_HB[14]_P	User Defined I/O	AV23
FMC_B_HB[15]_N	User Defined I/O	AW21
FMC_B_HB[15]_P	User Defined I/O	AV21
FMC_B_HB[16]_N	User Defined I/O	AW24
FMC_B_HB[16]_P	User Defined I/O	AV24
FMC_B_HB[17]_CC_N	User Defined I/O (clock capable)	AL23
FMC_B_HB[17]_CC_P	User Defined I/O (clock capable)	AK23
FMC_B_HB[18]_N	User Defined I/O	AF22
FMC_B_HB[18]_P	User Defined I/O	AE22
FMC_B_HB[19]_N	User Defined I/O	AP23
FMC_B_HB[19]_P	User Defined I/O	AN23
FMC_B_HB[20]_N	User Defined I/O	AD21
FMC_B_HB[20]_P	User Defined I/O	AD20
FMC_B_HB[21]_N	User Defined I/O	AE21
FMC_B_HB[21]_P	User Defined I/O	AE20
FMC_B_LA[0]_CC_N	User Defined I/O (clock capable)	AN37
FMC_B_LA[0]_CC_P	User Defined I/O (clock capable)	AN36
FMC_B_LA[1]_CC_N	User Defined I/O (clock capable)	AR36
FMC_B_LA[1]_CC_P	User Defined I/O (clock capable)	AP36
FMC_B_LA[2]_N	User Defined I/O	AT33
FMC_B_LA[2]_P	User Defined I/O	AR33
FMC_B_LA[3]_N	User Defined I/O	AU34

FMC_B_LA[3]_P	User Defined I/O	AT34
FMC_B_LA[4]_N	User Defined I/O	AW36
FMC_B_LA[4]_P	User Defined I/O	AW35
FMC_B_LA[5]_N	User Defined I/O	AV37
FMC_B_LA[5]_P	User Defined I/O	AU37
FMC_B_LA[6]_N	User Defined I/O	AV36
FMC_B_LA[6]_P	User Defined I/O	AU36
FMC_B_LA[7]_N	User Defined I/O	AP38
FMC_B_LA[7]_P	User Defined I/O	AN38
FMC_B_LA[8]_N	User Defined I/O	AV39
FMC_B_LA[8]_P	User Defined I/O	AV38
FMC_B_LA[9]_N	User Defined I/O	AU39
FMC_B_LA[9]_P	User Defined I/O	AT39
FMC_B_LA[10]_N	User Defined I/O	AU35
FMC_B_LA[10]_P	User Defined I/O	AT35
FMC_B_LA[11]_N	User Defined I/O	AL38
FMC_B_LA[11]_P	User Defined I/O	AL37
FMC_B_LA[12]_N	User Defined I/O	AP39
FMC_B_LA[12]_P	User Defined I/O	AN39
FMC_B_LA[13]_N	User Defined I/O	AM35
FMC_B_LA[13]_P	User Defined I/O	AM34
FMC_B_LA[14]_N	User Defined I/O	AM37
FMC_B_LA[14]_P	User Defined I/O	AM36
FMC_B_LA[15]_N	User Defined I/O	AK36
FMC_B_LA[15]_P	User Defined I/O	AK35
FMC_B_LA[16]_N	User Defined I/O	AK38
FMC_B_LA[16]_P	User Defined I/O	AK37
FMC_B_LA[17]_CC_N	User Defined I/O (clock capable)	AM29
FMC_B_LA[17]_CC_P	User Defined I/O (clock capable)	AL29
FMC_B_LA[18]_CC_N	User Defined I/O (clock capable)	AM30
FMC_B_LA[18]_CC_P	User Defined I/O (clock capable)	AL30
FMC_B_LA[19]_N	User Defined I/O	AV31
FMC_B_LA[19]_P	User Defined I/O	AU31
FMC_B_LA[20]_N	User Defined I/O	AU30
FMC_B_LA[20]_P	User Defined I/O	AU29
FMC_B_LA[21]_N	User Defined I/O	AL32
FMC_B_LA[21]_P	User Defined I/O	AK32
FMC_B_LA[22]_N	User Defined I/O	AR32
FMC_B_LA[22]_P	User Defined I/O	AR31
FMC_B_LA[23]_N	User Defined I/O	AV32
FMC_B_LA[23]_P	User Defined I/O	AU32

FMC_B_LA[24]_N	User Defined I/O	AK31
FMC_B_LA[24]_P	User Defined I/O	AJ31
FMC_B_LA[25]_N	User Defined I/O	AK33
FMC_B_LA[25]_P	User Defined I/O	AJ33
FMC_B_LA[26]_N	User Defined I/O	AK30
FMC_B_LA[26]_P	User Defined I/O	AJ30
FMC_B_LA[27]_N	User Defined I/O	AP33
FMC_B_LA[27]_P	User Defined I/O	AN33
FMC_B_LA[28]_N	User Defined I/O	AJ29
FMC_B_LA[28]_P	User Defined I/O	AH29
FMC_B_LA[29]_N	User Defined I/O	AH32
FMC_B_LA[29]_P	User Defined I/O	AH31
FMC_B_LA[30]_N	User Defined I/O	AG29
FMC_B_LA[30]_P	User Defined I/O	AF29
FMC_B_LA[31]_N	User Defined I/O	AF30
FMC_B_LA[31]_P	User Defined I/O	AE30
FMC_B_LA[32]_N	User Defined I/O	AJ28
FMC_B_LA[32]_P	User Defined I/O	AH28
FMC_B_LA[33]_N	User Defined I/O	AF28
FMC_B_LA[33]_P	User Defined I/O	AE28
FMC_B_PG_M2C_F		B15
FMC_B_PRSNT_M2C_L_F		C14
FPGA_GC_FMC_B_N		AT38
FPGA_GC_FMC_B_P		AR38
CLK_GTH_FMC_B_N		V33
CLK_GTH_FMC_B_P		V32

Table (9): FMC_B Mezzanine Connector FPGA Pin Assignment

2.6.1.) V_Adjust

V_Adjust is provided on the FMC connector to simplify the power management on the FMC module so that the limited space on the module can be fully used for the I/O functionality and to minimize any noise that would come from a power supply onboard the module.

With the wide range of I/O that may exist on a FMC module, it is difficult to specify a single universal voltage that would not need conversion to suit the devices on the modules. Therefore, this flexible mechanism of obtaining a preconditioned power source from the carrier card and defined by the IPMI provides a powerful feature for simplified system design.

V_Adjust for the FMC_A and FMC_B is generated and controlled by U2 (Linear Tech LTM4644) and setting value of the R7 and R12 resistors using the following formula:

R= [30.2] / [(V_Adjust / 0.6) -1]

Default setting of the V_Adjust for the FMC_A and FMC_B is 1.8V (Maximum)

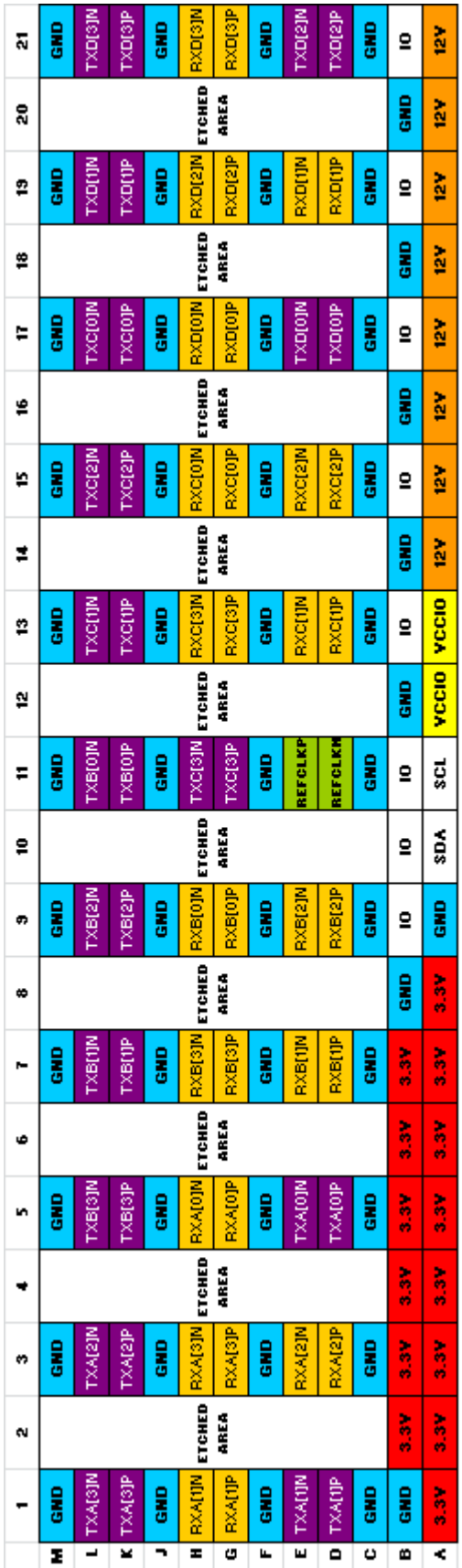
2.7) Z-RAY High-Speed Serial Bus

****** Available with the 085 and 115 models**

Z-Ray® micro array interposer is ultra-low profile, high density, highly customizable solution for board-to-board, IC-to-board, and cable-to-board applications. With performance of 20GHz, this interface is ideal for serial transceivers and signals running at 28Gbps.

The Z-RAY High-Speed Serial bus of the HTG-K800 platform provides access to sixteen GTH serial transceivers, control signals, clock, and voltage pins for additional daughter card interface. HiTech Global provides Z-RAY daughter cards with Hybrid Memory Cube (HMC), Gearbox CFP4, and QSFP28 ports.

Table (10) and (11) illustrate Z-RAY pinouts and FPGA pin assignment for the Z-RAY interface.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	13	20	21
M	GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND
L	TXA[3]N		TXA[2]N		TXB[3]N		TXB[1]N		TXB[2]N		TXB[0]N		TXC[1]N		TXC[2]N		TXC[0]N		TXD[1]N		TXD[3]N
K	TXA[3]P		TXA[2]P		TXB[3]P		TXB[1]P		TXB[2]P		TXB[0]P		TXC[1]P		TXC[2]P		TXC[0]P		TXD[1]P		TXD[3]P
J	GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND
H	RXA[1]N	ETCHED AREA	RXA[3]N	ETCHED AREA	RXA[0]N	ETCHED AREA	RXB[3]N	ETCHED AREA	RXB[0]N	ETCHED AREA	TXC[3]N	ETCHED AREA	RXC[3]N	ETCHED AREA	RXC[0]N	ETCHED AREA	RXD[0]N	ETCHED AREA	RXD[2]N	ETCHED AREA	RXD[3]N
G	RXA[1]P		RXA[3]P		RXA[0]P		RXB[3]P		RXB[0]P		TXC[3]P		RXC[3]P		RXC[0]P		RXD[0]P		RXD[2]P		RXD[3]P
F	GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND
E	TXA[1]N		RXA[2]N		TXA[0]N		RXB[1]N		RXB[2]N		REFCLKP		RXC[1]N		RXC[2]N		TXD[0]N		RXD[1]N		TXD[2]N
D	TXA[1]P		RXA[2]P		TXA[0]P		RXB[1]P		RXB[2]P		REFCLKM		RXC[1]P		RXC[2]P		TXD[0]P		RXD[1]P		TXD[2]P
C	GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		GND
B	GND	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	GND	IO	IO	IO	GND	IO	GND	IO	GND	IO	GND	IO	GND	IO
A	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	GND	$DA	$CL	YCCIO	YCCIO	12V	12V	12V	12V	12V	12V	12V	12V

Table (10): Z-RAY Bus Pinouts

Signal Name	Z-RAY Pin #	FPGA Pin #
L2RX[0]_N	H5	N3
L2RX[0]_P	G5	N4
L2RX[1]_N	H1	P1
L2RX[1]_P	G1	P2
L2RX[2]_N	E3	R3
L2RX[2]_P	D3	R4
L2RX[3]_N	H3	T1
L2RX[3]_P	G3	T2
L2RX[4]_N	H9	J3
L2RX[4]_P	G9	J4
L2RX[5]_N	E7	K1
L2RX[5]_P	D7	K2
L2RX[6]_N	E9	L3
L2RX[6]_P	D9	L4
L2RX[7]_N	H7	M1
L2RX[7]_P	G7	M2
L2RX[8]_N	H15	E3
L2RX[8]_P	G15	E4
L2RX[9]_N	E13	G3
L2RX[9]_P	D13	G4
L2RX[10]_N	E15	F1
L2RX[10]_P	D15	F2
L2RX[11]_N	H13	H1
L2RX[11]_P	G13	H2
L2RX[12]_N	H17	D1
L2RX[12]_P	G17	D2
L2RX[13]_N	E19	C3
L2RX[13]_P	D19	C4
L2RX[14]_N	H19	B1
L2RX[14]_P	G19	B2
L2RX[15]_N	H21	A3
L2RX[15]_P	G21	A4
L2TX[0]_N	E5	N7
L2TX[0]_P	D5	N8
L2TX[1]_N	E1	P5
L2TX[1]_P	D1	P6
L2TX[2]_N	L3	T5
L2TX[2]_P	K3	T6
L2TX[3]_N	L1	U3

L2TX[3]_P	K1	U4
L2TX[4]_N	L11	J7
L2TX[4]_P	K11	J8
L2TX[5]_N	L7	K5
L2TX[5]_P	K7	K6
L2TX[6]_N	L9	L7
L2TX[6]_P	K9	L8
L2TX[7]_N	L5	M5
L2TX[7]_P	K5	M6
L2TX[8]_N	L17	E7
L2TX[8]_P	K17	E8
L2TX[9]_N	L13	G7
L2TX[9]_P	K13	G8
L2TX[10]_N	L15	F5
L2TX[10]_P	K15	F6
L2TX[11]_N	H11	H5
L2TX[11]_P	G11	H6
L2TX[12]_N	E17	D5
L2TX[12]_P	D17	D6
L2TX[13]_N	L19	C7
L2TX[13]_P	K19	C8
L2TX[14]_N	E21	B5
L2TX[14]_P	D21	B6
L2TX[15]_N	L21	A7
L2TX[15]_P	K21	A8
MGT_ZSP_REFCLK0_N		F9
MGT_ZSP_REFCLK0_P		F10
MGT_ZSP_REFCLK1_N		P9
MGT_ZSP_REFCLK1_P		P10
ZSP_IO1_F	B9	AP29
ZSP_IO2_F	B10	AW29
ZSP_IO3_F	B11	AV29
ZSP_IO4_F	B13	AT29
ZSP_IO5_F	B15	AW30
ZSP_IO6_F	B17	AT30
ZSP_IO7_F	B19	AR30
ZSP_IO8_F	B21	AW31
ZSP_REFCLK_N	D11	
ZSP_REFCLK_P	E11	

Table (11): Z-RAY FPGA Pin Assignment

Figure (10) illustrates mechanical dimension of mating Z-RAY connector (Samtec : ZSP-184731-01-ZA8-D) for daughter card development.

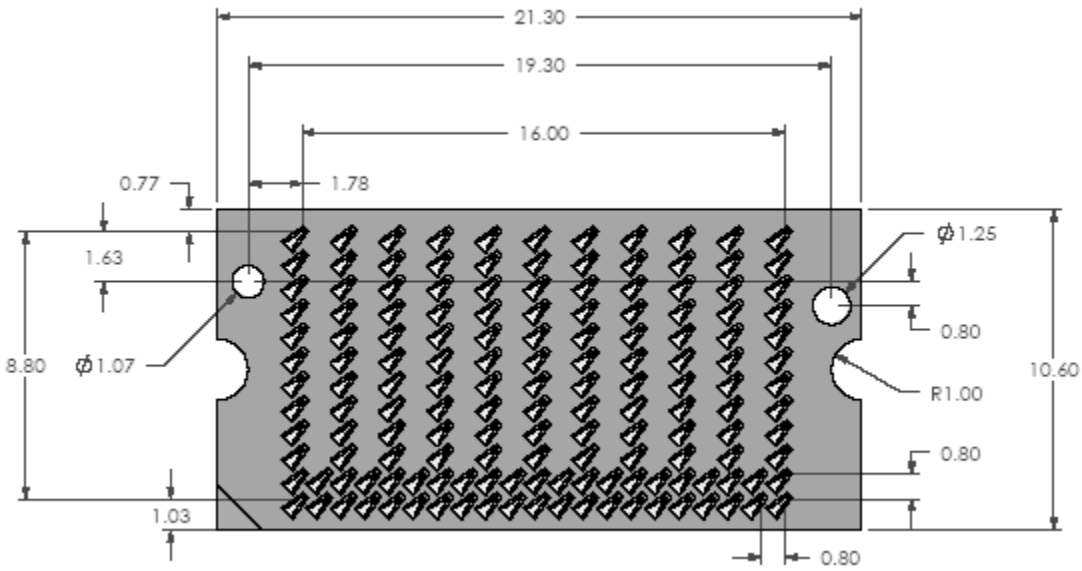


Figure (10): Z-RAY Mating Connector's Mechanical Dimensions

For faster and easier procurement process, the Z-RAY connector is available for purchase through HiTech Global's online store at https://hitechglobal.us/index.php?route=product/product&path=25&product_id=186

2.8) USB To UART Bridge

The HTG-K800 platform provides one UART port through a peripheral USB connector. The port is supported by the Silicon labs CP2103 USB to UART controller chip.

The CP2103 is a highly-integrated USB-to-UART Bridge Controller providing a simple solution for updating RS-232/RS-485 designs to USB using a minimum of components and PCB space. The CP2103 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) with full modem control signals. No other external USB components are required.

The on-chip EEPROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number, and Device Serial Number as desired for OEM applications. The EEPROM is programmed on-board via the USB, allowing the programming step to be easily integrated into the product manufacturing and testing process.

Royalty-free Virtual COM Port (VCP) device drivers provided by Silicon Laboratories allow a CP2103-based product to appear as a COM port to PC applications. The CP2103 UART interface implements all RS-232/RS-485 signals, including control and handshaking signals; so, existing system firmware does not need to be modified. The device also features up to four GPIO signals that can be user-defined for status and control information.

Direct access driver support is available through the Silicon Laboratories USBXpress driver set.

Table (12) illustrates FPGA pin assignment for the USB-TO-UART interface:

UART/USB Bridge Signal Name	FPGA Pin #
UART_CTS	AR15
UART_GPIO0	AR13
UART_GPIO1	AT13
UART_GPIO2	AN12
UART_GPIO3	AJ13
UART_RST_N	AN13
UART_RTS	AM14
UART_RXD	AP15
UART_SUSPEND_N	AJ14
UART_TXD	AL14

Table (12): USB To UART FPGA Pin Assignment

2.9 LEDs, GPIO Headers & Pushbuttons

Table (13) illustrates FPGA pins assignments for the user LEDs, Push Buttons, Switches, and XADC interfaces.

Signal Name	Location	FPGA Pin #
USER_IO1	J7 -1	AV16
USER_IO2	J7 -3	AW15
USER_IO3	J7 -5	AV14
USER_IO4	J7 -7	AW14
USER_IO5	J7 -9	AU14
USER_IO6	J7 -11	AT14
USER_IO7	J7 -13	AU12
USER_IO8	J7 -15	AV12
USER_LED1_G_F	D1	J31
USER_LED2_G_F	D2	H31
USER_LED3_G_F	D3	J29
USER_LED4_G_F	D4	G31
USER_LED5_R_F	D5	K30
USER_LED6_R_F	D6	M26
USER_LED7_R_F	D7	L28
USER_LED8_R_F	D8	M32
USER_PB1	PB1	D36
USER_PB2	PB2	D33
USER_SW1	S2-1	F35
USER_SW2	S2-2	H28
USER_SW3	S2-3	J25
USER_SW4	S2-4	B29
USER_SW5	S2-5	A33
USER_SW6	S2-6	E38
USER_SW7	S2-7	F34

USER_SW8	S2-8	F39
XDAC_AD12_F_N	J9-13	AT12
XDAC_AD12_F_P	J9-14	AR12
XDAC_AD15_F_N	J9-11	AW13
XDAC_AD15_F_P	J9-12	AV13
XDAC_AD4_F_N	J9-7	AP13
XDAC_AD4_F_P	J9-8	AP14
XDAC_AD7_F_N	J9-9	AU15
XDAC_AD7_F_P	J9-10	AT15
XDAC_VN_F	J9-5	AA15
XDAC_VP_F	J9-6	Y16
I2C_SCLK_65	J9-3	AE12
I2C_SDA_65	J9-4	AF12

Table (13): User Interface FPGA pin assignment

2.10) I2C Bus Switch

As illustrated by figure (11), the onboard devices with I2C signals are controlled by an I2C Bus Switch (PCA9538APW) and the UltraScale FPGA.

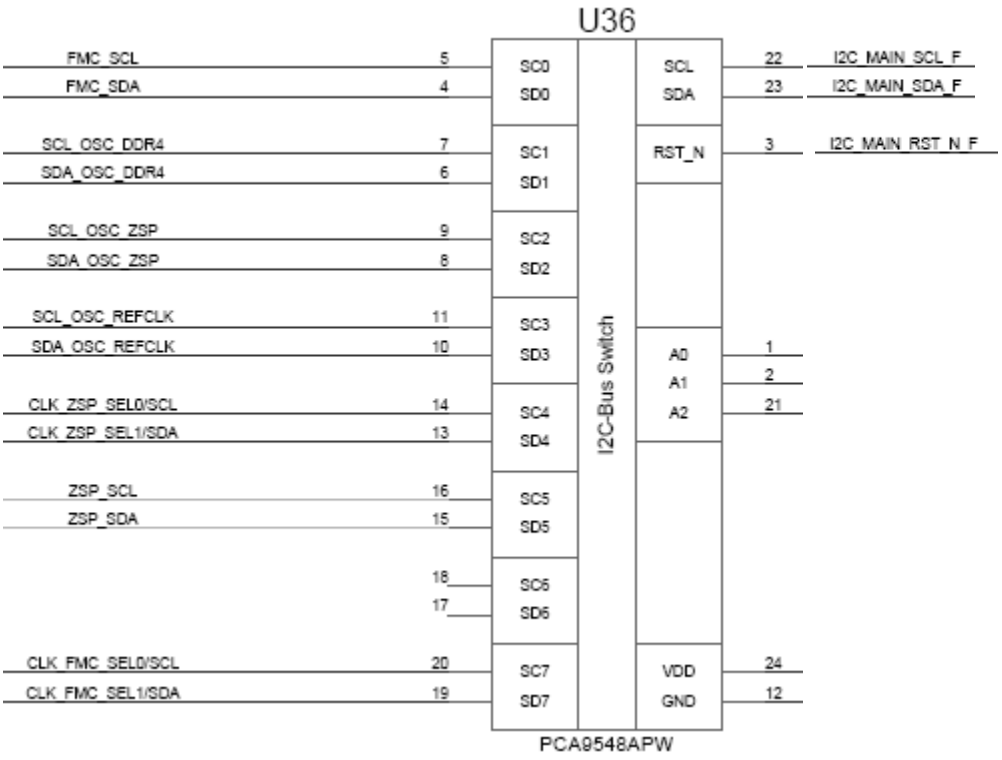


Figure (11): I2C Bus Switch Diagram

Table (14) illustrates FPGA pin assignment for the I2C control.

Signal Name	FPGA Pin #
I2C_MAIN_RST_N_F	AL15
I2C_MAIN_SCL_F	AK13
I2C_MAIN_SDA_F	AK12

Table (14): I2C Bus Switch FPGA Pin Assignment

2.11) Configuration

Xilinx FPGAs are CMOS configurable latch (CCL) based and must be configured at power-up from a non-volatile source. FPGA configuration is traditionally accomplished with a JTAG interface, a microprocessor, or PROMs.

The following configuration options are available for the HTG-K800 platforms:

1) Direct FPGA configuration through the onboard JTAG header (J2) and Xilinx USB programming cable. The J2 header is located at the upper left corner of the HTG-K800 platform.

2) Two onboard Spansion SPI Flash memory components (U30 and U31 with part number S25FL512SAGMFIR). Xilinx XAPP1233 provides details of indirect programming of SPI flash components.

   http://www.xilinx.com/support/documentation/application_notes/xapp1233-spi-config-ultrascale.pdf

Upon successful configuration D11 (DONE) LED illuminates and stays ON.

Additional information for programming of Xilinx UltraScale FPGAs is provided by Xilinx UG570 user manual
http://www.xilinx.com/support/documentation/user_guides/ug570-ultrascale-configuration.pdf

Table (15) illustrates FPGA pin assignment for the SPI flash interface.

Signal Name	FPGA Pin #
QSPI0_CS_N	AB9
QSPI0_D0_MOSI	AE11
QSPI0_D1_DIN	AD10
QSPI0_D2	AC9
QSPI0_D3	AD9
QSPI1_CS_N	AW16
QSPI1_D4	AF14
QSPI1_D5	AG14
QSPI1_D6	AE13
QSPI1_D7	AF13
QSPI_CLK	AC11

Table (15): SPI Flash FPGA Pin Assignment

Chapter 3:Mezannine Cards

3.1) Z-RAY High-Speed Serial Bus Modules

The Z-RAY High-Speed Serial Bus provides access to up to 16 GTH (16G) serial transceivers, clock, control signals, and multiple voltage rails for interfacing high-speed / high-performance (20GHz) expansion modules.

HiTech Global offers series of daughter cards which can be used for expanding functionality of the main platform through the Z-RAY interface.

3.1.1) Hybrid Memory Cube (HMC)

Each Hybrid Memory Cube (HMC) provides access to 2GB of serial memory. Modules can be connected in daisy chain for increasing the density.

Image (2): HMC Module

3.1.2) QSFP+ Module

The X2QSFP+ Module provides access to two 40Gbps ports.

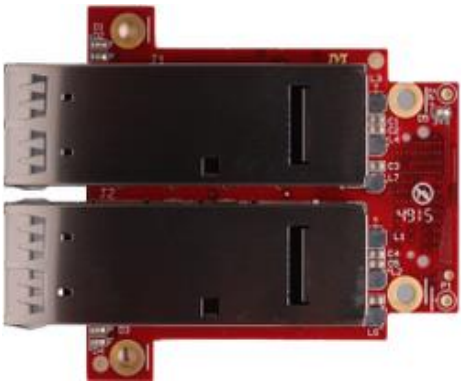


Image (3): QSFP+ Module

3.1.3) X3SFP+ Module

The X3SFP+ Module provides access to three SFP+ ports (3x10G)

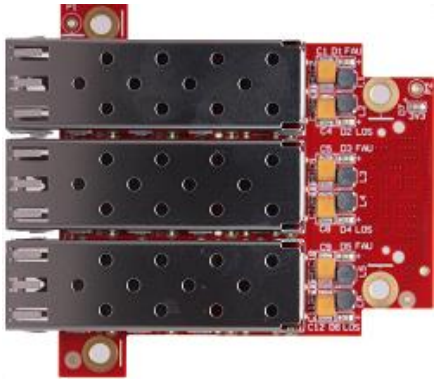
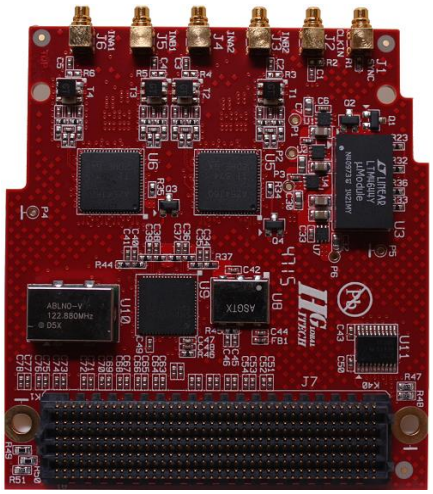


Image (4): X3 SFP+ Module

3.2) FMC Vita 57.x Modules

HiTech Global offers a wide range of FMC daughter cards which can be used for expanding functionality of the main platform.

3.2.1) 4-Channel 16-Bit ADC (Analog to Digital Convertor)



The HTG-ADC16 Module plugs into Vita 57.4 FMC+ HSPC (FMC_B or/and FMC_C on the HTG-830 board) or/and into Vita 57.1 FMC HPC (FMC_A) slots on compliant FPGA carrier boards and provides access to four 16-bit ADC channels.

The module uses two Texas Instruments ADS54J60 ADC devices with JESD204B support.

The **ADS54J60** is a low-power, wide-bandwidth, 16-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). Designed for high signal-to-noise ratio (SNR), the device delivers a noise floor of –159 dBFS/Hz for applications aiming for highest dynamic range over a wide instantaneous bandwidth. The device supports the JESD204B serial interface with data rates up to 10.0 Gbps, supporting two or four lanes per ADC. The buffered

analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. Each ADC channel optionally can be connected to a wideband digital down-converter (DDC) block. The ADS54J60 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption.

More information is available at http://hitechglobal.com/FMCModules/16-bit_AD-DA.htm

3.2.2) 2-Channel 16-Bit DAC (Digital To Analog Convertor)

The HTG-X2DAC16 Module plugs into Vita 57.4 FMC+ HSPC (FMC_B or/and FMC_C on the HTG-830 board) or/and into Vita 57.1 FMC HPC (FMC_A) slots on compliant FPGA carrier boards and provides access to two 16-bit DAC channels.

The module uses one Texas Instruments DAC39J84 DAC device with JESD204B support.

The **DAC39J84** is a low power, 16-bit, quad-channel, 2.8 GSPS digital to analog converter (DAC) with JESD204B interface.Digital data is input to the device through 1, 2, 4 or 8 configurable serial JESD204B lanes running up to 12.5 Gbps with on-chip termination and programmable equalization. The interface allows JESD204B Subclass 1 SYSREF based deterministic latency and full synchronization of multiple devices.

The device includes features that simplify the design of complex transmit architectures. Fully bypassable 2x to 16x digital interpolation filters with over 90 dB of stop-band attenuation simplify the data interface and reconstruction filters. An on-chip 48-bit Numerically Controlled Oscillator (NCO) and independent complex mixers allow flexible and accurate carrier placement.

A high-performance low jitter PLL simplifies clocking of the device without significant impact on the dynamic range. The digital Quadrature Modulator Correction (QMC) and Group Delay Correction (QDC) enable complete IQ compensation for gain, offset, phase, and group delay between channels in direct up-conversion applications. A programmable Power Amplifier (PA) protection mechanism is available to provide PA protection in cases when the abnormal power behavior of the input data is detected.

More information is available at http://hitechglobal.com/FMCModules/16-bit_AD-DA.htm

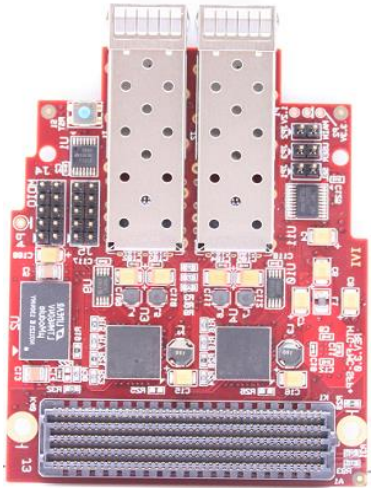
3.2.3) Gearbox / Re-timer QSFP28

The FMC-GB-QSFP28 module is powered by Broadcom 100Gbps Gearbox PHY (BCM82790)that multiplexes and de-multiplexes four 25 Gbps channels to/from ten 10Gbps channels supporting Ethernet and Optical Transport Networking (OTN). The module supports one full-duplex 100Gbe port and complies with 100GBASE-CR4/SR4/LR4 for QSFP28 line-card applications. 100GbE Ethernet support includes CL91 RS FEC as well as CL92 transmit training, and CL73 auto-negotiation.

Test and debug features included in the Gearbox are PRBS pattern generation and checking, eye monitoring on all data receive interfaces, programmable loopbacks, as well as JTAG. Every port on the chip is equipped with an eye monitor. All features are accessed through an IEEE standard MDIO control interface.

More information is available at http://hitechglobal.com/FMCModules/FMC_GB_QSFP28.htm

3.2.4) Dual SFP+ (with external PHY)



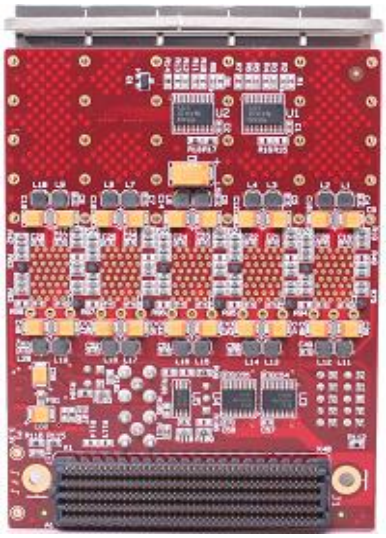
The Dual SFP+ FMC daughter card provides access to two SFP+ ports (10Gbps each) interfacing to total of 8 serial transceivers (XUAI).

The onboard 10Gig PHY device is a physical layer transceiver with an integrated Electronic Dispersion Compensation (EDC) engine - compliant with IEEE802.3aq specifications. The device integrates industry-leading SerDes/PHY technology with low-power EDC engine with up to 5db of margin over the symmetric stress test pulse sensitivity specifications defined in the 10GASE-LRM standard.

Each PHY device provides full PCS, PMA, and XGXS sub-layer functionality through the consolidation of the receiver and transmitter PHY functions on a single chip along with the integration of encode/decode/alignment logic, FIFOs, on-chip clock drivers, multiple loop-back features and PRBS & Ethernet frame generation & verification for both the line side and the system side.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_SFP+.htm

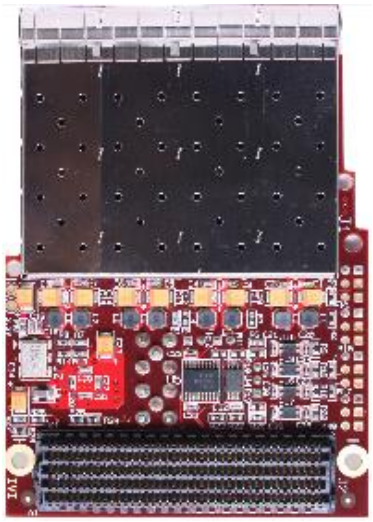
3.2.5) 10-Port SFP+



The X10-SFP+ FMC module is supported by ten SFP/SFP+ ports and high-performance low-jitter Silicon Labs programmable Si570 oscillator with default frequency value of 156.25MHz. The I2C interface between the oscillator and FPGA allows direct control of the SFP/SFP+ ports for wide range of different frequencies. The SFP/SFP+ ports are directly connected to 10 multi-gigabit serial transceivers of the FPGA carrier board (DP0-DP9).

More information is available at http://hitechglobal.com/FMCModules/x10SFP+_FMC_Module.htm

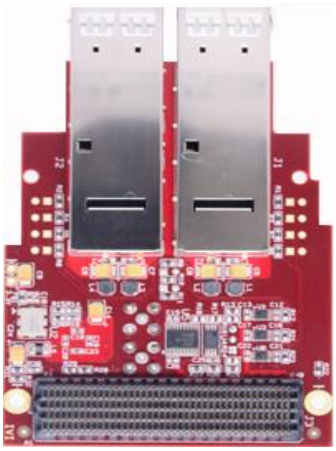
3.2.6) Quad SFP/SFP+



The Quad SFP/SFP+ FMC module is supported by four SFP/SFP+ ports and high-performance low-jitter Silicon Labs programmable clock (default = 156.25MHz). The I2C interface between the oscillator and FPGA allows direct control of the SFP/SFP+ ports for wide range of different frequencies. The SFP/SFP+ ports are directly connected to four multi-gigabit serial transceivers of the FPGA carrier board.

More information is available at http://hitechglobal.com/FMCModules/FMC_4SFP+_Module.htm

3.2.7) Dual QSFP+



The Dual QSFP/QSFP+ FMC module is supported by two QSFP/QSFP+ ports and high-performance low-jitter Silicon Labs programmable clock (default = 156.25MHz). The I2C interface between the oscillator and FPGA allows direct control of the SFP/SFP+ ports for wide range of different frequencies. The QSFP/QSFP+ ports are directly connected to eight multi-gigabit serial transceivers of the FPGA carrier board.

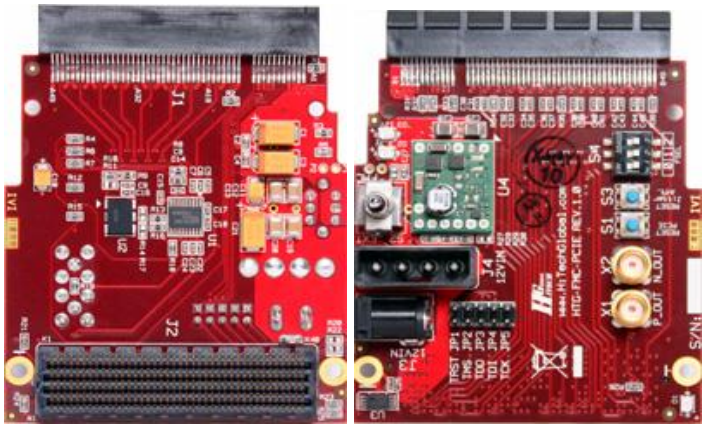
More information is available at http://hitechglobal.com/FMCModules/FMC_2QSFP+.htm

3.2.8) QSFP/QSFP+ /SFP+

The CPRI/OBSAI FMC module is supported by one QSFP+ and two SFP+ connectors. The required 122.88MHz and 153.60MHz crystal oscillators for CPRI/OBSAI standards are available on the module. Different gigabit standards can also be supported by changing crystal value (i.e. 10G and 40G Ethernet)

More information is available at http://hitechglobal.com/FMCModules/FMC_QSFP+.htm

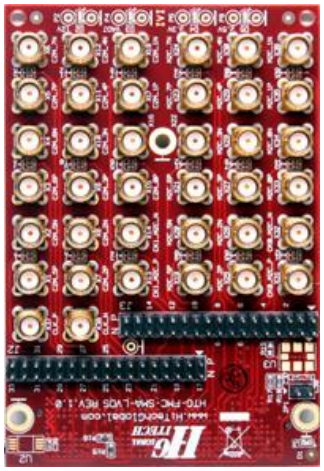
3.2.9) PCI Express Root Complex



The PCI Express Root FMC daughter card provides access to 8 lanes of PCI Express Gen 1 and port. The module is supported by 100MHz and 250MHz low-jitter clocks.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_PCIExpress.htm

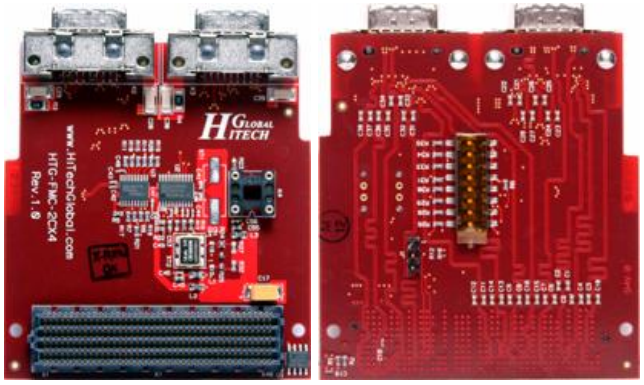
3.2.10) 8-port SMA/LVDS



The FMC SMA/LVDS (HTG-FMC-SMA-LVDS) is a single-size FPGA Mezzanine Connector (FMC) daughter card with support for 8 SMA ports through 32 SMA connectors and 33 pairs of LVDS signals through standard pin headers.

More information is available at http://hitechglobal.com/FMCModules/FMC_SMA_LVDS.htm

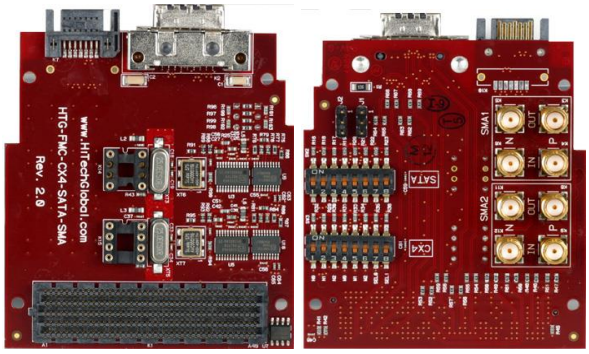
3.2.11) Dual CX4



The dual CX4 FMC daughter card provides access to two CX4 ports (10Gbps) interfacing to total of 8 serial transceivers (XUAI).

More information is available at http://www.hitechglobal.com/FMCModules/FMC_Dual_CX4.htm

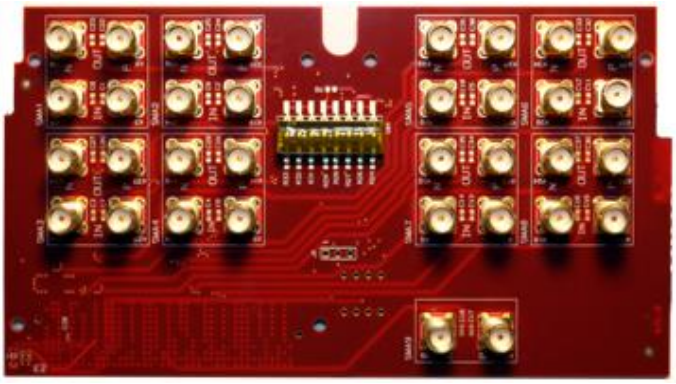
3.2.12) CX4/SATA/SMA Serial Connectivity



The Serial Connectivity FMC daughter card provides access to one CX4, two SATA, and two SMA ports (interfacing to total of 8 serial transceivers). Each port has its own on-board dedicated clock for maximum flexibility and ease of use.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_CX4-SMA-SATA.htm

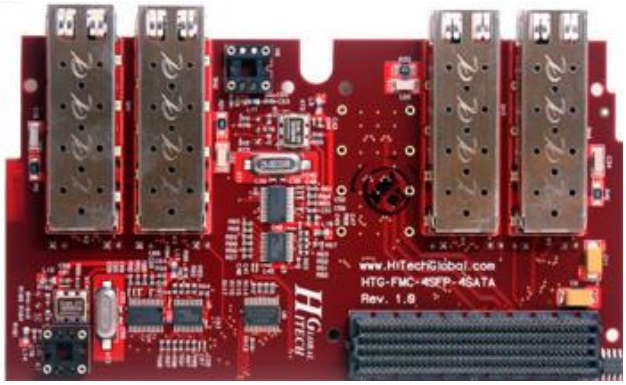
3.2.13) 8-Port SMA



The 8-Port SMA FMC daughter card provides access to 32 SMA connecters providing access to 8 Serial Transceivers. The module is supported by on-board and external clocks.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_SMA.htm

3.2.14) Quad SFP/SATA



The Quad SFP/SATA FMC daughter card provides access to four SFP and four SATA connectors. Each interface is supported by its own independent clock.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_x4SFP_x4SATA.htm

3.2.15) Quad RJ45 Ethernet

The HTG-4RJ45 FMC module provides access to four RJ45 connectors through Marvel Alaska® Quad family of single-chip device (88E1240-A0-BAM1C000) with four independent Gigabit Ethernet transceivers. Each transceiver performs all the physical layer functions for 100BASE-TX and 1000BASE-T full or half-duplex Ethernet on CAT 5 twisted pair cable, and 10BASET full or half-duplex Ethernet on CAT 3, 4, and 5 cable.

The Alaska 88E1240 device supports the Serial Gigabit Media Independent Interface (SGMII) for direct connection to a MAC/Switch port. The 88E1240 device is fully compliant with the IEEE 802.3 standard. The 88E1240 device includes the PMD, PMA, and PCS sub layers. The 88E1240 device performs PAM5, 8B/10B, 4B/5B, MLT-3, NRZI, and Manchester encoding/decoding, digital clock/data recovery, stream cipher scrambling/ descrambling, digital adaptive equalization for the receiver data path as well as digital filtering for pulse-shaping for the line transmitter, and Auto-Negotiation and management functions.

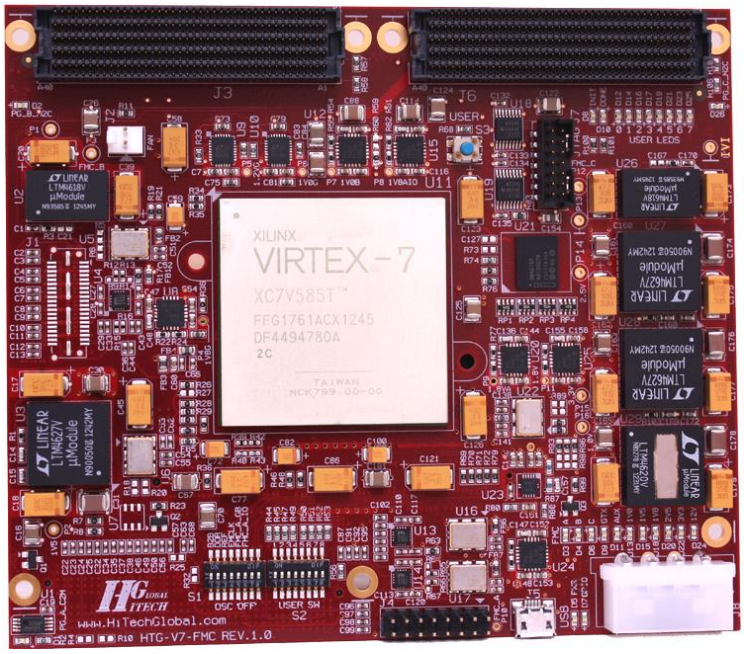
More information is available at http://hitechglobal.com/FMCModules/FMC_RJ45.htm

3.2.16) 42-Channel RS485/RS422

The RS485/RS422 FMC module is powered by Linear Tech LTC2854 and provides 42 differential channels using 20Mb RS485/RS422 transceivers.

More information is available at http://hitechglobal.com/FMCModules/FMC_RS485.htm

3.2.17) FPGA Gate Expansion



Populated with one Xilinx Virtex UltraScaleV2000T, X690T, or V585T FPGA and supported by three High Pin Count (HPC) FMC connectors, UART/USB port, DDR3 SODIMM (up to 8 GB), Flash, and additional MGT based expansion connectors, the HTG-777 card is ideal for any FPGA development requiring large logic, memory, and I/O bandwidth. The V7-FMC is designed for stand-alone, stackable, or carrier-mating operation.

Stand Alone Mode - In this mode the card is self-contained and provides the smallest form factor (5 1/2 " x 4 1/2") for large scale FPGA development, ASIC prototyping, or emulation.

Stackable Mode - In this mode multiple HTG-777 modules can be stacked up either through the onboard Samtec QSE/QTE (MGTs only) or two FMC connectors (LVDS I/Os and MGTs). Supported by separate power supplies, in this mode multiple modules can be connected to each other in daisy chain fashion as well. The provided flexibility allows many different mix and match combinations.

FMC Mode - In this mode the card mates with a FMC based FPGA carrier card and provides additional logic density to the system.

Technical Support:

Technical support can be provided by contacting support@HiTechGlobal.com Support requests are responded in less than 24 hours.

Sales Support:

Sales support can be provided by contacting info@HiTechGlobal.com or +1 408 781-7778 (8:00 AM – 6:00 PM Pacific Standard Time)