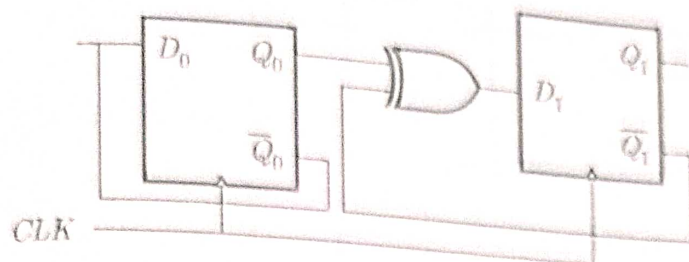


MCQ 5.1.19

Consider the following circuit

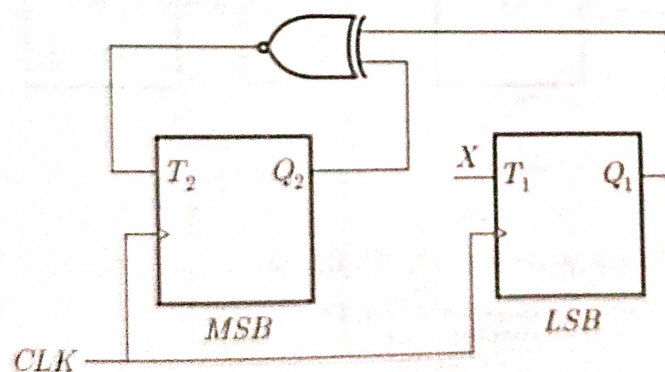


The flip-flops are positive edge triggered D -FFs. Each state is designated as a two bit string $Q_0 Q_1$. Let the initial state be 00. The state transition sequence is

- (A) $00 \rightarrow 11 \rightarrow 01$
 (B) $00 \rightarrow 11$
 (C) $00 \rightarrow 10 \rightarrow 01 \rightarrow 11$
 (D) $00 \rightarrow 11 \rightarrow 01 \rightarrow 10$

MCQ 5.1.20

Consider the partial implementation of a 2-bit counter using T flip-flop following the sequence 0-2-3-1-0 as shown below.

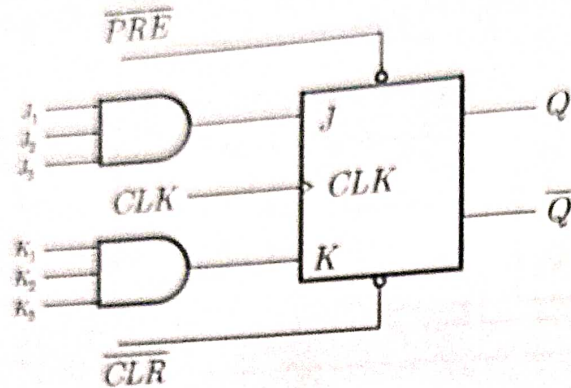


- To complete
- (A) $\overline{Q_2}$
- (B) $Q_2 + Q_1$
- (C) $\overline{(Q_1 \oplus Q_2)}$
- (D) $Q_1 \oplus Q_2$

MCQ 5.1.21

The following serial data are applied to the flip-flop through the AND gates as shown in figure.

$J_1 : 1010011, J_2 : 0111010, J_3 : 1111000$
 $K_1 : 0001110, K_2 : 1101100, K_3 : 1010101$

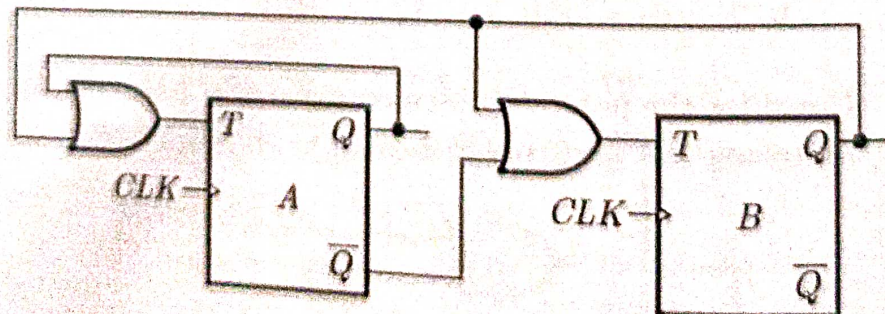


There is one clock pulse for each bit time. Q is initially 0 and \overline{PRE} and \overline{CLR} are high. If leftmost bits are applied first then output Q is

- (A) 0000111
- (B) 0011000
- (C) 0101000
- (D) 1010101

MCQ 5.1.22

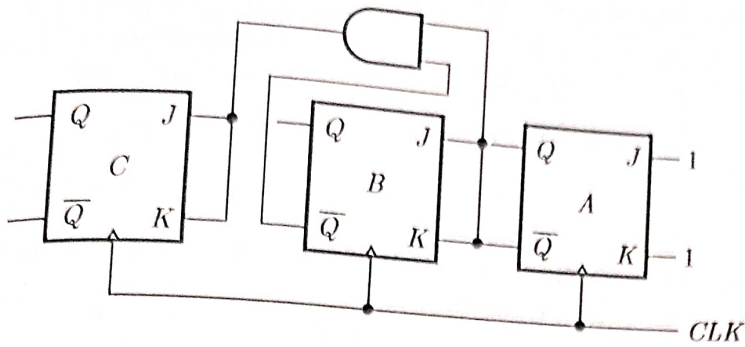
The circuit shown in figure below is



- (A) a MOD-2 counter
- (B) a MOD-3 counter
- (C) generate sequence 00, 10, 01, 00 ...
- (D) generate sequence 00, 10, 00, 10, 00 ...

MCQ 5.1.23

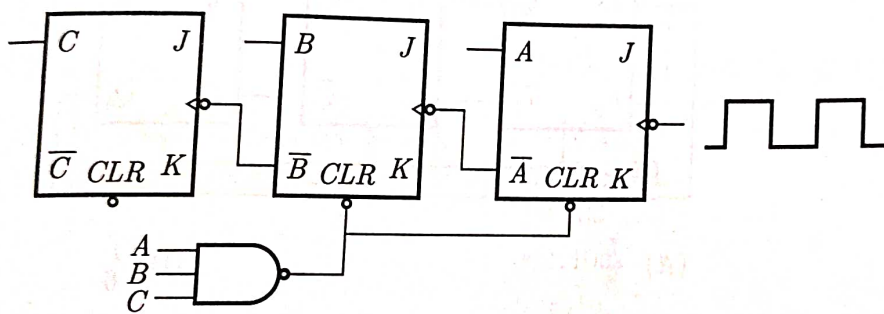
The counter shown in figure below is a



- (A) MOD-8 up counter
- (B) MOD-8 down counter
- (C) MOD-6 up counter
- (D) MOD-6 down counter

MCQ 5.1.24

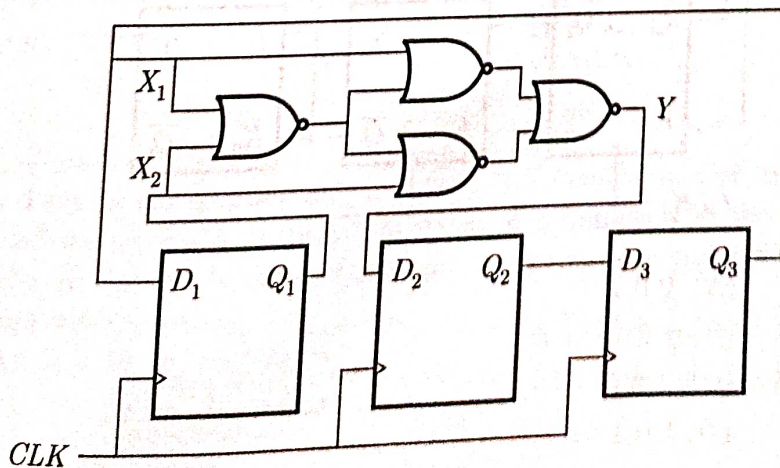
The counter shown in figure below counts from



- (A) 0 0 0 to 1 1 1
- (B) 1 1 1 to 0 0 0
- (C) 1 0 0 to 0 0 0
- (D) 0 0 0 to 1 0 0

Common Data For Q. 25 and 26 :

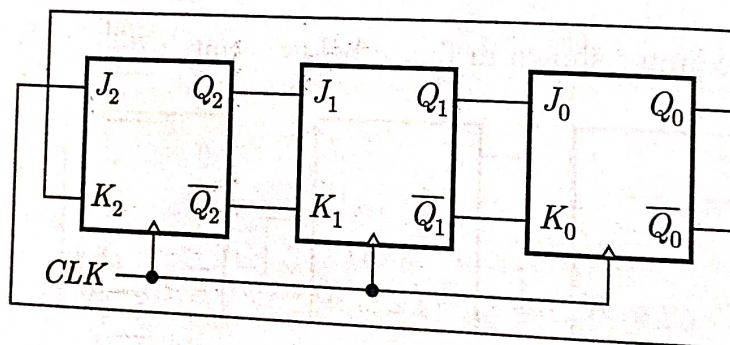
Consider the circuit shown in following figure.



- MCQ 5.1.25** The correct input output relationship between Y and (X_1, X_2) is
 (A) $Y = X_1 + X_2$
 (B) $Y = X_1 X_2$
 (C) $Y = X_1 \oplus X_2$
 (D) $Y = \overline{X_1 \oplus X_2}$

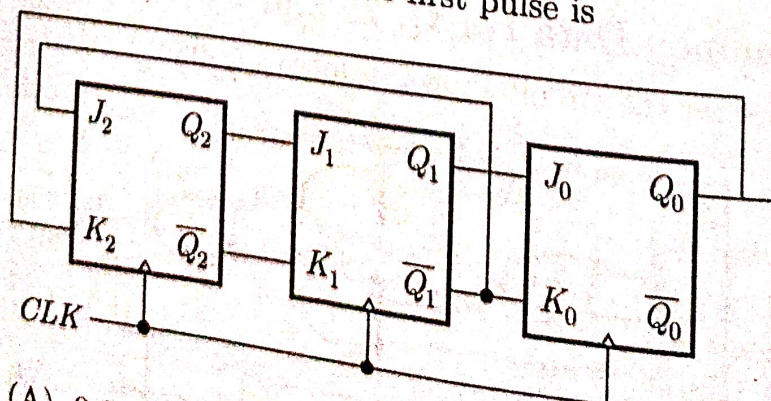
- MCQ 5.1.26** The D flip-flop are initialized to $Q_1 Q_2 Q_3 = 000$. After 1 clock cycle, $Q_1 Q_2 Q_3$ is equal to
 (A) 011 (B) 010
 (C) 100 (D) 101

- MCQ 5.1.27** The three-stage Johnson counter as shown in figure below is clocked at a constant frequency of f_c from the starting state of $Q_2 Q_1 Q_0 = 101$. The frequency of output $Q_2 Q_1 Q_0$ will be



- (A) $\frac{f_c}{8}$ (B) $\frac{f_c}{6}$
 (C) $\frac{f_c}{3}$ (D) $\frac{f_c}{2}$

- MCQ 5.1.28** The counter shown in the figure below has initially $Q_2 Q_1 Q_0 = 000$. The status of $Q_2 Q_1 Q_0$ after the first pulse is



- (A) 001
 (B) 010
 (C) 100
 (D) 101