8x8 Signed Serial-Parallel Multiplier Using Verilog and FPGA

Team Members

- Aly Youssef
- Omar Beheiry
- Omar Khalil ElSawy

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1. Introduction

Multiplication is a core operation in digital signal processing, computer arithmetic, and embedded systems. This project focuses on implementing an 8x8 signed Serial-Parallel Multiplier (SPM), which combines efficient resource usage with moderate speed. The SPM receives the multiplier serially and the multiplicand in parallel. The product is shown on a 7-segment display in decimal form, with user controls for navigation and reset.

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2. Project Objectives

- Implement an 8x8 signed Serial-Parallel Multiplier in Verilog.
- Simulate components in Logisim Evolution.
- Display the signed result using four 7-segment displays.
- Control the process using pushbuttons (BTNL, BTNR, BTNC).
- Deploy the design on a Basys 3 board with an Artix-7 FPGA.
- Document and manage the project using GitHub.

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3. System Architecture

Block Diagram Overview

- **Input Interface:** 16 switches (SW15-SW0) for multiplicand and multiplier.
- **SPM Module:** Handles signed multiplication using serial input.
- **Control Unit:** Manages the state machine, synchronization, and LED signaling.
- **7-Segment Driver:** Converts binary product to decimal and displays it.
- **Scroll Controller:** Uses BTNL and BTNR for digit scrolling.
- **Start Control:** Uses BTNC to trigger computation.
- **LED Output:** LD0 indicates when the computation is complete.

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4. Design Methodology

Signed Representation

- 2’s complement is used for representing signed 8-bit inputs and 16-bit outputs.

Serial-Parallel Multiplication

- The multiplicand is loaded in parallel.
- The multiplier bits are processed serially from LSB to MSB.
- Each ‘1’ bit triggers a shift-add operation.
- Sign extension is handled to preserve signed multiplication behavior.

Decimal Conversion for Display

- A binary-to-decimal conversion module (Double Dabble algorithm) is used.

- The product is stored in a shift register.
- Results are paginated using a scroll controller.

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5. Verilog Implementation

Modules

- `CSFA.v`: Implements the Carry-Save Full Adder which the multiplier is based on.
- `DFF.v`: Implements the D Flip-Flops which the registers are based on.
- `SPM.v`: Implements the core Serial-Parallel multiplier.
- `tcmp.v`: Gets the two's complement of a number.
- `SixteenBitShiftRightReg.v`: Used in the SPM module.
- `UniversalReg.v`: Also used in the SPM module.
- `binToBCD.v`: Converts binary to 7-segment signals.
- `display_controller.v`: Handles digit navigation.
- `top_module.v`: Integrates all components and connects to board I/O.

6. FPGA Implementation

I/O Mapping Summary

Input/Output	Board Pins
SW0–SW7	Multiplier
SW8–SW15	Multiplicand
BTNC	Start signal
BTNL / BTNR	Scroll digits

LD0	Completion flag
7-Segment	Output display

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7. Validation and Testing

Multiplier	Multiplicand	Expected Product	Display Output
12	-3	-36	-036
-15	-2	30	030
127	1	127	127
-128	1	-128	-128

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8. Conclusion

This project successfully implemented an 8x8 signed Serial-Parallel Multiplier using Verilog and deployed it on a Basys 3 FPGA. The design is modular, extensible, and demonstrates solid understanding of digital design, control logic, and FPGA workflows.