# Graduation Projects Booklet

## 2022 / 2023

*Department of Electronics and Electrical*
*Communications Engineering*
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*Cairo University*

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| Project Code | Project Title |
|---|---|
| 1 | Safety Arm Set |


**Abstract**

Disabled people face many obstaclesin their daily life as for the deaf and mute people, they are facing the problem
of communication with the outside world. Most of the people worldwide have very poor knowledge of the sign
language. So, with our duty to the society as communication engineers specialized in the embedded systems, we
found that implementing the Safety Arm Set would be helpful in bypassing the communication problem.
In addition, disabled people may have difficulties expressing and explaining their feelings/problems in case of
injuries or illness and may even fail to ask for immediate help in case of emergencies which require support from
other people or calling the ambulance. The Safety Arm Set comes in handy during these situations, as it provides
a healthcare monitoring system that also automatically reacts when needed.



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| **Funding Source** | N/A |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 2 | The Design of a Single Inductor Multiple Output (SIMO) DC-DC Converter IC (SIMO) for System-On-Chips (SOCS) |


**Abstract**

Power Management is how we deliver different power requirements from a battery to the different building blocks of a System-On-Chip (SOC). With more integration of different systems on a single SOC, the requirements of power management are tough and the need for high efficiency is mandatory. As a result, innovative ideas are needed to build a power management unit for SOCs with multiple outputs. This project aims to implement a complete SIMO DC-DC converter that can provide up to 500 mA of current from a single source to multiple different circuits on an SOC



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| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 3 | 5G Low-PHY Modem |

**Abstract**

The project goal is to implement and test the algorithm and the RTL of some functionalities (e.g. DPD, CFR, FFT, precoding, etc.) of the 5G low-physical layer and Digital Front-End (DFE) on a digital platform (e.g. FPGA).

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| **Sponsers** | Analog Devices |
| **Funding Source** | N/A |
| **Project Budget** | More than 10,000 EGP |

| Project Code | Project Title |
|---|---|
| 4 | Ethernet PHY/MAC Design and Verification |

**Abstract**

The projects aims to design and verify the physical layer and MAC sublayer of Ethernet following IEEE 802.3 standard.

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| **Sponsers** | SIEMENS EDA |
| **Funding Source** | N/A |
| **Project Budget** | More than 10,000 EGP |

| Project Code | Project Title |
|---|---|
| 5 | Automated RTL and Testbenches EDA Tool (ART) |

**Abstract**

ART is an EDA tool that helps in the design and verification of digital ICs.

- Design:

• A Standard library is provided with the most commonly used digital blocks that are completely configurable and synthesizable.
• Finite State Machine can be designed graphically to generate FSM verilog file.
• A top module file is generated given a schematic of sub-modules connection defined in CellView.

- Verification:

• Testbench file is provided given a simple relationship between the inputs and expected output.
• UVM environment is automatically generated by embedding system verilog assertions into UVM templates generated by the tool.
• System verilog assertions are translated from natural language specifications provided in specs documents.

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| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 6 | Automatic Generation of SystemVerilog Assertions for Verification of Safety Mechanisms |


**Abstract**

Safety-Critical Applications are a major focus in the automotive industry. Ensuring that a digital circuit is working and functioning correctly when there is an issue with some nodes in the design is what makes a safe design.

The purpose of this project is to implement different safety mechanisms: parity checking , replication and duplication techniques , and validate the safety mechanisms using System Verilog Assertions and UVM to make sure that target faults are being detected.

The final stage will be to automatically generate assertions to be injected into the safe RTL and to automatically generate testbench to be used in the functional verification.



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| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 7 | Cloud Connected On-chip Analytics Subsystem Design IP |


**Abstract**

design on-chip monitors (analytics subsystem) to capture SoC design self-test data and convert that into Meta data format and store in System memory. The system memory will be cloud connected for descriptive analytics, anomaly detection and adversarial defences.
A Dashboard of the SoC will show different analytics related to components of the SoC design including health and security status of each component.



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| **Sponsers** | Siemens EDA |
| **Funding Source** | Siemens EDA |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 8 | MIPI D-PHY Design and Verification |


**Abstract**

MIPI D-PHY is designed for transmission and reception of video or pixel data for camera and display interfaces.
Our target will be to implement RTL for transmitter D-PHY that supports HS (High Speed) burst, ULPS (Ultra-Low Power State), LPDT (Low Power Data Transmission), Trigger operations. It will be an all-digital implementation with maximum data rate 500 Mbps.
We will also work on developing a verification plan for these requirements then implementing a UVM-PY environment using python and UVM environment using system verilog to test and cover that all the requirements
are functioning properly.



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| **Sponsers** | MIXEL-EGYPT |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 9 | Verification of an openHMC Controller IP |

**Abstract**

In digital IC field, at each stage in the design cycle such as specification, coding, synthesis, manufacturing, the cost of fixing a bug goes up by a factor of 10. The purpose of a verification engineer is to make sure the design accomplishes its task successfully without any bugs. In our project, we start by creating a verification plan after reading the documentations of the design and list all its features and functionality. Perform functional verification by using self-checking testbenches for all different scenarios then report the coverage. The Universal Verification Methodology (UVM) is a standardized methodology for verifying integrated circuit designs. It's derived mainly from the Open Verification Methodology (OVM). We will build a UVM testing environment architecture using SystemVerilog HVL language going through development and debugging phases till we achieve complete coverage. Hence our project is implementing a UVM environment for the OpenHMC (Hybrid Memory Cube) Controller which is a focal point.

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| **Funding Source** | Si-Vision |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 10 | Deep Learning in Covert Communication: Hardware Trojan Detection |

**Abstract**

Data leakage is an important problem in digital information security, and one of the ways that data can be leaked is through hardware trojan technologies. In this project we are going to use deep learning techniques in an attempt to detect possible data leakage done through hardware trojans, and find ways to counteract it.

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| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 11 | A massive MIMO digital beamforming mmWave Transmitter for 5G |


**Abstract**

TX Digital Beamforming: The beamforming system operates to allow the combination of the multiple channels
through different phase shifters to construct a beam that directs a signal within air to create a spatial multiplexing. To create a higher precision with limited phase errors, digital beamforming is chosen to allow
higher precisions and direct conversion of RF to bits. The digital back-end development include a digital phase
shifter followed by an interpolation filter for up sampling followed by digital up conversion (Used only in case
of BP sigma delta) and finally a digital sigma delta



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| **Funding Source** | N/A |
| **Project Budget** | Between 1,000-5,000 EGP |

| Project Code | Project Title |
|---|---|
| 12 | 5G Technology hardware implementation and integration (Digital Design) |

**Abstract**

5g hardware implementation with additional peripherals

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| **Funding Source** | STMicroelectronics |
| **Project Budget** | Between 1,000-5,000 EGP |

| Project Code | Project Title |
|---|---|
| 13 | Low Power NB-LTE Transceiver Design (Downlink Receiver) |

**Abstract**

The target of this project is to implement low power transceiver for the Narrow Band Long Term Evolution (NB-LTE). NB-LTE is a new cellular technology introduced in 3GPP Release 13 to support IOT (Internet-Of-Things) applications.

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| **Funding Source** | Si-Vision company |
| **Project Budget** | More than 10,000 EGP |

| Project Code | Project Title |
|---|---|
| 14 | Secure Patient Data Management Platform using Blockchain Technology |


**Abstract**

Currently, Egypt uses traditional methods to manage patient data management. So, to follow up the digitalization methods developed to
make it easier to deal with and sharing the data between authorities.
We aim to digitalize the data and protect it from tampering or lost, and share it in a secure way without affecting patient's privacy.
And we are willing to implement that project using the blockchain technology, as it can provide the decentralization method to store data, also easily exchange that data and prevent third parties from manipulating that data.



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| **Funding Source** | N/A |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 15 | Master Information Block Decoding for NR Technology |

**Abstract**

The NR modem includes many basic building blocks such as the carrier scanning, cell selection, physical channels decoding, measurements, and more. In this project, although we consider a system on chip solution, we focus on only one building block within the NR modem. For simplicity, we will treat this building block as a complete independent processor despite that fact that it is one gear in the whole NR system. This processor is basically the full decoding chain for the Physical Broadcast Channel (PBCH) that carries the important Master Information Block (MIB)


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| **Sponsers** | STMicroelectronics |
| **Funding Source** | ONE lab |
| **Project Budget** | More than 10,000 EGP |

| Project Code | Project Title |
|---|---|
| 16 | Admission Control and resource allocation in 5G core slicing network |


**Abstract**

The proposed scope is designing an Admission Control (AC) mechanism is needed to decide the acceptance of the slice request, considering the support of QoS requirements as well as the availability of physical resources, and also a Resource Allocation mechanism (RAM) allocates the resources for the request on the network nodes aiming to achieve the minimum the network resource utilization.



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| **Sponsers** | Orange |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 17 | RTL Design and Verification for MIPI D-PHY Transmitter |

**Abstract**

This is a project to design and verify a MIPI D-PHY Transmitter using UVM (Univeral Verification Medothology) with Python and SystemVerilog.

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| **Sponsers** | MIXEL EGYPT |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 18 | Fault Simulation Framework using PyUVM |


**Abstract**

Fault Simulation is a critical topic in the industry of electronics as it helps us expect the behavior of ICs to defects or long-time usage after manufacturing. In this paper we introduce a complete fault simulation solution built using PyUVM that creates an environment capable of injecting the design with faults and monitoring the behavior of the nodes of interest and hence recognize any change to the intended functional behavior of the design under test



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| **Sponsers** | Siemens EDA Digital Industry |
| **Funding Source** | Siemens EDA Digital Industry |
| **Project Budget** | More than 10,000 EGP |

| Project Code | Project Title |
|---|---|
| 19 | Wireless Jamming Detection Using Deep Learning |


**Abstract**

Wireless communication systems are vulnerable to jamming attacks, which can disrupt the reliable transmission of information. This project proposes an approach to detect the presence of jamming attacks at the receiver using deep learning techniques. The project focuses on utilizing architectures such as Long Short-Term Memory (LSTM) and Convolutional Neural Networks (CNN) to accurately identify jamming signals.

The project investigates the performance of the deep learning models under various circumstances. Factors such as the distance between the transmitter/jammer and the receiver, the jamming power, and different types of jamming are considered. By measuring the accuracies of the models in different scenarios, the project aims to provide insights into the robustness of the proposed detection system.

To evaluate the effectiveness of the models, the project compares their performance using both real-world data and generated data. By examining how the models perform on real data, collected from practical jamming scenarios, and generated data, the project aims to assess the models' ability to generalize and adapt to unseen situations.

The results of this project have the potential to contribute to the development of reliable and efficient jamming detection systems for wireless communication networks. By leveraging deep learning architectures and comprehensive evaluations, the proposed approach offers promising prospects for enhancing the security and resilience of wireless systems against jamming attacks.



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| **Sponsers** | Seamless Waves |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 20 | Low Power NB-LTE Transceiver Design |

**Abstract**

The target of this project is to implement low power transceiver for the Narrow Band Long Term Evolution (NB-LTE). NB-LTE is a new cellular technology introduced in 3GPP Release 13 to support IOT (Internet-Of-Things) applications. The main goal is to design the Physical Layer chain of the LTE Rel.14 that targets the NB-LTE.

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| **Sponsers** | Si-Vision |
| **Funding Source** | Si-Vision with tools |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 21 | Implement of CNN for crowd detection through high bandwidth memory interface |


**Abstract**

We aim to design and implement a high-speed memory interface unit that can keep up with the processor's speed and decrease power consumption. To improve the efficiency of crowd surveillance systems, reduce energy consumption, and improve the accuracy of identifying Covid-19 susceptible individuals. We will also explore the potential applications of CNN video processing in various industries, further improving machine technical skills that require video processing.



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| **Sponsers** | N/A |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 22 | Single-Diode Photovoltaic (PV) System Control Design |

**Abstract**

Solar power is a renewable method of generating electricity that converts energy from the sun into usable electrical energy. Solar panels are typically installed on buildings or concentrated in solar farms to facilitate the conversion of the sun's radiation into electrical energy. Photovoltaic (PV) cells within a solar panel convert sunlight into direct current (DC) electricity. Once the conversion process is complete, the electricity can be used, fed into the power grid, or stored in a battery. The optimal utilization of photovoltaic (PV) systems occurs at the maximum power point (MPP), which is influenced by fluctuations in solar irradiation and temperature. To maximize the power output of a photovoltaic (PV) panel, an MPPT (maximum power point tracking) algorithm is utilized. One commonly used MPPT control algorithm is Perturb and Observe (P&O). This algorithm adjusts the operating point of the solar panel based on variations in solar irradiation and temperature. The P&O control algorithm has undergone testing and verification through MATLAB simulations in various case studies that involved different levels of irradiation and temperatures. Moreover, a PV array was implemented and tested to verify the feasibility of the P&O control scheme. The results demonstrate consistency between the simulation and the hardware implementation.

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| **Sponsers** | N/A |
| **Funding Source** | Self-financing |
| **Project Budget** | Between 1,000-5,000 EGP |

| Project Code | Project Title |
|---|---|
| 23 | AUTOSAR CAN Communication Stack |

**Abstract**

Implementation of 4 modules in CAN Stack based on AUTOSAR version 4.3.1:
1) Can Driver (MCAL) : Responsible for configuring the hardware (filtering and accepting messages in memory hardware).
2) CanIF (ECUAL) : Responsible for mapping each L-Pdu to specific mailbox(s).
3) PduR (Service layer) : Responsible for routing the I-Pdus according to their IDs to specific communication modules (Can,LIN, FlexRay,...etc)
4) Comm (Service layer) :
Responsible for packing signals into Pdus and pass them from RTE layer to PduR, and unpacking Pdus into signals bits and pass them to RTE

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| **Sponsers** | Brightskies |
| **Funding Source** | Brightskies |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 24 | Auto Braking System (ABS) designed for collision avoidance through the PreScan simulation program. |

**Abstract**

Collaborated with team colleagues to design and implement the system's hardware and software components, including Discovery Board STM32f429, Raspberry PI 3, MCP2515, MCP2551, Radar Sensors, and Webcam.
Implemented an auto braking system algorithm using C programming language, tested using many PreScan scenarios and Simulink, achieving a high accuracy rate in detecting and responding to potential collisions. The main objective of the algorithm is the instantaneous computation of Time-to-Collision (TTC) for potential collision only from the motion information captured with the vehicle’s Radars.
Improved the algorithm by adding a Lane change feature, depending on the Time-to-Collision factor the system either provides a warning to the driver when there is an imminent collision or takes action autonomously without any driver input (by braking or steering or both).
Designed CAN communication protocol between the discovery board and Raspberry PI using MCP2515 and MCP 2551.
Implemented a camera-based system using the Raspberry Pi and computer vision techniques to detect car owner drowsiness and distraction. The algorithm is developed using OpenCV and Python, which analyzed the driver's facial expressions and head movements to determine their level of alertness and attention.
Identified and resolved several technical challenges during the development process, including improving the system's accuracy and reducing its response time by using RTOS to split the algorithm

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| **Sponsers** | Swift Act |
| **Funding Source** | Swift Act |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 25 | Application Specific Deep Learning Accelerator (ASDLA meister) |


**Abstract**

The project aims to implement digital design of conventional neural network of any architecture automatically using specification from the user


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| **Sponsers** | siemens EDA |
| **Funding Source** | Siemens EDA |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 26 | A Digital Implementation for a ZigBee Transceiver |


**Abstract**

a digital implementation for the PHY Layer in the IEEE Standard for Low-Rate Wireless Networks (802.15.4) which ZigBee standard is based on , thus we are designing a low power ,low rate transmitter and receiver following the requirements provided in the IEEE standard



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| **Funding Source** | Si-Vision (CAD) and FECU (FPGA) |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 27 | RISC-V based Microcontroller for Smart Utility Meters |


**Abstract**

This project focuses on the development of a RISC-V-based microcontroller tailored for smart utility meters. Leveraging the open-source RTL (Register Transfer Level) design of the PULPino microcontroller from the PULP platform, we embarked on enhancing its functionality by integrating additional peripherals and a dedicated hardware accelerator for security purposes. Our hardware accelerator, named AEGIS, is based on the Advanced Encryption Standard (AES), providing robust encryption capabilities to safeguard sensitive data within the utility meters.

To support the expanded functionality, two hard macros memories, one for data and another for instructions, were integrated into the design. The modified RTL underwent a comprehensive ASIC (Application-Specific Integrated Circuit) design flow, encompassing synthesis, placement, and routing stages. This process ensured the efficient transformation of the design into a Gate-Level Description (GDS II) representation, which is the standard format for manufacturing integrated circuits.

To verify the functionality and performance of the designed microcontroller, we implemented it on a Field-Programmable Gate Array (FPGA) platform. The FPGA-based testing allowed us to assess the microcontroller's operation and evaluate its ability to handle the intended tasks effectively. Through extensive testing and analysis, we confirmed the successful integration of the peripherals, the secure hardware accelerator, and the memory modules within the microcontroller.


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| **Funding Source** | EOIP company |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 28 | Smart vertical farming |

**Abstract**

The project is a smart vertical farm that is divided into the following:
1-Vertical farming is the practice of growing crops in vertically stacked layers. It often incorporates controlled-environment agriculture, which aims to
optimize plant growth, and soilless farming techniques such as hydroponics, aquaponics, and aeroponics. Some common choices of structures to
house vertical farming systems include buildings, shipping containers, tunnels, and abandoned mine shafts. As of 2020, there is the equivalent of
about 30 ha (74 acres) of operational vertical farmland in the world.
2- Hydroponics is a type of horticulture and a subset of hydroculture that involves growing plants, usually crops or medicinal plants, without soil, by
using water-based mineral nutrient solutions in aqueous solvents. Terrestrial or aquatic plants may grow with their roots exposed to the nutritious
liquid. In addition, the roots may be mechanically supported by an inert medium such as perlite, gravel, or other substrates
3-- artificial intelligence
We use artificial intelligence techniques to identify plants and their condition, and to notice diseases that may appear in these plants through deep
learning algorithms
.4-- Robots use a robotic arm that is able to move between different floors and carry out traditional farming tasks

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| **Funding Source** | أكاديمية البحث العلمى و التكنولوجيا |
| **Project Budget** | More than 10,000 EGP |

| Project Code | Project Title |
|---|---|
| 29 | Design of Power-Efficient Capacitance to Digital Converter. |


**Abstract**

Capacitance sensors are widely used to measure various physical quantities, including position, pressure, and concentration of certain chemicals. The main task of a capacitive sensor electronic interface is to convert the variable capacitance into an electrical signal (voltage, current, charge), followed by a form of analog-to-digital conversion. Capacitive sensor interfaces have an inherent energy benefit because they do not draw static current, unlike resistive sensors. However, a capacitive-sensor interfacing circuit could dominate system power, and hence there is continuous demand for energy-efficient capacitance-to-digital converter (CDC). In this project, we have utilized zoom architecture with SAR and time domain delta sigma to achieve the best compromise between energy and resolution in delivering an energy-efficient CDC.



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| **Sponsers** | MEMS vision |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 30 | FOTA (Firmware Over The Air) |

**Abstract**

The Project is mainly targeting to upgrade the firmware of remote Hardware ECUs OTA (Over the air). The project is an initialization phase to create a portable, configurable platform to update remotely ECUs with different methods and Hardware.
FOTA is based on the wireless communication between the server which will have the updated firmware and the main control unit which is responsible for updating and installing of the firmware.

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| **Funding Source** | N/A |
| **Project Budget** | Between 1,000-5,000 EGP |

| Project Code | Project Title |
|---|---|
| 31 | Intra-Data Center Coherent Optical Links |


**Abstract**

Data traffic demand increases rapidly inside data centers across the world. The data rates coming to/getting out of one electrical switch chip in a data center can reach up to 25.6 Tb/s. Electrical links can not cope with such data rates for long distances, up to 10 Km, due to the limited bandwidth of copper cables. Therefore, optical communication links using fibers are the viable solution for transferring these huge data rates between switches inside data centers.

Simple intensity modulation optical links are used nowadays inside data centers. Such links can meet the stringent energy requirement while using a simple transmission/reception mechanism. Nevertheless, the future prediction of traffic demands inside data centers indicates that intensity modulation optical links would not be sufficient anymore. More sophisticated, yet efficient, optical links, such as coherent optical links, will be required in near future.

the coherent optical link is already in-use in long-haul communications with distances reaching thousands of kilometers. Therefore, it requires complex signal processing techniques for properly modulating and demodulating the data streams which consume a lot of energy. However, the longest fiber connection inside a data center can rarely reach 10 Km. As a result, the complex signal processing required can be greatly simplified such that it consumes less energy.

This capstone project will focus on simulating and developing simple signal processing techniques to modulate/demodulate coherent optical links inside data centers.


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| **Sponsers** | N/A |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 32 | Advanced Driving Assistance System Using Embedded Linux |

**Abstract**

The project is about creating an Advanced Drivers Assistance System. And our aim is to create the system from the bottom up starting with the operating system which will be built on embedded Linux all the way up to the GUI and the Deep Learning models.

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| **Sponsers** | Valeo |
| **Funding Source** | N/A |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 33 | FPGA implementation of optimized cache memory for coherence |


**Abstract**

Many devices need external memory when they deal with large data. As cache memory is a small and fast memory that stores frequently accessed data so we aim to implement a cache memory to optimize the speed and performance of the system.
In our project we implement two level caches (Level 1 cache has two caches) and apply cache coherence protocols (MSI,MESI) between them as they have significant impact on the performance of the shared -memory multiprocessor, then we do 3 experiments to calculate the total clock cycles taken in read and write operations in case of cache hit or cache miss to make sure that this cache memory achieve the required optimization.
Our proposed system is implemented on ZYBO System on-chip that supports RTL implementation on Artix-7 FPGA.



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| **Sponsers** | N/A |
| **Funding Source** | Supervisor |
| **Project Budget** | Between 1,000-5,000 EGP |

| Project Code | Project Title |
|---|---|
| 34 | Enhancing DDR4 and DDR3 Performance through Charge Cache Technique and matrix multiplication Integration for CNN |


**Abstract**

This project aims to improve the performance of DDR4 and DDR3 memory modules by implementing a charge cache technique and integrating convolutional neural network (CNN) applications.
In this project, we propose a novel approach that leverages a charge cache technique to optimize data access and retrieval from DDR4 and DDR3 memory modules. By strategically managing charge storage and retrieval within the memory cells, we aim to reduce latency and increase the overall data transfer rate.



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| **Sponsers** | N/A |
| **Funding Source** | N/A |
| **Project Budget** | More than 10,000 EGP |

| Project Code | Project Title |
|---|---|
| 35 | Hardware accelerator for deep learning inference |

**Abstract**

Configure a Hw accelerator for DL inference using gemmini framework and do the digital Backend flow ( synthesis and pnr ) to generate the GDSII files ready for silicon implementation.

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| **Sponsers** | Seamless Waves |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |

| Project Code | Project Title |
|---|---|
| 36 | Firmware Over The Air (FOTA) |


**Abstract**

The Project is mainly targeting to upgrade the firmware of remote Hardware ECUs OTA (Over the air). The project is an initialization phase to create a portable, configurable platform to update remotely ECUs with different methods and Hardware.
FOTA, or firmware over-the-air, is a technology that enables the operators of Internet-connected devices to perform upgrades of their firmware versions remotely and seamlessly, without the need of physical intervention into the device. The ability to refresh the operating system of connected assets is essential in keeping the devices secure, adding new functionalities and fixing bugs.



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| **Sponsers** | N/A |
| **Funding Source** | N/A |
| **Project Budget** | Between 5,000-10,000 EGP |

| Project Code | Project Title |
|---|---|
| 37 | A 76-81 GHz FMCW Radar Transceiver |

**Abstract**

In the realm of automotive safety, radar plays a crucial role in collision avoidance and advanced driver assistance systems (ADAS). Radar sensors integrated into vehicles provide essential information about the surrounding environment, including the presence of other vehicles, pedestrians, and obstacles.
In this work, different radar system models are investigated with the design and implementation of the RF front-end of frequency-modulated, continuous-wave (FMCW) radar transceiver (TRX) in 65-nm CMOS technology for a frequency range of 76–81-GHz. Direct conversion architecture is used with different implementations for each block are proposed to compare the different topologies.

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| **Sponsers** | Analog Devices inc. (ADI) |
| **Funding Source** | N/A |
| **Project Budget** | Less than 1,000 EGP |