

Individual Progress Report

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1 Introduction

1.1 Project Overview

Our project is a solar-powered traffic light that will reduce power consumption and nighttime light pollution, in addition to reducing the risks that arise from drivers, cyclists, and pedestrians sharing the intersection. Solar power will be the primary power source, although the device will be grid-connected to ensure functionality at night and during cloudy days. The system will switch autonomously between the sources. Pulse-width modulation (PWM) will be utilized to control the intensity of the LED traffic light modules when the ambient light is sufficiently low. Cyclists and pedestrians will alert the device of their presence by pressing one of two buttons, at which point the traffic lights will cycle until turning red and the bike light will turn green.

1.2 Subsystem Design

The solar-powered traffic light project contains many different subsystems that come together to operate the overall design. These include the power, sensing, control, and traffic light subsystems. Of these, I have primarily worked on the power and sensing subsystems, particularly in the realms of designing circuit portions and selecting components.

1.2.1 Power Subsystem

The power subsystem is vital to the success of our project, thus I have put extensive time into its design. Power conversion, especially that at the output of the solar panel, needs to be fully functional for our project to be completed. I designed a single-ended primary-inductor converter (SEPIC) to accomplish the regulation of our solar output to a smooth 24 V. This will work with other components of the power subsystem, such as the switching network, and of other subsystems to ensure proper operation of our design. Additionally, the switching network provides autonomous switching between grid and solar power sources. This will be controlled by our ATmega328P microcontroller within the control subsystem, which takes power readings from the sensing subsystem. Together, these portion of the power subsystem are a sizable portion of my work thus far and are necessary for the overall functionality of our design.

1.2.2 Sensing Subsystem

In order to create autonomous switching between the power sources, it is necessary to sense the power available by the solar panel. I designed a power monitor featuring the LTC4151-1 chip and a power resistor as a dead load that will dissipate the monitored power. The ATmega328P communicates with this sensor via the I²C protocol. I selected this chip and designed the schematic of this portion of the sensing subsystem.

1.2.3 Control Subsystem

While the control subsystem possesses less room for design than other aspects of the project, I designed the schematic and PCB for the microcontroller (MCU) board. This board will communicate with our sensors and other systems to control each aspect of the device.

1.2.4 Accomplishments

I have been able to design and simulate via LTspice the 24 V SEPIC converter and switching network, design the power monitor, and design and verify the PCB schematics and layouts for the MCU board and our 5

V buck board. Additionally, I have taken part in most design conversations about each subsystem listed above. As of March 30, I have tested and verified the functionality of the switching network and helped Bowen debug the 24 V SEPIC converter.

1.2.5 Current Work

Currently, I am working on debugging the previous version of the power board and putting together the physical design based on what the Machine Shop built.

1.2.6 Future Work

Our newest iteration of the power, light, and buck boards will arrive around April 11. At that point, I plan to solder and test the switching network (power board) and buck board to ensure their functionality. Once this is completed, I will help to assemble the whole enclosure and test the functionality of the device as a whole.

If there are any flaws or errors within the most recent PCBs, I, along with Bowen and Richard, will piece together our components and attempt to overcome them in the final assembly of our device.

2 Design

2.1 Power Consumption Estimate

Before proceeding with the design of various portions of the system, it was necessary to estimate the worst-case power consumption. The red, yellow, and green LED modules draw 4.4 W, 4.5 W, and 6.6 W, respectively.[1] Accounting for the power consumption of the LED traffic light modules, a conservative 3 W for the ATmega328P and sensors, and a derating factor of 1.2 due to potential losses, a worst-case scenario with all lights on is approximately 20 W of power drawn. The 100 W solar panel in the Senior Design Lab is more than sufficient and can be partially covered to simulate lower power conditions.

2.2 SEPIC Converter

The entire system will be supplied by 24 V, whether from the grid via AC-DC conversion or from a solar panel via DC-DC conversion. In order to attain the desired 24 V from the solar panel, a step-up converter is required. The nominal operating voltage of the solar panel is 18 V, so the converter must be able to perform step-up conversion. However, I decided to design the converter for up to 25 V input based on the higher no-load voltage of the solar panel. Additionally, based on the 20 W power consumption estimate, I set the power rating of the converter to 40 W to provide a sufficient margin for any components that may need to be added later. Thus, the converter requirements can be seen in 1. A suitable converter for step-up and step-down conversion is the SEPIC converter, which contains more components than a standard buck-boost converter but provides a smooth non-polarized output voltage. A simple sketch of a SEPIC converter can be seen in Figure 1. The design of a SEPIC converter is relatively simple following the general instructions of a controller's datasheet. I chose the LT3757A chip due to its wide input voltage range and closed-loop control of the output voltage.[2]

Table 1: SEPIC converter requirements

| | |
|---------------|-------|
| $V_{in,min}$ | 12 V |
| $V_{in,max}$ | 25 V |
| V_{out} | 24 V |
| $I_{out,max}$ | 1.7 A |

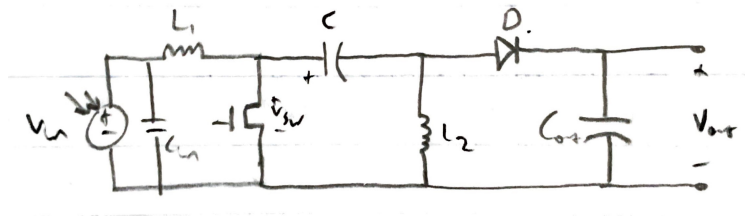


Figure 1: SEPIC converter diagram

Following the instructions located within the datasheet for the LT3757A chip, all necessary equations to select parts are easily accessible. All calculations can be seen in Figure 2. After selecting parts based on these calculations, I simulated the design in LTspice and arrived at a design that maintained an output voltage of 24 V with minimal ripple. The schematic and waveforms for this simulation can be seen in Figures 3 and 4, respectively.

$$\begin{aligned}
 12 \leq V_{in} \leq 25 \text{ V} \quad V_{out} &= 24 \text{ V} \quad I_{out} \leq 1.7 \text{ A} \\
 D_{max} &= \frac{24 \times 0.2}{12 \times 24 \times 10^{-7}} = 0.673 \\
 I_{L1, max} = I_{L2, max} = I_{q, max} &= \frac{D_{max}}{1 - D_{max}} = 1.7 \left(\frac{0.673}{1 - 0.673} \right) = 3.5 \text{ A} \\
 I_{L2, max} &= I_{out, max} = 1.7 \text{ A} \\
 R_T &= 41.2 \text{ k}\Omega \\
 I_{sq, max} &= I_{L1, max} + I_{L2, max} = 3.5 + 1.7 = 5.2 \text{ A} \\
 \text{Let } \chi &= 0.2 \Rightarrow 20\% \text{ ripple current} \\
 I_{sq, peak} &= (1 + \frac{\chi}{2}) I_{sq, max} = 5.72 \text{ A} \\
 \Delta I_{sq} &= \chi I_{sq, max} = 1.04 \text{ A} \\
 \Delta I_{L1} = \Delta I_{L2} &= 0.5 \Delta I_{sq} = 0.52 \text{ A} \\
 L_1 = L_2 &= \frac{V_{in, min}}{0.5 \Delta I_{sq}} D_{max} = \frac{12}{0.5(1.04)(3000)} (0.673) = 51.769 \mu\text{H} \\
 \text{or if coupled: } L &= \frac{V_{in, min}}{0.5 \Delta I_{sq}} D_{max} = \frac{12}{0.5(1.04)(3000)} (0.673) = 25.885 \mu\text{H} \\
 I_{L1, peak} = I_{L1, max} + 0.5 \Delta I_{L1} &= 3.76 \text{ A} \quad I_{L2, peak} = I_{L2, max} + 0.5 \Delta I_{L2} = 1.96 \text{ A} \\
 R_{sense} &= \frac{80 \text{ mV}}{I_{sq, peak}} = \frac{0.08}{5.72} = 0.013986 = 13.99 \text{ m}\Omega \approx 14 \text{ m}\Omega \\
 V_{sq, rated} &= 24 \times 25 + 10 \approx 60 \text{ V} \quad I_{sq, rated} \geq 1.2(5.2) \approx 7 \text{ A} \\
 \text{Minimize } R_{DS(on)} \text{ } C_{iss} \\
 I_{sq, peak} &= (1 + \frac{0.2}{2}) I_{sq, max} = 5.72 \text{ A} \quad V_{ds, rated} = 24 \times 1.5 + 10 = 60 \text{ V} \\
 V_{GDC} > V_{sq, max} &= 25 \text{ V} \quad I_{avg, GDC} > I_{sq, peak} \sqrt{\frac{V_{in} - V_{ds}}{V_{ds}}} = 1.7 \sqrt{\frac{24 - 60}{60}} = 2.439 \text{ A} \\
 ESR_{GDC} &\leq \frac{0.01 V_{ds}}{I_{sq, peak}} = \frac{0.01(24)}{5.72} = 0.04196 = 41.958 \text{ m}\Omega \\
 C_{out} &\geq \frac{I_{sq, max}}{0.01 V_{out} f} = 23.61 \mu\text{F} \quad I_{avg, out} > I_{sq, max} \sqrt{\frac{D_{max}}{1 - D_{max}}} = 2.439 \text{ A}
 \end{aligned}$$

Figure 2: SEPIC converter calculations

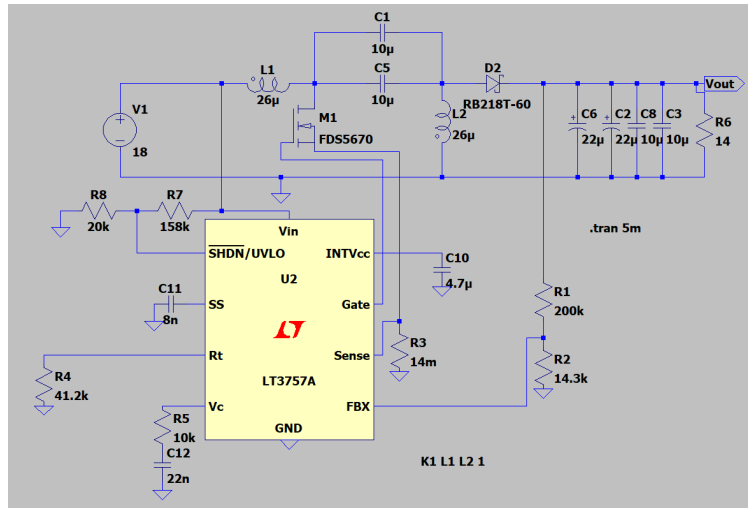


Figure 3: SEPIC converter schematic

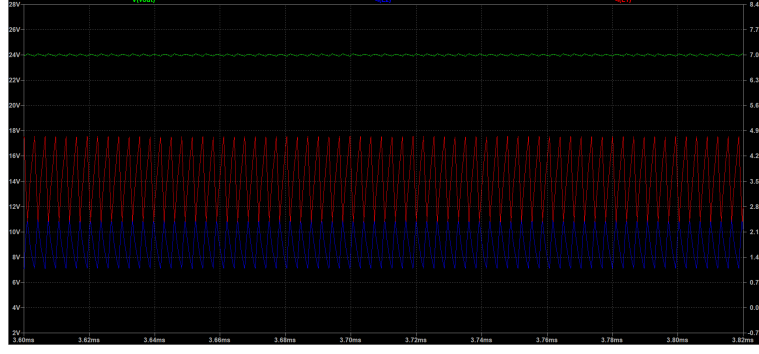


Figure 4: SEPIC converter simulation - Output voltage (green), L_1 current (red), L_2 current (blue)

2.3 Switching Network

When solar power drops below a given power threshold, the system will transfer to grid power. Once the solar panel is able to exceed this power threshold, the system will switch back to solar power. An autonomous switching network with two sources as inputs, solar power and grid power, is able to accommodate this functionality. This portion of the power subsystem takes inputs from the ATmega328P microcontroller and switches between the power sources without allowing reverse current to flow between them. To accomplish this, I initially intended to utilize either two LTC4357 chips or two LTC4359 chips. A pair of either chips drives a pair of MOSFETs with the intent of paralleling power supplies, while the LTC4359 does so while protecting each input against reverse currents from the other.[3][4] An LTspice schematic and corresponding simulation can be seen in Figures 5 and 6, respectively.

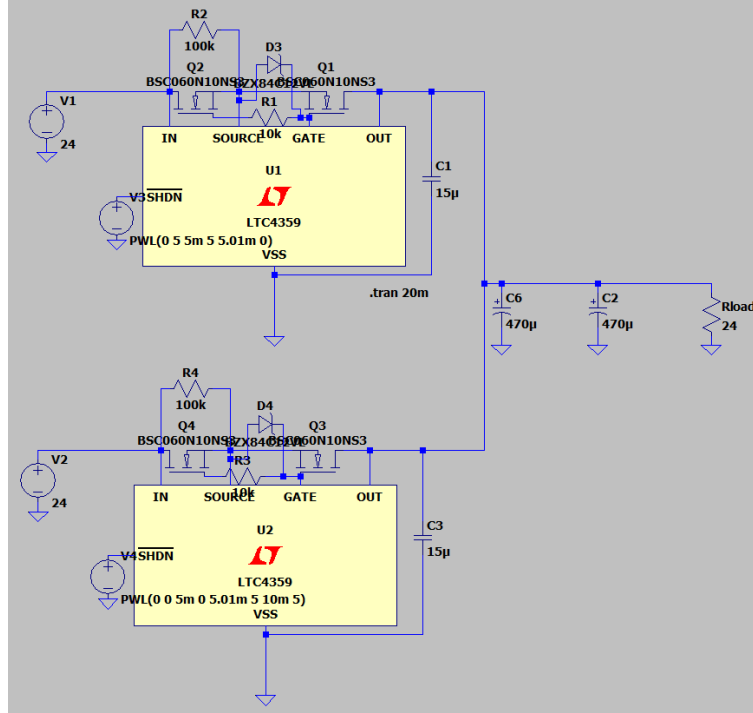


Figure 5: Initial switching network schematic



Figure 6: Initial switching network simulation

However, the output voltage dips significantly while switching between sources because the LTC4359 chip is not intended to be turned off to provide exact control of the current source being utilized. Thus, I decided to move in a different direction with the switching network design. Rather than relying on chips that are not controllable, it seemed intuitive to connect two MOSFETs with opposite orientation to each of the power sources. The opposite orientation ensure that when the switches are off, the body diodes will not allow any current to pass through back to the opposite source. In order to drive these MOSFETs, a high-side gate driver is required. This is due to the fact that the source pin of each MOSFET is not connected to ground, but is instead floating until it is turned on and connected to the corresponding source. I selected the LT1161 quad high-side gate driver, which drives four high-side MOSFETs by sending a signal to each gate that is 12 V greater than the input voltage. Additionally, it takes four inputs to drive these MOSFETs, which makes it easily controllable by our ATmega328P.[5] An LTspice schematic and simulation can be seen in Figures 7 and 8, respectively.

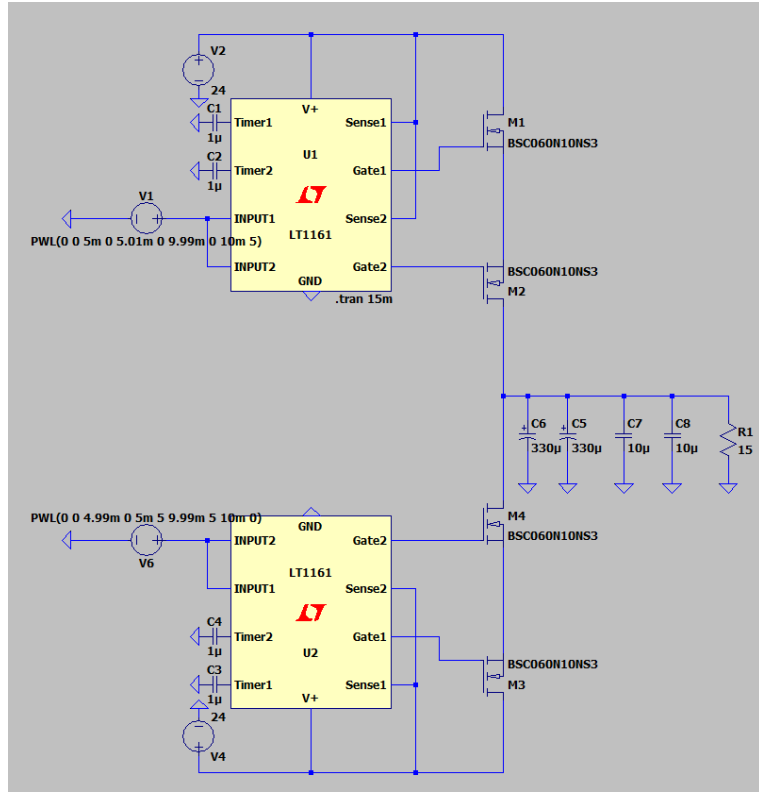


Figure 7: Final switching network schematic

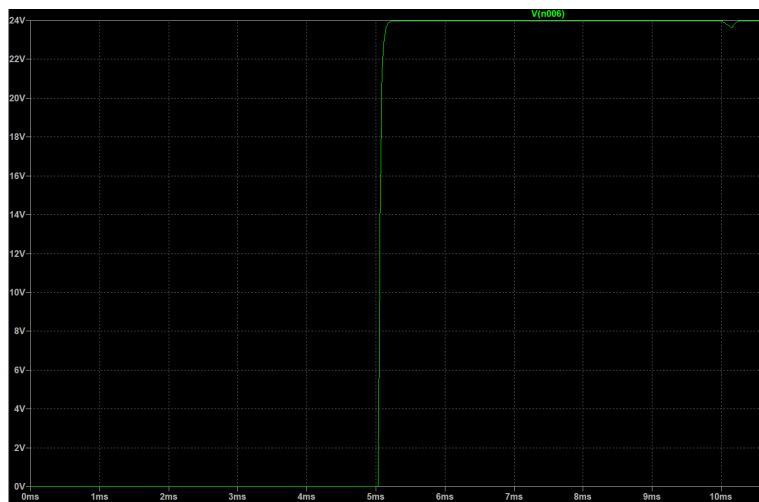


Figure 8: Final switching network simulation

2.4 Power Monitor

In order to detect whether the solar panel is able to supply power at or above the aforementioned threshold, this portion of the sensing subsystem must periodically provide the microcontroller with data regarding the voltage available and current through a sense resistor. I came across and selected the LTC4151-1 chip, which is a high-side power monitor that possesses a wide range of operating voltages and communicates with the ATmega328P via the I²C protocol.[6] The circuit diagram for the power monitor can be seen in Figure 9, which also contains two MOCD207M optoisolators to ensure signal integrity along the I²C SCL and SDA lines. It is key to note that a 33 Ω power resistor, with a necessary heat sink, is connected at the output of the 24 V SEPIC converter to detect the power available from the solar panel. A MOSFET controlled by the ATmega328P will connect this resistor momentarily to make a power reading when the system is currently operating on grid power, otherwise it will remain disconnected to avoid interference with the rest of the system.

2.5 MCU Board Design

I worked on the design of our MCU board, which contains the ATmega328P and necessary components, a 24 V to 5 V isolated DC-DC converter, and pin headers for 24 V input, 5 V output, and connection to sensors and components that will be controlled by the microcontroller. The circuit schematic, PCB layout, and 3D PCB layout can be seen in Figures 10, 11, and 12, respectively.

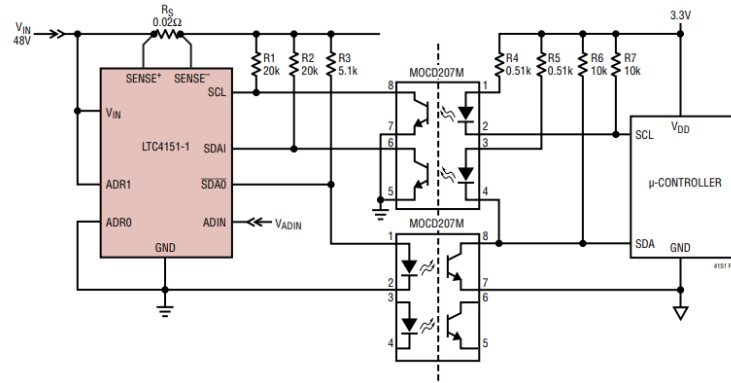


Figure 9: Power monitor schematic

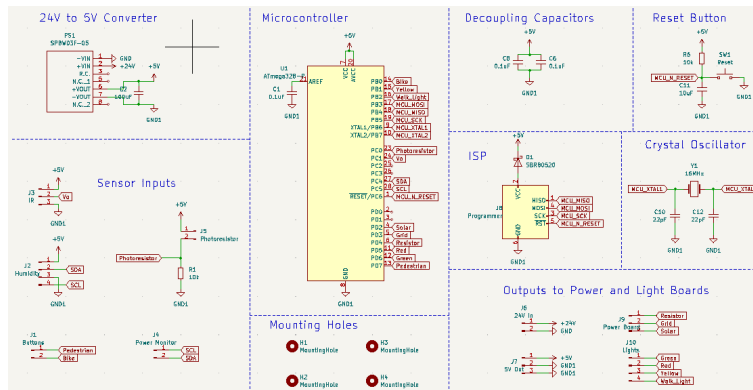


Figure 10: MCU board schematic

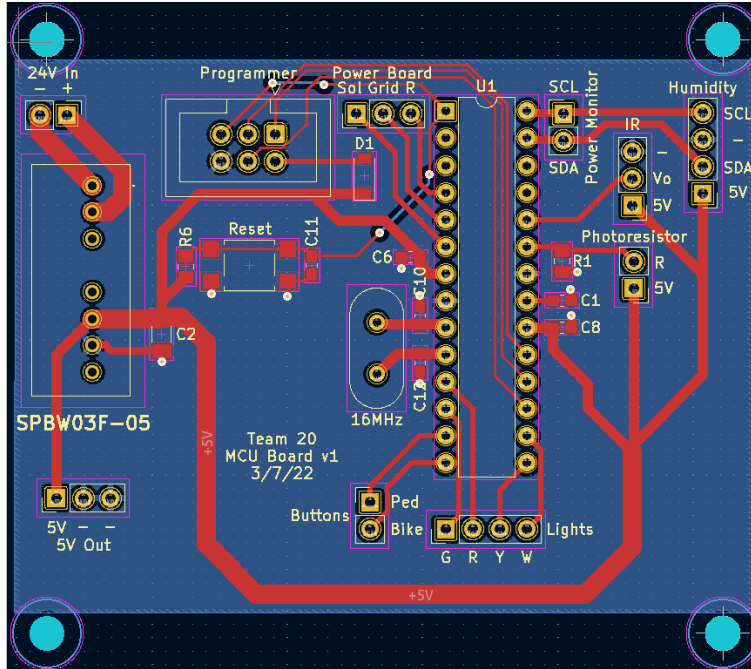


Figure 11: MCU board layout

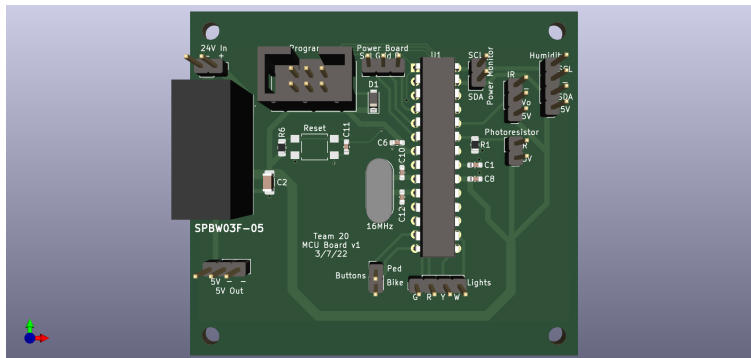


Figure 12: MCU board 3D layout

2.6 Buck Board Design

I also designed the PCB for a 5 V buck converter utilizing components left over from a previous parts order. This 5 V voltage level will be utilized where voltage isolation is unnecessary. The circuit schematic, PCB layout, and 3D PCB layout can be seen in Figures 13, 14, and 15, respectively.

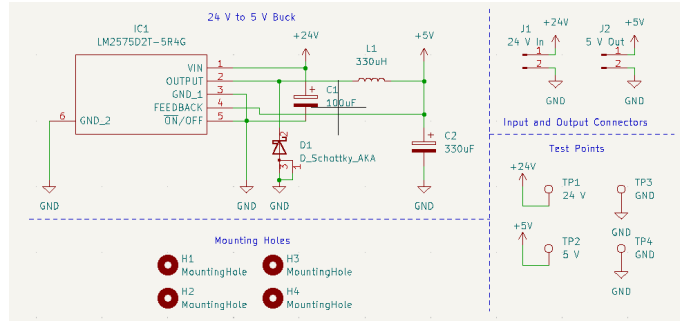


Figure 13: Buck board schematic

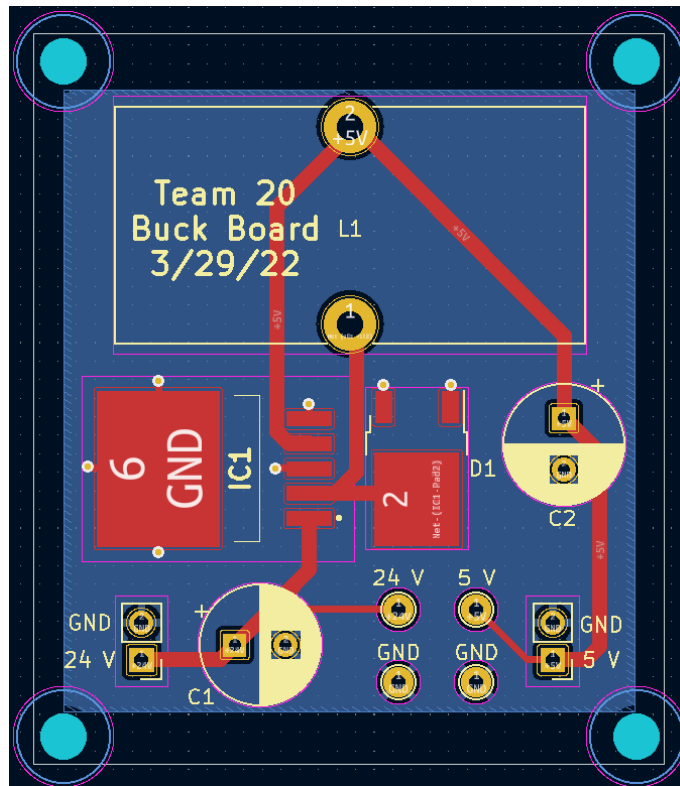


Figure 14: Buck board layout

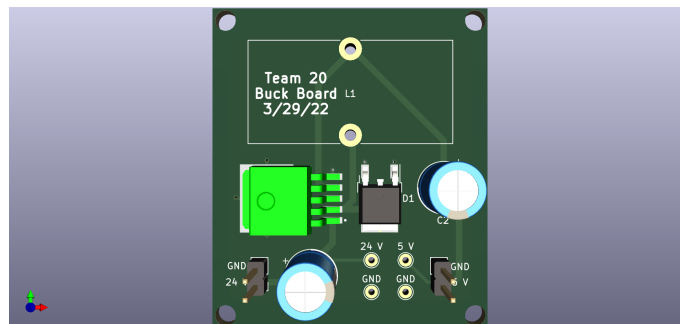


Figure 15: Buck board 3D layout

3 Verification

3.1 Switching Network

On 3/28, I spent six hours testing the switching network and ensuring its functionality. I soldered parts onto our first iteration of the power board and manually tested the board using an oscilloscope, two channels of a waveform generator, a DC power supply, and a digital multimeter to probe voltages and perform continuity checks. Separate 24 V lines from the power supply were connected to the grid and solar inputs on the board and complementary square waves with dead-time between them controlled the gate driver inputs.

The switching network seemed to fail, as only the grid voltage would be connected to the output while the solar voltage was unable to do so. After checking and resoldering connections, I decided to scour the LT1161 datasheet[5] to determine if I had made a mistake. I eventually realized that when one does not utilize the sensing function of the gate driver, one does not need capacitors connected to the timer pins. However, we had 1 μ F capacitors connected to each of these four pins, which hindered the functionality of the circuit. Upon removing these capacitors, the switching network became fully functional and the output smoothly transitioned between input sources based on the complementary square wave inputs controlling the gate driver.

3.2 Remaining Tests

Bowen was able to test the functionality of the SEPIC converter I designed, but the remaining tests will not be completed until the most recent iterations of our PCBs arrive around April 11. However, I am confident that we will be able to test, verify, and assemble our project in the week between receiving our new boards and our mock demonstration the week of April 18.

4 Conclusion

4.1 Completing Responsibilities

As mentioned previously, I plan to complete my testing of the remaining portions of the project once the newest PCBs arrive around April 11. Until then, I will begin work on the mock demonstration and prepare for the remaining tests and presentations between now and the end of the semester.

4.2 Ethical Consideration

I strive to adhere to the IEEE Code of Ethics in all the work I plan and complete throughout this project and design course. Particularly, it is necessary to be mindful of the safety of our design, seeing as it is a device that could be used in a commercial and public setting. I will fully commit my effort “to hold paramount the safety, health, and welfare of the public, to strive to comply with ethical design and sustainable development practices, to protect the privacy of others, and to disclose promptly factors that might endanger the public or the environment.” [7] If any portion of our project was not fully functional and, thus, posed a danger to anyone near the system during its operation, I would make it my main objective to disclose this information.

Additionally, in a highly collaborative setting, it is exceedingly important “to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, to be honest and realistic in stating claims or estimates based on available data, and to credit properly the contributions of others.” [7] As an engineer whose work depends on that of others and is often intertwined with it, it is critical for me to accept criticism and give credit where it is due. Without this, it would be impossible for one to produce the highest quality of their own work, or to help others do the same.

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