I2C Controlled 4.5A Single Cell USB / Adaptor Charger With Narrow VDC Power Path Management and USB OTG

FEATURES

- Up to 4.5A fast charge rate and 6A discharge rate
- Single input USB-compliant charger
  - 3.9V-17V input operating voltage range
  - Input voltage and current limit supports USB2.0 and USB 3.0
  - Support USB OTG (bq24190, bq24192(192I), 193)
  - USB host/charging port detection compatible to USB Battery Charger Spec 1.2
- Narrow VDC (NVDC) power path management
  - Instant-on works with no battery or deeply discharged battery
  - Battery supplements system when adapter is fully-loaded
- 1.5MHz switching frequency for low profile inductor
- I2C port for optimal system performance and status reporting
  - Input current limits: 100mA, 150mA, 500mA, 900mA, 1.2A, 1.5A, 2A and 3A
- Autonomous battery charging with or without host management
  - Battery charge enable
  - Battery charge preconditioning
  - Charge termination and recharge
- Accuracy
  - +/-0.5% charge voltage regulation
  - +/-5% charge current regulation
  - +/-5% input current regulation
  - +/-2% 5V OTG output voltage regulation
- High integration
  - Power path management
  - Synchronous switching MOSFETs
  - Integrated current sensing
  - Bootstrap diode
  - Internal loop compensation
- Safety
  - Battery temperature sensing and charging safety timer
  - JEITA guideline compliant (bq24193)
  - Thermal regulation and Thermal shutdown
  - Input/system over-voltage protection
  - MOSFET over-current protection
- Accelerate charge time by battery path impedance compensation
- Charge status outputs for LED or host processor
- Maximum power tracking capability by input voltage regulation
- Low battery leakage current
- 4mmx4mm QFN-24 Package

APPLICATIONS

- Tablet PC
- Portable Media Players
- Portable Internet Devices

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DESCRIPTION

The bq24190/191/192(192I)/193 is a highly-integrated switch-mode battery charge management and system power path management device for 1 cell Li-Ion and Li-polymer battery in a wide range of tablet and other portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I2C serial interface with charging and system settings makes the device a truly flexible solution.

The bq24190/191/192(192I)/193 supports a wide range of input sources, including standard USB host port, USB charging port and high power DC adapter. To set the default input current limit, the bq24190 detects the input source following the USB battery charging spec 1.2, and the bq24191/192(192I)/193 takes the result from detection circuit in the system, such as USB PHY device. The bq24190/191/192(192I)/193 is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. Meanwhile, the bq24190/192(192I)/193 supports USB On-the-Go operation by supplying 5V on VBUS with current limit up to 1.3A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system keeps operating even when the battery is completely depleted or removed. When the input source current or voltage limit is reached, the power path management automatically reduces the charge current to zero and then starts discharges the battery until the system power requirement is met. This supplement mode operation keeps the input source from getting overloaded.

The bq24190/191/192(192I)/193 can initiate and complete a charging cycle when host control is not available. It automatically detects the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. In the end, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. Later on, when the battery voltage falls below the recharge threshold, the charger will automatically start another charging cycle.

The bq24190/191/192(192I)/193 provides various safety features for battery charging and system operation, including dual pack negative thermistor monitoring, charging safety timer and over-voltage/over-current protections. The bq24193 supports JEITA guideline compliant temperature profile. The thermal regulation reduces charge current when the junction temperature exceeds 120C (programmable).

The STAT output reports the charging status and any fault conditions. The /PG output in bq24191/bq24192(192I)/193 indicates if a good power source is present. The INT immediately notifies host when fault occurs.

The bq24190/191/192(192I)/193 is available in 24-pin, 4x4 mm^2 thin QFN package.

DEVICE CONFIGURATION

	bq24190	bq24191	bq24192	bq24192I	bq24193
I2C Address	6BH	6AH	6BH	6BH	6BH
USB OTG	Yes	No	Yes	Yes	Yes
USB Detection	D+/D-	PSEL	PSEL	PSEL	PSEL
Default Battery Voltage	4.2V	4.2V	4.2V	4.1V	4.2V
Default Charge Current	2A	2A	2A	1A	2A
Default Adapter Current Limit (PSEL=0)	1.5A	1.5A	3A	1.5A	3A
Maximum Pre-charge Current	2A	2A	2A	640mA	2A
Charging Temperature Profile	Cold/Hot	Cold/Hot	Cold/Hot	Cold/Hot	JEITA
Status Output	STAT	STAT, /PG	STAT, /PG	STAT, /PG	STAT, /PG
STAT during Fault	Blinking @ 1Hz	Blinking @ 1Hz	Blinking @ 1Hz	10k to ground	Blinking @ 1Hz

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE	ORDERING NUMBER	QUANTITY
bq24190	bq24190	24-pin 4mmx4mm VQFN	bq24190RGER	3000
			bq24190RGET	250
bq24191	bq24191	24-pin 4mmx4mm VQFN	bq24191RGER	3000
			bq24191RGET	250
bq24192	bq24192	24-pin 4mmx4mm VQFN	bq24192RGER	3000
			bq24192RGET	250
Bq24192I	bq24192I	24-pin 4mmx4mm VQFN	bq24192IRGER	3000
			bq24192IRGET	250
bq24193	bq24193	24-pin 4mmx4mm VQFN	bq24193RGER	3000
			bq24193RGET	250

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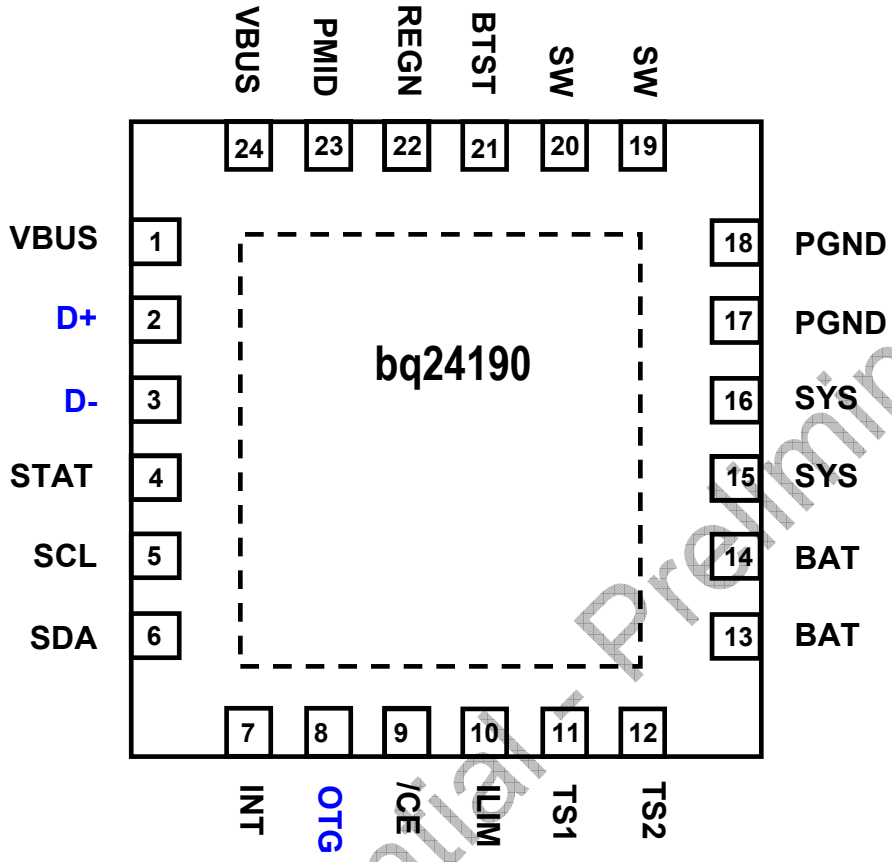
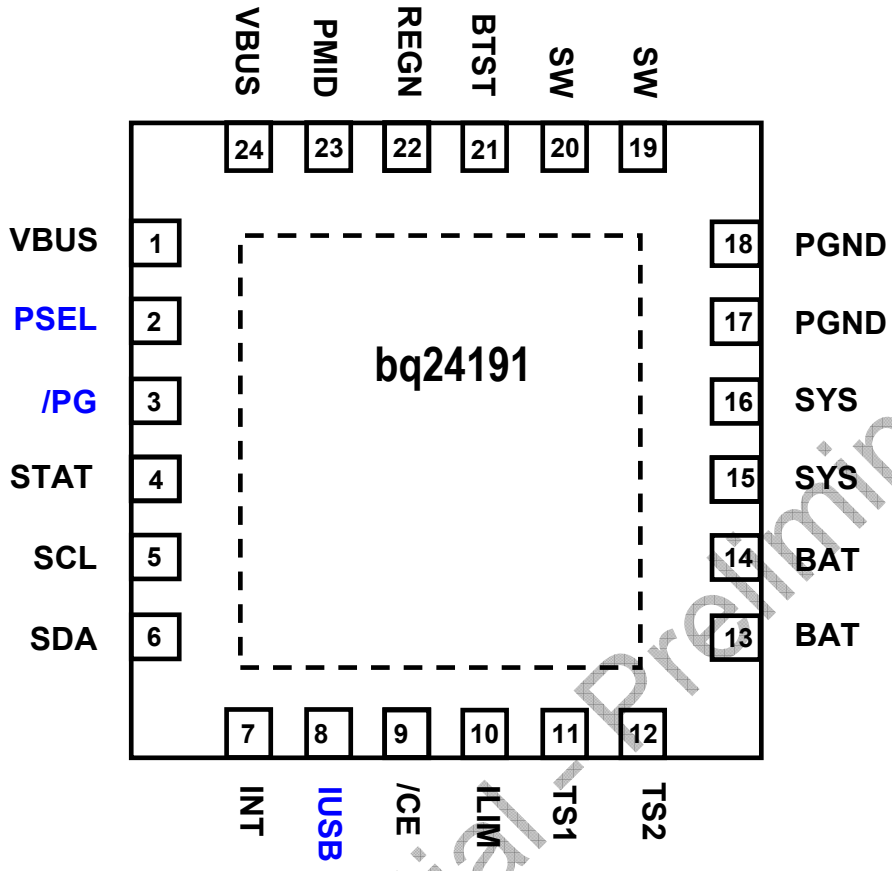
PINOUT





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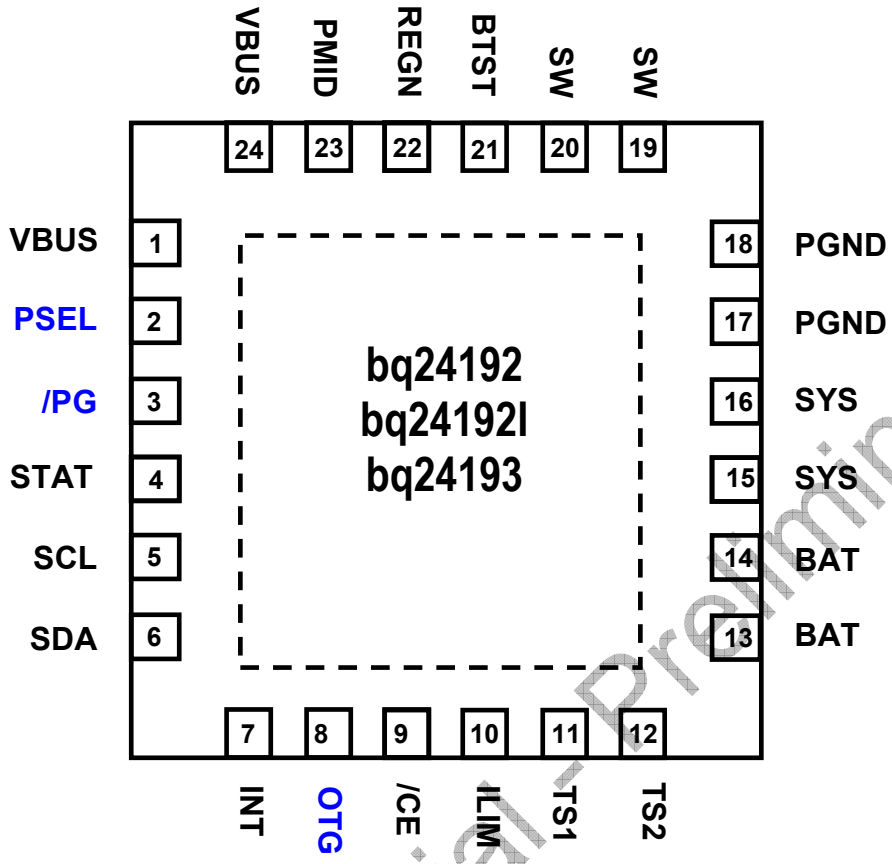

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ABSOLUTE MAXIMUM RATING

PARAMETER	PIN NAME	VALUE
Voltage Range (with respect to gnd)	VBUS	-2V – 20V
	PMID, STAT, /PG	-0.3V – 20V
	BTST	-0.3V – 26V
	SW	-2V – 20V
	BAT, SYS	-0.3V – 5V
	SDA, SCL, INT, OTG/IUSB, ILIM, REGN, TS1, TS2, /CE, PSEL, D+, D-	-0.3V – 7V
	BTST to SW	-0.3V – 7V
	PGND to GND	-0.3V – 0.3V
Output Sink Current	INT	1mA
	STAT	5mA
Junction temperature		-40C – 150C
Storage temperature		-65C – 150C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	VALUE
V_{IN}	Input Voltage	3.9V – 17V (1)
I_{IN}	Input Current (VBUS)	Up to 3A
I_{SYS}	Output Current (SW)	Up to 4.5A
I_{BAT}	Fast Charging Current	0.5A – 4.5A
	Discharging Current with internal MOSFET	Up to 6A continuous 9A peak
T_A	Operating free-air temperature range	-40C – 85C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A *tight* layout minimizes switching noise.

THERMAL INFORMATION

		RGE 24-pin	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	32.2	ºC/W
θ_{JC}	Junction-to-case thermal resistance	29.8	
θ_{JB}	Junction-to-board thermal resistance	9.1	
ψ_{JT}	Junction-to-top characterization parameter	0.35	
ψ_{JB}	Junction-to-board characterization parameter	9.1	

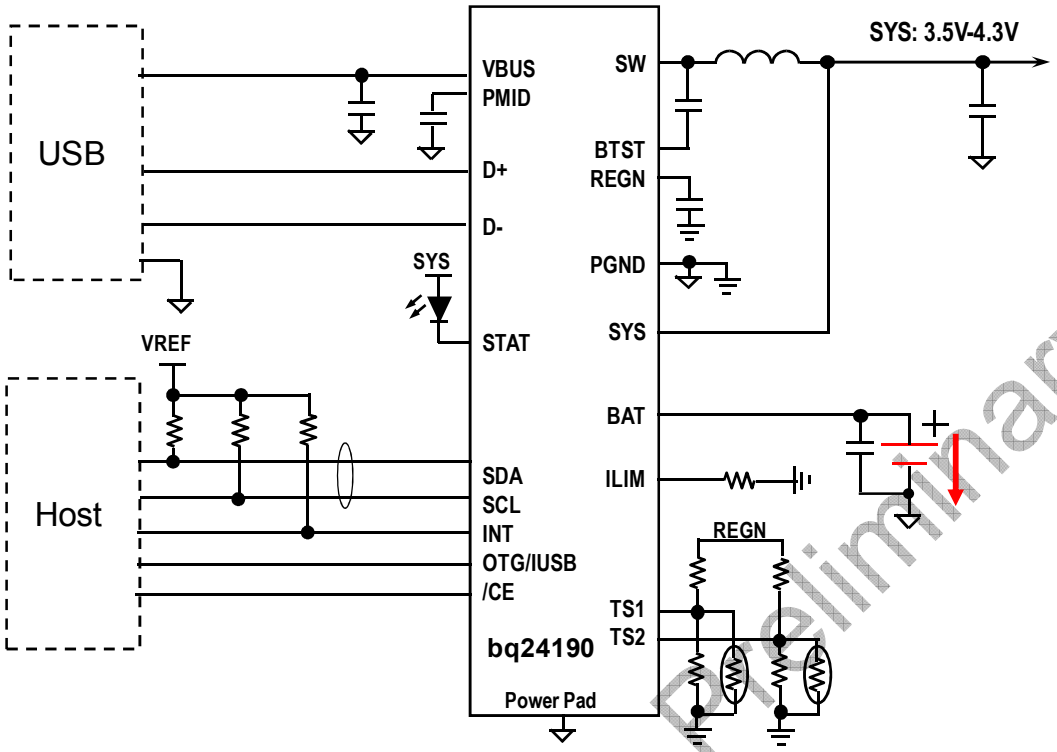
Note: For more information about traditional and new thermal metrics, see the “IC Package Thermal Metrics” application report SPRA953.

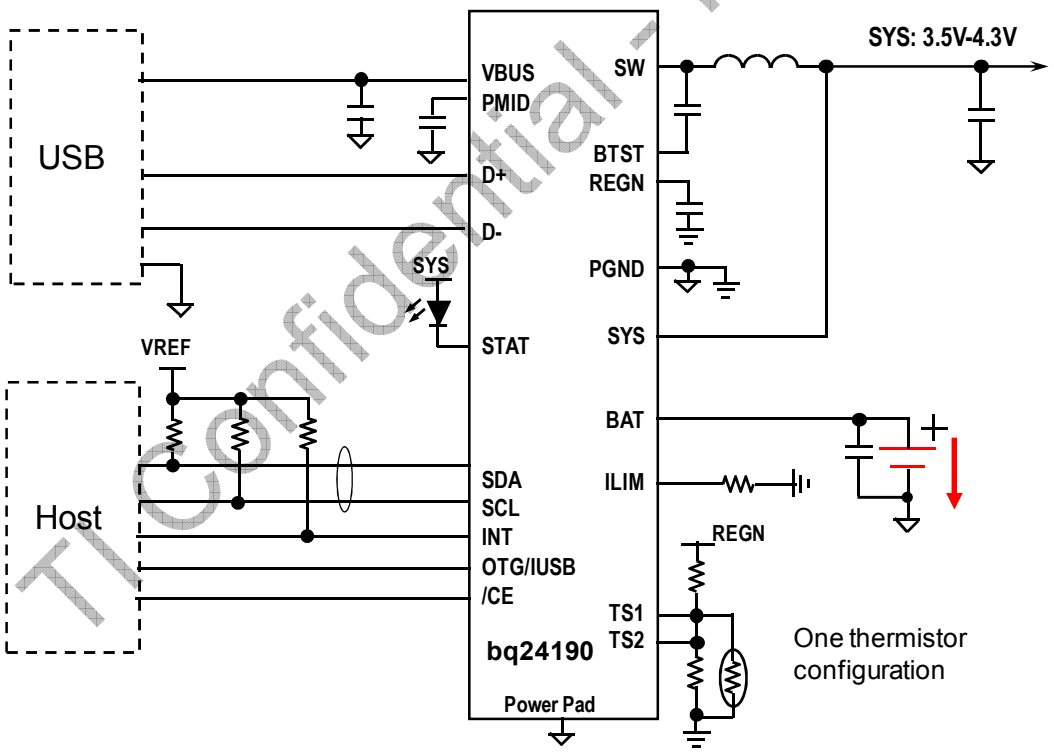
PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION DESCRIPTION
1,24	VBUS	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-μF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
2	D+ bq24190	I Analog	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The whole detection includes data contact detection and USB host (SDP) detection.
	PSEL bq24191, bq24192(192I), bq24193	I	Power source selection input. High indicates a USB source and Low indicates an adapter source.
3	D- bq24190	I Analog	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The whole detection includes data contact detection and USB host (SDP) detection.
	/PG bq24191, bq24192(192I) bq424193	O	Power good active low indicator. Connect to the pull up rail via 10kohm resistor. LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30mA.
4	STAT	O	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10kohm. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin in bq24190/191/192/193 blinks at 1Hz, and STAT pin in bq24192I has 10k to ground.
5	SCL	I	I2C Interface clock. Connect SCL to the logic rail through a 10kOhm resistor.
6	SDA	I/O	I2C Interface data. Connect SDA to the logic rail through a 10kOhm resistor.
7	INT	O	Open-drain Interrupt Output. Connect the INT to a logic rail via 10kOhm resistor. The INT pin sends active low, 256us pulse to host to report charger device status and fault.
8	OTG bq24190, bq24192(192I) bq24193	I Digital	USB current limit selection pin during buck mode, and enable pin during boost mode. In buck mode with USB host, when OTG = High, IIN limit = 500mA and when OTG = Low, IIN limit = 100mA. The boost mode is activated when the REG01[5:4]=10 and OTG pin is HIGH.
	IUSB Bq24191	I	In buck mode with USB host, when IUSB = High, IIN limit = 500mA and when IUSB = Low, IIN limit = 100mA.
9	/CE	I	Active low Charge Enable. Battery charge is enabled when REG01[5:4]=01 and /CE pin = Low.
10	ILIM	I	ILIM sets the maximum input current limit by regulating the ILIM voltage at 1V. A resistor is connected from ILIM pin to ground to set the limit as $I_{INMAX} = \frac{1V}{R_{ILIM}} * 450$. The actual input current limit is the lower one set by ILIM and by I2C. The minimum input current programmed on ILIM pin is 500mA.
11	TS1	I	Temperature qualification voltage input #1. Connect a negative

			temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from REGN to TS1 to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor. TS1 and TS2 pins have to be shorted together in bq24193.
12	TS2	I	Temperature qualification voltage input #2. Connect a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from REGN to TS2 to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor. TS1 and TS2 pins have to be connected together in bq24193.
13,14	BAT	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10uF closely to the BAT.
15,16	SYS	I	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage.
17,18	PGND	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
19,20	SW	O	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047-μF bootstrap capacitor from SW to BTST.
21	BTST	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047uF bootstrap capacitor from SW to BTST.
22	REGN	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. Connect a 1-μF ceramic capacitor from REGN to analog GND, close to the IC. REGN also serves as the pull-up rail of the logic I/Os and TS1/TS2 bias rail.
23	PMID	O	Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. Bypass it with up to 8.2uF capacitor from PMID to PGND.
Power Pad		P	Exposed pad beneath the IC for heat dissipation. Always solder Power Pad to the board, and have vias on the Power Pad plane star-connecting to PGND and ground plane for high-current power converter.

APPLICATION DIAGRAM





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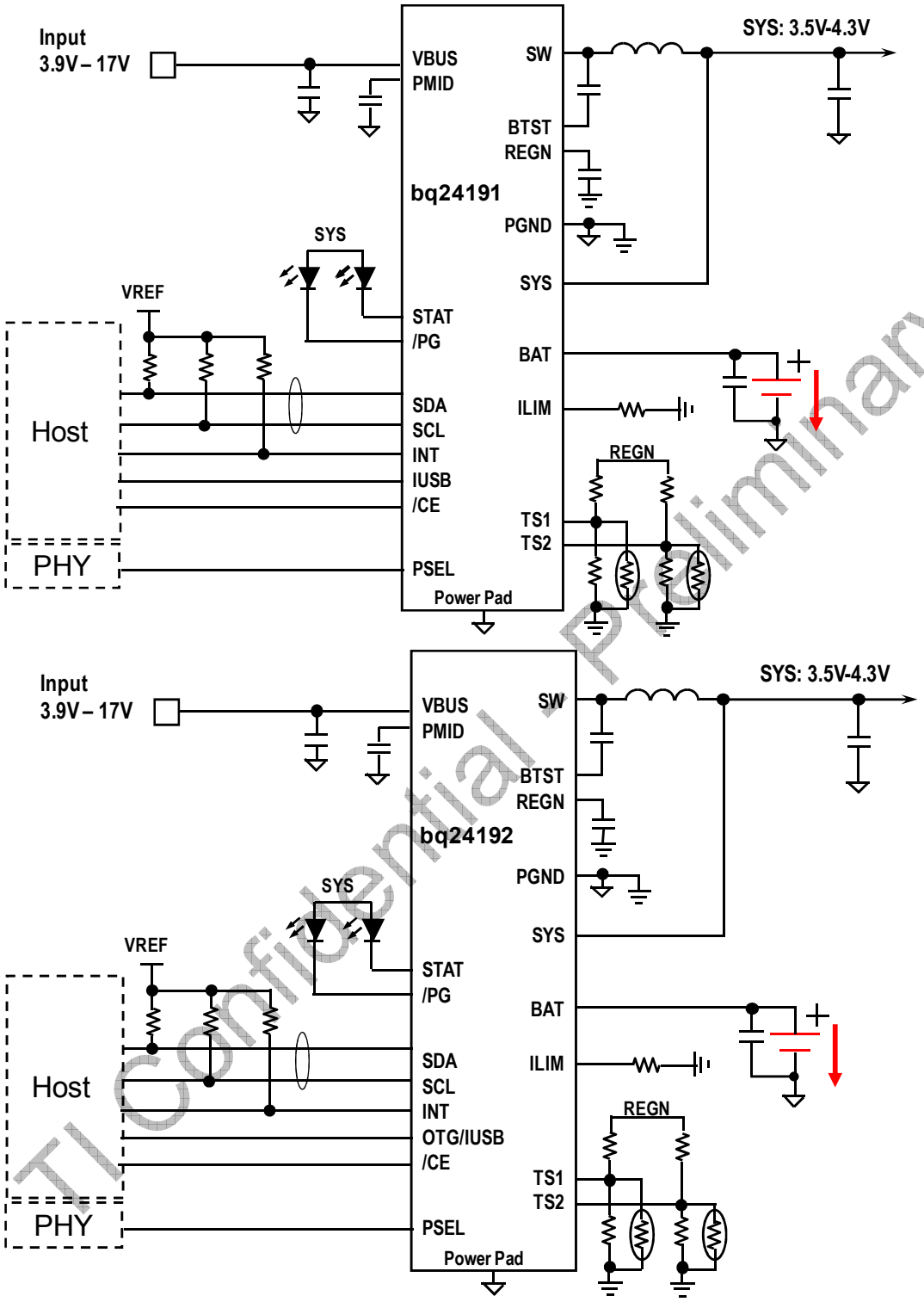

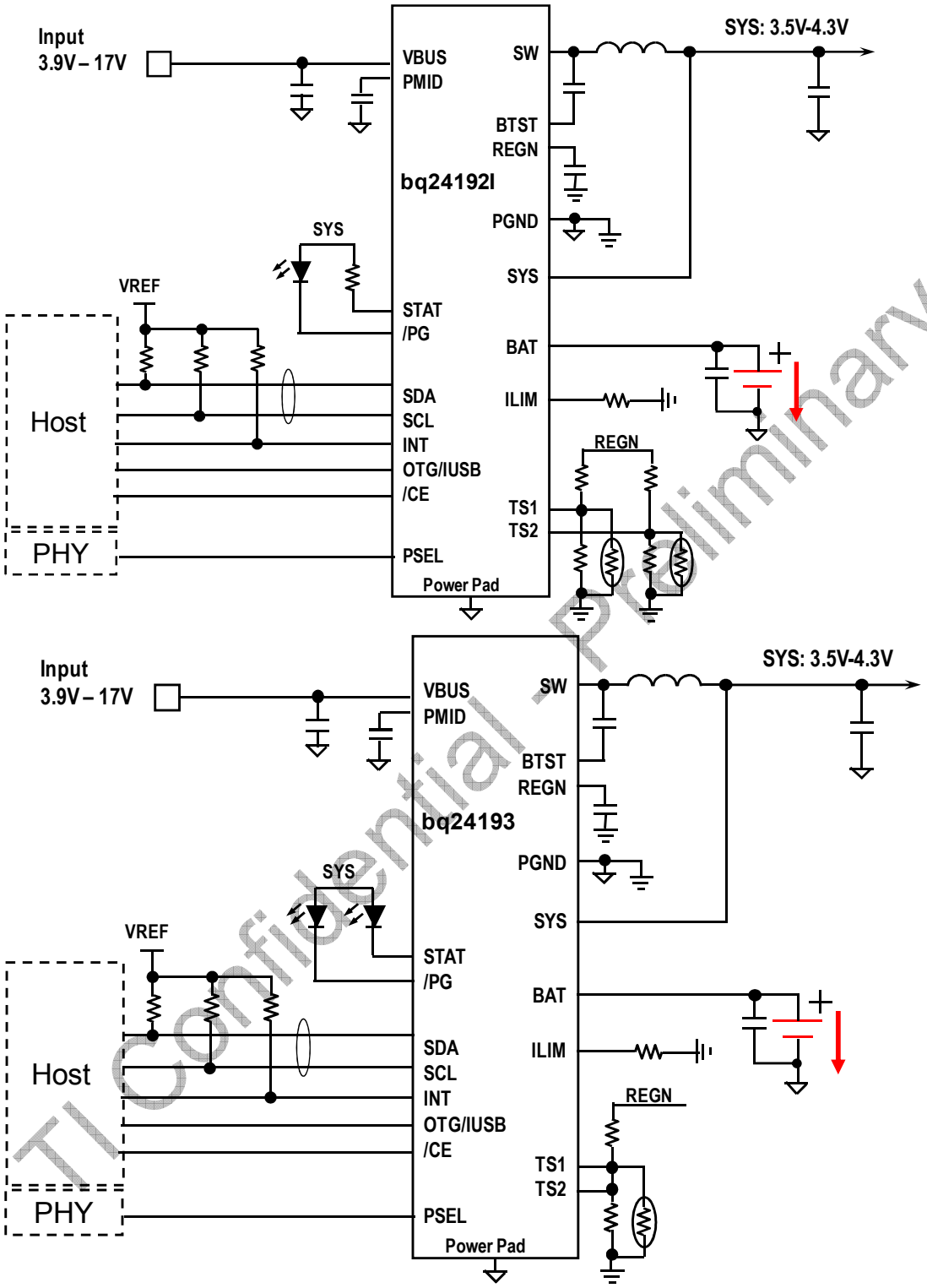

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I2C Register

Input Source Control Register REG00 (default 00110000, or 30)

Bit		Description	
Bit 7	EN_HIZ	0 – Disable, 1 – Enable	Default: Disable (0)
Input Voltage Limit			
Bit 6	VINDPM[3]	640mV	Offset 3.88V, Range: 3.88V-5.08V Default: 4.36V
Bit 5	VINDPM[2]	320mV	
Bit 4	VINDPM[1]	160mV	
Bit 3	VINDPM[0]	80mV	
Input Current Limit (Actual input current limit is the lower of I2C and ILIM)			
Bit 2	IINLIM[2]	000 – 100mA, 001 – 150mA, 010 – 500mA, 011 – 900mA, 100 – 1.2A, 101 – 1.5A, 110 – 2A, 111 – 3A	Default sdp: 100mA(OTG/IUSB pin=0) / 500mA (OTG/IUSB pin=1) Default dcp/cdp: 1.5A
Bit 1	IINLIM[1]		
Bit 0	IINLIM[0]		

Power-On Configuration Register REG01 (default 00011011, or 1B)

Bit		Description	
Bit 7	Register Reset	0 – Keep current register setting, 1 – Reset	Default: Keep current register setting (0)
Bit 6	I2C Watchdog Timer Reset	0 – Normal ; 1 – Reset	Default: Normal (0)
Charger Configuration			
Bit 5	CHG_CONFIG[1]	00 – Charge Disable, 01 – Charge Battery, 10/11 – OTG	Default: Charge Battery (01)
Bit 4	CHG_CONFIG[0]		
Minimum System Voltage Limit			
Bit 3	SYS_MIN[2]	0.4V	Offset: 3.0V, Range 3.0V-3.7V Default: 3.5V
Bit 2	SYS_MIN[1]	0.2V	
Bit 1	SYS_MIN[0]	0.1V	
USB OTG			
Bit 0	BOOST_LIM	0 – 500mA, 1 – 1.3A	Default: 1.3A

Charge Current Control Register REG02 (bq24190/191/192/193 default 01100000, or 60; bq24192I default 00100000, or 20)

Bit		Description	Note
Fast Charge Current Limit			
Bit 7	ICHG[5]	2048mA	Offset: 500mA Range: 500-4532mA Default: 2036mA (bq24190/1/2/3), 1012mA (bq24192I)
Bit 6	ICHG[4]	1024mA	
Bit 5	ICHG[3]	512mA	
Bit 4	ICHG[2]	256mA	
Bit 3	ICHG[1]	128mA	
Bit 2	ICHG[0]	64mA	
Bit 1	NOT IN USE		
Bit 0	NOT IN USE		

Pre-Charge/Termination Current Control Register REG 03 (default 00010001, or 11)

Bit		Description	Note
Pre-Charge Current Limit			
Bit 7	IPRECHG[3]	1024mA	Offset: 128mA, Range:
Bit 6	IPRECHG[2]	512mA	

Bit 5	IPRECHG[1]	256mA	128mA – 2048mA (bq24190/1/2/3) 128mA – 640mA(0100) (bq24192I) Default: 256mA (0001)
Bit 4	IPRECHG[0]	128mA	
Termination Current Limit			
Bit 3	ITERM[3]	1024mA	Offset: 128mA Range: 128mA – 2048mA Default: 256mA (0001)
Bit 2	ITERM[2]	512mA	
Bit 1	ITERM[1]	256mA	
Bit 0	ITERM[0]	128mA	

Charge Voltage Control Register REG04 (bq24190/191/192/193 default: 10110010, or B2; bq24192I default 10011010, or 9A)

Bit		Description	Note
Charge Voltage Limit			
Bit 7	VREG[5]	512mV	Offset: 3.504V Range: 3.504V – 4.400V Default: 4.208V (bq24190/1/2/3), 4.112V (bq24192I)
Bit 6	VREG[4]	256mV	
Bit 5	VREG[3]	128mV	
Bit 4	VREG[2]	64mV	
Bit 3	VREG[1]	32mV	
Bit 2	VREG[0]	16mV	
Bit 1	BATLOWV	0 – 2.8V, 1 – 3.0V	Default: 3.0V (1) (pre-charge to fast charge)
Battery Recharge Threshold, below battery regulation voltage			
Bit 0	VRECHG	0 – 100mV, 1 – 300mV	Default: 100mV (0)

Charge Termination/Timer Control Register REG05 (default 10011010, or 9A)

Bit		Description	Note
Termination Setting			
Bit 7	EN_TERM	0 – Disable, 1 – Enable	Default: Enable termination (1)
Termination Indicator Threshold			
Bit 6	TERM_STAT	0 – Match ITERM, 1 – Indicate before the actual termination on STAT	Default Match ITEM (0)
I2C Watchdog timer Limit			
Bit 5	WATCHDOG[1]	00 – Disable timer, 01 – 40s, 10 – 80s, 11 – 160s	Default: 40s (01)
Bit 4	WATCHDOG[0]		
Safety Timer Setting			
Bit 3	EN_TIMER	0 – Disable, 1 – Enable	Default: Enable timers (1)
Fast Charge Timer (2X during VINDPM, IINDPM, Thermal Regulation)			
Bit 2	CHG_TIMER[1]	00 – 5 hrs, 01 – 8 hrs, 10 – 12 hrs, 11 – 20 hrs	Default: 8 hours (01)
Bit 1	CHG_TIMER[0]		
JEITA Low Temperature Current Setting			
Bit 0	JEITA_ISET (0C-10C)	0 – 50%, 1 – 20%	Percentage with respect to ICHG in REG02, Default: 50% (0)

IR Compensation / Thermal Regulation Control Register REG06 (default 00000011, or 03)

Bit		Description	Note
IR Compensation Resistor Setting			
Bit 7	BAT_COMP[2]	40mOhm	Range: 0 – 70mOhm Default: 0Ohm (000)
Bit 6	BAT_COMP[1]	20mOhm	
Bit 5	BAT_COMP[0]	10mOhm	
IR Compensation Voltage Clamp (above regulation voltage)			

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Bit 4	VCLAMP[2]	64mV	Default: 0V (000)
Bit 3	VCLAMP[1]	32mV	
Bit 2	VCLAMP[0]	16mV	
Thermal Regulation Threshold			
Bit 1	TREG[1]	00 – 60C, 01 – 80C, 10 – 100, 11 – 120C	Default: 120C
Bit 0	TREG[0]		

Misc Operation Control Register REG07 (default 01001011, or 4B)

Bit		Description	Note
Bit 7	DPDM_EN	0 – Not in D+/D- detection; 1 – Force D+/D- detection	Default: Not in DPDM detection (0)
Bit 6	TMR2X_EN	0 – Disable 2X extended safety timer, 1 – Enable 2X extended safety timer	Default: Enable (1) to run safety timer in half clock rate during DPM and thermal regulation.
Bit 5	BATFET_Disable	0 – Enable Q4, 1 – Turn off Q4	Default: Enable Q4(0)
Bit 4	JEITA_VSET (45C-60C)	0 – 4.05V, 1 – 4.2V	Default: 4.05V (0)
Bit 3	NOT IN USE		
Bit 2	NOT IN USE		
Bit 1	INT_MASK[1]	0 – No INT during CHRG_FAULT, 1 – INT on CHRG_FAULT	Default: INT on CHRG_FAULT (1)
Bit 0	INT_MAST[0]	0 – No INT during BAT_FAULT, 1 – INT on BAT_FAULT	Default: INT on BAT_FAULT (1)

System Status Register REG08

Bit		Description
Bit 7	VBUS_STAT[1]	00 – Unknown (no input, or DPDM detection incomplete), 01 – USB host, 10 – Adapter port, (from DPDM detection or PSEL detection) 11 – OTG
Bit 6	VBUS_STAT[0]	
Bit 5	CHRG_STAT[1]	00 – Not Charging, 01 – Pre-charge (<$V_{BATDEPL}$), 10 – Fast Charging, 11 – Charge Done
Bit 4	CHRG_STAT[0]	
Bit 3	DPM_STAT	0 – Not DPM, 1 – VINDPM or IINDPM
Bit 2	PG_STAT	0 – Not Power Good, 1 – Power Good
Bit 1	THERM_STAT	0 – Normal, 1 – TREG
Bit 0	VSYS_STAT	0 – Not in VSYSMIN regulation (BAT>VSYSMIN), 1 – In VSYSMIN regulation, battery is too low

Fault Register REG09

Bit		Description
Bit 7	WATCHDOG_FAULT	0 – Normal, 1- Watchdog timer expiration
Bit 6	OTG_FAULT	0 – Normal, 1 – VBUS overloaded in OTG, or VBUS OVP
Bit 5	CHRG_FAULT[1]	00 – Normal, 01 – Input fault (OVP or bad source), 10 - Thermal shutdown, 11 – Charge timer expiration
Bit 4	CHRG_FAULT[0]	
Bit 3	BAT_FAULT	0 – Normal, 1 – BATOVP[1]
Bit 2	NTC_FAULT[2]	000 – Normal, 001 – TS1 Cold, 010 – TS1 Hot, 011 – TS2 Cold, 100 – TS2 Hot, 101 – Both Cold, 110 – Both Hot, 111 – one Hot, one Cold (bq24190/191/192/192I) 000 – Normal, 010 – Warm, 011 – Cool, 101 – Cold, 110 – Hot (bq24193)
Bit 1	NTC_FAULT[1]	
Bit 0	NTC_FAULT[0]	

[1] BATOVP will be available in PG1.3.

Vender / Part / Revision Status Register REG0A

Bit		Description
Bit 7	NOT IN USE	
Bit 6	NOT IN USE	
Bit 5	PN[2]	TBD
Bit 4	PN[1]	
Bit 3	PN[0]	
Bit 2	TS_PROFILE	0 – Cold/Hot window, 1 – JEITA profile
Bit 1	Not In Use	
Bit 0	Not In Use	

ELECTRICAL CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
QUIESCENT CURRENTS						
I_{BAT}	Battery Discharge Current (BAT, SW, SYS)	V_{VBUS} < V_{UVLO} , VBAT=4.2V, leakage between BAT and VBUS			5	μA
		V_{VBUS} > V_{UVLO}, V_{VBUS} > V_{BAT}, High-Z Mode, BATFET disabled			20	μA
		V_{VBUS} > V_{UVLO}, V_{VBUS} > V_{BAT}, High-Z Mode			50	μA
I_{VBUS}	Input Supply Current (VBUS)	V_{VBUS} =5V, High-Z Mode		15	30	uA
		V_{VBUS} > V_{UVLO}, V_{VBUS} > V_{BAT}, PWM not switching		2	5	mA
		V_{VBUS} > V_{UVLO}, V_{VBUS} > V_{BAT}, PWM switching		15		mA
VBUS/BAT Power Up						
V_{VBUS_OP}	VBUS Operating Range		3.9		17	V
V_{VBUS_UVLOZ}	VBUS UVLOZ, no battery, I2C active	V_{VBUS} rising			3.6	V
V_{SLEEP}	Sleep Mode falling threshold,	V_{VBUS} falling, V_{VBUS}-V_{BAT}		80		mV
V_{SLEEPZ}	Sleep Mode rising threshold	V_{VBUS} rising, V_{VBUS}-V_{BAT}		300		mV
V_{ACOV}	VBUS Over-Voltage Rising Threshold	V_{VBUS} rising		18		V
V_{BAT_UVLOZ}	VBUS UVLOZ, no VBUS, I2C active	V_{BAT} rising	2.3			V
V_{BAT_DEPL}	Battery Depletion Threshold	V_{BAT} falling		2.4	2.6	V
V_{BAT_DEPL}	Battery Depletion rising hysteresis	V_{BAT} rising		200		mV
$V_{VBUSMIN}$	Bad adapter detection threshold	V_{VBUS} falling		3.8		V
I_{BADSRC}	Bad adapter detection current source			30		mA
t_{BADSRC}	Bad source detection duration			30		ms
Power Path Management						
V_{SYS_RANGE}	System Regulation Voltage	Isys=0A, Q4 off, V_{BAT_REG}=4.2V, V_{SYSMIN}=3.5V	3.5		4.3	V
V_{SYS_MIN}	System Voltage Output	V_{SYSMIN}=3.5V	3.5	3.65		V
$R_{ON(RBFET)}$	Internal top reverse blocking MOSFET on-resistance	Measured between VBUS and PMID		28	40	mΩ
$R_{ON(HSFET)}$	Internal top switching MOSFET on-resistance	Measured between PMID and SW		25	35	mΩ
$R_{ON(LSFET)}$	Internal bottom switching MOSFET on-resistance	Measured between SW and PGND		25	35	mΩ
V_{FWD}	BATFET forward voltage in supplement mode	BAT discharge current 10mA		20		mV
V_{BATGD}	Battery good comparator rising threshold	V_{BAT} rising		3.6		V
V_{BATGD_HYST}	Battery Good Comparator Falling Threshold	V_{BAT} falling		100		mV

ELECTRICAL CHARACTERISTICS (CONTINUED)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Battery Charger						
V_{BAT_REG}	Charge voltage regulation accuracy		-0.5		0.5	%
I_{ICHG_REG}	Fast charge current regulation accuracy	Precharge to fast charge, REG04[1]=1	-5		5	%
$V_{BATLOWV}$	Battery LOWV falling Threshold	Fast charge to precharge, REG04[1]=1		2.8		V
$V_{BATLOWV\_HYST}$	Battery LOWV Falling Threshold	Precharge to fast charge, REG04[1]=1		3.0		mV
I_{PRECHG_REG}	Precharge Current Regulation Accuracy		-25		25	%
I_{TERM}	Termination Current Accuracy		-25		25	%
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0]=0		100		mV
R_{ON_BATFET}	SYS-BAT MOSFET on-resistance			12	15	mΩ
Input Voltage/Current Regulation						
V_{INDPM_REG}	Input Voltage Regulation Accuracy		-2		2	%
I_{INDPM}	Input Current Regulation Limit	USB100			100	mA
		USB150			150	mA
		USB500			500	mA
		USB900			900	mA
		USB1500			1500	mA
I_{INDPM_REG}	Input Current Regulation Accuracy		-5		5	%

ELECTRICAL CHARACTERISTICS (CONTINUED)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BAT Over-Voltage Protection [1]						
V_{BATOVP}	Battery over-voltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104		%
V_{BATOVP_HYST}	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		2		%
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			10		ms
Thermal Regulation and Thermal Shutdown						
$T_{Junction\_REG}$	Junction Temperature Regulation Accuracy	REG06[1:0]=11	115	120	125	°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature Increasing		160		°C
T_{SHUT_HYS}	Thermal Shutdown Hysteresis			30		°C
	Thermal Shutdown Rising Deglitch	Temperature Increasing Delay		100		µs
	Thermal Shutdown Falling Deglitch	Temperature Decreasing Delay		10		ms
Cold/Hot Thermister Comparator (bq24190/191/192/192I)						
V_{LTF}	Cold Temperature Threshold, TS pin Voltage Rising Threshold	Charger suspends charge. As Percentage to V_{REGN}	73	73.5	74	%
V_{LTF_HYS}	Cold Temperature Hysteresis, TS pin Voltage Falling	As Percentage to V_{REGN}	0.2	0.4	0.6	%
V_{HTF}	Hot Temperature TS pin voltage falling Threshold	As Percentage to V_{REGN}	46.6	47.2	48.8	%
V_{TCO}	Cut-off Temperature TS pin voltage falling Threshold	As Percentage to V_{REGN}	44.2	44.7	45.2	%
	Deglitch time for Temperature Out of Range Detection	$V_{TS} > V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		400		ms
JEITA Thermister Comparator (bq24193)						
V_{T1}	T1 (0 °C) threshold, Charge suspended T1 below this temperature.	V_{TS} rising, As Percentage to V_{REGN}	70.2	70.8	71.4	%
V_{t1_HYS}	Charge back to $I_{CHG}/2$ and 4.2V above this temperature.	Hysteresis, V_{TS} falling		0.6		%
V_{T2}	T2 (10°C) threshold, Charge back to $I_{CHG}/2$ and 4.2V below this temperature.	V_{TS} rising, as percentage of V_{REGN}	68.0	68.6	69.2	%
V_{T2_HYS}	Charge back to I_{CHG} and 4.2V above this temperature.	Hysteresis, V_{TS} falling		0.8		%
V_{T3}	T3 (45°C) threshold, Charge back to I_{CHG} and 4.05V above this temperature.	V_{TS} falling, as percentage of V_{REGN}	55.5	56.1	56.7	%
V_{T3_HYS}	Charge back to I_{CHG} and 4.2V below this temperature.	Hysteresis, V_{TS} rising		0.8		%
V_{T5}	T5 (60°C) threshold, charge suspended above this temperature.	V_{TS} falling, as percentage of V_{REGN}	47.6	48.1	48.6	%
V_{T5_HYS}	Charge back to I_{CHG} and 4.05V below this temperature.	Hysteresis, V_{TS} rising		1.2		%

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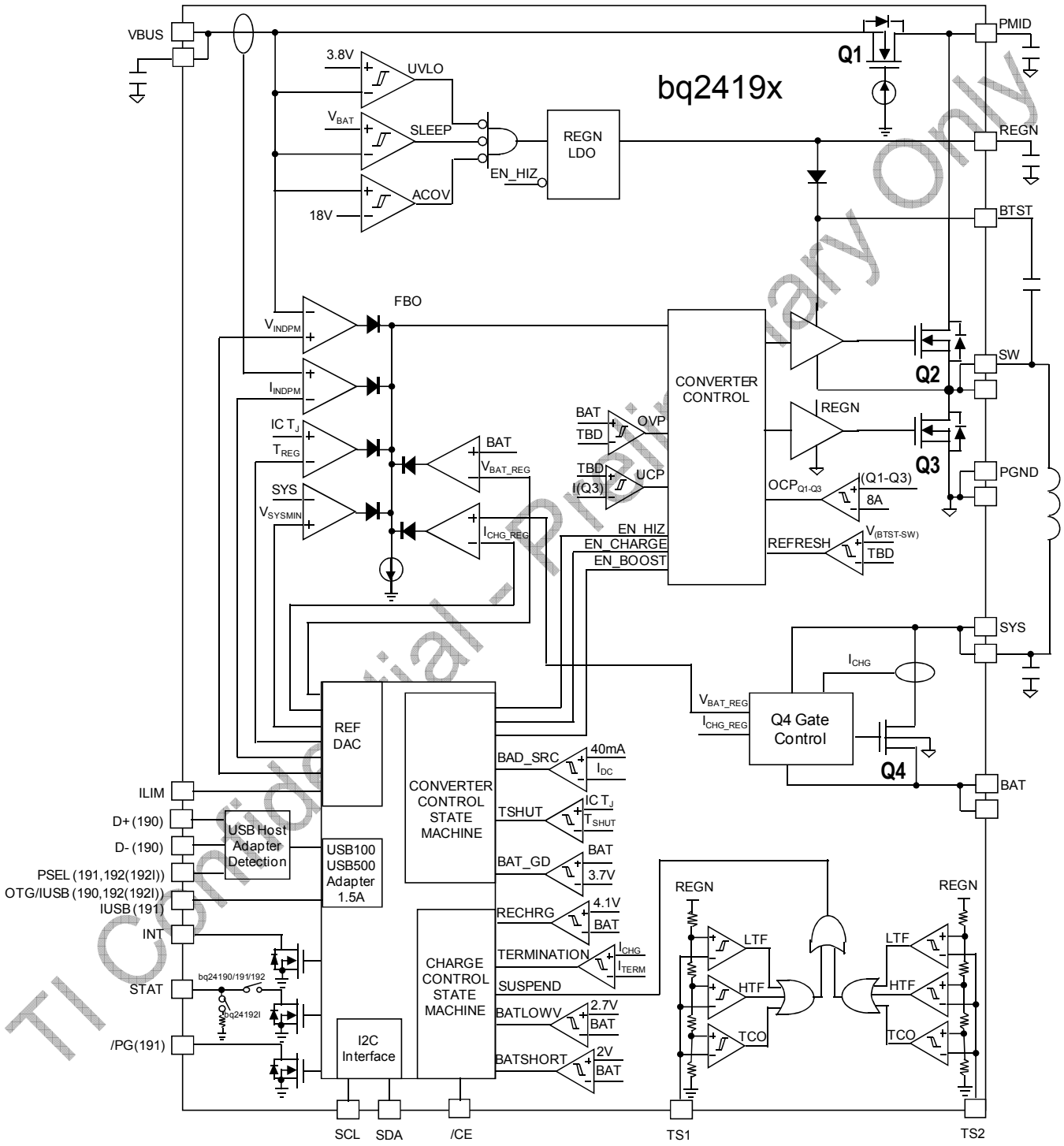
ELECTRICAL CHARACTERISTICS (CONTINUED)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Charge Over-Current Comparator						
I_{RBFET_OCP}	RBFET over-current threshold			5		A
I_{HSFET_OCP}	HSFET over-Current threshold		5.3	7		A
I_{BATFET_OCP}	System over load threshold		9			A
Charge Under-Current Comparator (Cycle-by-Cycle)						
V_{LSFET_UCP}	LSFET charge under-current falling threshold	From sync mode to non-sync mode		100		mA
Switching Frequency						
F_{SW}	PWM Switching Frequency		1300	1500	1700	kHz
Boost Mode Operation						
V_{OTG_REG}	OTG output voltage	I(VBUS)=0	-2		2	%
		I(VBUS)=1.3A	-3		3	%
V_{OTG_BAT}	Battery operating voltage for boost mode		3.0			V
V_{OTG_OVP}				5.4		V
V_{OTG_ILIM}	LSFET Cycle by cycle current limit			4.6		A
I_{RBFET_OCP}	RBFET over-current threshold	REG01[0]=1		1.8		A
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS}=10V, I_{REGN}=40mA	5.7	6	6.3	V
		V_{VBUS}=5V, I_{REGN}=40mA	4.75	4.8	4.85	V
I_{REGN}	REGN LDO current limit	V_{VBUS}=10V, V_{REGN}=3.8V	50			mA

ELECTRICAL CHARACTERISTICS (CONTINUED)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Logic I/O pin Characteristics (OTG/IUSB, /CE, PSEL, STAT, /PG)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold		1.3			V
V_{OUT_LO}	Output Low Saturation Voltage	Sink Current = 5 mA			0.4	V
I_{BIAS}	High Level Leakage Current	Pull up rail 1.8V			1	uA
I2C Interface (SDA, SCL, INT)						
V_{IH}	Input high threshold level	VPULL-UP=1.8V, SDA and SCL	1.3			V
V_{IL}	Input low threshold level	VPULL-UP=1.8V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	IL=10mA, sink current			0.4	V
I_{BIAS}	High-Level leakage current	VPULL-UP=1.8V, SDA and SCL			1	µA
f_{SCL}	SCL clock frequency				400	kHz

Block Diagram



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Detail description

The bq24190/191/192(192I)/193 is an I2C controlled power path management device and a single cell Li-Ion battery charger. The bq24190/191/192(192I)/193 integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

Power Path Management

The bq24190/191/192(192I)/193 accommodates a wide range of sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system from input source (VBUS), battery (BAT), or both.

Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage on VBUS and BAT. As soon as on VBUS or VBAT rises above UVLO, the internal sleep comparator, battery depletion comparator and BATFET driver are active, I2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

Battery Only

If only battery is present and the voltage is above depletion threshold, the BATFET turns on and connects battery to system. The 10mΩ BATFET minimizes the conduction loss during discharge. The low R_{DSON} in the power path and the low quiescent current on BAT help extend the battery run time.

The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and keep BATFET off until the input source plugs in again.

The BATFET can be forced off by the host through I2C REG07[5]. This bit allows the user to independently turn off the BATFET when the battery becomes abnormal.

Input Source with Battery

When the voltage on VBUS is above the battery voltage, the device is no longer in SLEEP mode. The REGN LDO and the bias circuits are active to get ready for buck operation.

REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. Additionally, the LDO provides bias rail to TS1/TS2 external resistors. The pull-up rail of STAT and /PG can be connected to REGN as well.

The REGN is enabled under the following buck and boost modes.

Buck Mode

1. VBUS above UVLO
2. VBUS above battery (not in sleep mode)
3. OTG operation is not enabled

Boost (OTG) Mode

1. BAT above BATLOWV threshold (REG04[1])
2. VBUS below BAT (in sleep mode)
3. OTG operation is enabled (OTG pin HIGH and REG01[5:4]=10/11)

Input Source Qualification

The bq24190/191/192(192I)/193 checks the voltage and current of the input source before starting the converter. The input source has to meet the following requirements to power the buck converter.

1. VBUS voltage above BAT voltage (not in SLEEP mode) and below 18V (not in ACOV)
2. VBUS voltage above 3.8V when pulling 30mA (not poor source)
3. OTG operation is not enabled

Once the input source passes all the conditions above, the device starts the converter in buck operation. The status register REG08[2] goes high and the /PG pin (bq24191/192(192I)) goes low. An INT is asserted to the host.

Converter Power-up

After the input source is qualified, and the input current limit is set (refer to "USB Detection and Input Current Limit Setting"), the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the higher of the minimum system voltage (default 3.5V).

When charging a depleted battery, the BATFET starts in linear operation (LDO mode), and the system is 100mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

The system is always regulated with a margin above the minimum system voltage setting. Therefore, even during transient drop, the system is always above the minimum voltage setting. The status register REG08[0] goes high when the system is in minimum system voltage regulation.

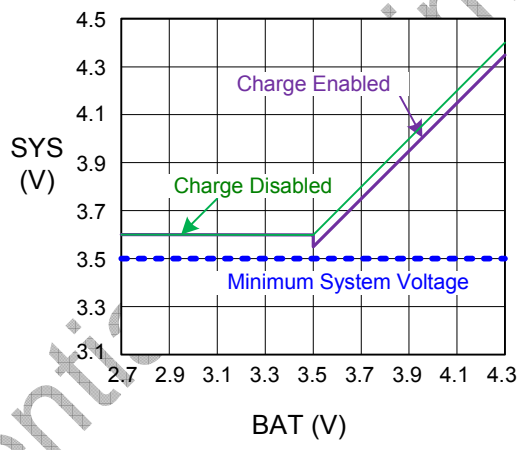


Figure V(SYS) vs V(BAT)

Dynamic Power Management

To meet USB maximum current limit and avoid over loading the adapter, the bq24190/191/192(192I) features Dynamic Power Management (DPM) and continuously monitors the input current and input voltage.

When input source is over-loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below input voltage limit (REG00[6:3]). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is down to zero, but the input source is still overloaded, the system voltage starts to fall. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode. The BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During supplement mode, the status register REG08[3] will go high to indicate the device is in dynamic power management regulation (either input current or voltage regulation).

BATFET turns off to stop supplement when the battery is below battery depletion threshold.

The figure shows the DPM response with 9V/1.2A adapter, 3.2V battery, 2.8A charge rate and 3.4V minimum system voltage setting.

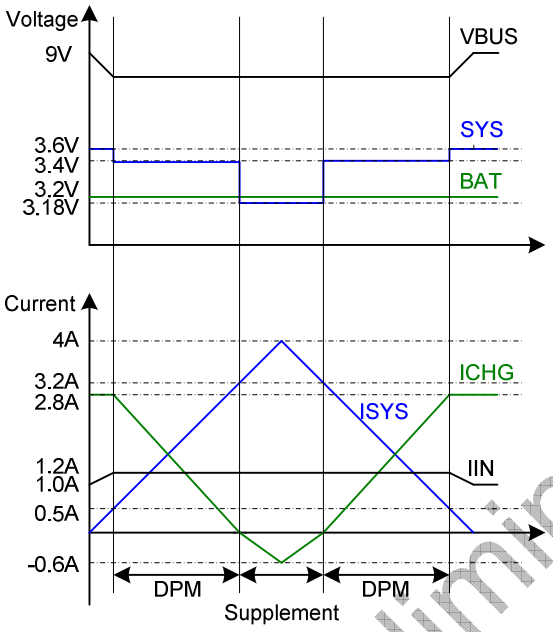


Figure DPM Response

Supplement Mode

During the supplement mode, the BATFET operates as a diode. When the system falls below the battery, the BATFET turns on and regulate the gate drive of BATFET so that the minimum BATFET V_{DS} stays at 20mV when the current is low. Therefore, there is no oscillation when entering and exiting the supplement mode. As the discharge current goes higher, the BATFET gets bigger gate drive and smaller R_{DSON} until the BATFET is in full conduction. Afterwards, the BATFET V_{DS} linearly increases with discharge current. The figure shows the V-I curve of the diode operation.

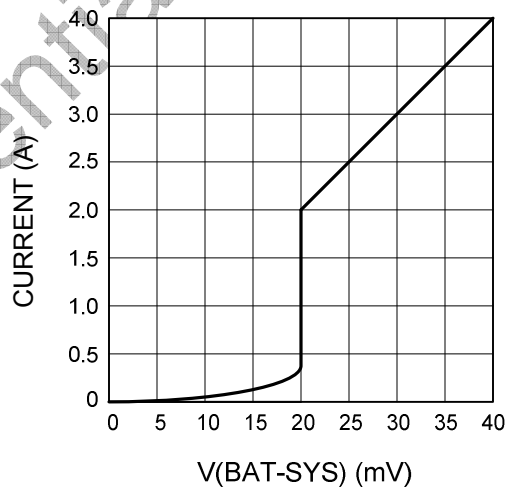


Figure BATFET V-I Curve

Boost Mode Operation

The bq24190/192(192I)/193 supports USB On-The-Go (OTG) to deliver power from the battery back to other USB OTG devices. The boost operation can be enabled if the conditions are valid:

1. VBUS voltage is below battery (in sleep mode)

2. Host enables boost operation (REG01 bit[5:4]=10) and OTG/IUSB pin is HIGH
3. Battery above BATLOWV threshold (REG04[1])

The OTG output current can be selected as 500mA or 1.3A via I2C (REG01[0]). During boost mode, the status register REG08[7:6] is set to 11.
Any fault during boost operation, including VBUS over voltage or shorted, sets the fault register REG09[6] to 1 and an INT is asserted.

Battery Charging Profile

The bq24190/191/192(192I)/193 charges 1-cell Li-Ion battery with up to 4.5A charge current to reduce charge time. The 10mΩ BATFET minimizes the charging conduction loss and improve the efficiency during battery charging and discharging.

Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4]=01), the bq24190/191/192(192I)/193 doesn't need host involvement to complete a charging cycle.
A new charge cycle starts when the following conditions are valid:

- The input source qualification is complete (Refer to "Input Source Qualification" section)
- Battery charging is enabled by I2C register bit (REG01[5:4]) and /CE is low
- No thermistor fault on TS1 and TS2
- No safety timer fault
- BATFET is not forced to turn off (REG07[5])

When charge is complete and the device terminates the charging cycle if the charge current is below termination threshold (REG03[3:0]). Later on, when the battery voltage gets discharged below recharge threshold (REG05[0]), the bq24190/191/192(192I)/193 automatically starts another charging cycle.
The STAT output indicates the charging status of charging on going (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge and voltage regulation, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host.
The device default settings are listed below.

Default Mode	bq24190/191/192	bq24192I	bq24193
Charging Voltage	4.208V	4.112V	4.208V
Charging Current	2.036A	1.012A	2.036A
Pre-charge Current	256mA	256mA	256mA
Termination Current	256mA	256mA	256mA
Temperature Profile	Hot/Cold	Hot/Cold	JEITA
Safety Timer	8 hours	8 hours	8 hours

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I2C.

Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage.
At the beginning of a charging cycle, the device applies current according to the battery voltage.
When the battery is below batshort threshold, the device applies 100mA to safely bring up the battery voltage. As the battery is out of batshort, the device applies pre-charge current as register setting (REG03[7:4]) till the voltage above the batlowv threshold. During the batshort and batlowv, the BATFET is linearly regulated so that the system is maintained at minimum system voltage. The status register REG08[5:4] is 01.

Though the battery is above batlowv threshold, the device may stay in minimum system regulation and BATFET keeps linearly regulated. As the battery rises above minimum system regulation threshold, the BATFET is getting into full conduction. The system floats slightly above battery considering the V_{DS} of BATFET.
During the whole charging process, the actual charge current may be less than the register setting due to other loop regulations like DPM regulation (See “Dynamic Power Management” section), or thermal regulation (See “Thermal Regulation” section).

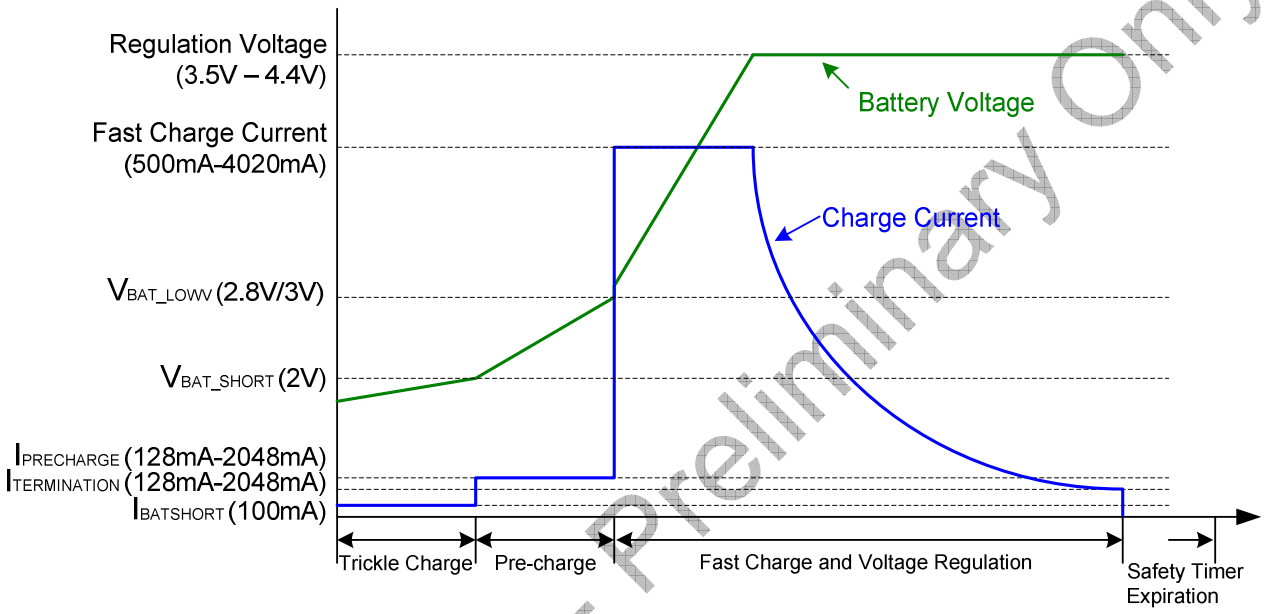


Figure Battery Charging Profile

Thermistor Qualification

The high capacity battery usually has two or more single cells in parallel. The bq24190/191/192(192I) provides two TS pins to monitor the thermistor in each cell independently. The bq24193 applies JEITA profile with TS1/TS2 shorted.

Cold/Hot Temperature Window (bq24190/191/192(192I))

The bq24190/191/192(192I)/193 continuously monitors battery temperature by measuring the voltage between the TS pins and ground. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds. Otherwise, the device suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range.

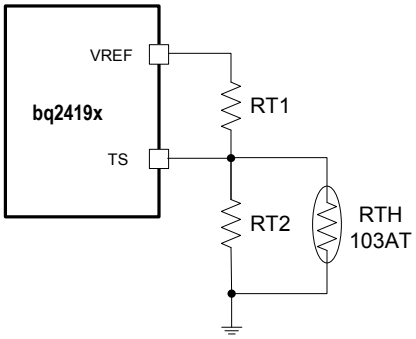


Figure TS Resistor Network

When the TS fault occurs, the fault register REG09[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. The STAT pin blinks when charge is suspended (bq24190/191/192/193) or has a 10k pull down to ground (bq24192I).

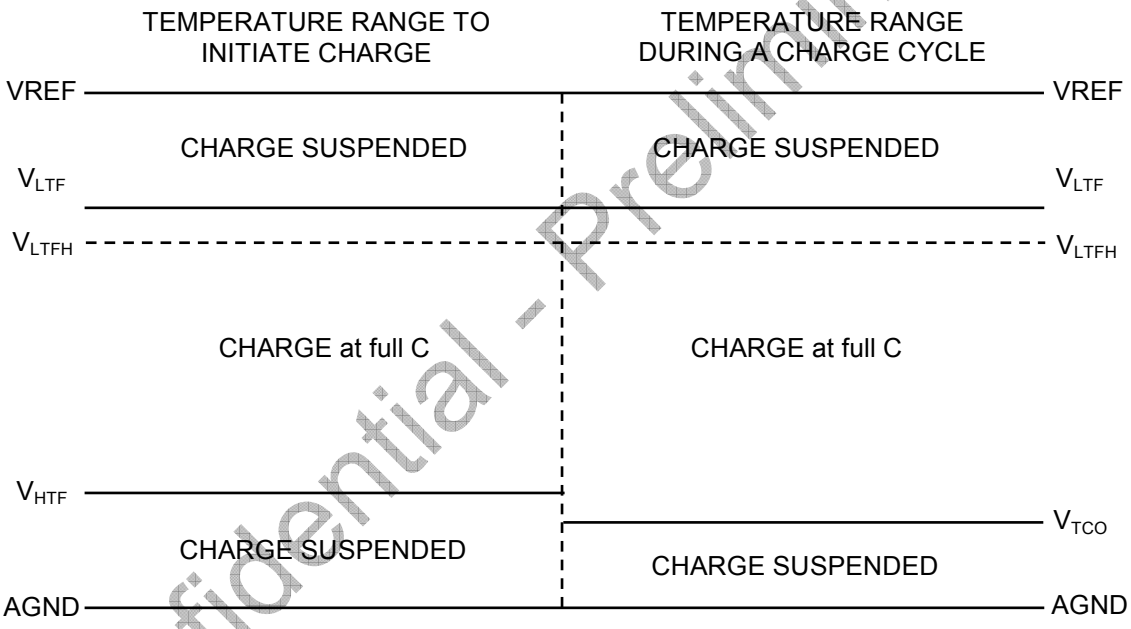


Figure TS pin Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure, the value RT1 and RT2 can be determined by using the following equations:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}} \right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1 \right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1 \right)}$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery,

RTH_{COLD}=27.28KΩ

RTH_{HOT}=4.911KΩ

RT1=5.23KΩ

RT2=30.1KΩ

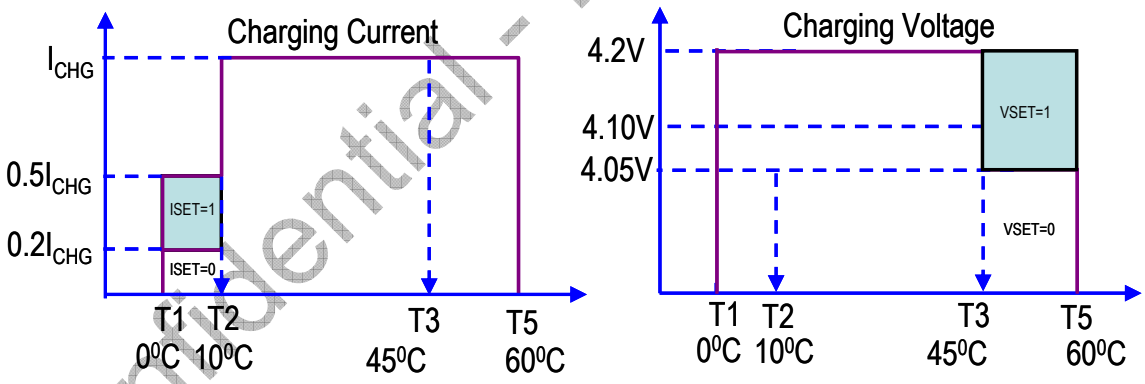
JEITA Guideline Compliance (bq24193)

To improve the safety of charging Li-ion batteries, JEITA and the Battery Association of Japan released new safety guidelines on April 20, 2007. Their guidelines emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the V_{T1} to V_{T5} thresholds. If V_{TS} is outside of this range, the controller suspends charge and waits until the battery temperature is within the V_{T1} to V_{T5} range.

At cold temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1V.

The device also provides flexible settings for warm/cold temperature charging requirement other than JEITA. The voltage setting at warm temperature can keep to 4.2V (REG07 bit[4]), and the current setting at cold temperature can be further reduced to 20% of fast charge current (REG05 bit[0]).



The resistor bias network has been updated as below.

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{VT1} - 1\right)}$$

$$RT1 = \frac{\frac{V_{VREF}}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery,

RTH_{T1}=27.28KΩ

RTH_{T5}=3.02KΩ

RT1=2.27KΩ

RT2=6.86KΩ

Charging Termination

The bq24190/191/192(192I)/193 terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current.

When termination occurs, the status register REG09[5:4] goes 11, and an INT is asserted to the host.

Usually the STAT bit indicates charging complete when the charging current falls below termination threshold. User can write to REG05[6] to enable early “charge done” indication on STAT pin. The STAT pin goes high when the charge current goes below 800mA. The charging cycle is still on-going till the current falls below the termination threshold.

Termination is disabled if the bq24190/191/192(192I)/193 is in input current/voltage regulation or thermal regulation. The user can disable the termination by writing 0 to REG05[7].

Safety Timer

The bq24190/191/192(192I) has safety timer to prevent extended charging cycle due to abnormal battery conditions.

The safety timer is 1 hour when the battery is below batlowv threshold. The user can program fast charge safety timer through I2C (REG05[2:1]). The safety timer feature can be disabled via I2C (REG05[3]).

During input voltage/current regulation or thermal regulation, the safety timer counting at half clock rate since the actual charge current is likely below the preset value. The user can disable this feature by writing 0 to REG07[6].

The safety timer is reset at the beginning of a new charging cycle. It can also get reset by toggle the /CE pin or write 00 and 01 sequentially to the REG01[5:4].

When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host.

Host Mode and Default Mode

The bq24190/191/192(192I)/193 is a host controlled device, but it can operate in default mode with all default settings during host down time. In default mode, the user can use bq24190/191/192(192I)/193 as an autonomous charger with no host or with host in sleep.

After power-on-reset, the device starts in watchdog timer expiration state, or default mode. All the registers are in the default settings. The bq24190 runs the D+/D-detection, and the bq24191/192(192I) checks out the PSEL and OTG/IUSB level, to set the input current limit (Refer to “USB Detection and Input Current Limit Setting” section).

The REG09[7] becomes HIGH after watchdog timer expiration and an INT is asserted.

In default mode, the device keeps charging the battery with 8-hour fast charging safety timer. At the end of the 8 hours, the charge will stop but the switching regulator keeps running to supply the system.

Any write to bq24190/191/192(192I)/193 transits the device from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer regularly by writing 1 to REG01[6] before the watchdog timer expires (REG05 bit[5:4]).

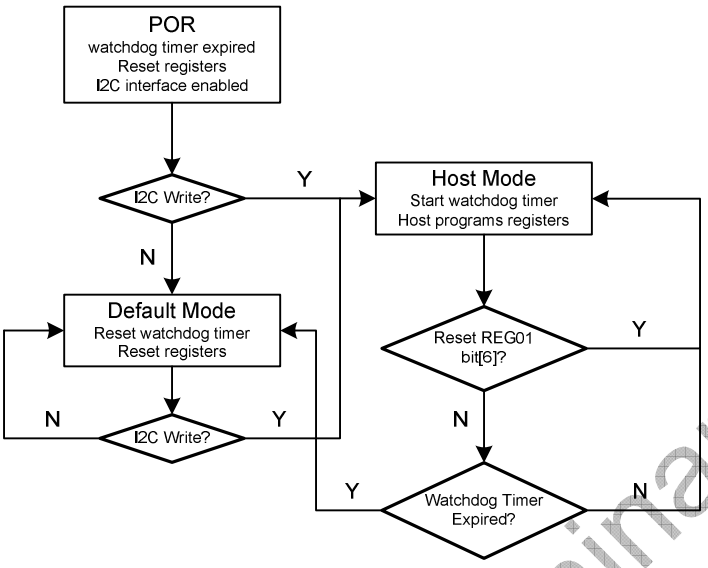


Figure Watchdog Timer Flow Chart

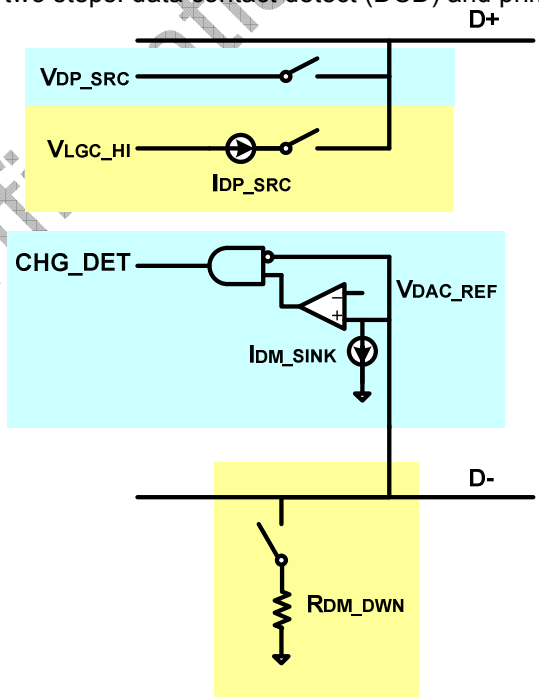
USB Detection and Input Current Limit Setting

The USB ports on personal computers are convenient places for portable devices (PDs) to draw current for charging their batteries. If the portable device is attached to a USB host or hub, then the USB specification requires the portable device to draw limited current (100mA/500mA in USB 2.0, and 150mA/900mA in USB 3.0). In the portable device is attached to a charging port, it is allowed to draw up to 1.5A.

The bq24190 contains a D+/D- based input source detection to program the input current limit during default mode. The user can force D+/D- detection in the host mode by writing 1 to REG07[7].

Every time the input source plugs in to the portable device, and passes the input source qualification, the bq24190 starts D+/D- detection, and the bq24191/192(192I)/193 checks PSEL and OTG/IUSB pin voltage to set the input current limit.

The D+/D- detection has two steps: data contact detect (DCD) and primary detection.



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DCD (Data Contact Detection) detects uses a current source to detect when the data pins have made contact during an attach event. The protocol for data contact detect is as follows:

- PD detects VBUS asserted
- PD turn on D+ I_{DP_SRC} and the D- pull-down resistor
- PD waits for D+ line to be low for a time of T_{DCD_DBNC}
- PD turn off I_{DP_SRC} and D- pull-down resistor

If nothing is attached to the PD, the D+ line stays high.
The primary detection is used to distinguish between and USB host (or SDP) and different type of charging ports (CDP and DCP).
During primary detection, the portable device turns on V_{DP_SRC} on D+ and I_{DM_SINK} on D-. If the portable device is attached to a USB host, the D- is low.
The bq24191/192(192I)/193 has PSEL instead of D+/D-. It directly takes the USB PHY device output to decide whether the input is USB host or charging port.

D+/D- Detection (bq24190)	PSEL (bq24191/192(192I)/193)	OTG/IUSB	Input Current Limit	REG08[7:6]
Fail DCD	-	-	100mA	00
USB Host	HIGH	LOW	100mA	01
USB Host	HIGH	HIGH	500mA	01
Charging Port	LOW	-	1.5A (bq24191/192I) 3A (bq24192/193)	10

There are two operations in USB host 100mA to meet USB specification.
When the input source is 100mA USB host, and the battery is above batgood threshold, the device will enters high impedance state (HIZ) so minimize the quiescent current and meet the current requirement in USB suspend mode. The host can force the device to enter HIZ by writing 1 to REG00[7].
The device keeps battery charging with 100mA USB host for up to 45 mins. Afterwards, it will stop charging and go to HIZ.

DC-DC Converter

As a battery charger, the bq24190/191/192(192I)/193 employs a 1.5MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.
A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.
In order to improve light-load efficiency, the device switches to PFM control at light load when the battery is below minimum system voltage.
In OTG boost mode, the bq24190/192(192I)/193 employs a 1.5MHz step-up switching regulator. At light load, similar to buck operation, the device switches to PFM control to improve efficiency.

Status Outputs (/PG, STAT, and INT)

In bq24191/192(192I)/193, the /PG goes LOW to indicate a good input source when:

1. VBUS above UVLO
2. VBUS above battery (not in sleep)
3. VBUS below ACOV threshold
4. VBUS above 3.8V when 30mA current is applied (not a poor source)

The bq24190/191/192(192I)/193 indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

Charging State	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, TS fault, timer fault, input or system over-voltage)	blinking @ 1Hz (bq24190/191/192/193) or 10k pull down (bq24192I)

In some applications, the host doesn't always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256us INT pulse.

- USB/adapter source identified (through PSEL or DPDM detection, with OTG/IUSB pin)
- Input source becomes good: not in sleep, not in acov, and current limit above 30mA
- Input source becomes bad: in sleep, in acov or current limit less than 30mA
- Charge Complete
- Any FAULT event in REG09

Protections

Input Current Limit on ILIM

For safe operation, the bq24190/191/192(192I)/193 limits maximum input current on ILIM pin. The user connects a resistor from ILIM pin to ground. The input maximum current is set as:

$$I_{INMAX} = \frac{1V}{R_{ILIM}} * 450$$

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3A, and ILIM has a 300Ω resistor to ground for 1.5A, the input current limit is 1.5A. The user can use ILIM to set the input current limit other than the register settings.

The device regulates ILIM pin at 1V. If ILIM voltage exceeds 1V, the device enters input current regulation (Refer to "Dynamic Power Path Management" section).

The voltage on ILIM pin is proportional to the input current. The user can read the ILIM pin voltage to monitor the input current following the equation below:

$$I_{IN} = \frac{V_{ILIM}}{1V} \times I_{IN\_MAX}$$

For example, if the user sets 3A on ILIM pin, and the ILIM voltage is 0.6V, the actual current 1.8A.

If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 1V. If ILIM pin is short, the input current is regulated at the limit sets by the register.

Thermal Regulation and Thermal Shutdown

The bq24190/191/192(192I)/193 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device starts to lower down the charge current. The wide thermal regulation range from 60ºC to 120ºC allows the user to optimize the system thermal performance. During thermal regulation, the status register REG08[1] goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when the IC is overheated with charge current already reduced to zero. The fault register REG09[5:4] goes 10 and an INT is asserted to the host.

Over Voltage/Current Protection in Buck Mode

The bq24190/191/192(192I)/193 provides the voltage limits on input source side and system/battery side, and informs the abnormality the host in time.

In maximum input voltage for buck mode operation is 18V. If VBUS voltage exceeds 18V, the device stops switching immediately to avoid any damage to the IC since the maximum rating is 20V. RBFET turns off as well

and the device enters high impedance mode (HIZ) to minimize the quiescent current. BATFET turns on to supply the system. During input over voltage (ACOV), the status register REG08[2] goes low and the fault register REG09[5:4] will be set to 01. An INT is asserted to the host. The /PG pin in bq24191/192(192I)/193 goes high, indicating the input source is faulty.

The bq24190/191/192(192I)/193 monitors the current in all the integrated MOSFETs and turns off the FETs when an over current condition is detected. The over-current limits protect the device from various fault conditions such as input short, system short, etc.

During the buck mode, the HSFET has cycle-by-cycle over-current limit. At every switching cycle, if the HSFET current exceeds the over-current limit, the HSFET turns off immediately. The HSFET keeps off until the beginning of the next switching cycle.

Over Voltage/Current Protection in Boost Mode

The boost mode regulated output is 5V. Once the output voltage exceeds 5.4V, the bq24190/192(192I)/193 stops switching and the device exits boost mode. During the over-voltage, the fault register REG09[6] is set high to indicate fault in OTG operation. An INT is asserted to the host.

During boost mode, the LSFET has cycle-by-cycle over-current limit. At every switching cycle, if the LSFET current exceeds the over-current limit, the LSFET turns off immediately, and stays off till the end of the cycle.

The device also monitors RBFET current to detect boost mode over current or VBUS short. During RBFET over-current, the boost converter stops switching. When the over current event goes away, the boost converter keeps running.

The over voltage/current faults will be reported to REG09[6] with INT asserted.

If the system is shorted or significantly overloaded so that its current exceeds the over-current limit, the device latches off BATFET. The user has to insert the dc source on VBUS again to reset the latch and turn on BATFET.

Battery Protection

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the converter stops switching and the system load brings down the battery voltage. Meanwhile, the fault register REG09[5] goes high and an INT is asserted to the host.

If the battery voltage falls below 2V, the device immediately turns off BATFET to disable the battery charging or supplement mode. 1ms later, the BATFET turns on and charge the battery with 100mA current. The device does not turn on BATFET to discharge a battery that is below 2.5V.

Serial Interface

The bq24190/191/192(192I) uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C^{TM} is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH (bq24190/192(192I)/193), or 6AH (bq24191), receiving control inputs from the master device like micro controller or a digital signal processor. The I2C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

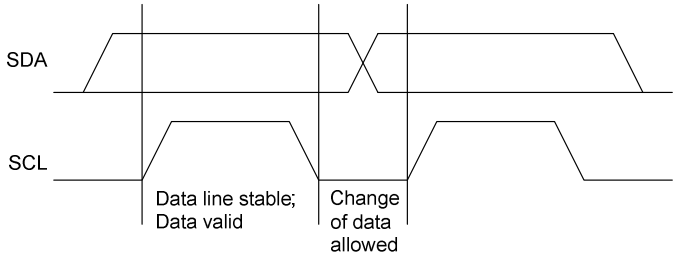


Figure Bit Transfer on the I2C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

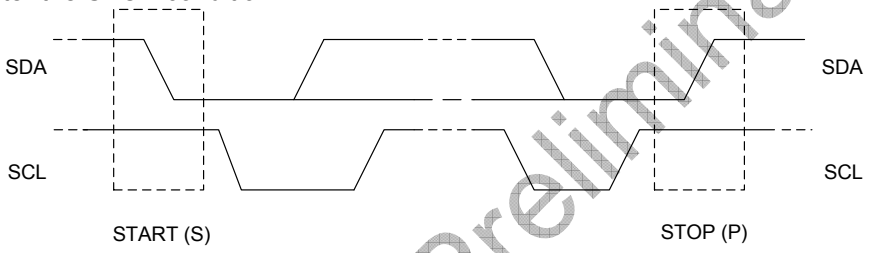


Figure START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

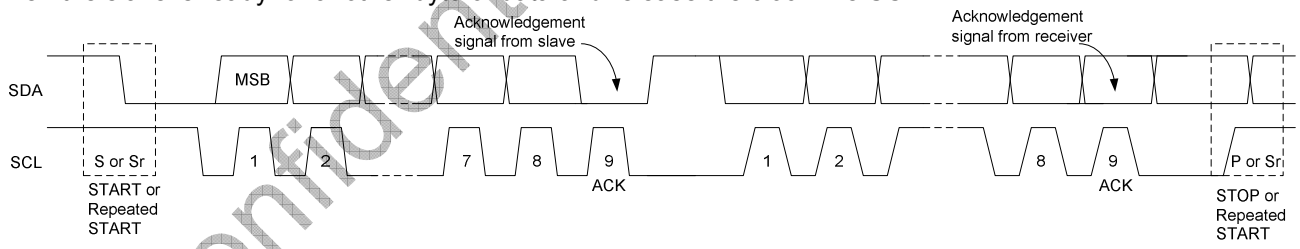


Figure Data Transfer on the I2C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

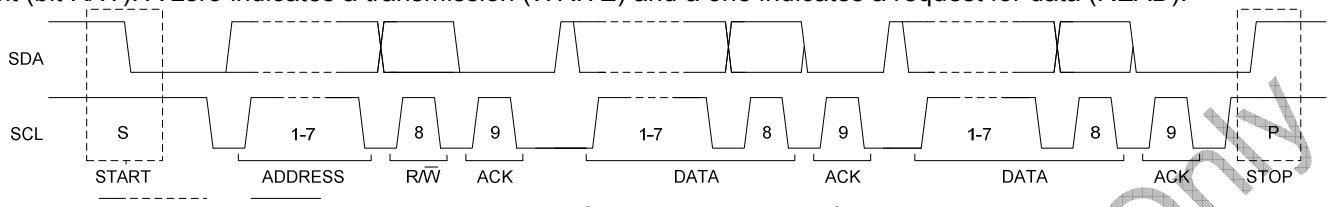


Figure A Complete Data Transfer

PCB Layout

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 24) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the QFN information, refer to SCBA017 and SLUA271.

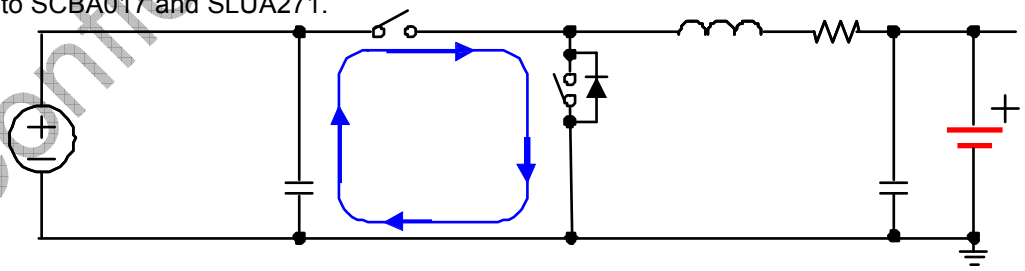
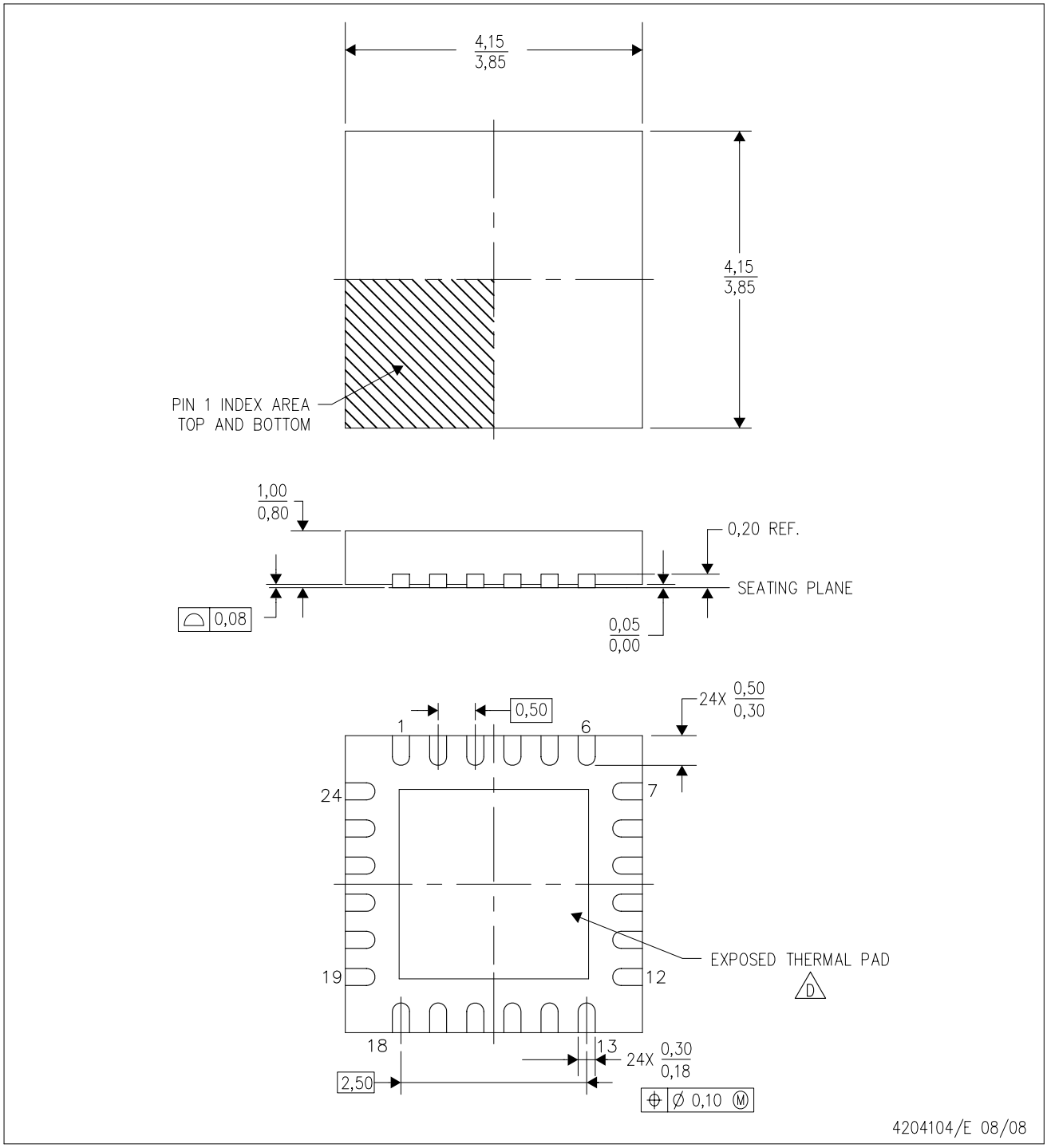


Figure High Frequency Current Path

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

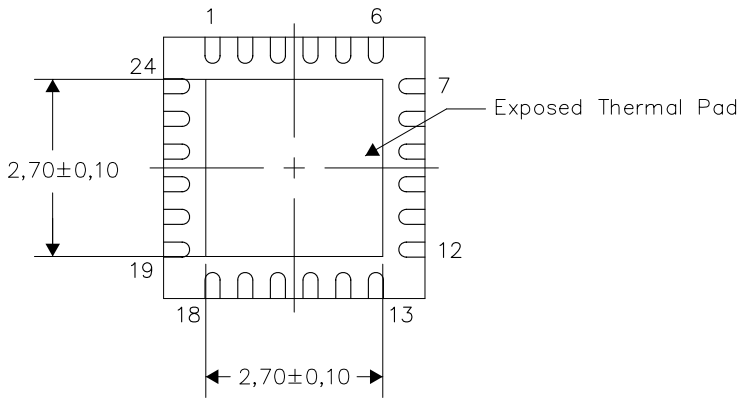
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



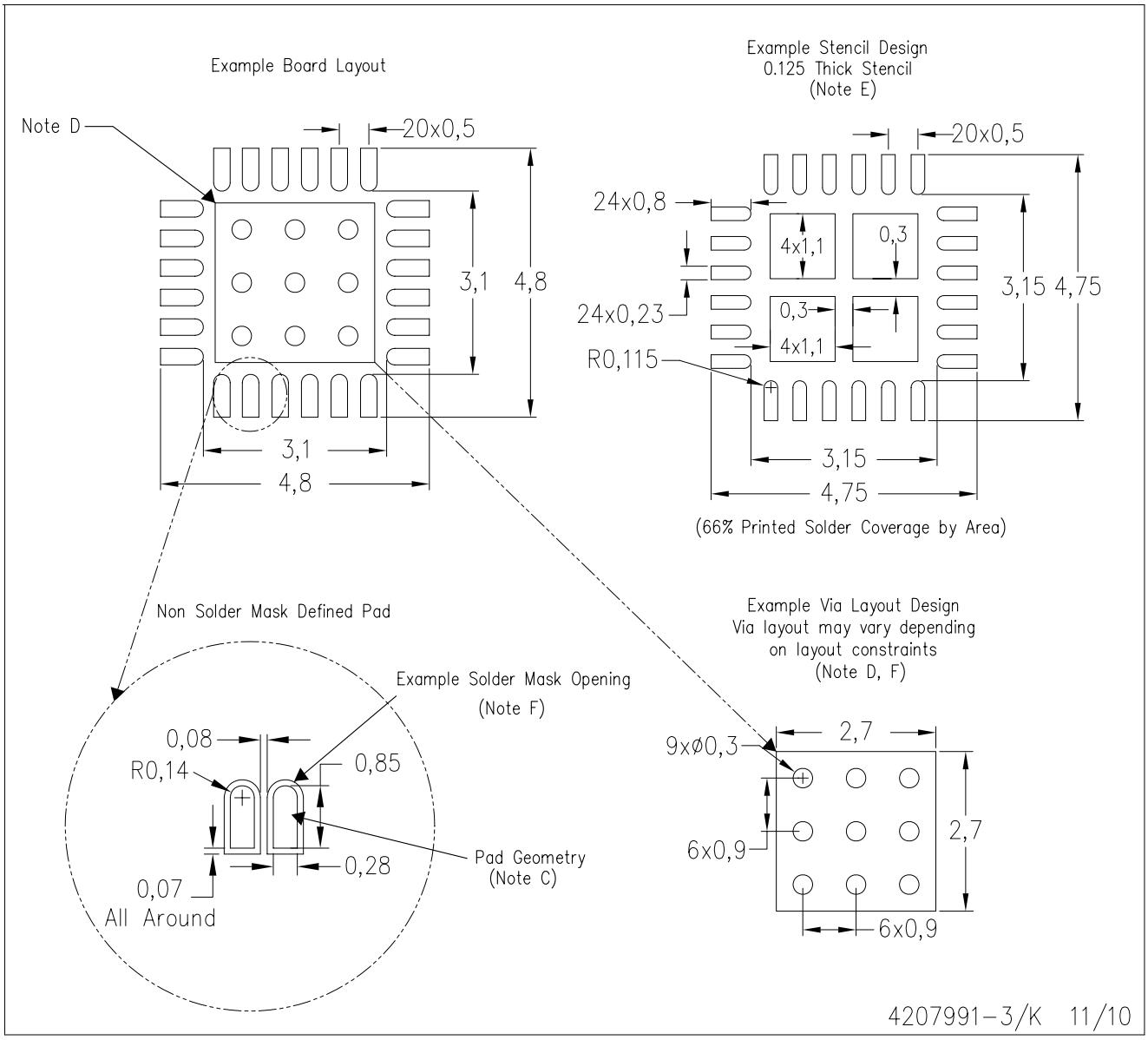
Bottom View

Exposed Thermal Pad Dimensions

4206344–4/W 01/11

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

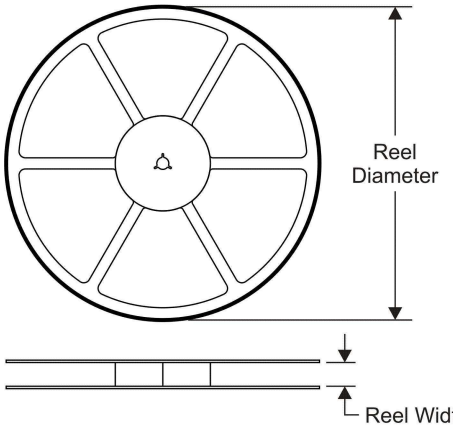
PACKAGING INFORMATION

Orderable Device	Status (1)	Pack Type	Pack Drawing	Pins	Pack Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)
bq24190RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
bq24190RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
bq24191RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
bq24191RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
bq24192RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
bq24192RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

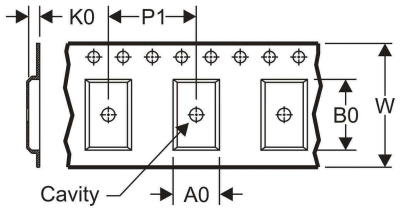
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
(2) Eco Plan -The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) -please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and lead frame. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
(3) MSL, Peak Temp. --The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

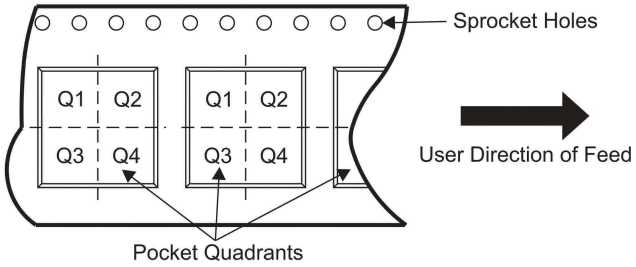


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

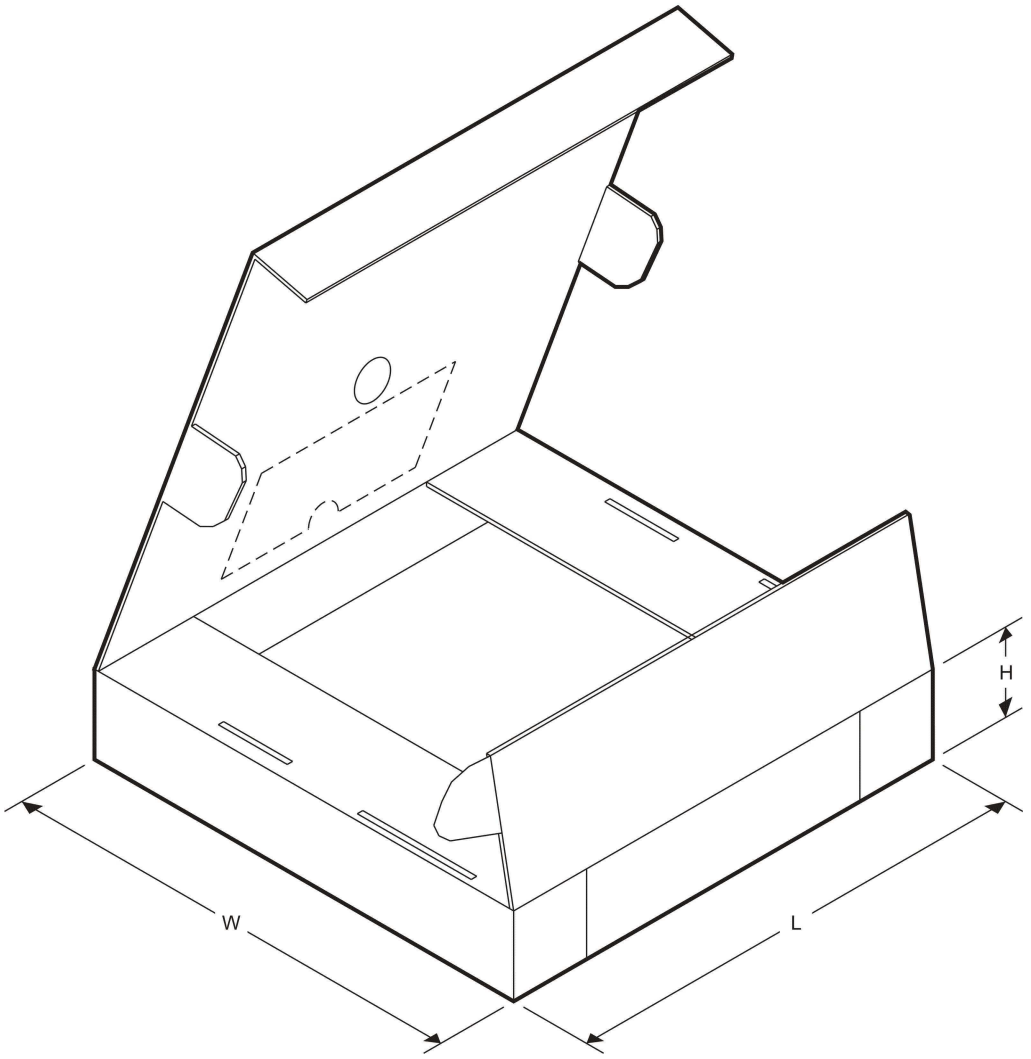
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
bq24190RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
bq24190RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
bq24191RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
bq24191RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
bq24192RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
bq24192RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
bq24190RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
bq24190RGET	VQFN	RGE	24	250	190.5	212.7	31.8
bq24191RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
bq24191RGET	VQFN	RGE	24	250	190.5	212.7	31.8
bq24192RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
bq24192RGET	VQFN	RGE	24	250	190.5	212.7	31.8