

# Lecture11 & IC\_Compiler: Quiz

**Due** Nov 19 at 11:55pm**Points** 8**Questions** 8**Available** Nov 12 at 10:05am - Nov 19 at 11:59pm**Time Limit** 11 Minutes

This quiz was locked Nov 19 at 11:59pm.

## Attempt History

	Attempt	Time	Score
LATEST	<a href="#">Attempt 1</a>	11 minutes	7.75 out of 8

⚠ Correct answers are hidden.

Score for this quiz: **7.75** out of 8

Submitted Nov 19 at 8:49pm

This attempt took 11 minutes.

### Question 1

**1 / 1 pts**

You are working for Hughes Avionics making the fly by wire system (will control the flight surfaces like ailerons, flaps, rudder, ...) for the next generation fighter jets. Only a few thousand of these will be made. The best choice is.

☒ Standard Cell for reliability reasons.

Correct...even though the volume can't justify the NRE of a standard cell design, it is a mission critical operation. An FPGA has configuration reboot time, and has so many SRAM cells that it is more vulnerable to alpha particle strikes (which will be more common in the thin atmosphere of high altitude flight).

☐ Full custom because it has to be the highest performance possible



FPGA because the volumes are too low to justify the NRE of Standard Cell or Full Custom

Partial

## Question 2

0.75 / 1 pts

The basic building blocks of a FPGA are CLBs and the LUT is in turn a basic building block of the CLB . All of this wonderful flexibility is configured by Tedious boolean algebra

Answer 1:

CLBs

Answer 2:

LUT

Answer 3:

CLB

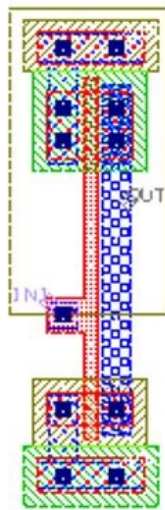
Answer 4:

Tedious boolean algebra

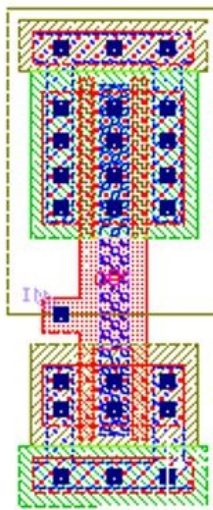
## Question 3

1 / 1 pts

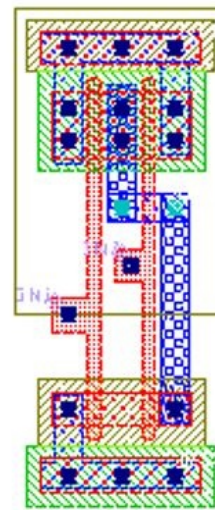
Match the labeled standard cell layout to what they represent.  
Remember a NAND has series N-MOS devices. A NOR has series P-MOS devices.



A



B



C

Cell A represents Standard size inverter

Cell B represents A 4X size inverter

Cell C represents A NAND gate

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**Answer 1:**

Standard size inverter

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**Answer 2:**

A 4X size inverter

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**Answer 3:**

A NAND gate

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**Question 4**

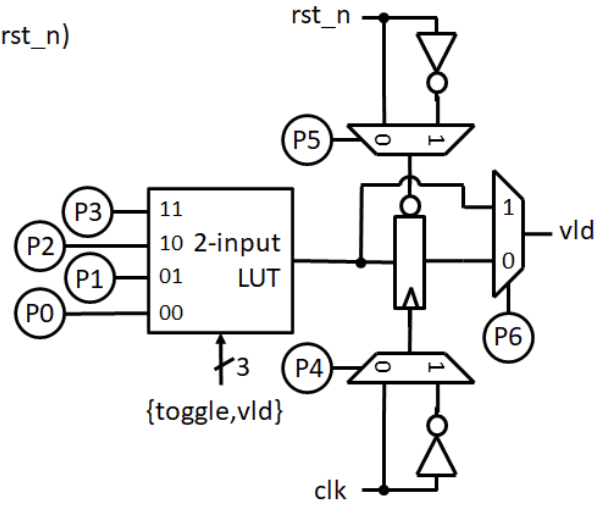
**1 / 1 pts**

```

always @(negedge clk, negedge rst_n)
  if (!rst_n)
    vld <= 1'b0;
  else if (toggle)
    vld <= ~vld;

```

Each  $P_x$  represents an SRAM cell to be configured by Quartus. Indicate the contents of each cell to implement the verilog shown



P0 = 0 , P1 = 1

P2 = 1 , P3 = 0

P4 = 1 , P5 = 0 , P6 = 0

**Answer 1:**

0

**Answer 2:**

1

**Answer 3:**

1

**Answer 4:**

0

**Answer 5:**

1

**Answer 6:**

0

**Answer 7:**

0

**Question 5****1 / 1 pts**

Custom Logic is more rare these days because The cost of transistors has fallen to the point where a more efficient design is not worth the extra man hours of custom .

**Answer 1:**

The cost of transistors has fallen to the point where a more efficient design is not worth the extra man hours of custom

The human is still better but the APR tool is so much quicker and cheaper than the human that it is not worth it to use humans in most instances. Transistors are dirt cheap these days, so area efficiency be damned.

**Question 6****1 / 1 pts**

The script **setup\_apr.icc** should be:



Sourced from within IC\_Compiler to let it know where all the technology files are



Sourced only once at the linux prompt



Sourced every time at the linux prompt before you launch IC\_Compiler



Sourced when you are finished with the design to output the collateral files

**Question 7****1 / 1 pts**

The instructor says a lot of confusing things . Like to become and expert in IC\_Compiler one has to spend a lot of time behind the wheel . If you do you will become a tool jockey . This does not make sense because horses do not have steering wheels .

**Answer 1:**

a lot of confusing things

**Answer 2:**

IC\_Compiler

**Answer 3:**

time behind the wheel

**Answer 4:**

tool jockey

**Answer 5:**

horses do not have steering wheels

**Question 8****1 / 1 pts**

It is important that adjacent metal layers be routed orthoganal . For our

9-layer metal process we will use M5 and below for APR preserving higher metals for global distribution of clock, reset, and power .

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**Answer 1:**

adjacent metal layers

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**Answer 2:**

routed orthoganal

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**Answer 3:**

9-layer metal process

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**Answer 4:**

M5 and below for APR

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**Answer 5:**

higher metals for global distribution of clock, reset, and power

Quiz Score: **7.75** out of 8