Lecture09&10Quiz

Due Nov 12 at 11:55pm **Points** 8 **Questions** 8
Available Nov 5 at 9:55am - Nov 12 at 11:59pm **Time Limit** 11 Minutes

This quiz was locked Nov 12 at 11:59pm.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	11 minutes	7.42 out of 8

ⓘ Correct answers are hidden.

Score for this quiz: **7.42** out of 8
Submitted Nov 12 at 10:17pm
This attempt took 11 minutes.

Partial

Question 1 — 0.67 / 1 pts

Which of the following are technology independent *(independent of cell library)* steps of synthesis optimization?

- [ ] Upsizing gate for more drive strength
- [ ] Using an adder/subtractor block for a mutually exclusive add vs subtract operation.
- [x] Choosing a CLA topology over a RCA topology
- [ ] buffering a signal on a critical path
- [x] sharing common boolean terms when forming two or more signals

Partial

Question 2

0.75 / 1 pts

Match the pre-compile synthesis step with either analyze or elaborate.

unroll loops	elaborate step
syntax checking	analyze step
check against synthesizeable constructs	analyze step
create initial structural representation in GTECH library	elaborate step

Question 3

1 / 1 pts

The code shown below synthesizes to:

```
reg [1:0] sel;

always @(a,b)
  if (a) sel = 2'b00;
  else if (b) sel = 2'b01;
  else sel = 2'b10;

always @(posedge clk)
  if (sel==2'b11) out <= ~(c & d);
  else out <= ~(c | d);
endmodule
```

- It does not synthesize, can't have an "if" inside a @(posedge clk) statement

It synthesizes to 2:1 mux feeding into a flop. The "sel" logic of the flop is combinational based on "a" and "b".

It synthesizes to a flop and a NOR gate

It will result in a 2-bit wide latch for "sel" and a flop for out.

Due to the unreachable state of **sel** being 11 it simplifies to a flop and a NOR gate.

Question 4

1 / 1 pts

In the context of lecture10 the acronym SWAG stands for: [SWAG]

Sophisticated Wild Ass Guess

Stuff We All Get

Stolen Without A Gun

Special Warfare Action Group

Stuff We Ain't Getting

Some Women Are Great

Still Without A Girlfriend

Sold Without A Gaurantee

Students Working to Achieve Greatness

- Sold Without Any Guarantee
- Still Wondering And Guessing
- Simulated Wire And Gate

Question 5

1 / 1 pts

They are called parasitic capacitances because they are both unavoidable and undesirable . There is capacitance between Eric's guts and the conductors in his laptop .

Answer 1:

unavoidable

Answer 2:

undesirable

Answer 3:

Eric's guts

Answer 4:

the conductors in his laptop

Question 6

1 / 1 pts

Check all statements regarding a parasitic extraction tool:

- It removes the parasitics

- [ ] It optimizes the layout of the circuit to reduce the parasitics
- [x] It determines the value of the parasitic capacitances
- [ ] It uses a Newton-Raphson algorithm
- [x] It uses a field solver
- [x] It cannot change the laws of physics

Question 7

1 / 1 pts

Eric's first manager at Intel was an idiot because he thought parasitic capacitances should be removed

Answer 1:

first manager at Intel

Answer 2:

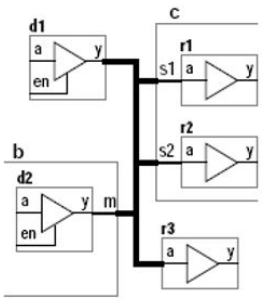
an idiot

Answer 3:

he thought parasitic capacitances should be removed

Question 8

1 / 1 pts



Example

```
(INSTANCE top)
(DELAY
  (ABSOLUTE
    (INTERCONNECT  d1.y   c.r1.a (0.01:0.02:0.03))
    (INTERCONNECT  d1.y   c.r2.a (0.03:0.04:0.05))
    (INTERCONNECT  d1.y   r3.a   (0.05:0.06:0.07))
    (INTERCONNECT  b.d2.y c.r1.a (0.04:0.05:0.06))
    (INTERCONNECT  b.d2.y c.r2.a (0.02:0.03:0.04))
    (INTERCONNECT  b.d2.y r3.a   (0.02:0.03:0.04))
  )
)
```

The flight time (wire delay) of the interconnect from the output of gate **d2** to the input of gate **r1** is: is 0.05ns in the typical case .

Answer 1:

is 0.05ns in the typical case

Quiz Score: **7.42** out of 8