ECE 551
Digital Design And Synthesis

Fall ‘23

Final Exam Review

Administrative Matters

- Friday 12/21 at 12:25PM
  - Microbial Sciences 1520
  - 1:45 duration
- Can have an 8.5x11 cheatsheet.
  - The act of making a cheatsheet is actually a good way to study.

How Best to Study

- Review Lecture Slides
  - Focus on Lectures 8 - 12
  - Project stuff too
- Something you don't understand?
  - Reference the video for that section
  - Study First…then look at practice exam
- Look over the video quizzes. Perhaps the questions there hit topics I considered important.
- Look over verilog you wrote for HW/exercises.

Tasks and Functions

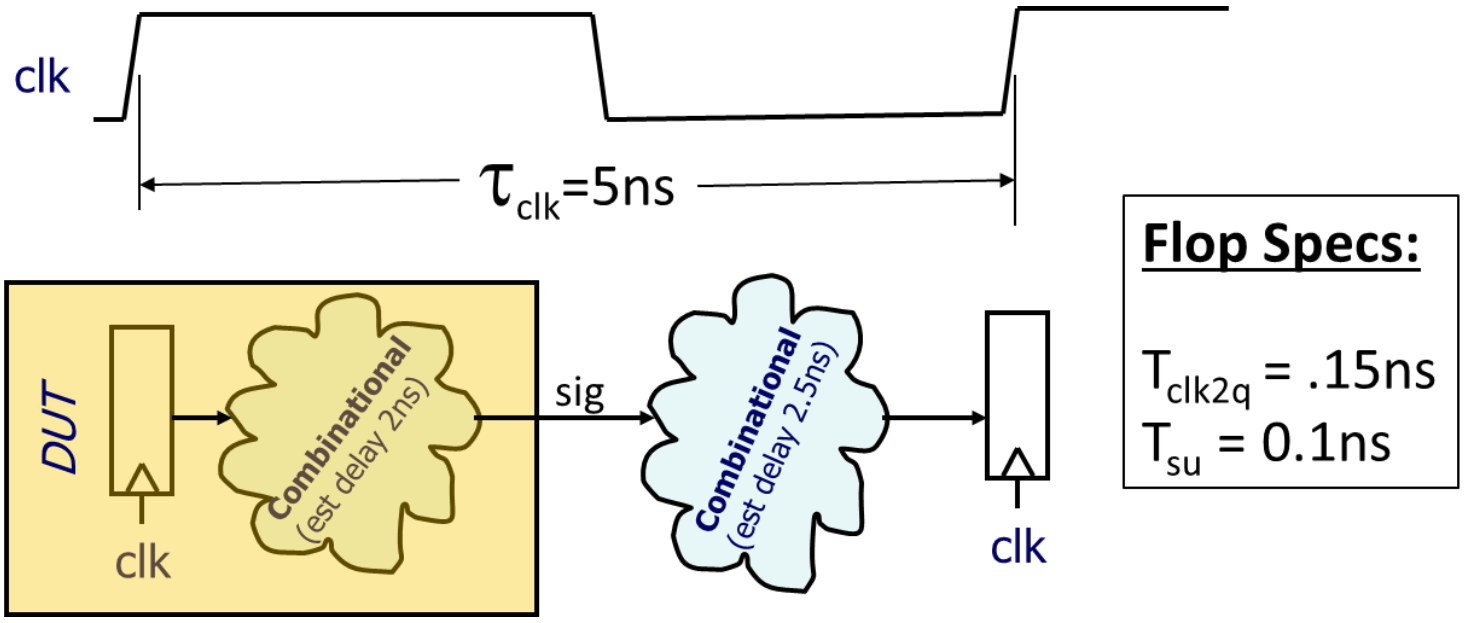
- Properties of each
- Basic syntax
- Could you write a task or function if I asked you to?
- How would a task:
  - Pass a “live” version of a signal to a task
  - Access global signals?
  - Access signals inside a child
  - Perform a self check

Synthesis

- Know your synthesis constraints
  - How do you constrain an input
  - How do you constrain an output
  - How do you constrain frequency
  - What are some of the other constraints we used? What is their purpose?
- What does Synopsys do if not meeting timing
- Timing
  - Hold time & hold time fixing
  - max_transition time
  - wireload model

Constraints (telling Synopsys what it doesn't know)

- Create output delay statement for your DUT



Other

- How code would synthesize
- Some basics from lecture12
  - Definitions Terms (not much diff than VQ12)
- FPGA implementation *(basic LUT & config understanding)*
  - FPGA vs IC vs uController *(advantages…when to use which)*
- Gated clocks
  - Advantages/disadvantages
  - Why the latch
  - Could you code a gate clock?
  - Power savings specifics

Static Timing Analysis

- Analyze a circuit
  - Both from max & min delay perspective
  - Analyze a clock tree
    - ✓uncertainty
    - ✓Insertion delay
  - Effect of clock uncertainty on STA
    - ✓Effect on max delay
    - ✓Effect on min delay
- Interpret a Synopsys timing report

Synthesis Constraints

- Understand all the constraints and **why** we need them
  - Clock period
  - Input delay/output delay (and how to specify)
  - Set input drive
  - Set output load
  - Max_transition?
  - Wireload model
- Other Synthesis commands
  - Flattening
  - Generating output reports and .vg netlist

Synthesis continued

- Generate statements
  - When appropriate when not
- Loops in synthesis
  - What can synthesize and what cannot
- Coding for optimization
  - Use of don’t cares
  - Arithmetic block sharing
  - Late arriving signals
  - Avoiding latches

Project Stuff

- Do you know the basics of what you made
  - Its behavior
  - How to write a basic test for it
  - Synthesis difficulties
  - Common errors/bugs

Testbench

- Fork/Join
- Named Blocks
- Disable of blocks
- Assertions
  - Immediate *(not all that awesome)*
  - Concurrent *(new capability in SV. Can be powerful)*
- Using a package
- Including a file (tb_tasks)

Other Things to Know

- It will be a large packet of paper type exam like the midterm. Short answer, you write code, you show how code would synthesize, …

- There is a practice exam (& solution) posted.