Lecture06Quiz

Due Oct 15 at 11:55pm **Points** 8 **Questions** 8
Available Oct 8 at 9:55am - Oct 15 at 11:59pm **Time Limit** 11 Minutes

This quiz was locked Oct 15 at 11:59pm.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	9 minutes	8 out of 8

ⓘ Correct answers are hidden.

Score for this quiz: **8** out of 8
Submitted Oct 15 at 10:15pm
This attempt took 9 minutes.

Question 1 — 1 / 1 pts

In the synthesis demonstration of the multiply accumulate what lessons/scenarios were covered:

- [x] The initial synthesis was with a 2ns clock
- [x] The area only increased slightly when the clock period was reduced to 1.5ns
- [ ] The area increased substantially when the clock period was reduced to 1.5ns

- [ ] Eric seemlessly showed us -help for set_clock_uncertainty
- [x] Eric stumbled a bit, but eventually showed -help for set_clock_uncertainty
- [ ] after setting a clock skew one simply had to re-compile to fix hold times
- [x] after setting a clock skew a re-compile did not fix hold times
- [x] setting a clock uncertainty made the design larger.
- [ ] setting the clock uncertainty did not change the size
- [ ] setting the clock uncertainty made the design smaller
- [x] the number of combinational cells was initially 6
- [ ] the number of combinational cells was initially 425

Question 2

1 / 1 pts

You are a unit owner on a design team and trying to come up with your initial synthesis constraints. A batch of your outputs go to the DMA unit. You speak to the unit designer of the DMA unit and they tell you all those inputs *(your outputs are their inputs)* go straight into flops. This will make your job easier , because almost all the clock period is available for your logic and coming up with your output delay constraint is simple...it is just setup time of flops from your library .

Answer 1:

easier

Answer 2:

almost all the clock period is available for your logic

Answer 3:

simple...it is just setup time of flops from your library

Question 3

1 / 1 pts

Small area and low power often go together. true

Fast speed and low area often do **not** go together. true

Power consumption in CMOS mainly comes from. charging and discharging capacitance

Answer 1:

true

Answer 2:

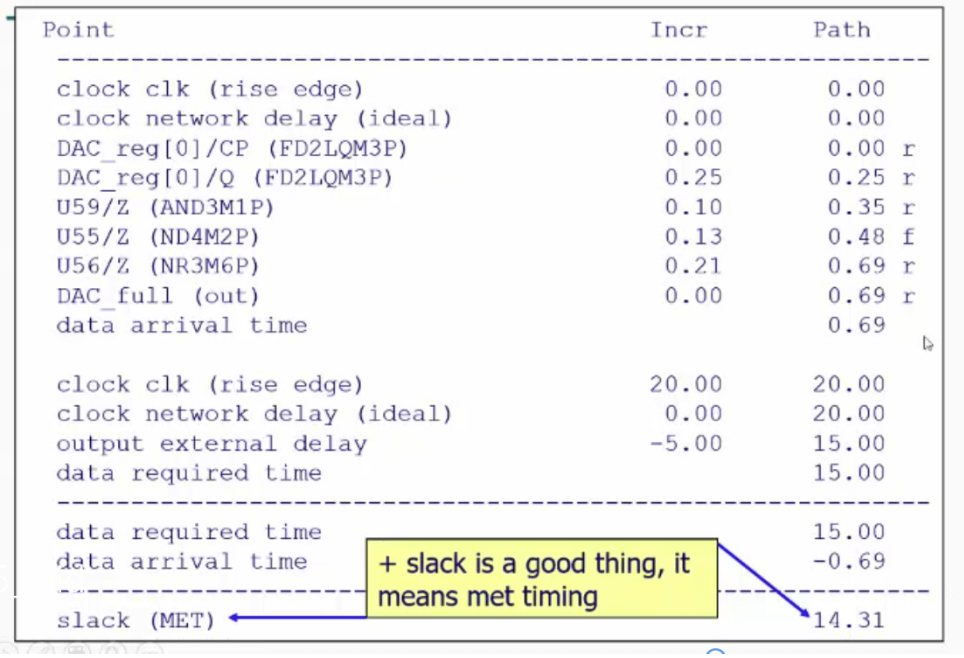
true

Answer 3:

charging and discharging capacitance

Question 4

1 / 1 pts



This timing report is for max delay

The clk2q delay of the flop in this path is: 0.25ns

The approx delay of a 3-input NOR gate in this library is: 0.21ns

The clock period used to constrain this synthesis run was: 20ns

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Answer 1:

max delay

Answer 2:

0.25ns

Answer 3:

0.21ns

Answer 4:

20ns

Question 5

1 / 1 pts

For small to medium size designs like we do in this class the best compile methodology/strategy is top down compile . For really large designs you might use a bottom up compile strategy, but the biggest pain with this is developing constraints for each lower level unit

Answer 1:

top down compile

Answer 2:

bottom up compile

Answer 3:

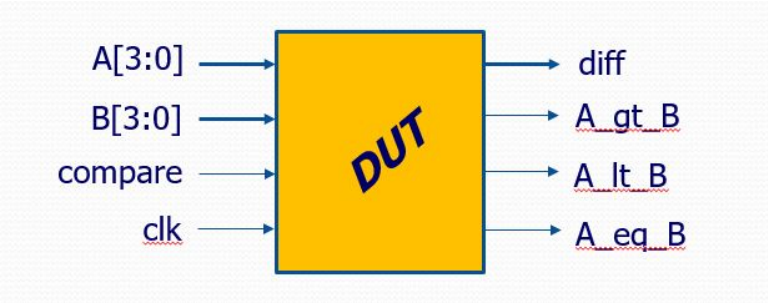
developing constraints for each lower level unit

Question 6

1 / 1 pts

For the design shown below, what would be the output for the design_compiler statement:

remove_from_collection [all_inputs] [find port clk]



- {diff, A_gt_B, A_lt_B, A_eq_B}

- No meaningful output, that is not a valid design compiler command
- {A, B, compare}
- {A,B,compare,clk}
- {}

Question 7

1 / 1 pts

Which of the following factors contribute to clock skew:

- [x] On die variation in dielectric thicknesses
- [ ] Incomplete knowledge about how many flops are on each branch of the clock tree
- [x] on die variation in junction doping densities
- [x] on die variations of junction temperature (some parts of chip will be hotter than others)

Question 8

1 / 1 pts

Synopsys gets an estimate of power consumption of your design using the following formula:

- P = I * V
- P = I^2 * R

- P = (1/2)m*V^2
- (selected) P = C*V^2*f
- P = m*c^2

Quiz Score: **8** out of 8