Running ModelSim Command Line:

1) Compiling the Verilog
   a) From the command prompt run 'vlog'.
      i) `%vlog -work work ring.v ring_tb.v`
      ii) In this example we are compiling two Verilog files in our design (ring.v & ring_tb.v) into a ModelSim library called 'work'.
2) Run the Verilog
   a) From the command prompt run 'vsim'
      i) `%vsim -c work.ring_tb`
      ii) Note that ring_tb is the module name for the top level test bench I will be running.
   b) Actually kick off the Verilog simulation from the ModelSim command prompt with:
      i) `%run -all`

Simple "do file" method:

Create a simple 3-line file <doFile>.do with the following:

```
vlog -work work Verilog_file1.v [Verilog_file2.v] [Verilog_file3.v] …
vsim work.<toplevel_module_name>
run -all
```

Then execute this do file from the command prompt

%vsim –c –do <doFile>.do

Better yet….create a python or perl script to run it.