ECE 551

Digital Design And Synthesis

Fall '21

Parasitic Capacitance
SDF & Back Annotation

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Administrative Matters

- HW5 is assigned and due Mon Nov 22nd
  - Most of it is as team, but prob 1 & 2 are individual

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Capacitance is Unavoidable

- Any two conducting geometries separated by an insulator will have capacitance between them.

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d}$$

- In digital circuits capacitances slow the circuit down.

$$Q = CV = \int I(t)$$

- Time to charge a capacitance C to a voltage V is proportional to C.

$$\int I(t) \approx I \bullet t$$

More cap ➔ Slower charge up

$$t \approx \frac{CV}{I}$$

Unavoidable & Undesireable:

Any questions on why we call it parasitic capacitance?

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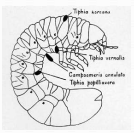
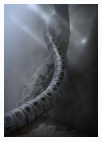
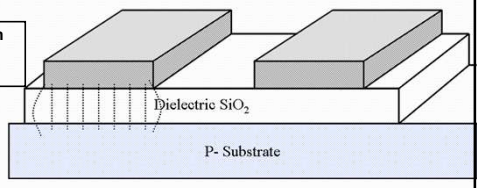
What do Our Parasitics Look Like?





Wisconsin's most prevalent

No…I meant on an integrated circuit



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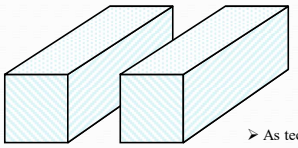
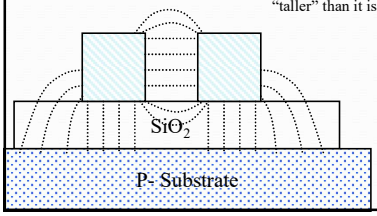
Modern Processes Are Worse



- As the spacing shrank the height did not shrink, or even grew to try to recoup some of the conductance lost by narrowing the line.
- As technologies scaled smaller the aspect ratio of the wires changed. Typical wire is now "taller" than it is wide.



- Fringe components and line to line components now dominate. Parallel plate is a small percent of the total cap.

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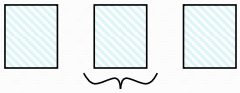
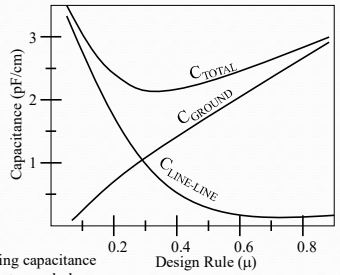
Cap to ground & Cap to neighbors



This graph is for the middle conductor "sandwiched" between two other conductors at minimum spacing.



- Not only is this sidewall and fringing capacitance brining the total cap higher, but it creates a whole new noise problem called cross-talk due to the line to line capacitances.

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How do we Simulate this Effect?

- Synopsys Doesn't Have a Clue
  - Sad reality is wireload model is a S.W.A.G.
  - Might as well go ask the local fortune teller if your circuit is going to work
- Need to extract the value of parasitic capacitance from actual layout of the circuit.
  - Since parasitics are dominated by wiring, the wiring has to be routed to extract it.
  - Need to perform APR first!

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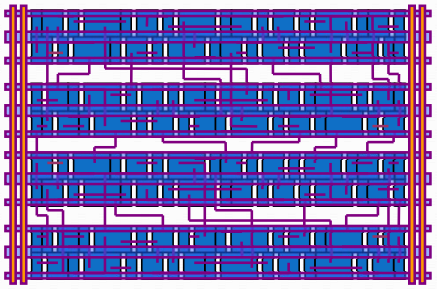
- **What is an APR (Auto Place & Route) Block?**
  - Netlist mapped to standard logic cells (from synthesis tool) is read into a CAD tool.
  - Standard Cells (typically of a fixed height) are placed by an automated program in cell rows **(Place)**
  - Then they are interconnected **(Route)**



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What is a Parasitic Extractor

- Does it remove the parasitics?
  - Quit asking stupid questions…"I cannot change the laws of physics Captain"
- No, it just reads all the geometries of the interconnecting and overlapping metal layers that wire up the standard cells in the APR blocks
- It analyzes these geometries and **extracts the value** of the parasitic capacitances

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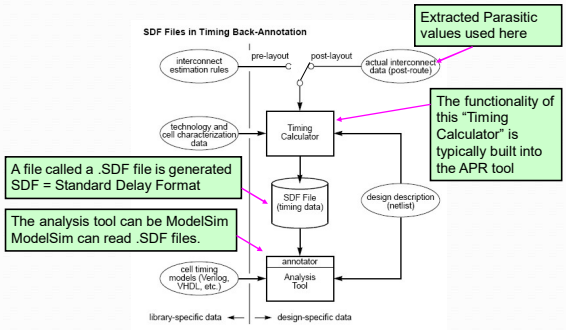
What is Done with These Values?



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Post Layout Simulation

- This whole process of analyzing with extracted parasitics is often referred to as "back annotation"
- Back annotation of parasitics can be to dynamic or static timing analysis tools
  - Static timing analysis tools are like what Synopsys does
    - Timing reports like Synopsys shows for max and min paths
    - NanoTime (also a Synopsys tool) is a really good static timing analysis tool
  - ModelSim can accept .SDF files for back annotation of parasitics.
    - Now you would re-run some/all of your tests with this timing back annotated. (This is dynamic simulation)

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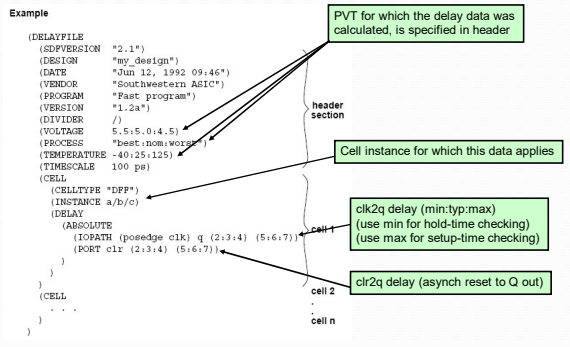
What Does This SDF File Look Like?



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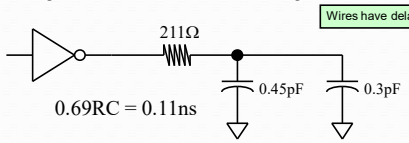
Parasitics Don't Just Slow Down Cells

➢ Resistance:
- When Rdriver >> Rwire then it is not useful to look at interconnect in terms of RC. Lumped capacitance works fine.
- Now that chips are larger and drivers are faster these RC components become significant.

➢ Consider a 2000µ M2 line at 0.18u wide. The route it self has a 0.45pF capacitance. It drives a 0.3pF load. The resistance M2 = 19mΩ/sq.

Wires have delay too…RC Delay



If your targeting 1GHz this is over 10% of your period

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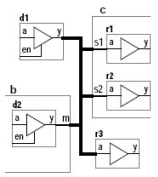
SDF Can Handle Wire RC Delay Too



Example

```
(INSTANCE top)
(DELAY
  (ABSOLUTE
    (INTERCONNECT  d1.y   c.r1.a (0.01:0.02:0.03))
    (INTERCONNECT  d1.y   c.r2.a (0.03:0.04:0.05))
    (INTERCONNECT  d1.y   r3.a   (0.05:0.06:0.07))
    (INTERCONNECT  b.d2.y c.r1.a (0.04:0.05:0.06))
    (INTERCONNECT  b.d2.y c.r2.a (0.02:0.03:0.04))
    (INTERCONNECT  b.d2.y r3.a   (0.02:0.03:0.04))
  )
)
```

- The timing calculation tool can calculate RC delays of intecconnects between cells.
- It uses both the extracted parasitic capacitance data, as well as extracted resistance data.
- SDF file has an INTERCONNECT delay specifier

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How Do I Use SDF with Verilog?

- Back annotate SDF to your post-synthesis (gate level) netlist simulation.
  - Now you will be simulating with accurate timing
  - Simulate your test suite (or a least a large fraction of it)
    - Simulate at typical delays to sanity check the whole environment
    - Simulate at max delays to stress setup times
    - Simulate at min delays to stress hold times
- Verilog contains a directive: **$sdf_annotate** to control .SDF back annotation.

```
$sdf_annotate ("sdf_file" [ , [ module_instance ] [ , [
"config_file" ]
[ , [ "log_file" ] [ , [ "mtm_spec" ]
[ , [ "scale_factors" ] [ , [ "scale_type" ] ] ] ] ] ] );
```

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How Do I Use SDF with Verilog?

Example: Your APR tool created 3 separate files for max/typ/min delays of your digital core (dig_core). (sss=slow,slow,slow PVT), (fff=fast,fast,fast PVT)

Inside the testbench code you apply the SDF to the instance of the digital core. You have 3 such **$sdf_annotate** lines and just comment out the ones you are not simulating.

```
module testbench();

// $sdf_annotate("~ehoffman\verilog\dig_core_sss.sdf",testbench.idig_core);
$sdf_annotate("~ehoffman\verilog\dig_core_fff.sdf",testbench.idig_core);
// $sdf_annotate("~ehoffman\verilog\dig_core_typ.sdf",testbench.idig_core);

dig_core idig_core(.clk(clk), .por_n(por_n), .dst(dst), …
   .
   .
   .
endmodule
```

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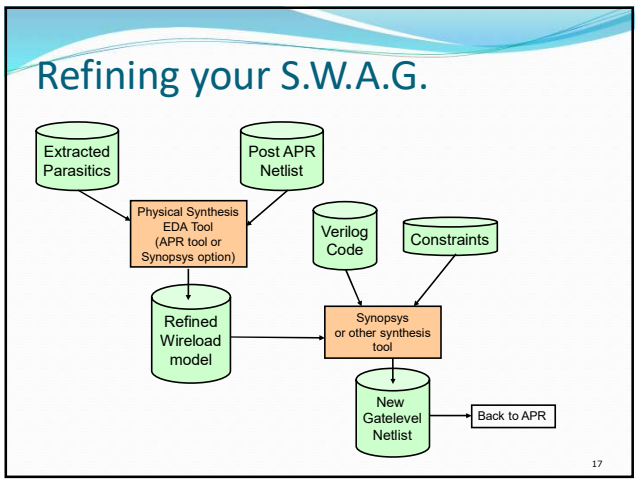
Refining your S.W.A.G.
Extracted Parasitics
Post APR Netlist
Physical Synthesis EDA Tool (APR tool or Synopsys option)
Verilog Code
Constraints
Refined Wireload model
Synopsys or other synthesis tool
New Gatelevel Netlist
Back to APR
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