Syllabus for ECE 551 Digital System Design & Synthesis

1. **ECE 551 Digital System Design & Synthesis**
2. **3 credits and 37.5 contact hours**
3. **Canvas Course URL:** https://canvas.wisc.edu/courses/321104
4. **Course Designations and Attributes:** General Education
5. **Meeting Times and Locations:** **LEC001 MWF 9:55 – 11:00 in 3654EH**
6. **Required course for CompE, elective for EE**
7. **Instructional Mode:** Inverted/Blended.
8. **How Credit Hours Are Met by the Course:**

This course follows the Traditional Carnegie Definition. The class meets for three 50-minute class periods each week over the fall/spring semester and carries the expectation that students will work on course learning activities (reading, writing, problem sets, studying, etc) for about 2 hours out of classroom for every class period. The syllabus includes more information about meeting times and expectations for student work.

9 INSTRUCTORS AND TEACHING ASSISTANTS

9.1 Eric Hoffman, Teaching Faculty → ericholffman@wisc.edu

9.2 Harish Batchu, Teaching Assistant → harishbabu.batchu@wisc.edu

9.2 Instructor Availability

Eric Hoffman: erichoffman@wisc.edu

Mon 2:30 – 4:30PM = Office hours in 3615EH
Thurs 2:30 – 4:00PM = Office hours in 3615EH
Thurs: 9:30 – 10:30PM = Office hours via "OfficeHours" Channel of MS Teams

Harish Batchu: harishbabu.batchu@wisc.edu

Tues 5:30 – 6:30PM = Office hours in B555 (basement Linux lab)
Weds 6:30 – 8:00PM = Office hours via "OfficeHours" Channel of MS Teams

10 OFFICIAL COURSE DESCRIPTION

Course Description

Introduction to the use of hardware description languages and automated synthesis in design. Advanced design principles. Verilog and systemVerilog description languages. Synthesis from hardware description languages. Timing-oriented synthesis. Relation of integrated circuit layout to timing-oriented design. Design for reuse.

11. Requisites

ECE/Comp Sci 352 & Jr. standing

12 LEARNING OUTCOMES

12.1 Course Learning Outcomes

Students on completion of the ECE 551 course will be able to:

- "Think Hardware First" then code it to a Hardware Description Language
- Design and Code a digital circuit in a HDL (Verilog) using both dataflow and behavioral coding styles.
    - Partition a functional block (control vs datapath)
    - Code verilog for both proper behavior and synthesis
- Properly verify correct functionality of digital implementation
    - Evaluate testing requirements for a complex digital system
    - Build self-checking test benches
- Simulate their HDL implementation
    - Simulate DUT and test bench using ModelSim
    - Simulate a post synthesis netlist
- Synthesis of dataflow and behavioral designs
    - Understand how to constrain a digital circuit
    - Optimize hardware designs (timing, area, power) through synthesis
    - Read/understand static timing analysis reports
    - Map verilog circuit descriptions to an FPGA implementation
- Partition and complete the implementation of a complex digital circuit
    - Work on a team to partition, code, simulate, and synthesize a complex digital design project.

12.2 ABET STUDENT OUTCOMES

c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability

d) an ability to function on multidisciplinary teams

e) an ability to identify formulate, and solve engineering problems.
i) a recognition of the need for, and an ability to engage in life-long learning. (CAD tools & techniques)
k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

13 BRIEF LIST OF TOPICS TO BE COVERED

- Verilog coding styles (structural, dataflow, and behavioral)
- Datapath implementation using dataflow
- Sequential circuits, and how to properly infer flops in verilog.
- Proper coding for synthesis. Coding counters, coding state machines, blocking vs non-blocking statements,
- Building basic testbenches.
- Simulator mechanics…understanding what goes on "under the hood" of Verilog simulator.
- Synthesis constraints
- Synthesis commands and writing a synthesis script
- Synthesis optimizations
- Interpreting synthesis timing reports
- Advanced test bench constructs and self-checking test benches
- Understanding synthesis flow and optimizations built into the tool
- Coding for synthesis optimizations
- Intro to gated clocks
- Parasitic capacitance, SDF files and back annotation
- Digital circuit implementations. Std Cell vs FPGA vs Full Custom
- Introduction to Universal Verification Methodology

14 DISCUSSION SESSIONS

There are two offerings of an optional 50 min discussion session offered weekly lead by the TA. Sometimes these time slots will be used to cover tutorials on how to use a CAD tool like ModelSim or Synopsys.

Tuesday 6:00 – 7:00PM in 2535EH
Thursday 6:00 – 7:00 on MS Teams "General" channel

15 LABORATORY SESSIONS

There are no "laboratory" sessions, but there are 3 tutorial training session for learning the CAD tools used (ModelSim, Synopsys, and post synthesis simulation)

16 REQUIRED TEXTBOOK, SOFTWARE & OTHER COURSE MATERIALS

- No textbook. Will use the IEEE Verilog standard posted on class website as a reference. Also two papers posted on website.

- Software (CAD Tools)
    - ModelSim (Verilog simulation)
    - Synopsys Design Compiler (Verilog synthesis to TSMC std cell library)
    - Quartus (FPGA synthesis to Altera)
    - IC Compiler (Simple APR of netlist)

GRADING

Course Grading & Evaluation:

Final letter grade is determined from an overall cumulative total. Grades determined by curve looking for natural breaks. Average class GPA will be in the vicinity of 3.3.

- Approximately:
    - 15% Homework (5 homework assignments)
    - 11% Quizzes on video lectures (lowest 1 score dropped)
    - 10% In class exercise results (lowest 2 scores dropped)
    - 1% Cummings paper quiz
    - 1% Sutherland/Mills paper quiz
    - 22% Design Project (groups of 4)
        - Graded at end of semester on quantitative and qualitative assessments based on thorough review/evaluation of each team's submission
    - 20% Midterm
    - 20% Final

ACADEMIC INTEGRITY

By enrolling in this course, each student assumes the responsibilities of an active participant in UW-Madison's community of scholars in which everyone's academic work and behavior are held to the highest academic integrity standards. Academic misconduct compromises the integrity of the university. Cheating, fabrication, plagiarism, unauthorized collaboration, and helping others commit these acts are examples of academic misconduct, which can result in disciplinary action. This includes but is not limited to failure on the assignment/course, disciplinary probation, or suspension. Substantial or repeated cases of misconduct will be forwarded to the Office of Student Conduct & Community Standards for additional review. For more information, refer to https://conduct.students.wisc.edu/academic-integrity/.

ACCOMMODATIONS FOR STUDENTS WITH DISABILITIES

McBurney Disability Resource Center syllabus statement: "The University of Wisconsin-Madison supports the right of all enrolled students to a full and equal educational opportunity. The Americans with Disabilities Act (ADA), Wisconsin State Statute (36.12), and UW-Madison policy (Faculty Document 1071) require that students with disabilities be reasonably accommodated in instruction and campus life. Reasonable accommodations for students with disabilities is a shared faculty and student responsibility. Students are expected to inform faculty [me] of their need for instructional accommodations by the end of the third week of the semester, or as soon as possible after a disability has been incurred or recognized. Faculty [I], will work either directly with the student [you] or in coordination with the McBurney Center to identify and provide reasonable instructional accommodations. Disability information, including instructional accommodations as part of a student's educational record, is confidential and protected under FERPA." http://mcburney.wisc.edu/facstaffother/faculty/syllabus.php

DIVERSITY & INCLUSION

Institutional statement on diversity: "Diversity is a source of strength, creativity, and innovation for UW-Madison. We value the contributions of each person and respect the profound ways their identity, culture, background, experience, status, abilities, and opinion enrich the university community. We commit ourselves to the pursuit of excellence in teaching, research, outreach, and diversity as inextricably linked goals.

The University of Wisconsin-Madison fulfills its public mission by creating a welcoming and inclusive community for people from every background – people who as students, faculty, and staff serve Wisconsin and the world." https://diversity.wisc.edu/