Exercise 8 (Testbench for Sequential Circuit):

Around slide 30 of Lecture03 there is a discussion of stimulus for sequential circuits.

If your DUT is purely combinational (like many we have worked with so far) then it is fine to apply stimulus, wait for some time (# delay) and then check results.

If the DUT is a sequential circuit (uses clock and performs a more complex operation) then it is best to use events (like clock periods, or assertions of status/done signals) as the gate keeper for when the self checks should be performed.

A sequential DUT is provided (**sqrt.sv**). It calculates the sqrt of an incoming 16-bit **signed** number. It provides a **done** status signal, and an **err** flag is asserted if the incoming value was negative (no real sqrt).

Your testbench should reset the DUT and perform at least 3 different calculations

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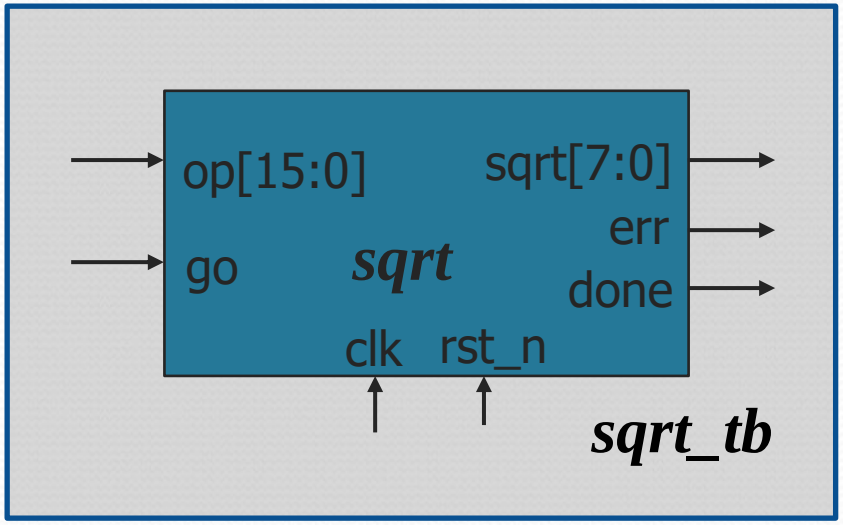

Signal:	Dir:	Description:
clk,rst_n	in	clk & active low asynch reset
go	in	When asserted op is sampled and sqrt calculation commences.
op[15:0]	In	**signed** operand to take sqrt of
sqrt[7:0]	out	result
done	out	Asserts when calculation completed, deasserts with next **go**
err	out	Last value had no sqrt

Download ***sqrt.sv*** (DUT)

Submit ***sqrt_tb.sv*** to dropbox by end of class