

邏輯系統實驗

Final Project - Frequency Analysis System

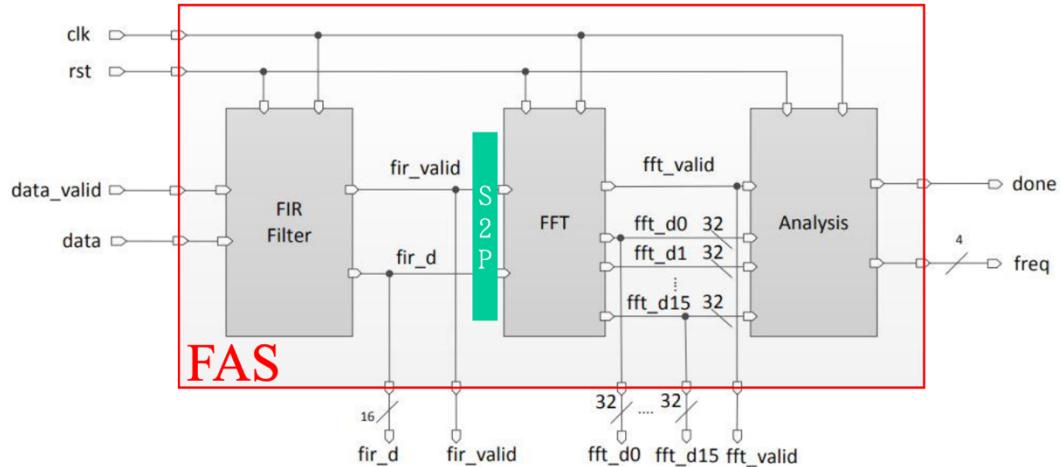
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大綱：

- 簡介題目
- 實現方式
- 結果展現
- 程式說明與遇到的困難
- 心得

簡介題目：



Given discrete time domain signal for a period of the time. Please **find the main frequency band** which is the frequency whose sum of square of the real part data and imaginary part data is maximum.

實現方式：

< Using 3 steps >

- a. Use low-pass filter to filter noise which frequency higher than cut-off frequency
- b. Use FFT to transform signal from time domain into frequency domain
- c. Analysis all frequencies and find the main frequency band

< System structure: 4 components >

1. **FIR Filter** (Finite Impulse Response Filter) : Filter out the high frequency noise (限定欲處理的頻率範圍)
2. **S2P** (Serial to Parallel) : Transfer the serial outputs which output from FIR Filter to FFT in parallel
3. **FFT** (Fast Fourier Transform) : Time domain -> Frequency domain
4. **Analysis** : Find the main frequency band

FAS.v

```
module FAS(
    input clk,
    input rst,
    input data_valid,
```

```

    input [15:0] data,
    output fir_valid,
    output wire signed [15:0] fir_d,
    output fft_valid,
    output [31:0] fft_d0, fft_d1, fft_d2, fft_d3, fft_d4, fft_d5, fft_d6,
    fft_d7, fft_d8, fft_d9, fft_d10, fft_d11, fft_d12, fft_d13, fft_d14,
    fft_d15,
    output done,
    output wire [3:0] freq
);

    wire s2p_valid;
    wire [15:0] x0, x1, x2, x3, x4, x5, x6, x7, x8, x9, x10, x11, x12, x13,
x14, x15;

    FIR fir(clk, rst, data_valid, data, fir_valid, fir_d);
    S2P s2p(clk, rst, fir_valid, fir_d, s2p_valid, x0, x1, x2, x3, x4, x5,
x6, x7, x8, x9, x10, x11, x12, x13, x14, x15);
    FFT fft(clk, rst, s2p_valid, x0, x1, x2, x3, x4, x5, x6, x7, x8, x9,
x10, x11, x12, x13, x14, x15, fft_valid, fft_d0, fft_d1, fft_d2, fft_d3,
fft_d4, fft_d5, fft_d6, fft_d7, fft_d8, fft_d9, fft_d10, fft_d11, fft_d12,
fft_d13, fft_d14, fft_d15);
    Analysis analysis(clk, rst, fft_valid, fft_d0, fft_d1, fft_d2, fft_d3,
fft_d4, fft_d5, fft_d6, fft_d7, fft_d8, fft_d9, fft_d10, fft_d11, fft_d12,
fft_d13, fft_d14, fft_d15, done, freq);

endmodule

```

FIR.v

```

module FIR(
    input clk,
    input rst,
    input data_valid,
    input signed [15:0] data,
    output reg fir_valid,
    output signed [15:0] fir_d
);

```

```

`include "FIR_coefficient.dat"

reg signed [15:0] D[30:0];//31顆D flip-flop
reg signed [35:0] mul [31:0];//乘法結果
reg signed[35:0] sum = 0;
integer k;
integer counter = 0;

always @(posedge clk or posedge rst)
begin
  if(rst)
    begin
      fir_valid <= 0;
      counter <= 0;
      for(k = 0; k < 31; k = k+1)
        begin
          D[k] <= 0;
        end
      for(k = 0; k < 32; k = k+1)
        begin
          mul[k] <= 0;
        end
    end
  else
    begin
      if(data_valid)
        begin
          D[0] <= data;
          for(k = 1; k < 31; k = k+1)
            begin
              D[k] <= D[k-1];
            end
          counter <= counter + 1;
          if(counter >= 32)
            begin
              fir_valid <= 1'b1;
            end
        end
    end
  end
end

```

```
    end

end

always@(posedge clk)
begin
    if(data_valid)
        begin
            mul[0] <= data*FIR_C00;
            mul[1] <= D[0]*FIR_C01;
            mul[2] <= D[1]*FIR_C02;
            mul[3] <= D[2]*FIR_C03;
            mul[4] <= D[3]*FIR_C04;
            mul[5] <= D[4]*FIR_C05;
            mul[6] <= D[5]*FIR_C06;
            mul[7] <= D[6]*FIR_C07;
            mul[8] <= D[7]*FIR_C08;
            mul[9] <= D[8]*FIR_C09;
            mul[10] <= D[9]*FIR_C10;
            mul[11] <= D[10]*FIR_C11;
            mul[12] <= D[11]*FIR_C12;
            mul[13] <= D[12]*FIR_C13;
            mul[14] <= D[13]*FIR_C14;
            mul[15] <= D[14]*FIR_C15;
            mul[16] <= D[15]*FIR_C16;
            mul[17] <= D[16]*FIR_C17;
            mul[18] <= D[17]*FIR_C18;
            mul[19] <= D[18]*FIR_C19;
            mul[20] <= D[19]*FIR_C20;
            mul[21] <= D[20]*FIR_C21;
            mul[22] <= D[21]*FIR_C22;
            mul[23] <= D[22]*FIR_C23;
            mul[24] <= D[23]*FIR_C24;
            mul[25] <= D[24]*FIR_C25;
            mul[26] <= D[25]*FIR_C26;
            mul[27] <= D[26]*FIR_C27;
            mul[28] <= D[27]*FIR_C28;
            mul[29] <= D[28]*FIR_C29;
            mul[30] <= D[29]*FIR_C30;
```

```

mul[31] <= D[30]*FIR_C31;
sum =
mul[0]+mul[1]+mul[2]+mul[3]+mul[4]+mul[5]+mul[6]+mul[7]+mul[8]+
mul[9]+mul[10]+mul[11]+mul[12]+mul[13]+mul[14]+mul[15]+mul[16]+mul[17]+
mul[18]+mul[19]+mul[20]+mul[21]+mul[22]+mul[23]+mul[24]+mul[25]+mul[26]+
mul[27]+mul[28]+mul[29]+mul[30]+mul[31];
end
end

assign fir_d = sum[31:16];

endmodule

```

S2P.v
<pre> module S2P (clk,rst,fir_valid,fir_d,s2p_valid,x0,x1,x2,x3,x4,x5,x6,x7,x8,x9,x10,x11,x 12,x13,x14,x15); input clk; input rst; input fir_valid; input [15:0] fir_d; output reg s2p_valid; output reg signed [15:0] x0,x1,x2,x3,x4,x5,x6,x7,x8,x9,x10,x11,x12,x13,x14,x15; reg [3:0] cnt; always@(posedge clk or posedge rst) begin if (rst) begin s2p_valid <= 0; cnt <= 4'd0; </pre>

```
x0 <= 16'd0;
x1 <= 16'd0;
x2 <= 16'd0;
x3 <= 16'd0;
x4 <= 16'd0;
x5 <= 16'd0;
x6 <= 16'd0;
x7 <= 16'd0;
x8 <= 16'd0;
x9 <= 16'd0;
x10 <= 16'd0;
x11 <= 16'd0;
x12 <= 16'd0;
x13 <= 16'd0;
x14 <= 16'd0;
x15 <= 16'd0;
end
else if (fir_valid)
begin
if (cnt == 4'd15)
begin
s2p_valid <= 1;
end
else
begin
s2p_valid <= 0;
end

x0 <= x1;
x1 <= x2;
x2 <= x3;
x3 <= x4;
x4 <= x5;
x5 <= x6;
x6 <= x7;
x7 <= x8;
x8 <= x9;
```

```

x9 <= x10;
x10 <= x11;
x11 <= x12;
x12 <= x13;
x13 <= x14;
x14 <= x15;
x15 <= fir_d + {15'd0,fir_d[15]};

cnt <= cnt + 4'd1;
end

end

endmodule

```

FFT.v

```

module FFT (clk, rst, s2p_valid,
    x0, x1, x2, x3, x4, x5, x6, x7, x8, x9,
    x10, x11, x12, x13, x14, x15, fft_valid,
    fft_d0, fft_d1, fft_d2, fft_d3, fft_d4, fft_d5, fft_d6, fft_d7,
    fft_d8, fft_d9, fft_d10, fft_d11, fft_d12, fft_d13, fft_d14, fft_d15);

`include "FFT_coefficient.dat"

input clk, rst;
input s2p_valid;
input signed [15:0] x0,x1,x2,x3,x4,x5,x6,x7,x8,x9,x10,x11,x12,x13,x14,x15;
output reg fft_valid;
output reg [31:0] fft_d1, fft_d2, fft_d3, fft_d4, fft_d5, fft_d6, fft_d7,
fft_d8;
output reg [31:0] fft_d9, fft_d10, fft_d11, fft_d12, fft_d13, fft_d14,
fft_d15, fft_d0;

//=====
=====
```

```

// Stage 1
//=====
=====

wire signed [15:0]
mul_S1_R0,mul_S1_R1,mul_S1_R2,mul_S1_R3,mul_S1_R4,mul_S1_R5,mul_S1_R6,mul_
S1_R7;
assign mul_S1_R0 = x0 + x8;
assign mul_S1_R1 = x1 + x9;
assign mul_S1_R2 = x2 + x10;
assign mul_S1_R3 = x3 + x11;
assign mul_S1_R4 = x4 + x12;
assign mul_S1_R5 = x5 + x13;
assign mul_S1_R6 = x6 + x14;
assign mul_S1_R7 = x7 + x15;

wire signed [47:0]
mul_S1_R8,mul_S1_R9,mul_S1_R10,mul_S1_R11,mul_S1_R12,mul_S1_R13,mul_S1_R14
,mul_S1_R15;
assign mul_S1_R8 = ((x0 - x8)*FFT_R0);
assign mul_S1_R9 = ((x1 - x9)*FFT_R1);
assign mul_S1_R10 = ((x2 - x10)*FFT_R2);
assign mul_S1_R11 = ((x3 - x11)*FFT_R3);
assign mul_S1_R12 = ((x4 - x12)*FFT_R4);
assign mul_S1_R13 = ((x5 - x13)*FFT_R5);
assign mul_S1_R14 = ((x6 - x14)*FFT_R6);
assign mul_S1_R15 = ((x7 - x15)*FFT_R7);

wire signed [47:0]
mul_S1_I8,mul_S1_I9,mul_S1_I10,mul_S1_I11,mul_S1_I12,mul_S1_I13,mul_S1_I14
,mul_S1_I15;
assign mul_S1_I8 = ((x0 - x8)*FFT_I0);
assign mul_S1_I9 = ((x1 - x9)*FFT_I1);
assign mul_S1_I10 = ((x2 - x10)*FFT_I2);
assign mul_S1_I11 = ((x3 - x11)*FFT_I3);
assign mul_S1_I12 = ((x4 - x12)*FFT_I4);
assign mul_S1_I13 = ((x5 - x13)*FFT_I5);
assign mul_S1_I14 = ((x6 - x14)*FFT_I6);
assign mul_S1_I15 = ((x7 - x15)*FFT_I7);

```

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//=====
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// Stage 2
//=====

=====

wire signed [15:0] mul_S2_R0,mul_S2_R1,mul_S2_R2,mul_S2_R3;
wire signed [31:0] mul_S2_R8,mul_S2_R9,mul_S2_R10,mul_S2_R11;
assign mul_S2_R0 = mul_S1_R0 + mul_S1_R4;
assign mul_S2_R1 = mul_S1_R1 + mul_S1_R5;
assign mul_S2_R2 = mul_S1_R2 + mul_S1_R6;
assign mul_S2_R3 = mul_S1_R3 + mul_S1_R7;
assign mul_S2_R8 = mul_S1_R8[39:8] + mul_S1_R12[39:8];
assign mul_S2_R9 = mul_S1_R9[39:8] + mul_S1_R13[39:8];
assign mul_S2_R10 = mul_S1_R10[39:8] + mul_S1_R14[39:8];
assign mul_S2_R11 = mul_S1_R11[39:8] + mul_S1_R15[39:8];

wire signed [31:0] mul_S2_I8,mul_S2_I9,mul_S2_I10,mul_S2_I11;
assign mul_S2_I8 = mul_S1_I8[39:8] + mul_S1_I12[39:8];
assign mul_S2_I9 = mul_S1_I9[39:8] + mul_S1_I13[39:8];
assign mul_S2_I10 = mul_S1_I10[39:8] + mul_S1_I14[39:8];
assign mul_S2_I11 = mul_S1_I11[39:8] + mul_S1_I15[39:8];

wire signed [47:0] mul_S2_R4,mul_S2_R5,mul_S2_R6,mul_S2_R7;
wire signed [47:0] mul_S2_I4,mul_S2_I5,mul_S2_I6,mul_S2_I7;
assign mul_S2_R4 = (mul_S1_R0 - mul_S1_R4)*FFT_R0;
assign mul_S2_R5 = (mul_S1_R1 - mul_S1_R5)*FFT_R2;
assign mul_S2_R6 = (mul_S1_R2 - mul_S1_R6)*FFT_R4;
assign mul_S2_R7 = (mul_S1_R3 - mul_S1_R7)*FFT_R6;
assign mul_S2_I4 = (mul_S1_R0 - mul_S1_R4)*FFT_I0;
assign mul_S2_I5 = (mul_S1_R1 - mul_S1_R5)*FFT_I2;
assign mul_S2_I6 = (mul_S1_R2 - mul_S1_R6)*FFT_I4;
assign mul_S2_I7 = (mul_S1_R3 - mul_S1_R7)*FFT_I6;

wire signed [63:0] mul_S2_R12,mul_S2_R13,mul_S2_R14,mul_S2_R15;
wire signed [63:0] mul_S2_I12,mul_S2_I13,mul_S2_I14,mul_S2_I15;

```

```

assign mul_S2_R12 = ($signed(mul_S1_R8[39:8]) -
$signed(mul_S1_R12[39:8]))*FFT_R0 + ($signed(mul_S1_I12[39:8]) -
$signed(mul_S1_I8[39:8]))*FFT_I0;
assign mul_S2_R13 = ($signed(mul_S1_R9[39:8]) -
$signed(mul_S1_R13[39:8]))*FFT_R2 + ($signed(mul_S1_I13[39:8]) -
$signed(mul_S1_I9[39:8]))*FFT_I2;
assign mul_S2_R14 = ($signed(mul_S1_R10[39:8]) -
$signed(mul_S1_R14[39:8]))*FFT_R4 + ($signed(mul_S1_I14[39:8]) -
$signed(mul_S1_I10[39:8]))*FFT_I4;
assign mul_S2_R15 = ($signed(mul_S1_R11[39:8]) -
$signed(mul_S1_R15[39:8]))*FFT_R6 + ($signed(mul_S1_I15[39:8]) -
$signed(mul_S1_I11[39:8]))*FFT_I6;
assign mul_S2_I12 = ($signed(mul_S1_R8[39:8]) -
$signed(mul_S1_R12[39:8]))*FFT_I0 + ($signed(mul_S1_I8[39:8]) -
$signed(mul_S1_I12[39:8]))*FFT_R0;
assign mul_S2_I13 = ($signed(mul_S1_R9[39:8]) -
$signed(mul_S1_R13[39:8]))*FFT_I2 + ($signed(mul_S1_I9[39:8]) -
$signed(mul_S1_I13[39:8]))*FFT_R2;
assign mul_S2_I14 = ($signed(mul_S1_R10[39:8]) -
$signed(mul_S1_R14[39:8]))*FFT_I4 + ($signed(mul_S1_I10[39:8]) -
$signed(mul_S1_I14[39:8]))*FFT_R4;
assign mul_S2_I15 = ($signed(mul_S1_R11[39:8]) -
$signed(mul_S1_R15[39:8]))*FFT_I6 + ($signed(mul_S1_I11[39:8]) -
$signed(mul_S1_I15[39:8]))*FFT_R6;

//=====
=====

// Stage 3
//=====
=====

wire signed [15:0] mul_S3_R0,mul_S3_R1;
wire signed [31:0]
mul_S3_R4,mul_S3_R5,mul_S3_R8,mul_S3_R9,mul_S3_R12,mul_S3_R13;
assign mul_S3_R0 = mul_S2_R0 + mul_S2_R2;
assign mul_S3_R1 = mul_S2_R1 + mul_S2_R3;
assign mul_S3_R4 = mul_S2_R4[39:8] + mul_S2_R6[39:8];
assign mul_S3_R5 = mul_S2_R5[39:8] + mul_S2_R7[39:8];
assign mul_S3_R8 = mul_S2_R8 + mul_S2_R10;

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```

assign mul_S3_R9 = mul_S2_R9 + mul_S2_R11;
assign mul_S3_R12 = mul_S2_R12[47:16] + mul_S2_R14[47:16];
assign mul_S3_R13 = mul_S2_R13[47:16] + mul_S2_R15[47:16];

wire signed [31:0]
mul_S3_I4,mul_S3_I5,mul_S3_I8,mul_S3_I9,mul_S3_I12,mul_S3_I13;
assign mul_S3_I4 = mul_S2_I4[39:8] + mul_S2_I6[39:8];
assign mul_S3_I5 = mul_S2_I5[39:8] + mul_S2_I7[39:8];
assign mul_S3_I8 = mul_S2_I8 + mul_S2_I10;
assign mul_S3_I9 = mul_S2_I9 + mul_S2_I11;
assign mul_S3_I12 = mul_S2_I12[47:16] + mul_S2_I14[47:16];
assign mul_S3_I13 = mul_S2_I13[47:16] + mul_S2_I15[47:16];

wire signed [47:0] mul_S3_R2,mul_S3_R3;
wire signed [47:0] mul_S3_I2,mul_S3_I3;
assign mul_S3_R2 = (mul_S2_R0 - mul_S2_R2)*FFT_R0;
assign mul_S3_R3 = (mul_S2_R1 - mul_S2_R3)*FFT_R4;
assign mul_S3_I2 = (mul_S2_R0 - mul_S2_R2)*FFT_I0;
assign mul_S3_I3 = (mul_S2_R1 - mul_S2_R3)*FFT_I4;

wire signed [63:0]
mul_S3_R6,mul_S3_R7,mul_S3_R10,mul_S3_R11,mul_S3_R14,mul_S3_R15;
wire signed [63:0]
mul_S3_I6,mul_S3_I7,mul_S3_I10,mul_S3_I11,mul_S3_I14,mul_S3_I15;
assign mul_S3_R6 = ($signed(mul_S2_R4[39:8]) -
$signed(mul_S2_R6[39:8]))*FFT_R0 + ($signed(mul_S2_I6[39:8]) -
$signed(mul_S2_I4[39:8]))*FFT_I0;
assign mul_S3_R7 = ($signed(mul_S2_R5[39:8]) -
$signed(mul_S2_R7[39:8]))*FFT_R4 + ($signed(mul_S2_I7[39:8]) -
$signed(mul_S2_I5[39:8]))*FFT_I4;
assign mul_S3_R10 = (mul_S2_R8 - mul_S2_R10)*FFT_R0 + (mul_S2_I10 -
mul_S2_I8)*FFT_I0;
assign mul_S3_R11 = (mul_S2_R9 - mul_S2_R11)*FFT_R4 + (mul_S2_I11 -
mul_S2_I9)*FFT_I4;
assign mul_S3_R14 = ($signed(mul_S2_R12[47:16]) -
$signed(mul_S2_R14[47:16]))*FFT_R0 + ($signed(mul_S2_I14[47:16]) -
$signed(mul_S2_I12[47:16]))*FFT_I0;

```

```

assign mul_S3_R15 = ($signed(mul_S2_R13[47:16]) -
$signed(mul_S2_R15[47:16]))*FFT_R4 + ($signed(mul_S2_I15[47:16]) -
$signed(mul_S2_I13[47:16]))*FFT_I4;
assign mul_S3_I6 = ($signed(mul_S2_R4[39:8]) -
$signed(mul_S2_R6[39:8]))*FFT_I0 + ($signed(mul_S2_I4[39:8]) -
$signed(mul_S2_I6[39:8]))*FFT_R0;
assign mul_S3_I7 = ($signed(mul_S2_R5[39:8]) -
$signed(mul_S2_R7[39:8]))*FFT_I4 + ($signed(mul_S2_I5[39:8]) -
$signed(mul_S2_I7[39:8]))*FFT_R4;
assign mul_S3_I10 = (mul_S2_R8 - mul_S2_R10)*FFT_I0 + (mul_S2_I8 -
mul_S2_I10)*FFT_R0;
assign mul_S3_I11 = (mul_S2_R9 - mul_S2_R11)*FFT_I4 + (mul_S2_I9 -
mul_S2_I11)*FFT_R4;
assign mul_S3_I14 = ($signed(mul_S2_R12[47:16]) -
$signed(mul_S2_R14[47:16]))*FFT_I0 + ($signed(mul_S2_I12[47:16]) -
$signed(mul_S2_I14[47:16]))*FFT_R0;
assign mul_S3_I15 = ($signed(mul_S2_R13[47:16]) -
$signed(mul_S2_R15[47:16]))*FFT_I4 + ($signed(mul_S2_I13[47:16]) -
$signed(mul_S2_I15[47:16]))*FFT_R4;

//=====
=====

// Stage 4
//=====
=====

wire signed [15:0] mul_S4_R0;
wire signed [31:0]
mul_S4_R2,mul_S4_R4,mul_S4_R6,mul_S4_R8,mul_S4_R10,mul_S4_R12,mul_S4_R14;
assign mul_S4_R0 = mul_S3_R0 + mul_S3_R1;
assign mul_S4_R2 = mul_S3_R2[39:8] + mul_S3_R3[39:8];
assign mul_S4_R4 = mul_S3_R4 + mul_S3_R5;
assign mul_S4_R6 = mul_S3_R6[47:16] + mul_S3_R7[47:16];
assign mul_S4_R8 = mul_S3_R8 + mul_S3_R9;
assign mul_S4_R10 = mul_S3_R10[47:16] + mul_S3_R11[47:16];
assign mul_S4_R12 = mul_S3_R12 + mul_S3_R13;
assign mul_S4_R14 = mul_S3_R14[47:16] + mul_S3_R15[47:16];

```

```

wire signed [31:0]
mul_S4_I2,mul_S4_I4,mul_S4_I6,mul_S4_I8,mul_S4_I10,mul_S4_I12,mul_S4_I14;
assign mul_S4_I2 = mul_S3_I2[39:8] + mul_S3_I3[39:8];
assign mul_S4_I4 = mul_S3_I4 + mul_S3_I5;
assign mul_S4_I6 = mul_S3_I6[47:16] + mul_S3_I7[47:16];
assign mul_S4_I8 = mul_S3_I8 + mul_S3_I9;
assign mul_S4_I10 = mul_S3_I10[47:16] + mul_S3_I11[47:16];
assign mul_S4_I12 = mul_S3_I12 + mul_S3_I13;
assign mul_S4_I14 = mul_S3_I14[47:16] + mul_S3_I15[47:16];

wire signed [47:0] mul_S4_R1;
wire signed [47:0] mul_S4_I1;
assign mul_S4_R1 = (mul_S3_R0 - mul_S3_R1)*FFT_R0;
assign mul_S4_I1 = (mul_S3_R0 - mul_S3_R1)*FFT_I0;

wire signed [63:0]
mul_S4_R3,mul_S4_R5,mul_S4_R7,mul_S4_R9,mul_S4_R11,mul_S4_R13,mul_S4_R15;
wire signed [63:0]
mul_S4_I3,mul_S4_I5,mul_S4_I7,mul_S4_I9,mul_S4_I11,mul_S4_I13,mul_S4_I15;
assign mul_S4_R3 = ($signed(mul_S3_R2[39:8]) -
$signed(mul_S3_R3[39:8]))*FFT_R0 + ($signed(mul_S3_I3[39:8]) -
$signed(mul_S3_I2[39:8]))*FFT_I0;
assign mul_S4_R5 = (mul_S3_R4 - mul_S3_R5)*FFT_R0 + (mul_S3_I5 -
mul_S3_I4)*FFT_I0;
assign mul_S4_R7 = ($signed(mul_S3_R6[47:16]) -
$signed(mul_S3_R7[47:16]))*FFT_R0 + ($signed(mul_S3_I7[47:16]) -
$signed(mul_S3_I6[47:16]))*FFT_I0;
assign mul_S4_R9 = (mul_S3_R8 - mul_S3_R9)*FFT_R0 + (mul_S3_I9 -
mul_S3_I8)*FFT_I0;
assign mul_S4_R11 = ($signed(mul_S3_R10[47:16]) -
$signed(mul_S3_R11[47:16]))*FFT_R0 + ($signed(mul_S3_I11[47:16]) -
$signed(mul_S3_I10[47:16]))*FFT_I0;
assign mul_S4_R13 = (mul_S3_R12 - mul_S3_R13)*FFT_R0 + (mul_S3_I13 -
mul_S3_I12)*FFT_I0;
assign mul_S4_R15 = ($signed(mul_S3_R14[47:16]) -
$signed(mul_S3_R15[47:16]))*FFT_R0 + ($signed(mul_S3_I15[47:16]) -
$signed(mul_S3_I14[47:16]))*FFT_I0;

```

```

assign mul_S4_I3 = ($signed(mul_S3_R2[39:8]) -
$signed(mul_S3_R3[39:8]))*FFT_I0 + ($signed(mul_S3_I2[39:8]) -
$signed(mul_S3_I3[39:8]))*FFT_R0;
assign mul_S4_I5 = (mul_S3_R4 - mul_S3_R5)*FFT_I0 + (mul_S3_I4 -
mul_S3_I5)*FFT_R0;
assign mul_S4_I7 = ($signed(mul_S3_R6[47:16]) -
$signed(mul_S3_R7[47:16]))*FFT_I0 + ($signed(mul_S3_I6[47:16]) -
$signed(mul_S3_I7[47:16]))*FFT_R0;
assign mul_S4_I9 = (mul_S3_R8 - mul_S3_R9)*FFT_I0 + (mul_S3_I8 -
mul_S3_I9)*FFT_R0;
assign mul_S4_I11 = ($signed(mul_S3_R10[47:16]) -
$signed(mul_S3_R11[47:16]))*FFT_I0 + ($signed(mul_S3_I10[47:16]) -
$signed(mul_S3_I11[47:16]))*FFT_R0;
assign mul_S4_I13 = (mul_S3_R12 - mul_S3_R13)*FFT_I0 + (mul_S3_I12 -
mul_S3_I13)*FFT_R0;
assign mul_S4_I15 = ($signed(mul_S3_R14[47:16]) -
$signed(mul_S3_R15[47:16]))*FFT_I0 + ($signed(mul_S3_I14[47:16]) -
$signed(mul_S3_I15[47:16]))*FFT_R0;

always@(posedge clk or posedge rst)
begin

if(rst)
begin
fft_valid <= 0;
fft_d0 <= 32'd0;
fft_d1 <= 32'd0;
fft_d2 <= 32'd0;
fft_d3 <= 32'd0;
fft_d4 <= 32'd0;
fft_d5 <= 32'd0;
fft_d6 <= 32'd0;
fft_d7 <= 32'd0;
fft_d8 <= 32'd0;
fft_d9 <= 32'd0;
fft_d10 <= 32'd0;
fft_d11 <= 32'd0;
fft_d12 <= 32'd0;

```

```

fft_d13 <= 32'd0;
fft_d14 <= 32'd0;
fft_d15 <= 32'd0;

end
else if (s2p_valid)
begin
    fft_valid <= 1;
    fft_d0 <= {mul_S4_R0,16'd0};
    fft_d1 <= {mul_S4_R8[23:8],mul_S4_I8[23:8]};
    fft_d2 <= {mul_S4_R4[23:8],mul_S4_I4[23:8]};
    fft_d3 <= {mul_S4_R12[23:8],mul_S4_I12[23:8]};
    fft_d4 <= {mul_S4_R2[23:8],mul_S4_I2[23:8]};
    fft_d5 <= {mul_S4_R10[23:8],mul_S4_I10[23:8]};
    fft_d6 <= {mul_S4_R6[23:8],mul_S4_I6[23:8]};
    fft_d7 <= {mul_S4_R14[23:8],mul_S4_I14[23:8]};
    fft_d8 <= {mul_S4_R1[31:16],mul_S4_I1[31:16]};
    fft_d9 <= {mul_S4_R9[39:24],mul_S4_I9[39:24]};
    fft_d10 <= {mul_S4_R5[39:24],mul_S4_I5[39:24]};
    fft_d11 <= {mul_S4_R13[39:24],mul_S4_I13[39:24]};
    fft_d12 <= {mul_S4_R3[39:24],mul_S4_I3[39:24]};
    fft_d13 <= {mul_S4_R11[39:24],mul_S4_I11[39:24]};
    fft_d14 <= {mul_S4_R7[39:24],mul_S4_I7[39:24]};
    fft_d15 <= {mul_S4_R15[39:24],mul_S4_I15[39:24]};

end
else
begin
    fft_valid <= 0;
    fft_d0 <= fft_d0;
    fft_d1 <= fft_d1;
    fft_d2 <= fft_d2;
    fft_d3 <= fft_d3;
    fft_d4 <= fft_d4;
    fft_d5 <= fft_d5;
    fft_d6 <= fft_d6;
    fft_d7 <= fft_d7;
    fft_d8 <= fft_d8;
    fft_d9 <= fft_d9;
    fft_d10 <= fft_d10;

```

```

    fft_d11 <= fft_d11;
    fft_d12 <= fft_d12;
    fft_d13 <= fft_d13;
    fft_d14 <= fft_d14;
    fft_d15 <= fft_d15;
end

end

endmodule

```

Analysis.v

```

module Analysis(clk, rst, fft_valid, fft_d0, fft_d1, fft_d2, fft_d3,
fft_d4, fft_d5, fft_d6, fft_d7, fft_d8, fft_d9, fft_d10, fft_d11, fft_d12,
fft_d13, fft_d14, fft_d15, done, freq);
input clk, rst, fft_valid;
input signed [31:0] fft_d0, fft_d1, fft_d2, fft_d3, fft_d4, fft_d5,
fft_d6, fft_d7, fft_d8, fft_d9, fft_d10, fft_d11, fft_d12, fft_d13,
fft_d14, fft_d15;
output reg done;
output [3:0] freq;
integer k;
reg [3:0] n;
reg signed [31:0] a[15:0];
reg signed [31:0]
max_level1_1,max_level1_2,max_level1_3,max_level1_4,max_level1_5,max_level
1_6,max_level1_7,max_level1_8;
reg signed [31:0]
max_level2_1,max_level2_2,max_level2_3,max_level2_4,max_level3_1,max_level
3_2,max;

always @(posedge clk or posedge rst)
begin
if(rst)
begin
done <= 0;

```

```

max <= 0;
n <= 0;
for(k = 0; k < 32; k = k+1)
begin
    a[k] <= 0;
end
max_level1_1 <= 0;max_level1_2 <= 0;max_level1_3 <= 0;max_level1_4
<= 0;
max_level1_5 <= 0;max_level1_6 <= 0;max_level1_7 <= 0;max_level1_8
<= 0;
max_level2_1 <= 0;max_level2_2 <= 0;max_level2_3 <= 0;max_level2_4
<= 0;
max_level3_1 <= 0;max_level3_2 <= 0;max <= 0;
end
else if (fft_valid)
begin
    a[0] <= $signed(fft_d0[31:16])*$signed(fft_d0[31:16]) +
$signed(fft_d0[15:0])*$signed(fft_d0[15:0]);
    a[1] = $signed(fft_d1[31:16])*$signed(fft_d1[31:16]) +
$signed(fft_d1[15:0])*$signed(fft_d1[15:0]);
    a[2] = $signed(fft_d2[31:16])*$signed(fft_d2[31:16]) +
$signed(fft_d2[15:0])*$signed(fft_d2[15:0]);
    a[3] = $signed(fft_d3[31:16])*$signed(fft_d3[31:16]) +
$signed(fft_d3[15:0])*$signed(fft_d3[15:0]);
    a[4] = $signed(fft_d4[31:16])*$signed(fft_d4[31:16]) +
$signed(fft_d4[15:0])*$signed(fft_d4[15:0]);
    a[5] = $signed(fft_d5[31:16])*$signed(fft_d5[31:16]) +
$signed(fft_d5[15:0])*$signed(fft_d5[15:0]);
    a[6] = $signed(fft_d6[31:16])*$signed(fft_d6[31:16]) +
$signed(fft_d6[15:0])*$signed(fft_d6[15:0]);
    a[7] = $signed(fft_d7[31:16])*$signed(fft_d7[31:16]) +
$signed(fft_d7[15:0])*$signed(fft_d7[15:0]);
    a[8] = $signed(fft_d8[31:16])*$signed(fft_d8[31:16]) +
$signed(fft_d8[15:0])*$signed(fft_d8[15:0]);
    a[9] = $signed(fft_d9[31:16])*$signed(fft_d9[31:16]) +
$signed(fft_d9[15:0])*$signed(fft_d9[15:0]);
    a[10] = $signed(fft_d10[31:16])*$signed(fft_d10[31:16]) +
$signed(fft_d10[15:0])*$signed(fft_d10[15:0]);

```

```

    a[11] = $signed(fft_d11[31:16])*$signed(fft_d11[31:16]) +
$signed(fft_d11[15:0])*$signed(fft_d11[15:0]);
    a[12] = $signed(fft_d12[31:16])*$signed(fft_d12[31:16]) +
$signed(fft_d12[15:0])*$signed(fft_d12[15:0]);
    a[13] = $signed(fft_d13[31:16])*$signed(fft_d13[31:16]) +
$signed(fft_d13[15:0])*$signed(fft_d13[15:0]);
    a[14] = $signed(fft_d14[31:16])*$signed(fft_d14[31:16]) +
$signed(fft_d14[15:0])*$signed(fft_d14[15:0]);
    a[15] = $signed(fft_d15[31:16])*$signed(fft_d15[31:16]) +
$signed(fft_d15[15:0])*$signed(fft_d15[15:0]);

    max_level1_1 = a[0]>a[1]?a[0]:a[1];
    max_level1_2 = a[2]>a[3]?a[2]:a[3];
    max_level1_3 = a[4]>a[5]?a[4]:a[5];
    max_level1_4 = a[6]>a[7]?a[6]:a[7];
    max_level1_5 = a[8]>a[9]?a[8]:a[9];
    max_level1_6 = a[10]>a[11]?a[10]:a[11];
    max_level1_7 = a[12]>a[13]?a[12]:a[13];
    max_level1_8 = a[14]>a[15]?a[14]:a[15];
    max_level2_1 = max_level1_1>max_level1_2?max_level1_1:max_level1_2;
    max_level2_2 = max_level1_3>max_level1_4?max_level1_3:max_level1_4;
    max_level2_3 = max_level1_5>max_level1_6?max_level1_5:max_level1_6;
    max_level2_4 = max_level1_7>max_level1_8?max_level1_7:max_level1_8;
    max_level3_1 = max_level2_1>max_level2_2?max_level2_1:max_level2_2;
    max_level3_2 = max_level2_3>max_level2_4?max_level2_3:max_level2_4;
    max = max_level3_1>max_level3_2?max_level3_1:max_level3_2;

    n =
max==a[0]?4'b0000:(max==a[1]?4'b0001:(max==a[2])?4'b0010:(max==a[3])?4
'b0011:(max==a[4])?4'b0100:(max==a[5])?4'b0101:(max==a[6])?4'b0110:(max
==a[7])?4'b0111:(max==a[8])?4'b1000:(max==a[9])?4'b1001:(max==a[10])?4
'b1010:(max==a[11])?4'b1011:(max==a[12])?4'b1100:(max==a[13])?4'b1101:(
max==a[14])?4'b1110:(max==a[15])?4'b1111:0);
    done = 1;
    end
  else
    begin
      done <= 0;

```

```

    max <= 0;

    n <= 0;

end

assign freq = n;

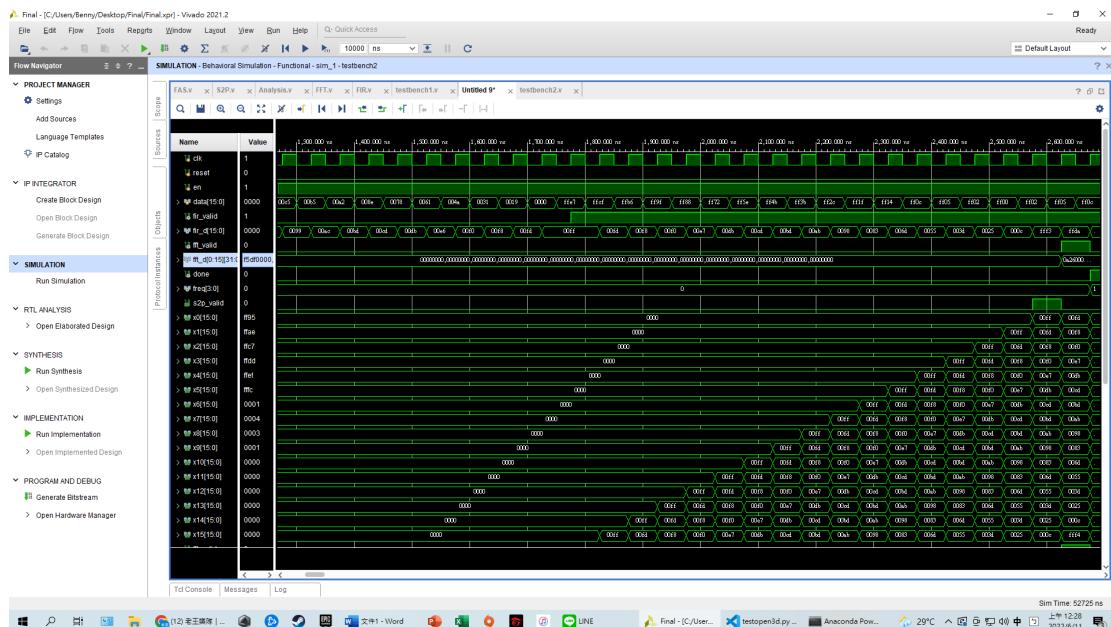
endmodule

```

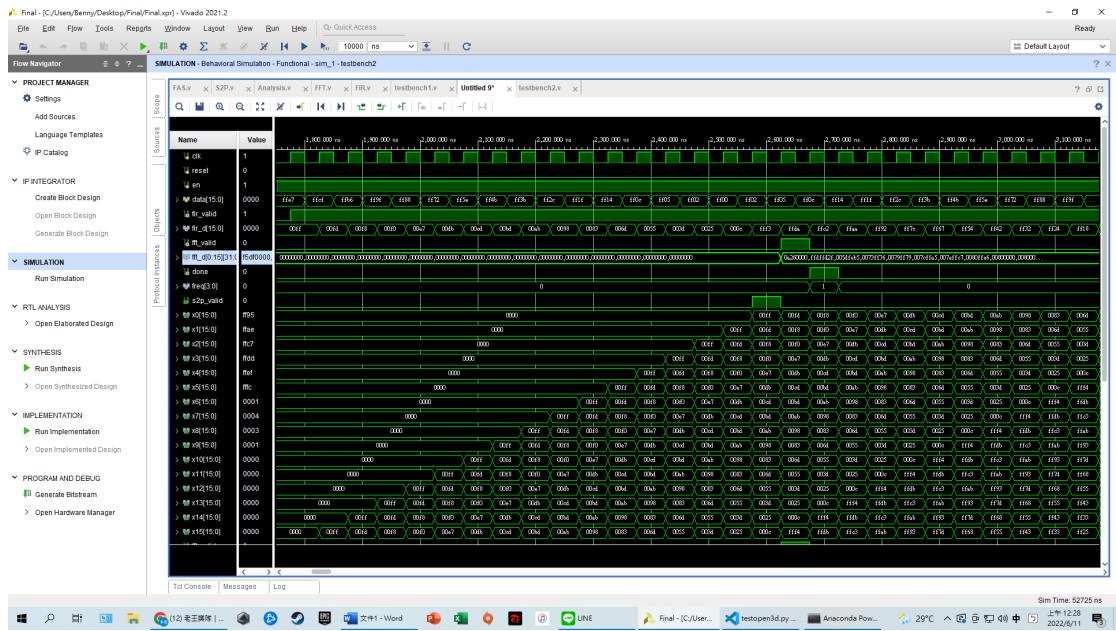
結果展示：

1. 波形 Simulate :

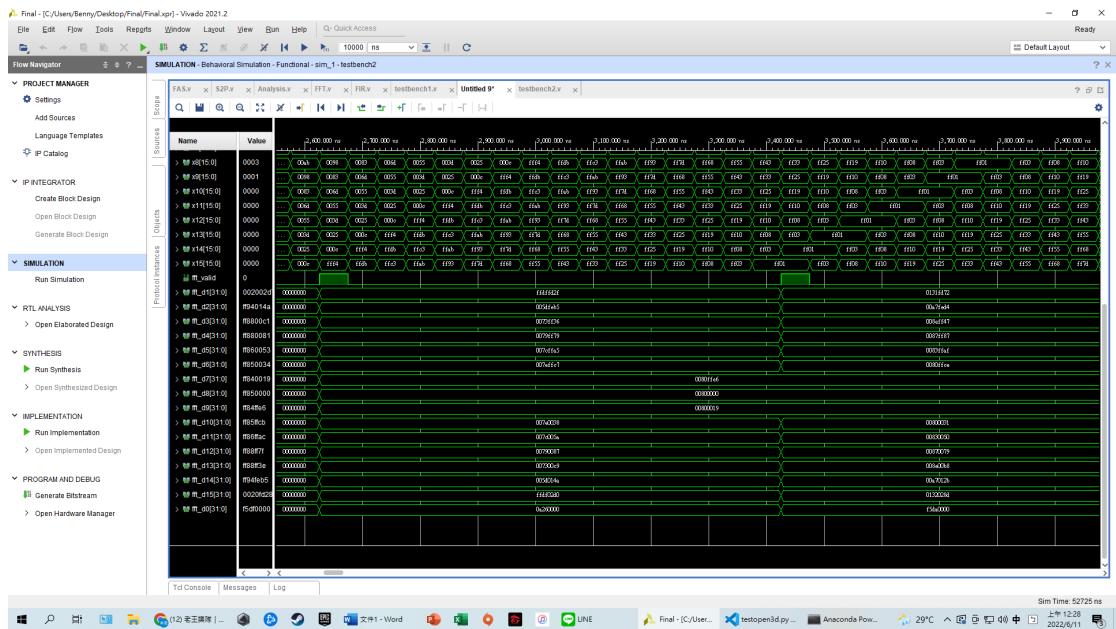
(1) FIR :



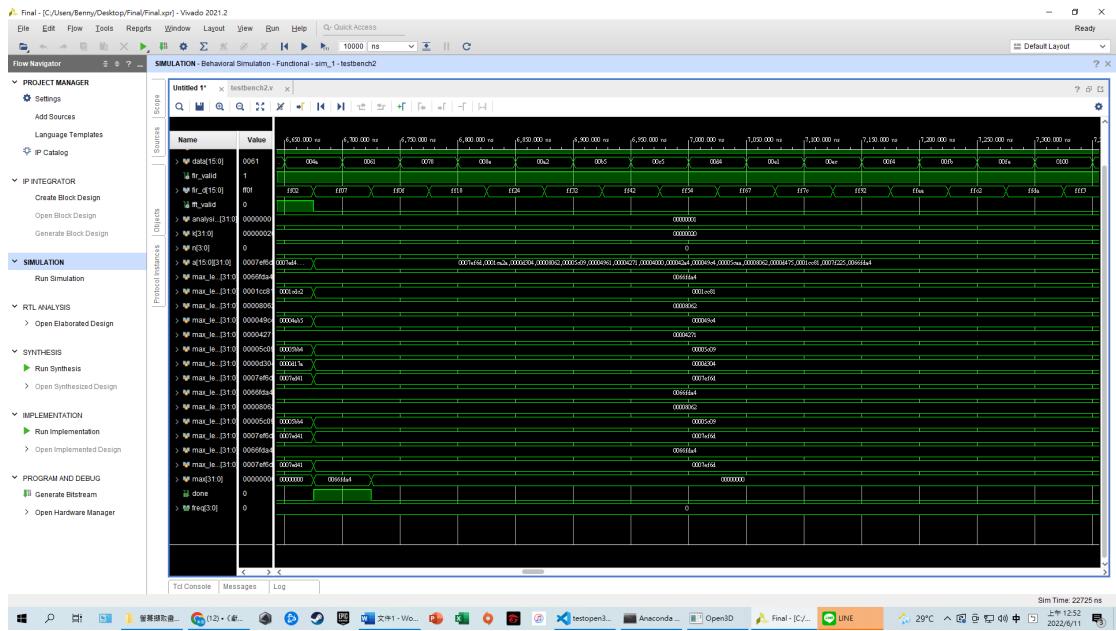
(2) S2P :



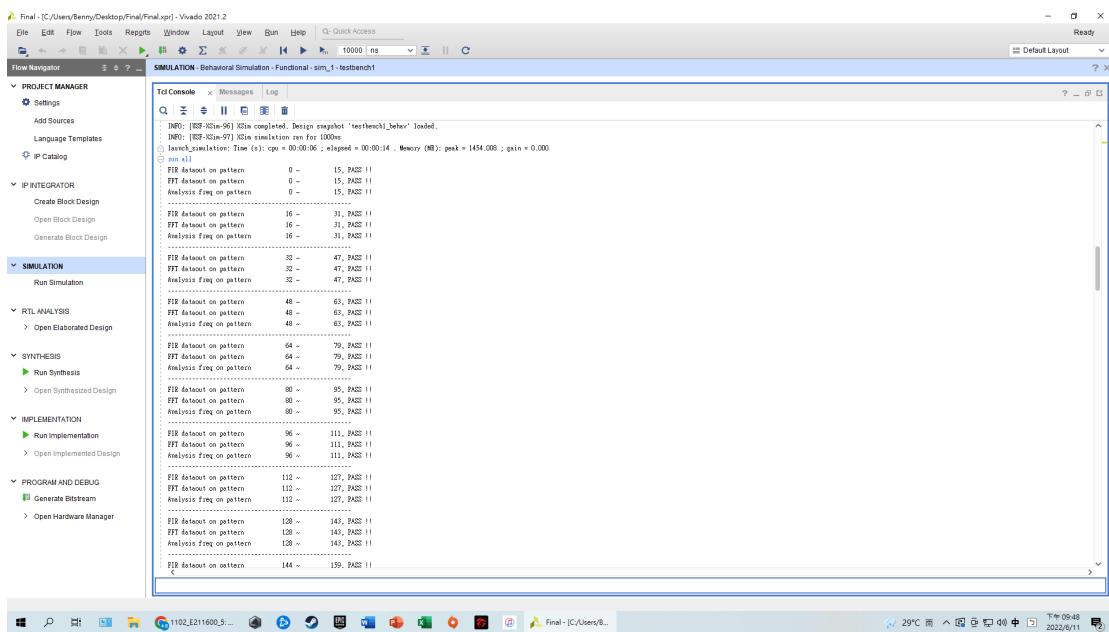
(3) FFT :



(4) Analysis :



(二) Testbench1 測試結果



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- Open Implemented Design

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Tcl Console Messages Log

```
FIR Analysis on pattern 144 ~ 159, PASS !!  
FFT Analysis on pattern 144 ~ 159, PASS !!  
Analysis Freq on pattern 144 ~ 159, PASS !!  
  
FIR Analysis on pattern 160 ~ 175, PASS !!  
FFT Analysis on pattern 160 ~ 175, PASS !!  
Analysis Freq on pattern 160 ~ 175, PASS !!  
  
FIR Analysis on pattern 176 ~ 191, PASS !!  
FFT Analysis on pattern 176 ~ 191, PASS !!  
Analysis Freq on pattern 176 ~ 191, PASS !!  
  
FIR Analysis on pattern 192 ~ 207, PASS !!  
FFT Analysis on pattern 192 ~ 207, PASS !!  
Analysis Freq on pattern 192 ~ 207, PASS !!  
  
FIR Analysis on pattern 208 ~ 223, PASS !!  
FFT Analysis on pattern 208 ~ 223, PASS !!  
Analysis Freq on pattern 208 ~ 223, PASS !!  
  
FIR Analysis on pattern 224 ~ 239, PASS !!  
FFT Analysis on pattern 224 ~ 239, PASS !!  
Analysis Freq on pattern 224 ~ 239, PASS !!  
  
FIR Analysis on pattern 240 ~ 255, PASS !!  
FFT Analysis on pattern 240 ~ 255, PASS !!  
Analysis Freq on pattern 240 ~ 255, PASS !!  
  
FIR Analysis on pattern 256 ~ 271, PASS !!  
FFT Analysis on pattern 256 ~ 271, PASS !!  
Analysis Freq on pattern 256 ~ 271, PASS !!  
  
FIR Analysis on pattern 272 ~ 287, PASS !!  
FFT Analysis on pattern 272 ~ 287, PASS !!  
Analysis Freq on pattern 272 ~ 287, PASS !!  
  
FIR Analysis on pattern 288 ~ 303, PASS !!  
FFT Analysis on pattern 288 ~ 303, PASS !!  
Analysis Freq on pattern 288 ~ 303, PASS !!
```

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Tcl Console Messages Log

```
Analysis Freq on pattern 380 ~ 393, PASS !!  
  
FIR Analysis on pattern 304 ~ 319, PASS !!  
FFT Analysis on pattern 304 ~ 319, PASS !!  
Analysis Freq on pattern 304 ~ 319, PASS !!  
  
FIR Analysis on pattern 320 ~ 335, PASS !!  
FFT Analysis on pattern 320 ~ 335, PASS !!  
Analysis Freq on pattern 320 ~ 335, PASS !!  
  
FIR Analysis on pattern 356 ~ 351, PASS !!  
FFT Analysis on pattern 356 ~ 351, PASS !!  
Analysis Freq on pattern 356 ~ 351, PASS !!  
  
FIR Analysis on pattern 352 ~ 367, PASS !!  
FFT Analysis on pattern 352 ~ 367, PASS !!  
Analysis Freq on pattern 352 ~ 367, PASS !!  
  
FIR Analysis on pattern 368 ~ 383, PASS !!  
FFT Analysis on pattern 368 ~ 383, PASS !!  
Analysis Freq on pattern 368 ~ 383, PASS !!  
  
FIR Analysis on pattern 384 ~ 399, PASS !!  
FFT Analysis on pattern 384 ~ 399, PASS !!  
Analysis Freq on pattern 384 ~ 399, PASS !!  
  
FIR Analysis on pattern 400 ~ 415, PASS !!  
FFT Analysis on pattern 400 ~ 415, PASS !!  
Analysis Freq on pattern 400 ~ 415, PASS !!  
  
FIR Analysis on pattern 416 ~ 431, PASS !!  
FFT Analysis on pattern 416 ~ 431, PASS !!  
Analysis Freq on pattern 416 ~ 431, PASS !!  
  
FIR Analysis on pattern 432 ~ 447, PASS !!  
FFT Analysis on pattern 432 ~ 447, PASS !!  
Analysis Freq on pattern 432 ~ 447, PASS !!  
  
FIR Analysis on pattern 448 ~ 463, PASS !!  
FFT Analysis on pattern 448 ~ 463, PASS !!  
Analysis Freq on pattern 448 ~ 463, PASS !!
```

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Tcl Console x Messages Log

```

FIR Analysis on pattern 464 ~ 479, PASS !!!
FFT Analysis on pattern 464 ~ 479, PASS !!!
Analysis Freq on pattern 464 ~ 479, PASS !!!
-----
FIR Analysis on pattern 480 ~ 495, PASS !!!
FFT Analysis on pattern 480 ~ 495, PASS !!!
Analysis Freq on pattern 480 ~ 495, PASS !!!
-----
FIR Analysis on pattern 496 ~ 511, PASS !!!
FFT Analysis on pattern 496 ~ 511, PASS !!!
Analysis Freq on pattern 496 ~ 511, PASS !!!
-----
FIR Analysis on pattern 512 ~ 527, PASS !!!
FFT Analysis on pattern 512 ~ 527, PASS !!!
Analysis Freq on pattern 512 ~ 527, PASS !!!
-----
FIR Analysis on pattern 528 ~ 543, PASS !!!
FFT Analysis on pattern 528 ~ 543, PASS !!!
Analysis Freq on pattern 528 ~ 543, PASS !!!
-----
FIR Analysis on pattern 544 ~ 559, PASS !!!
FFT Analysis on pattern 544 ~ 559, PASS !!!
Analysis Freq on pattern 544 ~ 559, PASS !!!
-----
FIR Analysis on pattern 560 ~ 575, PASS !!!
FFT Analysis on pattern 560 ~ 575, PASS !!!
Analysis Freq on pattern 560 ~ 575, PASS !!!
-----
FIR Analysis on pattern 576 ~ 591, PASS !!!
FFT Analysis on pattern 576 ~ 591, PASS !!!
Analysis Freq on pattern 576 ~ 591, PASS !!!
-----
FIR Analysis on pattern 592 ~ 607, PASS !!!
FFT Analysis on pattern 592 ~ 607, PASS !!!
Analysis Freq on pattern 592 ~ 607, PASS !!!
-----
FIR Analysis on pattern 608 ~ 623, PASS !!!
FFT Analysis on pattern 608 ~ 623, PASS !!!
Analysis Freq on pattern 608 ~ 623, PASS !!!
-----
FIR Analysis on pattern 624 ~ 639, PASS !!!

```

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Tcl Console x Messages Log

```

FIR Analysis on pattern 624 ~ 639, PASS !!!
FFT Analysis on pattern 624 ~ 639, PASS !!!
Analysis Freq on pattern 624 ~ 639, PASS !!!
-----
FIR Analysis on pattern 640 ~ 655, PASS !!!
FFT Analysis on pattern 640 ~ 655, PASS !!!
Analysis Freq on pattern 640 ~ 655, PASS !!!
-----
FIR Analysis on pattern 656 ~ 671, PASS !!!
FFT Analysis on pattern 656 ~ 671, PASS !!!
Analysis Freq on pattern 656 ~ 671, PASS !!!
-----
FIR Analysis on pattern 672 ~ 687, PASS !!!
FFT Analysis on pattern 672 ~ 687, PASS !!!
Analysis Freq on pattern 672 ~ 687, PASS !!!
-----
FIR Analysis on pattern 688 ~ 703, PASS !!!
FFT Analysis on pattern 688 ~ 703, PASS !!!
Analysis Freq on pattern 688 ~ 703, PASS !!!
-----
FIR Analysis on pattern 704 ~ 719, PASS !!!
FFT Analysis on pattern 704 ~ 719, PASS !!!
Analysis Freq on pattern 704 ~ 719, PASS !!!
-----
FIR Analysis on pattern 720 ~ 735, PASS !!!
FFT Analysis on pattern 720 ~ 735, PASS !!!
Analysis Freq on pattern 720 ~ 735, PASS !!!
-----
FIR Analysis on pattern 736 ~ 751, PASS !!!
FFT Analysis on pattern 736 ~ 751, PASS !!!
Analysis Freq on pattern 736 ~ 751, PASS !!!
-----
FIR Analysis on pattern 752 ~ 767, PASS !!!
FFT Analysis on pattern 752 ~ 767, PASS !!!
Analysis Freq on pattern 752 ~ 767, PASS !!!
-----
FIR Analysis on pattern 768 ~ 783, PASS !!!
FFT Analysis on pattern 768 ~ 783, PASS !!!
Analysis Freq on pattern 768 ~ 783, PASS !!!

```

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Tcl Console x Messages Log

```

FIR Analysis on pattern 784 ~ 799, PASS !!!
FFT Analysis on pattern 784 ~ 799, PASS !!!
Analysis Freq on pattern 784 ~ 799, PASS !!!

```

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Flow Navigator E 7

SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench1

Tcl Console Messages Log

```

Analysis Freq on pattern 769 ~ 763, PASS !!!
FIR Analysis on pattern 784 ~ 799, PASS !!!
FFT Analysis on pattern 784 ~ 799, PASS !!!
Analysis Freq on pattern 784 ~ 799, PASS !!!
FIR Analysis on pattern 800 ~ 815, PASS !!!
FFT Analysis on pattern 800 ~ 815, PASS !!!
Analysis Freq on pattern 800 ~ 815, PASS !!!
FIR Analysis on pattern 816 ~ 831, PASS !!!
FFT Analysis on pattern 816 ~ 831, PASS !!!
Analysis Freq on pattern 816 ~ 831, PASS !!!
FIR Analysis on pattern 832 ~ 847, PASS !!!
FFT Analysis on pattern 832 ~ 847, PASS !!!
Analysis Freq on pattern 832 ~ 847, PASS !!!
FIR Analysis on pattern 848 ~ 863, PASS !!!
FFT Analysis on pattern 848 ~ 863, PASS !!!
Analysis Freq on pattern 848 ~ 863, PASS !!!
FIR Analysis on pattern 864 ~ 879, PASS !!!
FFT Analysis on pattern 864 ~ 879, PASS !!!
Analysis Freq on pattern 864 ~ 879, PASS !!!
FIR Analysis on pattern 880 ~ 895, PASS !!!
FFT Analysis on pattern 880 ~ 895, PASS !!!
Analysis Freq on pattern 880 ~ 895, PASS !!!
FIR Analysis on pattern 896 ~ 911, PASS !!!
FFT Analysis on pattern 896 ~ 911, PASS !!!
Analysis Freq on pattern 896 ~ 911, PASS !!!
FIR Analysis on pattern 912 ~ 927, PASS !!!
FFT Analysis on pattern 912 ~ 927, PASS !!!
Analysis Freq on pattern 912 ~ 927, PASS !!!
FIR Analysis on pattern 928 ~ 943, PASS !!!
FFT Analysis on pattern 928 ~ 943, PASS !!!
Analysis Freq on pattern 928 ~ 943, PASS !!!
C

```

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Flow Navigator E 7

SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench1

Tcl Console Messages Log

```

FIR Analysis on pattern 906 ~ 911, PASS !!!
FFT Analysis on pattern 906 ~ 911, PASS !!!
Analysis Freq on pattern 906 ~ 911, PASS !!!
FIR Analysis on pattern 912 ~ 927, PASS !!!
FFT Analysis on pattern 912 ~ 927, PASS !!!
Analysis Freq on pattern 912 ~ 927, PASS !!!
FIR Analysis on pattern 928 ~ 943, PASS !!!
FFT Analysis on pattern 928 ~ 943, PASS !!!
Analysis Freq on pattern 928 ~ 943, PASS !!!
FIR Analysis on pattern 944 ~ 959, PASS !!!
FFT Analysis on pattern 944 ~ 959, PASS !!!
Analysis Freq on pattern 944 ~ 959, PASS !!!
FIR Analysis on pattern 960 ~ 975, PASS !!!
FFT Analysis on pattern 960 ~ 975, PASS !!!
Analysis Freq on pattern 960 ~ 975, PASS !!!
FIR Analysis on pattern 976 ~ 991, PASS !!!
FFT Analysis on pattern 976 ~ 991, PASS !!!
Analysis Freq on pattern 976 ~ 991, PASS !!!
FIR Analysis on pattern 992 ~ 1007, PASS !!!
FFT Analysis on pattern 992 ~ 1007, PASS !!!
Analysis Freq on pattern 992 ~ 1007, PASS !!!
Congratulations ! Testbench 1 ver2 Pass !!! All data have been generated successfully !!!
PASS
Finish called at time : 53600 ns : File "C:/Users/Benny/Desktop/Final/sim/sim_1/import/IL_FinalProject/testbench1.v" Line 332
| 
<

```

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Testbench2 測試結果：

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SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench2

Tcl Console Messages Log

```

INFO : [EDS-Xsim-96] Xsim completed. Design snapshot "testbench2_hevey" loaded.
INFO : [EDS-Xsim-97] Xsim simulation ran for 1000ns
INFO : [EDS-Xsim-98] Simulation Time (s): cpu = 00:00:00 ; elapsed = 00:00:07 . Memory (MB): peak = 1454.008 ; gain = 0.000
INFO : [EDS-Xsim-99] Simulation ended at time : 2725 ns : File "C:/Users/Benny/Desktop/Final/Final.srcs/sources_1/import/LL_FinalProject/testbench2.v" Line 297
run 10000 ns
TIR dataset on pattern 0 ~ 15, PASS !!
FFT dataset on pattern 0 ~ 15, PASS !!
ERROR at "ANALYZE2 Stage", the freq signal output 1 != expect 0
Analysis freq on pattern 16 ~ 31, PASS !!
TIR dataset on pattern 32 ~ 47, PASS !!
FFT dataset on pattern 32 ~ 47, PASS !!
Analysis freq on pattern 32 ~ 47, PASS !!
TIR dataset on pattern 48 ~ 63, PASS !!
FFT dataset on pattern 48 ~ 63, PASS !!
Analysis freq on pattern 48 ~ 63, PASS !!
TIR dataset on pattern 64 ~ 79, PASS !!
FFT dataset on pattern 64 ~ 79, PASS !!
Analysis freq on pattern 64 ~ 79, PASS !!
TIR dataset on pattern 96 ~ 95, PASS !!
FFT dataset on pattern 96 ~ 95, PASS !!
Analysis freq on pattern 96 ~ 95, PASS !!
TIR dataset on pattern 96 ~ 111, PASS !!
FFT dataset on pattern 96 ~ 111, PASS !!
Analysis freq on pattern 96 ~ 111, PASS !!
TIR dataset on pattern 112 ~ 127, PASS !!
FFT dataset on pattern 112 ~ 127, PASS !!
Analysis freq on pattern 112 ~ 127, PASS !!
TIR dataset on pattern 128 ~ 143, PASS !!
FFT dataset on pattern 128 ~ 143, PASS !!
Analysis freq on pattern 128 ~ 143, PASS !!

```

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SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench2

Tcl Console Messages Log

```

TIR dataset on pattern 144 ~ 159, PASS !!
FFT dataset on pattern 144 ~ 159, PASS !!
Analysis freq on pattern 144 ~ 159, PASS !!
TIR dataset on pattern 160 ~ 175, PASS !!
FFT dataset on pattern 160 ~ 175, PASS !!
Analysis freq on pattern 160 ~ 175, PASS !!
TIR dataset on pattern 176 ~ 191, PASS !!
FFT dataset on pattern 176 ~ 191, PASS !!
Analysis freq on pattern 176 ~ 191, PASS !!
TIR dataset on pattern 192 ~ 207, PASS !!
FFT dataset on pattern 192 ~ 207, PASS !!
Analysis freq on pattern 192 ~ 207, PASS !!
run 10000 ns
TIR dataset on pattern 208 ~ 223, PASS !!
FFT dataset on pattern 208 ~ 223, PASS !!
Analysis freq on pattern 208 ~ 223, PASS !!
TIR dataset on pattern 224 ~ 239, PASS !!
FFT dataset on pattern 224 ~ 239, PASS !!
Analysis freq on pattern 224 ~ 239, PASS !!
TIR dataset on pattern 240 ~ 255, PASS !!
FFT dataset on pattern 240 ~ 255, PASS !!
Analysis freq on pattern 240 ~ 255, PASS !!
TIR dataset on pattern 256 ~ 271, PASS !!
FFT dataset on pattern 256 ~ 271, PASS !!
Analysis freq on pattern 256 ~ 271, PASS !!
TIR dataset on pattern 272 ~ 287, PASS !!
FFT dataset on pattern 272 ~ 287, PASS !!
Analysis freq on pattern 272 ~ 287, PASS !!
TIR dataset on pattern 288 ~ 303, PASS !!
FFT dataset on pattern 288 ~ 303, PASS !!
Analysis freq on pattern 288 ~ 303, PASS !!

```

Windows Taskbar

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- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Protocol Instances

Tcl Console

```

FFT dataset on pattern 304 ~ 319, PASS !!!
Analysis freq on pattern 304 ~ 319, PASS !!!
FFT dataset on pattern 309 ~ 335, PASS !!!
FFT dataset on pattern 320 ~ 335, PASS !!!
Analysis freq on pattern 320 ~ 335, PASS !!!
FFT dataset on pattern 336 ~ 351, PASS !!!
FFT dataset on pattern 337 ~ 351, PASS !!!
Analysis freq on pattern 336 ~ 351, PASS !!!
FFT dataset on pattern 352 ~ 367, PASS !!!
FFT dataset on pattern 352 ~ 367, PASS !!!
Analysis freq on pattern 352 ~ 367, PASS !!!
FFT dataset on pattern 368 ~ 383, PASS !!!
FFT dataset on pattern 369 ~ 383, PASS !!!
Analysis freq on pattern 368 ~ 383, PASS !!!
FFT dataset on pattern 384 ~ 399, PASS !!!
FFT dataset on pattern 394 ~ 399, PASS !!!
Analysis freq on pattern 394 ~ 399, PASS !!!
FFT dataset on pattern 400 ~ 415, PASS !!!
FFT dataset on pattern 400 ~ 415, PASS !!!
Analysis freq on pattern 400 ~ 415, PASS !!!
run 100000 ns
FFT dataset on pattern 416 ~ 431, PASS !!!
FFT dataset on pattern 416 ~ 431, PASS !!!
Analysis freq on pattern 416 ~ 431, PASS !!!
FFT dataset on pattern 432 ~ 447, PASS !!!
FFT dataset on pattern 432 ~ 447, PASS !!!
Analysis freq on pattern 432 ~ 447, PASS !!!
FFT dataset on pattern 448 ~ 463, PASS !!!
FFT dataset on pattern 449 ~ 463, PASS !!!
Analysis freq on pattern 448 ~ 463, PASS !!!
FFT dataset on pattern 464 ~ 479, PASS !!!
C

```

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Protocol Instances

Tcl Console

```

FFT dataset on pattern 464 ~ 479, PASS !!!
FFT dataset on pattern 464 ~ 479, PASS !!!
Analysis freq on pattern 464 ~ 479, PASS !!!
FFT dataset on pattern 480 ~ 495, PASS !!!
FFT dataset on pattern 490 ~ 495, PASS !!!
Analysis freq on pattern 480 ~ 495, PASS !!!
FFT dataset on pattern 496 ~ 511, PASS !!!
FFT dataset on pattern 496 ~ 511, PASS !!!
Analysis freq on pattern 496 ~ 511, PASS !!!
FFT dataset on pattern 512 ~ 527, PASS !!!
FFT dataset on pattern 512 ~ 527, PASS !!!
Analysis freq on pattern 512 ~ 527, PASS !!!
FFT dataset on pattern 528 ~ 543, PASS !!!
FFT dataset on pattern 528 ~ 543, PASS !!!
Analysis freq on pattern 528 ~ 543, PASS !!!
FFT dataset on pattern 544 ~ 559, PASS !!!
FFT dataset on pattern 544 ~ 559, PASS !!!
Analysis freq on pattern 544 ~ 559, PASS !!!
FFT dataset on pattern 560 ~ 575, PASS !!!
FFT dataset on pattern 560 ~ 575, PASS !!!
Analysis freq on pattern 560 ~ 575, PASS !!!
FFT dataset on pattern 576 ~ 591, PASS !!!
FFT dataset on pattern 576 ~ 591, PASS !!!
Analysis freq on pattern 576 ~ 591, PASS !!!
run 100000 ns
FFT dataset on pattern 600 ~ 622, PASS !!!
FFT dataset on pattern 600 ~ 623, PASS !!!
Analysis freq on pattern 600 ~ 623, PASS !!!
C

```

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Protocol Instances

Tcl Console

```

FFT dataset on pattern 600 ~ 622, PASS !!!
FFT dataset on pattern 600 ~ 623, PASS !!!
Analysis freq on pattern 600 ~ 623, PASS !!!
C

```

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Tcl Console

```

FFT dataset on pattern 600 ~ 603, PASS !!
Analysis freq on pattern 600 ~ 603, PASS !!

FFT dataset on pattern 624 ~ 629, PASS !!
FFT dataset on pattern 624 ~ 630, PASS !!
Analysis freq on pattern 624 ~ 629, PASS !!

FFT dataset on pattern 640 ~ 655, PASS !!
FFT dataset on pattern 640 ~ 655, PASS !!
Analysis freq on pattern 640 ~ 655, PASS !!

FFT dataset on pattern 656 ~ 671, PASS !!
FFT dataset on pattern 656 ~ 671, PASS !!
Analysis freq on pattern 656 ~ 671, PASS !!

FFT dataset on pattern 672 ~ 687, PASS !!
FFT dataset on pattern 672 ~ 687, PASS !!
Analysis freq on pattern 672 ~ 687, PASS !!

FFT dataset on pattern 688 ~ 703, PASS !!
FFT dataset on pattern 688 ~ 703, PASS !!
Analysis freq on pattern 688 ~ 703, PASS !!

FFT dataset on pattern 704 ~ 719, PASS !!
FFT dataset on pattern 704 ~ 719, PASS !!
Analysis freq on pattern 704 ~ 719, PASS !!

FFT dataset on pattern 720 ~ 735, PASS !!
FFT dataset on pattern 720 ~ 735, PASS !!
Analysis freq on pattern 720 ~ 735, PASS !!

FFT dataset on pattern 736 ~ 751, PASS !!
FFT dataset on pattern 736 ~ 751, PASS !!
Analysis freq on pattern 736 ~ 751, PASS !!

FFT dataset on pattern 752 ~ 767, PASS !!
FFT dataset on pattern 752 ~ 767, PASS !!
Analysis freq on pattern 752 ~ 767, PASS !!

FFT dataset on pattern 768 ~ 783, PASS !!
FFT dataset on pattern 768 ~ 783, PASS !!
Analysis freq on pattern 768 ~ 783, PASS !!

<

```

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Tcl Console

```

FFT dataset on pattern 760 ~ 765, PASS !!
FFT dataset on pattern 760 ~ 765, PASS !!
Analysis freq on pattern 760 ~ 763, PASS !!

FFT dataset on pattern 784 ~ 799, PASS !!
FFT dataset on pattern 784 ~ 799, PASS !!
Analysis freq on pattern 784 ~ 799, PASS !!

FFT dataset on pattern 800 ~ 815, PASS !!
FFT dataset on pattern 800 ~ 815, PASS !!
Analysis freq on pattern 800 ~ 815, PASS !!

run 10000 ns
FFT dataset on pattern 816 ~ 831, PASS !!
FFT dataset on pattern 816 ~ 831, PASS !!
Analysis freq on pattern 816 ~ 831, PASS !!

FFT dataset on pattern 832 ~ 847, PASS !!
FFT dataset on pattern 832 ~ 847, PASS !!
Analysis freq on pattern 832 ~ 847, PASS !!

FFT dataset on pattern 848 ~ 863, PASS !!
FFT dataset on pattern 848 ~ 863, PASS !!
Analysis freq on pattern 848 ~ 863, PASS !!

FFT dataset on pattern 864 ~ 879, PASS !!
FFT dataset on pattern 864 ~ 879, PASS !!
Analysis freq on pattern 864 ~ 879, PASS !!

FFT dataset on pattern 880 ~ 895, PASS !!
FFT dataset on pattern 880 ~ 895, PASS !!
Analysis freq on pattern 880 ~ 895, PASS !!

FFT dataset on pattern 896 ~ 911, PASS !!
FFT dataset on pattern 896 ~ 911, PASS !!
Analysis freq on pattern 896 ~ 911, PASS !!

FFT dataset on pattern 912 ~ 927, PASS !!
FFT dataset on pattern 912 ~ 927, PASS !!
Analysis freq on pattern 912 ~ 927, PASS !!

<

```

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Tcl Console

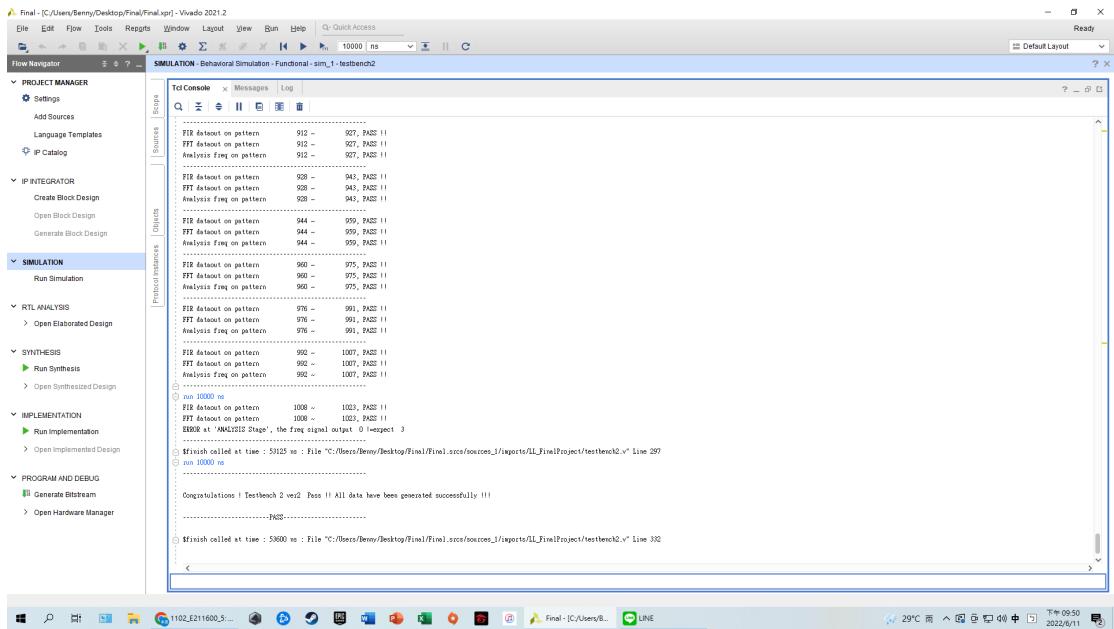
```

run 10000 ns
FFT dataset on pattern 896 ~ 911, PASS !!
FFT dataset on pattern 896 ~ 911, PASS !!
Analysis freq on pattern 896 ~ 911, PASS !!

FFT dataset on pattern 912 ~ 927, PASS !!
FFT dataset on pattern 912 ~ 927, PASS !!
Analysis freq on pattern 912 ~ 927, PASS !!

<

```



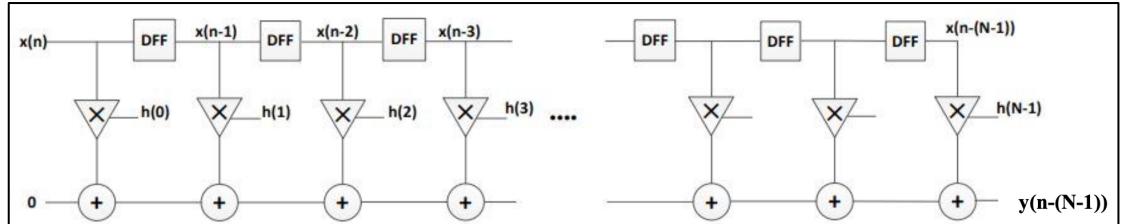
程式說明與遇到的困難：

一、FIR

(1) 程式碼說明

1. 變數說明

此次 FIR 濾波器有 32 階，需要 31 顆 DFF，故宣告 31 個 16bits 的 signed reg D 來儲存輸入的 data (如下圖)



DFF 儲存的資料需要與 20bits 的係數相乘，其積是 36bits，故宣告 32 個 36bits 的 signed reg mul 儲存乘法結果。最後要將乘法結果相加得到輸出，故宣告一個 36bits 的 reg sum 儲存。整數 k 用於每次將 DFF 的資料平移時的 for 迴圈使用；整數 counter 用於紀錄目前已輸入幾個資料。

2. 程式邏輯說明

程式分為兩個 always block 和一個 assign block，第一個 always block 在 clock 正緣或 rst 正緣觸發，達成非同步 reset 的效果。若觸發時 rst 為 1，將所有變數及 DFF 歸零；若 rst 不為 1 且 data_valid 為 1，將 D[k-1] 儲存的資料以 non-blocking

方式平移給 $D[k]$ ，並把 counter 加一，若 counter 大於或等於 32，代表所有 DFF 都充滿有效資料，可將 fir_valid 設為 1。

第二個 always block 負責乘法運算，在 clock 正緣時觸發，若 data_valid 為 1，則將對應的 DFF 與係數相乘，之後以 non-blocking 的方式賦值給對應的 mul，最後以 blocking 的方式，把所有的 mul 相加並賦值給 sum，這時使用 blocking 可確保 sum 計算時是以最新的 mul 計算。

雖然 sum 有 36bits，但 output 的 fir_d 僅有 16bits，故從 MSB 開始，將 sum[31:16]assign 給 fir_d 作為輸出。

(2) 遇到的問題與解決辦法

一開始在計算時，忽略了 2 進位相乘時，結果的 bit 數會是兩個 bit 相加，直接計算完賦值給 fir_d 時會出現溢位問題，導致結果錯誤。解決辦法為將乘法與加法步驟分開，並要小心計算 reg 所需的 bit 數，最後取 MSB 開始的 16bits 賦值給 fir_d。

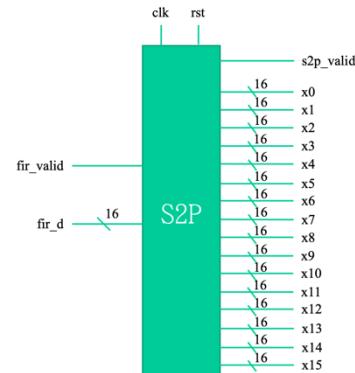
在構思時，發現係數的十進位值與二進位不同，因此不知道如何計算乘法。解決辦法為在 verilog 中，沒有小數點的存在，計算浮點數的乘法時，是將結果視為整數計算後，再人工決定小數點的位置並選擇取值範圍。

二、S2P

(1) 程式碼說明

1. 變數說明：

S2P 顧名思義是 serial to parallel，能將一個一個進來的訊號做平行輸出。將 FIR 個別傳入的 16 個 x 值，一次輸出給 16 個 FFT。過程利用 count 計入傳入次數。



2. 程式邏輯說明：

reset==1 時需要把儲存的訊號全歸 0。reset==0/clock triggers 且 fir_valid==1 時將 fir_d 存入 x_{15} ，同時將 x_i 皆前推一階(x_{i-1})。最後在 count==15 時， $s2p_valid==1$ 並且將 x_0-x_{15} 輸出給 FFT。輸出之後再把 $s2p_valid$ 歸零，直到下一批 16 個變數都到齊之後才會拉起來。

(2) 遇到的問題與解決辦法：

原先我們是開 16 個 reg(r0-r15) 存一個個進來的 x_i ，等到最後一個 FIR_d 進來才把 r0-r15 存進 x0-x15。但看波形發現 x0-x15 會晚一個 cycle 才送給 FFT，所以一開始我們的解決方式是先把 r15 拿

掉，直接將最後一個進來的 FIR_d 紙 x15，同時將 $x_0 \leq r_0$, $x_1 \leq r_1 \dots$ 。

不過後來發現傳入的資料仍然有誤。事後參考助教的 code 發現其實不需要多開 r_0-r_{15} ，只需要將每次進來的資料往前推一個 x ，等到 16 個進來，再把 s2p_valid 打開，此時 x_i 的數據才有用，也不需擔心 FIR 進來的值會直接傳給 x_i 而無法達到平行傳輸的效果。

三、FFT

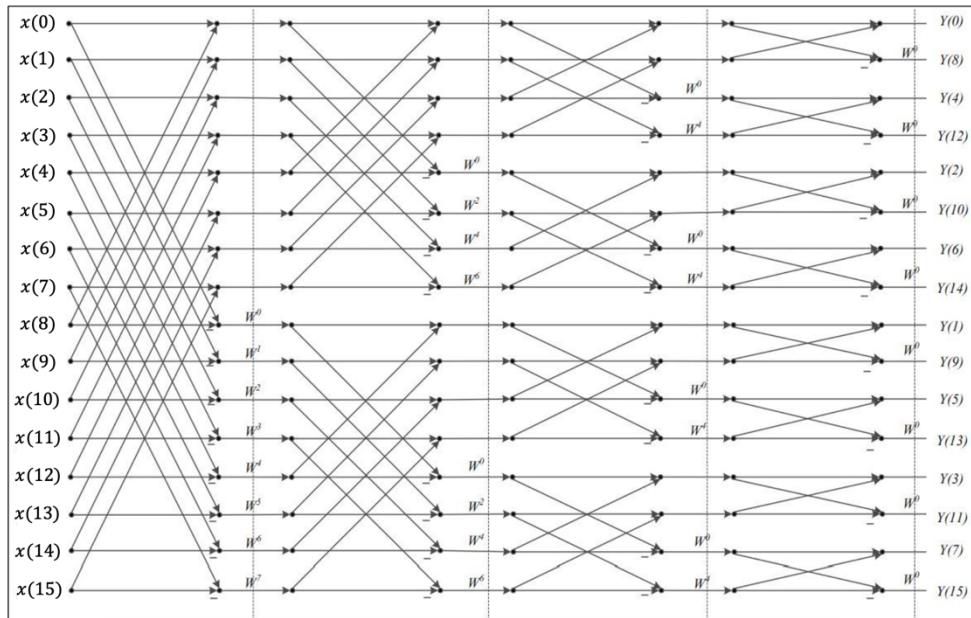
(1) 程式碼說明

1. 變數說明：

由 S2P 傳進來的 16 個值放在 input 變數： x_0-x_{15} ，經過 FFT 運算之後，output 變數存在 $\text{fft_d}0-\text{fft_d}15$ 。依據運算需求開了四層 mux 的 wire，且因為數值有實部及虛部之分，所以每層 mux 有分層 R 和 I 兩種。例如 `signed [15:0] mul_S1_R0~mul_S1_R7`、`signed [47:0] mul_S1_R8~mul_S1_R15`、`signed [31:0] mul_S4_R2~mul_S4_R14`。

2. 程式邏輯說明：

照著下圖 FFT hardware architecture 刻出 FFT 運算後的數值。數值運算完後把數值存入 $\text{fft_d}0-\text{fft_d}15$ ，同時把 fft_valid 打開，使其傳入 Analysis 找最大值。



其中 $W^n = \text{FFT coefficient}$ ，而 $W^n = W_{real}^n + jW_{imag}^n$

而 $\text{fft_a} = X + Y$ 、 $\text{fft_b} = (X - Y) \times W^n$ 。

$$[(a + bj) - (c + dj)] \times (W_{real}^n + jW_{imag}^n)$$

《註》 W_{real}^n 、 W_{imag}^n 為已知參數，請見檔案 FFT_coefficient.dat

《註》實部和虛部的運算方式如下表

Real part of fft_b	$(a - c) \times W_{real}^n + (d - b) \times W_{imag}^n$
imaginary part of fft_b	$(a - c) \times W_{imag}^n + (b - d) \times W_{real}^n$

(2) 遇到的問題與解決方法

我們有照著架構圖一一列出數學式，但過程遇到不少問題。一開始是我們不知道如果兩數要做乘法的話，要記得多開位元數，否則乘出來的數值會 overflow，例如若 16bit 的 data 要乘上 32bit 的係數 w，則需要開 [47:0] 的變數存取結果。

解決這個問題之後，接著我們遇到取值的範圍抓取問題，由於變數的位元空間有分給整數和小數，我們要清出知道第一個 bit 是給 sign、哪幾位是給整數，以及後面幾位給小數。否則如果抓錯範圍可能會導致運算結果出錯。

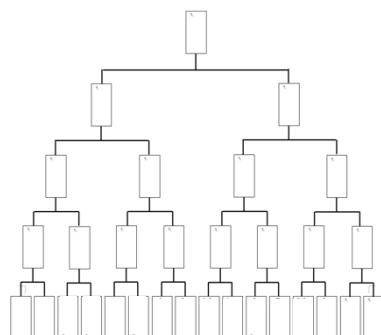
事後參考助教的 code 我們發現每一層的運算可以寫在 always 外面，直接做 combinational 電路，然後當要賦予值給 fft_d0~fft_d15 時再寫在 always 裡面即可，因為這時才需要用到 sequential 暫存功能。

四、Analysis

(1) 程式碼說明

1. 變數說明

FFT 會輸出 16 個波的實部與虛部做 analysis 的 input，analysis 要計算出每個波的振幅並比較，因此宣告 16 個 32bits 的 signed reg a 來儲存計算完的振幅。比較振幅大小時，採用多工器的方式比較（如下圖）



故宣告 max_level_1 1~8，8 個 32bits 的 signed reg 儲存第一層比較結果；max_level_2 1~4，4 個 32bits 的 signed reg 儲存第二層比較結果；max_level_3 1~2，2 個 32bits 的 signed reg 儲存第三層比較結果；32bits 的 signed reg max 儲存最終結果。4bits 的 signed reg n 是儲存結果頻率的暫存器。整數 k 用於將 a 全數歸零。

2. 程式邏輯說明

程式分為一個 always block 和一個 assign block，always block 在 clock 正緣或 rst 正緣時觸發，達成非同步 reset 的效果。若觸發時 rst 為 1，將所有變數及歸零；若 rst 不為 1 且 fft_valid 為 1，則以 blocking 方式，計算出各個波的振幅再賦值給對應的 a 儲存。之後開始進行振幅比較得到 max，最後比對 max 與哪個 a 的值相等，找出最大振幅是第幾個波（即 a 的 index）賦值給 n，並將 done 設為 1。

assign block 會將 n 儲存的主頻編號賦值給 freq 作為輸出。

(2) 遇到的問題與解決辦法

- 一開始的振幅比較是以 non-blocking 的方式寫，但波形圖會一直維持 0。解決辦法為將 non-blocking 改為 blocking，因為比較時下一層會用到上一層比較的結果，若寫成 non-blocking 會在 end 的時候才給值，自然就會變成大家都是 0，改成 blocking 後，每一層比較完結果立刻就會被儲存，下一層的比較才有依據及資料。

五、FAS

(1) 程式碼說明

做為最上端的 module，呼叫 FIR、S2P、FFT、和 Analysis 並負責將各自的 input 和 output 連接。

(2) 遇到的問題與解決辦法

這份沒有遇到問題，基本上就是將 FIR、S2P、FFT 和 Analysis 之間的所需的輸入輸出做對應之模組變數呼叫與串聯。

心得

組員一 林珮玉 E24084096

雖然這次 Final Project 很爆炸，但是我學到超級多的，真的十分有成就感，而且還有機會教其他同學！這次我負責打 S2P, FFT, Analysis，雖然花一下午完成，不過跑 testbench 的時候發現一堆問題，我們反覆修改了好幾次，還是找不出結果，事後有請修過超大的同學教我，學到超多，包括釐清 always 和 assign 的差別，知道到如果要用 reg 就不能寫在 assign，也更懂的 combinational 和 sequential circuit 的使用情境。最重要的是透過這次的專案體驗，我終於知道做電路設計的辛苦了，接線瑣碎又沒辦法馬上看到模擬的結

果，我可能不會走電路設計吧 QQ 過程最感謝我的夥伴本恩，因為我的電腦沒有 vivado，只好先用 visual studio 打完再傳檔案給他測，這樣遠端討論確實會比較反鎖些，很謝謝他的積極我們才能順利完成。最後也謝謝助教無私提供 FFT 檔案讓我們可以參考，因為之前都只練填空題，自己打過之後才發現有超多問題，有時候直接偷看解答有時候也是很棒且有效率的學習 XD 整體來說，我十分感謝有這次的實戰機會，讓我能以真的了解 verilog 的神秘語法！

組員二 廖本恩 E24102179

這一次的 final project 不僅分量多，每個檔案還都要自己重頭開始寫。雖然很痛苦且 debug 很不容易，但寫完後發現自己對 verilog 的理解更深，真的有感受到電路與軟體的差別，如硬體對四則運算和浮點數的處理就與軟體有很大的不同；non-blocking 與 blocking 該如何選擇。對 always、reg、wire 有更深的認識，以前都覺得 wire 跟 reg 沒有甚麼差別，這次才體會到邏輯中有記憶性的元件與單純接線的不同。看到 assign 時也不再把它當成簡單的賦值，而是真的以接一條線過去的角度看它，之前都會被軟體的想法誤導，覺得 verilog 應該也是一行一行執行，時常搞不清楚哪個功能該寫在哪行，但有了接線的概念後，就知道其時它只是描述一個電路的行為，將接線以語言描述出來而已，沒有想像中那麼複雜。此外，也重新認識計概中為什麼要學這麼多二進位的知識，在這次都是數值計算的 project 有很大的幫助。最後也重新思考底層與高階語言的利弊，平常總抱怨底層的語言如 C 和 verilog 很麻煩，要考慮很多細節，高階語言則用一些簡單的語法就可以達成。但實作這次 project 後，發現在使用底層語言時，會讓自己以計算機的方式思考，真實的模擬一次這些二進制數在計算機裡運算的邏輯，真正的了解運作的機制，相信在日後有關課程能有很大的助益。

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這次的 project 實際因為許多事情而沒能幫上什麼忙，甚至幾乎沒有時間重新理解並製作完整的一個部件，資訊只能全靠組員沒做成的內容獲得，有做過與助教做法相似的猜測，但也就止步如此，甚至從頭到尾都沒想到補數的部分，只有分析助教程式時才算是有對同組成員的貢獻。謝謝組員們在我後三分之一學期時的各種作業與考試的壓力下幫了我許多，也謝謝助教在這段時間對大家的協助。