ECE 445 Assignment 4

PEI-YU LIN

Code

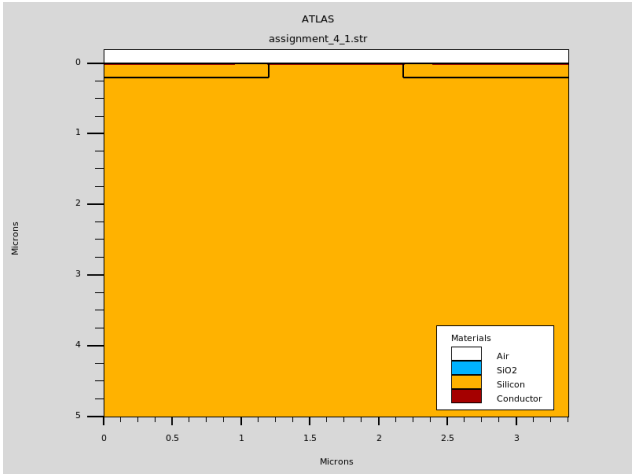
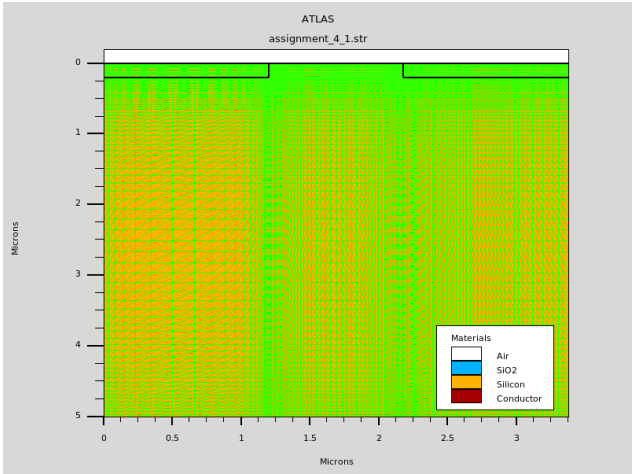
```
go atlas

#set constant
#Gate width and length
set LG=1 #2, 1(default), 0.5
set WG=0.02 #10nm, 20nm(default)

#Source width and length
set WS=0.2
set LS=1.2

#Drain width and length
set WD=0.2
set LD=1.2

#Silicon width and length
set WSi=5
set LSi=$LG-0.02+2.4

mesh  space.mult=2.0

x.mesh loc=0.00 spac=0.02
x.mesh loc=0.50 spac=0.08
x.mesh loc=$LS-0.01 spac=0.005
x.mesh loc=$LS spac=0.005
x.mesh loc=$LSi/2 spac=0.02
x.mesh loc=$LSi-$LD spac=0.005
x.mesh loc=$LSi-$LD+0.01 spac=0.008
x.mesh loc=$LSi spac=0.02
```

```
#
y.mesh loc=0.00 spac=0.002
y.mesh loc=$WG/2 spac=0.005
y.mesh loc=$WG spac=0.005
y.mesh loc=$WG+$WD/2 spac=0.008
y.mesh loc=$WG+$WD spac=0.005
y.mesh loc=$WG+$WSi/2 spac=0.08
y.mesh loc=$WG+$WSi spac=0.02


#region
region num=1 material=air
region num=2 y.min=0 y.max=$WG x.min=$LS-0.01 x.max=$LS-0.01+$LG material=sio2
region num=3 y.min=$WG y.max=$WG+$WSi x.min=0 x.max=$LSi material=silicon
region num=4 y.min=$WG y.max=$WG+$WS x.min=0 x.max=$LS material=silicon
region num=5 y.min=$WG y.max=$WG+$WD x.min=$LSi-$LD x.max=$LSi material=silicon

# Electrode
electr  name=Gate  x.min=$LS-0.01  length=$LG
electr  name=Source  x.min=0  length=1  y.min=$WG  y.max=$WG
electr  name=Drain  x.min=$LSi-1  length=1  y.min=$WG  y.max=$WG

# Doping
doping  p.type conc=1e16 uniform region=3
doping  n.type conc=1e19 uniform region=4
doping  n.type conc=1e19 uniform region=5

# Material
#material material=Si user.default=silicon

# Models
model srh drift.diff print

# Contact
contact name=Gate
contact name=Source
contact name=Drain
```

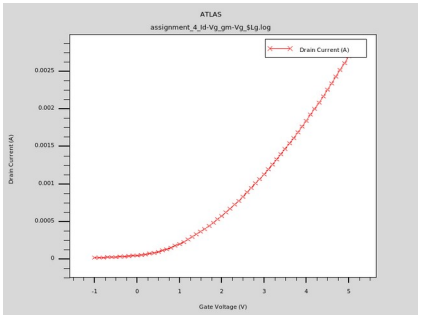
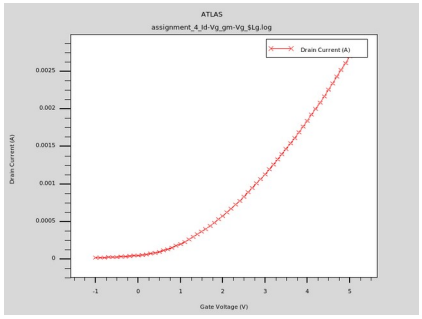
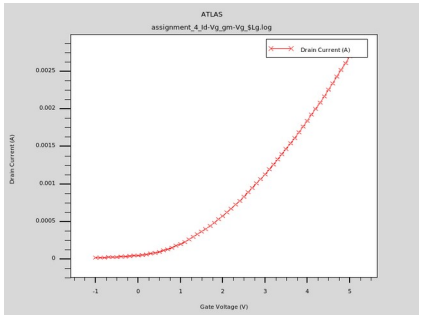
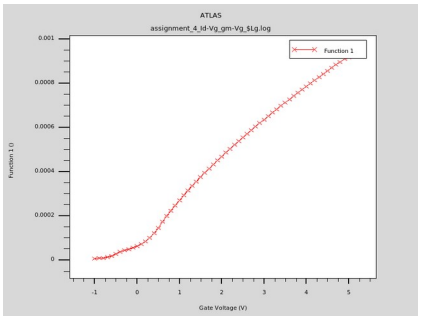
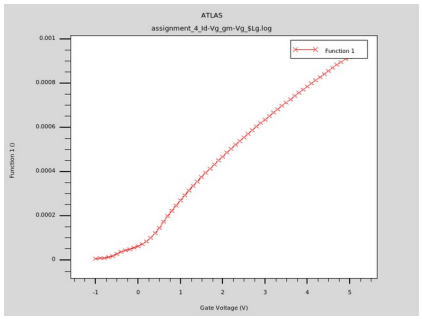
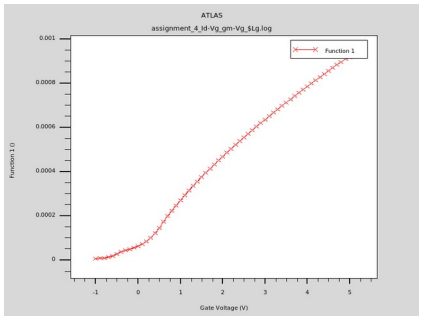
```
# Method
method newton trap

# Output
output band.param con.band val.band flowline u.bbt

# Save the structure
save outf=assignment_4_1.str
#tonyplot assignment_4_1.str

# Q1-4
#solve init
#solve Vdrain=10
#log outfile=assignment_4_Id-Vg_gm-Vg_$Lg.log
#solve Vgate=-1 vstep=0.1 vfinal=8 name=gate
#log off

# Q5: VG changes from 0V-5V
solve init
log outfile=assignment_4_Id-Vg-0.log
solve Vgate=0 name=gate
solve Vdrain=0 vstep=0.2 vfinal=5 name=drain
log off

solve init
log outfile=assignment_4_Id-Vg-1.log
solve Vgate=1 name=gate
solve Vdrain=0 vstep=0.2 vfinal=5 name=drain
log off

solve init
log outfile=assignment_4_Id-Vg-2.log
solve Vgate=2 name=gate
solve Vdrain=0 vstep=0.2 vfinal=5 name=drain
log off
```

```
solve init
log outfile=assignment_4_Id-Vg-3.log
solve Vgate=3 name=gate
solve Vdrain=0 vstep=0.2 vfinal=5 name=drain
log off

solve init
log outfile=assignment_4_Id-Vg-4.log
solve Vgate=4 name=gate
solve Vdrain=0 vstep=0.2 vfinal=5 name=drain
log off

solve init
log outfile=assignment_4_Id-Vg-5.log
solve Vgate=5 name=gate
solve Vdrain=0 vstep=0.2 vfinal=5 name=drain
log off

quit
```

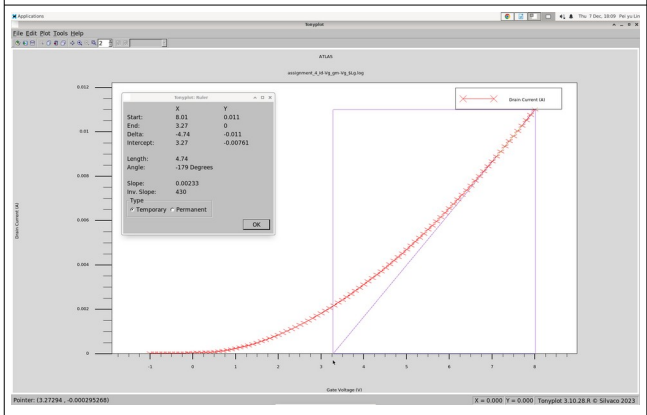
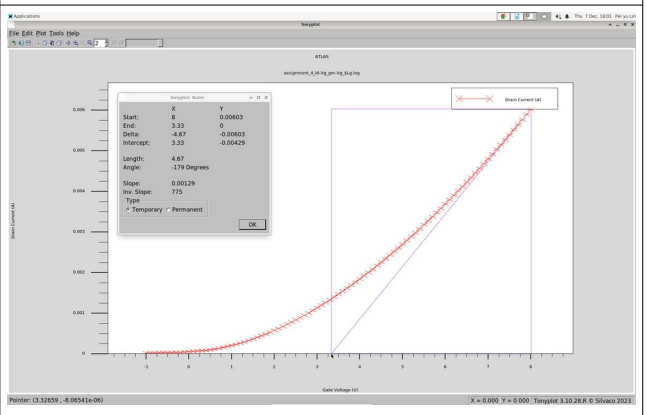
Meshing and Structure

Structure	Meshing
	

Q1

Plot Drain current (ID) vs Gate voltage (VG)		
LG=2um	LG=1um	LG=0.5um
		
Plot the transconductance (gm) vs Gate voltage (VG) * transconductance = dydx(drain current, gate voltage)		
LG=2um	LG=1um	LG=0.5um
		

Q2

Plot Drain current (ID) vs Gate voltage (VG)	
d = 10nm → VT = 3.27	D = 20nm → VT = 3.33
	

Explain the reason that threshold voltage change with oxide thickness

For p-type Si (“NMOS”):

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\psi_B)}}{C_{ox}}$$, and Cox=E0*Er/tox

As you can see, a thinner oxide layer increases the gate capacitance, which lowers the threshold voltage needed to form a conductive channel in the semiconductor. Additionally, when the oxide is very thin, electrons can tunnel through it more easily, altering the threshold voltage. The electric field across the oxide also becomes stronger with a thinner layer, affecting the voltage needed to invert the semiconductor surface. These concepts are essential in understanding how scaling down the oxide layer in MOSFETs impacts their electrical properties and overall performance.

Q3

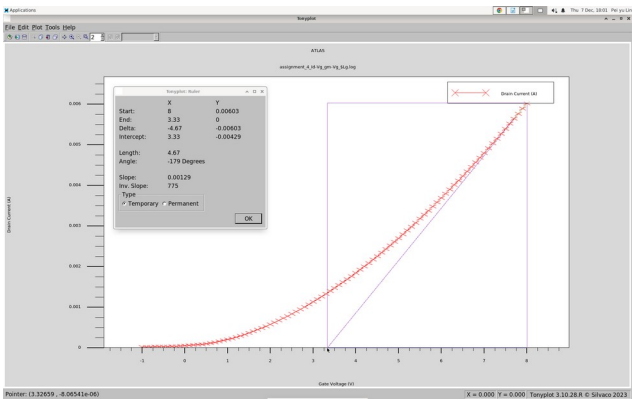
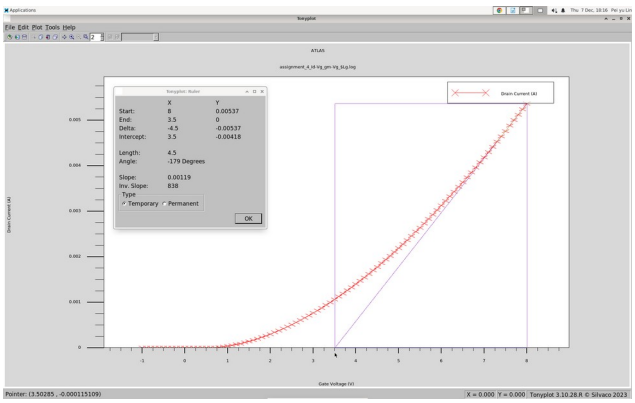
If we would replace SiO2 with HfO2 and want to keep the threshold voltage same as SiO2 with 10 nm thickness, what is the HfO2 thickness we can use?
Explain how to calculate the thickness of HfO2.

$E_{SiO2} / t_{sio2} = E_{HfO2} / t_{HfO2}$ => 3.9 / 1nm = 25 / t_{HfO2} => t_{HfO2} = 6.41 nm

The thickness of HfO2 should be 6.41nm to have the simular threshold voltage as SiO2 with 10nm thickness as well as under the same other parameters.

Q4

Plot ID vs VG

Substrate Doping concentration=1e15	Substrate Doping concentration=1e16
	

Explain the threshold voltage change

For p-type Si (“NMOS”):

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\psi_B)}}{C_{ox}}$$, and Cox=E0*Er/tox

As you can see, increasing the substrate doping concentration in a MOSFET affects its threshold voltage. A higher doping concentration in the substrate leads to an increase in the charge carrier concentration. This change requires a higher gate voltage to establish the inversion layer, where a conductive channel forms at the semiconductor-oxide interface. Essentially, more positive charge is needed at the gate to counterbalance the increased negative charge from the higher doping. As a result, the threshold voltage, which is the minimum gate voltage needed to create this conductive channel, increases with the increase in substrate doping concentration.

Q5

Plot ID vs VD (0-5 V with a step of 0.2 V) graph for different VG (0-5 V, with step of 1 V)