

CDA 4203L Spring 2018
Computer System Design Lab
Lab 2 – Behavioral and Structural Verilog
Handed out on Monday, 29th January
Due Date: 11:59 PM, Friday, 9th February

This is an individual assignment. No teaming allowed.

Objectives: To learn and practice Verilog based circuit modeling and validation by simulation.

Problem: Implement an ALU (Arithmetic Logic Unit) satisfying the following functional requirements. You should complete schematic capture tutorial, before you start on this lab. **You should complete tutorial 2 before starting this lab.**

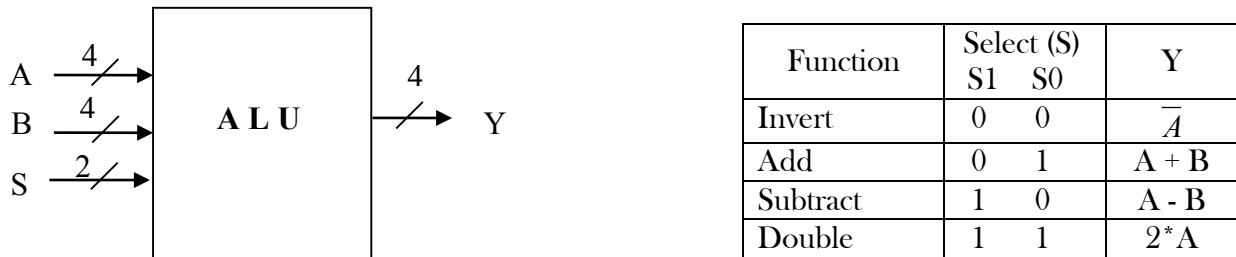


Figure 1: ALU Port Interface and Function Table

- (10 pts.) **Behavioral Verilog:** Design an ALU in behavioral Verilog with port interface and functionality as shown in Figure 1. Test the ALU functionality by simulation. Include at least two vectors per function.
- (20 pts.) **Structural Verilog:** Design the ALU in structural Verilog. Only use the following components: NOT, Full Adder, and 2-to-1 Mux. First you need to develop behavioral Verilog module for each of the above components. Then, you can instantiate these components to build the ALU. Test the ALU functionality by simulation. Include at least two vectors per function. You may re-use the test bench you have created in Lab 1.

Deliverables: (1) a concise PDF report that includes your Verilog code and simulation results; (2) A zipped file of your design files (Verilog models and test benches). Include a README file. Organize your files in folders named Problem1 and Problem2.

Report Organization (A template is provided on Canvas):

- ☐ Cover sheet
- ☐ Problem 1: Behavioral Verilog Code, Test Bench, and Simulation Results (Waveforms)
- ☐ Problem 2: Behavioral Verilog for Components, ALU Structural Code, Test Bench, and Simulation Results (Waveforms)

Important:

- ☐ Do not discard your designs. They may be used as starting point for subsequent labs.
- ☐ You need to submit your report on Canvas in PDF format. No hardcopy is needed.
- ☐ You need to upload the zipped file of your project folder.