(1)

(a)

D_1	D_2	D_3	Q_1	Q_2	Q_3	Y
0	0	0	0	0	1	0
0	0	1	0	1	1	0
0	1	0	X	X	X	X
0	1	1	1	0	1	0
1	0	0	X	X	X	X
1	0	1	1	1	0	0
1	1	0	1	1	1	1
1	1	1	0	0	0	0

$$Q_1 = (D_1 + D_2)(D_1' + D_2' + D_3')$$

$$Q_2 = (D_1 + D_3)(D_2' + D_3')$$

$$Q_3 = D_3' + D_1'$$

$$Y = D_1 D_2 D_3$$

(b)

Q_1

D_3 \ D_1D_2	00	01	11	10
0	0	X	1	X
1	0	1	0	1

Q_2

D_3 \ D_1D_2	00	01	11	10
0	0	X	1	X
1	1	0	0	1

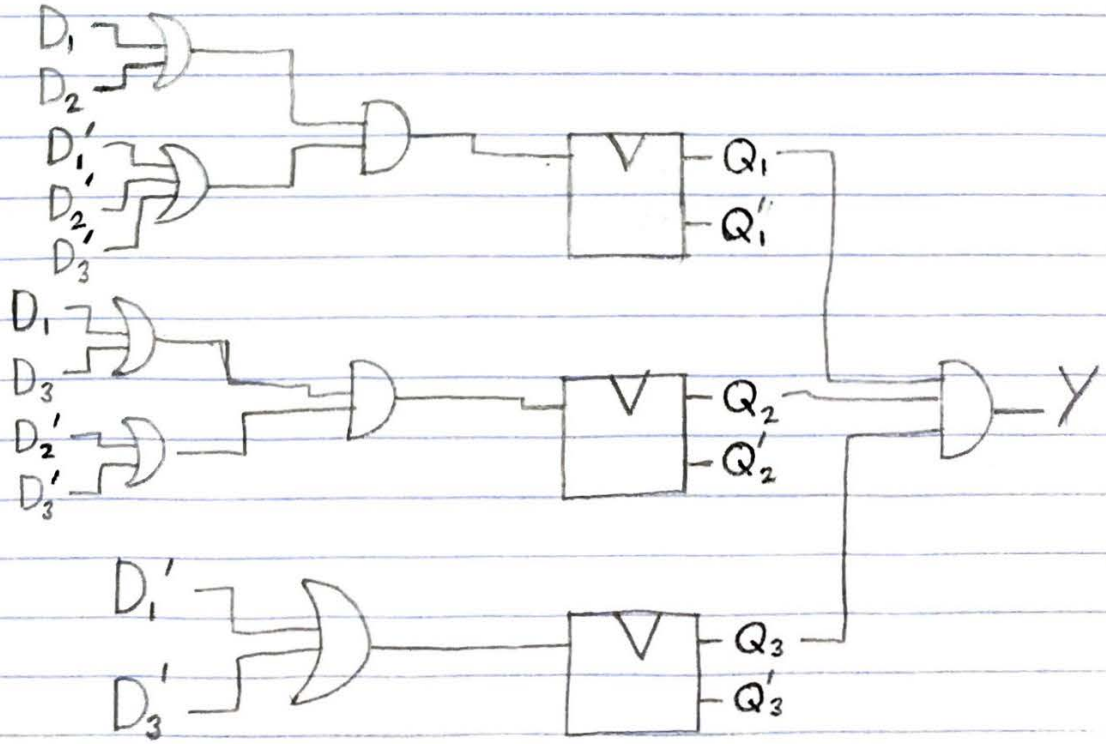
Q_3

D_3 \ D_1D_2	00	01	11	10
0	1	X	1	X
1	1	1	0	0

Y

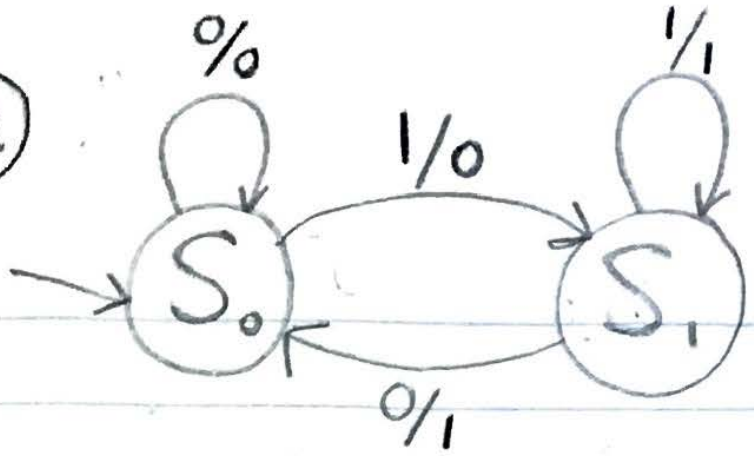
D_3 \ D_1D_2	00	01	11	10
0	0	X	0	X
1	0	0	1	0

(c)



(2)

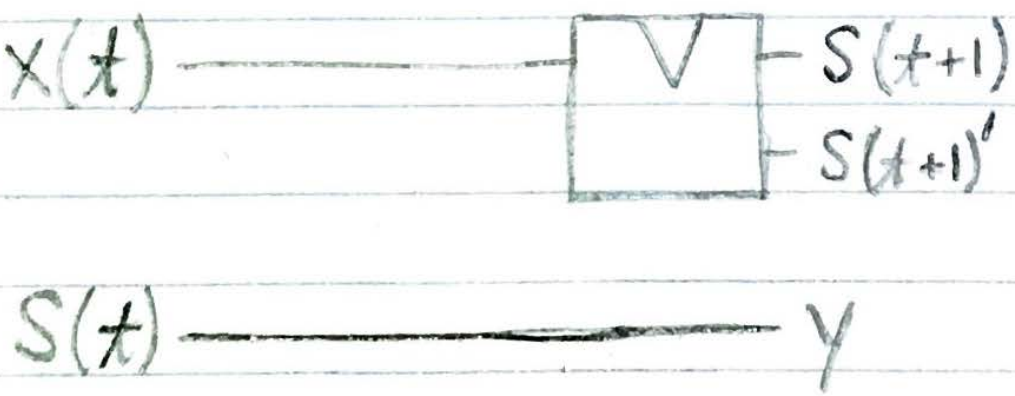
(a)



(b)

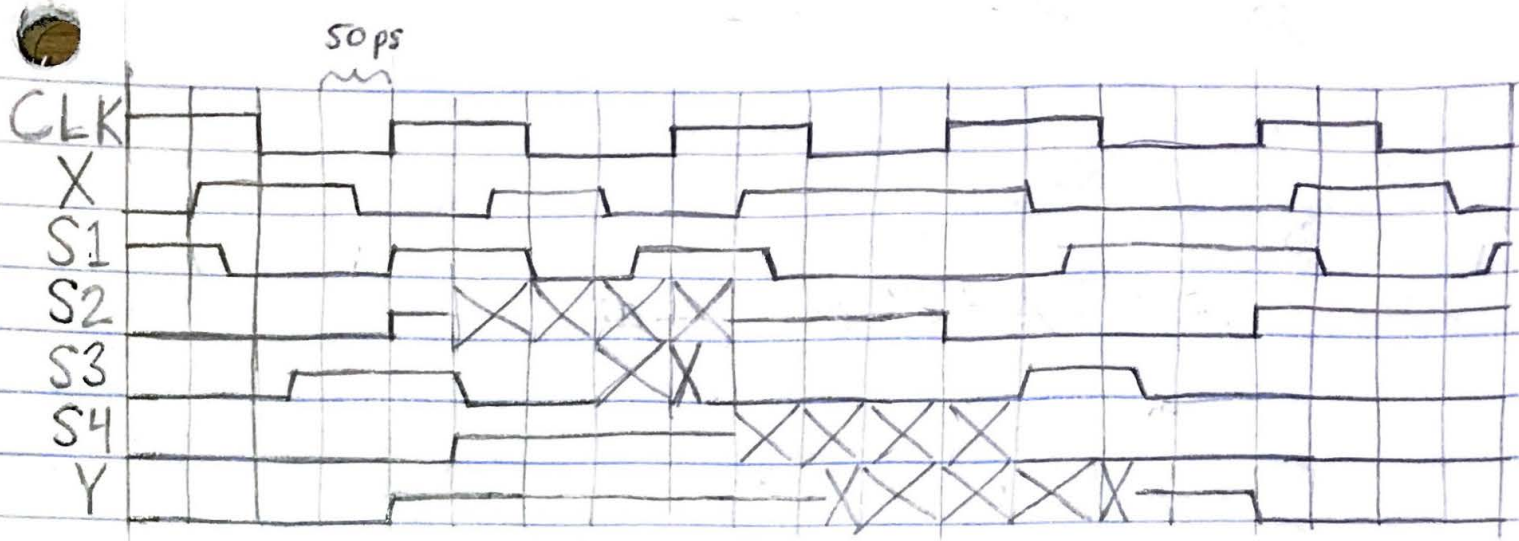
$S(t)$	$x(t)$	$S(t+1)$	$y(t+1)$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

(c)



(3)

(a) 5 GHz → T_c = 200 ps



(b)

There is a setup violation during the first rising edge of the clock because the input to the first flip-flop changes during the 10 ps prior to the rising edge.

There is also a setup violation during the second rising edge of the clock because S3 is not stable during the 10 ps prior to the rising edge of the second flip flop.

(c)

There are no hold time violations because, at all times, $t_{hold} < t_{ccq} + t_{cd}$ since t_{hold} is constantly 10 ps and t_{ccq} is constantly 50 ps.

(4)

(a)

Q1 → Q2

50 ps + 15 ps + 20 ps = 85 ps

50 ps + 10 ps + 20 ps = 80 ps

Q1 → Q3

50 ps + 15 ps + 25 ps + 20 ps = 110 ps

50 ps + 10 ps + 10 ps + 20 ps = 90 ps

Q2 → Q3

50 ps + 25 ps + 20 ps = 95 ps

50 ps + 10 ps + 20 ps = 80 ps

X → Q1

10 ps + 20 ps = 30 ps

10 ps + 20 ps = 30 ps

Q3 → Z

50 ps + 25 ps = 75 ps

50 ps + 10 ps = 60 ps

X → Q2

10 ps + 15 ps + 20 ps = 45 ps

10 ps + 10 ps + 20 ps = 40 ps

X → Q3

10 ps + 15 ps + 25 ps + 20 ps = 70 ps

10 ps + 10 ps + 10 ps + 20 ps = 50 ps

Q1 → Z

50 ps + 15 ps + 25 ps = 90 ps

50 ps + 10 ps + 10 ps = 70 ps

X → Z

10 ps + 15 ps + 25 ps = 50 ps

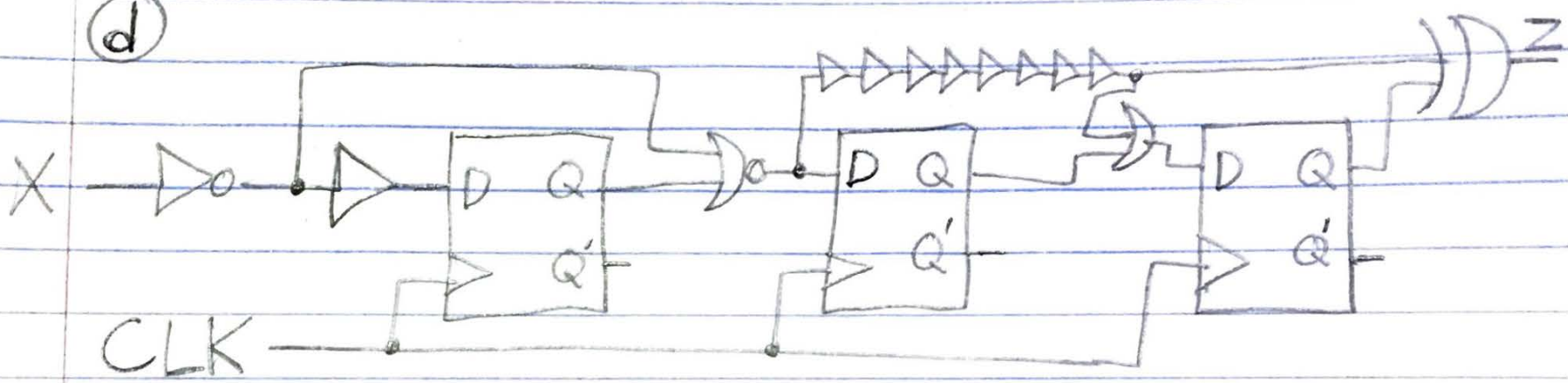
10 ps + 10 ps + 10 ps = 30 ps

(4)

(b) 110 ps

(c) DFF-1 and DFF-3

(d)



(e)

$50_{ps} + 15_{ps} + (20_{ps} * 8) + 25_{ps} + 20_{ps} = 270\,ps$

clock→Q NOR buffers OR setup

270 ps