1. Description

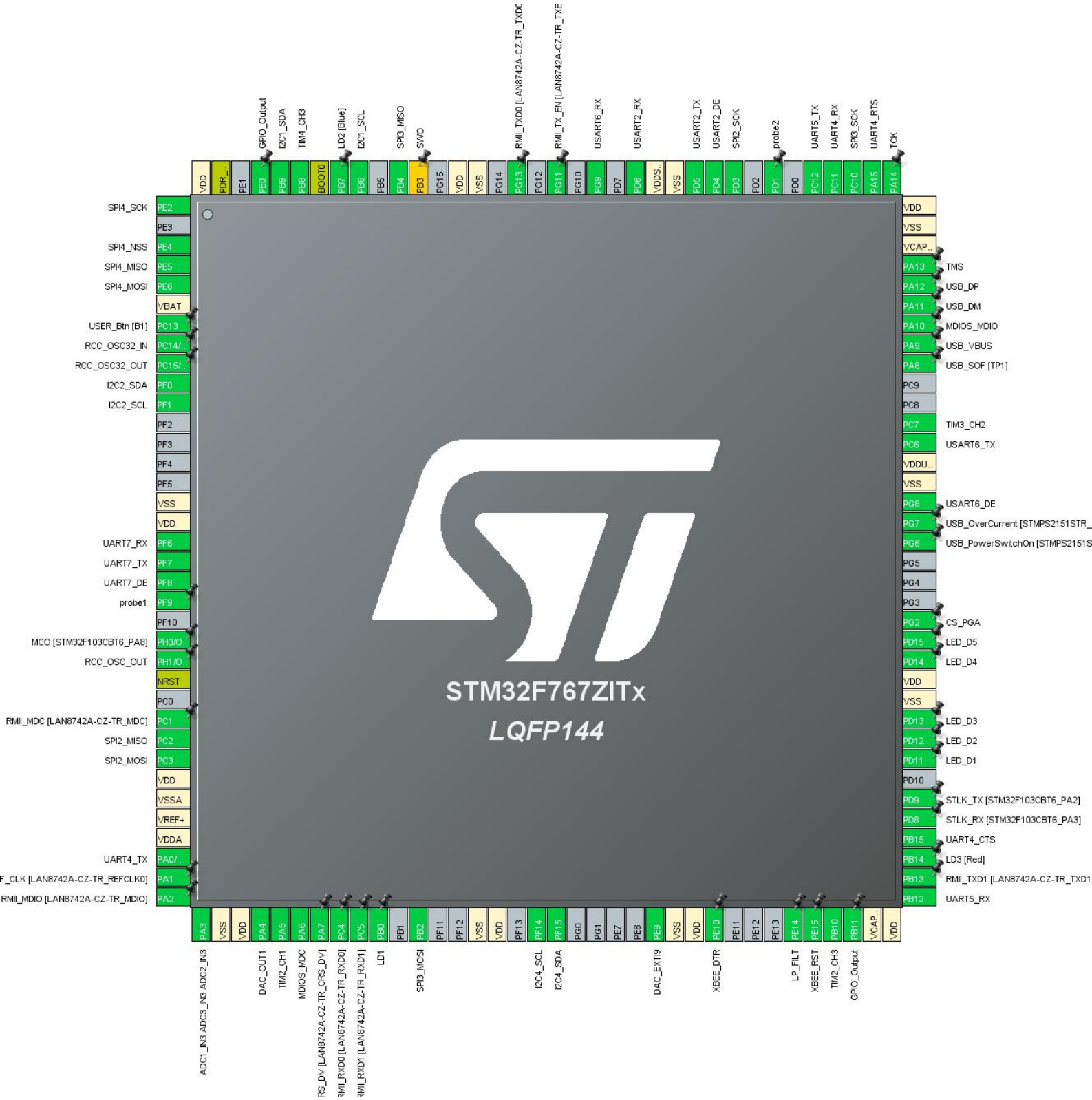
1.1. Project

Project Name	my10
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 5.2.1
Date	06/26/2019

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	
3	PE4	I/O	SPI4_NSS	
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	UART7_RX	
19	PF7	I/O	UART7_TX	
20	PF8	I/O	UART7_DE	
21	PF9 *	I/O	GPIO_Output	probe1
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ-TR_MDC]
28	PC2	I/O	SPI2_MISO	
29	PC3	I/O	SPI2_MOSI	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	UART4_TX	
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
36	PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
37	PA3	I/O	ADC1_IN3, ADC3_IN3, ADC2_IN3	
38	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	VDD	Power		
40	PA4	I/O	DAC_OUT1	
41	PA5	I/O	TIM2_CH1	
42	PA6	I/O	MDIOS_MDC	
43	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
44	PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
45	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
46	PB0 *	I/O	GPIO_Output	LD1
48	PB2	I/O	SPI3_MOSI	
51	VSS	Power		
52	VDD	Power		
54	PF14	I/O	I2C4_SCL	
55	PF15	I/O	I2C4_SDA	
60	PE9	I/O	DAC_EXTI9	
61	VSS	Power		
62	VDD	Power		
63	PE10 *	I/O	GPIO_Output	XBEE_DTR
67	PE14 *	I/O	GPIO_Output	LP_FILT
68	PE15 *	I/O	GPIO_Output	XBEE_RST
69	PB10	I/O	TIM2_CH3	
70	PB11 *	I/O	GPIO_Output	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	UART5_RX	
74	PB13	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
76	PB15	I/O	UART4_CTS	
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
80	PD11 *	I/O	GPIO_Output	LED_D1
81	PD12 *	I/O	GPIO_Output	LED_D2
82	PD13 *	I/O	GPIO_Output	LED_D3
83	VSS	Power		
84	VDD	Power		

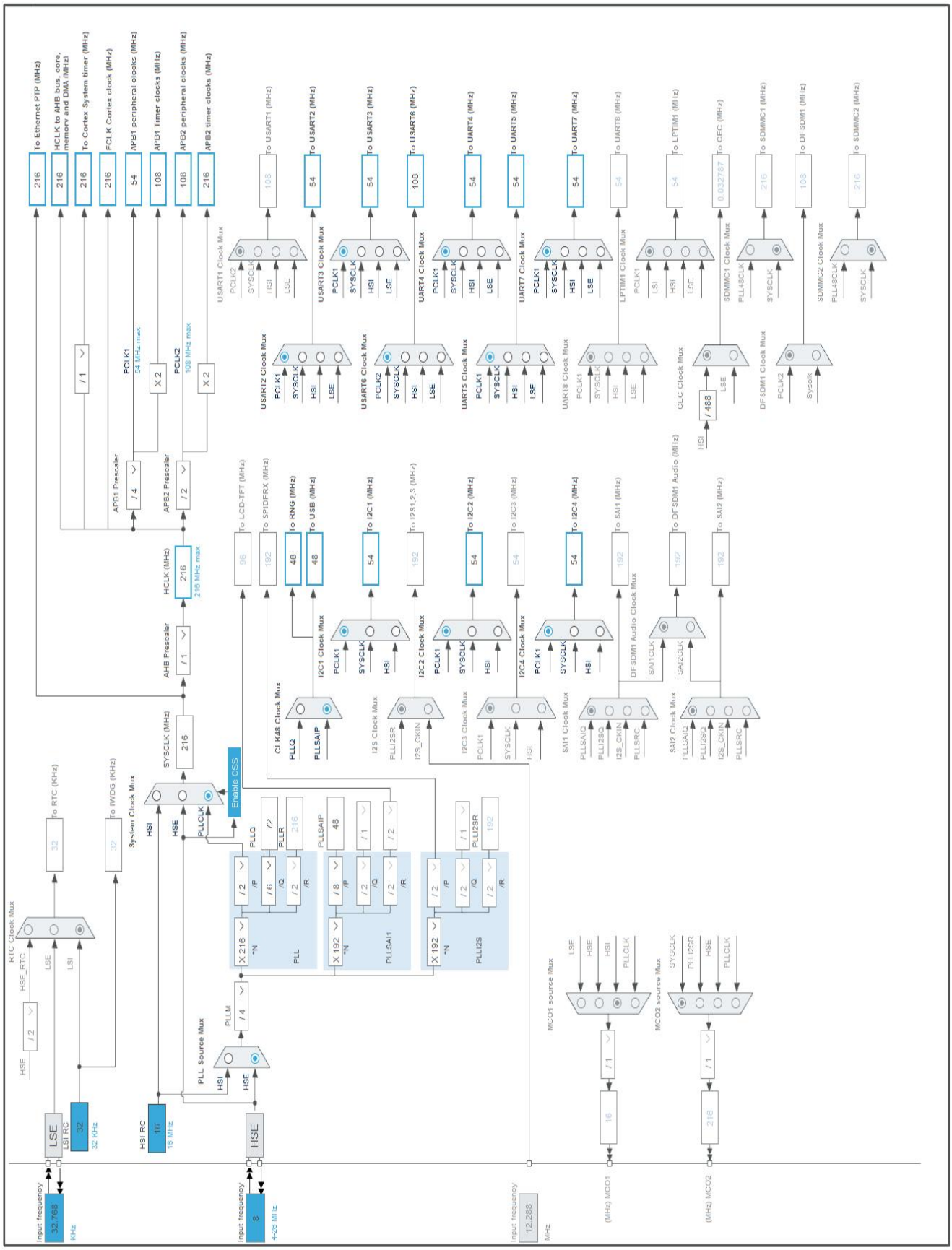
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
85	PD14 *	I/O	GPIO_Output	LED_D4
86	PD15 *	I/O	GPIO_Output	LED_D5
87	PG2 *	I/O	GPIO_Output	CS_PGA
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
93	PG8	I/O	USART6_DE	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	TIM3_CH2	
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10	I/O	MDIOS_MDIO	
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
110	PA15	I/O	UART4_RTS	
111	PC10	I/O	SPI3_SCK	
112	PC11	I/O	UART4_RX	
113	PC12	I/O	UART5_TX	
115	PD1 *	I/O	GPIO_Output	probe2
117	PD3	I/O	SPI2_SCK	
118	PD4	I/O	USART2_DE	
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6	I/O	USART2_RX	
124	PG9	I/O	USART6_RX	
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
128	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
130	VSS	Power		
131	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
133	PB3 **	I/O	SYS_JTDO-SWO	SWO
134	PB4	I/O	SPI3_MISO	
136	PB6	I/O	I2C1_SCL	
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		
139	PB8	I/O	TIM4_CH3	
140	PB9	I/O	I2C1_SDA	
141	PE0 *	I/O	GPIO_Output	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	my10
Project Folder	C:\projects\lightning\my10
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN3

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Triple interleaved mode only ***
DMA Access Mode	DMA access mode 2
Delay between 2 sampling phases	5 Cycles

<html><img src='jar:file:/C:/Program%20Files/STMicroelectronics/STM32Cube/STM32CubeMX/STM32CubeMX.exe!/com/st/microxplorer/image/snk/error.png'   ADC_Settings</html>:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**ADC_SCAN_DISABLE ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN3

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Triple interleaved mode only ***
DMA Access Mode	**DMA access mode 2 ***
Delay between 2 sampling phases	5 Cycles

<html><img src='jar:file:/C:/Program%20Files/STMicroelectronics/STM32Cube/STM32CubeMX/STM32CubeMX.exe!/com/st/microxplorer/image/snk/error.png'   ADC_Settings</html>:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**ADC_SCAN_DISABLE ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	1
Rank	1
Channel	Channel 3
Sampling Time	3 Cycles
Rank	1
Channel	Channel 3
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. ADC3

mode: IN3

7.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Triple interleaved mode only ***
DMA Access Mode	**DMA access mode 2 ***
Delay between 2 sampling phases	5 Cycles

<html><img src='jar:file:/C:/Program%20Files/STMicroelectronics/STM32Cube/STM32CubeMX/STM32CubeMX.exe!/com/st/microxplorer/image/snk/error.png'   ADC_Settings</html>:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**ADC_SCAN_DISABLE ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	1
Rank	1
Channel	Channel 3
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.4. CORTEX_M7

7.4.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCLERATOR	Disabled
Instruction Prefetch	**Enabled ***
CPU ICache	**Enabled ***
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.5. CRC

mode: Activated

7.5.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.6. DAC

mode: OUT1 Configuration

mode: External Trigger

7.6.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 7 Trigger Out event ***
Wave generation mode	Disabled

7.7. ETH

Mode: RMII

7.7.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	**00:80:E1:00:AA:02 ***
PHY Address	**0 ***

Ethernet Basic Configuration:

Rx Mode	Interrupt Mode
TX IP Header Checksum Computation	By hardware

7.7.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	0
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Interrupt Source Flag register Offset	**0x001D ***
PHY Link down inturrupt	**0x000B ***

7.8. GFXSIMULATOR

7.8.1. Simulator Graphic:

7.9. I2C1

I2C: I2C

7.9.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.10. I2C2

I2C: I2C

7.10.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.11. I2C4

I2C: I2C

7.11.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.12. MDIOS

mode: Activate

7.12.1. Parameter Settings:

Basic Parameters:

Port Address	0
Preamble Check State	Enable

7.13. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.13.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3

Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.14. RNG

mode: Activated

7.15. SPI2

Mode: Full-Duplex Master

7.15.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**27.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.16. SPI3

Mode: Full-Duplex Slave

7.16.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.17. SPI4

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.17.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**54.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware

7.18. SYS

Debug: Serial Wire

Timebase Source: TIM12

7.19. TIM1

Clock Source : Internal Clock

7.19.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

7.20. TIM2

Slave Mode: Reset Mode
Trigger Source: TI1FP1
Clock Source : Internal Clock
Channel1: Input Capture direct mode
Channel2: Input Capture indirect mode
Channel3: Input Capture direct mode

7.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**4000000000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Indirect
Prescaler Division Ratio	No division

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.21. TIM3

Clock Source : Internal Clock

Channel2: PWM Generation CH2

7.21.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**10800 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**10 ***
Fast Mode	Disable
CH Polarity	High

7.22. TIM4

Channel3: PWM Generation CH3

7.22.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.23. TIM6

mode: Activated

7.23.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**10800 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Enable (CNT_EN) ***

7.24. TIM7

mode: Activated

7.24.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1100 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

7.25. UART4

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.25.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.26. UART5

Mode: Asynchronous

7.26.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.27. UART7

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.27.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.28. USART2

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.28.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.29. USART3

Mode: Multiprocessor Communication

7.29.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Wake-Up Method	Idle Line

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.30. USART6

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.30.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***

MSB First	Disable

7.31. USB_OTG_FS

Mode: Device_Only

mode: Activate_SOF

mode: Activate_VBUS

7.31.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

7.32. FATFS

mode: User-defined

7.32.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8

FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

7.33. FREERTOS

Interface: CMSIS_V1

7.33.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	**0x100 ***
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled

USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**131072 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	**Enabled ***
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	**Option1 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	512

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.33.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled

vTaskDelete	Enabled
vTaskCleanUpResources	**Enabled ***
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	**Enabled ***
xSemaphoreGetMutexHolder	**Enabled ***
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	**Enabled ***
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

7.34. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.34.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.0.3

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	Enabled

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled

MBEDTLS Dependency:

WITH_MBEDTLS (Use MBEDTLS ** CubeMX specific **)	Enabled

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Enabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled

MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.34.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	**12000 ***
MEMP_OVERFLOW_CHECK (Memory Pool Overflow Protection)	**2 ***
MEMP_SANITY_CHECK (Memory Pool Sanity Check)	**Enabled ***

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	**16 ***
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	**32 ***
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled
ARP_TABLE_SIZE (Number of Active MAC-IP Address Pairs Cached)	**32 ***
ARP_QUEUEING (Multiple Outgoing Queued Packets)	**Enabled ***
ARP_QUEUE_LEN (Max ARP Queue Length)	**32 ***

Callback - Raw Options:

LWIP_RAW (Use Raw LwIP API)	**Enabled ***

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	

	Enabled *
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	**Enabled ***

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	3
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0
RECV_BUFSIZE_DEFAULT (SO_RCVBUF Size Value)	**20000 ***

7.34.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.34.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.34.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	**Enabled ***
LWIP_HTTPD_CGI_SSI (HTTP CGI New Style)	**Enabled ***
LWIP_HTTPD_SSI (HTTP Server Side Includes)	**Enabled ***

LWIP_HTTPD_SSI_RAW (HTTP SSI Tag Handler Callback)	**Enabled ***
LWIP_HTTPD_SUPPORT_POST (HTTP POST)	**Enabled ***
LWIP_HTTPD_SUPPORT_EXTSTATUS (Error Pages Display)	**Enabled ***
LWIP_HTTPD_SUPPORT_11_KEEPALIVE (HTTP 1.1 Persistent Connections)	**Enabled ***
LWIP_HTTPD_ABORT_ON_CLOSE_MEM_ERROR (Call TCP Abort on TCP Close with Memory Error)	**Enabled ***

7.34.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.34.7. SNTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

7.34.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.34.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.34.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.34.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	**Enabled ***
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.34.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

7.35. MBEDTLS

mode: Enabled

7.35.1. Version and modes:

Version:

MBEDTLS version	2.11.0

TCP/IP stack:

TCP/IP stack	LWIP

RNG dependency:

RNG IP	HW RNG

Modes:

MBEDTLS_SSL_CLI_C	Defined
MBEDTLS_SSL_SRV_C	Defined

7.35.2. Feature support:

System support:

MBEDTLS_HAVE_ASM	Defined
MBEDTLS_NO_UDBL_DIVISION	Defined
MBEDTLS_HAVE_TIME	Defined
MBEDTLS_HAVE_TIME_DATE	Defined

General:

MBEDTLS_ECP_NIST_OPTIM	Defined
MBEDTLS_ECDSA_DETERMINISTIC	Defined
MBEDTLS_PK_PARSE_EC_EXTENDED	Defined
MBEDTLS_ERROR_STRERROR_DUMMY	Defined
MBEDTLS_GENPRIME	Defined
MBEDTLS_NO_PLATFORM_ENTROPY	Defined
MBEDTLS_PK_RSA_ALT_SUPPORT	Defined
MBEDTLS_PKCS1_V15	Defined
MBEDTLS_PKCS1_V21	Defined
MBEDTLS_SELF_TEST	Defined
MBEDTLS_VERSION_FEATURES	Defined

Ciphering:

MBEDTLS_CIPHER_MODE_CBC	Defined
MBEDTLS_CIPHER_MODE_CFB	Defined
MBEDTLS_CIPHER_MODE_CTR	Defined
MBEDTLS_CIPHER_MODE_OFB	Defined
MBEDTLS_CIPHER_MODE_XTS	Defined
MBEDTLS_CIPHER_PADDING_PKCS7	Defined
MBEDTLS_CIPHER_PADDING_ONE_AND_ZEROS	Defined
MBEDTLS_CIPHER_PADDING_ZEROS_AND_LEN	Defined
MBEDTLS_CIPHER_PADDING_ZEROS	Defined
MBEDTLS_REMOVE_ARC4_CIPHERSUITES	Defined

Elliptic curves:

MBEDTLS_ECP_DP_SECP192R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP224R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP256R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP384R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP521R1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP192K1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP224K1_ENABLED	Defined
MBEDTLS_ECP_DP_SECP256K1_ENABLED	Defined
MBEDTLS_ECP_DP_BP256R1_ENABLED	Defined
MBEDTLS_ECP_DP_BP384R1_ENABLED	Defined
MBEDTLS_ECP_DP_BP512R1_ENABLED	Defined
MBEDTLS_ECP_DP_CURVE25519_ENABLED	Defined

MBEDTLS_ECP_DP_CURVE448_ENABLED	Defined

Key exchange:

MBEDTLS_KEY_EXCHANGE_PSK_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_DHE_PSK_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_ECDHE_PSK_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_RSA_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_DHE_RSA_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_ECDHE_RSA_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_ECDH_ECDSA_ENABLED	Defined
MBEDTLS_KEY_EXCHANGE_ECDH_RSA_ENABLED	Defined

SSL:

MBEDTLS_SSL_ALL_ALERT_MESSAGES	Defined
MBEDTLS_SSL_ENCRYPT_THEN_MAC	Defined
MBEDTLS_SSL_EXTENDED_MASTER_SECRET	Defined
MBEDTLS_SSL_FALLBACK_SCSV	Defined
MBEDTLS_SSL_CBC_RECORD_SPLITTING	Defined
MBEDTLS_SSL_RENEGOTIATION	Defined
MBEDTLS_SSL_PROTO_TLS1	Defined
MBEDTLS_SSL_PROTO_TLS1_1	Defined
MBEDTLS_SSL_PROTO_DTLS	Defined
MBEDTLS_SSL_ALPN	Defined
MBEDTLS_SSL_DTLS_ANTI_REPLAY	Defined
MBEDTLS_SSL_DTLS_HELLO_VERIFY	Defined
MBEDTLS_SSL_DTLS_CLIENT_PORT_REUSE	Defined
MBEDTLS_SSL_DTLS_BADMAC_LIMIT	Defined
MBEDTLS_SSL_SESSION_TICKETS	Defined
MBEDTLS_SSL_EXPORT_KEYS	Defined
MBEDTLS_SSL_SERVER_NAME_INDICATION	Defined
MBEDTLS_SSL_TRUNCATED_HMAC	Defined

X509:

MBEDTLS_X509_CHECK_KEY_USAGE	Defined
MBEDTLS_X509_CHECK_EXTENDED_KEY_USAGE	Defined
MBEDTLS_X509_RSASSA_PSS_SUPPORT	Defined

7.35.3. Alternate implementation:

7.35.4. Modules:

General:

MBEDTLS_AESNI_C	Defined

MBEDTLS_AES_C	Defined
MBEDTLS_ARC4_C	Defined
MBEDTLS_ASN1_PARSE_C	Defined
MBEDTLS_ASN1_WRITE_C	Defined
MBEDTLS_BASE64_C	Defined
MBEDTLS_BIGNUM_C	Defined
MBEDTLS_BLOWFISH_C	Defined
MBEDTLS_CAMELLIA_C	Defined
MBEDTLS_CCM_C	Defined
MBEDTLS_CERTS_C	Defined
MBEDTLS_CIPHER_C	Defined
MBEDTLS_CTR_DRBG_C	Defined
MBEDTLS_DES_C	Defined
MBEDTLS_DHM_C	Defined
MBEDTLS_ECDH_C	Defined
MBEDTLS_ECDSA_C	Defined
MBEDTLS_ECP_C	Defined
MBEDTLS_ENTROPY_C	Defined
MBEDTLS_ERROR_C	Defined
MBEDTLS_GCM_C	Defined
MBEDTLS_HKDF_C	Defined
MBEDTLS_HMAC_DRBG_C	Defined
MBEDTLS_MD_C	Defined
MBEDTLS_MD5_C	Defined
MBEDTLS_NET_C	Defined
MBEDTLS_OID_C	Defined
MBEDTLS_PADLOCK_C	Defined
MBEDTLS_PEM_PARSE_C	Defined
MBEDTLS_PEM_WRITE_C	Defined
MBEDTLS_PK_C	Defined
MBEDTLS_PK_PARSE_C	Defined
MBEDTLS_PK_WRITE_C	Defined
MBEDTLS_PKCS5_C	Defined
MBEDTLS_PKCS12_C	Defined
MBEDTLS_PLATFORM_C	Defined
MBEDTLS_RIPEMD160_C	Defined
MBEDTLS_RSA_C	Defined
MBEDTLS_SHA1_C	Defined
MBEDTLS_SHA256_C	Defined
MBEDTLS_SHA512_C	Defined
MBEDTLS_SSL_CACHE_C	Defined
MBEDTLS_SSL_COOKIE_C	Defined
MBEDTLS_SSL_TICKET_C	Defined

MBEDTLS_SSL_TLS_C	Defined
MBEDTLS_VERSION_C	Defined
MBEDTLS_X509_USE_C	Defined
MBEDTLS_X509_CRT_PARSE_C	Defined
MBEDTLS_X509_CRL_PARSE_C	Defined
MBEDTLS_X509_CSR_PARSE_C	Defined
MBEDTLS_X509_CREATE_C	Defined
MBEDTLS_X509_CRT_WRITE_C	Defined
MBEDTLS_X509_CSR_WRITE_C	Defined
MBEDTLS_XTEA_C	Defined

7.35.5. Modules Configuration:

7.36. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.36.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

7.36.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336

PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA3	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PA3	ADC3_IN3	Analog mode	No pull-up and no pull-down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PE9	DAC_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C4	PF14	I2C4_SCL	Alternate Function Open	Pull-up		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			Drain		**Very High ***	
	PF15	I2C4_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
MDIOS	PA6	MDIOS_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA10	MDIOS_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI3	PB2	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE4	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-	n/a	n/a	n/a	TCK

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		SWCLK				
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PA0/WKUP	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	UART4_CTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA15	UART4_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART5	PB12	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART7	PF6	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF8	UART7_DE	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART2	PD4	USART2_DE	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART3	PD8	USART3_TX	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	STLK_TX [STM32F103CBT6_PA2]
USART6	PG8	USART6_DE	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG9	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	USB_VBUS
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PF9	GPIO_Output	Output Push Pull	**Pull-up ***	**High ***	probe1
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	XBEE_DTR
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LP_FILT
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	XBEE_RST
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_D1
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_D2
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_D3
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_D4
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_D5
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_PGA
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PD1	GPIO_Output	Output Push Pull	**Pull-up ***	**High ***	probe2
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
DAC1	DMA1_Stream5	Memory To Peripheral	Low
USART6_RX	DMA2_Stream1	Peripheral To Memory	**Medium ***
ADC1	DMA2_Stream4	Peripheral To Memory	**High ***
TIM2_UP/CH3	DMA1_Stream1	Peripheral To Memory	Low

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	**Three Quarters Full ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	Single

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream4 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	

	Word *
Peripheral Burst Size:	Single
Memory Burst Size:	**4 Increment ***

TIM2_UP/CH3: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Word
Memory Data Width:	Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
RCC global interrupt	true	6	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	6	0
ADC1, ADC2 and ADC3 global interrupts	true	6	0
TIM2 global interrupt	true	6	0
TIM3 global interrupt	true	6	0
USART2 global interrupt	true	6	0
EXTI line[15:10] interrupts	true	6	0
TIM8 break interrupt and TIM12 global interrupt	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	6	0
DMA2 stream1 global interrupt	true	6	0
DMA2 stream4 global interrupt	true	5	0
Ethernet global interrupt	true	6	0
USB On The Go FS global interrupt	true	6	0
USART6 global interrupt	true	6	0
FPU global interrupt	true	6	0
MDIO slave global interrupt	true	6	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI2 global interrupt	unused		
USART3 global interrupt	unused		
SPI3 global interrupt	unused		
UART4 global interrupt	unused		
UART5 global interrupt	unused		
TIM7 global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
HASH and RNG global interrupts	unused		
UART7 global interrupt	unused		
SPI4 global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		

*** User modified value**

9. Software Pack Report