# zasady obsługi układów wejścia/wyjścia

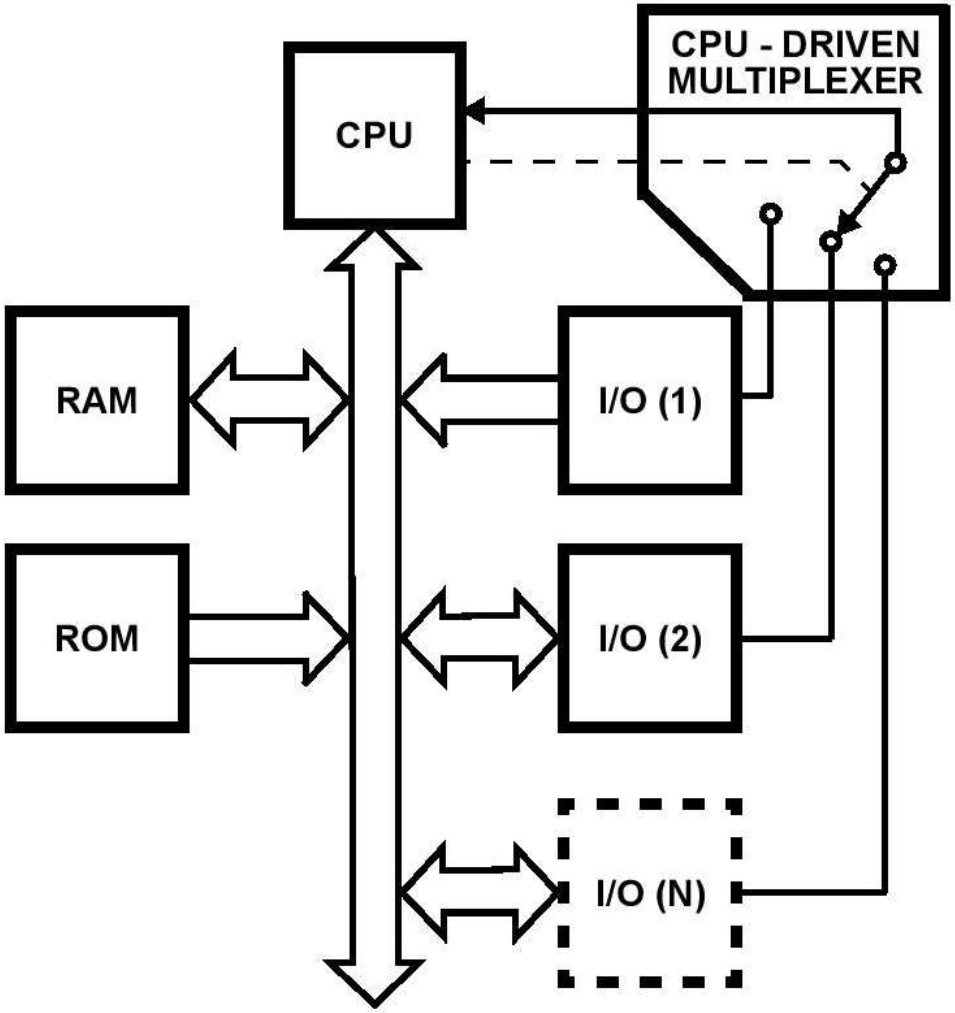



FIGURE 2. POLLED METHOD

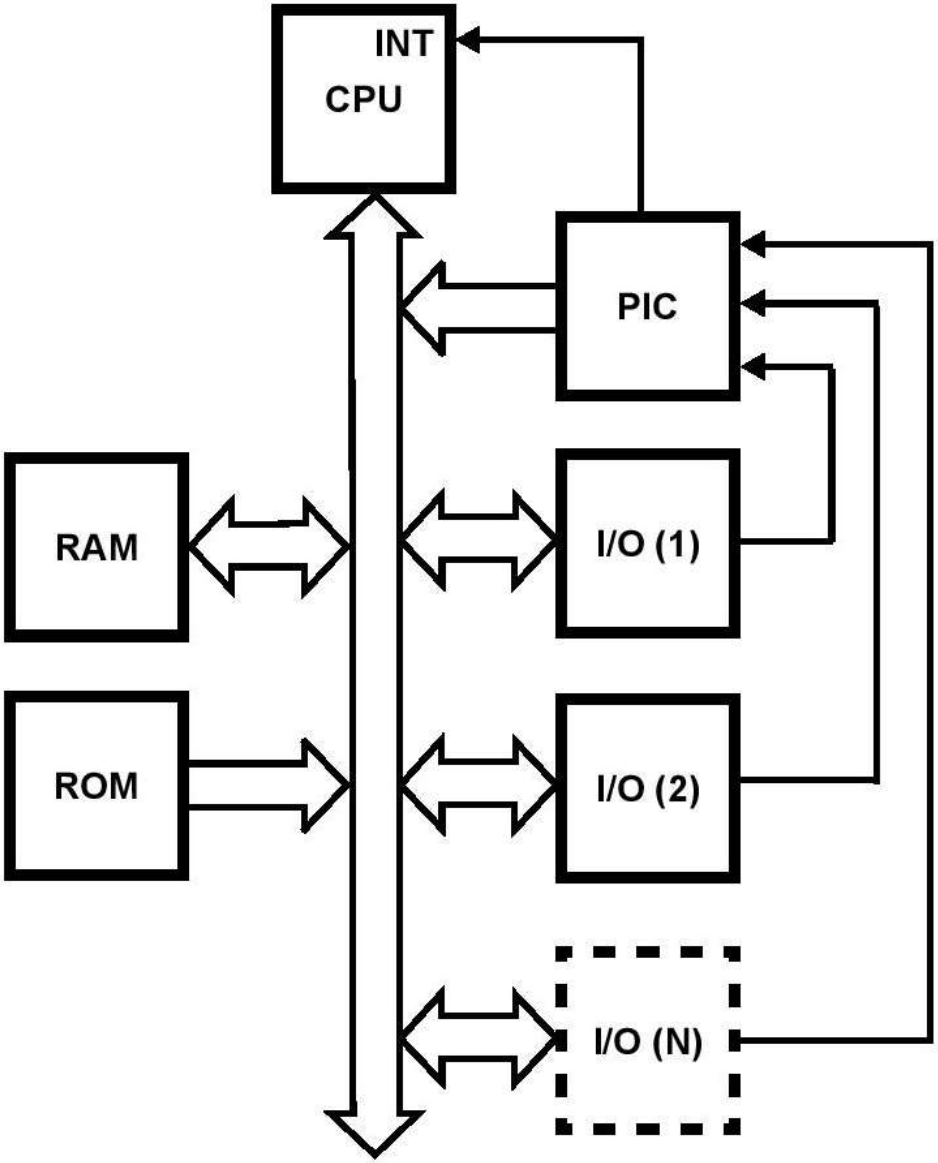



FIGURE 3. INTERRUPT METHOD

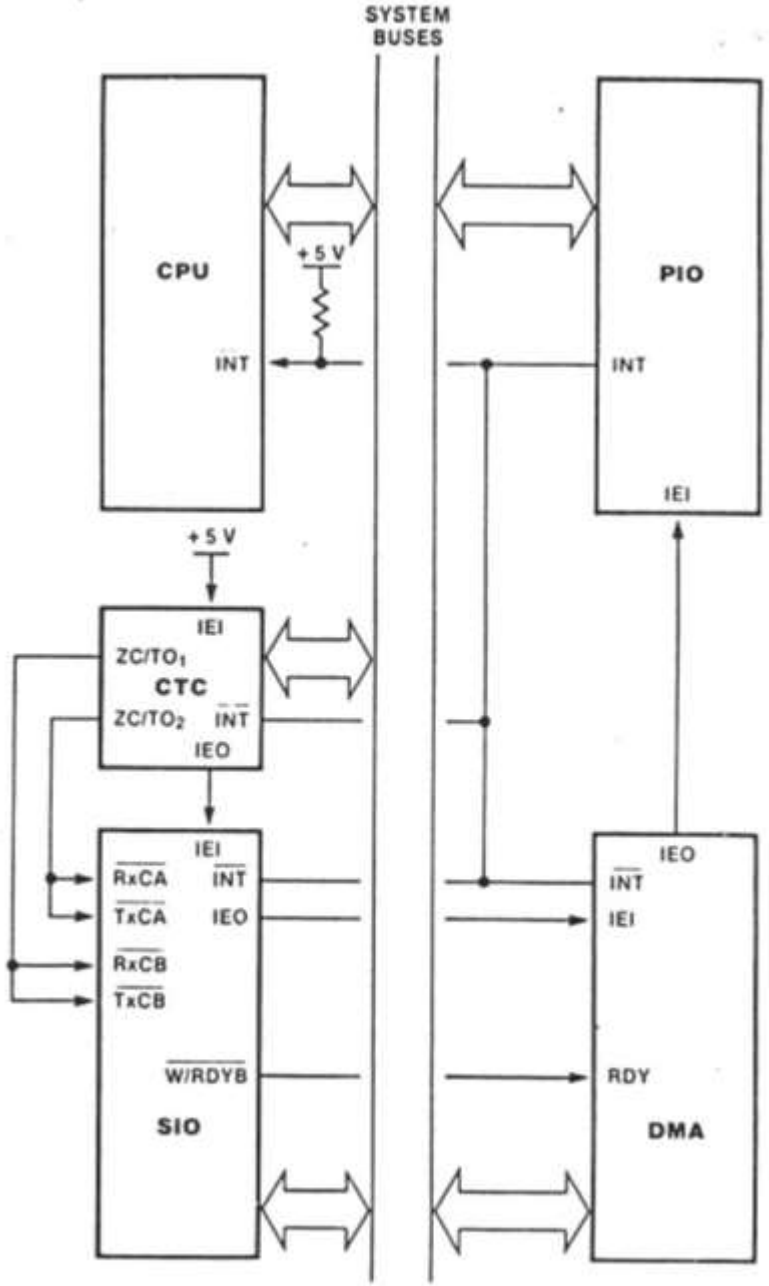



Figure 3. PIO in a Typical Z80 Family Environment

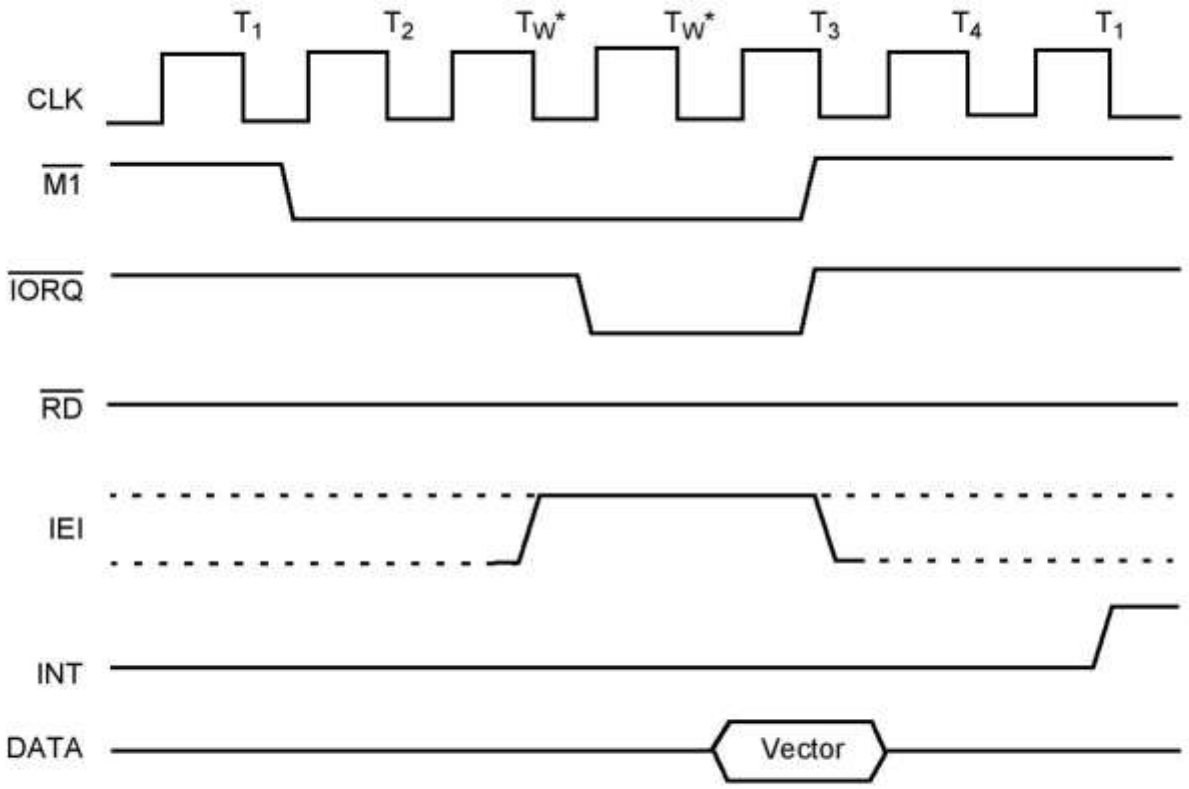
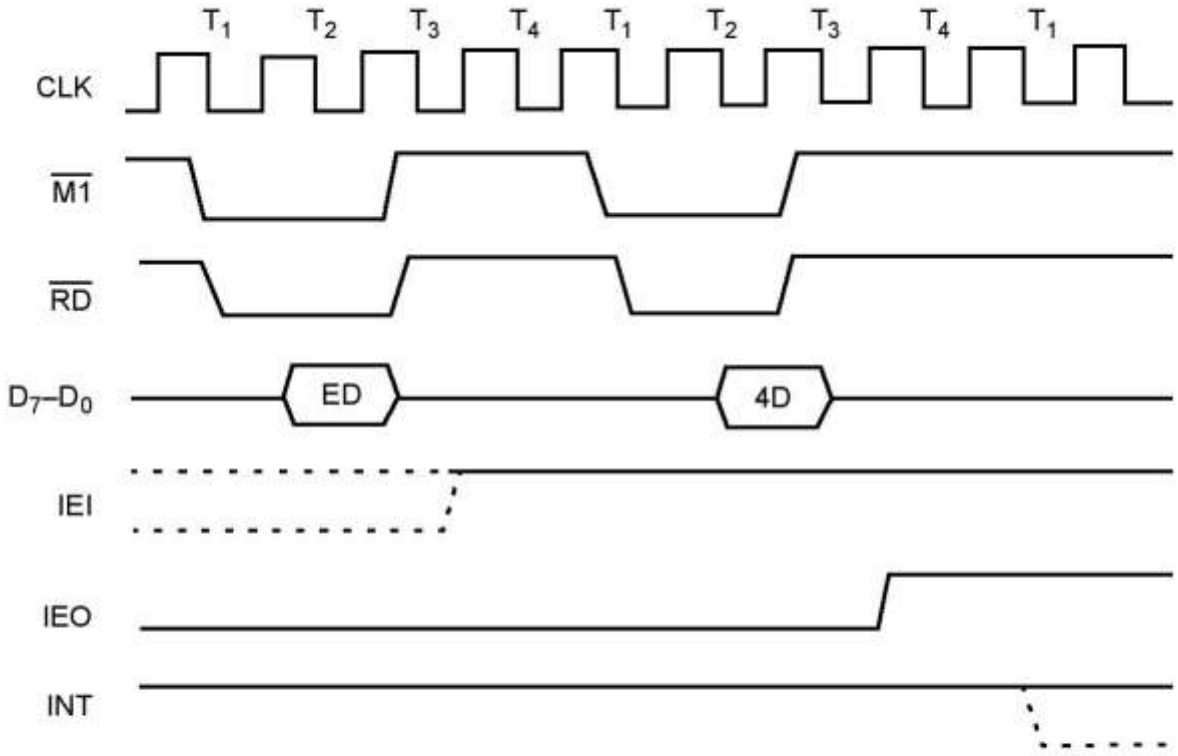



**Figure 12. Interrupt Acknowledge Cycle**




*INT goes Low if more interrupts are pending on the $\overline{\text{RTC}}$.

**Figure 13. Return from Interrupt Cycle**

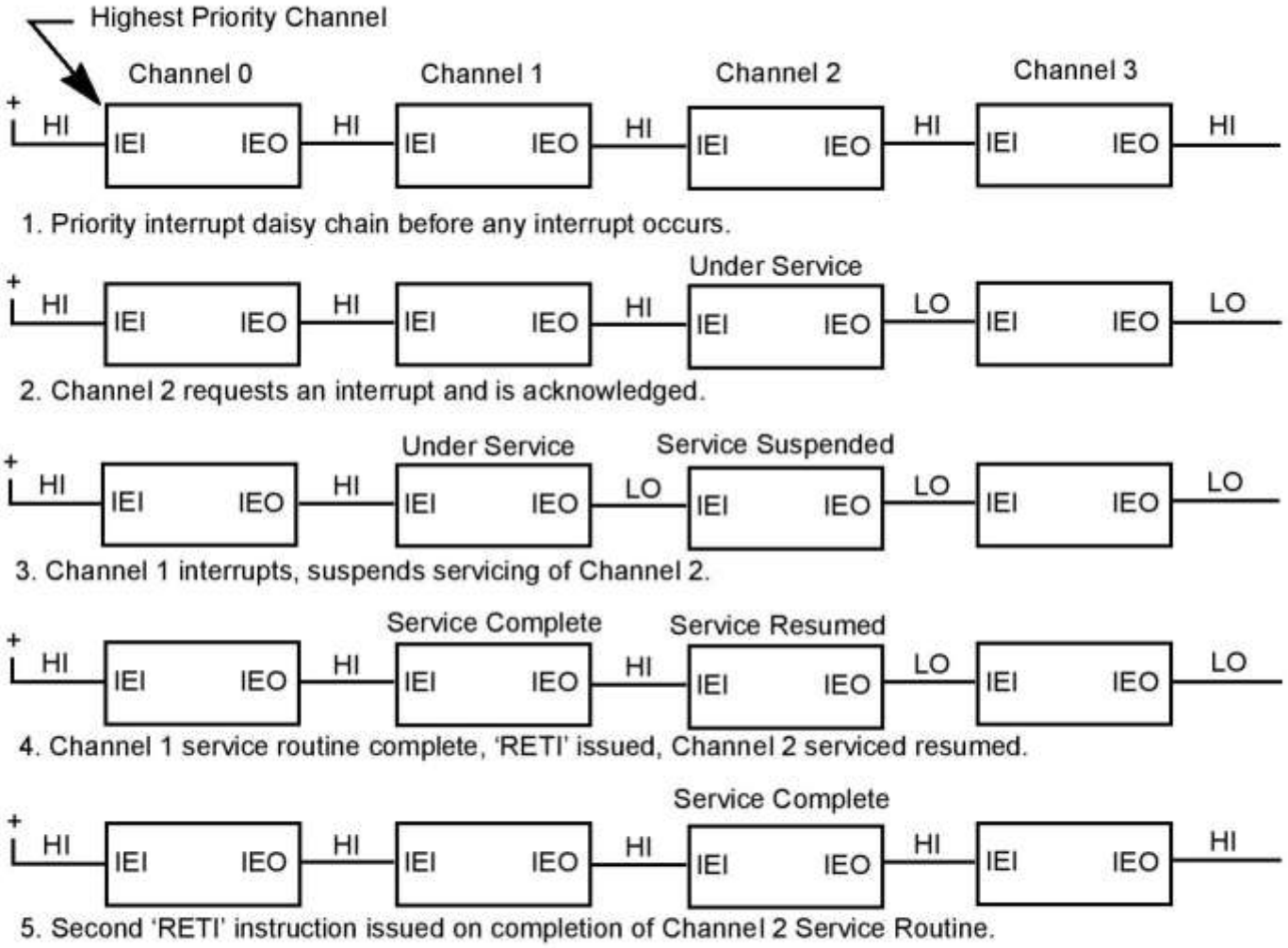



**Figure 14. Daisy-Chain Interrupt Servicing**

| Action | $IFF_1$ | $IFF_2$ | Comments |
|---|---|---|---|
| CPU Reset | 0 | 0 | Maskable interrupt $\overline{INT}$ disabled |
| DI instruction execution | 0 | 0 | Maskable interrupt $\overline{INT}$ disabled |
| EI instruction execution | 1 | 1 | Maskable interrupt $\overline{INT}$ enabled |
| LD A,I instruction execution | • | • | $IFF_2$ → Parity flag |
| LD A,R instruction execution | • | • | $IFF_2$ → Parity flag |
| Accept $\overline{NMI}$ | 0 | $IFF_1$ | $IFF_1$ → $IFF_2$ (Maskable interrupt $\overline{INT}$ disabled) |
| RETN instruction execution | $IFF_2$ | • | $IFF_2$ → $IFF_1$ at completion of an $\overline{NMI}$ service routine. |

**Table 2. State of Flip-Flops**

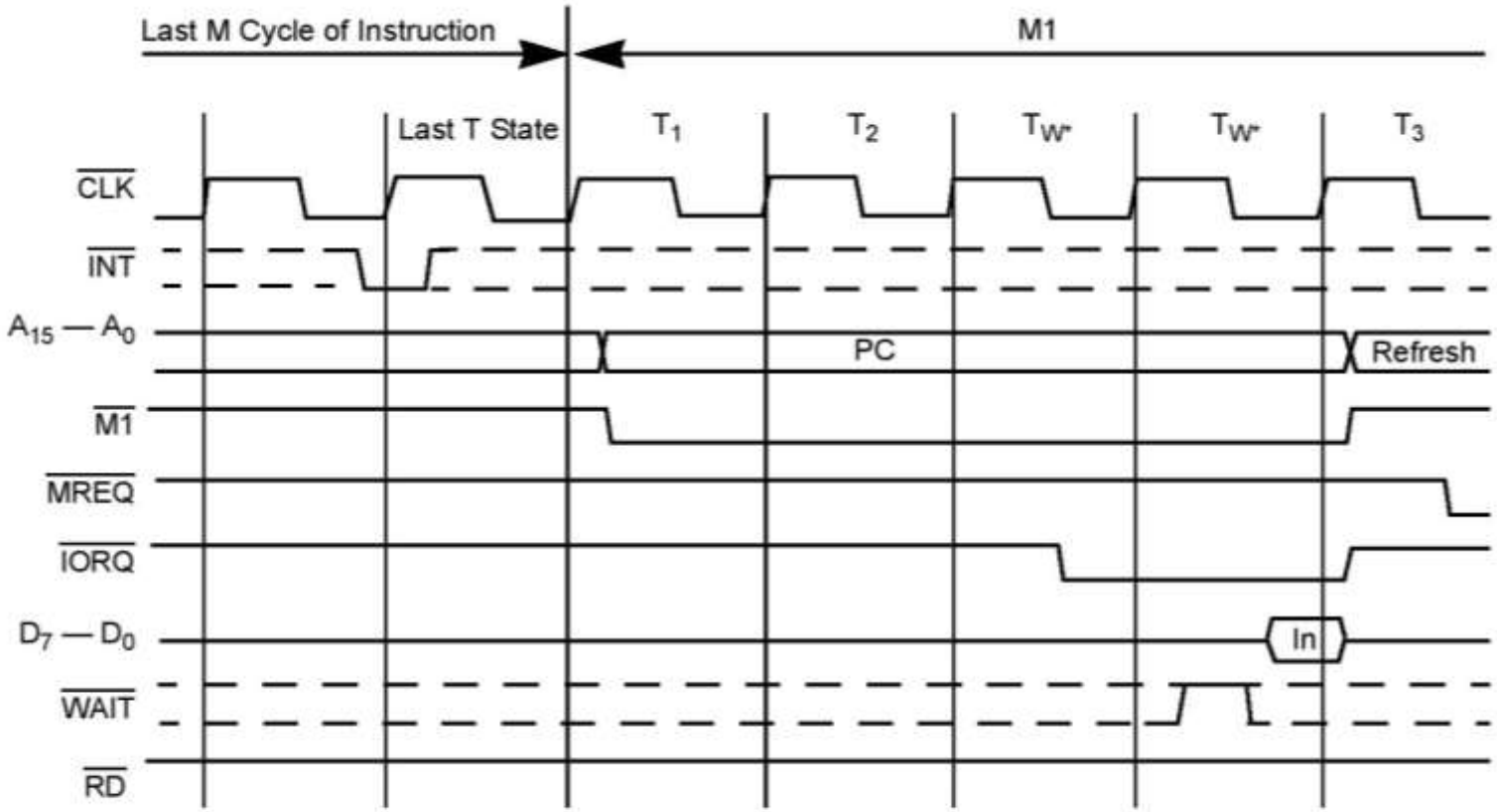



**Figure 9. Interrupt Request/Acknowledge Cycle**

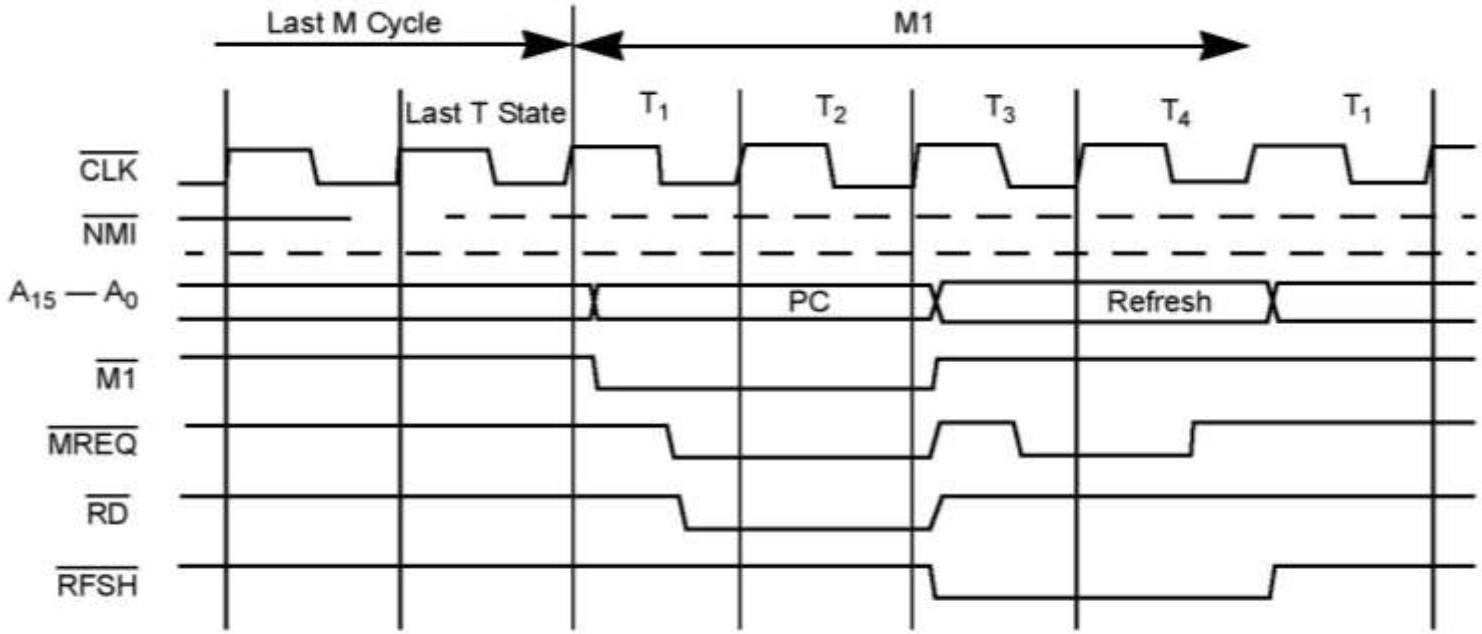



**Figure 10. Non-Maskable Interrupt Request Operation**

Data Sheet | March 17, 2006 | FN2784.5

## CMOS Priority Interrupt Controller

The Intersil 82C59A is a high performance CMOS Priority Interrupt Controller manufactured using an advanced 2µm CMOS process. The 82C59A is designed to relieve the system CPU from the task of polling in a multilevel priority system. The high speed and industry standard configuration of the 82C59A make it compatible with microprocessors such as 80C286, 80286, 80C86/88, 8086/88, 8080/85 and NSC800.

The 82C59A can handle up to eight vectored priority interrupting sources and is cascadable to 64 without additional circuitry. Individual interrupting sources can be masked or prioritized to allow custom system configuration. Two modes of operation make the 82C59A compatible with both 8080/85 and 80C86/88/286 formats.

Static CMOS circuit design ensures low operating power. The Intersil advanced CMOS process results in performance equal to or greater than existing equivalent products at a fraction of the power.

## Features

- Pb-Free Plus Anneal Available (RoHS Compliant)
- 12.5MHz, 8MHz and 5MHz Versions Available
- High Speed, "No Wait-State" Operation with 12.5MHz 80C286 and 8MHz 80C86/88
- Pin Compatible with NMOS 8259A
- 80C86/88/286 and 8080/85/86/88/286 Compatible
- Eight-Level Priority Controller, Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Fully Static Design
- Fully TTL Compatible
- Low Power Operation
  - ICCSB. . . . . 10µA Maximum
  - ICCOP . . . . . 1mA/MHz Maximum
- Single 5V Power Supply
- Commercial, Industrial and Military Operating Temperature Ranges Available

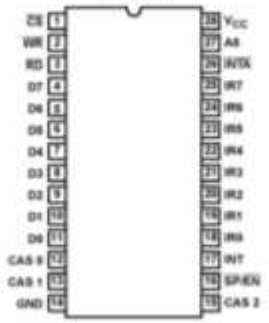




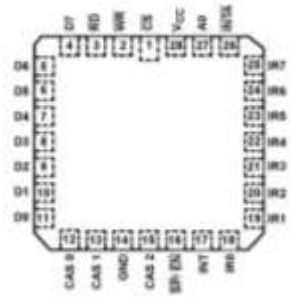


## Pinouts

82C59A (PDIP, CERDIP)
TOP VIEW




82C59A (PLCC, CLCC)
TOP VIEW




| PIN | DESCRIPTION |
|---|---|
| D7 - D0 | Data Bus (Bidirectional) |
| $\overline{RD}$ | Read Input |
| $\overline{WR}$ | Write Input |
| A0 | Command Select Address |
| $\overline{CS}$ | Chip Select |
| CAS 2 - CAS 0 | Cascade Lines |
| SP/$\overline{EN}$ | Slave Program Input Enable |
| INT | Interrupt Output |
| $\overline{INTA}$ | Interrupt Acknowledge Input |
| IR0 - IR7 | Interrupt Request Inputs |

## Functional Diagram

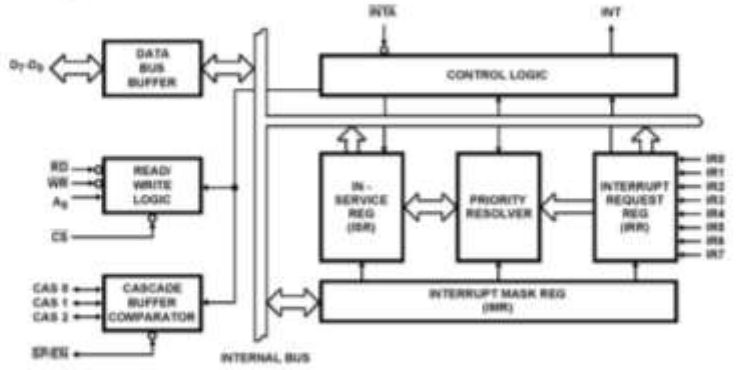



FIGURE 1.

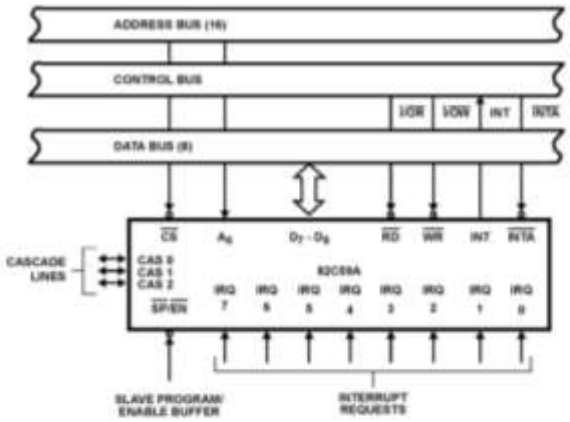



FIGURE 5. 82C59A STANDARD SYSTEM BUS INTERFACE

These events occur in an 8080/8085 system:

1. One or more of the INTERRUPT REQUEST lines (IR0 - IR7) are raised high, setting the corresponding IRR bit(s).
2. The 82C59A evaluates those requests in the priority resolver and sends an interrupt (INT) to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 82C59A will also release a CALL instruction code (11001101) onto the 8-bit data bus through D0 - D7.
5. This CALL instruction will initiate two additional $\overline{\text{INTA}}$ pulses to be sent to 82C59A from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the 82C59A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte CALL instruction released by the 82C59A. In the AEOI mode, the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86/88/286 system are the same until step 4.

4. The 82C59A does not drive the data bus during the first $\overline{\text{INTA}}$ pulse.
5. The 80C86/88/286 CPU will initiate a second $\overline{\text{INTA}}$ pulse. During this $\overline{\text{INTA}}$ pulse, the appropriate ISR bit is set and the corresponding bit in the IRR is reset. The 82C59A outputs the 8-bit pointer onto the data bus to be read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration), the 82C59A will issue an interrupt level 7. If a slave is programmed on IR bit 7, the CAS lines remain inactive and vector addresses are output from the master 82C59A.

## Interrupt Sequence Outputs

### 8080, 8085 Interrupt Response Mode

This sequence is timed by three $\overline{\text{INTA}}$ pulses. During the first $\overline{\text{INTA}}$ pulse, the CALL opcode is enabled onto the data bus.

First Interrupt Vector Byte Data: Hex CD

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Call Code | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |

During the second $\overline{\text{INTA}}$ pulse, the lower address of the appropriate service routine is enabled onto the data bus.





e. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode (see note), no Auto-EOI, 8080/85 system).

NOTE: Master/Slave in ICW4 is only used in the buffered mode.

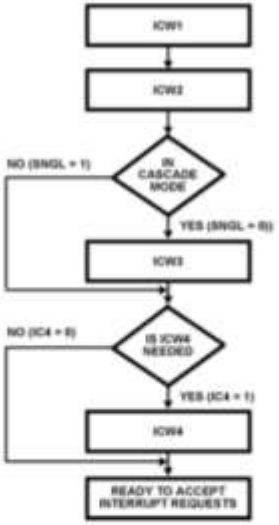



FIGURE 6. 82C59A INITIALIZATION SEQUENCE

### Initialization Command Words 1 and 2 (ICW1, ICW2)

A5 - A15: Page starting address of service routines. In an 8080/85 system the 8 request levels will generate CALLS to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus, the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A0 - A15). When the routine interval is 4, A0 - A4 are automatically inserted by the 82C59A, while A5 - A15 are programmed externally. When the routine interval is 8, A0 - A5 are automatically inserted by the 82C59A while A6 - A15 are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 80C86/88/286 system, A15 - A11 are inserted in the five most significant bits of the vectoring byte and the 82C59A sets the three least significant bits according to the interrupt level. A10 - A5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 82C59A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: ALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 82C59A in the system. If SNGL = 1, no ICW3 will be issued.

IC4: If this bit is set - ICW4 has to be issued. If ICW4 is not needed, set IC4 = 0.

### Initialization Command Word 3 (ICW3)

This word is read only when there is more than one 82C59A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when $\overline{\text{SP}}$ = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the bit corresponding to the appropriate IR line for the slave. The master then will release byte 1 of the call sequence (for 8080/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86/88/286, only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{\text{SP}}$ = 0, or if BUF = 1 and M/S = 0 in ICW4), bits 2 - 0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86/88/286) are released by it on the Data Bus.

NOTE: (The slave address must correspond to the IR line it is connected to in the master ID).

### Initialization Command Word 4 (ICW4)

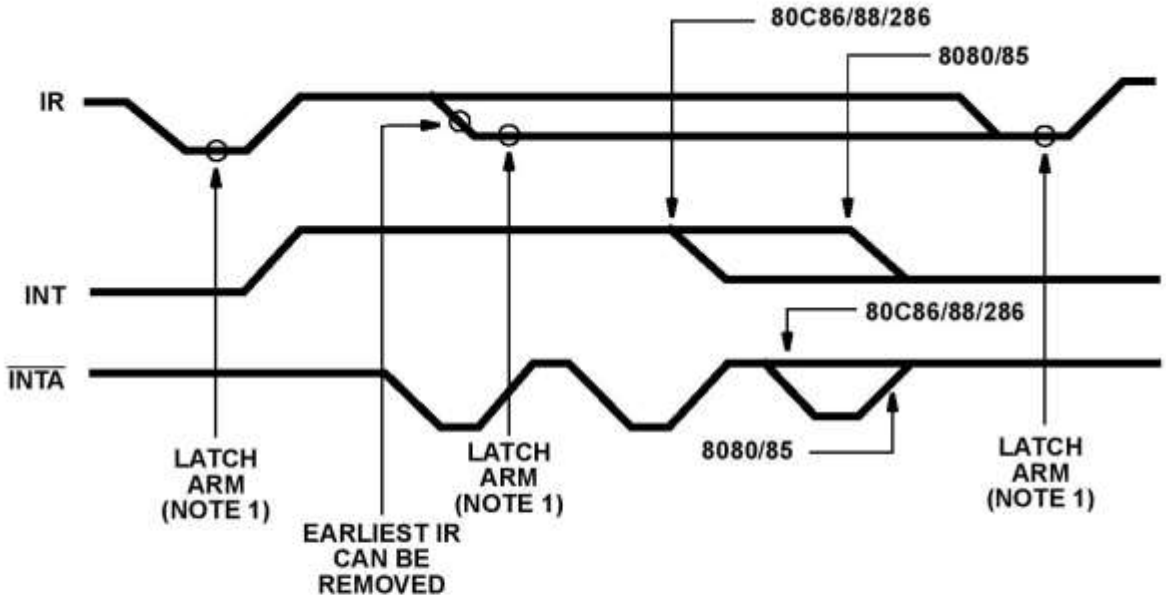
SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, $\overline{\text{SP}}/\overline{\text{EN}}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A is programmed to be a master, M/S = 0 means the 82C59A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

$\mu$PM: Microprocessor mode: $\mu$PM = 0 sets the 82C59A for 8080/85 system operation, $\mu$PM = 1 sets the 82C59A for 80C86/88/286 system operation.




NOTE:

1. Edge triggered mode only.

**FIGURE 10. IR TRIGGERING TIMING REQUIREMENTS**

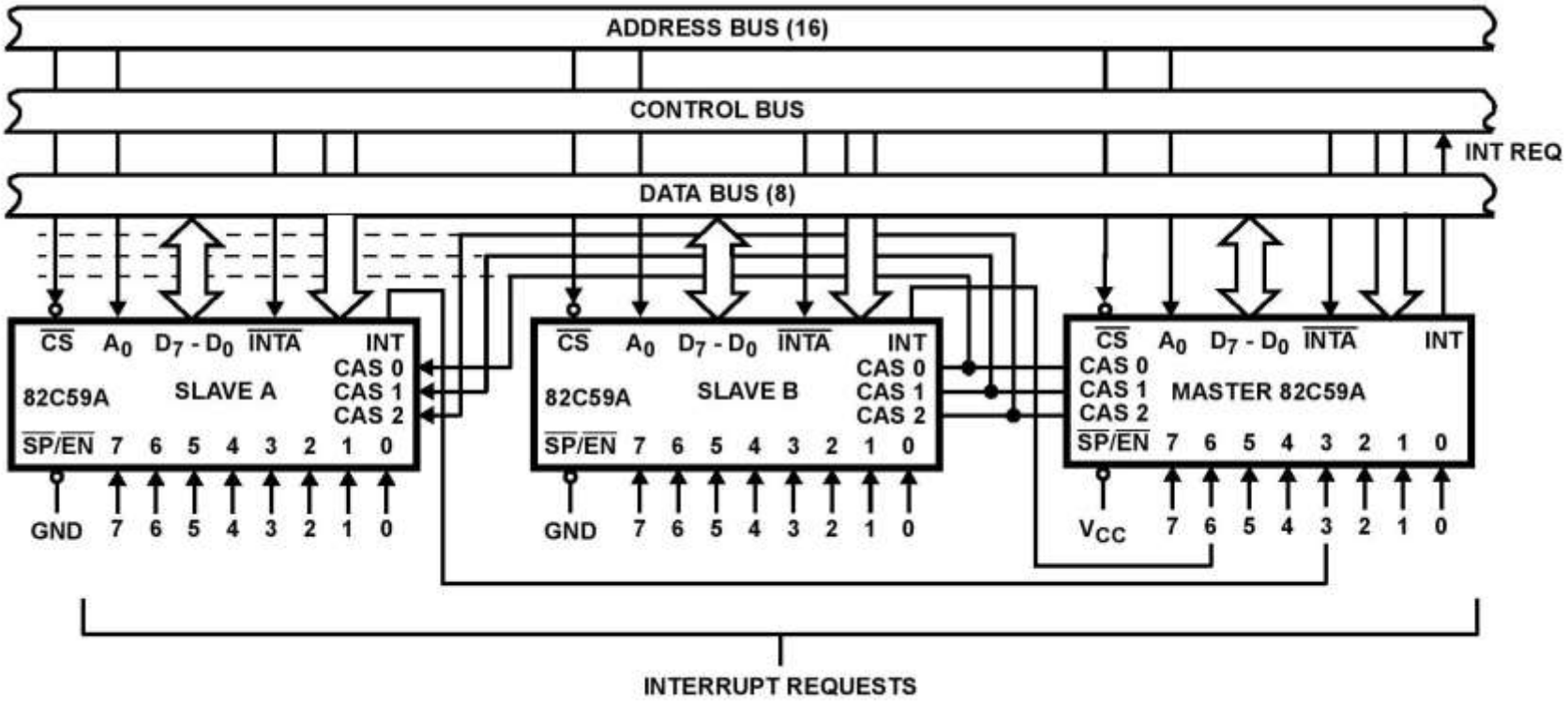
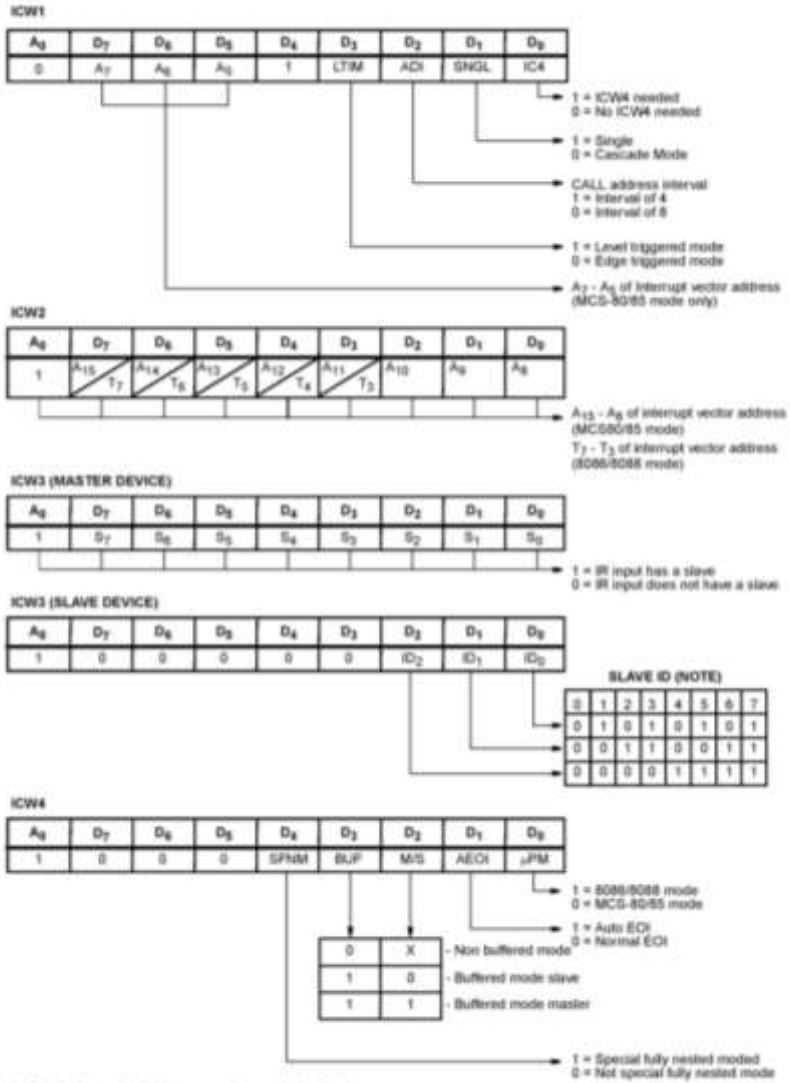



FIGURE 11. CASCADING THE 82C59A




NOTE: Slave ID is equal to the corresponding master IR input.

FIGURE 7. 82C59A INITIALIZATION COMMAND WORD FORMAT





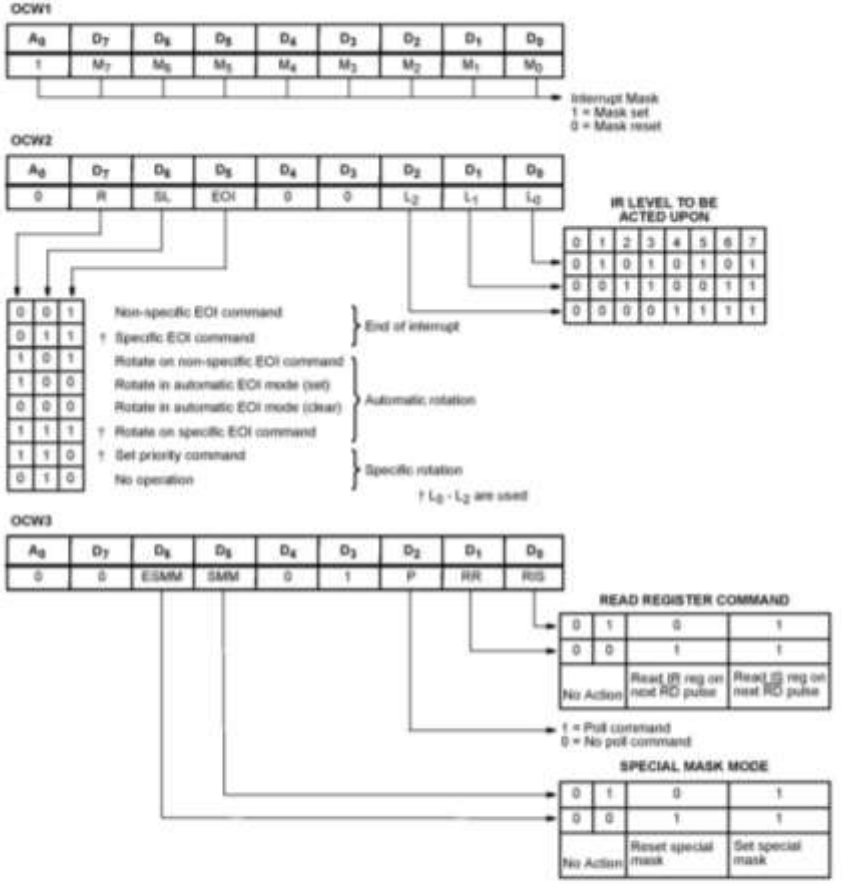



FIGURE 8. 82C59A OPERATION COMMAND WORD FORMAT