Device Usage Page (usage_statistics_webtalk.html)

This HTML page displays the device usage statistics that will be sent to Xilinx.
To see the actual file transmitted to Xilinx, please click here.

software_version_and_target_device			
beta	FALSE	**build_version**	2729669
date_generated	Thu Apr 7 16:11:56 2022	**os_platform**	WIN64
product_version	Vivado v2019.2.1 (64-bit)	**project_id**	85ded234d4c6496c9324c0ce92ea2a3b
project_iteration	4	**random_id**	b2e5dc7b1137534897af11b66bd0cca3
registration_id	b2e5dc7b1137534897af11b66bd0cca3	**route_design**	TRUE
target_device	xc7a35t	**target_family**	artix7
target_package	cpg236	**target_speed**	-1
tool_flow	Vivado		

user_environment			
cpu_name	Intel(R) Core(TM) i7-9700 CPU @ 3.00GHz	**cpu_speed**	3000 MHz
os_name	Windows Server 2016 or Windows 10	**os_release**	major release (build 9200)
system_ram	8.000 GB	**total_processors**	1

vivado_usage		
gui_handlers		
abstractsearchablepanel_show_search=3	addsrcwizard_specify_hdl_netlist_block_design=1	addsrcwizard_specify_or_create_constraint_fi
basedialog_apply=18	basedialog_cancel=18	basedialog_no=1
closeplanner_yes=3	cmdmsgdialog_messages=1	cmdmsgdialog_ok=19
codeview_toggle_column_selection_mode=1	confirmsavetexteditsdialog_cancel=2	constraintschooserpanel_create_file=1
createsrcfiledialog_file_name=18	createsrcfiledialog_file_type=5	expruntreepanel_exp_run_tree_table=1
floatingtopdialog_select_top_module_of_your_design=1	floatingtopdialog_specify_new_top_module=1	flownavigatortreepanel_flow_navigator_tree=
fpgachooser_package=1	fpgachooser_speed=1	gettingstartedview_create_new_project=2
hardwareview_expand_next_level=1	hcodeeditor_close=1	hcodeeditor_search_text_combo_box=2
hpopuptitle_close=4	logmonitor_monitor=1	mainmenumgr_file=2
mainmenumgr_reports=2	mainmenumgr_run=2	mainmenumgr_simulation_waveform=1
mainmenumgr_view=8	mainmenumgr_window=2	maintoolbarmgr_run=5
messagewithoptiondialog_dont_show_this_dialog_again=1	msgtreepanel_message_view_tree=8	msgview_clear_messages_resulting_from_usc
msgview_status_messages=2	msgview_warning_messages=1	netlistschematicview_show_cells_in_this_sch
netlistschematicview_show_nets_in_this_schematic=1	netlisttreeview_netlist_tree=3	newprojectwizard_do_not_specify_sources_at
pacommandnames_add_sources=12	pacommandnames_auto_connect_target=3	pacommandnames_auto_update_hier=14
pacommandnames_log_window=1	pacommandnames_message_window=1	pacommandnames_open_hardware_manager=
pacommandnames_run_bitgen=2	pacommandnames_run_implementation=1	pacommandnames_run_synthesis=1
pacommandnames_simulation_live_break=1	pacommandnames_simulation_live_run=67	pacommandnames_simulation_live_run_all=5
pacommandnames_simulation_run_behavioral=246	pacommandnames_simulation_run_post_synthesis_functional=2	pacommandnames_simulation_settings=33
paviews_project_summary=104	paviews_schematic=5	programdebugtab_open_target=3
programfpgadialog_program=5	progressdialog_cancel=9	projectnamechooser_choose_project_location=
projectsettingssimulationpanel_tabbed_pane=2	projecttab_close_design=1	projecttab_reload=6
rdicommands_delete=2	rdicommands_redo=1	rdicommands_save_file=2
rdiviews_waveform_viewer=49	reportmethodologydialog_results_name=1	saveprojectutils_save=46
schematicview_regenerate=2	selecttopmoduledialog_select_top_module=35	settingsdialog_project_tree=5
simulationliverunforcomp_specify_time_and_units=6	simulationscopespanel_simulate_scope_table=1	srcchooserpanel_add_hdl_and_netlist_files_to
srcchoosertable_src_chooser_table=1	srcmenu_ip_hierarchy=16	stalerundialog_open_design=1
taskbanner_close=40	tclconsoleview_clear_all_output_in_tcl_console=3	tclconsoleview_tcl_console_code_editor=640
waveformnametree_waveform_name_tree=18		

java_command_handlers			
addsources=22	autoconnecttarget=3	closeproject=3	editcopy=1
editdelete=3	launchprogramfpga=5	newproject=1	openhardwaremanager=4
openproject=3	openrecenttarget=1	reportmethodology=1	runbitgen=6
runimplementation=14	runschematic=6	runsynthesis=14	savedesign=5
savefileproxyhandler=3	settopnode=4	showview=9	simulationbreak=1
simulationrelaunch=1	simulationrun=243	simulationrunall=5	simulationrunfortime=63
timingconstraintswizard=1	toolssettings=33	viewtaskimplementation=3	viewtaskrtlanalysis=2
viewtasksynthesis=3			

other_data
guimode=8

project_data			
constraintsetcount=1	core_container=false	currentimplrun=impl_1	currentsynthesisrun=synth_1
default_library=xil_defaultlib	designmode=RTL	export_simulation_activehdl=0	export_simulation_ies=0
export_simulation_modelsim=0	export_simulation_questa=0	export_simulation_riviera=0	export_simulation_vcs=0

export_simulation_xsim=0	implstrategy=Vivado Implementation Defaults	launch_simulation_activehdl=0	launch_simulation_ies=0
launch_simulation_modelsim=0	launch_simulation_questa=0	launch_simulation_riviera=0	launch_simulation_vcs=0
launch_simulation_xsim=244	simulator_language=Mixed	srcsetcount=21	synthesisstrategy=Vivado Synthesis Defaults
target_language=Verilog	target_simulator=XSim	totalimplruns=1	totalsynthesisruns=1

unisim_transformation			
post_unisim_transformation			
bufg=1	fdre=3	gnd=1	ibuf=1
lut1=1	lut2=5	lut3=8	obuf=11
vcc=1			
pre_unisim_transformation			
bufg=1	fdre=3	gnd=1	ibuf=1
lut1=1	lut2=5	lut3=8	obuf=11
vcc=1			

phys_opt_design_post_place			
command_line_options			
-aggressive_hold_fix=default::[not_specified]	-bram_register_opt=default::[not_specified]	-clock_opt=default::[not_specified]	-critical_cell_opt=default::[not_specified]
-critical_pin_opt=default::[not_specified]	-directive=default::[not_specified]	-dsp_register_opt=default::[not_specified]	-effort_level=default::[not_specified]
-fanout_opt=default::[not_specified]	-hold_fix=default::[not_specified]	-insert_negative_edge_ffs=default::[not_specified]	-multi_clock_opt=default::[not_specified]
-placement_opt=default::[not_specified]	-restruct_opt=default::[not_specified]	-retime=default::[not_specified]	-rewire=default::[not_specified]
-shift_register_opt=default::[not_specified]	-uram_register_opt=default::[not_specified]	-verbose=default::[not_specified]	-vhfn=default::[not_specified]

report_drc			
command_line_options			
-append=default::[not_specified]	-checks=default::[not_specified]	-fail_on=default::[not_specified]	-force=default::[not_specified]
-format=default::[not_specified]	-internal=default::[not_specified]	-internal_only=default::[not_specified]	-messages=default::[not_specified]
-name=default::[not_specified]	-no_waivers=default::[not_specified]	-return_string=default::[not_specified]	-ruledecks=default::[not_specified]
-upgrade_cw=default::[not_specified]	-waived=default::[not_specified]		
results			
cfgbvs-1=1	plck-12=1		

report_utilization			
clocking			
bufgctrl_available=32	bufgctrl_fixed=0	bufgctrl_used=1	bufgctrl_util_percentage=3.13
bufhce_available=72	bufhce_fixed=0	bufhce_used=0	bufhce_util_percentage=0.00
bufio_available=20	bufio_fixed=0	bufio_used=0	bufio_util_percentage=0.00
bufmrce_available=10	bufmrce_fixed=0	bufmrce_used=0	bufmrce_util_percentage=0.00
bufr_available=20	bufr_fixed=0	bufr_used=0	bufr_util_percentage=0.00
mmcme2_adv_available=5	mmcme2_adv_fixed=0	mmcme2_adv_used=0	mmcme2_adv_util_percentage=0.00
plle2_adv_available=5	plle2_adv_fixed=0	plle2_adv_used=0	plle2_adv_util_percentage=0.00

dsp			
dsps_available=90	dsps_fixed=0	dsps_used=0	dsps_util_percentage=0.00

io_standard			
blvds_25=0	diff_hstl_i=0	diff_hstl_i_18=0	diff_hstl_ii=0
diff_hstl_ii_18=0	diff_hsul_12=0	diff_mobile_ddr=0	diff_sstl135=0
diff_sstl135_r=0	diff_sstl15=0	diff_sstl15_r=0	diff_sstl18_i=0
diff_sstl18_ii=0	hstl_i=0	hstl_i_18=0	hstl_ii=0
hstl_ii_18=0	hsul_12=0	lvcmos12=0	lvcmos15=0
lvcmos18=0	lvcmos25=0	lvcmos33=1	lvds_25=0
lvttl=0	mini_lvds_25=0	mobile_ddr=0	pci33_3=0
ppds_25=0	rsds_25=0	sstl135=0	sstl135_r=0
sstl15=0	sstl15_r=0	sstl18_i=0	sstl18_ii=0
tmds_33=0			

memory			
block_ram_tile_available=50	block_ram_tile_fixed=0	block_ram_tile_used=0	block_ram_tile_util_percentage=0.00
ramb18_available=100	ramb18_fixed=0	ramb18_used=0	ramb18_util_percentage=0.00
ramb36_fifo_available=50	ramb36_fifo_fixed=0	ramb36_fifo_used=0	ramb36_fifo_util_percentage=0.00

primitives			
bufg_functional_category=Clock	bufg_used=1	fdre_functional_category=Flop & Latch	f
ibuf_functional_category=IO	ibuf_used=1	lut1_functional_category=LUT	l
lut2_functional_category=LUT	lut2_used=5	lut3_functional_category=LUT	l

obuf_functional_category=IO	obuf_used=11

slice_logic			
f7_muxes_available=16300	f7_muxes_fixed=0	f7_muxes_used=0	f7_muxes_util_percenta
f8_muxes_available=8150	f8_muxes_fixed=0	f8_muxes_used=0	f8_muxes_util_percenta
lut_as_logic_available=20800	lut_as_logic_fixed=0	lut_as_logic_used=8	lut_as_logic_util_percer
lut_as_memory_available=9600	lut_as_memory_fixed=0	lut_as_memory_used=0	lut_as_memory_util_pe
register_as_flip_flop_available=41600	register_as_flip_flop_fixed=0	register_as_flip_flop_used=3	register_as_flip_flop_ut
register_as_latch_available=41600	register_as_latch_fixed=0	register_as_latch_used=0	register_as_latch_util_p
slice_luts_available=20800	slice_luts_fixed=0	slice_luts_used=8	slice_luts_util_percenta
slice_registers_available=41600	slice_registers_fixed=0	slice_registers_used=3	slice_registers_util_perc
lut_as_distributed_ram_fixed=0	lut_as_distributed_ram_used=0	lut_as_logic_available=20800	lut_as_logic_fixed=0
lut_as_logic_used=8	lut_as_logic_util_percentage=0.04	lut_as_memory_available=9600	lut_as_memory_fixed=(
lut_as_memory_used=0	lut_as_memory_util_percentage=0.00	lut_as_shift_register_fixed=0	lut_as_shift_register_us
register_driven_from_outside_the_slice_fixed=0	register_driven_from_outside_the_slice_used=0	register_driven_from_within_the_slice_fixed=0	register_driven_from_w
slice_available=8150	slice_fixed=0	slice_registers_available=41600	slice_registers_fixed=0
slice_registers_used=3	slice_registers_util_percentage=<0.01	slice_used=6	slice_util_percentage=0
slicel_fixed=0	slicel_used=1	slicem_fixed=0	slicem_used=5
unique_control_sets_available=8150	unique_control_sets_fixed=8150	unique_control_sets_used=1	unique_control_sets_uti
using_o5_and_o6_fixed=0.01	using_o5_and_o6_used=6	using_o5_output_only_fixed=6	using_o5_output_only_
using_o6_output_only_fixed=0	using_o6_output_only_used=2		

specific_feature			
bscane2_available=4	bscane2_fixed=0	bscane2_used=0	bscane2_util_percentage=0.00
capturee2_available=1	capturee2_fixed=0	capturee2_used=0	capturee2_util_percentage=0.00
dna_port_available=1	dna_port_fixed=0	dna_port_used=0	dna_port_util_percentage=0.00
efuse_usr_available=1	efuse_usr_fixed=0	efuse_usr_used=0	efuse_usr_util_percentage=0.00
frame_ecce2_available=1	frame_ecce2_fixed=0	frame_ecce2_used=0	frame_ecce2_util_percentage=0.00
icape2_available=2	icape2_fixed=0	icape2_used=0	icape2_util_percentage=0.00
pcie_2_1_available=1	pcie_2_1_fixed=0	pcie_2_1_used=0	pcie_2_1_util_percentage=0.00
startupe2_available=1	startupe2_fixed=0	startupe2_used=0	startupe2_util_percentage=0.00
xadc_available=1	xadc_fixed=0	xadc_used=0	xadc_util_percentage=0.00

synthesis			
command_line_options			
-assert=default::[not_specified]	-bufg=default::12	-cascade_dsp=default::auto	-constrset=default::[not_specified]
-control_set_opt_threshold=default::auto	-directive=default::default	-fanout_limit=default::10000	-flatten_hierarchy=default::rebuilt
-fsm_extraction=default::auto	-gated_clock_conversion=default::off	-generic=default::[not_specified]	-include_dirs=default::[not_specified]
-keep_equivalent_registers=default::[not_specified]	-max_bram=default::-1	-max_bram_cascade_height=default::-1	-max_dsp=default::-1
-max_uram=default::-1	-max_uram_cascade_height=default::-1	-mode=default::default	-name=default::[not_specified]
-no_lc=default::[not_specified]	-no_srlextract=default::[not_specified]	-no_timing_driven=default::[not_specified]	-part=xc7a35tcpg236-1
-resource_sharing=default::auto	-retiming=default::[not_specified]	-rtl=default::[not_specified]	-rtl_skip_constraints=default::[not_specified]
-rtl_skip_ip=default::[not_specified]	-seu_protect=default::none	-sfcu=default::[not_specified]	-shreg_min_size=default::3
-top=main	-verilog_define=default::[not_specified]		

usage			
elapsed=00:00:25s	hls_ip=0	memory_gain=687.836MB	memory_peak=1018.125MB

xsim	
command_line_options	
-sim_mode=default::behavioral	-sim_type=default::