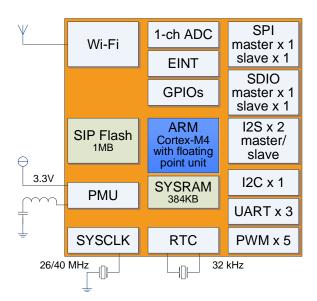


### **PRODUCT OVERVIEW**

MediaTek MT7682S is based around a highly integrated chipset containing a microcontroller unit (MCU), a low power 1x1 11n single-band Wi-Fi subsystem and a power management unit (PMU). The MCU is an <u>ARM Cortex-M4</u> processor with floating point unit, integrated with 1MB flash memory.

The Wi-Fi subsystem contains 802.11b/g/n radio, baseband and MAC designed for low power and high throughput application development. It also contains a 32-bit RISC CPU that could fully offload the application processor.

MT7682 also supports interfaces including UART, I2C, SPI, I2S, PWM, SDIO and ADC.



# **BENEFITS**

- Highly integrated with RF, MCU and memory
- Low power mode with RTC

# **TARGET APPLICATIONS**

- Home appliances
- Home automation
- Smart gadget
- IoT bridge
- Multi-cloud connectivity



# **IoT Wireless Connectivity**

#### **FEATURES**

### Wi-Fi

- IEEE 802.11 b/g/n (2.4GHz, 1x1)
- Supports 20MHz, 40MHz bandwidth in 2.4GHz band
- Wi-Fi security WEP/WPA2/WPS
- SoftAP, sniffer
- Dynamically switching between STA and SoftAP modes at runtime
- MediaTek smart connection
- Multi-cloud connectivity
- Receiver antenna diversity
- Wi-Fi and Bluetooth LE coexistence
- Integrated Balun, PA/LNA
- Optional external LNA and PA support

### Microcontroller subsystem

- 192MHz ARM® Cortex®-M4 with FPU
- 14 DMA channels
- 1 RTC timer, 1 64-bit and 5 32-bit general purpose timers
- Hardware DFS from 3MHz to 192MHz
- Development support: SWD, JTAG
- Crypto engine
  - o AES 128/192/256 bits
  - o DES, 3DES
  - o MD5, SHA-1/224/256/384/512
- True random number generator
- JTAG password protection

# **Memory**

- Up to 384KB SRAM, with zero-wait state and 96MHz maximum frequency
- Up to 32KB L1 cache, with high hit rate, zerowait state and 192MHz maximum frequency
- Embedded 8Mbits flash, with less than 0.1μA (typical) and 80MHz maximum frequency deep power-down current

#### **Communication interfaces**

- 1 SDIO 2.0 master and 1 SDIO 2.0 slave
- 1 I2C (3.4Mbps) interface
- 3 UARTs (3Mbps)
- 1 SPI master and 1 SPI slave (both SCKs are up to 48MHz, quad mode)

- 2 I2S interfaces
  - 1 16/24-bit, master/slave mode
    1 16-bit, master/slave mode with TDM
  - TX/RX channels with 16/24/48/96/192 kHz and 11.025kHz, 22.05kHz, 44.1kHz frequencies
- 5 PWM channels
- 14 GPIOs (fast IOs, 5V-tolerant)
- 1 channel 12-bit AUXADC

# **Power management**

- Integrated DC-DC
- Power input
  - o V<sub>RTC</sub>: from 1.62V to 3.63V
  - O V<sub>PMU</sub> / V<sub>RF</sub>: 3.3V (+/-10%)
  - o V<sub>IO\*</sub>: 1.8V/2.8V/3.3V (+/-10%)
- Off mode: <0.5µA
- Retention mode (with RTC)
  - <2μA (RTC only)</li>
  - o ~4.4μA with 8KB RAM sleep mode
- Deep sleep mode (with external 32kHz clock)
  - 57μA with 0KB RAM sleep mode
  - o 89μA with 384KB RAM sleep mode
- G-band RX power: 59 mA
- G-band TX power
  - o FPA: 268 mA at 19 dBm CCK
  - o HPA: 203 mA at 16.5 dBm OFDM
- DTIM interval with 32kHz external clock source and 384KB SRAM
  - o DTIM=1: 0.74mA
  - o DTIM=3: 0.33mA
- Ambient temperature from -40°C to 85°C

#### **Clock source**

- 26MHz or 40MHz crystal oscillator
- 32kHz crystal oscillator or internal 32kHz RC for RTC

### **Package**

5-mm x 5-mm x 0.9-mm 40-pin QFN with 0.4mm lead pitch

#### Note:

■ The power consumption data is measured at 25°C