MT7687F and MT7697 HDKs' Stamp Module V3.1 Layout Guide

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Document Revision History

Revision	Date	Description
1.0	4 November 2016	Initial version.

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1. Introduction

MT7687F hardware development kit (HDK) is a single chip IEEE 802.11 b/g/n Wi-Fi microcontroller unit (MCU) integrated with high-performance ARM® Cortex®-M4 MCU. MT7687F HDK enables convenient application development with a single integrated circuit (IC). With the on-chip Wi-Fi, internet and robust security protocols, no prior Wi-Fi experience is required for developers to rapidly develop a connected application. MT7687F HDK includes a main board and a MT7687F stamp module, as shown in Figure 1.

This document provides design guidelines for a 4-layer PCB board of the MT7687F stamp module. MT7687F is simple to layout the Quad Flat No-Lead (QFN) packaged devices. This document guides you to achieve high performance results using the MT7687F HDK with a customized design. The content can also be applied to MT7697. In addition to the MT7687F features, MT7697 also supports Bluetooth Low Energy.

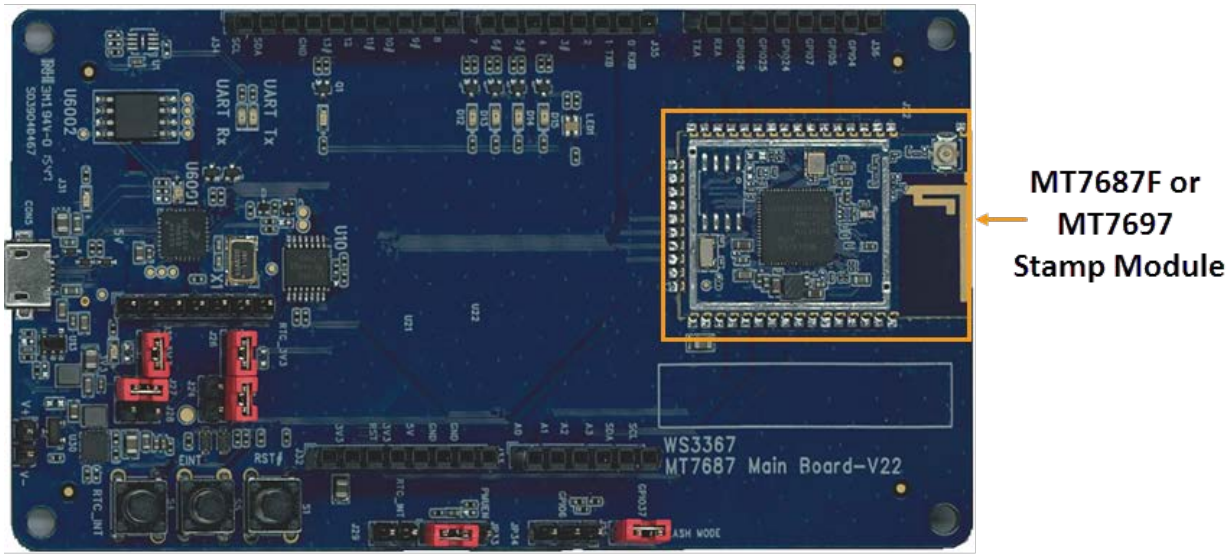

Figure 1. MT7687F HDK's front view with the stamp module

2. PCB Specifications

2.1. PCB stack-up

The MT7687F stamp module has four different layers, as shown in a stack-up diagram (see Table 1). The developers can alter the stack-up layers based on their requirements, but the impedance of 50Ω lines should be recalculated see section 2.2, ”PCB design rules” for more details on impedance control. Having the L1-L2 distance reduced helps improve the grounding and the RF decoupling.

Table 1. The stack-up diagram of the MT7687F stamp module

Top side solder mask				1.00	mils
L1	**TOP**	**Differential and Signal**	**Copper and plating**	1.70	mils
			Prepreg	5.90	mils
L2		**GND**	**copper**	1.25	mils
			core	20.00	mils
L3		**VCC**	**copper**	1.25	mils
			Prepreg	5.90	mils
L4	**Bottom**	**Differential and Signal**	**copper**	1.70	mils
Bottom side solder mask				1.00	mils
TOTAL				39.70	mils
				1.01	mm

Total thickness: 1.0mm (±10%)

Note, it is recommended to keep the L1-L2 distance the same as the suggested value (see Table 1).

2.2. PCB design rules

This section provides the PCB design rules for MT7687F stamp module (see Table 2).

Table 2. PCB design rules

Parameter	Value	Comments
Number of layers	4	
Thickness	1.0 mm (±10%)	For greater thickness increase the distance between L2 and L3.
Size of PCB	20.5mm x 33mm	
Solder mask	Blue	Can be replaced with any color.
Dielectric	FR4	
Silk	White	Can be replaced with any color.
Minimum track width	5 mils	Minimum track width can be reduced but the cost would be higher.

Parameter	Value	Comments
Minimum spacing	5 mils	Minimum spacing can be reduced but the cost would be higher.
Middle drill diameter	8 mils	
Copper thickness	1 oz	
Lead free / Restriction of Hazardous Substances (ROHS)	Yes	
Impedance control	Yes	50Ω controlled impedance trace of 8 mils width on L1 with respect to L2 (GND). Air gap = 5mils Note, the above calculations are based on coplanar waveguide (CPW) not the microstrip.

2.3. Layer Information

The 4-layer PCB is used with the configuration, as shown in Table 3.

Table 3. Layer Information

Layer	Usage	Notes
1	Signal + RF	RF trace is a CPW on L1 with respect to L2 ground.
2	GND	Reference plane for RF.
3	Power + Signal	
4	Power + Signal	

3. Layout Information

3.1. Component placement

The component placement on the MT7687F stamp module is provided in Figure 2. This placement provides optimum device performance. Great care has to be given to the power inductor to ensure reduced emissions and optimum error vector magnitude (EVM) and mass performance. The power inductor should be placed very close to the device and the power trace should be minimized. The MT7687F is sensitive to the layout of the DC-DC converter and it can impact the performance of the device.

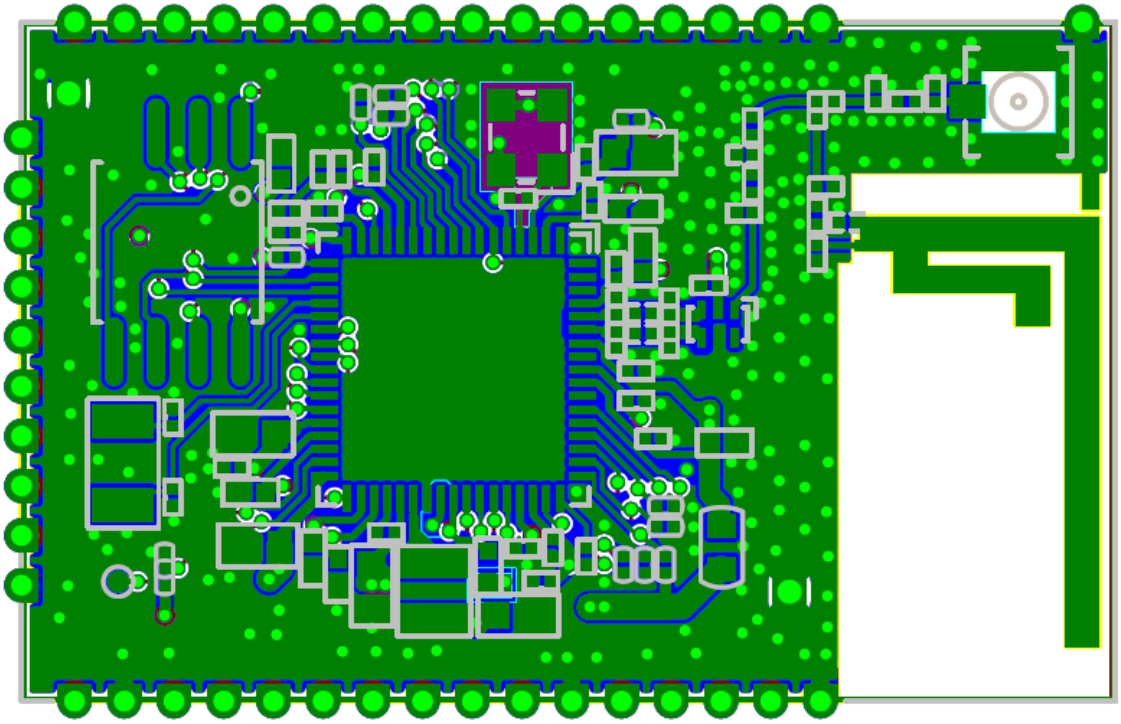

Figure 2. MT7687F stamp module placement diagram

3.2. 4 Layer PCB design

3.2.1. Layer 1

Most of the routing is performed on Layer 1 to avoid power vias on the board (see Figure 3). The trace widths are maximized for high current pins and minimized for signal pins.

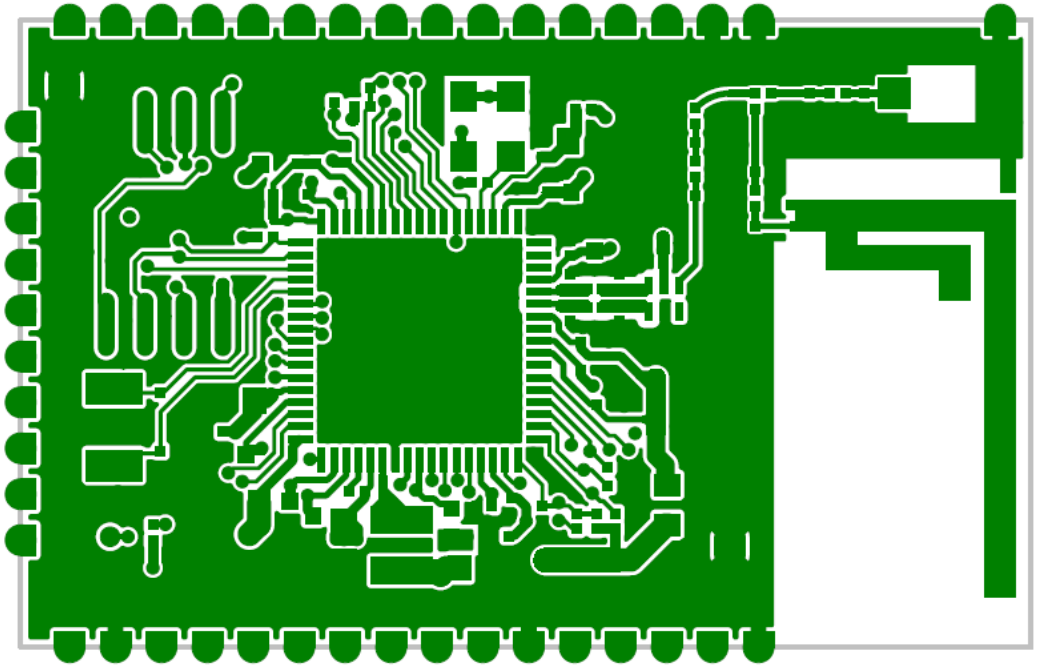

Figure 3. Layer 1

3.2.2. Layer 2

Layer 2 is the primary ground plane for the board reference. It has a void for the antenna section based on the antenna guidelines (see Figure 4).

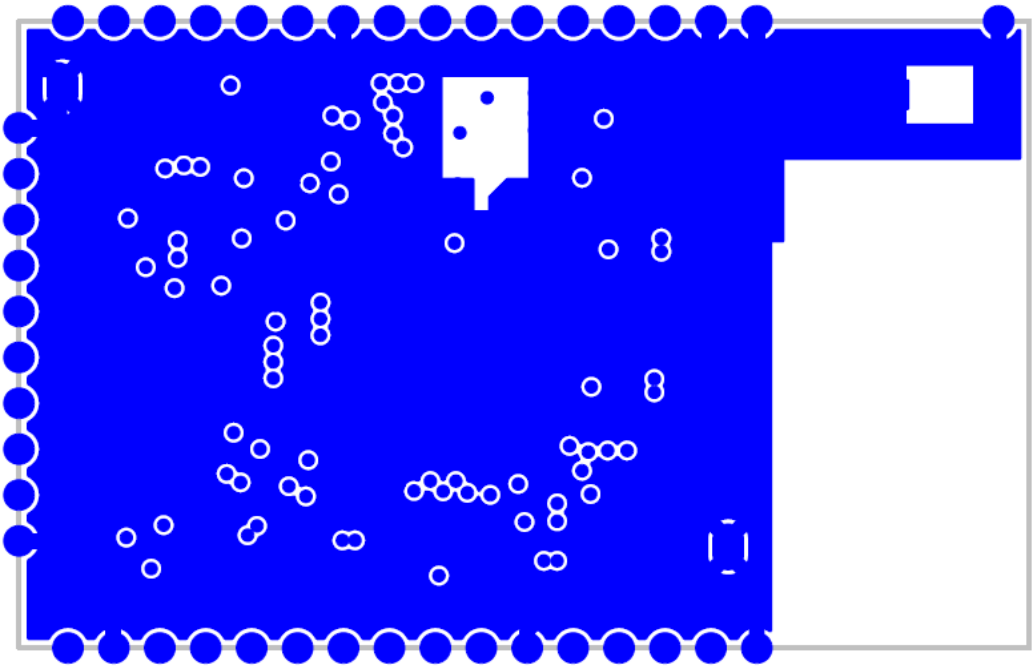

Figure 4. Layer 2

3.2.3. Layer 3

Layer 3 is used to route the power lines to the device (see Figure 5). The width of the power traces is necessary for the main input supply to the device.

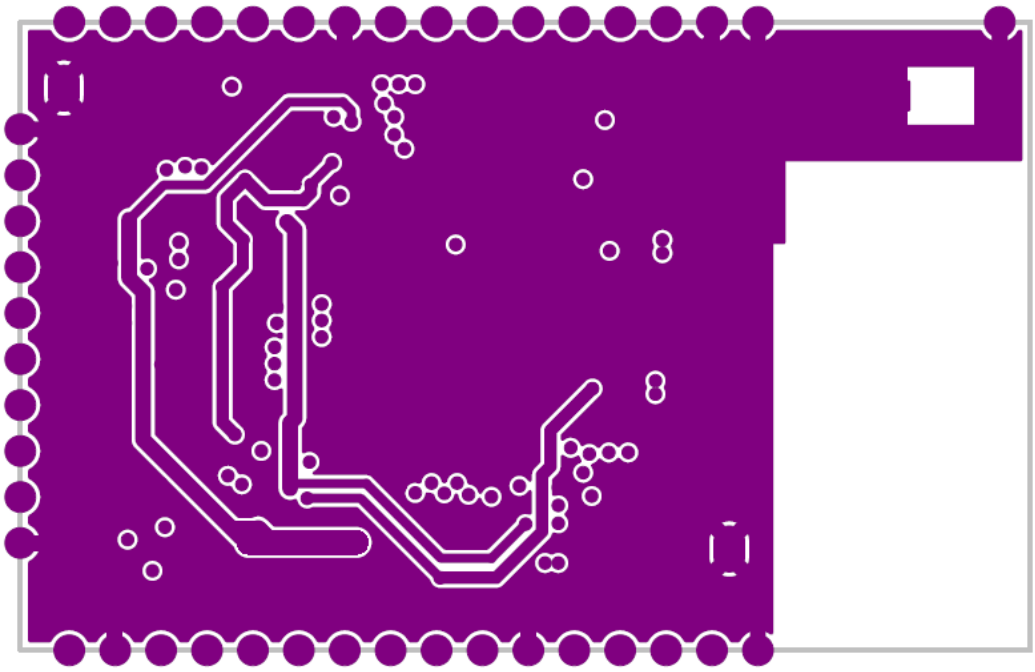

Figure 5. Layer 3

3.2.4. Layer 4

Layer 4 is used for routing the power and the signal lines on the board. It is also the main power dissipation ground (GND) layer for the QFN package (see Figure 6). The bottom GND plane has to be maximized for the best thermal performance.

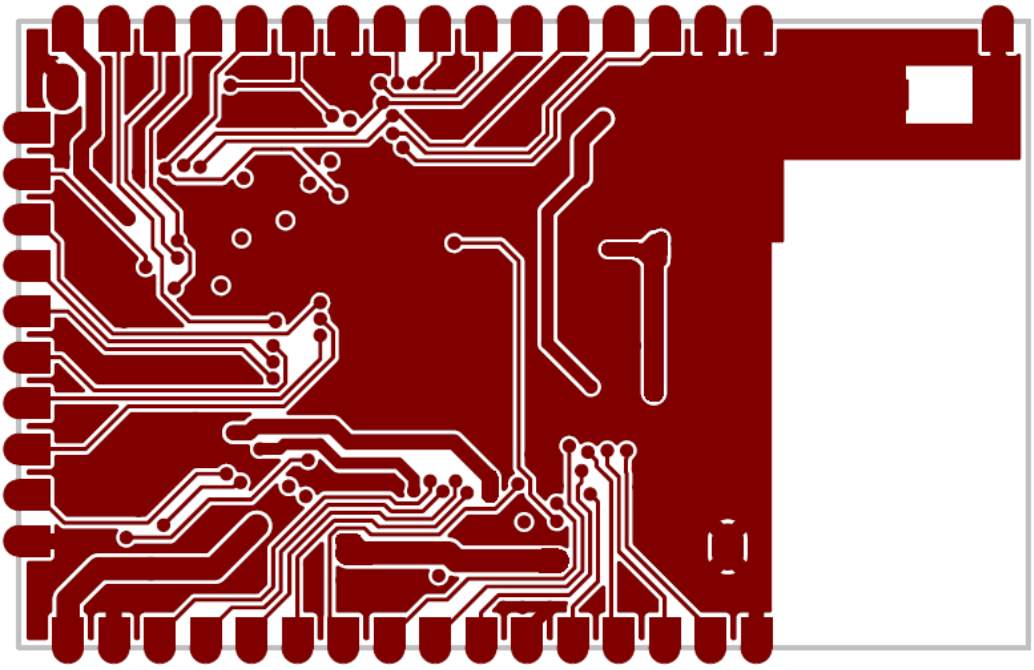

Figure 6. Layer 4

4. Layout Guidelines

4.1. RF section

It is essential to provide a correct layout for the RF section (see Figure 7) for the wireless device in order to achieve optimum device performance. A poor layout can cause performance degradation for the output power, the EVM, the harmonic emission, the sensitivity and the spectral mask.

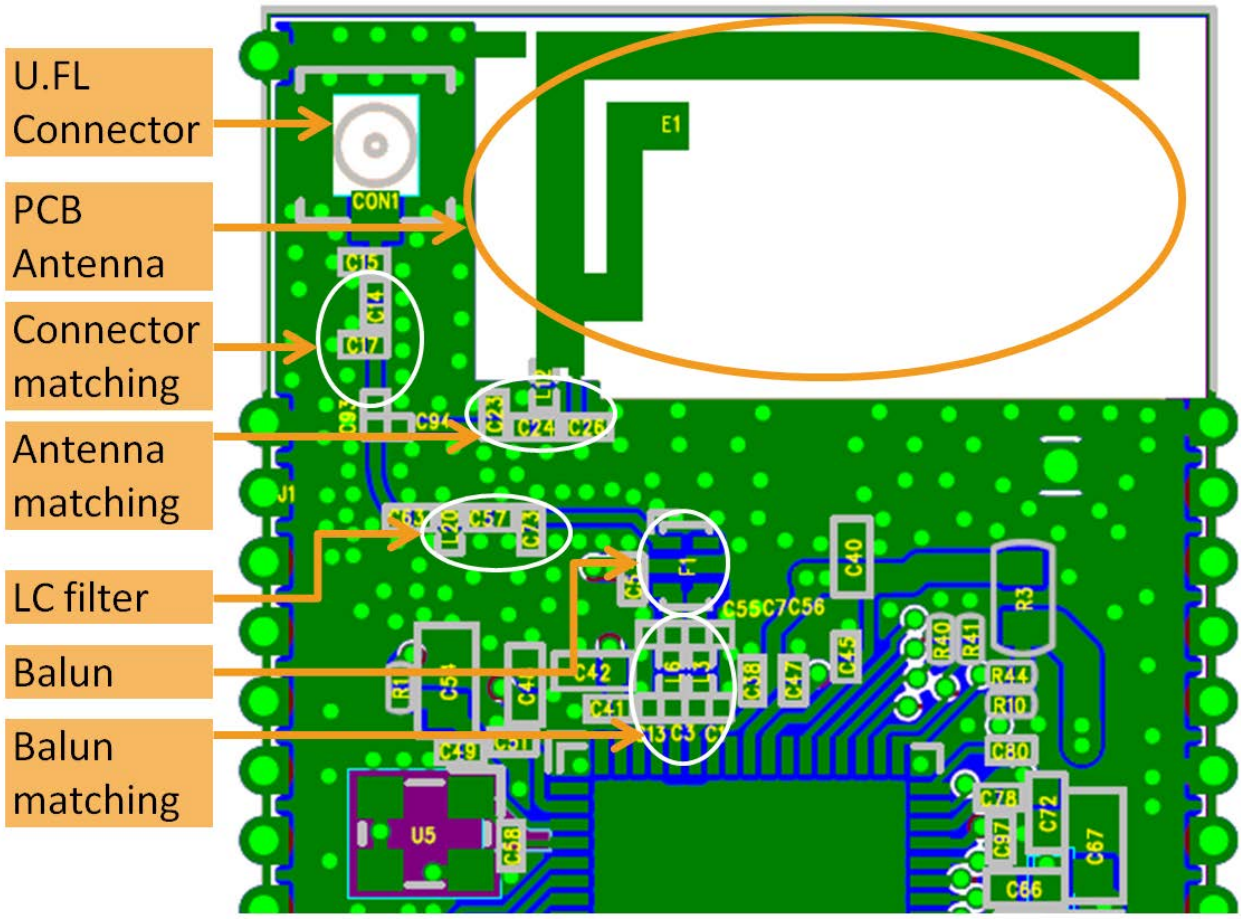

Figure 7. RF section

4.1.1. RF component placement and routing

The balun, balun matching and LC filter are used on the board to perform the important function of attenuating the out-of-band emissions from the device, as shown in Figure 8. Because MT7687F RF output is differential, it needs a balun to convert to a single-ended output. Reserve the balun matching and LC filter to optimize transmit and receive performance. The component placement and routing also effects the performance of wireless transmit and receive operations. The recommended balun is of type BL1608-05A2450TB. The datasheet of the balun can be accessed here.

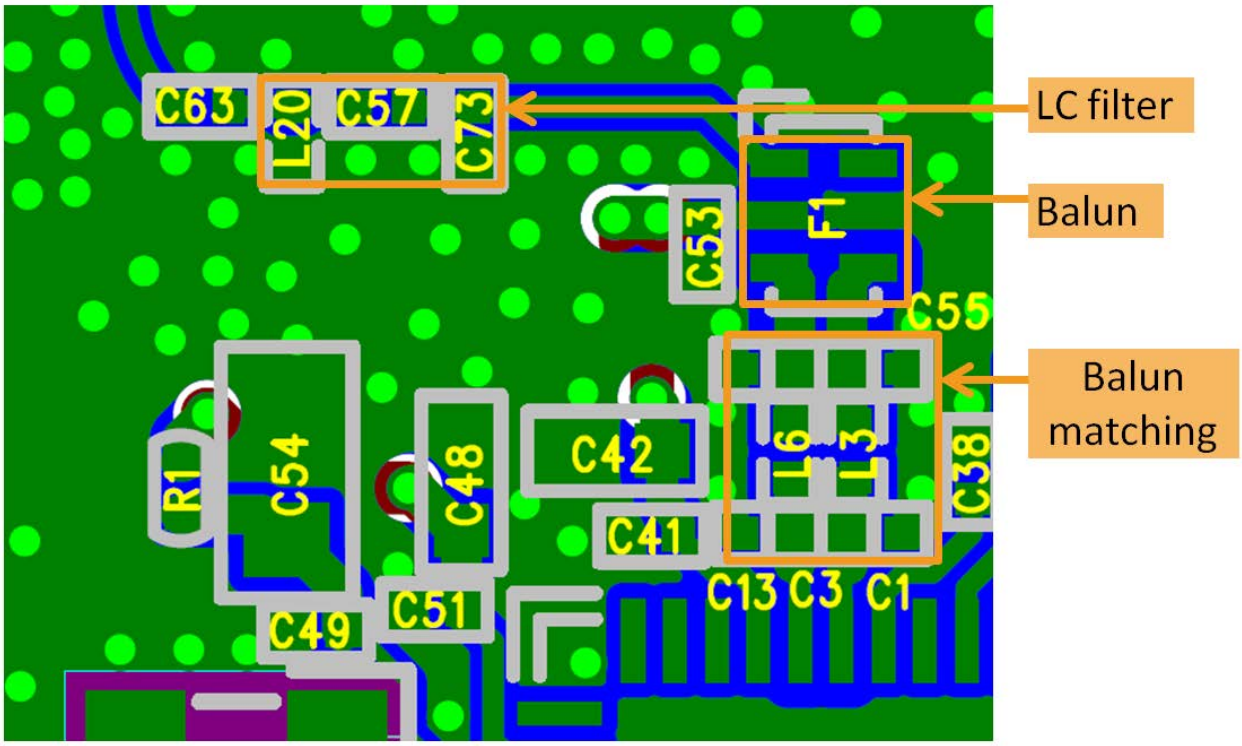

Figure 8. RF component placement and routing

Apply the following RF component placement and routing guidelines.

1) Place balun matching network close to the MT7687F pinout. Route the RF lines at the output of the balun using a CPW with ground structure.
2) Use via stitching along the RF trace to reduce emissions and keep the fields confined within the trace boundary.
3) Use an impedance of 50Ω only with a tolerance of 10%. Use the stack-up and the trace width provided for reference see section 2.2, “PCB design rules”.
4) In case a conducted test is required on the PCB, it is recommended to add a U.FL connector, as shown in Figure 7.

4.1.2. Antenna placement and routing

The antenna is the element used to convert the guided waves on the PCB traces to the free-space electromagnetic radiation. The placement and layout of the antenna is the key to increase in range and data rates. MT7687F module is designed with a stamp module and a PCB antenna. In order to optimize the antenna performance, it needs to mount the stamp module on a main board as shown in Figure 9.

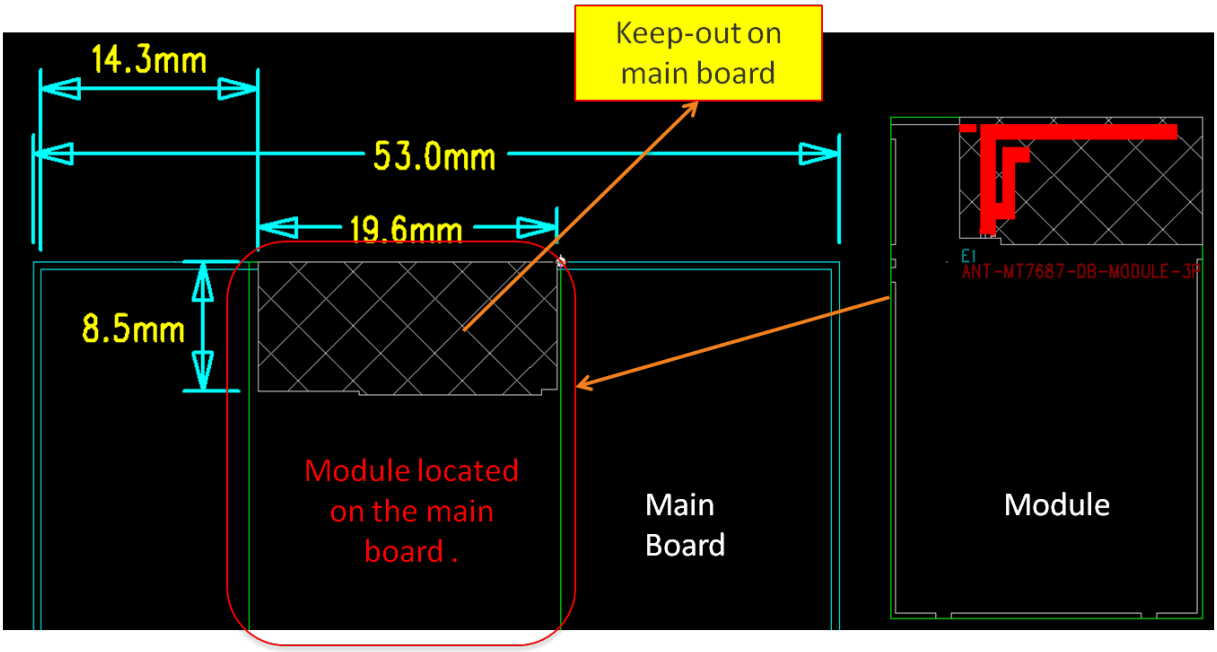

Figure 9. Stamp module located on the main board

Apply the following guidelines for the antenna placement.

1) Place the PCB antenna on an intermediate edge of the PCB.
2) Make sure that no signals are routed across the antenna elements on all the layers of the PCB.
3) The antenna requires ground clearance on all layers of the PCB. Ensure that the ground is cleared on inner layers as well.
4) Ensure that there is provision to place matching components for the antenna. These need to be tuned for the best return loss once the complete board is assembled. Any plastics or casing should also be mounted while tuning the antenna as this can impact the impedance.
5) Ensure that the antenna impedance is 50Ω as the device is rated to work only with a 50Ω system.

4.1.3. Transmission line

The RF signal from the balun output is routed to the antenna using a CPW with ground structure. This structure offers the best possible shielding to the RF lines, as shown in Figure 10. In addition to the ground on the Layer 1, placing GND vias along the line also provides additional shielding.

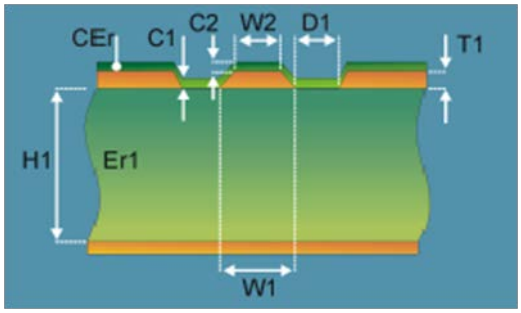

Figure 10. CPW with ground

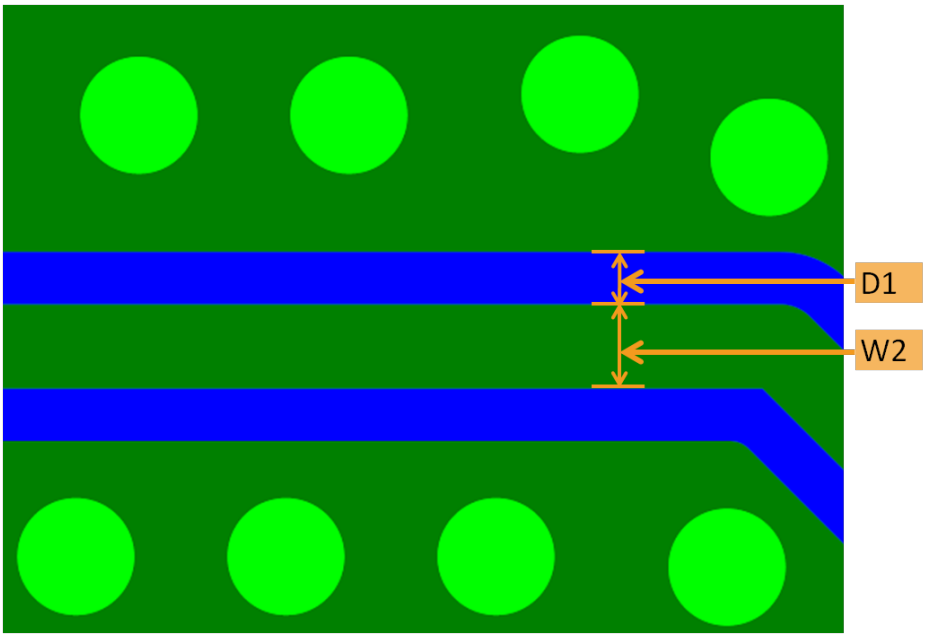

Figure 11. CPW with ground top view

The recommended values for the PCB (see Figure 10 and Figure 11) are provided in Table 4.

Table 4. Recommended values for the PCB

Parameter	Value (mils)
W2	8
D1	5
H1	5.9
Er1	3.66

4.2. Power section

This section provides detailed description to design a power efficient device. The details on net or pin locations are shown in Figure 12, Figure 13, and Figure 14.

1) Make the buck inductor trace loop as short as possible.
2) The de-cap routing has to be in a correct order.
3) The LXBK (net of Buck output) trace width should be 30mil (recommended) not less than 9mil because of the large current flow. LXBK trace width that is close to IC should be no less than 9mil.
4) Connect AVDD16_XO (Pin 3) to de-coupling capacitor 10pF first. Place the 4.7uF capacitor closer to IC.
5) MT7687 power input pins' decouple capacitors should be placed as close as possible (especially the small capacitors.)
    - AVDD16_WF0_AFE, AVDD16_XO and AVDD16 (see Figure 13).

- AVDD33_WF0_G_TX, AVDD33_WF0_G_PA (see Figure 14).

6) Decouple capacitor (C53) at DC feed port of the balun should also be placed as close as possible. The small capacitor is the DC feed port.

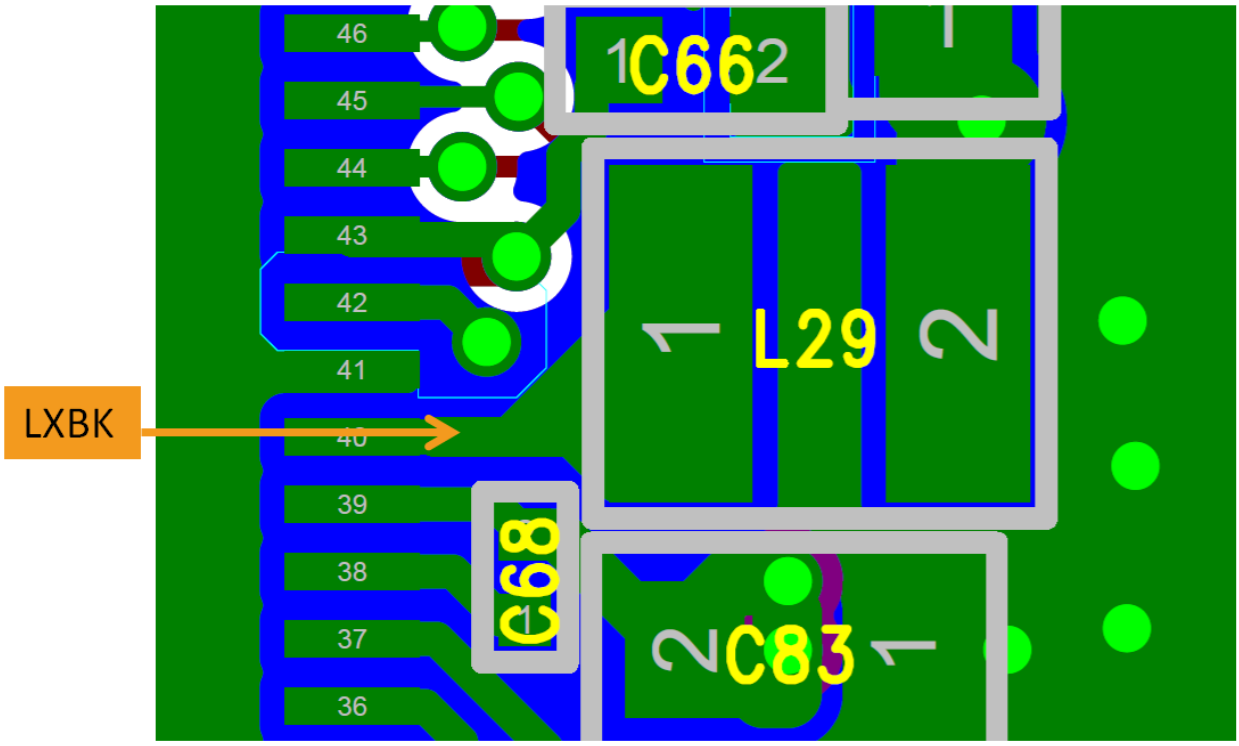

Figure 12. Placement and routing example of LXBK

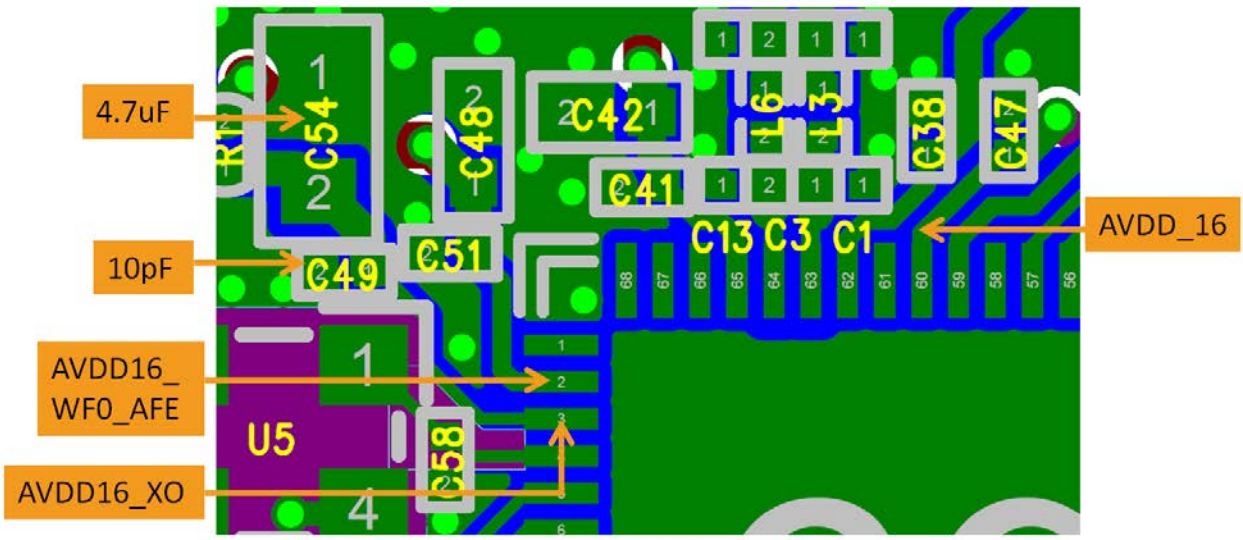

Figure 13. Placement and routing example of AVDD16

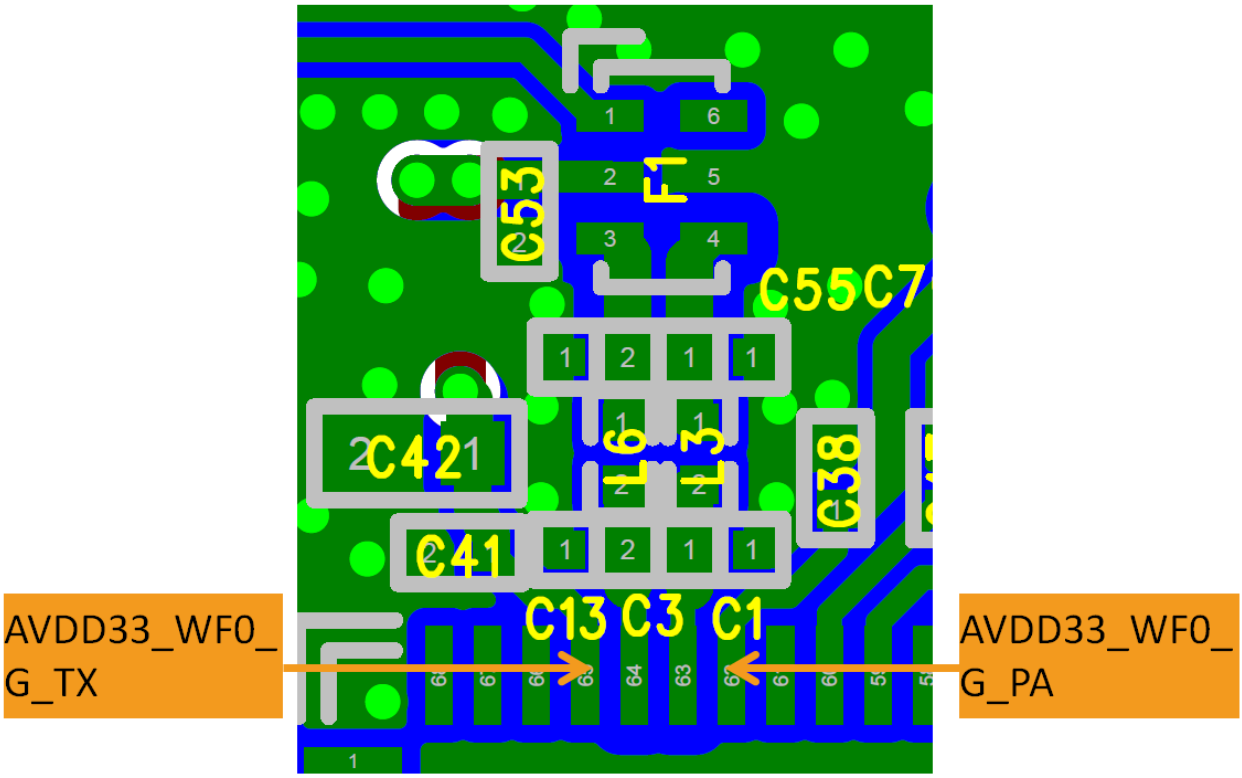

Figure 14. Placement and routing of AVDD33_WF0_G_PA and AVDD33_WF0_G_TX

4.3. Clock section

4.3.1. 40MHz XTAL

The 40M XTAL should be placed closer to the QFN package. The frequency tolerance for the XTAL across temperature with aging should be +/-20ppm. In addition, ensure no high frequency lines are routed closer to the XTAL routing to avoid any phase noise degradation.

4.3.2. 32.768kHz XTAL

The 32.768K XTAL should be placed closer to the QFN package. Ensure the load capacitance is tuned based on board parasitic so that the frequency tolerance is within ± 150ppm.

4.4. Digital I/O

Route serial peripheral interface (SPI) and universal asynchronous receiver/transmitter (UART) lines away from any RF traces since these digital I/O lines are high frequency lines and can cause interference to the RF signal.

4.5. QFN Ground

Make sure QFN 8x8 ground vias are placed on the ground pad for optimum thermal dissipation as shown in Figure 15.

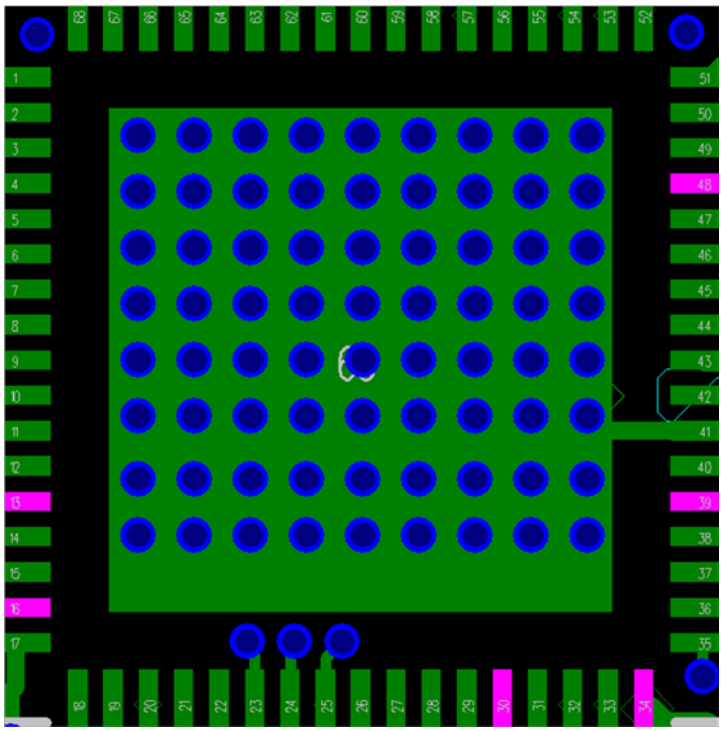

Figure 15. QFN 8x8 ground vias on the ground pad