LinkIt 2523 HDK V11 Layout Guide

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Document Revision History

Revision	Date	Description
1.0	2 September 2016	Initial version. This layout guide is for LinkIt 2523 HDK V11.

Table of contents

Lists of tables and figures

1. Introduction

LinkIt 2523 hardware development kit (HDK) for RTOS is a fully functional platform for IoT and Wearables applications powered by MT2523G/MT2523D and an ARM Cortex-M4 core-based microcontroller unit (MCU). The HDK has rich connectivity features and interfaces such as SPI, I2S, PCM, UART, ADC, PWM, JTAG and clock-out generators. The front view of the board is shown in Figure 1, and bottom view is in Figure 2.

This document provides design guidelines for a 4-layer PCB board of the LinkIt 2523 HDK. The HDK is designed in thin and fine-pitch BGA (TFBGA) package to achieve high performance results with a customized design.

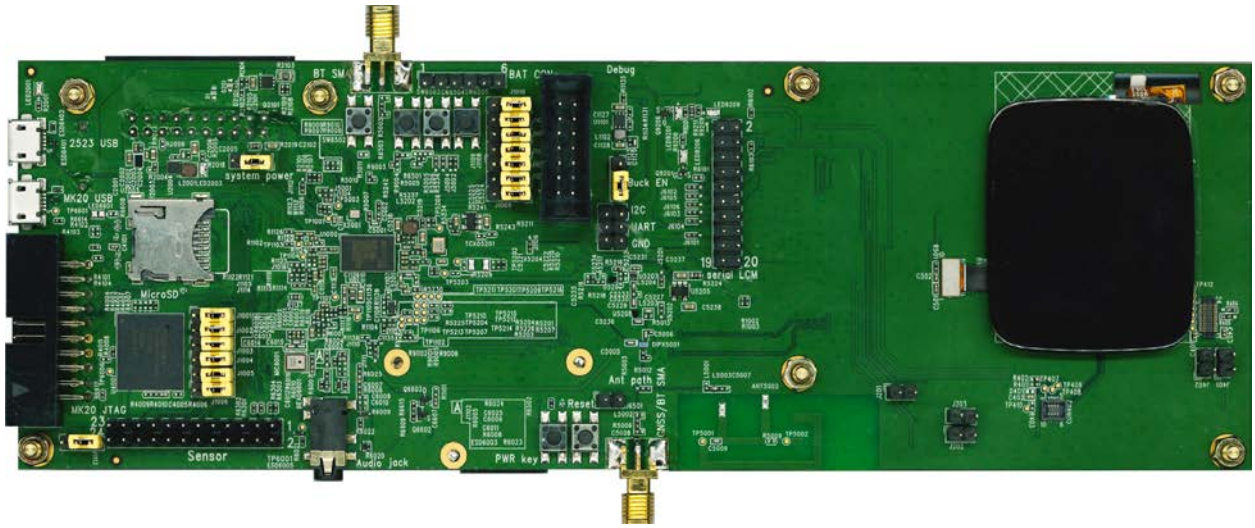

Figure 1. LinkIt 2523 HDK's front view

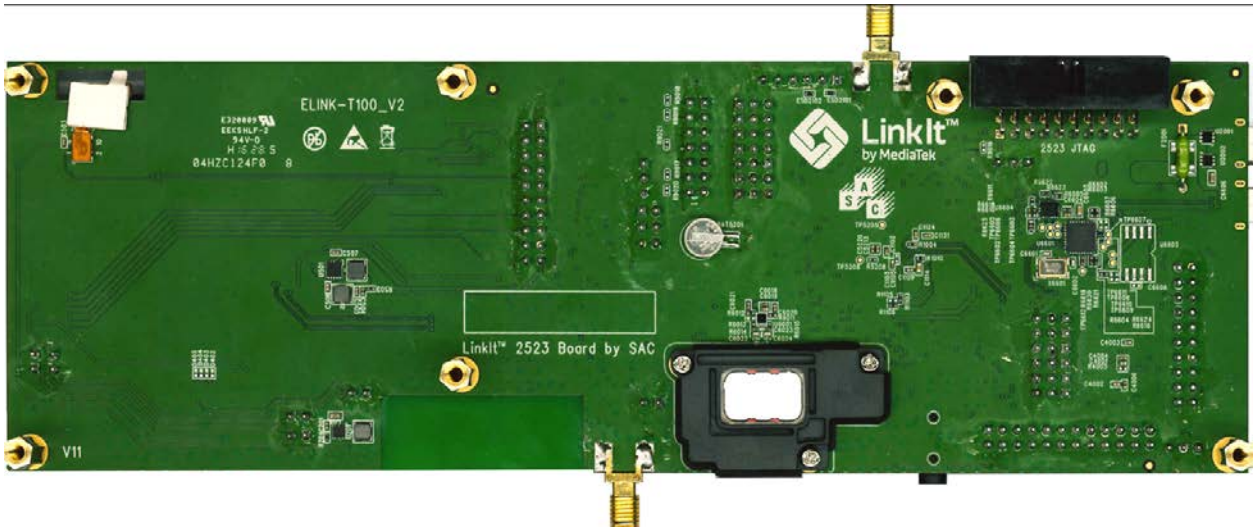

Figure 2. LinkIt 2523 HDK's bottom view

2. PCB Specifications

2.1. PCB stack-up

The LinkIt 2523 HDK has four different layers, as shown in a stack-up layout in Table 1. The developers can alter the stack-up layers based on their requirements, but the impedance of 50Ω lines should be recalculated as in see section 2.2, “PCB design rules” for more details on impedance control. Having the L1-L2 distance reduced helps improve the grounding and the RF decoupling.

Table 1. The stack-up layers of the LinkIt 2523 HDK

Top side solder mask				1.00	mils
L1	**TOP**	**Differential and signal**	**Copper and plating**	1.60	mils
			Prepreg	3.00	mils
L2		**GND**	**Copper**	1.20	mils
			Core	48.78	mils
L3		**VCC**	**Copper**	1.20	mils
			Prepreg	3.00	mils
L4	**Bottom**	**Differential and signal**	**Copper**	1.60	mils
Bottom side solder mask				1.00	mils
TOTAL				62.38	mils
				1.58	mm

Total thickness: 1.6mm (±10%)

2.2. PCB design rules

This section provides the PCB design rules for LinkIt 2523 HDK (see Table 2).

Table 2. PCB design rules

Parameter	Value	Comments
Number of layers	4	
Thickness	1.6 mm (±10%)	For greater thickness increase the distance between L2 and L3.
Size of PCB	150mm x 70mm	
Solder mask	Green	Can be replaced with any color.
Dielectric constant	FR4	Flame resistance of grade four.
Silk	White	Can be replaced with any color.
Minimum track width	4 mils	Minimum track width can be reduced but the cost would be higher.
Minimum spacing	4 mils	Minimum spacing can be reduced but the cost would be higher.

Parameter	Value	Comments
Middle drill diameter	8 mils	
Copper thickness	0.5 oz	
Lead free / Restriction of Hazardous Substances (ROHS)	Yes	
Impedance control	Yes	50Ω controlled impedance trace of 8 mils width on L1 with respect to L2 (GND). Air gap = 4mils Note, the above calculations are based on coplanar waveguide (CPW), not the microstrip.

2.3. Layer Information

The 4-layer PCB is used with the configuration, as shown in Table 3.

Table 3. PCB layers

Layer	Usage	Notes
1	Signal and RF	RF trace is a CPW on L1 with respect to L2 ground.
2	GND	Reference plane for the RF.
3	Power and signal	
4	Power and signal	

3. Layout Information

3.1. Component placement

The component placement on the LinkIt 2523 HDK is provided in Figure 1 and Figure 2. It considers efficient placement of the peripherals; the peripherals of LCM, audio jack, USB connectors, SMA headers are placed on the edge of the PCB. The sensor daughterboard and battery daughterboard overlap on the HDK to make the HDK dimensions smaller. The speaker, buck LDO and CMSIS-DAP are placed on the bottom side for dimension consideration. The buck LDO is placed near the USB connector for power efficiency.

3.2. 4 Layer PCB design

3.2.1. Layer 1

Most of the routing and placement is implemented on Layer 1 for an easier access to the peripherals and board functionality, as shown in Figure 3. The functionality of the board can be conveniently switched using jumpers, such as switching between eMMC and micro SD or camera and sensor daughterboard. The trace widths are maximized for high current pins and minimized for signal pins. Onboard GNSS and Bluetooth antenna is also placed in this layer, at the bottom side of the PCB; to provide better antenna performance, isolated area for pure FR4 material without copper poured is needed.

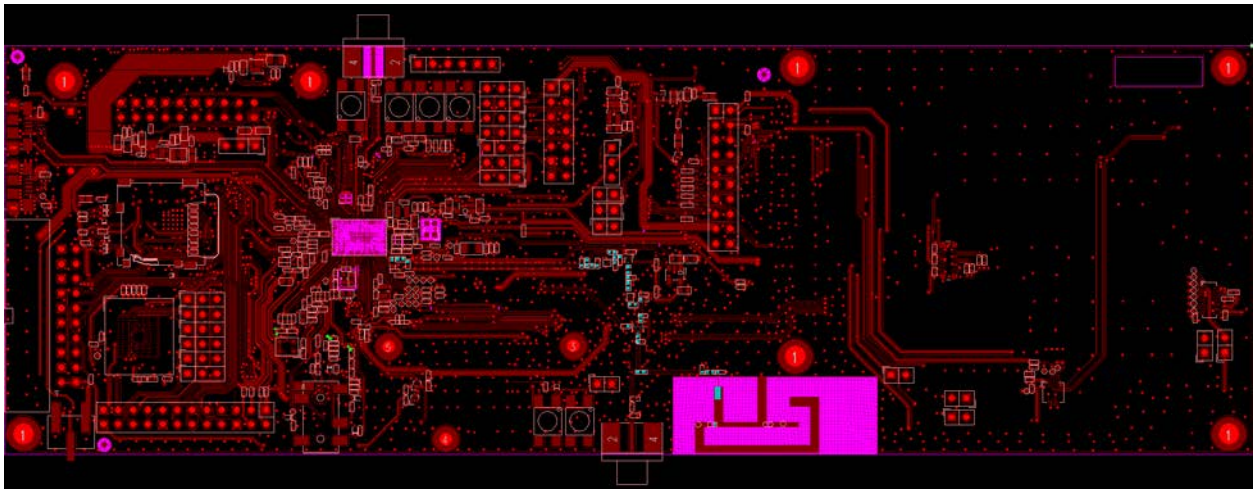

Figure 3. Layer 1 of the HDK's PCB layout

3.2.2. Layer 2

Layer 2 is the primary ground plane of the HDK and for the MCU's internal ball fan out, as shown in Figure 4. It has a void for the antenna section based on the antenna guidelines. The area of onboard antenna is excluded from the routing or grounding for better antenna performance.

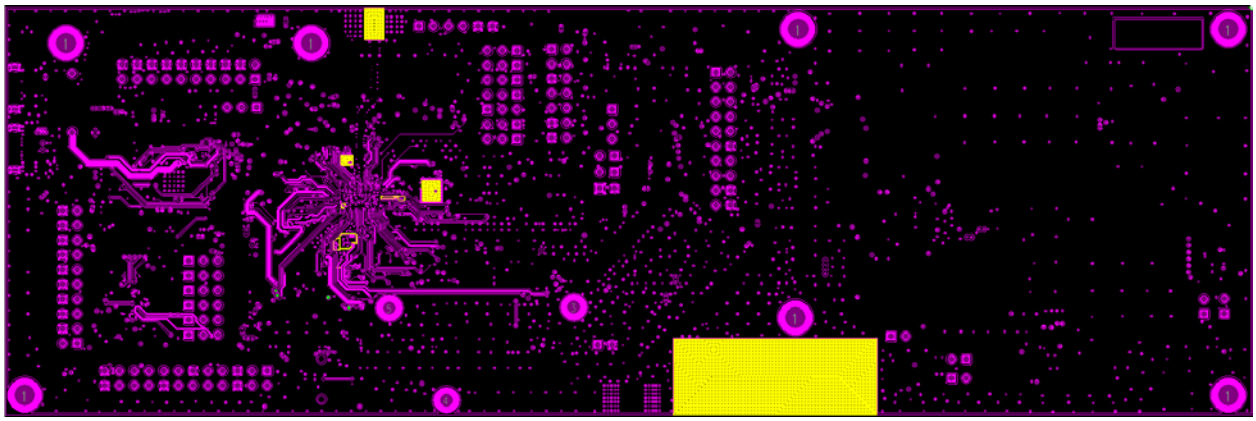

Figure 4. Layer 2 of the HDK's PCB layout

3.2.3. Layer 3

Layer 3 is used to route the power lines to the device that includes some of the high speed signal routing. The width of the power traces is required for the main input supply to the device. High speed signal routing is also available to reference the bottom layer of the main ground. The area of onboard antenna is excluded from routing or grounding for better antenna performance. Figure 5 provides the Layer 3 routing of the HDK.

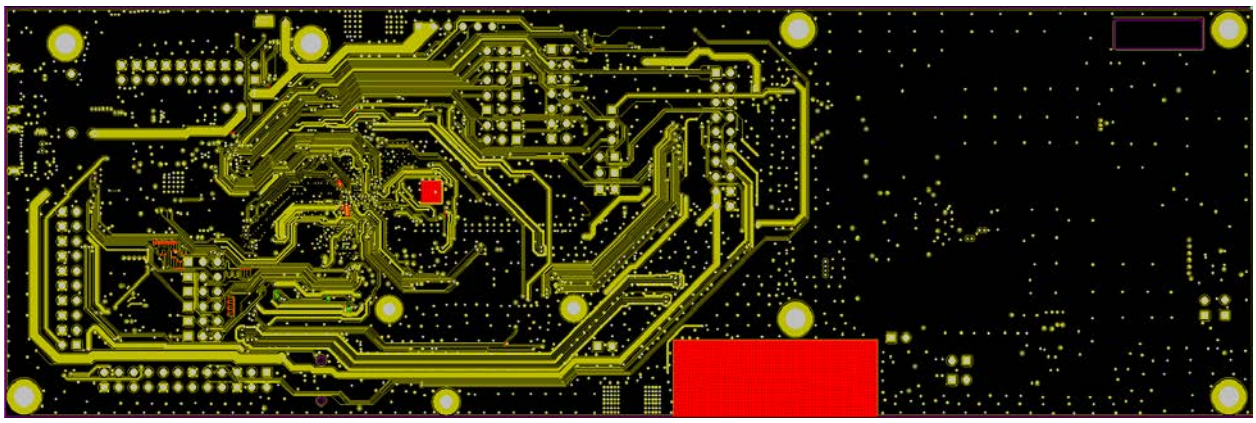

Figure 5. Layer 3 of the HDK's PCB layout

3.2.4. Layer 4

Layer 4 is used for routing the power and the signal lines on the board, as shown in Figure 6. The bottom GND plane has to be maximized for the best thermal performance and high speed signal reference layer. Some components are also placed in the bottom layer for dimension consideration. Only a few high speed signals are routed through this layer. The area of an onboard antenna is excluded from the routing or grounding for better antenna performance.

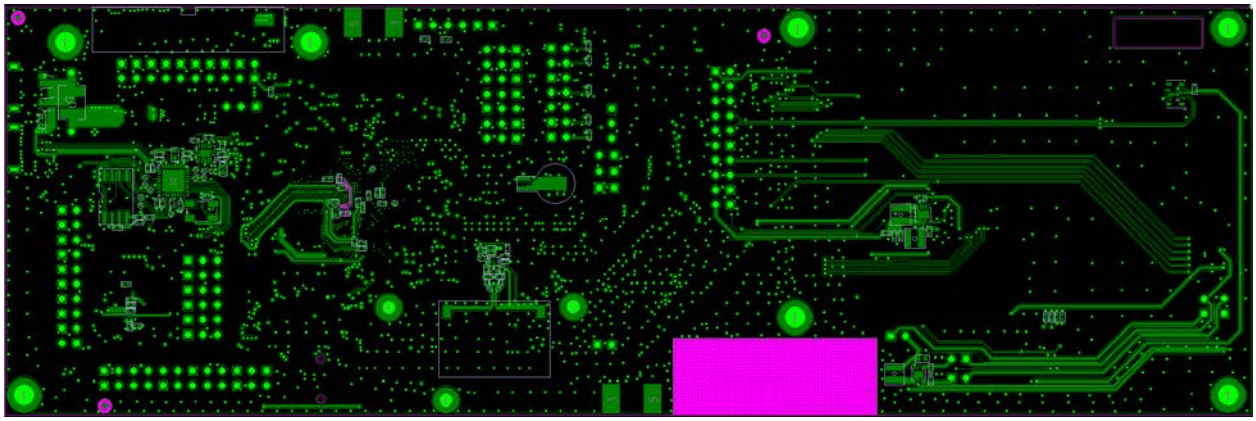

Figure 6. Layer 4 of the HDK's PCB layout

4. Layout Guidelines

4.1. GNSS section layout guide

LinkIt 2523 HDK supports GNSS connectivity. This section provides details on the GNSS layout routing. The GNSS RF front-end is responsible to receive the navigation signal. TCXO should be placed far from the heat source to avoid the thermal impact. The LDO provides stable power source for GNSS module's operation. The RTC enables warm start of the GNSS module for faster satellite acquisition.

4.1.1. GNSS RF trace routing guide

For the RF path routing, path length should be as short as possible to reduce the RF signal loss. The RF trace also should be considered under 50Ω impedance controlled only with a tolerance of 10%, and these impedance traces need ground trace to cover them to avoid noise impact. Keep the active GNSS antenna as far from the interference source as possible. Parts of layout are shown in Figure 7 based on the layout guidelines. Apply the following guidelines for the antenna placement and reference routing design.

1) Place the PCB antenna on an intermediate edge of the PCB.
2) Make sure that no signals are routed across the antenna elements on all the layers of the PCB.
3) The antenna requires ground clearance on all layers of the PCB. Ensure that the ground is cleared on inner layers as well.
4) Ensure that there is provision to place matching components for the antenna. These need to be tuned for the best return loss once the complete board is assembled. Any plastics or casing should also be mounted while tuning the antenna as this can impact the impedance.
5) Ensure that the antenna impedance is 50Ω as the device is rated to work only with a 50Ω system.

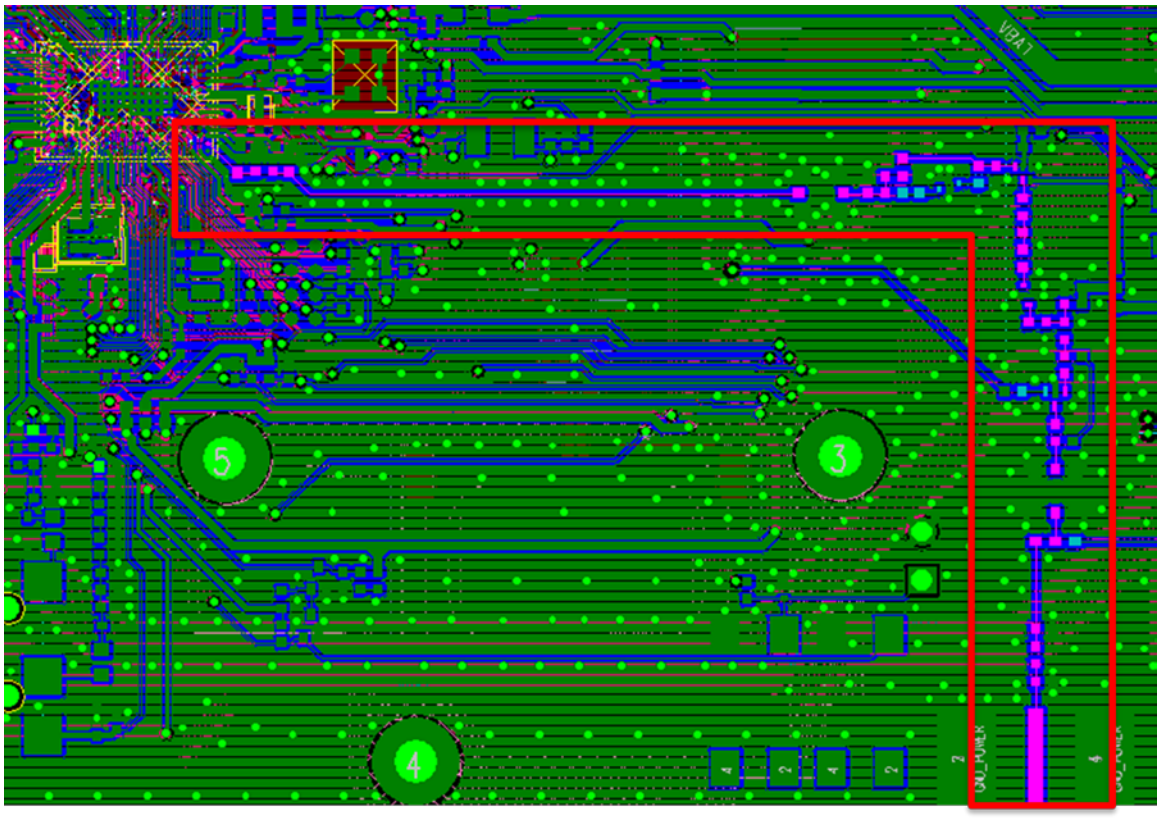

Figure 7. RF component placement and routing

4.1.2. TCXO placement and routing

To reduce the thermal impact and to improve the clock stability, it's advised not to apply any copper over Layer 2 to provide empty spacing. Keeping a shorter length trace from the TCXO ground pad to the PCB ground provides resistance to reduce the thermal impact. The routing of TCXO in multi layers is shown in Figure 8.

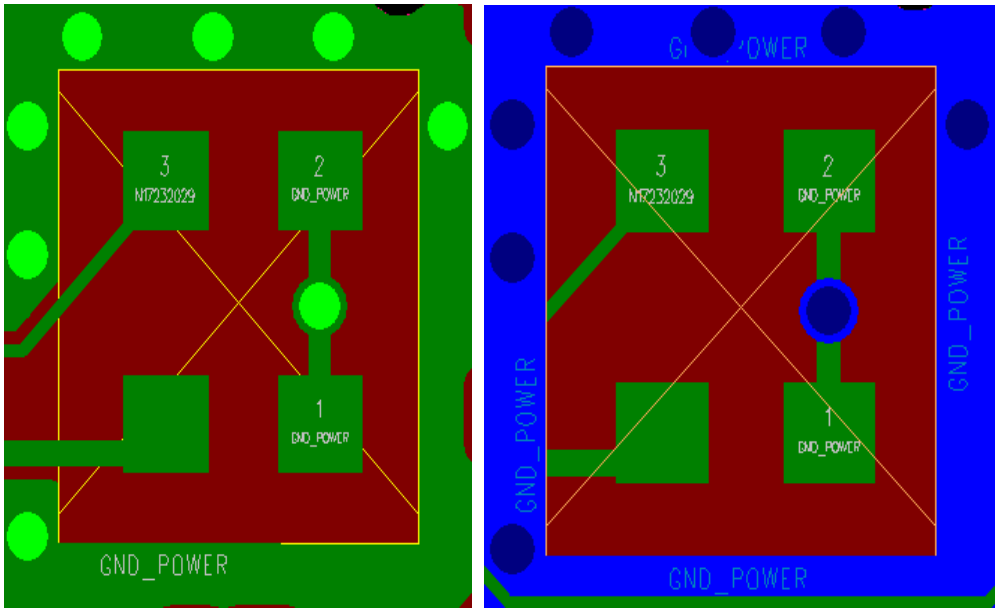

Figure 8. TCXO layout routing in multiple layers

4.1.3. GNSS components placement guide

To improve the HDK's internal buck LDO performance, route the ball AVSS43_DCV to ground the bypass capacitor located near the IC, and then connect to the main ground. Apply a capacitor, to provide a more stable signal, shorter trace and shorter wiring. The routing and placement of LDO capacitor are shown in Figure 9.

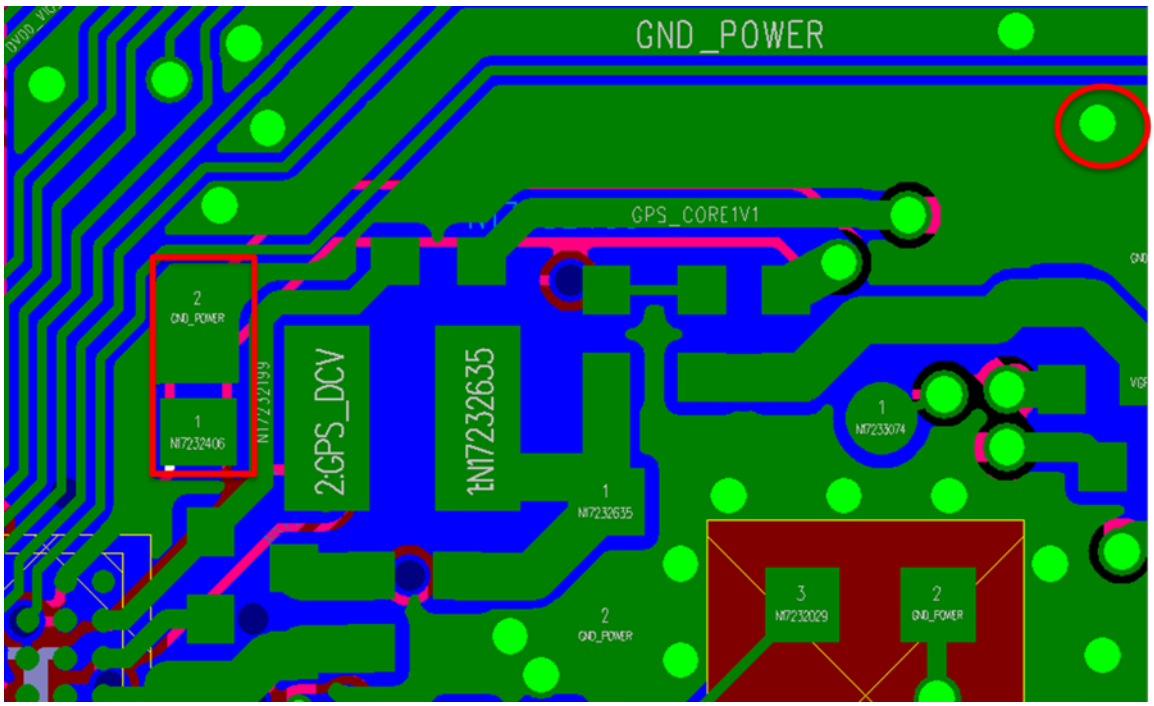

Figure 9. AVSS43_DCV pin to ground the bypass the capacitor

The AVDD18_RXFE and AVDD18_CM pins are needed for the bypass capacitor; place at least one piece of 4.7nF capacitor, as shows in Figure 10.

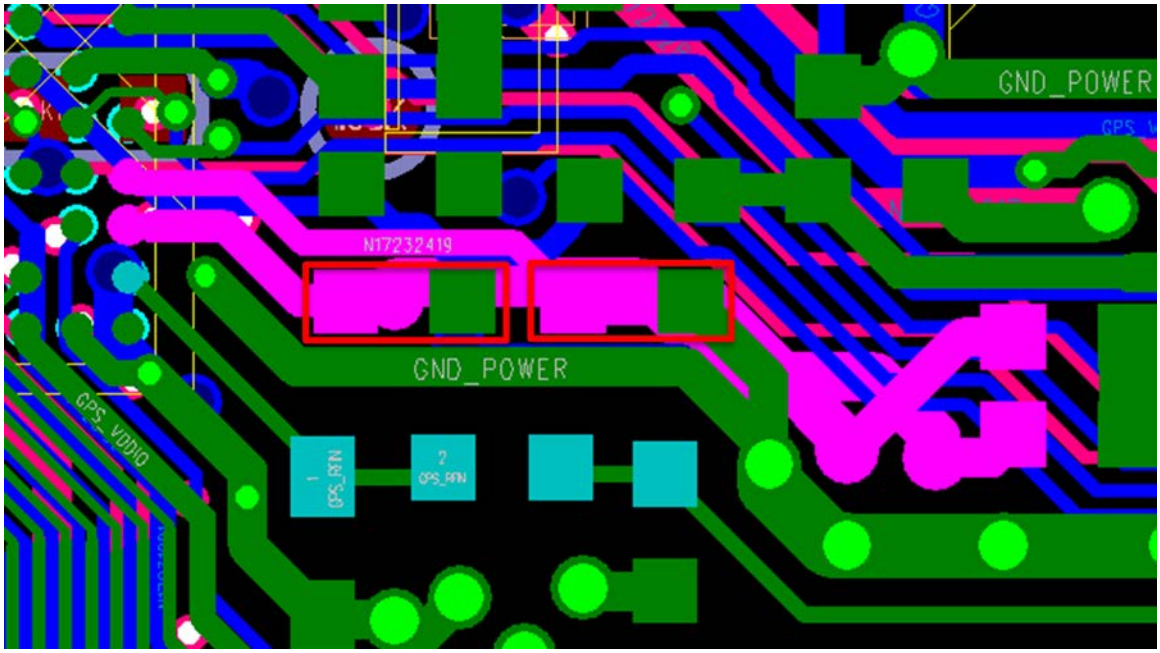

Figure 10. AVDD18_RXFE/AVDD18_CM pins for bypass capacitors

All bypass capacitors should be placed near the input and output pins of built-in LDOs, as shown in Figure 11.

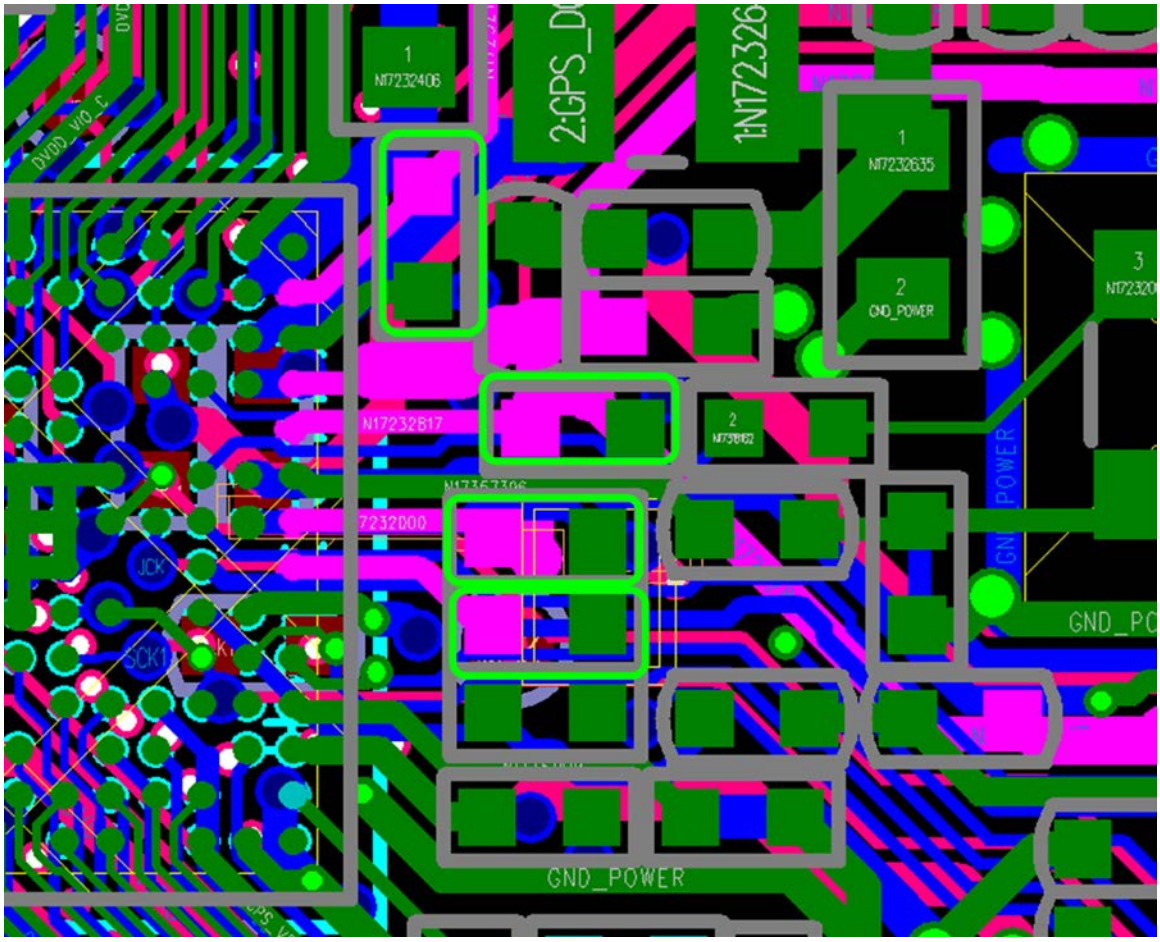

Figure 11. The built-in LDO bypass capacitor placement

4.2. Bluetooth/Bluetooth Low Energy layout guide

This section provides detailed description to design an efficient Bluetooth device. The details on net or pin locations are shown below.

1) Make the decoupling capacitors C5001 and C5002 close to the IC as short as possible with enough ground vias. The power rail should be routed to the completed ground plane for noise reduction. It also cannot overlap with crystal oscillator's signals, 26MHz clock signal and other digital signal traces. Figure 12 shows

how to power up the capacitors and Figure 13 shows the capacitors placed near the IC.

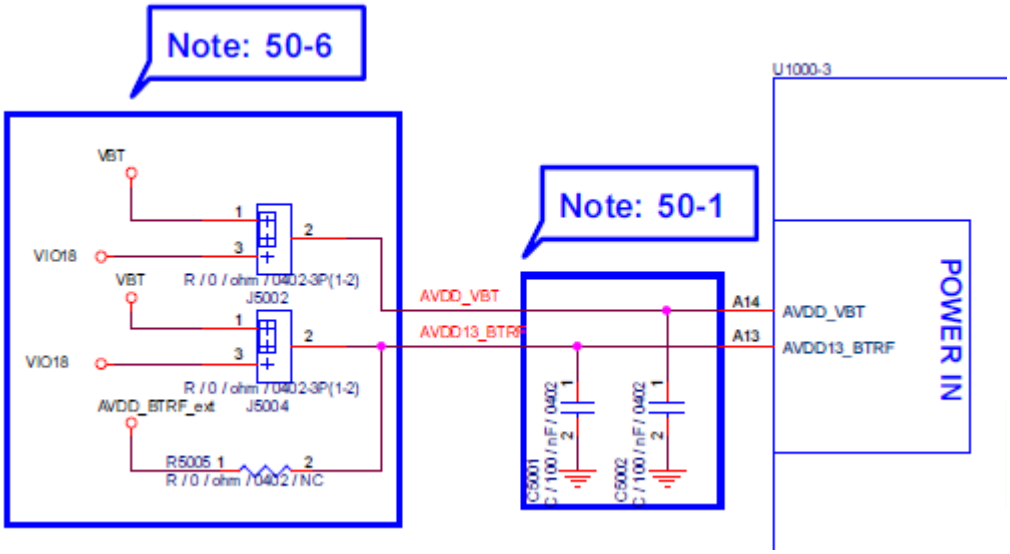

Figure 12. The decoupling capacitors for Bluetooth support

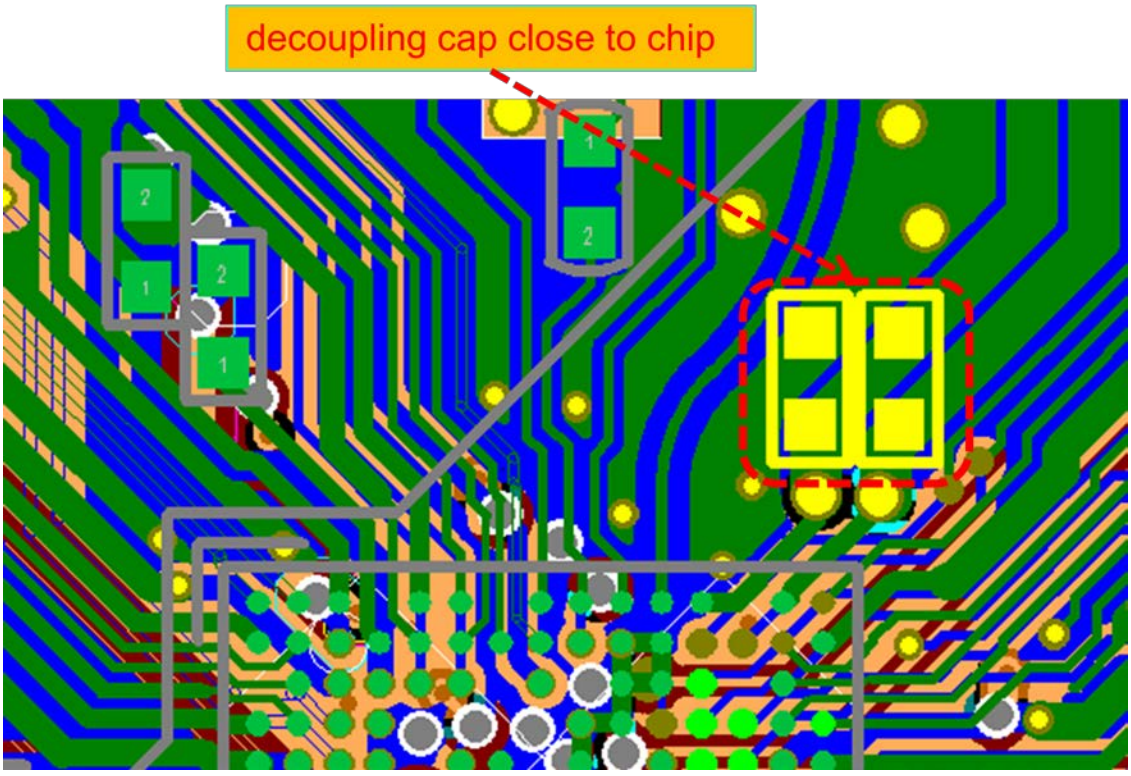

Figure 13. The decoupling capacitors placement on the PCB

2) LinkIt 2523 HDK's Bluetooth support has integrated match filters, so there is no need to reserve any other component except a π shape net for antenna matching, the net is shown in Figure 14 and Figure 15 for schematic and layout routing. Keep 50Ω impedance with tolerance of 10% offset.

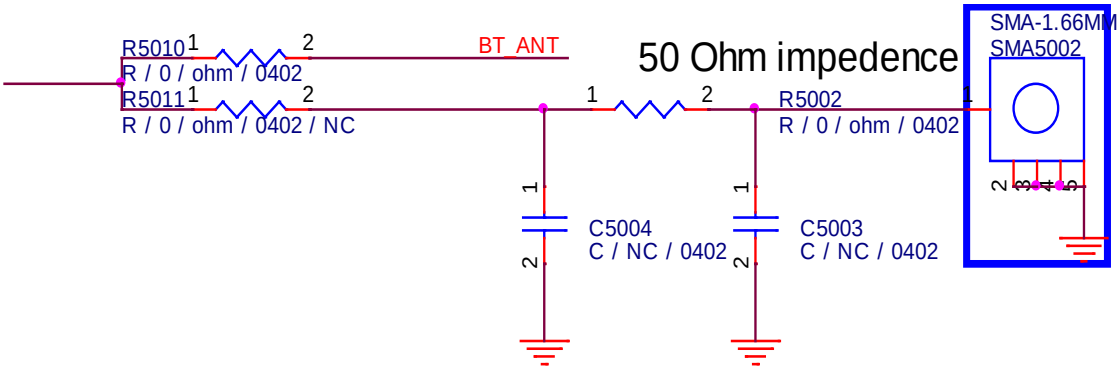

Figure 14. The π shape for antenna matching

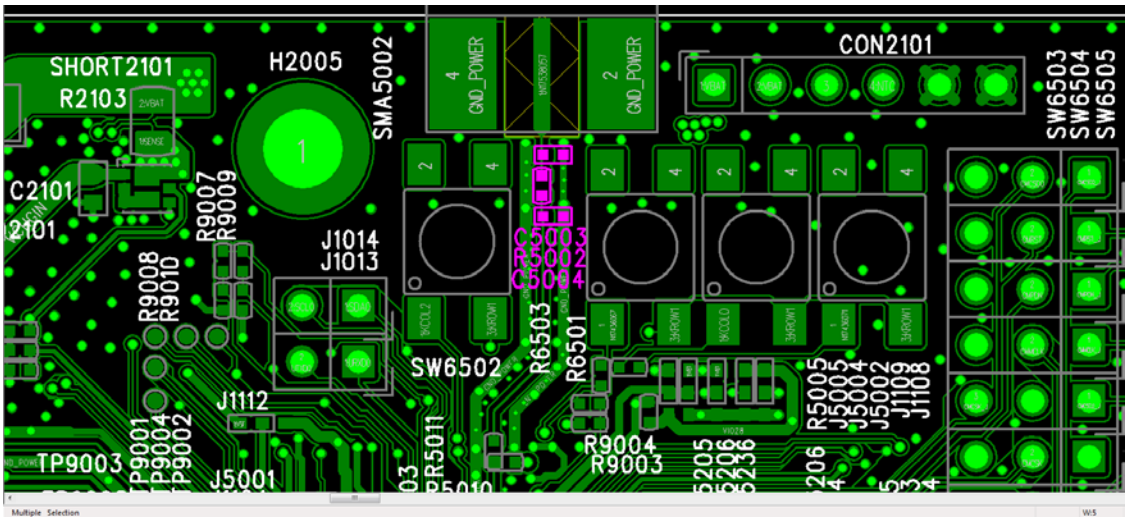

Figure 15. The matching adjustment placement on PCB

3) The 26MHz crystal oscillator should be placed as close as possible to the IC. If there are only two layers in your PCB design, the crystal oscillator can be placed on the Layer 1 and the Layer 2 will still be covered with copper.

4) For a four layer PCB design:

   a) Place the crystal oscillator on Layer 1 and the matching position on Layer 2 should be either empty or at least not covered with copper.

   b) Layer 4 should be covered with copper for reference ground.

   The crystal oscillator's ground pad cannot be connected to the main ground directly. First, the ground pads are connected with a trace then to the ground. The resistance creates extra heat and noise making it impossible to connect the crystal directly. This approach is useful to lessen the thermal impact.

For 4 layer PCB design, the Layer 1 and Layer 2 shouldn't be covered with copper, as shown in Figure 16.

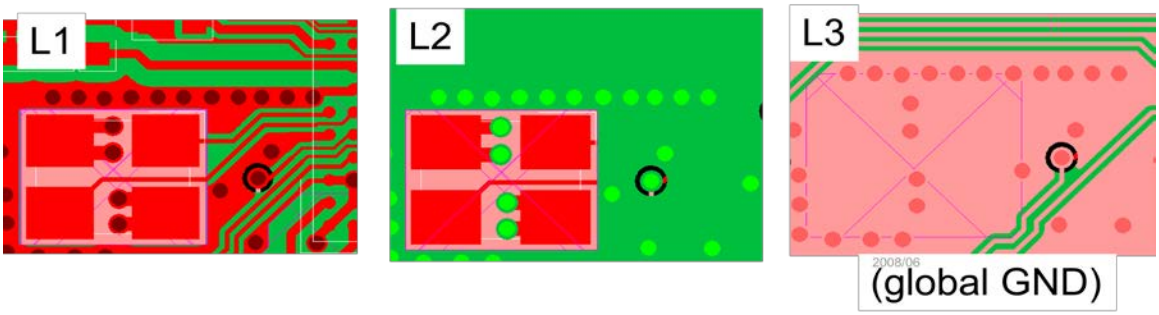

Figure 16. The 26MHz crystal oscillator keep-out routing in multiple layers

5) Add ground vias between the Bluetooth antenna trace and crystal oscillator for signal isolation and for noise reduction. The ground vias are close to the RF trace to reduce other signal impact, as shown in Figure 17.

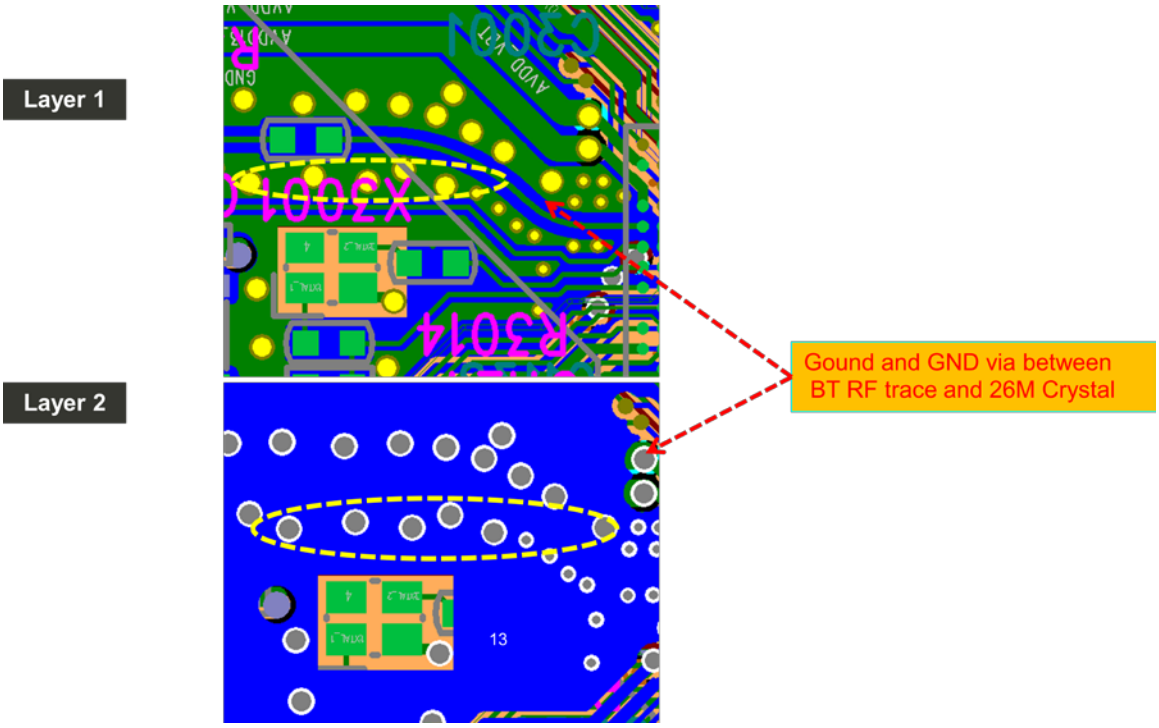

Figure 17. The ground vias between crystal oscillator and antenna trace

6) The line width and ground layer reference for RF traces should be kept close to 50Ω line for better impedance control. All RF traces should be connected to single complete ground plane to preserve better signal quality. The RF trace cannot overlap with the crystal oscillator's signal, 26 MHz clock signal and other digital signal traces. The RF trace is routed to Layer 1, as shown in Figure 18. The Layer 2 is the

reference ground plane completely covered with global ground.

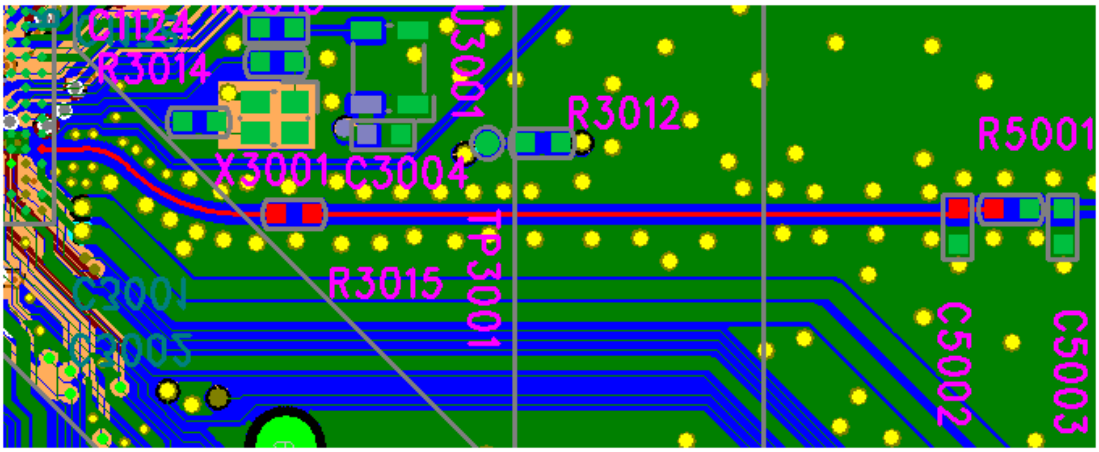

Figure 18. RF trace reference on the ground plane on Layer 2

5. Appendix A: Acronyms and Abbreviations

The acronyms and abbreviations used in this layout guide are listed in Table 4.

Table 4. Acronyms and abbreviations

Acronym	Description	Acronym	Description
UART	Universal Asynchronous Receiver/Transmitter	LCM	LCD (Liquid Crystal Display) Module
TCXO	Temperature Compensate crystal Oscillator	LDO	Low dropout regulator
I2S	Integrated Inter-chip Sound	RTC	Real Time Counter
GPIO	General Purpose I/O	HDK	Hardware Development Kit
USB	Universal Serial Bus	GPS	Global Positioning System
GNSS	Global Navigation Satellite System	PCB	Printed circuit board
SPI	Serial Peripheral Interface Bus	CLKO	Clock out
ADC	Analog-to-Digital Converter	PCM	Pulse-code modulation
CMSIS-DAP	ARM Cortex Microcontroller Software Interface Standard Debug Access Port	Prepreg	A pre-impregnated fabric.
JTAG	Joint Test Action Group		