USB3300

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB3300. These checklist items should be followed when utilizing the USB3300 in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 7. Detailed information on these subjects can be found in the corresponding section:

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The USB3300 implementor should have the following documents on hand:

- *USB3300 Data Sheet*
- *AN19.17 ULPI Design Guide*
- *AN18.15 PCB Design Guidelines for QFN and DQFN Packages*
- *AN26.21 USB Device Design Checklist*
- USB 2.0 Specification
- ULPI Specification

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground flag, **GND**, must be connected to the solid ground plane on the board.
- **GND** is the only circuit ground. Other signals that are connected to the ground should not be relied upon to provide circuit ground.
- **GND** is also the main path for removing heat from the USB3300. It is therefore important that there are enough vias under the USB3300 connecting it to the ground and that those vias are evenly distributed.
- It is also important that the vias be plugged or vented in such a way as to prevent voids from forming in the solder connection. For details on this topic, see *AN18.15* and *AN26.21* application notes.

3.0 POWER

- USB3300 requires power at:
  - 3.3V for USB analog circuits on **VDD33** pins
  - 1.8V for internal digital circuits on **VDD18** pins
  - 1.8V for internal analog circuits on **VDDA18** pin
- USB3300 contains an internal voltage regulator at 1.8V, which can be enabled or disabled by the **REG_EN** input pin. This regulated 1.8V can be used for both **VDD18** and **VDDA18**.

- If the internal regulator is enabled, then **VDD18** and **VDDA18** must have 4.7 µF filter capacitors attached.
- If the internal regulator is disabled, then **VDD18** and **VDDA18** must be supplied from an external source.
- **VDD18** and **VDDA18** may not be used to supply power to other devices.

The power and ground connections are shown in Figure 3-1 and Figure 3-2.

FIGURE 3-1: POWER AND GROUND CONNECTIONS, INTERNAL REGULATION

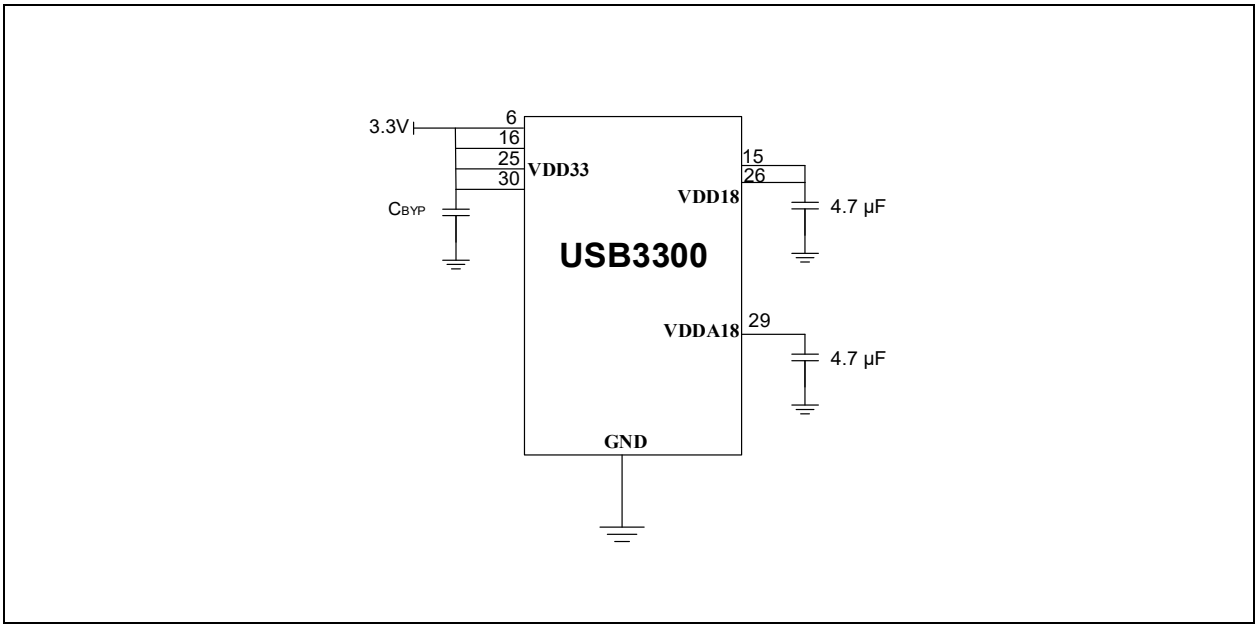
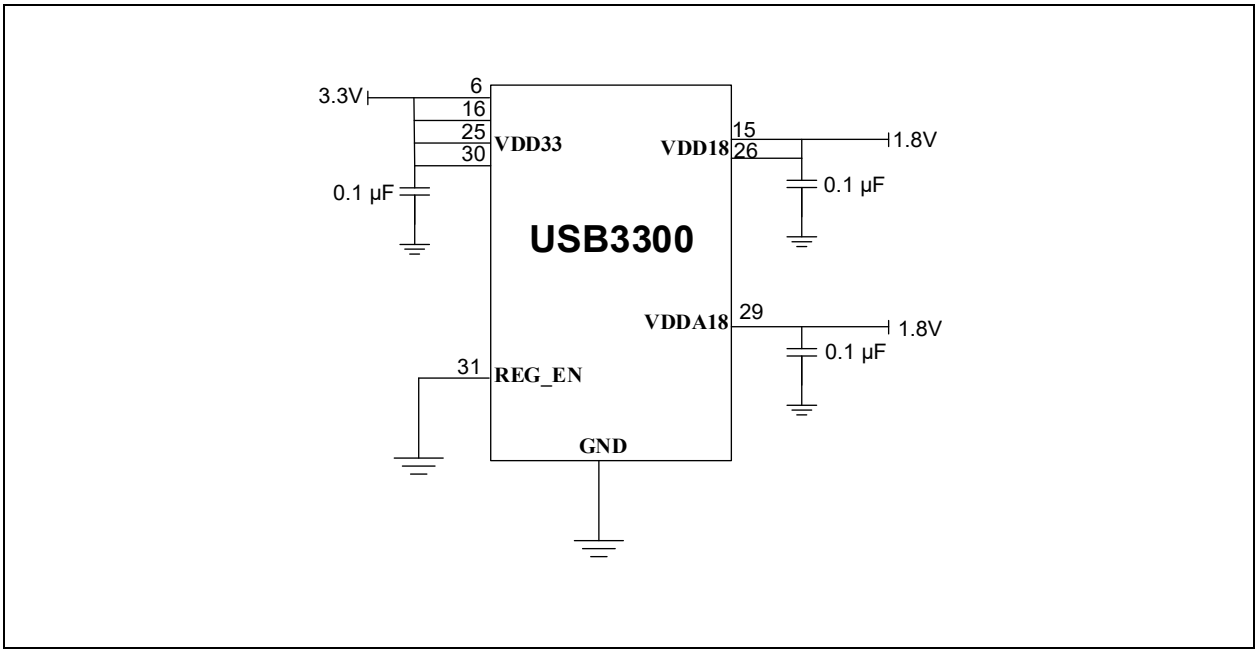


FIGURE 3-2: POWER AND GROUND CONNECTIONS, EXTERNAL REGULATION



4.0 USB

USB operation is defined by the USB 2.0 Specification. This specification may be obtained from USB Implementers Forum (USB-IF) at www.usb.org. USB3300 implementors should have a copy of the USB 2.0 Specification and should be familiar with its contents.

USB3300 can be used for the PHY level of a USB peripheral (device) or a USB host, or a USB On-The-Go (OTG) device (capable as either host or peripheral). The required behaviors of each is defined in the USB 2.0 Specification.

4.1 USB Signals

- **DP** (pin 7): This is the positive signal of the USB signal pair.
- **DM** (pin 8): This is the negative signal of the USB signal pair.
  - **DP** and **DM** signals should have controlled impedance. Control the single-ended characteristic impedance (Z0) of USB signals to between 40Ω and 55Ω. Control the differential impedance (Zdiff) of the DP/DM signals to 90Ω, +5/-10Ω.
- **VBUS** (pin 4): This is the VBUS signal. The USB3300 uses this pin for the VBUS comparator inputs and for VBUS pulsing during session request protocol.
  - R_{VBUS} may be installed in this configuration to assist in protecting the **VBUS** pin. 820Ω will protect against VBUS transients up to 8.5V; 10 KΩ will protect against transients up to 10V.
  - C_{VBUS} is a transient-suppressing capacitor that is required for USB 2.0 compliance. For a USB 2.0 host, C_{VBUS} should be 120 µF. For a USB 2.0 device, C_{VBUS} is 1 µF. C_{VBUS} should be located near the USB receptacle and nearer to the receptacle than R_{VBUS}.
- **ID** (pin 5): This is the ID input, used for USB On-The-Go (OTG) applications. In OTG applications, the ID pin is used to determine the type of USB cable that is connected.
  - When connected to a non-OTG device or an OTG B-Device, this pin floats and is pulled up by an internal resistor.
  - When connected to an OTG A-Device, the ID pin is pulled to the ground by the device.

FIGURE 4-1: USB CONNECTIONS IN A PERIPHERAL APPLICATION

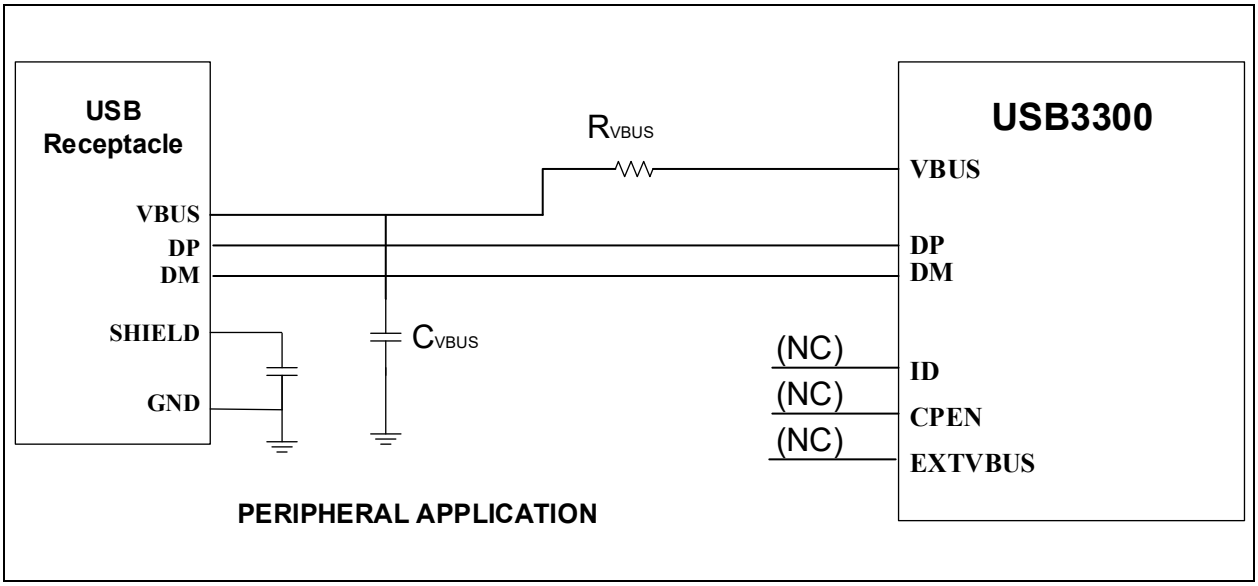
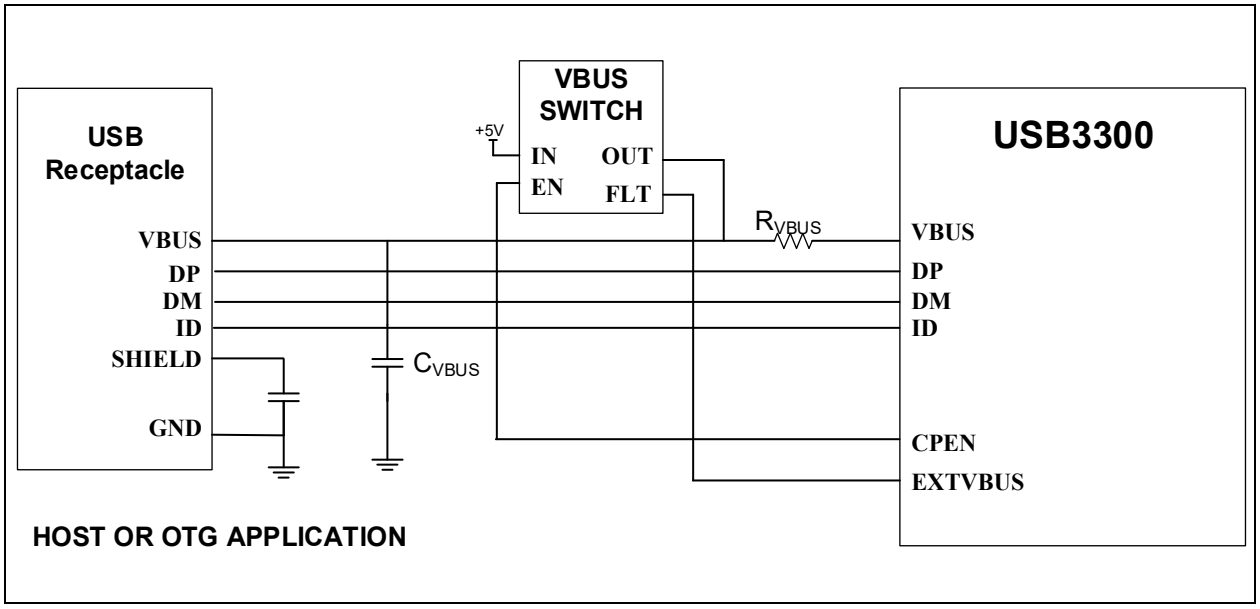


FIGURE 4-2: USB CONNECTIONS IN A HOST OR OTG APPLICATION



4.2 VBUS Switch

USB 2.0 host or OTG applications must be able to provide 5V on VBUS to supply power to USB devices that are attached. The current requirement varies considerably. The USB 2.0 Specification should be consulted for a complete explanation of the VBUS power requirements:

- 100 mA is required for all devices at connection and for low-power bus powered devices.
- 500 mA is required for high-power bus powered devices.
- As much as 5A total may be required for battery charging and other device circuits.

USB3300 supports these requirements by means of an external 5V switch. The VBUS switch connects a 5V supply to VBUS under ULPI register instruction and can detect the current that is supplied through VBUS.

The switch is controlled by the CPEN signal from the USB3300. The state of CPEN is determined by ULPI registers.

The switch should feature current detection. Current over the limit determined by the switch causes the FLGT signal to be asserted that is detected by the USB3300 on the EXTVBUS pin. To be compliant with the USB 2.0 Specification, the current limit must be no more than 5A.

Factors to consider in selecting a VBUS switch include:

- The current rating of the switch, the current at which the switch asserts the FTL signal, and the amount of current the system is required to provide
- The capability of the switch to provide protection from reverse currents in the On and Off states

The *USB3300 Data Sheet* contains additional detail regarding the operation of an external VBUS switch by the USB3300.

4.3 ESD and EMI

The use of external components (diodes, capacitors, and inductors) applied to USB signals is not generally recommended unless there is a specific need for such protection. Such components tend to make USB-IF compliance tests more difficult to pass, which can add time and cost to a project. At the same time, USB3300 is tolerant of protection devices that have been designed specifically for USB 2.0 signal application, and which are guaranteed compliant by their manufacturers.

5.0 CLOCK CIRCUIT

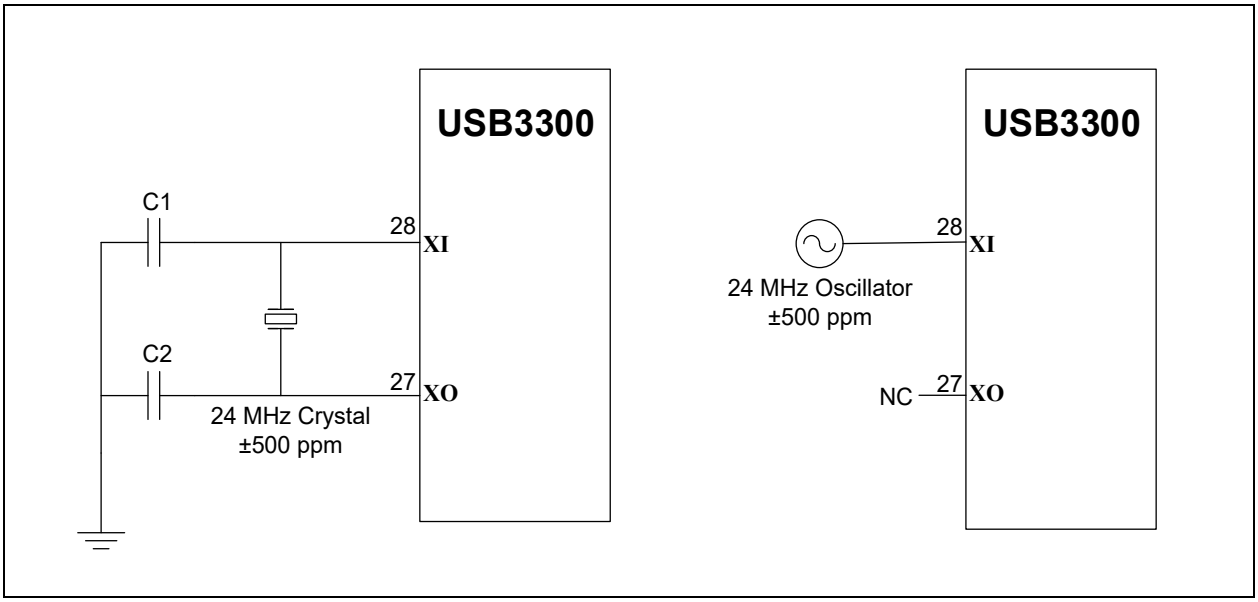
5.1 Crystal and External Clock Connection

A 24.000 MHz (±500 ppm) crystal should be used to provide the clock source. For the complete crystal specifications and tolerances, refer to the *USB3300 Data Sheet*. The crystal should be rated for a drive level of at least 500 µW.

- **XI** (pin 15) is the clock circuit input for the USB3300. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XO** (pin 14) is the clock circuit output for the USB3300. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system-dependent, based on the C_L spec of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.

Alternatively, a 24.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the USB3300. When using a single-ended clock source, **XO** (pin 27) should not be connected (NC).

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS



6.0 ULPI INTERFACE

- The ULPI interface connects the PHY layer (USB3300) to the LINK layer. The LINK layer consists of an ASIC, FPGA, or other SOC combined with the LINK layer firmware.The ULPI interface is a single-ended, bidirectional bus that operates at 60 MHz.

TABLE 6-1: ULPI SIGNALS

ULPI Signal	Description
DATA[7:0]	Bidirectional data signals
STP	Input from the link layer
DIR	Output to the link layer
NXT	Output to the link layer

- The ULPI interface is intended to cover short distances between integrated circuits on the same PCB. It is not expected to operate through connectors or a cable.
- ULPI DATA traces should be of similar length, although precisely equal lengths are not required.
- ULPI traces should not have stubs or components to V_{CC} or ground (such as capacitors).
- ULPI operation is covered in the *USB3300 Data Sheet* and in *AN19.17* application note.

7.0 STARTUP

7.1 Reset Circuit

The **RESET** pin is an active-high transceiver reset. The use of the RESET pin is optional. A logical high on the RESET pin is the same as a write to the Reset bit of the Function Control Register, address 04h, bit5. This does not reset the ULPI register set. This pin includes an integrated pull-down resistor to the ground. If not used, this pin can be floated but connecting the pin to the ground is recommended. If RESET is driven high from an external source, the logical high must last for at least one full cycle of the CLKOUT signal. No other PHY digital input signals may change state for two CLKOUT clock cycles after the negation of the RESET signal.

8.0 MISCELLANEOUS

8.1 RBIAS Resistor

The **RBIAS** pin on the USB3300 must connect to the ground through a 12 KΩ resistor with a tolerance of 1.0%. This is essential to the correct setup of critical bias currents.

8.2 Connector Selection

The normal connector type selection is based on the role of the USB3300.

- For a host, a Type-A receptacle is used.
- For a device, a Type-B, Mini-B, or Micro-B receptacle is used.

For USB 2.0 Specification compliance, the designer should select a USB receptacle to which the USB Integrators Forum has assigned a Test Certification ID (TID). TID numbers that exist for connectors are listed at https://usb.org/products.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
Section 3.0, "Power"	Section 3.0, "Power"	Each VDD33 pin is supplied between 3.0V and 3.6V.		
		For **REG_EN** high, 4.7 µF is present on **VDD18** and **VDDA18**.		
		For **REG_EN** low, 0.1 µF is present on **VDD18** and **VDDA18**.		
		For **REG_EN** low, each **VDD18** and **VDDA18** pin is supplied at 1.8V.		
		VDD18 or **VDDA18** is not connected to other devices.		
Section 4.0, "USB"	Section 4.0, "USB"	A copy of the USB 2.0 Specification has been downloaded from www.usb.org.		
	Section 4.1, "USB Signals"	**DP** and **DM** are routed with differential impedance of 90Ω.		
		DP and **DM** are routed with single-ended impedance of 40Ω - 55Ω.		
		VBUS is connected to CVBUS of 120 µF if host, otherwise 1 µF. CVBUS is located near the USB receptacle.		
		VBUS is connected with optional RVBUS no greater than 820Ω.		
		For host, **ID** pin is connected to the receptacle.		
	Section 4.2, "VBUS Switch"	For host, **CPEN** and **EXTVBUS** are connected to the VBUS switch as per Figure 4-2.		
		A VBUS switch has been selected according to system requirements.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Clock Connection"	For the internal oscillator, the crystal is rated 500 µW or greater.		
		For the internal oscillator, the crystal is 24.000 MHz ±500 ppm.		
		For internal oscillator, loading capacitors match the crystal manufacturer specification.		
		For the internal oscillator, the crystal or capacitor traces are short.		
		For the external oscillator, the frequency is 24.000 MHz ±500 ppm.		
		For the external oscillator, the signal amplitude is 0V to 3.3V (nominal).		
		For the external oscillator, **XO** is not connected.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "ULPI Interface"	Section 6.0, "ULPI Interface"	ULPI DATA signals are of similar length to the extent practical.		
		ULPI DATA signals have no stubbing (parallel) components connected.		
		No ULPI signal is connected to a header or external connection.		
		ULPI DATA signals do not traverse stubbing vias.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	If RESET is to be driven, the signal complies with the data sheet, Section 6.1.11.		
		If RESET is not to be driven, the signal is not connected or is connected to the ground.		
Section 8.0, "Miscellaneous"	Section 8.0, "Miscellaneous"	**RBIAS** resistor is 12 kΩ ±1.0%.		
		In layout, the ground flag is connected with at least nine vias in a square pattern.		
		In layout, gas blocking or venting techniques have been implemented in the ground flag vias.		
		In layout, the guidance of *AN26.21* and *AN18.15* have been followed.		
		The USB receptacle has a TID assigned.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002886A (12-14-18)	Initial release	

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