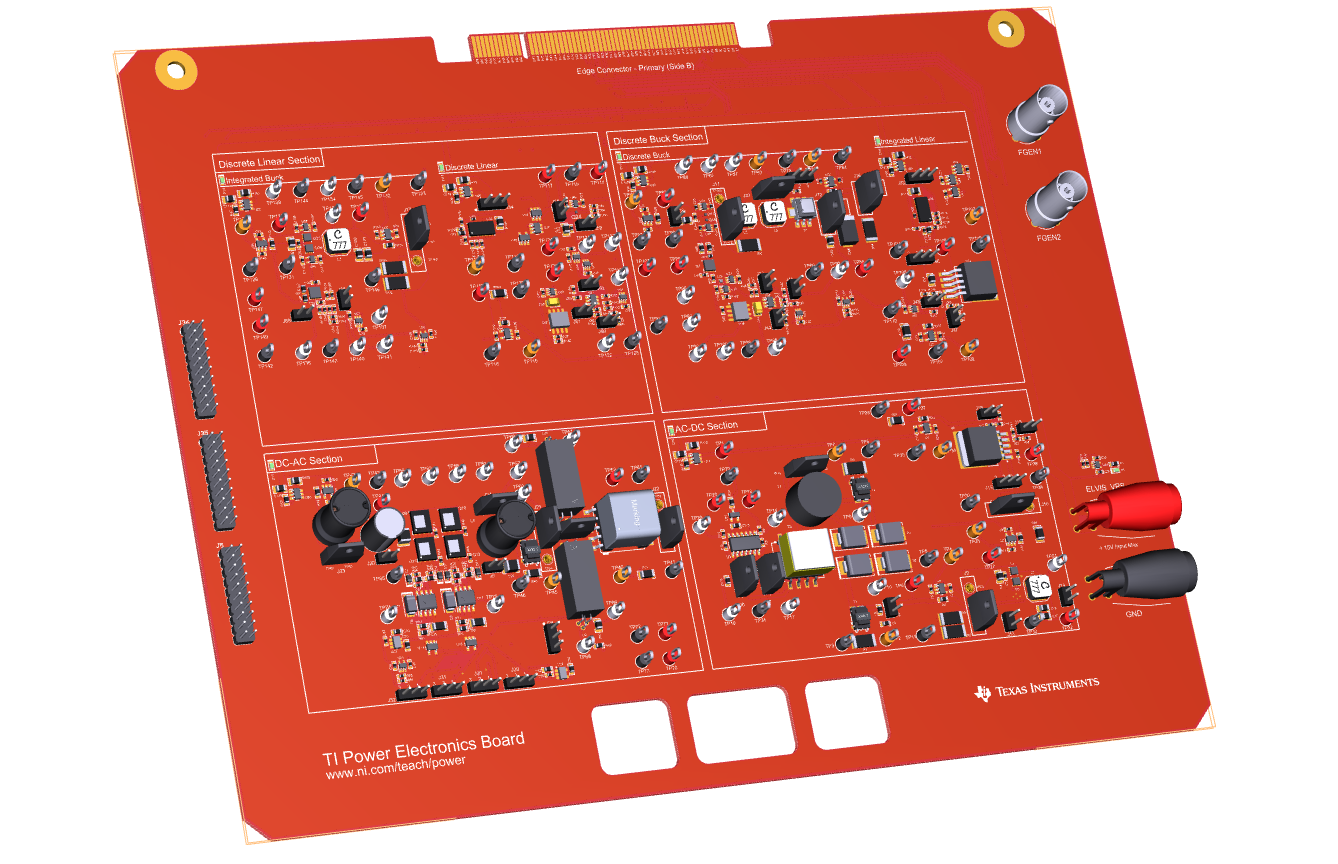


Lab Manual: Power Electronics

Using the TI Power Electronics Board for NI ELVIS III



by Nicola Femia

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# *"There is nothing more practical than a good theory."*

James C. Maxwell (1831-1879)

*About the Author*

Nicola Femia is Professor of Power Electronics at the University of Salerno, Italy, where he has founded the Power Electronics Research Group and the Power Electronics and Renewable Sources Laboratory. He is co-author of more than 180 scientific papers, one book and five patents. He has developed over 25 university and industry research projects on power electronics topics, and held over 50 invited lectures, courses and seminars on Power Electronics Design and Education in universities and industries over Europe, United States, China and India. In 2014 he has been Visiting Professor at the Electrical Engineering Department of Stanford University, Stanford, CA.

# Introduction

This manual provides a guidance to a comprehensive hands-on learning experience on fundamentals of Power Electronics, tailored for Electrical Engineering and Electrical and Computer Engineering Undergraduate Programs. The education vision implemented in the laboratories anthology collected in the manual is founded on the intent of stimulating investigation and understanding capabilities of students, beyond the learning of technical topics. Problem-oriented theoretical models, circuit simulations and experimental tests are the ingredients of each laboratory, focusing on topics of wide interest in real world power electronics applications. The laboratories are inspired by the following key ideas:

1. whatever technical problem you need to solve regarding a physical device, circuit or system, there is always a good simplified theoretical model providing the key information, about what are the physical and functional factors majorly impacting the features of interest to the problem under investigation;
2. circuit simulators allow to implement models of different level of complexity to emulate the behavior of real devices, circuits and system, and help exploring their operability limits and observing the impact of model parameters and functional configurations on the resulting performances;
3. hands-on experimental tests and measurements are essential to validate and improve theoretical models, while understanding the impact of real physical parameters and functional features on the feasibility of targeted performance and reliability of devices, circuits and systems.

The combination of theory, simulations and experiments proposed in each laboratory engages the student into a virtuous learning loop, rich of observations and assessments, ending with a clear vision of a problem and of methods and tools to solve it. The laboratories, indeed, stimulate the students to interleave calculations, simulations and measurements, while changing model parameters based on observations of results, thus converging toward the improvement of models and the achievement of a desired real world behavior.

The laboratories are connected each other, forming four groups, which cover the fundamentals of DC-DC linear regulators, DC-DC buck regulators, DC-AC inverters, and AC-DC rectifiers. Each group of laboratories is performed by means of dedicated Multisim Live circuit schematics for simulations, and a dedicated section of the TI Power Electronics Board for experimental measurements. Although each lab is self-consistent, performing the entire sequence of laboratories dedicated to a given topology boosts the understanding of concepts and the achievement of a system level vision.

An important concept underlies the labs conception: power electronic circuits are systems made of single interconnected elements, conceived and configured to perform specific functional tasks and coordinated each other, to implement specified system features. Accordingly, the groups of laboratories from LAB1 to LAB4 and from LAB5 to LAB8 present and discuss a logical sequence of concepts and topics that guide the students step-by-step in understanding the transition from elements to systems, and from functions to features.

The four groups of labs offer also an opportunity to students to understand the manifold utilizations of a given device or concept over power electronics applications, to achieve different practical goals, or the same goal in different ways. This can be achieved, for example, trough laboratories from LAB1 to LAB8, discussing the utilization of power MOSFETs either as variable resistors or as switches, to perform voltage regulation in linear and switching regulators, respectively, and trough laboratories from LAB5 to LAB10, showing the utilization of pulse width modulation in DC-DC and DC-AC regulators, respectively. Crossed references of labs each other are included in the manual to highlight these connections.

The brief theory overview introducing each lab summarizes the main facts of interest to the topic under investigation, including simplified models tailored to the specific problem to be analyzed and solved. Passing from a lab to the next one, the student learns that different simplified models can be used to represent a given device or system under different operating conditions. Students can use the models proposed in the labs theory overview, or they can replace them with the models discussed by instructors in the specific curriculum classes they teach.

This manual does not provide design rules and methodologies: indeed, the topics and the tools discussed throughout the labs intend to help students in achieving a good understanding of the operation of power electronics fundamental bricks, thus preparing them to better assimilate the design topics taught by instructors in their classes.

Suggestions on possible expansion activities are also provided, to stimulate the exploration of further interesting aspects beyond the specific case studies discussed in each lab. Indeed, the anthology of labs proposed in the manual can be easily personalized and extended by instructors, also to cover topics regarding power semiconductors, magnetics, circuit theory, analog electronics, and control theory. Many test points and jumpers are available for this purpose in the TI Power Electronics Board, allowing to observe voltages and currents and to change the circuit configuration setup.

## Learning Objectives

After completing the labs in this manual, you should have the ability to complete the following actions.

1. given a linear regulator, with specified components characteristics, you will be able to analyze and predict its behavior, under DC and AC operating conditions, in open-loop and closed-loop operation, by determining the values of voltages and currents of interest to evaluate static and dynamic performances, with specified units and accuracy;
2. given a buck regulator, with specified components characteristics, you will be able to analyze and predict its behavior, under DC and AC operating conditions, in open-loop and closed-loop operation, in continuous and discontinuous mode, by determining the values of voltages and currents of interest to evaluate the static and dynamic performances, with specified units and accuracy;
3. given a DC-AC pulse width modulated inverter, with specified components characteristics and modulation signals, you will be able to analyze and predict its behavior, under different load impedance conditions, by determining the amplitude of output current and voltage AC components, with specified units and accuracy:
4. given a high-frequency transformer and a square-wave inverter, with specified components characteristics and modulation signals, you will be able to analyze and predict its behavior, under different coils configurations, by determining the amplitude of input and output current and voltage AC components, with specified units and accuracy;
5. given an AC-DC rectifier, with specified components characteristics, you will be able to analyze and predict its behavior, under different input inductance and output capacitance conditions, by determining the amplitude of output current and voltage DC and AC components, with specified units and accuracy;
6. given a system comprises of a AC-DC rectifier with buck and linear post-regulators, with specified characteristics, you will be able to analyze and predict the behavior of the system, under different operating conditions, by determining the amplitude of input and output current and voltage DC and AC components of each stage, with specified units and accuracy.

### Prerequisites

This lab manual was designed for students who have completed the following courses and have a working knowledge of the following hardware, software, and tools.

### Completed Courses

1. *Introduction to Circuits*, or equivalent
2. *Semiconductor Devices*, or equivalent
3. *Introduction to Analog Electronics*, or equivalent

### Hardware, Software, and Tool Knowledge

1. Oscilloscope
2. Scientific Calculator

## Organization of the Lab Manual

The manual is organized as a sequence of twelve labs, regarding four different power electronic topologies:

### 1-Linear Regulator

The four labs from Lab1 to Lab4 are dedicated to the linear regulator, focusing on the following topics:

### Lab1: Linear Regulator in Open Loop DC Operation

The lab investigates the DC operation of a MOSFET as linear regulator, and the relationships among physical parameters and electrical variables determining the DC operating point

### Lab2: Linear Regulator in Open Loop AC Operation

The lab investigates the AC operation of a MOSFET as linear regulator, and the relationships among physical parameters and electrical variables determining the effect of AC source perturbations on the output voltage

### Lab3: Error Amplifier Operation

The lab investigates the operation of an error amplifier as feedback element, and the relationships among output voltage perturbations and the signal controlling the MOSFET gate drive voltage

### Lab4: Linear Regulator in Closed Loop Operation

The lab investigates the impact of the closed loop feedback control on the capability of the linear regulator of maintaining the output voltage well regulated under DC and AC operating conditions, rejecting the source perturbations.

### 2-Buck Regulator

The four labs from Lab5 to Lab8 are dedicated to the buck regulator, focusing on the following topics:

### Lab5: Buck Regulator Half-Bridge PWM Operation

The lab investigates the operation MOSFETs as switches, implementing the half-bridge used in buck regulator to convert a given DC input voltage into a lower DC output voltage

### Lab6: Buck Regulator L-C Filter Operation

The lab investigates the operation of the L-C filter used to remove the high-frequency AC component generated by the MOSFET half-bridge of a buck regulator, and the relationships among physical and operating parameters determining the amplitude of AC ripple components of current and voltage.

### Lab7: Buck Regulator in Discontinuous Mode Operation

The lab investigates the impact of a MOSFET-diode half-bridge on the operation of a buck regulator, and the relationships among physical and operating parameters determining the amplitude of AC ripple components of current and voltage and the voltage conversion ratio.

### Lab8: Buck Regulator in Closed Loop Operation

The lab investigates the impact of the closed loop feedback control on the capability of the buck regulator of maintaining the output voltage well regulated under DC and AC operating conditions, rejecting the load perturbations.

### 3-DC-AC Inverter

Lab9 and Lab10 are dedicated to the single-phase DC-AC inverter and to the high-frequency transformer, focusing on the following topics:

### Lab9: DC-AC PWM Inverter Operation

The lab investigates the operation of a MOSFETs full-bridge, driven by a sinusoidal pulsed width modulation, under different load impedance conditions, and the relationships among physical parameters and operating conditions determining the amplitude of output current and voltage AC components.

### Lab10: High-Frequency Transformer Operation

The lab investigates the operation of a high-frequency transformer under square-wave voltage generated by a MOSFET full-bridge DC-AC inverter, , and the relationships among physical parameters and operating conditions determining the output current and voltage and the amplitude of magnetizing current, under different coils configurations.

### 4-AC-DC Rectifier

Lab11 and Lab12 are dedicated to the single-phase AC-DC rectifier, focusing on the following topics:

### Lab11: AC-DC Rectifier Operation

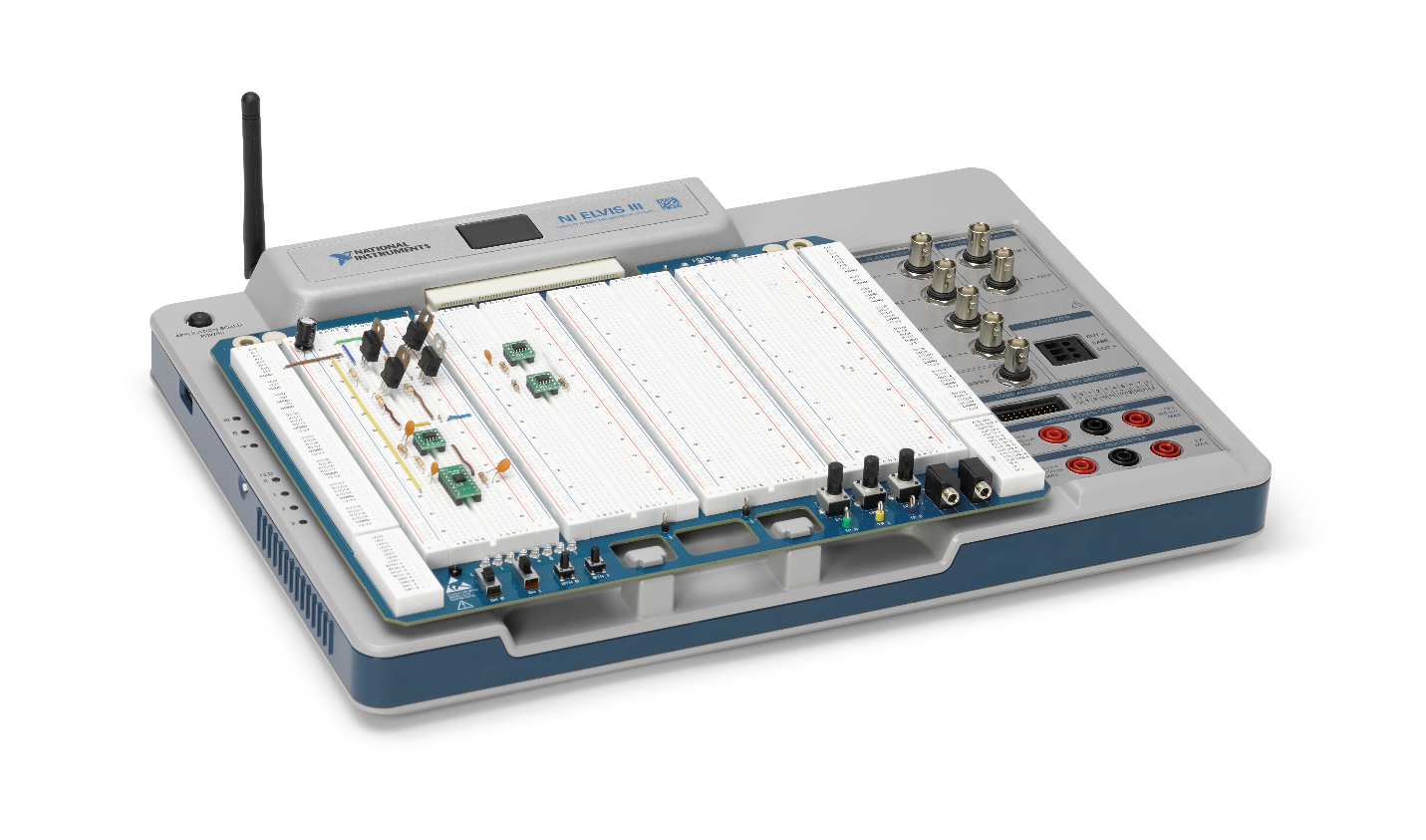
The lab investigates the operation of a single-phase diode full-bridge rectifier, under different input inductance and output capacitance conditions, and the relationships among physical parameters and operating conditions determining the amplitude of output voltage AC component.

### Lab12: Post Regulators

The lab investigates the operation of a system comprised of an AC-DC diode rectifier with a cascade of buck and linear post-regulators, and the relationships among physical parameters and operating conditions determining the behavior of the system and the amplitude of input and output current and voltage DC and AC components of each stage.

## Lab Tools and Technology

### Platform: NI ELVIS III

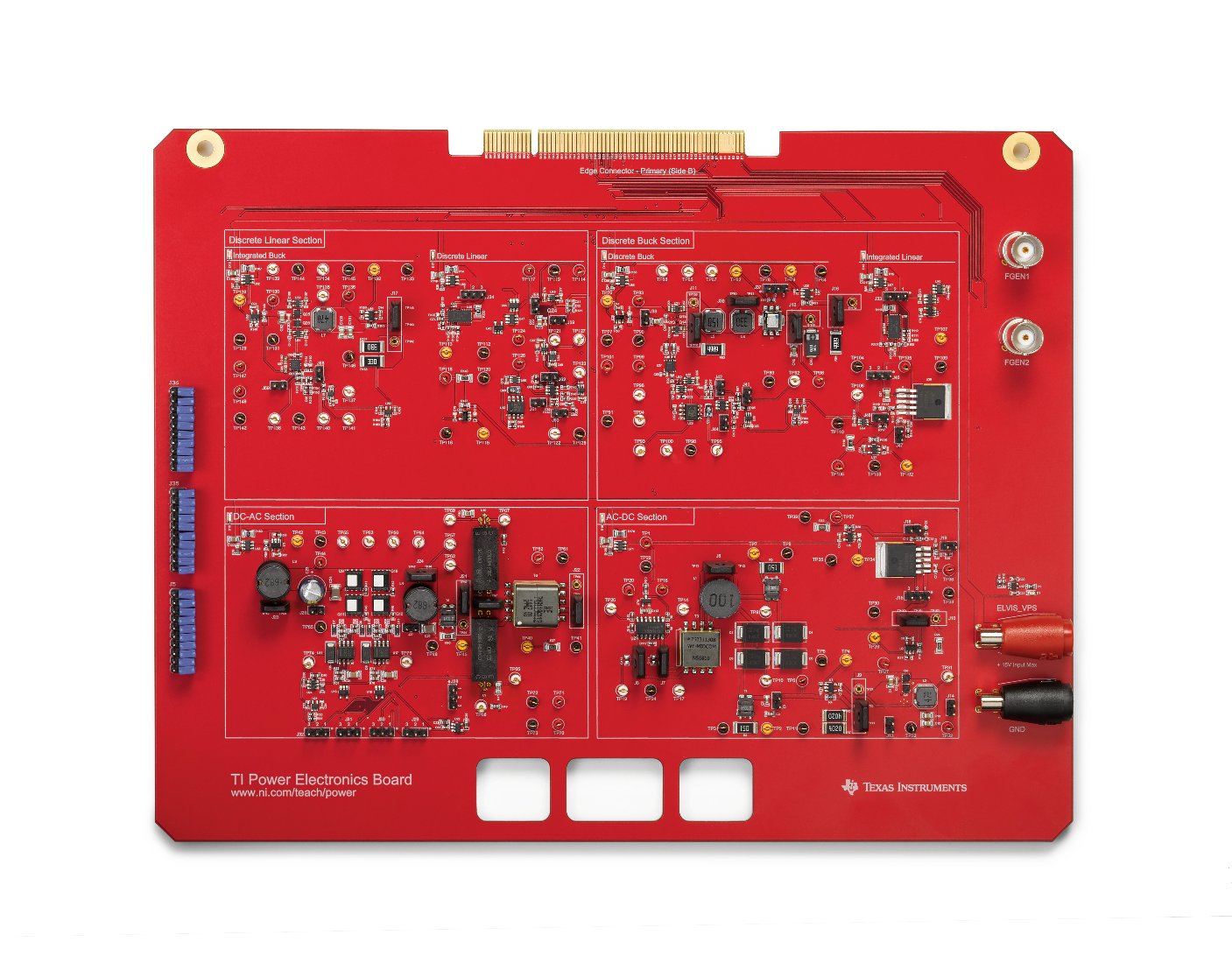


The NI Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) is an engineering laboratory solution for project-based learning that combines instrumentation and embedded design with a web-driven experience to create an active learning environment in the lab and studio and flipped classrooms, delivering a greater understanding of engineering fundamentals and system design. NI ELVIS addresses engineering curriculum by integrating project-based learning, teamwork, and design with course-specific application boards and labs developed by experts from education and industry. NI ELVIS, as a programmable platform, gives educators the ability to scale to future multidisciplinary applications driving student employability.

**

Learn more at [http://www.ni.com/en-us/support/model.ni-elvis-iii.html](http://www.ni.com/en-us/support/model.ni-elvis-iii.html%20)

### Hardware: TI Power Electronics Board



The TI Power Electronics Board is an application board for NI ELVIS III which provides a hands-on platform for learning power electronics and power management. Using functional blocks, students build their own buck converters, regulators, and both DC-AC and AD-DC converters. Students will gain an in-depth understanding of each component in a power electronics system and how it influences other components to create a cohesive system all while using industry-standard Texas Instruments circuits.



Learn more at <http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html>

### Software: Multisim Live



Multisim Live brings SPICE simulation to you anywhere, anytime with an interactive, online, touch-optimized environment that works on any device. With a database of over 30,000 community circuits, engineers, students, and makers can immediately turn inspiration into simulation.



Learn more at https://www.multisim.com/

# Lab 1: Linear Regulator in Open Loop DC Operation

The goal of this lab is to investigate the properties of a MOSFET in DC operation, when it works as a pass device in linear regulators. First, we review the equations describing the behavior of a MOSFET in DC operation, and discuss the impact of the gate-to-source voltage on the operating point. Next, we predict the MOSFET operating region and calculate the power losses and temperature under different conditions. Then, we simulate the MOSFET using its physical model. Finally, we perform lab experiments to estimate the real value of MOSFET parameters and compare their impact on the accuracy of theoretical and simulation predictions.

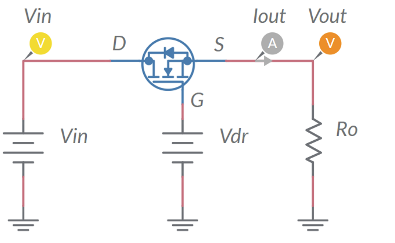


Figure 1-1. Linear Regulator

## Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given the parameters of a MOSFET, a source voltage and a load resistance, you will calculate the gate driver voltage required to achieve a desired output voltage, you will determine the MOSFET operating region and calculate its drain-to-source voltage and current, power losses and junction temperature, with specified units and accuracy, by applying the appropriate MOSFET equations
2. Given the parameters of a MOSFET, a source voltage, and a load resistance, you will determine the gate driver voltage required to achieve a desired output voltage by simulating the MOSFET operation, you will determine the MOSFET operating region and calculate its drain-to-source voltage and current, power losses and junction temperature, with specified units and accuracy, and you will determine the accuracy of theoretical predictions.
3. Given a real MOSFET, a DC power supply, a load resistor of given resistance, and a function generator, you will set experimentally the MOSFET gate driver voltage allowing to achieve a desired output voltage, you will record the measurement, with specified units and accuracy, you will compare the measured values with the simulations, and you will determine the accuracy of simulations.

## Required Tools and Technology

|  |  |
| --- | --- |
| Platform: NI ELVIS III Instruments used in this lab:   * Function generator * Digital multimeter * Oscilloscope * Power Supply   **Note**: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments. ​ | * Access Instruments   https://measurementslive.ni.com/   * View User Manual http://www.ni.com/en-us/support/model.ni-elvis-iii.html * View Tutorials   <youtube link> |
| Hardware: TI Power Electronics Board | * View User Manual   http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html |
| Software: NI Multisim Live | * Access   <https://www.multisim.com/>   * View Tutorial   https://www.multisim.com/get-started/ |
| Software: TI Power Electronics Configuration Utility | * Download (Windows OS Only)   http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip   * Note: Mac Version will be available soon |

## 

## Expected Deliverables

In this lab, you will collect the following deliverables:

* Calculations based on equations provided in the Theory and Background Section
* Results of circuit simulations performed by NI Multisim Live
* Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
* Observations and comparisons on simulations and experimental results
* Questions Answers

Your instructor may expect you to complete a lab report. Refer to your instructor for specific requirements or templates.

## 1 Theory and Background

1-1 Introduction

In this section, we review the fundamental concepts relevant to the operation of a MOSFET as a linear regulator. This important feature is utilized in a large variety of low-power applications, where a well-regulated DC voltage is required.

1-2 The linear regulator concept

Figure 1-2 shows a circuit composed of a voltage generator, *Vin*, a load resistor, *Ro*, and a variable resistor, *Rvar*.

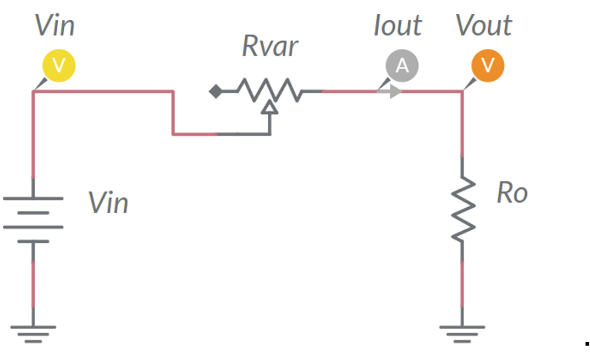


Figure 1-2. Resistive Voltage Divider

If the voltage *Vout* required by the load is lower than *Vin*, then the voltage drop across the variable resistor must equal the difference *Vin-Vout*. The value of the resistance *Rvar* required to achieve the desired load voltage *Vout*, is given by Equation 1-1:

*Equation 1-1* 

The resistance *Rvar* depends on the input voltage *Vin*, and on the load current, *Iout*: it must be adjusted to maintain the output voltage regulated at the desired value *Vout*, when *Vin* and *Iout* are subjected to time variations. This happens in many practical applications, where the source voltage *Vin* can be affected by disturbances (e.g. automotive power electronics) and the load can require a variable power (e.g. power signal amplifiers).

1-3 MOSFET operating as linear regulator

Figure 1-3 shows the basic circuit schematic of a linear regulator, using an N-channel MOSFET as a “pass device”.

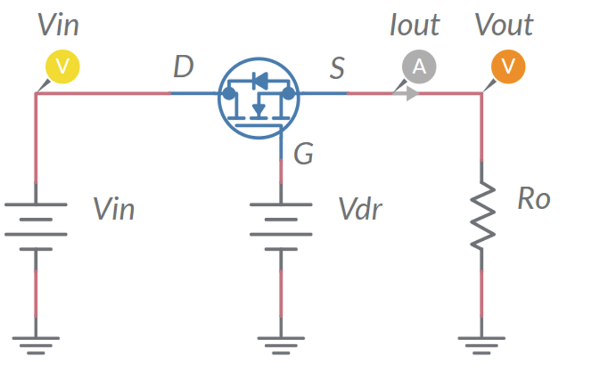
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Figure 1-3. MOSFET Operating as Linear Regulator

The linear regulator uses the MOSFET capability to emulate a variable resistor, whose resistance is driven by the gate-to-source voltage applied between the gate (G) and the source (S). The output voltage *Vout* can be regulated at the desired value by adjusting the gate-to-source voltage. The circuit driving the MOSFET gate-to-source voltage works as a source, providing a voltage *Vdr*. The voltage *Vdr* is applied to the gate terminal G and yields a gate-to-source voltage *VGS* = *VG* - *Vout* = *Vdr* - *Vout*. Equations 1-2 (also called MOSFET output characteristics) describe the MOSFET drain-to-source current in DC operation, as function of the drain-to-source voltage and gate-to-source voltage:

*Equations 1-2* 

*Vth* is the gate-to source threshold voltage, *β* is the trans-conductance coefficient, and *λ* is the channel-length modulation coefficient. Equations 1-2 highlight that, given the drain-to-source voltage *VDS*, the current *IDS* the MOSFET lets to pass from drain to source is determined by the gate-to-source voltage *VGS*. The operating point of the MOSFET is determined by the combination of its own characteristics with the source and load parameters.

1-4 MOSFET DC operating point

The grey lines in Figure 1-4 are the plots of Equations 1-2, parameterized with respect to the gate-to-source voltage. The red line in Figure 1-4 is the locus of operating points of the MOSFET determined while varying the gate-to-source voltage, given the source voltage *Vin* and the load resistance *Rload*, while the green line is locus of the MOSFET DC operating points allowed by a given gate-to-source voltage *VGS\**.

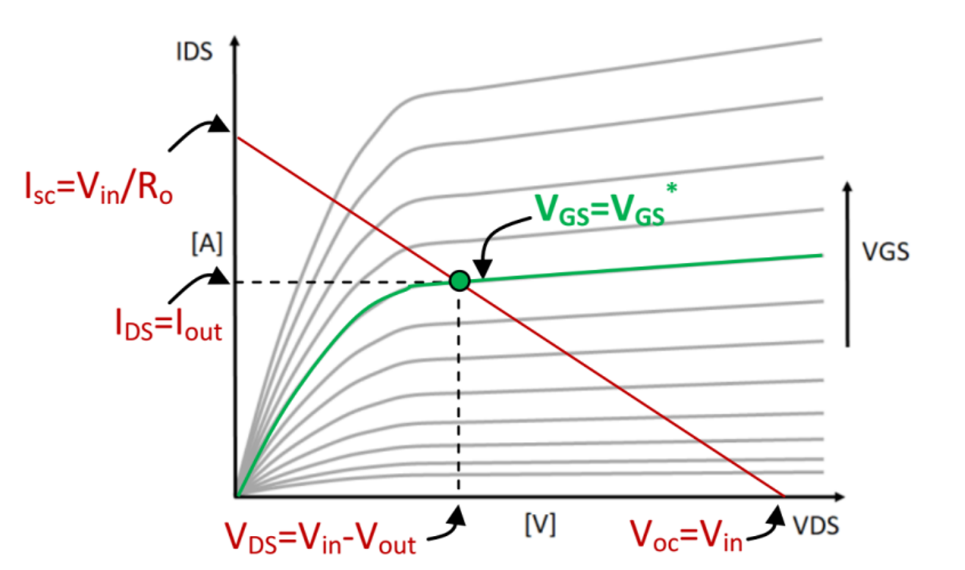


Figure 1-4. Determination of the MOSFET DC Operating Point.

The intersection of the red and green lines is the MOSFET DC operating point. It can be determined by means of the constraints given by Equations 1-3 to 1-5:

*Equation 1-3* 

*Equation 1-4* 

*Equation 1-5* 

Combining Equations 1-2 to 1-5 allows determining the gate driver voltage *Vdr*, given the input voltage *Vin*, the load resistance *Ro* and the desired output voltage *Vout*. Neglecting the minor impact of the channel-length modulation coefficient *λ* in DC operation yields the simplified Equations 1-6 and 1-7:

***saturation region*** *(the equations are valid if ):*

*Equation 1-6* 

***ohmic region*** *(the equations are valid if ):*

*Equation 1-7* 

The gate driver voltage *Vdr* required to achieve the desired output voltage *Vout* is independent of the input voltage *Vin* when *Vin* > *Vdr* - *Vth* (MOSFET operating in the saturation region), whereas it increases while the input voltage *Vin* decreases when *Vin* < *Vdr* - *Vth* (MOSFET operating in the ohmic region). Equations 1-6 and 1-7 highlight that a MOSFET with a higher *Vth* requires a higher driver voltage *Vdr* to achieve the desired output voltage *Vout*. The minimum input voltage *Vinmin* allowing the output voltage regulation is determined by the gate driver voltage rating *Vdrmax*. The difference *Vinmin – Vout* is the “dropout voltage” of the linear regulator. *Low Dropout Regulators* (LDO) are characterized by a small dropout voltage.

1-5 MOSFET thermal properties

The MOSFET can operate at a maximum junction temperature rating *Trating* of 150°C or 175°C, depending on its technology. Exceeding the maximum junction temperature may result in damage of the MOSFET and possible fault in the operation of the circuit where the MOSFET is used. The junction temperature depends on the MOSFET power loss, which can be calculated by means of Equation 1-8:

*Equation 1-8* 

Given the ambient temperature *Ta*, the MOSFET junction temperature *Tj* is given by Equation 1-9:

*Equation 1-9* 

The coefficient *R*θ*ja* is the thermal resistance of the MOSFET, determined by the package.

Check Your Understanding

*Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all “Check your Understanding” questions at the end of the lab.*

1-1 Given the source voltage and load resistance, how does the MOSFET drain-to-source **current change** as the gate driver voltage increases?

1. it increases
2. it decreases
3. it is not influenced

1-2 Given the source voltage and load resistance, how does the MOSFET drain-to-source **voltage change** as the gate driver voltage increases?

1. it increases
2. it decreases
3. it not influenced

1-3 Given the desired output voltage and load resistance, how does the required MOSFET gate driver voltage change while the input voltage decreases, if the MOSFET operates in the saturation region?

1. it increases
2. it decreases
3. it is not influenced

1-4 When does the MOSFET operate in the ohmic region as a linear regulator?

1. never
2. when the input voltage is much higher than the required output voltage
3. when the input voltage is a little higher than the required output voltage

1-5 Given the source voltage and load resistance, how does the MOSFET power loss change as the gate driver voltage increases?

1. increases
2. not influenced
3. non- monotonic

## 2 Exercise

The Texas Instruments CSD15380F3 (<http://www.ti.com/lit/ds/symlink/csd15380f3.pdf>) N-channel MOSFET Q1 used in the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III has the following nominal parameters:

* *Vth* = 1.1V [the real value of *Vth* can range between 0.85V and 1.35]
* *β* = 0.24A/V2 [the real value of *β* can range between 0.19V and 0.33]
* *λ* =0.02V**-1** [the real value of *λ* can range between 0.01V and 0.05]
* *R*θ*ja* = 255°C/W [the real value of *R*θ*ja* is influenced by the device mounting]

Assume the following operating parameters:

* *Vin* = 7V
* *Ro* = 120Ω
* *Ta* = 30°C

2-1 Using the rules and equations provided in the **Theory and Background** section, calculate the gate driver voltage *Vdr* required to achieve the values of output voltage listed in column 1 of Table 2-1, determine the status of the MOSFET (OFF = cut-off, SAT = saturation, OHM = ohmic), calculate the drain-to-source voltage and current, the power loss and the junction temperature of the MOSFET, with three decimal digits (for the temperature use one decimal digit), and report the results in Table 2-1.

Table 2-1 Gate driver voltage required to achieve a desired output voltage, given the source voltage and load resistance

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Vout [V] | status | Vdr [V] | VDS [V] | IDS [A] | Ploss [W] | Tj [°C] |
| 1.5 |  |  |  |  |  |  |
| 3.0 |  |  |  |  |  |  |
| 4.5 |  |  |  |  |  |  |
| 6.0 |  |  |  |  |  |  |

## 3 Simulate

The simulations you will perform in this section allow you to analyze the impact of the gate driver voltage *Vdr* on the operating point of a MOSFET operating as a linear regulator. You will compare the results of the simulations with the results of calculations performed in the **Exercise** section, based on the simplified Equations 1-6 - 1-9, to verify the theoretical prediction and evaluate the impact of MOSFET parameters on the DC operating point.

#### 3.1 Instructions

1. Open *Lab1 – MOSFET DC operation* from this file path:

<https://www.multisim.com/content/vuVttWyHxrRuPfki7F33Ad/lab-1-linear-regulator-open-loop-dc-operation/>

The circuit schematic for the analysis of MOSFET DC operating points is shown in Figure 3-1. The MOSFET is modeled by means of an *Analog Behavioral Modeling* current source (*ABM* current source). The *ABM* model implements the MOSFET Equations 1-2 provided in the **Theory and Background** section. The MOSFET parameters are set by means of the voltage sources *Vth*, *beta* and *lam* at the values used in the **Exercise** section.

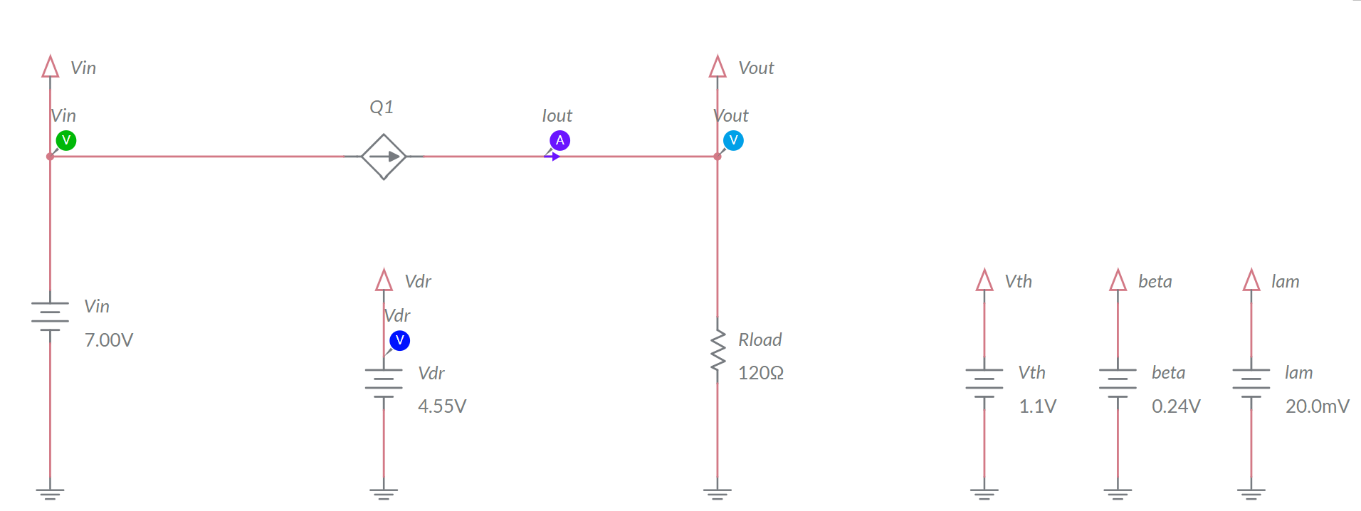


Figure 3-1. Multisim Live Circuit Schematic for the Analysis of a Linear Regulator in Open Loop DC Operation

1. Select the *Interactive* simulation option and the *Schematic* visualization option.
2. Set the gate driver voltage *Vdr* at zero.
3. Run the simulation and increase the gate driver voltage (*Vdr*) until the number shown by the output voltage probe (*Vout*) equals the value of the output voltage indicated in the first column-first row of Table 3-1, with three decimal digits.
4. Record the value of the gate driver voltage in the second column of Table 3-1.
5. Repeat the simulation for all the values of the output voltage *Vout* listed in column 1 of Table 3-1.
6. Import in column 3 of table 3-1 the values of gate driver voltage reported in column 2 of Table 2-1 of **Exercise** section.
7. Calculate the % error (*Vdr,cal*-*Vdr,sim*)/*Vdr,sim* x 100 between the values of the gate driver voltage *Vdr* obtained with calculations and simulations.
8. Calculate the power loss and the junction temperature of the MOSFET.
9. Calculate the % efficiency *η* = *Pout*/*Pin* x 100= *Vout*/*Vin* x 100.

Table 3-1 Gate driver voltage required to achieve a desired output voltage, given the source voltage and load resistance

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Vout [V] | Vdr,sim [V] | Vdr,cal [V]  from column 2 of Table 2-2 | Vdr  error [%] | Ploss [W] | Tj [°C] | η [%] |
| 1.5 |  |  |  |  |  |  |
| 3.0 |  |  |  |  |  |  |
| 4.5 |  |  |  |  |  |  |
| 6.0 |  |  |  |  |  |  |

3-1 Does the maximum power loss correspond to the minimum efficiency?

1. yes
2. no

Please provide your comment \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

3-2 What is the maximum *Vdr* % error between calculations and simulations?

1. max % error <1%
2. 1% < max % error < 10%
3. max % error >10%

3-3 Do you identify a trend in the *Vdr* error values vs the output voltage *Vout*?

1. yes
2. no

Please provide your comment \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

3-4 What is the possible origin of the error between *Vdr* calculations and simulations?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Troubleshooting tips:

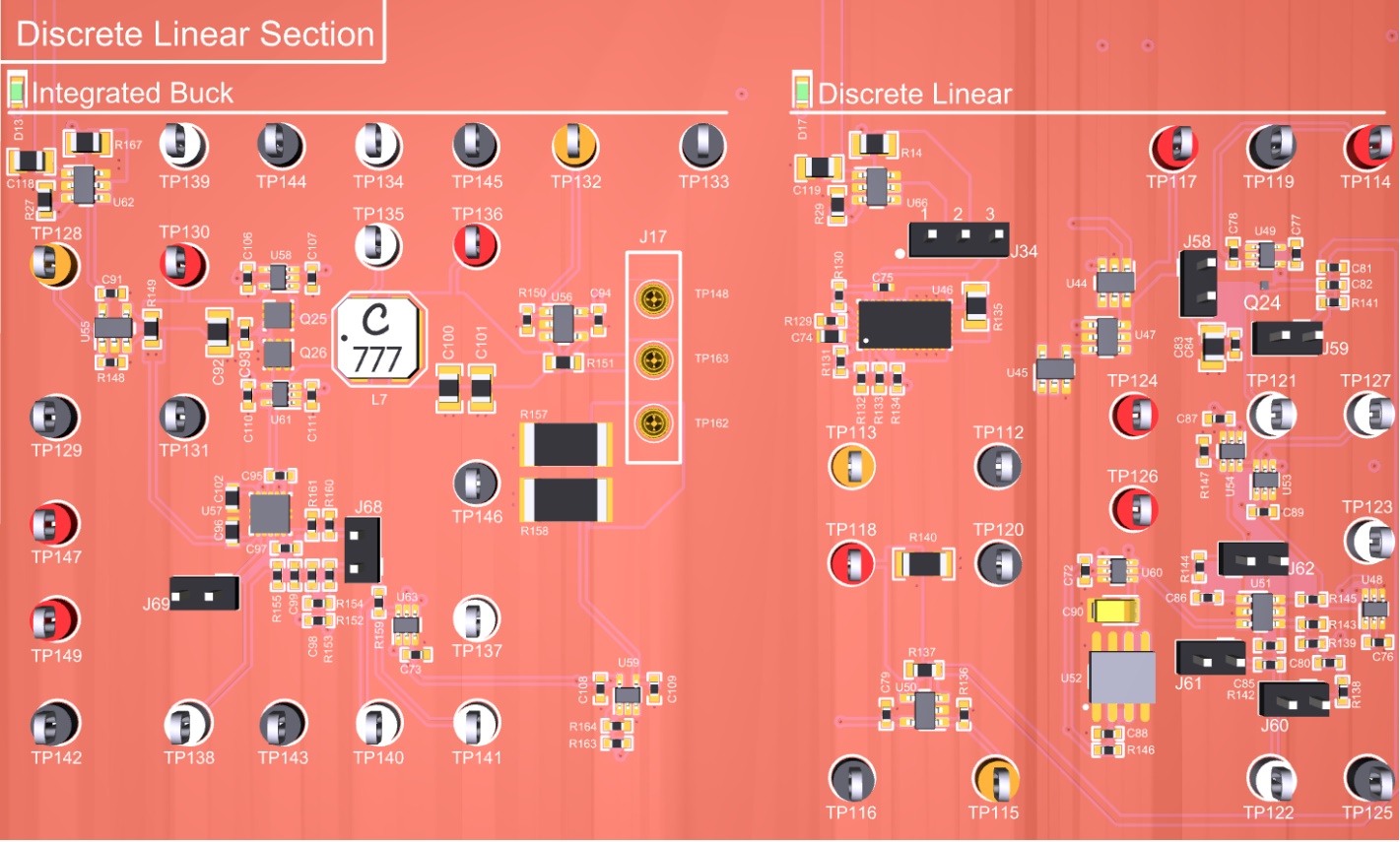
* If you get an error greater than 10% between simulation and calculation results, check the values of source voltage, load resistance and MOSFET parameters.
* If the simulation does not converge and you get some error message, reload *Lab1 – Linear Regulator in Open Loop DC Operation* from this file path:

https://www.multisim.com/content/vuVttWyHxrRuPfki7F33Ad/lab-1-linear-regulator-open-loop-dc-operation/

and restart the simulation following the relevant instructions.

### **4 Implement**

The **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1 allows performing experiments on MOSFET DC Operation as linear regulator. The jumpers and test points used to setup the tests and measure the signals of interest are highlighted. The experiments you perform in this section allow you to observe the behavior of a real MOSFET in DC operation, to verify the effect of the gate driver voltage on the MOSFET status and operating condition. You will compare the experimental measurements with the results of simulations. Next, you will verify the compliance of the MOSFET simulation model with the real MOSFET behavior. Finally, you will determine possible adjustments of MOSFET model parameters to improve accuracy of simulations. The MOSFET Q24 of the linear regulator is a Texas Instruments CSD15380F3 (<http://www.ti.com/lit/ds/symlink/csd15380f3.pdf>).



***TP114***

***J17***

***J68***

***J69***

***J59***

***Ro***

***Vdr***

***J62***

***Vout***

***J60***

***J61***

***J58***

***Iout***

***Ta***

***Vin***

***MOSFET***

***J34***

Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of a Linear Regulator in Open Loop DC Operation.

#### 4-1 Instructions

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to the tolerances of components on the TI Power Electronics Board]

1. Open *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter* using Measurements Live. For help on launching instruments, refer to this help document: <http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/>
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: <http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html>
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III(See Required Tools and Technology section for download instructions), and select *Lab1 – Linear Regulator in Open Loop DC Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.
6. Configure and connect the instruments as indicated in Tables 4-2 and 4-3.

Table 4-1 Jumpers setup

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| J17 | J34 | J58 | J59 | J60 | J61 | J62 | J68 | J69 |
| short TP162-TP163 | short 2-3 | open | short | short | short | short | short | short |

Table 4-2 Instruments Configuration and setup

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| *Power Supply* | *Channel “+”*: Static, 7.00V, *Channel “-“*: Inactive | | | |
| *Oscilloscope* | *Trigger*:  Immediate | *Horizontal*:  100us/div | *Acquisition*:  average | *Measurements*:  show |
| *Channel 1*: ON   * DC coupling * 1V/div * offset -4.0V | *Channel 2*: ON   * DC coupling * 1V/div * offset -4.0V | *Channel 3*: ON   * DC coupling * 1V/div * offset -4.0V | *Channel 4*: OFF |
| *Function Generator* | *Channel 1*: Inactive  *Channel 2*: Sine, Frequency 1Hz, Amplitude 0.00Vpp, DC offset 0.00V | | | |
| *Digital Multimeter* | *Measurement mode*: DC voltage; *Range*: Automatic | | | |

Table 4-3 Instruments Connections

|  |  |
| --- | --- |
| *Power Supply* | connect to red and black banana connectors |
| *Oscilloscope* | connect Ch-1 to TP117 (*Vin*), connect Ch-2 to TP118 (*Vout*)  connect Ch-3 to TP121 (*Vdr*) |
| *Function Generator* | connect Ch-2 to FGEN2 BNC connector (→TP121 = Discrete Linear *Vdr*) |
| *Digital Multimeter* | connect Voltage input to TP115 (*Iout*) |

1. Run *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter*.
2. Adjust the *Power Supply* voltage until the RMS measurement of *Oscilloscope* Ch-1 (*Vin*) equals 7.00V [**Note:** in this experiment,use Volts, Ampères and Watts in voltage, current and power measurements and calculations, respectively, with three decimal digits].
3. Increase the DC offset of the *Function Generator* Ch-2 (*Vdr*) until the RMS measurement of the *Oscilloscope* Ch-2 (*Vout*) equals the value of the output voltage indicated in the first column-first row of Table 4-4. [**Note:** the maximum allowed value of gate driver voltage *Vdr* is ***Vdr,max* = 6.5V**]
4. Read the RMS measurement of the *Oscilloscope* Ch-3 (*Vdr*) and the *Digital Multimeter* measurement (*Iout*), calculate the input power *Pin* = *Vin* x *Iout*, and record the values in columns 2, 5 and 6 of Table 4-4, respectively.
5. Calculate the output power *Pout* = *Vout* x *Iout*, and the % efficiency *η* = *Pout*/*Pin* x 100, with one decimal digit, and report the result in columns 7 and 8 of Table 4-4, respectively.
6. Connect the *Digital Multimeter* to Test Point TP114, read the DC voltage measurement *VTP114* in Volts, calculate the ambient temperature according to the formula *Ta* = (*VTP114* – 0.5V) x 100, calculate the MOSFET junction temperature according to the formula *Tj* = *Ta* + (*Pin* – *Pout*)*R*θ*ja*, and report the result in column 9.
7. Repeat the measurements for all the values of the output voltage *Vout* listed in column 1 of Table 4-4.
8. Stop *Power Supply*, *Function Generator*, *Oscilloscope* and *Digital Multimeter*.
9. Import in column 3 of Table 4-4 the values of voltage *Vdr\_sim* reported in column 2 of Table 3-1 of **Simulate** section.
10. Calculate the % error (*Vdr,sim*-*Vdr,meas*)/*Vdr,meas* x 100 between the values of the voltage *Vdr* obtained with simulations and measurements.

Table 4-4 DC operating point of the MOSFET, given the source voltage, load resistance and gate driver voltage

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| Vout  [V] | Vdr,meas  [V] | Vdr.sim [V]  from column 2  of Tab 3-2 | Vdr error  [%] | Iout  [A] | Pin  [W] | Pout  [W] | eff  [%] | Tj  [°C] |
| 1.50 |  |  |  |  |  |  |  |  |
| 3.00 |  |  |  |  |  |  |  |  |
| 4.50 |  |  |  |  |  |  |  |  |
| 6.00 |  |  |  |  |  |  |  |  |

4-1 What is the maximum *Vdr* % error between simulations and measurements?

1. max % error <1%
2. 1% < max % error < 10%
3. max % error >10%

4-2 What is the possible origin of the error between *Vdr* calculations and simulations?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-3 Did you to achieve the required output voltage with a gate driver voltage lower than the maximum allowed value of 6.5V?

1. yes
2. no

Please provide your comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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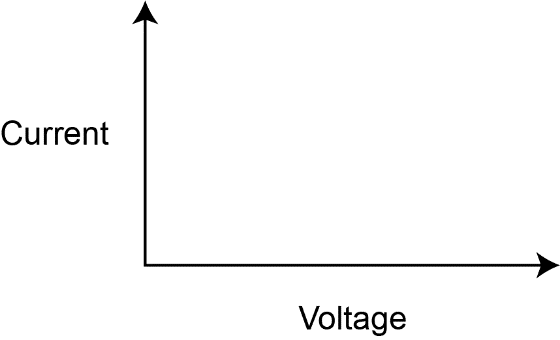
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#### Troubleshooting tips:

* If the MOSFET does not work, or if the error between simulation and measurement is greater than 20%, verify the correct setup and connections of instruments, based on directions provided in Tables 4-1 and 4-2, and restart the experiment.

### **5 Analyze**

5-1 Graph the values of voltage *Vdr* collected in columns 2 and 3 of Table 4-4 as a function of the required voltage *Vout*, including a legend that indicates which line style corresponds to which series (simulations, measurements).



Vdr [V]

Vout [V]

Figure 5-1 Simulated and Measured Values of Output Voltage Vout versus the Gate Driver Voltage Vdr.

5-2 Are the *Vdr* error values positive or negative?

1. always positive
2. always negative
3. either sign

Please provide your comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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5-3 Do you see a trend in the *Vdr* error values vs the output voltage *Vout*?

1. increasing
2. decreasing
3. no precise trend

Please provide your comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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5-4 Based on your observations and on the MOSFET properties discussed in the **Theory and Background** section, what parameter would you modify in the MOSFET model to reduce the error between measurements and simulations? How and why?

1. Vth: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
2. β: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
3. λ: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

5-5 Re-run the simulation by changing the parameters of MOSFET model, based on your answers to Question 5-5, and verify your predictions. Are the new simulation results closer to experimental ones? Do you infer a rule or a procedure to obtain the parameters of a MOSFET from experimental measurements?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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### **6 Conclusion**

### 6-1 Summary

Write a summary of what you learned and observed about the impact of MOSFET gate driver voltage and physical parameters on the linear regulator open loop DC operation. Explain why it is important to predict correctly the gate driver voltage value needed to achieve a desired value of the output voltage, and how the MOSFET parameters influence the value of gate driver voltage.

### 6-2 Expansion Activities

1. Investigate how the source voltage *Vin* influences the MOSFET operation, by determining the transition from saturation region to ohmic region. The investigation can be performed by means of simulations and experiments. In both cases, set the source voltage *Vin* at a given value (not exceeding 10V) and find the gate driver voltage *Vdr* that determines an output voltage *Vout* = *Vin*/2. Then, decrease the source voltage *Vin* in 100mV steps, while observing the output voltage *Vout*. You will observe no change in the output voltage until the input voltage reaches a certain value, below which you will see the output voltage to decrease. The change of behavior of the MOSFET is determined by the transition from the saturation to the ohmic region.
2. Repeat the Simulation 2 discussed in the **Simulate** section, by changing the voltage of sources *Vth*, *beta* and *lam* in the ranges indicated in Table 6-1, to investigate the sensitivity of the MOSFET DC operation point with respect to its model parameters.

Table 6-1 Gate driver voltage required to achieve a desired output voltage, given the source voltage and load resistance

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| min Vth [V] | max Vth [V] | min beta [S] | max beta [S] | min lam [V-1] | max lam [V-1] |
| 0.85 | 1.35 | 0.19 | 0.33 | 0.01 | 0.05 |

### 6-3 Resources for learning more

* This document provides the fundamentals of linear regulators:

Linear Regulators: Theory of Operation and Compensation, http://www.ti.com/lit/an/snva020b/snva020b.pdf

## Answer Key – Check Your Understanding Questions Only



Check Your Understanding

1-1 A

1-2 B

1-3 C

1-4 C

1-5 C

# Lab 2: Linear Regulator in Open Loop AC operation

The goal of this lab is to investigate the properties of a linear regulator in open loop AC operation. First, we will review the simplified equations describing the behavior of MOSFET in AC operation. Next, we will use this model to analyze and predict the sensitivity of the output voltage to AC perturbations injected on source and gate driver voltage, at different frequencies. Then, we will observe the response of a MOSFET to AC perturbations through simulations based on real MOSFET physical model. Finally, we will perform experimental measurements on a real MOSFET in AC operation, and will compare the results of calculations, simulations and measurements to verify the consistency of theoretical predictions.

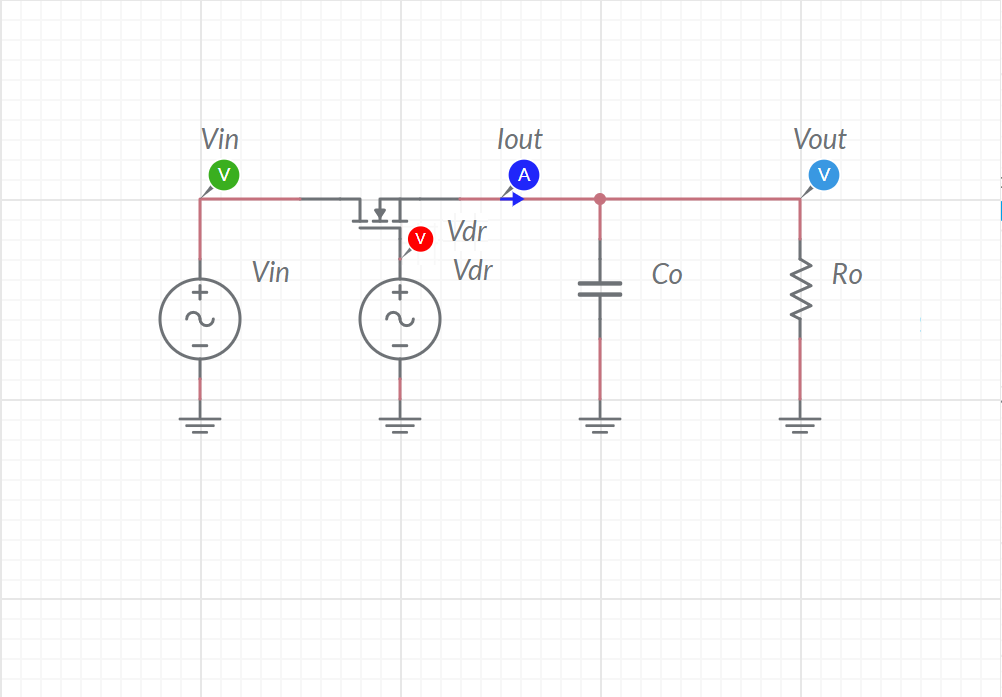


Figure 2-1 Linear Regulator

## Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a MOSFET, a load resistance, a DC source voltage, and a DC gate driver voltage, you will calculate the magnitude of the output voltage AC perturbation determined by AC perturbations injected on source and gate driver voltage, with specified units and accuracy, by applying the appropriate theoretical formulae.
2. Given a MOSFET, a load resistance, a DC source voltage, and a DC gate driver voltage, you will simulate the AC operation of the MOSFET to analyze the sensitivity of the output voltage with respect to AC perturbations injected by the source and gate driver voltage, with specified units and accuracy, to determine the accuracy of theoretical predictions.
3. Given a MOSFET, a dynamic power supply, a load resistor of given resistance, and a dynamic gate driver, you will analyze experimentally the output voltage AC perturbation determined by AC perturbations injected on source and gate driver voltage at different frequencies, with specified units and accuracy, to verify the consistency of theoretical predictions and simulations.

## Required Tools and Technology

|  |  |
| --- | --- |
| Platform: NI ELVIS III Instruments used in this lab:   * Function generator * Oscilloscope * Power Supply   **Note**: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments. ​ | * Access Instruments   https://measurementslive.ni.com/   * View User Manual http://www.ni.com/en-us/support/model.ni-elvis-iii.html * View Tutorials   <youtube link> |
| Hardware: TI Power Electronics Board | * View User Manual   http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html |
| Software: NI Multisim Live | * Access   <https://www.multisim.com/>   * View Tutorial   https://www.multisim.com/get-started/ |
| Software: TI Power Electronics Configuration Utility | * Download (Windows OS Only)   http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip   * Note: Mac Version will be available soon |

## Expected Deliverables

In this lab, you will collect the following deliverables:

* Calculations based on equations provided in the Theory and Background Section
* Results of circuit simulations performed by means of Multisim Live
* Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
* Observations on simulations and experiments
* Answers to questions

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

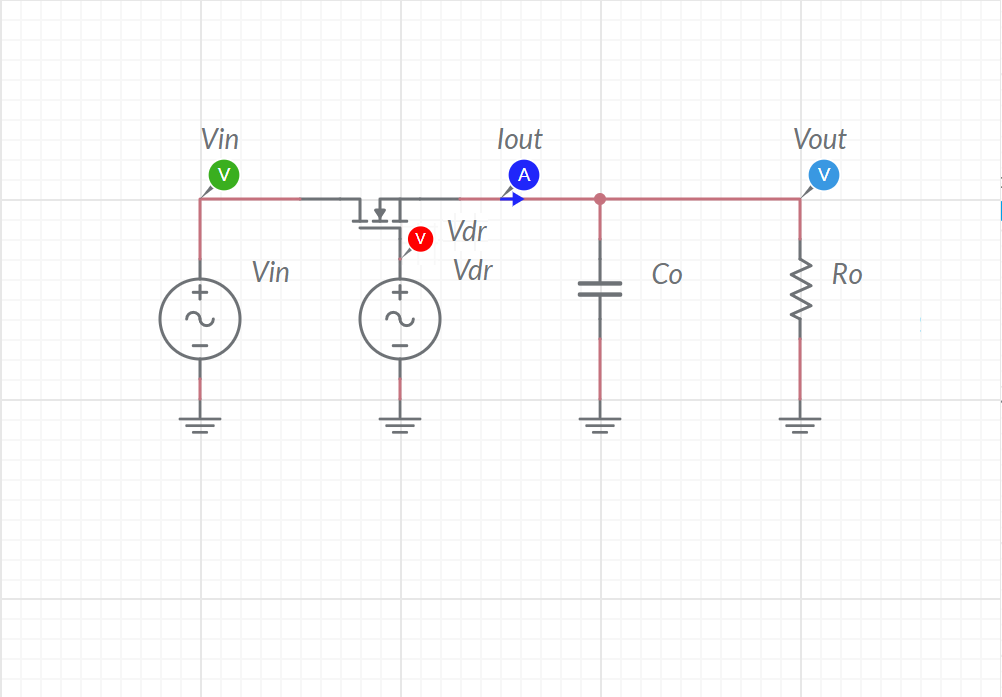
## 1 Theory and Background

1-1 Introduction.

In this section, we review the fundamental equations that are needed to analyze the AC operation of a MOSFET used in linear regulators applications. The AC response is an important feature of linear regulators, as it expresses the ability of the regulators to reject AC noise.

1-2 Linear Regulator in Open Loop AC Operation

Figure 1-2 shows a DC-DC linear regulator using a MOSFET as pass device, connected between a voltage source *Vin* and a load resistor *Ro*. The output voltage *Vout* is controlled by the MOSFET gate driver voltage *Vdr*. The capacitor *Co* damps the AC output voltage perturbations.



***+ =***

***VoutDC VoutAC Vout***

***+ =***

***VdrDC VdrAC Vdr***

***+ =***

***VinDC VinAC Vin***

Figure 1-2. Linear Regulator in Open Loop AC Operation

In steady-state, given the DC component of source voltage *VinDC*, the DC component of the gate driver voltage *VdrDC* can be adjusted to achieve the desired DC component value *VoutDC* of the output voltage. An AC perturbation *VinACsin*(2*πf∙t*) of frequency *f* is applied to the source voltage which causes an AC perturbation *VoutACsin*(2*πf∙t+ϕ*) on the output voltage, whose amplitude *VoutAC* and phase shift *ϕ* depend on MOSFET parameters, on *Co* and *Ro*, and on frequency *f*. An AC perturbation *VdrACsin*(2*πf∙t+θ*) injected on gate driver voltage at the same frequency *f*, with suitable amplitude *VdrAC* and phase shift *θ,* can cancel the output voltage AC perturbation.

1-3 Simplified Model of MOSFET in Open Loop AC Operation

A simplified model of a MOSFET in AC operation can be obtained by linearization of MOSFET drain-to-source DC current equations (see LAB1). The resulting simplified equations of the drain-to-source current *IdsAC* are:

*Equation 1-1* 

*Equation 1-2* 

, , , , 

where *Vth*, *β*, *λ* are the MOSFET gate-to-source threshold voltage, the transconductance coefficient and the channel-modulation coefficient, respectively. Equations 1-1 and 1-2 highlight that the AC response of the MOSFET depends on the DC operating point. Moreover, while the parameter *β* influences the output voltage sensitivity with respect to both *Vdr* and *Vin* (*Tin* and *Tdr* are both proportional to *β*), the parameter *λ* influences the output voltage sensitivity with respect to *Vin* (*Tin* is proportional to *λ*).

1-4 Open loop AC response of a linear regulator

The output voltage AC perturbation *VoutACsin*(2*πft+ϕ*) of a linear regulator caused by the effect of AC perturbations *VinACsin*(2*πft*) and *VdrACsin*(2*πft+θ*) of source and gate driver voltages can be analyzed by using the circuit shown in Figure 1-3. The amplitude *VoutAC* of the output voltage perturbation is given by Equation 1-3:

*Equation 1-3* 

Merging Equations 1-1, 1-2 and 1-3 provides the expression of the ratio between the amplitude *VoutAC* of the AC output voltage perturbation and the amplitudes *VinAC* and *VdrAC*:

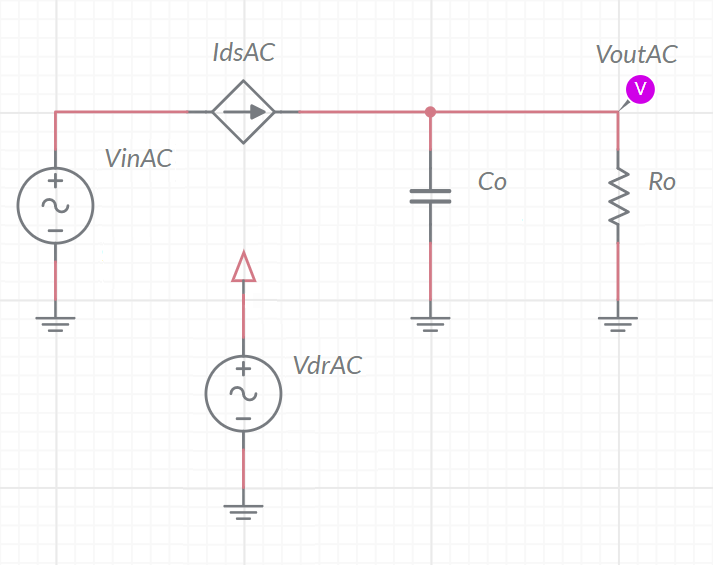


Figure 1-3. Simplified Circuit Model for the Analysis of Linear regulator in Open Loop AC Operation.

*Equations 1-4*



Equations 1-3 show that the sensitivity of the output voltage to AC source and gate driver voltage perturbations decreases as the frequency *f* increases. This means that the open loop linear regulator has a low-pass behavior. Moreover, the regulator has a different low-pass bandwidth, *fm* and *ft*, in the ohmic and saturation region respectively.

1-5 Effect of MOSFET capacitances.

The preceding simplified analysis neglects the impact of MOSFET capacitances. Therefore, Equations 1-6 and 1-7 are valid within a limited frequency range, whose boundary is influenced by the values of the MOSFET capacitances. Moreover, as the simplified model is based on linearization of MOSFET equations, the preceding analysis is more accurate if the amplitude of AC perturbations *VinAC* and *VdrAC* is small (less than 10%) compared to the amplitude of DC components *VinDC* and *VdrDC*.

Check Your Understanding

*Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all “Check your Understanding” questions at the end of the lab.*

1-1 How is the amplitude of the AC output voltage perturbations correlated to the frequency of the AC source and gate driver voltage perturbations?

1. it is not correlated
2. it increases as the frequency increases
3. it decreases as the frequency increases

1-2 How is the sensitivity of the AC output voltage perturbations correlated to the DC operating point of the MOSFET?

1. it is not correlated
2. it is higher in the ohmic region
3. it is higher in the saturation region

1-3 How can you cancel the effects of AC source voltage perturbations on the output voltage?

1. by means of a MOSFET with a big threshold voltage *Vth*
2. by means of an appropriate AC perturbation injected on the gate driver voltage
3. by means of a MOSFET with a small trans-conductance coefficient *β*

1-4 If your answer to Question 1-3 is “B”, what is the frequency of the AC perturbation to inject on the gate driver voltage?

1. the same of the AC source voltage disturbance
2. whatever
3. it depends on the DC output voltage

1-5 Is the accuracy of the simplified AC MOSFET model conditioned by the MOSFET AC operating conditions?

1. no
2. yes

if your answer is B, list the conditions ensuring better accuracy: \_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

## 2 Exercise

The Texas Instruments CSD15380F3 (<http://www.ti.com/lit/ds/symlink/csd15380f3.pdf>) N-channel MOSFET Q1 of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III has the following nominal parameters: *Vth* = 1.1V, *β* = 0.24A/V2*, λ* =0.02V**-1** [**Note:** if you have already performed **Lab1**, you can use the values of *Vth*, *β* and *λ* you have determined by means of the experiments]. Let us consider the following operating conditions and parameters:

A: *VinDC* = 5.00V, *VdrDC* = 4.55V, *VoutDC* = 3.00V, *Ro* = 120Ω, *Co* = 1μF.

B: *VinDC* = 3.30V, *VdrDC* = 4.60V, *VoutDC* = 3.00V, *Ro* = 120Ω, *Co* = 1μF.

2-1 Given the operating conditions A and B, for each value of the frequency *f* indicated in Table 2-1, use the equations provided in the **Theory and Background** section to:

* determine the MOSFET operating region (ohmic or saturation), calculate the relevant bandwidth *fm* or *ft* in kHz, with three decimal digits, and report the results in columns 2 and 5 of Table 2-1 (check the appropriate boxes), for case A and B respectively;
* calculate the amplitude in mV, with three decimal digits, of the AC output voltage perturbation *VoutAC* determined by an AC perturbation *VinAC* = 100mV applied to the source voltage, and report the results in columns 3 and 6 of Table 2-1, for case A and B respectively;
* calculate the amplitude in mV, with three decimal digits, of the AC output voltage perturbation *VoutAC* determined by an AC perturbation *VdrAC* = 100mV applied to the gate driver voltage, and report the results in columns 4 and 7 of Table 2-1, for case A and B respectively;

2-2 Repeat the calculations with *Co* = 11μF, and fill the relevant part of Table 2-2.

Table 2-1 Analysis of Linear Regulator in Open Loop AC operation, with Co=1μF.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Co=1μF | A: 🗹 SAT 🞏 OHM | | | B: 🞏 SAT 🗹 OHM | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| *f* [kHz] | 🞏 *fm* [kHz]  🗹 *ft* [kHz] | *VoutAC* [mV]  *VinAC*=100mV  *VdrAC*=0 | *VoutAC* [mV]  *VdrAC*=100mV  *VinAC*=0 | 🗹 *fm* [kHz]  🞏 *ft* [kHz] | *VoutAC* [mV]  *VinAC*=100mV  *VdrAC*=0 | *VoutAC* [mV]  *VdrAC*=100mV  *VinAC*=0 |
| 2 |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |
| 20 |  |  |  |  |  |  |

Table 2-2 Analysis of Linear Regulator in Open Loop AC operation, with Co=11μF.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Co=11μF | A: 🗹 SAT 🞏 OHM | | | B: 🞏 SAT 🗹 OHM | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| *f* [kHz] | 🞏 *fm* [kHz]  🗹 *ft* [kHz] | *VoutAC* [mV]  *VinAC*=100mV  *VdrAC*=0 | *VoutAC* [mV]  *VdrAC*=100mV  *VinAC*=0 | 🗹 *fm* [kHz]  🞏 *ft* [kHz] | *VoutAC* [mV]  *VinAC*=100mV  *VdrAC*=0 | *VoutAC* [mV]  *VdrAC*=100mV  *VinAC*=0 |
| 2 |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |
| 20 |  |  |  |  |  |  |

## 3 Simulate

The simulations you will perform in this section allow you to analyze AC perturbations on the output voltage of a MOSFET operating as linear regulator. You will observe the effects caused on the output voltage by AC perturbations injected on source voltage and on gate driver voltage. You will compare the results of the simulations with the results of calculations performed in the **Exercise** section, based on the simplified Equations 1-6 and 1-7, to verify the accuracy of theoretical calculations, and to observe the impact of the output capacitor on the AC perturbations of the output voltage.

#### 3.1 Instructions

1. Open *Lab2 – Linear Regulator in Open Loop AC operation* from this file path:

<https://www.multisim.com/content/WxHkfMbLxCkJrJVMqPbX8Y/lab-2-linear-regulator-ac-open-loop-operation/>

The circuit schematic for the analysis of MOSFET AC operation is shown in Figure 3-1. The MOSFET is modeled by means of current source Q1, and its parameters are set by means of the voltage sources *Vth*, *beta* and *lam*, and correspond to the values used in the **Exercise** section. The parameters {*VA*, *Freq*, *VO*} of the voltage generators *Vin* and *Vdr* correspond to the parameters {*VinAC*, *f*, *VinDC*}, and {*VdrAC*, *f*, *VdrDC*}, respectively, as defined in the **Theory and Background** section.

1. Enter the values recorded in columns 3, 4, 6 and 7 of Table 2-1 of Exercise section in columns 3, 5, 7 and 9 of Table 3-1, respectively.
2. Select the *Interactive* simulation option and the *Split* visualization option.
3. Set the switch S1 OPEN
4. Set the DC components *VinDC* and *VdrDC* of source and gate driver voltage generators at values indicated for ***Test A*** in Table 3-1.

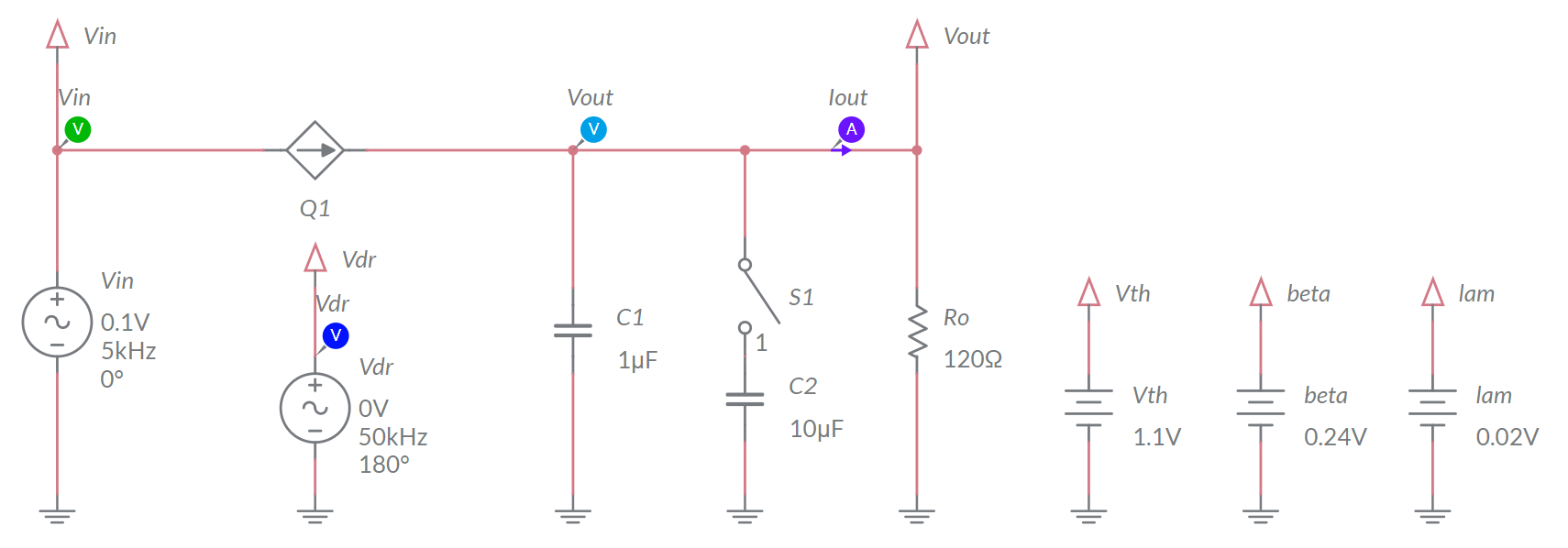


Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Linear Regulator in Open Loop AC Operation.

1. Set the AC component of source voltage generator *Vin* with amplitude *VinAC* = 0.1V.
2. Set the frequency of the AC component of source voltage generator *Vin* at the first value listed in column 1 of Table 3-1.
3. Set the AC component of gate driver generator *Vdr* with amplitude *VdrAC*=0.0V.
4. Run the simulation, read the measurement of peak-to-peak AC perturbation of the output voltage *Vpp* provided by the *Vout* voltage probe, calculate the amplitude *VoutAC* = *Vpp*/2 of the output voltage AC perturbation in mV, with two decimal digits resolution, and report the resulting value in column 2 of Table 3-1.
5. Repeat the step 9 for each value of the frequency listed in column 1.
6. Set the AC component of source voltage generator *Vin* with amplitude *VinAC* = 0V.
7. Set the AC component of gate driver generator *Vdr* with amplitude *VdrAC*=0.1V.
8. Set the frequency of the AC component of gate driver generator *Vdr* at the first value listed in column 1 of Table 3-1.
9. Run the simulation, read the measurement of peak-to-peak AC perturbation of the output voltage *Vpp* provided by the *Vout* voltage probe, calculate the amplitude *VoutAC* = *Vpp*/2 of the output voltage AC perturbation in mV, with two decimal digits resolution, and report the resulting value in column 4 of Table 3-1.
10. Repeat the step 14 for each value of the frequency listed in column 1.
11. Set the DC components *VinDC* and *VdrDC* of source and gate driver voltage generators at values indicated for ***Test B*** in Table 3-1.
12. Repeat the steps 6 to 15, and fill column 6 with values of *VoutAC* resulting from step 9 and column 8 with values of *VdrAC* resulting from step 14.
13. Set the switch S1 CLOSED, selecting the capacitor value, repeat the steps 5 to 17 and fill Table 3-2.

Table 3-1 Analysis of MOSFET in AC operation with Co=1μF.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | ***Test A:*** *VinDC* = 5.00V, *VdrDC* = 4.55V | | | | ***Test B:*** *VinDC* = 3.30V, *VdrDC* = 4.60V | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| *f* [kHz] | *VoutAC* [mV]  @*VdrAC*=0  simulation | *VoutAC* [mV]  *from col.3*  *of Tab 2-1* | *VoutAC* [mV]  @*VinAC*=0  simulation | *VdrAC* [mV]  *from col.4*  *of Tab 2-1* | *VoutAC* [mV]  @*VdrAC*=0  simulation | *VoutAC* [mV]  *from col.6*  *of Tab 2-1* | *VoutAC* [mV]  @*VinAC*=0  *simulation* | *VdrAC* [mV]  *from col.7*  *of Tab 2-1* |
| 2 |  |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |  |
| 20 |  |  |  |  |  |  |  |  |

Table 3-2 Analysis of MOSFET in AC operation with Co=11μF

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | ***Test A:*** *VinDC* = 5.00V, *VdrDC* = 4.55V | | | | ***Test B:*** *VinDC* = 3.30V, *VdrDC* = 4.60V | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| *f* [kHz] | *VoutAC* [mV]  @*VdrAC*=0  simulation | *VoutAC* [mV]  *from col.3*  *of Tab 2-1* | *VdrAC* [mV]  @*VoutAC*=0  simulation | *VdrAC* [mV]  *from col.4*  *of Tab 2-1* | *VoutAC* [mV]  @*VdrAC*=0  simulation | *VoutAC* [mV]  *from col.6*  *of Tab 2-1* | *VdrAC* [mV]  @*VoutAC*=0  *simulation* | *VdrAC* [mV]  *from col.7*  *of Tab 2-1* |
| 2 |  |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |  |
| 20 |  |  |  |  |  |  |  |  |

3-1 Do the values of *VoutAC* obtained with simulations and calculations show the same trend?

1. yes
2. no

Please provide your comment: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

3-2 Is the difference between calculations and simulations bigger in test A or in test B?

1. bigger in test A
2. bigger in test B
3. almost the same in test A and test B

Please provide your comment: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Troubleshooting tips:

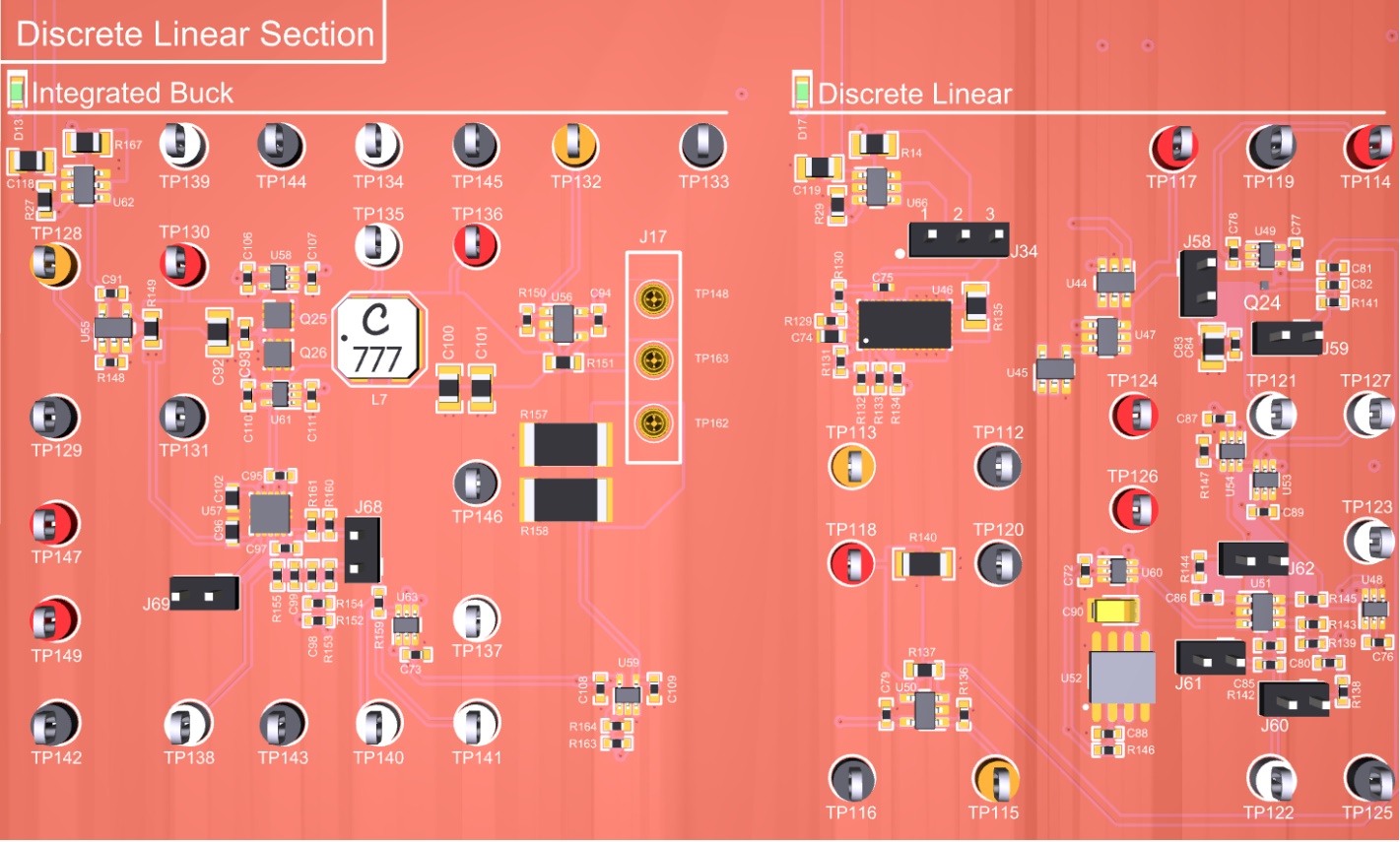
* If the simulation does not converge and you get some error message, reload *Lab2 – Linear Regulator in Open Loop AC Operation* from this file path:

<https://www.multisim.com/content/WxHkfMbLxCkJrJVMqPbX8Y/lab-2-linear-regulator-ac-open-loop-operation/>

and restart the simulation, following the instructions.

### **4 Implement**

The experiments in this section allow you to observe the behavior of a real MOSFET in AC operation, and to verify the effect of source and gate driver voltage AC perturbations on the output voltage. You will compare the measurements with calculations, to verify the consistency of the theoretical predictions. This experiment is performed by means of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1. The regulator uses the TI’s CSD15380F3 MOSFET and OPA835IDBVR OPAMP and is powered by a TI’s TPS40303DRCR Integrated Buck regulator, generating a 5V DC voltage. The AC disturbance on the input voltage of the Discrete Linear regulator is provided by the Integrated Buck regulator. The jumpers and test points used to setup the tests and to measure the signals are highlighted in Figure 4-1.



***J17***

***VFB***

***J69***

***J68***

***J59***

***Ro***

***Vdr***

***J62***

***Vout***

***J60***

***J61***

***J58***

***Iout***

***Ta***

***Vin***

***MOSFET***

***J34***

Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of Linear Regulator in Open Loop AC Operation

TI’s devices datasheets are available at the following links:

CSD15380F3 MOSFET: <http://www.ti.com/lit/ds/symlink/csd15380f3.pdf>

OPA835IDBVR OPAMP: <http://www.ti.com/lit/ds/symlink/opa835.pdf>

TPS40303DRCR Buck Regulator: <http://www.ti.com/lit/ds/symlink/tps40303.pdf>

#### 4-1 Instructions

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to the tolerances of components on the TI Power Electronics Board]

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: <http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/>
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: <http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html>
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III(See Required Tools and Technology section for download instructions), and select *Lab2 – Linear Regulator in Open Loop AC Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.

Table 4-1 Jumpers setup

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| J17 | J34 | J58 | J59 | J60 | J61 | J62 | J68 | J69 |
| short TP148-TP163 | short 2-3 | open | open | short | short | short | short | open |

1. Connect the instruments as indicated in Table 4-2.

Table 4-2 Instruments connections

|  |  |
| --- | --- |
| *Power Supply* | connect to red and black banana connectors |
| *Oscilloscope* | connect CH-1 to TP117 (Discrete Linear *Vin*)  connect CH-2 to TP118 (Discrete Linear *Vout*)  connect CH-3 to TP121 (Discrete Linear *Vdr*)  connect CH-4 to TP141 (Integrated Buck *VFB*) |
| *Function Generator* | connect Ch-1 to FGEN1 BNC connector (→TP141 = Integrated Buck *VFB*)  connect Ch-2 to FGEN2 BNC connector (→TP121 = Discrete Linear *Vdr*) |

1. Configure and setup the instruments as indicated in Table 4-3 for ***TEST A1***.

Table 4-3 Instruments initial configuration and setup

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *Power Supply* | *CH “+”*: Static, 7.00V, *CH “-“*: Inactive | | | | |
| *Oscilloscope* | *Trigger*:  Immediate | | *Horizontal*:  200us/div | *Acquisition*:  average | *Measurements*:  show |
| *CH-1*: ON   * DC coupling * 200mV/div * offset -5.0V | | *CH-2*: ON   * DC coupling * 50mV/div * offset -3.0V | *CH-3*: ON   * DC coupling * 50mV/div * offset -4.8V | *CH-4*: ON   * DC coupling * 50mV/div * offset -0.60V |
| *Function Generator* | ***TEST A1 and A2*** | | | | |
| *CH-1*: Sine, DC offset 600mV, Amplitude 0mV, Frequency 2kHz  *CH-2*: Sine, DC offset 4.85V, Amplitude 0mV, Frequency 2kHz | | | | |
| ***TEST B1 and B2*** | | | | |
| *CH-1*: Sine, DC offset 830mV, Amplitude 0mV, Frequency 2kHz  *CH-2*: Sine, DC offset 4.9V, Amplitude 0mV, Frequency 2kHz | | | | |
| *notes:* | * increasing the DC offset of CH-1 yields a decrease of *VinDC* * increasing the DC offset of CH-2 yields an increase of *VoutDC* | | | |

1. Run *Power Supply*, *Function Generator* and *Oscilloscope*.
2. Read the RMS Measurements of the *Oscilloscope* CH-1 (*Vin*) and CH-2 (*Vout*) in Volts: the expected values are *VinDC* = 5.0V and *VoutDC* = 3.0V. Adjust the DC offset of *Function Generator* CH-1 and CH-2 until you read the expected values, with at least one decimal digit accuracy.
3. Set the *Function Generator* CH-1 with amplitude = 190mV.
4. Stop the scope and use the horizontal cursors on the scope CH-1 waveform to measure the peak-peak *Vin,pk-pk* amplitude in milli Volts, with all decimal digits shown by the instrument, and report the result in column 2 of Table 4-4. [**Note:** a value *Vin,pk-pk* = 1000mV is expected, resulting in *VinAC* = 500mV. If needed, adjust the Amplitude of *Function Generator* CH-1 until you get *Vin,pk-pk* = 1000mV±50mV].
5. Measure the *Vout,pk-pk* amplitude in milli Volts, with all decimal digits shown by the instrument, calculate *VoutAC* = *Vout,pk-pk*/2 and report the result in column 3 of Table 4-4.
6. Calculate the ratio *VoutAC*/*VinAC*, with four decimal digits, and report the result in column 4 of Table 4-4.
7. Calculate the ratio *VoutAC*/*VinAC* by means of Equations 1-4 provided in **Theory and Background** section, with four decimal digits, and report the result in column 5 of Table 4-4.
8. Repeat steps 12-15 for the other values of frequency *f* listed in column 1 of Table 4-4, by adopting the following setups of Function Generator CH-1:

{Freq,Amp}= {10kHz,510mV}, {20kHz,980mV}.

Table 4-4 AC operation of the MOSFET in saturation region, with Co=1μF.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | ***test A1***  *VinDC* = 5.0V, *VdrDC* = 4.8V, *VoutDC* = 3.0V  *VinAC* = 500mV (nominal), *VdrAC* = 0 | | | | ***test A2***  *VinDC* = 5.0V, *VdrDC* = 4.8V, *VoutDC* = 3.0V  *VinAC* = 0, *VdrAC* = 100mV (nominal) | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| *f* [kHz] | *VinAC* [mV]  @*VdrAC*=0 | *VoutAC* [mV]  @*VdrAC*=0 | *measured* | *calculated* | *VdrAC* [mV]  @*VoutAC*=0 | *VoutAC* [mV]  @*VoutAC*=0 | *measured* | *calculated* |
| 2 |  |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |  |
| 20 |  |  |  |  |  |  |  |  |

[**Note:** adjust the oscilloscope horizontal scale to fit waveforms frequency. Suggested: 200us/div for 2kHz, 50us/div for 10kHz, 20us/div for 20kHz]

1. Configure the instruments as indicated in Table 4-3 for ***TEST A2***.
2. Read the RMS Measurement of the *Oscilloscope* CH-1 (*Vin*) and CH-2 (*Vout*) in Volts: the expected values are *VinDC*=5.0V and *VoutDC*=3.0V. Adjust the DC offset of *Function Generator* CH-1 and CH-2 until you read the expected values, with at least one decimal digit of accuracy.
3. Set the Amplitude of *Function Generator* CH-2 at 200mV.
4. Measure the amplitude of *Vdr,pk-pk* in milli Volts, with all decimal digits shown by the instrument, and report the result in column 6 of Table 4-4 [**Note:** a value *Vdr,pk-pk* = 200mV is expected, resulting in *VdrAC* = 100mV. If needed, adjust the Amplitude of *Function Generator* CH-2 until you get *Vdr,pk-pk* = 100mV±5mV].
5. Measure the amplitude of *Vout,pk-pk*, in milli Volts with all decimal digits shown by the instrument, calculate *VoutAC* = *Vout,pk-pk*/2 and report the result in column 7 of Table 4-4.
6. Calculate the ratio *VoutAC*/*VdrAC* and report the result in column 8 of Table 4-4.
7. Calculate the ratio *VoutAC*/*VdrAC* by means of Equations 1-4 provided in **Theory and Background** section, and report the result in column 9 of Table 4-4.
8. Repeat steps 20-23 for all frequency values listed in column 1 of Table 4-4.
9. Set the *Oscilloscope* offsets as follows: CH-1: -3.3V, CH3: -4.85V, CH-4: -0.8V.
10. Configure the instruments as indicated in Table 4-3 for ***TEST B1***
11. Repeat the steps 9-16 and report the results in Table 4-5, by adopting the following setup of *Function Generator* CH-1:

{Freq,Am} {2kHz,40mV}, {10kHz,100mV}, {20kHz,200mV}.

1. Configure the instruments as indicated in Table 4-3 for ***TEST B2***
2. Repeat the steps 18-24 and report the results in Table 4-5, by adopting the following setup of *Function Generator* CH-2:

{Freq,Amp}= {2kHz,200mV}, {10kHz,200mV}, {20kHz,200mV}.

1. Stop *Power Supply*, *Function Generator* and *Oscilloscope*.
2. Short the jumper J59 to set Co=11μF, repeat steps 8 to 30 and report the results in Tables 4-6 and 4-7.

Table 4-5 AC operation of the MOSFET in ohmic region, with Co=1μF.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | ***test B1***  *VinDC* = 3.3V, *VdrDC* = 4.9V, *VoutDC* = 3.0V  *VinAC* = 100mV (nominal), *VdrAC* = 0 | | | | ***test B2***  *VinDC* = 3.3V, *VdrDC* = 4.9V, *VoutDC* = 3.0V  *VinAC* = 0, *VdrAC* = 100mV (nominal) | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| *f* [kHz] | *VinAC* [mV]  @*VdrAC*=0 | *VoutAC* [mV]  @*VdrAC*=0 | *measured* | *calculated* | *VdrAC* [mV]  @*VoutAC*=0 | *VoutAC* [mV]  @*VoutAC*=0 | *measured* | *calculated* |
| 2 |  |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |  |
| 20 |  |  |  |  |  |  |  |  |

Table 4-6 AC operation of the MOSFET in saturation region, with Co=11μF.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | ***test A1***  *VinDC* = 5.0V, *VdrDC* = 4.8V, *VoutDC* = 3.0V  *VinAC* = 500mV (nominal), *VdrAC* = 0 | | | | ***test A2***  *VinDC* = 5.0V, *VdrDC* = 4.8V, *VoutDC* = 3.0V  *VinAC* = 0, *VdrAC* = 100mV (nominal) | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| *f* [kHz] | *VinAC* [mV]  @*VdrAC*=0 | *VoutAC* [mV]  @*VdrAC*=0 | *measured* | *calculated* | *VdrAC* [mV]  @*VoutAC*=0 | *VoutAC* [mV]  @*VoutAC*=0 | *measured* | *calculated* |
| 2 |  |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |  |
| 20 |  |  |  |  |  |  |  |  |

Table 4-7 AC operation of the MOSFET in ohmic region, with Co=11μF.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | ***test B1***  *VinDC* = 3.3V, *VdrDC* = 4.9V, *VoutDC* = 3.0V  *VinAC* = 100mV (nominal), *VdrAC* = 0 | | | | ***test B2***  *VinDC* = 3.3V, *VdrDC* = 4.9V, *VoutDC* = 3.0V  *VinAC* = 0, *VdrAC* = 100mV (nominal) | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| *f* [kHz] | *VinAC* [mV]  @*VdrAC*=0 | *VoutAC* [mV]  @*VdrAC*=0 | *measured* | *calculated* | *VdrAC* [mV]  @*VoutAC*=0 | *VoutAC* [mV]  @*VoutAC*=0 | *measured* | *calculated* |
| 2 |  |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |  |
| 20 |  |  |  |  |  |  |  |  |

4-1 Do you observe the same trend in the measured and calculated ratio *VoutAC*/*VinAC* as the frequency increases?

1. yes
2. no

Please provide your comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-3 Is the sensitivity of the output voltage with respect to source voltage AC perturbations higher in the saturation or in the ohmic region?

1. higher in saturation region
2. higher in ohmic region
3. it depends on the frequency of AC disturbances

4-2 Do you observe the same trend in the measured and calculated ratio *VoutAC*/*VdrAC* as the frequency increases?

1. yes
2. no

Please provide your comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-4 Is the sensitivity of the output voltage with respect to gate driver voltage AC perturbations higher in the saturation or in the ohmic region?

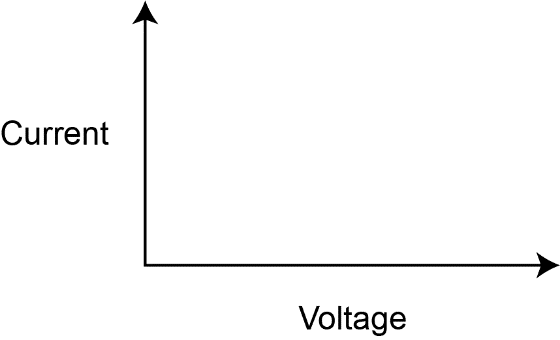
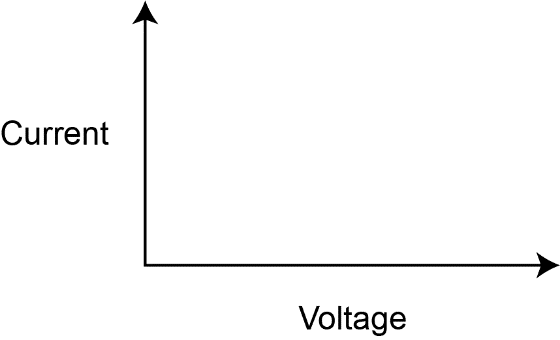
1. higher in saturation region
2. higher in ohmic region
3. it depends on the frequency of AC disturbances

#### Troubleshooting tips:

* If the MOSFET does not work as expected, verify the setup and connections of instruments provided in Tables 4-1, 4-2 and 4-3, and restart the experiment.

### **5 Analyze**

5-1 Graph the values of ratios *VoutAC*/*VinAC* and *VoutAC*/*VdrAC* collected in columns 4 and 5 and in columns 8 and 9 of Table 4-4, respectively, as a function of the frequency *f*, including a legend that indicates which line style corresponds to which series (calculations, measurements).

VoutAC

-------VdrAC

VoutAC

-------VinAC

f [kHz]

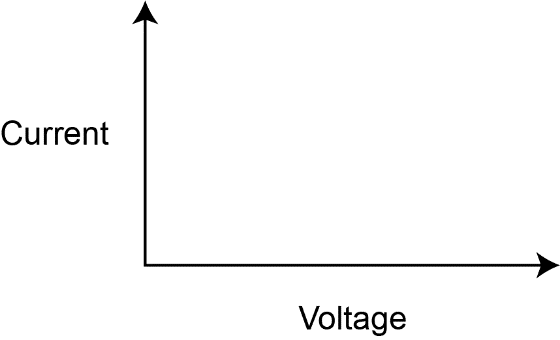
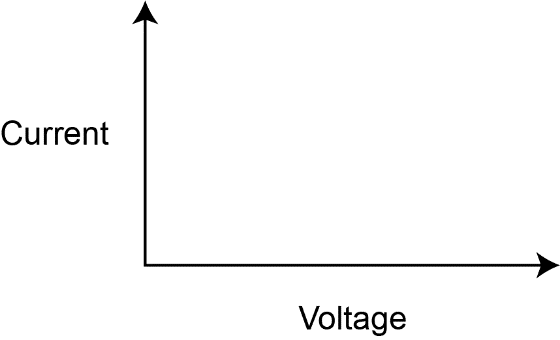
f [kHz]

Figure 5-1 Calculated and Measured Values of Ratios VoutAC/VinAC and VoutAC/VdrAC Obtained while Varying the Frequency, with the MOSFET Operating in the Saturation Region

5-2 Graph the values of ratios *VoutAC*/*VinAC* and *VoutAC*/*VdrAC* collected in columns 4 and 5 and in columns 8 and 9 of Table 4-5, respectively, as a function of the frequency *f*, including a legend that indicates which line style corresponds to which series (calculations, measurements).

VoutAC

-------VdrAC

VoutAC

-------VinAC

f [kHz]

f [kHz]

Figure 5-2 Calculated and Measured Values of Ratios VoutAC/VinAC and VoutAC/VdrAC Obtained while Varying the Frequency, with the MOSFET Operating in the Ohmic Region

5-3 In which operating region do you observe a bigger difference between calculated and measured values?

1. saturation region
2. ohmic region
3. they are similar

5-4 Based on your answer to question 5-3, what can be the cause of the difference between calculated and measured values?

1. the accuracy of the MOSFET linearized model given by Equations 1-1 and 1-2 is poor when the amplitude of AC perturbations is not small compared to the DC component of the source and gate driver voltage
2. the MOSFET parameters *Vth*, *β*, *λ* used for calculations are not sufficiently accurate
3. other: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

5-5 Based on your answers to previous questions, what corrective actions would you take on the MOSFET parameters *Vth*, *β*, *λ* to improve the accuracy of calculations?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

5-6 Repeat the calculations after making the actions you have proposed in you answer to Question 5-5, and verify your predictions. Are the new calculation results closer to experimental ones? Do you infer a practical guideline to obtain calculations better fitting experimental measurements?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

5-7 Based on your observations, what operating region would you adopt to achieve a better noise immunity of the output voltage under AC source perturbations?

1. ohmic
2. saturation
3. either

why? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

### **6 Conclusion**

### 6-1 Summary

Write a summary of what you learned and observed about the impact of the MOSFET DC bias point (saturation versus ohmic region) on its AC operation, regarding the sensitivity of the output voltage with respect to source and gate driver voltages AC perturbations. Explain why it is important to correctly determine the DC bias point of the MOSFET to predict its AC behavior by means of the mathematical model, and what are the main factors impacting the accuracy of theoretical calculations.

### 6-2 Expansion Activities

1. Investigate how the DC component of output voltage *VoutDC* influences the AC MOSFET operation, by repeating the previous calculations, simulations with Multisim Live circuit used in the **Simulate** section and measurements by means of the TI Power Electronics Board for NI ELVIS III used in the **Implement** section, with a different DC component of gate driver voltage *VdrDC*. You can analyze the operating conditions *VoutDC* = 1.5V (start with *VdrDC* = 2.9V, and adjust if needed) and *VoutDC* = 4.5V (start with *VdrDC* = 6.1V, and adjust if needed), with *VinDC* = 7.0V. [Notes: 1) **do not exceed** 7V on *VdrDC*; 2) the **Theory and Background** section of **LAB1** provides the general equations allowing to set the DC component of gate driver voltage *VdrDC* required to achieve the desired DC output voltage *VoutDC*; 3) set the offset of the *Oscilloscope* Ch-2 equal to -*VoutDC*].
2. Perform **LAB1**, to learn more about linear regulator in open loop DC operation
3. Perform the following actions to analyze the complete open loop AC frequency response of a linear regulator, by means of Bode plots:
4. Take the Multisim Live circuit used in the **Simulate** section, and select the *AC Sweep* simulation option and the *Split* visualization option.
5. Double click on the voltage generator *Vin*, select the *AC analysis value* menu option, and set AC\_mag = 0.1V
6. Double click on the voltage generator *Vdr*, select the *AC analysis value* menu option, and set AC\_mag = 0V
7. Open the *Configuration Panel* and set Start freq. = 10Hz and Stop freq. = 1MHz
8. Double click on probes *Vin*, *Vdr*, *Iout* and uncheck the *Show plots* box
9. Run the simulation and watch the resulting AC Sweep plots.

The continuous line is the magnitude of the ratio *VoutAC*/*VinAC*, while the dashed line is the phase shift between *VoutAC* and *VinAC*, over the selected frequency range. These plots are the graphic visualization (Bode plots) of the Equations 1-6 provided in the **Theory and Background** section. You can repeat the simulation to generate the Bode plots of the ratio *VoutAC*/*VdrAC*, by exchanging the setup of *Vin* and *Vdr* generators and probes.

### 6-3 Resources for learning more

* This document provides the fundamentals of linear regulators:

Linear Regulators: Theory of Operation and Compensation, <http://www.ti.com/lit/an/snva020b/snva020b.pdf>

## Answer Key – Check Your Understanding Questions Only



Check Your Understanding

1-1 C

1-2 B

1-3 B

1-4 A

1-5 B

## Lab 3: Error Amplifier Operation

The goal of this lab is to investigate the properties and the response of the error amplifier, which generates the MOSFET gate driver voltage in linear regulators. First, we will review the architecture and the simplified equations describing an error amplifier in DC and AC operation. Next, we will use the simplified error amplifier model to predict its AC gain. Then, we will simulate the response of the error amplifier to the perturbations of the output voltage with respect to the desired nominal value, in a linear regulator. Finally, we will perform experimental tests with a real error amplifier, and will compare the results of simulations and measurements to verify their consistency.

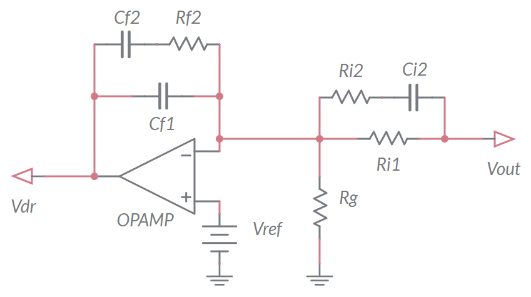


Figure 1-1. Error Amplifier.

## Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a MOSFET operating as linear regulator, a load resistance, a DC source, a gate driver generator, and an error amplifier, you will calculate the magnitude of the error amplifier voltage determined by DC deviations and AC perturbations on the output voltage of the linear regulator, with specified units and accuracy, by applying the appropriate theoretical formulae.
2. Given a MOSFET operating as linear regulator, a load resistance, a DC source, a gate driver generator, and an error amplifier, you will simulate the operation of the error amplifier to analyze the sensitivity of its voltage with respect to AC perturbations of the linear regulator output voltage, with specified units and accuracy, to verify the consistency of theoretical predictions.
3. Given a real MOSFET operating as linear regulator, a DC power supply, a load resistor of given resistance, a function generator, and a real error amplifier, you will measure the DC and AC components of the error amplifier voltage determined by DC and AC perturbations of the linear regulator output voltage, with specified units and accuracy, to verify the consistency of simulations and correct the model parameters.

## Required Tools and Technology

|  |  |
| --- | --- |
| Platform: NI ELVIS III Instruments used in this lab:   * Function generator * Oscilloscope * Power Supply   **Note**: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments. ​ | * Access Instruments   https://measurementslive.ni.com/   * View User Manual http://www.ni.com/en-us/support/model.ni-elvis-iii.html * View Tutorials   <youtube link> |
| Hardware: TI Power Electronics Board | * View User Manual   http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html |
| Software: NI Multisim Live | * Access   <https://www.multisim.com/>   * View Tutorial   https://www.multisim.com/get-started/ |
| Software: TI Power Electronics Configuration Utility | * Download (Windows OS Only)   http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip   * Note: Mac Version will be available soon |

## Expected Deliverables

In this lab, you will collect the following deliverables:

* Calculations based on equations provided in the Theory and Background Section
* Results of circuit simulations performed by means of Multisim Live
* Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
* Observations on simulations and experiments
* Answers to questions

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

## 1 Theory and Background

1-1 Introduction.

In this section, we review the fundamental equations used to analyze the DC and AC response of an error amplifier. The error amplifier is a fundamental part of linear regulators, as it drives the MOSFET gate voltage and regulates the output voltage.

1-2 Error Amplifier Architecture and Function

Figure 1-2 shows a linear regulator under open loop operation. The *error amplifier* consists of an operational amplifier (OPAMP), a voltage reference *Vref*, and a group of capacitors {*Cf1*,*Cf2*,*Ci2*} and resistors {*Rg*,*Ri1*,*Ri2*,*Rf2*}. The function of the error amplifier is to sense the output voltage *Vout* and compare it to a desired DC nominal value *VoutDC,nom*, to generate a gate driver voltage *VdrEA* ensuring that *Vout* = *VoutDC,nom*. The capacitors {*Cf1*,*Cf2*,*Ci2*} and the resistors {*Rg*,*Ri1*,*Ri2*,*Rf2*} determine the sensitivity of the error amplifier to the output voltage perturbations, and its capability to reject the effects of noise or undesired signals on the linear regulator output voltage.



power stage

error amplifier

Figure 1-2. Error Amplifier in Open Loop Operation.

1-3 DC Analysis of the Error Amplifier

The MOSFET of the linear regulator shown in Figure 1-2 is driven by the generator *Vdr*. The DC output voltage *VoutDC* is determined by the DC source voltage *VinDC* and by the DC gate driver voltage *VdrDC* (see **Lab1**). In DC steady-state operation, the capacitors *Ci2*, *Cf1* and *Cf2* are open, and the resistors *Rg* and *Ri1* form a *voltage divider sensor*, generating the feedback signal *VfbDC*. If the OPAMP operates in its linear region, we have *VfbDC* ≅ *Vref*, thus the DC output voltage fulfills Equation 1-1:

*Equation 1-1* 

where *H*=*Rg*/(*Rg*+*Ri1*). According to Equation 1-1, we can achieve a desired nominal DC output voltage *VoutDC,nom* > *Vref* with two resistances *Rg* and *Ri1* fulfilling Equation 1-2:

*Equation 1-2* 

In DC operation, the error amplifier generates the MOSFET gate driver voltage *VdrEA,DC* required to achieve the nominal value *VoutDC,nom* (see **Lab1**):

*Equation 1-3* 

If the DC output voltage deviates from the value *VoutDC,nom*, the error amplifier will generate a voltage given by

*Equation 1-4* 

The coefficient *GEA,DC* is the error amplifier *open loop DC gain*. Based on Equation 1-4, if *VoutDC* > *VoutDC,nom* the error amplifier decreases *VdrEA*, whereas if *VoutDC* < *VoutDC,nom* the error amplifier increases *VdrEA*. We can achieve *VoutDC* = *VoutDC,nom* only if *GEA,DC* = ∞. In reality, *GEA,DC* = *AdcH*, where *Adc* is the OPAMP DC open loop gain. An OPAMP with a higher DC open loop gain *Adc* ensures a smaller steady-state error *VoutDC* - *VoutDC,nom*. The output voltage *Vdr* of the error amplifier is upper bounded by the OPAMP positive supply rail voltage *Vcc+*, and lower bounded by the negative supply rail voltage *Vcc-*. Therefore, Equation 1-4 is valid only if the OPAMP operates in the linear region, which happens when *Vcc-* < *AdcH*(*VoutDC,nom* - *VoutDC*) < *Vcc+*.

1-4 AC Analysis of the Error Amplifier

An AC perturbation *VinACsin*(2*πf∙t*) injected on the source voltage generates an AC perturbation *VoutACsin*(2*πf∙t+ϕ*) on the output voltage (see **Lab2**). The error amplifier senses the output voltage AC perturbation and generates a signal *VdrACsin*(2*πf∙t+θ*). The amplitude *VdrAC* depends on the amplitude *VoutAC* and frequency *f* of the AC output voltage perturbation. The AC gain *GEA,AC* = *VdrAC*/*VoutAC* of the error amplifier is given by:

*Equation 1-5* 

where *fLPF* = *f0*/*Adc*. The pole frequencies *f0*, *fP* and the zero frequency *fZ* influence the sensitivity of the error amplifier with respect to output voltage AC perturbations, and impact the stability of the regulator. They are set by means of the capacitors {*Cf1*,*Cf2*,*Ci2*}, and the resistors {*Rg*,*Ri1*,*Ri2*,*Rf2*}. Equation 1-5 highlights that the parameters *f0*, *fP* and *fZ* are not influential on the error amplifier sensitivity at very low frequency. Normally, *fZ* < *fP*, and Equation 1-5 can be simplified as follows:

*Equation 1-6* 

The frequency *f0* determines the sensitivity of the error amplifier. A higher *f0* expands the range of frequency where the error amplifier is more sensitive to the output voltage AC perturbations. For the error amplifier shown in Figure 1-1 (known as *Type III* error amplifier) *f0* =1/(*Ri1*(*Cf1*+*Cf2*)). The sensitivity of the error amplifier decreases as the frequency *f* of the AC perturbation increases, except in the frequency range [*fZ*,*fP*]. The ratio *fP*/*fZ* is fixed based on *stability* requirements, and it is typically higher if *f0* is higher. The phase *θ* of the error amplifier output voltage *VdrACsin*(2*πf∙t+θ*) is correlated to the phase *ϕ* of the linear regulator output voltage *VoutACsin*(2*πf∙t+ϕ*) by Equation 1-7:

*Equation 1-7* 

Based on Equations 1-5 and 1-7, if *f* < *fLPF* we have an *inverting error amplifier* with a very high gain, whereas if *f* > *fLPF* the gain decreases and the error amplifier voltage is expected to be delayed 270° with respect to the output voltage perturbation, except for 0.3*fZ*<*f*<3*fP*.

Check Your Understanding

*Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all “Check your Understanding” questions at the end of the lab.*

1-1 What are the error amplifier parameters determining the nominal DC output voltage of a linear regulator?

1. the frequencies of zero and poles
2. the source voltage of the regulator
3. the reference voltage and the resistors of the voltage divider sensor

1-2 What parameter of the OPAMP determines the magnitude of the linear regulator output voltage DC error?

1. the DC open loop gain
2. the positive supply voltage
3. the low frequency pole

1-3 What is the amplitude of the error amplifier AC voltage correlated to the frequency of the linear regulator AC output voltage perturbations?

1. it is not correlated
2. it increases as the frequency increases
3. it decreases as the frequency increases

1-4 What parameter of the error amplifier majorly impacts its sensitivity with respect to the linear regulator AC output voltage perturbations?

1. the frequency of zero *fZ*
2. the frequency of pole *f0*
3. the reverence voltage *Vref*

1-5 Based on your answer to Question 1-4, say what actions you would make to improve the sensitivity of the error amplifier:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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## 2 Exercise

The error amplifier of the **Discrete Linear Section** in the TI Power Electronics Board for NI ELVIS III uses the TI’s OPA835IDBVR OPAMP) and has the following nominal parameters (<http://www.ti.com/lit/ds/symlink/opa835.pdf>):

* *Adc*=106, *Vcc+*=5.5V, *Vcc-*=0V.
* *Rg*=26.1kΩ, *Ri1*=39.2kΩ, *Vref*=1.024V.
* *f0* = 3.28kHz, *fZ* = 5.44kHz*, fP* = 172.95kHz, *fLPF* = 3.28mHz.

2-1 Given the parameters of the error amplifier, calculate the expected nominal value of the DC output voltage *VoutDC,nom*:

*VoutDC,nom* = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ (2.562V)

2-2 What are the values of resistances *Rg* and *Ri1* required to achieve a nominal DC output voltage *VoutDC,nom* = 3.3V?

Given *Rg*=26.1kΩ, *Ri1,nominal* = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ (58.011kΩ)

Given *Ri1*=39.2kΩ, *Rg,nominal* = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ (17.637kΩ)

2-3 You have an AC perturbation *VoutACsin*(2*πf∙t*) on the output voltage of the linear regulator, which has an amplitude *VoutAC* = 10mV and frequency *f* listed in Table 2-1. Calculate the ratio *VdrAC/VoutAC* and the expected value of the amplitude *VdrAC*, in milli Volts with one decimal digit, of the AC voltage *VdrACsin*(2*πf∙t+θ*) generated by the error amplifier.

Table 2-1 Analysis of error amplifier voltage in AC operation.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *f* [Hz] | 1 | 10 | 100 | 1000 | 10000 | 100000 |
| *VdrAC/VoutAC* |  |  |  |  |  |  |
| *VdrAC* [mV] |  |  |  |  |  |  |

2-4 Is the OPAMP able to generate all the *VdrAC* values you have collected in Table 2-1?

1. yes
2. no

if your answer is B, when? why?: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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## 3 Simulate

The simulations you will perform in this section will allow you to analyze the open loop behavior of an error amplifier. First, you will observe the voltage generated by the error amplifier, under different conditions determined by the deviations of the linear regulator output voltage with respect to the desired nominal value. Then, you will compare the results of the simulations with the results of calculations performed in the **Exercise** section, to verify the consistency of theoretical calculations and simulations.

#### 3.1 Simulation 1: Instructions

1. Open *Lab3 – Error Amplifier Operation* from the file path:

<https://www.multisim.com/content/QQ7QQ7drTxXe82G5zYttqc/lab-3-error-amplifier-operation/>.

The circuit is shown in Figure 3-1.

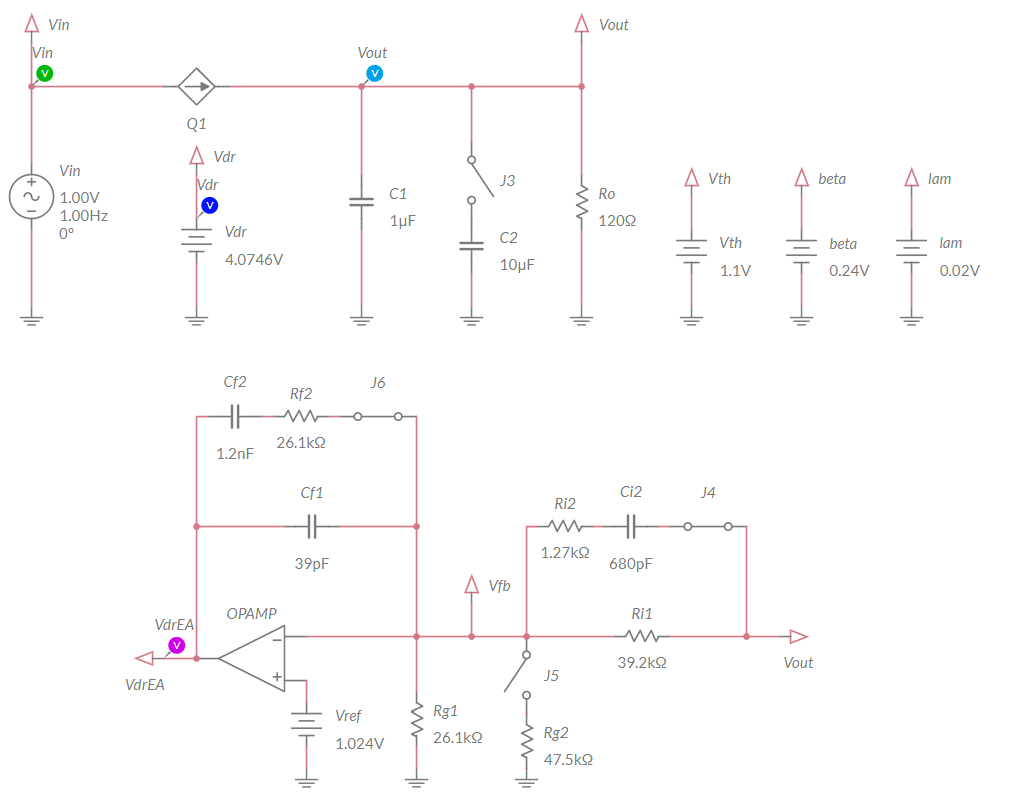


Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Error Amplifier Operation.

In this simulation, you will observe the response of the error amplifier to deviations of the output voltage of the linear regulator with respect to the nominal value. For this purpose, the error amplifier voltage *VdrEA* is not used directly as gate driver voltage. The generator *Vdr* is used indeed to set the desired DC output voltage *VoutDC* (see **Lab1**). Injecting an AC perturbation *VinACsin*(2*πf∙t*) on source voltage *Vin* generates an AC perturbation *VoutACsin*(2*πf∙t+ϕ*) on the output voltage (see **Lab2**).The auxiliary generators *Vth*, *beta* and *lam* allow to set the MOSFET parameters {*Vth*, *β*, *λ*}, respectively. The parameters {*VA*, *Freq*, *VO*} of generators *Vin* and *Vdr* correspond to the parameters {*VinAC*, *f*, *VinDC*}, and {*VdrAC*, *f*, *VdrDC*}, respectively, as defined in the **Theory and Background** section. The capacitors {*Cf1*,*Cf2*,*Ci2*}, and the resistors {*Rg*,*Ri1*,*Ri2*,*Rf2*} are set so that the resulting error amplifier zero and poles are approximately *f0* = 3.28kHz, *fZ* = 5.44kHz*, fP* = 172.95kHz. The OPAMP parameters are *Adc*=106, *fOPAMP* = 30Hz, *Vcc+*=5.5V, *Vcc-*=0V.

1. Set the switches J3 and J5 to be OPEN, and the switches J4 and J6 to be CLOSED in the simulation schematic.
2. Select the *Interactive* simulation option and the *Split* visualization option.
3. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
4. Check the *Instantaneous* option box for voltage probes *Vin*, *Vout*, and *VdrEA* in the *Measurement labels* menu.
5. Calculate the nominal value *VoutDC,nom* in Volts with three decimal digits, and report the result in Table 3-1.
6. Set *VA*=0, *Freq*=100Hz, *VO*=5V for the generator *Vin*, and *DC\_mag* = 4.05V for the generator *Vdr*.
7. For each value of *DC\_mag* of the DC voltage generator *Vdr* listed in Table 3-1, run the simulation, read the measurements of voltage probes *Vout* and *VdrEA* in Volts with three decimal digits and report the results in Table 3-1.

Table 3-1 Error Amplifier voltage as function of linear regulator output voltage Vout.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *VdrDC* (DC\_mag) [V] | 4.050 | 4.060 | 4.070 | 4.080 | 4.090 | 4.100 |
| *VoutDC,nom* [V] |  | | | | | |
| *VoutDC* [V] |  |  |  |  |  |  |
| *VoutDC* - *VoutDC,nom* [V] |  |  |  |  |  |  |
| *VdrEA* [V] |  |  |  |  |  |  |

3-1-1 How does the error *VoutDC* - *VoutDC,nom* vary as *Vdr* increases?

1. it increases
2. it decreases

other: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

3-1-2 How does the error amplifier voltage *VdrEA* vary as *Vdr* increases?

1. it increases
2. it decreases

other: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

3-1-3 Discuss the results of the error amplifier voltage *VdrEA*, based on the equations and relevant comments provided in the **Theory and Background** section:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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3-1-4 Set the values of the auxiliary generators *Vth =* 1.35, *beta* = 0.33 and *lam* = 0.05 in the circuit schematic, run the simulation and find the threshold value of *VdrDC* determining the transition of the error amplifier voltage *VdrEA* from *Vcc+* to *Vcc-*. Is this value greater or smaller than the threshold value of *VdrDC* from the Table 3-1?

1. greater
2. smaller

why?: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

#### 3.2 Simulation 2: Instructions

1. Open *Lab3 – Error Amplifier Operation* from the file path:

<https://www.multisim.com/content/QQ7QQ7drTxXe82G5zYttqc/lab-3-error-amplifier-operation/>

1. Set the switches J3 and J5 OPEN, and the switches J4 and J6 to be CLOSED.
2. Select the *Interactive* simulation option and the *Split* visualization option.
3. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
4. Check the *Periodic* option box for voltage probes *Vin*, *Vout*, and *VdrEA* in the *Measurement labels* menu.
5. Set *VA*=1V, *Freq*=1Hz, *VO*=5V for the generator *Vin*, and *DC\_mag* = 4.0746V for the generator *Vdr* and run the simulation.
6. Read the DC average measurement *VAV* and the AC peak-to-peak measurement *Vpp* of *Vout* voltage probe and report the values of *VoutDC* *= VAV* (in Volts with three decimal digits) and *VoutAC* (in milli Volts with three decimal digits) in Table 3-2
7. Read the DC average measurement *VAV* and the AC peak-to-peak measurement *Vpp* of *VdrEA* voltage probe and report the values of *VdrEA,DC* *= VAV* (in Volts with three decimal digits) and *VdrEA,AC* (in milli Volts with three decimal digits) in Table 3-2
8. Repeat steps 7-8 under *Vin* frequency and amplitude listed in Table 3-2.
9. Import in Table 3-2 the values of *VdrAC/VoutAC* recorded in Table 2-1 of **Exercise** section, for the corresponding frequencies.

Table 3-2 Error Amplifier response with Co=1μF.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| f [Hz] (Vin Freq) | 1 | 10 | 100 | 1000 | 10000 | 100000 |
| VinAC [V] (Vin VA) | 0.5 | 1 | 1 | 1 | 1 | 1 |
| VdrDC [V] (Vdr DC\_mag) | 4.0746 | | | | | |
| ML Simulation  Max. Time Step | 1e-5 | 1e-5 | 1e-5 | 1e-6 | 1e-7 | 1e-8 |
| ML Grapher  Horizontal Axis | 500ms/div | 50ms/div | 5ms/div | 500us/div | 50us/div | 5us/div |
| VoutDC,nom [V] |  | | | | | |
| VoutDC [V] |  |  |  |  |  |  |
| VoutAC [mV] |  |  |  |  |  |  |
| VdrEA,DC [V] |  |  |  |  |  |  |
| VdrEA,AC [mV] |  |  |  |  |  |  |
| VdrEA,AC/VoutAC |  |  |  |  |  |  |
| *VdrAC/VoutAC*  from Table 2-1 |  |  |  |  |  |  |

3-2-1 Do the values of *VdrEA,AC* obtained with simulations show the same trend of *VdrAC* results obtained with calculations?

1. yes
2. no

if your answer is B, highlight and discuss the differences: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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3-2-2 How does the ratio *VdrAC/VoutAC* vary with the frequency?

1. it increases
2. it decreases
3. other

if your answer is C, describe and discuss what you observe: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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3-2-3 Should the error amplifier exhibit a different ratio *VdrAC/VoutAC* if the MOSFET parameters *Vth*, *β* and *λ* are changed?

1. yes
2. no

why?: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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If you are not able to answer Question 3-2-3, change the value of the generators *Vth*, *lam* and *beta* in the circuit schematic and run the simulation. Analyze the results, read the **Theory and Background** section and then answer the question.

Troubleshooting tips:

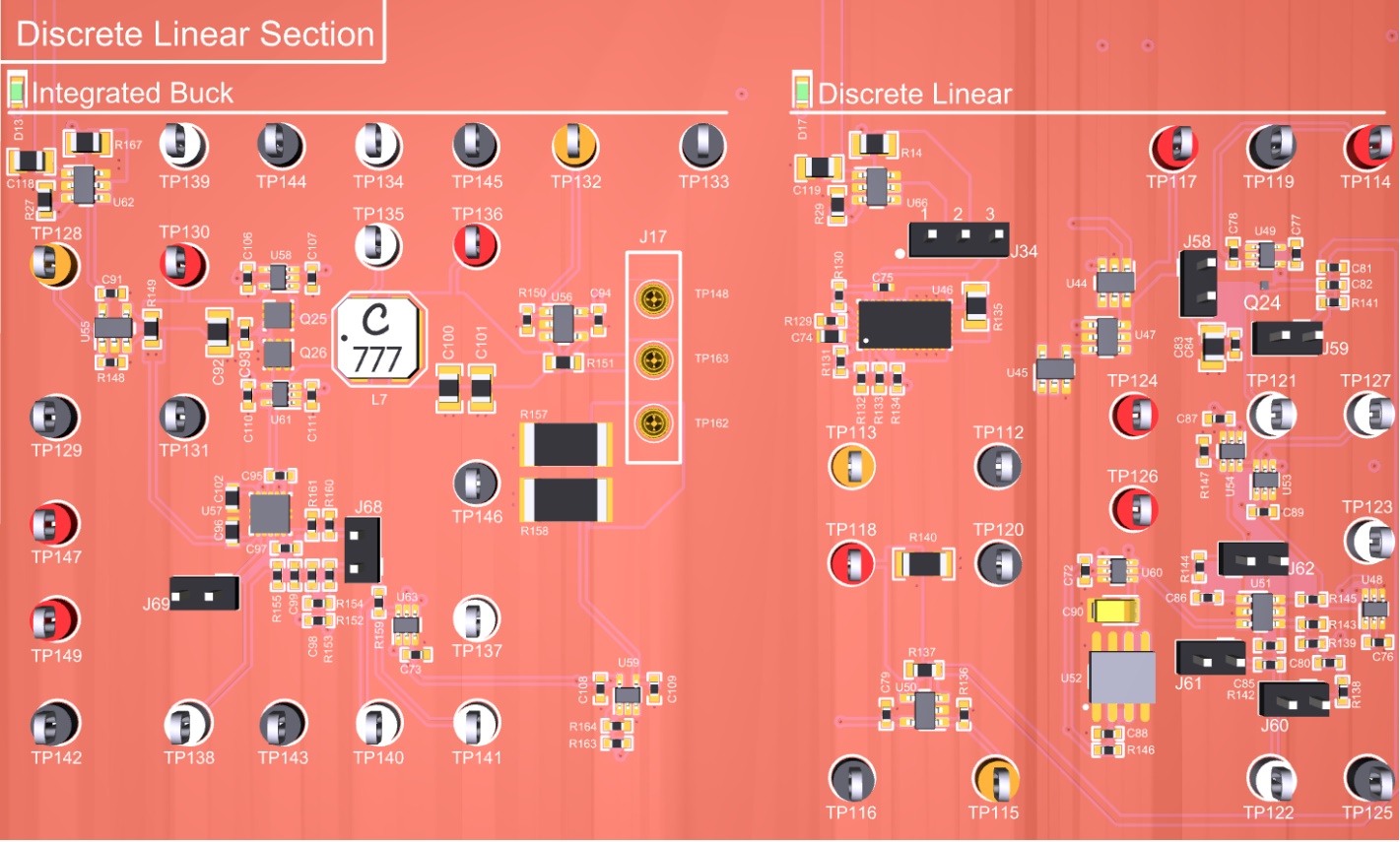
* If the simulation does not run and you get some error message, reload *Lab3 – Error Amplifier Operation* from this file path:

<https://www.multisim.com/content/QQ7QQ7drTxXe82G5zYttqc/lab-3-error-amplifier-operation/>

and restart the simulation, following the instructions.

### **4 Implement**

The experiments of this section allow you to observe the behavior of a real error amplifier, and to verify the response of the error amplifier to DC and AC deviations of the output voltage of a linear regulator with respect to the desired nominal value. You will compare the experimental measurements with simulations, to verify their consistency and determine possible adjustments of MOSFET model parameters to improve the accuracy of simulations. The experiments are performed by means of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1, which uses the TI’s CSD15380F3 MOSFET (pass device) and OPA835IDBVR OPAMP (error amplifier). The linear regulator is powered by a TI’s TPS40303DRCR Integrated Buck regulator, generating a 5V DC voltage. The AC disturbance on the output voltage of the Discrete Linear regulator is generated by applying an AC signal to the linear regulator gate driver voltage. The error amplifier pole frequency *f0* is 3.3kHz when jumpers J60 and J62 are shorted, and 104kHz when jumpers J60 and J62 are open. The output capacitance *Co* is 1µF with jumper J59 open, and 11µF with jumper J59 shorted. The nominal output voltage of the linear regulator is set at 2.5V with jumper J61 open, and at 3.3V with jumper J61 shorted.



***J17***

***J68***

***J69***

***J59***

***Ro***

***Vdr***

***J62***

***Vout***

***J60***

***J61***

***J58***

***Iout***

***Ta***

***Vin***

***MOSFET***

***J34***

Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of Error Amplifier Operation

TI’s devices datasheets are available at the following links:

CSD15380F3 MOSFET: <http://www.ti.com/lit/ds/symlink/csd15380f3.pdf>

OPA835IDBVR OPAMP: <http://www.ti.com/lit/ds/symlink/opa835.pdf>

TPS40303DRCR Buck Regulator: <http://www.ti.com/lit/ds/symlink/tps40303.pdf>

#### 4-1 General Instructions

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to the tolerances of components on the TI Power Electronics Board]

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: <http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/>
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: <http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html>
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS (See Required Tools and Technology section for download instructions), and select *Lab3 – Error Amplifier Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.
6. Connect the instruments as indicated in Table 4-2.

Table 4-1 Jumpers setup

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| J17 | J34 | J58 | J59 | J60 | J61 | J62 | J68 | J69 |
| short TP148-TP163 | short 2-3 | open | open | short | open | short | short | open |

Table 4-2 Instruments connections

|  |  |
| --- | --- |
| *Power Supply* | connect to red and black banana connectors |
| *Oscilloscope* | connect CH-1 to TP117 (input voltage *Vin*)  connect CH-2 to TP118 (output voltage *Vout*)  connect CH-3 to TP121 (gate driver voltage *Vdr*)  connect CH-4 to TP123 (error amplifier voltage *VdrEA*) |
| *Function Generator* | connect Ch-2 to FGEN2 BNC connector (→TP121 = gate driver voltage *Vdr*) |

#### 4-2 Experiment 1: Instructions

1. Use the instruments configuration and setup shown in Table 4-2-1.
2. Run *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 4-2-1 Instruments initial configuration and setup

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| *Power Supply* | *CH “+”*: Static, 7.00V, *CH “-“*: Inactive | | | | | | |
| *Oscilloscope* | *Trigger*:  Immediate | *Horizontal*:  100us/div | | *Acquisition*:  average | *Measurements*:  show | *Probe Attenuation*:  10x | |
| *CH-1*: ON   * DC coupling * 2V/div * offset 0V | | *CH-2*: ON   * DC coupling * 20mV/div * offset -2.55V | | *CH-3*: ON   * DC coupling * 20mV/div * offset -4.35V | | *CH-4*: ON   * DC coupling * 2V/div * offset 0V |
| *Function Generator* | *CH-2*: Inactive  *CH-2*: Sine, DC offset 3.9V, Amplitude 0mV, Frequency 1kHz | | | | | | |

1. Using horizontal cursors in Manual mode, read the average DC values of the *Oscilloscope* CH-2 (*Vout*), CH-3 (*Vdr*) and CH-4 (*VdrEA*), in Volts with all decimal digits shown by the instrument, and report the values in Table 4-2-2.

Table 4-2-2 Error Amplifier voltage as function of linear regulator output voltage Vout.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *VdrDC* [V]  (Function Generator CH2 DC offset) | 3.90 | 4.00 | 4.10 | 4.20 | 4.30 | 4.40 |
| *VoutDC,nom* [V] |  | | | | | |
| *Vdr* [V] |  |  |  |  |  |  |
| *Vout* [V] |  |  |  |  |  |  |
| *VdrEA* [V] |  |  |  |  |  |  |

1. Repeat the measurement for all the values of the driver voltage *VdrDC* indicated in Table 4-2-2, by changing the DC offset of *Function Generator* CH-2.
2. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

4-2-1 Do you observe a transition in the measured values of *VdrEA* from *Vcc+* to *Vcc-* like the one you have observed with the simulations?

1. yes
2. no

what is you comment? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-2-2 If your answer to Question 4-2-1 is A, does the threshold value of the gate driver voltage *Vdr* determine the transition of *VdrEA* of *VdrEA* from *Vcc+* to *Vcc-* the same you have observed with the simulations?

1. yes
2. no

what is you comment? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-2-3 Based on your answer to Question 4-2-2, what parameter of the MOSFET model would you change to improve the accuracy of simulations? How and why?

1. Vth: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
2. β: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
3. λ: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-2-4 Run again the simulation by changing the parameters of MOSFET model and verify your predictions based on your answers to Question 4-2-3. Are the new simulation results closer to experimental ones? Do you infer a rule or a procedure to obtain the parameters of a MOSFET from experimental measurements?

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#### 4-3 Experiment 2: Instructions

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* and use the instruments configuration and setup shown in Table 4-3-1.
2. Run *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 4-3-1 Instruments initial configuration and setup

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| *Power Supply* | *CH “+”*: Static, 7.00V, *CH “-“*: Inactive | | | | | | |
| *Oscilloscope* | *Trigger*:  Immediate | *Horizontal*:  200ms/div | | *Acquisition*:  average | *Measurements*:  show | *Probe Attenuation*:  10x | |
| *CH-1*: ON   * DC coupling * 1V/div * offset -4V | | *CH-2*: ON   * DC coupling * 10mV/div * offset -2.55V | | *CH-3*: ON   * DC coupling * 10mV/div * offset -4.33V | | *CH-4*: ON   * DC coupling * 1V/div * offset -3.5V |
| *Function Generator* | *CH-1*: Inactive  *CH-2*: Sine, DC offset 4.175V, Amplitude 20mV, Frequency 1Hz | | | | | | |

1. Using horizontal cursors in Manual mode, read the DC average values of the *Oscilloscope* CH-2 (*Vout*), CH-3 (*Vdr*) and CH-4 (*VdrEA*), in Volts with all decimal digits shown by the instrument, and report the values in Table 4-3-2.
2. Using cursors in Track mode, read the peak-peak values of the *Oscilloscope* CH-2 (*Vout*), CH-3 (*Vdr*) and CH-4 (*VdrEA*), in Volts with all decimal digits shown by the instrument, calculate the ratio VdrEA,AC/VoutAC, and report the values in Table 4-3-2.

Table 4-3-2 Error Amplifier response.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *f* [Hz] (FG CH-2 Frequency) | 1 | 10 | 100 | 1000 | 10000 | 100000 |
| suggested oscilloscope time/division | 200ms/div | 20ms/div | 2ms/div | 200µs/div | 20µs/div | 2µs/div |
| suggested oscilloscope CH-4 volt/division | 1V/div | 1V/div | 100mV/div | 10mV/div | 10mV/div | 10mV/div |
| suggested oscilloscope CH-4 offset | -3.5V | -3.5V | -5.54V | -5.54V | -5.54V | -5.54V |
| *VdrDC* [V] (FG CH-2 DC offset) | 4.175 | 4.182 | 4.182 | 4.182 | 4.175 | 4.175 |
| *VdrACpp* [mV] (FG CH-2 Amplitude) | 20 | 20 | 20 | 20 | 20 | 20 |
| *VdrACpp* [mV] (Scope CH-3 Volts pk-pk) |  |  |  |  |  |  |
| VoutDC,nom [V] |  | | | | | |
| *VoutDC* [V] (Scope CH-2 Average) |  |  |  |  |  |  |
| *VoutACpp* [mV] (Scope CH-2 Volts pk-pk) |  |  |  |  |  |  |
| *VdrEA*,*DC* [V] (Scope CH-4 Average) |  |  |  |  |  |  |
| *VdrEA,ACpp* [mV] (Scope CH-4 Volts pk-pk) |  |  |  |  |  |  |
| *VdrEA,ACpp*/*VoutACpp* |  |  |  |  |  |  |
| *VdrAC/VoutAC* from Table 3-2 (simulations) |  |  |  |  |  |  |

1. Repeat the measurement for all the values of Frequency, DC Offset and Amplitude of the driver voltage *Vdr* shown in Table 4-3-2, by changing the setup of *Function Generator* CH-2. [**Notes:** **1)** if you don’t see the CH-4 trace in the scope frame, decrease the DC offset *VdrDC*, with respect to the values shown in Table 4-3-2, in steps of -1mV, until the CH-4 sets in the frame; **2)** while measuring peak-peak voltage values, do not consider the high-frequency noise appearing as a rapid up-and-down swinging signal around the main sinusoidal waveform].
2. Enter in Table 4-3-2 the *VdrAC/VoutAC* values collected in Table 3-2.
3. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

4-3-1 Do you observe the same trend in the measured and simulated ratio *VoutAC*/*VinAC* as the frequency increases?

1. yes
2. no

if your answer is B, why? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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4-3-2 Should the error amplifier exhibit a different ratio *VdrAC/VoutAC* with *Co* = 11µF?

1. yes
2. no

why?: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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#### Troubleshooting tips:

* If the simulated and measured results do not match, verify the setup and connections of instruments, and restart the experiment.

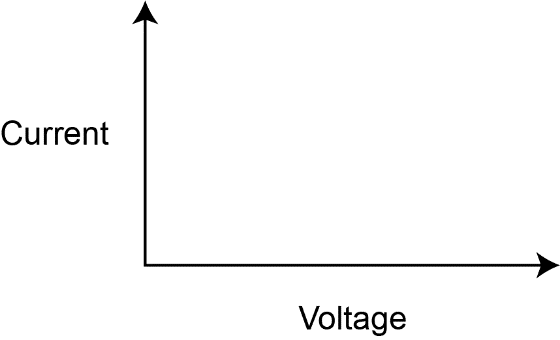
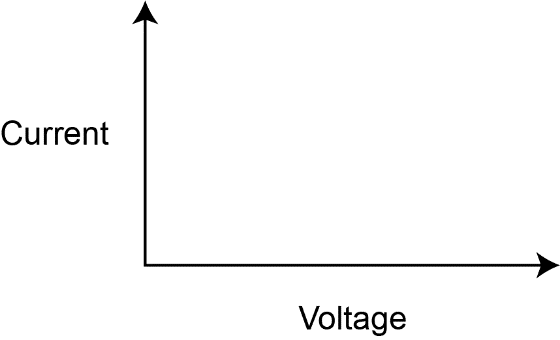
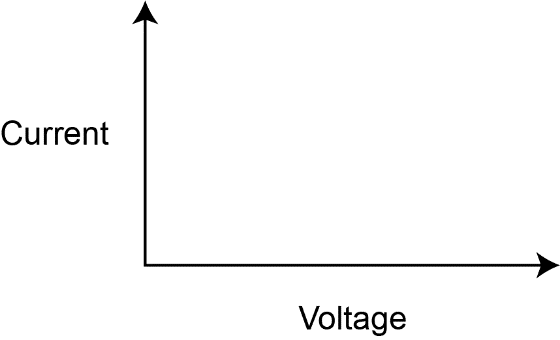
### **5 Analyze**

5-1 Using the results collected in Table 4-3-2, calculate the ratios *Gdr* = *VoutAC/VdrAC*, *GEA* = *VdrEA,AC/VoutAC* and *Tloop* = *GEAGdr* = *VdrEA,AC/VdrAC*, report the results in Table 5-1, and graph the values of ratios *Gdr*, *GEA* and *Tloop* as a function of the frequency *f* using a logarithmic scale for the horizontal axis and decibel scale for the vertical axis, including a legend that indicates which line style corresponds to which series (calculations, measurements).

Table 5-1 Error Amplifier response.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| f [Hz] | 1 | 10 | 100 | 1000 | 10000 | 100000 |
| *Gdr* = *VoutAC/VdrAC* |  |  |  |  |  |  |
| *GEA* = *VdrEA,AC/VoutAC* |  |  |  |  |  |  |
| *Tloop* = *VdrEA,AC/VdrAC* |  |  |  |  |  |  |

*Gdr*

f [Hz]

f [Hz]

*Tloop*

*GEA*

f [Hz]

Figure 5-1 Calculated and measured values of ratios VoutAC/VinAC and VoutAC/VdrAC obtained while varying the frequency, with the MOSFET operating in the saturation region

The ratio *Gdr* is the open loop *control-to-output* gain of the linear regulator, which expresses the sensitivity of the output voltage with respect to the gate driver voltage perturbations (see **Lab2**). The ratio *GEA* is the gain of the error amplifier, which expresses the sensitivity of the error amplifier voltage with respect to the output voltage perturbations (see **Theory and Background** section). The ratio *Tloop* is the loop gain of the linear regulator, which expresses the global sensitivity of the linear regulator to AC perturbations. A higher value of the loop gain involves a higher reactivity of the linear regulator to disturbances, which results in a more effective suppression of the disturbances and in a better output voltage regulation capability.

5-2 Based on the loop gain plot *Tloop* you have plotted in Figure 5-1, for what of the frequency values is the linear regulator better suppressing the disturbance effects?

1. 60Hz
2. 6kHz
3. 60kHz

5-3 Based on your observations and on the equations provided in the **Theory and Background** section, how would you modify the parameters *f0*, *fZ*, *fP* and *Adc* of the error amplifier to improve the disturbance suppression capability of the linear regulator?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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### **6 Conclusion**

### 6-1 Summary

Write a summary of what you observed and learned about the AC response of the error amplifier of a linear regulator, regarding its sensitivity with respect to output voltage AC perturbations. Discuss the parameters influencing the AC response of the error amplifier, in what frequency range is it important to have a high error amplifier gain, why, and how you can achieve it.

### 6-2 Expansion Activities

1. Using the Multisim Live schematic of Figure 3-1, determine the frequency response of the linear regulator and of the error amplifier, by means of the *AC Sweep* option:
   1. Set the switches J4 and J6 to be closed.
   2. Replace the *Vdr* DC generator with an AC generator and set VO=4.0746V, Freq=1Hz, VA=0.1V.
   3. Set AC\_mag = 0.1V in the *AC analysis value* menu option of the voltage generator *Vdr*.
   4. Set AC\_mag = 0 V in the *AC analysis value* menu option of the voltage generator *Vin*.
   5. Set Start freq. = 1Hz and Stop freq. = 1MHz in the *Configuration Panel*.
   6. Set *Show plots* box unchecked on probe *Vin*.
   7. Run the simulation and watch the resulting AC Sweep plots (Bode plots). The continuous lines are the magnitudes of the ratios *Gdr* = *VoutAC/VdrAC*, *Tloop* = *GEAGdr* = *VdrEA,AC/VdrAC*, while the dashed line is the phase shift between *VoutAC* and *VdrEA,AC* with respect to *VdrAC* over the selected frequency range.
   8. Verify that the plots follow the trend of results of Tables 3-2, 4-3-2 and 5-1.
2. Observe the behavior of an error amplifier with a higher gain, using the circuit schematic of Figure 3-1.
3. Open the switches J4 and J6. The resulting gain of the error amplifier will be:

*Equation 6-2-1* 

The pole frequency *f0* of the error amplifier is now given by *f0* =1/(*Ri1Cf1*) = 104kHz (*Type I* error amplifier), and consequently *fLPF* = 10.4Hz.

1. Open switches J4 and J6.
2. Repeat the simulations in the test conditions listed in Table 3-2 (use *VA*=100mV with *Freq* = 1Hz, 10Hz, 100Hz, for generator *Vin*).
3. Compare and discuss the results of simulations obtained with the two different error amplifier setup.
4. Verify experimentally the effect of a higher error amplifier gain
5. Open the jumpers J60 and J62 in the **Discrete Linear Section** of TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.
6. Test the regulator with Frequency = 10kHz, Amplitude = 30mVpp and DC offset = 4.328V on *Function Generator* CH-2, set the *Oscilloscope* CH-4 with AC coupling, 500mV/div, 0V offset, 50us/div.
7. Compare the error amplifier gain with the corresponding result reported in Table 4-3-2.

### 6-3 Resources for learning more

* This book provides the fundamentals of linear regulators control:

C.Basso, *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide*, Artech House

## Answer Key – Check Your Understanding Questions Only



Check Your Understanding

1-1 C

1-2 A

1-3 C

1-4 B

1-5 Increase *f0*, increase *Adc*

## Lab 4: Linear Regulator in Closed Loop Operation

The goal of this lab is to analyze the closed loop operation of a linear regulator. We investigate the impact of the loop gain on the ability to reject noise and changes in the output voltage, which is the most important feature of linear regulators. First, we will review the principle of operation and the simplified model of a closed loop linear regulator. Next, we will use the simplified model to predict its response to AC perturbations and its accuracy to the reference signal. Then, we will simulate the linear regulator in DC and AC operation to evaluate the impact of the MOSFET and error amplifier parameters. Finally, we will perform experimental tests with a real linear regulator, and will compare the results of simulations and measurements to verify their consistency.

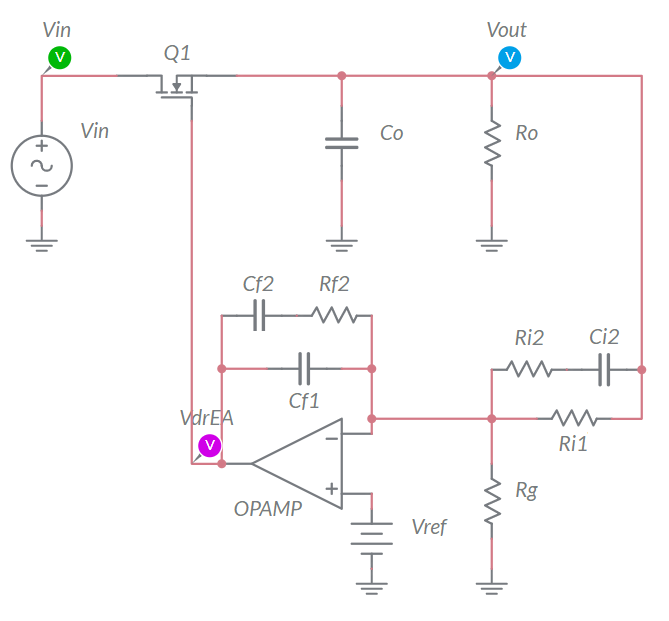


Figure 1-1. Closed Loop Linear Regulator.

## Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a linear regulator and its MOSFET and error amplifier characteristics, you will calculate the DC operating point and the AC response to input and reference voltage perturbations, with specified units and accuracy, by applying the appropriate theoretical formulae.
2. Given a linear regulator and its MOSFET and error amplifier characteristics, you will simulate the DC and AC operation with different error amplifier configurations, to determine the accuracy of theoretical model predictions, by comparing the appropriate sets of data and results
3. Given a real linear regulator, a dynamic power supply, and a function generator, you will measure the accuracy of the DC output voltage with respect to the desired nominal value, you will determine the AC response of the linear regulator, and you will determine the elements influencing the accuracy of simulations, by comparing the appropriate sets of data and results.

## Required Tools and Technology

|  |  |
| --- | --- |
| Platform: NI ELVIS III Instruments used in this lab:   * Function generator * Oscilloscope * Power Supply   **Note**: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments. ​ | * Access Instruments   https://measurementslive.ni.com/   * View User Manual http://www.ni.com/en-us/support/model.ni-elvis-iii.html * View Tutorials   <youtube link> |
| Hardware: TI Power Electronics Board | * View User Manual   http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html |
| Software: NI Multisim Live | * Access   <https://www.multisim.com/>   * View Tutorial   https://www.multisim.com/get-started/ |
| Software: TI Power Electronics Configuration Utility | * Download (Windows OS Only)   http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip   * Note: Mac Version will be available soon |

## Expected Deliverables

In this lab, you will collect the following deliverables:

* Calculations based on equations provided in the Theory and Background Section
* Results of circuit simulations performed by means of Multisim Live
* Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
* Observations on simulations and experiments
* Answers to questions

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

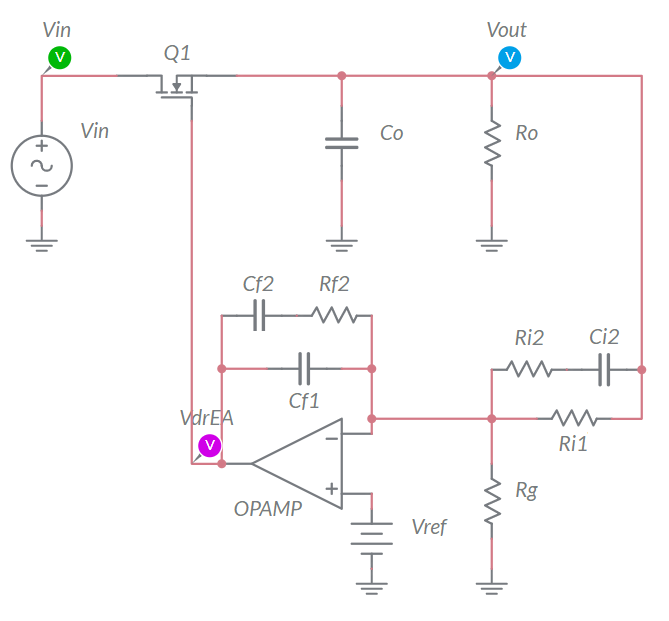
## 1 Theory and Background

1-1 Introduction.

In this section, we review the fundamental concepts and equations of a linear regulator in closed loop operation. We will discuss the impact of OPAMP and error amplifier characteristics on DC offset error and the noise rejection capability of the linear regulator.

1-2 Feedback Action of the Error Amplifier.

Figure 1-2 shows a linear regulator in closed loop operation. The error amplifier consists of the OPAMP, the voltage reference *Vref*, the capacitors {*Cf1*,*Cf2*,*Ci2*}, and the resistors {*Rg*,*Ri1*,*Ri2*,*Rf2*}. The error amplifier compares the output voltage *Vout* to the desired DC nominal value *VoutDC,nom*, and generates the gate driver voltage *VdrEA* ensuring that *Vout* = *VoutDC,nom*. Thanks to the error amplifier, the linear regulator is able to reject the AC noise, thus ensuring a well regulated low-noise output voltage, which is the most important feature of linear regulators. The components {*Cf1*,*Cf2*,*Ci2*} and {*Rg*,*Ri1*,*Ri2*,*Rf2*} set the poles and zeros of the error amplifier, and determine its sensitivity to noise.



error amplifier

Figure 1-2. Linear Regulator in Closed Loop Operation.

1-3 Closed Loop DC Analysis of the Linear Regulator

The DC output voltage *VoutDC* of a linear regulator is determined by the DC source voltage *VinDC* and by the DC gate driver voltage *VdrDC*. The MOSFET of a linear regulator normally operates in the saturation region, where we have:

*Equation 1-3-1* 

*Vth*, *β* and λ are the MOSFET gate-to-source threshold voltage, transconductance and channel-length-modulation coefficient, respectively. The DC error amplifier voltage is:

*Equation 1-3-2* 

where *Adc* is the error amplifier DC gain and *H*=(*1*+*Ri1*/*Rg*)-1 is the voltage sensor gain. Combining Equations 1-3-1 and 1-3-2 provides the linear regulator DC output voltage:

*Equation 1-3-3* 

As the open loop DC gain *Adc* of the OPAMP is normally very high (from 103 to 106), Equation 1-3-3 can be simplified as shown in Equation 1-3-4:

*Equation 1-3-4* 

An unlimited DC gain *Adc* = ∞ would determine an output voltage *VoutDC* equal to:

*Equation 1-3-5* 

Equations 1-3-4 and 1-3-5 highlight that the tolerance of *Vref*, *Rg* and *Ri1* influence the output voltage nominal value *VoutDC,nom*. Based on Equations 1-3-4 and 1-3-5, the output voltage offset error of a linear regulator is given by Equation 1-6:

*Equation 1-3-6* 

1-4 Closed Loop AC Analysis of the Linear Regulator

The ratio between the amplitude of the AC perturbations on the output voltage of a linear regulator and the AC perturbations on the source voltage and gate driver voltage in open loop operation is given by Equation 1-4-1 (see **Lab2**):

*Equations 1-4-1* 



where λ is the MOSFET channel-modulation coefficient. The corner frequency *ft* is the open loop bandwidth of the linear regulator. The error amplifier AC gain *GEA,AC* = *VdrAC*/*VoutAC* is given by the simplified Equation 1-4-2 (see **Lab3**):

*Equation 1-4-2* 

Equation 1-4-2 highlights that a higher pole frequency *f0* increases the error amplifier sensitivity with respect to output voltage AC perturbations. Combining Equations 1-4-1 and 1-4-2 results in the simplified closed loop Equation 1-4-3:

*Equation 1-4-3* 

where *Tloop = GEA,ACGdr* is the loop gain of the linear regulator, and the *Gin,CL* gain expresses the noise rejection capability of the linear regulator. The inverse of *Gin,CL* is the *Power Supply Rejection Ratio* (*PSRR*). From Equation 1-4-1 we see that the magnitude of the control-to-output gain *Gdr* is determined by the DC operating point, the MOSFET parameters, the load *Ro* and the capacitor *Co*, and it is flat for frequency *f* < *ft*. This results in a poor open loop noise rejection capability of the linear regulator at low frequency. From Equation 1-4-2 we see that the magnitude of the error amplifier gain is determined by the pole frequency *f0* and that it can be very high at low frequency, depending on the OPAMP DC open loop gain *Adc* and on the setup of the pole frequency *f0*. Equation 1-4-3 highlights that, given the DC operating conditions and the MOSFET characteristics, a high loop gain magnitude improves the linear regulator AC noise rejection capability. The loop gain of the linear regulator at low frequency is determined by the OPAMP dc open loop gain and by the error amplifier frequency pole frequency *f0*.

Check Your Understanding

*Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all “Check your Understanding” questions at the end of the lab.*

1-1 What parameters of a linear regulator determine the nominal value of its DC output voltage?

1. the MOSFET transconductance and gate-to-source threshold voltage
2. the error amplifier pole and OPAMP dc gain *Ad*
3. the reference voltage and the voltage sensor gain

1-2 What parameter of a linear regulator determine its DC output voltage offset error?

1. the MOSFET transconductance *β*
2. the error amplifier pole frequency *f0*
3. the OPAMP open loop dc gain *Adc*

1-3 At what frequency is the open loop linear regulator more sensitive to AC noise?

1. below the open loop bandwidth
2. above the open loop bandwidth
3. at any frequency

1-4 What parameters majorly influence the closed loop AC noise rejection capability of a linear regulator?

1. the reference voltage and the voltage sensor gain
2. the MOSFET transconductance and gate-to-source threshold voltage
3. the error amplifier pole frequency *f0* and OPAMP dc gain *Adc*

1-5 Based on your answers to Questions 1-1 to 1-4, what actions would you make to design a linear regulator with good DC accuracy and AC noise rejection capability?

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## 2 Exercise

The **Discrete Linear Section** in the TI Power Electronics Board for NI ELVIS III is based on the following setup:

* MOSFET*:* TI’s CSD15380F3, assume *Vth* = 1.35V, *β* = 0.24A/V2, *λ* =0.05V**-1**
* OPAMP: TI’s OPA835IDBVR, assume *Adc*=106, *Vcc+*=5.5V, *Vcc-*=0V.
* VOLTAGE REFERENCE: TI’s LM4140, assume *Vref*=1.024V±0.1%.
* ERROR AMPLIFER SETUP*: f0* = 3.28kHz, *Ri1*=39.2kΩ±1%, *Rg*=26.1kΩ±1%.

TI’s devices datasheets are available at the following links:

* CSD15380F3 MOSFET: <http://www.ti.com/lit/ds/symlink/csd15380f3.pdf>
* OPA835IDBVR OPAMP: <http://www.ti.com/lit/ds/symlink/opa835.pdf>
* LM4140 VOLTAGE REFERENCE: <http://www.ti.com/lit/ds/symlink/lm4140.pdf>

2-1 Calculate the ideal, minimum and maximum values of the nominal value of the DC output voltage *VoutDC,nom*, in Volts with four decimal digits, considering the tolerances of parameters:

ideal *VoutDC,nom* = 2.5219V ; min *VoutDC,nom* = 2.5297V ; max *VoutDC,nom* = 2.5956V.

2-2 Calculate the DC offset error of the output voltage, in micro Volts with three decimal digits, in the ideal, minimum and maximum nominal DC output voltage conditions determined with previous step 2-1:

*ERRDC* @ min *VoutDC,nom* = -6.573µV; *ERRDC* @ max *VoutDC,nom* = -6.252µV;

*ERRDC* @ ideal *VoutDC,nom* = -6.410µV;

2-3 Calculate the open loop bandwidth *ft* of the linear regulator, in Hz, with *Co=*1µF and *Co=*11µF, assuming *VinDC* = 5V and *VoutDC* = 2.5V:

*ff* @ *Co=*1µF = 17250Hz ; *ff* @ *Co=*11µF = 1568Hz

2-4 You have a source voltage with a 5V DC component and an AC noise *VinACsin*(2*πf∙t*), where *VinAC* = 1V and the frequency *f* can have the values listed in Table 2-1. Assuming *VoutDC* = 2.5V and *Co=*1µF, calculate the ratio *VoutAC/VinAC*, in the format XXX.XXXE-03, and the value of the amplitude *VoutAC* of the AC voltage *VoutACsin*(2*πf∙t+θ*), in milli Volts with three decimal digits, under a) open loop and b) closed loop conditions, and report the results in Table 2-1.

Table 2-1 Analysis of linear regulator AC noise rejection capability in open loop and closed loop operation.

|  |  |  |  |
| --- | --- | --- | --- |
| *f* [Hz] | 10 | 100 | 1000 |
| open loop *VoutAC/VinAC* |  |  |  |
| closed loop *VoutAC/VinAC* |  |  |  |
| open loop *VoutAC* [mV] |  |  |  |
| closed loop *VoutAC* [mV] |  |  |  |

2-5 Based on the results of your calculations, do you observe and improvement in the AC noise rejection capability of the linear regulator in closed loop operation compared to open loop operation?

1. yes
2. no

Please provide your comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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2-6 What parameter would you change to improve the low frequency rejection capability, and how?

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## 3 Simulate

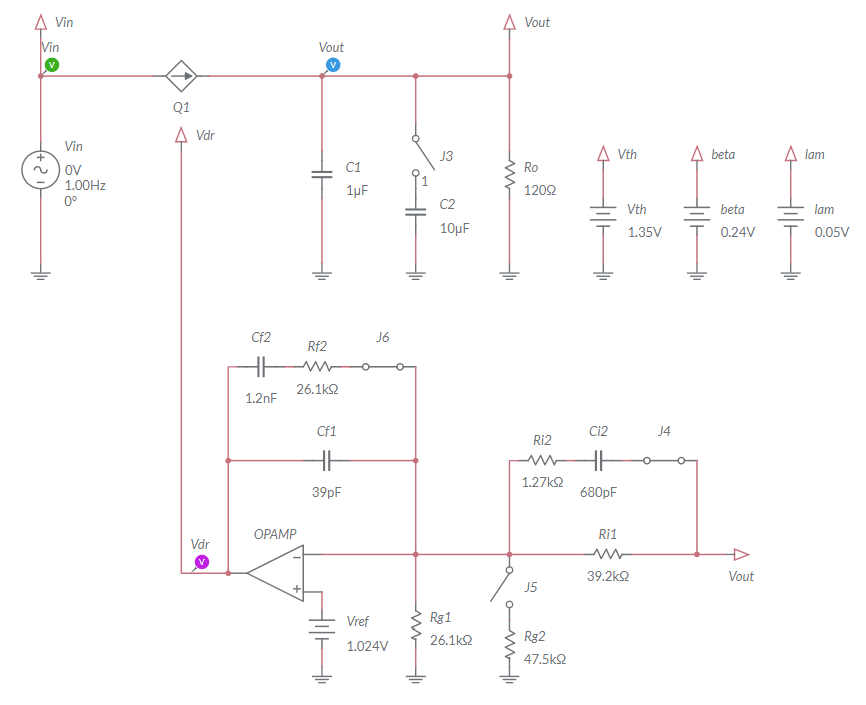
The simulations you will perform in this section allow you to analyze the closed loop behavior of an error amplifier. First, you will observe the DC output voltage and determine the DC offset error with respect to the nominal value. Next, you will observe the error amplifier voltage and compare it with the theoretical value required to achieve the desired output voltage. Finally, you will analyze the impact of output capacitor and error amplifier setup on the AC noise rejection capability of the linear regulator in closed loop operation.

#### 3.1 Simulation 1: Instructions

1. Open *Lab4 – Linear Regulator in Closed Loop Operation* from the file path:

<https://www.multisim.com/content/x2h5e2JkYifsnyFNTDZu95/lab-4-closed-loop-linear-regulator-oparation/>

The circuit shown in Figure 3-1 is used for simulating the DC and AC linear regulator closed loop operation.



error amplifier

Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Linear Regulator in Closed Loop Operation.

The error amplifier generates the gate driver voltage *Vdr*. The source voltage *Vin* includes a DC component and an AC perturbation. The parameters {*VA*, *Freq*, *VO*} of the generator *Vin* correspond to the parameters {*VinAC*, *f*, *VinDC*} as defined in the **Theory and Background** section. The auxiliary generators *Vth*, *beta* and *lam* allow to set the MOSFET parameters {*Vth*, *β*, *λ*}, respectively. The error amplifier pole frequency is *f0* = 1/(*Ri1*(*Cf1*+*Cf2*)) = 3.3kHz with switches J4 and J6 closed (Type III error amplifier), and *f0* = 1/(*Ri1Cf1*) =104kHz with jumpers J4 and J6 open (Type I error amplifier). The OPAMP is characterized by a dc gain *Adc*=106.

1. Set the switches J3 and J5 to be OPEN, and the switches J4 and J6 to be CLOSED.
2. Select the *Interactive* simulation option and the *Split* visualization option.
3. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
4. Check the *Instantaneous* option box for voltage probes *Vin*, *Vout*, and *Vdr* in the *Measurement labels* menu.
5. Calculate the nominal value *VoutDC,nom* in Volts with three decimal digits, and report the result in Table 3-1.
6. Set *VA*=0, *Freq*=10Hz for the generator *Vin*.
7. For each value of DC source voltage *VinDC* (*VO* voltage of the generator *Vin*) listed in Table 3-1, run the simulation, read the measurements of voltage probes *Vout* and *Vdr* in Volts with four decimal digits and report the results in Table 3-1.

Table 3-1 DC Output Voltage and Error Amplifier Voltage as function of DC Source Voltage.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *VinDC* (VO) [V] | 4.0 | 4.5 | 5.0 | 5.5 | 6.0 |
| *VoutDC,nom* [V] |  | | | | |
| *VoutDC* [V] |  |  |  |  |  |
| *VdrDC* [V] |  |  |  |  |  |

3-1-1 Does the DC output voltage *VoutDC* change as *VinDC* increases?

1. yes
2. no

Discuss the results based on the **Theory and Background** section equations:

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3-1-2 Does the error amplifier voltage *Vdr*  change as *VinDC* increases?

1. yes
2. no

Discuss the results based on the **Theory and Background** section equations:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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3-1-3 What change do you expect in the simulation results if you open the switches J4 and J6? why?

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3-1-4 What change do you expect in the simulation results if you close the switch J3 or J5? why?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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#### 3.2 Simulation 2: Instructions

1. Open *Lab4 – Linear Regulator in Closed Loop Operation* from the file path:

<https://www.multisim.com/content/x2h5e2JkYifsnyFNTDZu95/lab-4-closed-loop-linear-regulator-oparation/>

1. Set the switches J3 and J5 to be OPEN, and the switches J4 and J6 to be CLOSED.
2. Select the *Interactive* simulation option and the *Split* visualization option.
3. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
4. Check the *Periodic* option box for voltage probes *Vin*, *Vout*, and *Vdr* in the *Measurement labels* menu.
5. Set *VA*=1V, *Freq*=10Hz, *VO*=5V for the generator *Vin* and run the simulation.
6. Read the DC average measurement *VAV* and the AC peak-to-peak measurement *Vpp* of *Vout* voltage probe and report the values of *VoutDC* *= VAV* (in Volts with four decimal digits) and *VoutAC* (in milli Volts with three decimal digits) in Table 3-2.
7. Read the DC average measurement *VAV* and the AC peak-to-peak measurement *Vpp* of *Vdr* voltage probe and report the values of *VdrDC* *= VAV* (in Volts with four decimal digits) and *VdrAC* (in milli Volts with three decimal digits) in Table 3-2.
8. Repeat steps 7-8 under all *Vin* frequency and amplitude conditions of Table 3-2.

Table 3-2 Linear regulator AC response with Co=1μF.

|  |  |  |  |
| --- | --- | --- | --- |
| f [Hz] (Vin Freq) | 10 | 100 | 1000 |
| VinAC [Hz] (Vin VA) | 0.5 | 0.5 | 0.5 |
| ML Simulation Max. Time Step | 1e-5 | 1e-6 | 1e-7 |
| ML Grapher Horizontal Axis | 50ms/div | 5ms/div | 500us/div |
| VoutDC,nom [V] |  | | |
| VoutDC [V] |  |  |  |
| VoutAC [mV] |  |  |  |
| VdrDC [V] |  |  |  |
| VdrAC [mV] |  |  |  |

3-2-1 Does the DC output voltage *VoutDC* change as the source voltage noise frequency increases?

1. yes
2. no

Discuss the results based on the **Theory and Background** section equations:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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3-2-2 Does the amplitude *VoutAC* of the AC output voltage noise change as the source voltage noise frequency increases?

1. yes
2. no

Discuss the results based on the **Theory and Background** section equations:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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3-2-3 What change do you expect if you open the switches J4 and J6? why?

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3-2-4 What change do you expect if you close the switch J3 or J5? why?

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Troubleshooting tips:

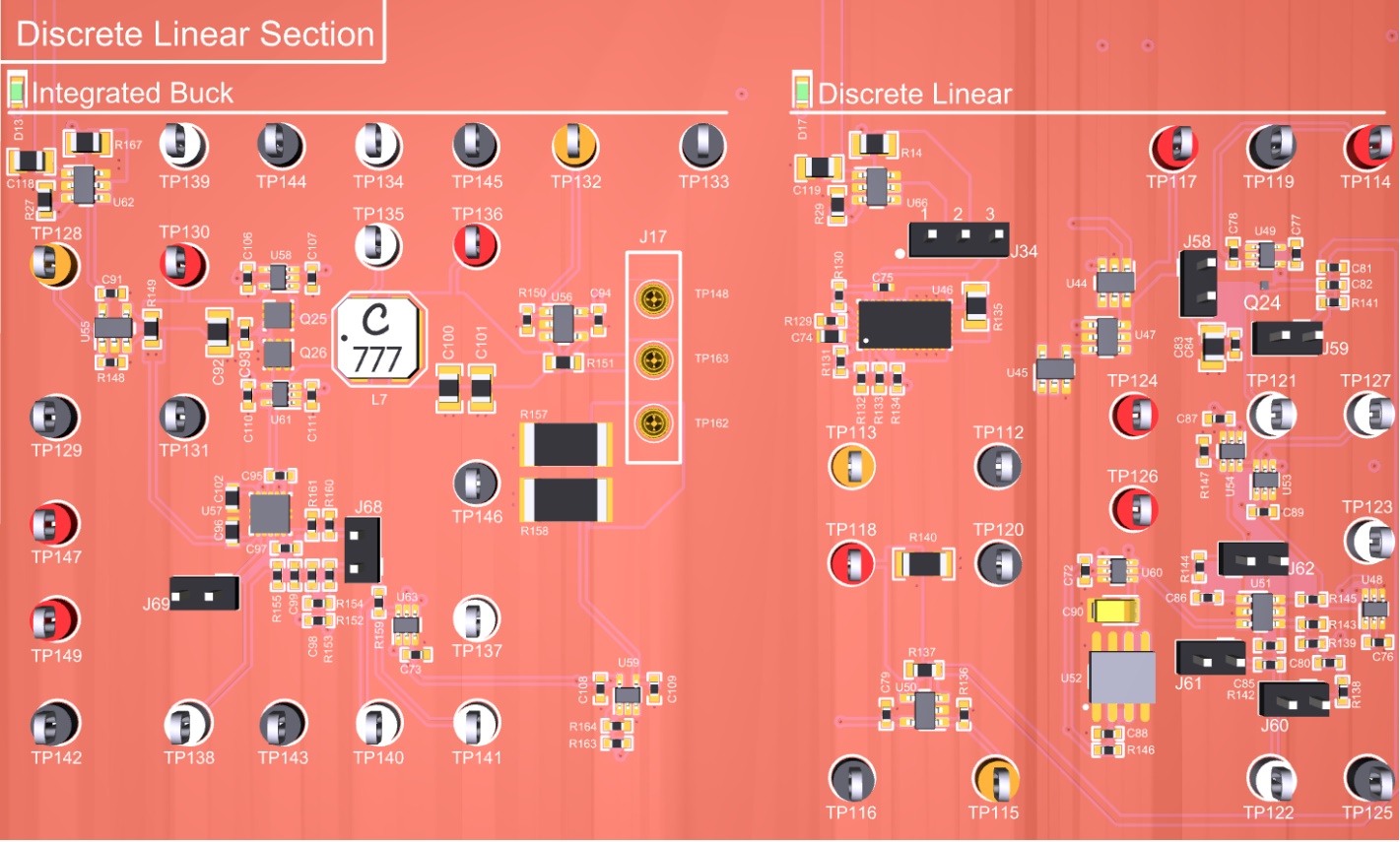
* If the simulation does not run and you get some error message, reload *Lab4 – Linear Regulator in Closed Loop Operation* from this file path:

<https://www.multisim.com/content/x2h5e2JkYifsnyFNTDZu95/lab-4-closed-loop-linear-regulator-oparation/>

and restart the simulation, following the instructions.

### **4 Implement**

The experiments of this section allow you to observe the behavior of a real linear regulator in closed loop operation. First, you will analyze the DC operating point of the linear regulator while varying the DC source voltage. Next, you will measure the AC output voltage generated by the AC noise of the source voltage. Finally, you will determine the impact of the error amplifier setup on the AC noise rejection capability of the linear regulator. The experiments are performed by means of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1, using the TI’s CSD15380F3 MOSFET as pass device and TI’s OPA835IDBVR OPAMP as error amplifier. The linear regulator is powered by a TI’s TPS40303DRCR Integrated Buck regulator, generating a 5V DC voltage and an AC noise.



***J17***

***J69***

***VFB***

***J68***

***J59***

***Ro***

***Vdr***

***J62***

***Vout***

***J60***

***J61***

***J58***

***Iout***

***Ta***

***Vin***

***MOSFET***

***J34***

Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of Linear Regulator in Closed Loop Operation

TI’s devices datasheets are available at the following links:

CSD15380F3 MOSFET: <http://www.ti.com/lit/ds/symlink/csd15380f3.pdf>

OPA835IDBVR OPAMP: <http://www.ti.com/lit/ds/symlink/opa835.pdf>

TPS40303DRCR Buck Regulator: <http://www.ti.com/lit/ds/symlink/tps40303.pdf>

The error amplifier pole frequency is *f0* = 1/(*Ri1*(*Cf1*+*Cf2*)) = 3.3kHz with jumpers J60 and J62 shorted (Type III error amplifier), and *f0* = 1/(*Ri1Cf1*) =104kHz with jumpers J60 and J62 open (Type I error amplifier). The output capacitance *Co* is 1µF with jumper J59 open, and 11µF with jumper J59 shorted. The nominal output voltage is 2.5V with jumper J61 open, and 3.3V with jumper J61 shorted.

#### 4-1 General Instructions

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to the tolerances of components on the TI Power Electronics Board]

1. Open *Variable Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: <http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/>
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: <http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html>
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open NI ELVIS III *PE Lab User Interface* (See Required Tools and Technology section for download instructions), and select *Lab4 – Linear Regulator in Closed Loop Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.
6. Connect the instruments as indicated in Table 4-2.

Table 4-1 Jumpers setup

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| J17 | J34 | J58 | J59 | J60 | J61 | J62 | J68 | J69 |
| short TP148-TP163 | short 2-3 | open | open | short | open | short | short | open |

Table 4-2 Instruments connections

|  |  |
| --- | --- |
| *Power Supply* | connect to red and black banana connectors |
| *Oscilloscope* | connect CH-1 to TP117 (input voltage *Vin*)  connect CH-2 to TP118 (output voltage *Vout*)  connect CH-3 to TP121 (gate driver voltage *Vdr*) |
| *Function Generator* | connect CH-1 to FGEN1 BNC connector (→TP137 = Integrated Buck output voltage control) |

#### 4-2 Experiment 1: Instructions

1. Use the instruments configuration and setup shown in Table 4-2-1.

Table 4-2-1 Instruments initial configuration and setup

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| *Power Supply* | *CH “+”*: Static, 7.00V, *CH “-“*: Inactive | | | | | | |
| *Oscilloscope* | *Trigger*:  Immediate | *Horizontal*:  100us/div | | *Acquisition*:  average | *Measurements*:  show | *Probe Attenuation*:  10x | |
| *CH-1*: ON   * DC coupling * 2V/div * offset 0V | | *CH-2*: ON   * DC coupling * 2V/div * offset 0V | | *CH-3*: ON   * DC coupling * 2V/div * offset 0V | | *CH-4*: OFF |
| *Function Generator* | *CH-1*: Sine, DC offset 735mV, Amplitude 0mV, Frequency 10Hz | | | | | | |

1. Run *Power Supply*, *Function Generator* and *Oscilloscope*.
2. Read the average DC values of the *Oscilloscope* CH-2 (*Vout*) and CH-3 (*Vdr*) and CH-4 (*VdrEA*), using the cursors in Track mode, and report the values in Table 4-2-2, with two decimal digits.
3. Repeat the measurement for all the values of the driver voltage *VdrDC* indicated in Table 4-2-2, by changing the DC offset of *Function Generator* CH-2.
4. Import in Table 4-2-2 the DC values of *VoutDC* and *VdrDC* collected in Table 3-1, in Volts with two decimal digits.
5. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

Table 4-2-2 Linear regulator DC output voltage and gate driver voltage as function of DC input voltage.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Function Generator CH1 DC offset [mV] | 735 | 670 | 600 | 540 | 470 |
| *VoutDC,nom* [V] |  | | | | |
| *VinDC* [V] |  |  |  |  |  |
| *VoutDC* [V] |  |  |  |  |  |
| *VoutDC* [V] from Table 3-1 |  |  |  |  |  |
| *VdrDC* [V] |  |  |  |  |  |
| *VdrDC* [V] from Table 3-1 |  |  |  |  |  |

4-2-1 Is the DC output voltage *VoutDC* trend, as *VinDC* increases, similar between simulations and measurements? what are the differences between the measured and simulated values?

1. yes
2. no

Discuss the possible origin of differences between simulations and experiments based on the **Theory and Background** section equations:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-2-2 Is the gate driver voltage *VdrDC* trend, as *VinDC* increases, similar between simulations and measurements? what are the differences between the measured and simulated values?

1. yes
2. no

Discuss the possible origin of differences between simulations and experiments based on the **Theory and Background** section equations:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-2-3 Based on your answer to Questions and 4-2-1 and 4-2-2, what parameter of the linear regulator model would you change to improve the accuracy of simulations? How and why?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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#### 4-3 Experiment 2: Instructions

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* and use the instruments configuration and setup shown in Table 4-3-1.

Table 4-3-1 Instruments initial configuration and setup

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| *Power Supply* | *CH “+”*: Static, 7.00V, *CH “-“*: Inactive | | | | | | | |
| *Oscilloscope* | *Trigger*: CH-1  Analog edge,  set to 50% | *Horizontal*:  50ms/div | | *Acquisition*:  average | | *Measurements*:  show | | *Probe Attenuation*:  10x |
| *CH-1*: ON   * DC coupling * 2V/div * offset -0V | | *CH-2*: ON   * DC coupling * 10mV/div * offset -2.55V | | *CH-3*: ON   * DC coupling * 10mV/div * offset -4.25V | | *CH-4*: OFF | |
| *Function Generator* | *CH-1*: Sine, DC offset 610mV, Amplitude 135mV, Frequency 10Hz  *CH-2:* Inactive | | | | | | | |

1. Run *Power Supply*, *Function Generator* and *Oscilloscope*.
2. Read the DC average values of the *Oscilloscope* CH-2 (*Vout*) and CH-3 (*Vdr*) and report the values in Table 4-3-2, with two decimal digits.
3. Read the peak-peak values of the *Oscilloscope* CH-2 (*Vout*) and CH-3 (*Vdr*) with two decimal digits, divide by 2 and report the values in Table 4-3-2.
4. Repeat the measurement for all the values of Frequency, DC Offset and Amplitude of the *Function Generator* CH-1 indicated in Table 4-3-2
5. Import in Table 4-3-2 the values of *VoutDC* and *VdrDC* collected in Table 3-2, in Volts with two decimal digits, and the values of *VoutAC* and *VdrAC* collected in Table 3-2, in milli Volts with the same decimal digits of the corresponding measured data.
6. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

Table 4-3-2 Error Amplifier response.

|  |  |  |  |
| --- | --- | --- | --- |
| Function Generator CH-1 Frequency [Hz] | 10 | 100 | 1000 |
| Function Generator CH-1 Amplitude [mV] | 135 | 135 | 135 |
| Function Generator CH-1 DC offset [mV] | 600 | 600 | 600 |
| VoutDC,nom [V] |  | | |
| Scope CH-2 Average VoutDC [V] |  |  |  |
| VoutDC from Table 3-2 [V] |  |  |  |
| Scope CH-2 Volts Vpk-pk/2 = VoutAC [mV] |  |  |  |
| VoutAC from Table 3-2 [mV] |  |  |  |
| Scope CH-3 Average VdrDC [V] |  |  |  |
| VdrDC from Table 3-2 [V] |  |  |  |
| Scope CH-3 Volts Vpk-pk/2 = VdrAC [mV] |  |  |  |
| VdrAC from Table 3-2 [mV] |  |  |  |

4-3-1 Is the AC output voltage *VoutAC* trend, as the frequency *f* increases, similar between simulations and measurements? what are the differences between the measured and simulated values?

1. yes
2. no

Discuss the possible origin of differences between simulations and experiments based on the **Theory and Background** section equations:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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4-3-2 Is the gate driver voltage *VdrAC* trend, as *VinAC* increases, similar between simulations and measurements? what are the differences between the measured and simulated values?

1. yes
2. no

Discuss the possible origin of differences between simulations and experiments based on the **Theory and Background** section equations:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4-3-3 Based on your answer to Questions and 4-3-1 and 4-3-2, what parameter of the linear regulator model would you change to improve the accuracy of simulations? How and why?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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#### Troubleshooting tips:

* If the simulated and measured results do not match, verify the setup and connections of instruments, and restart the experiment.

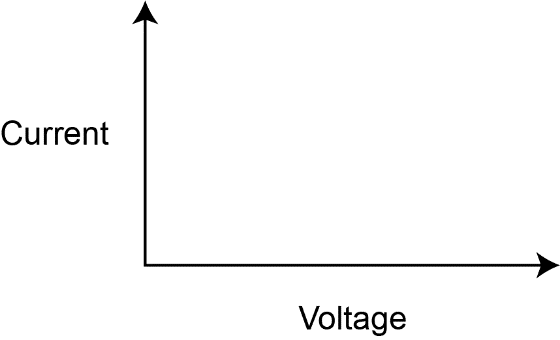
### **5 Analyze**

5-1 Using the results collected in Table 4-3-2, calculate the value in decibel of the Power Supply Rejection Ratio *PSRRdB* = 20log10(*VinAC*/*VoutAC*), with one decimal digit, at each frequency and report the results in Table 5-1. Graph the *PSRRdB* values as a function of the frequency *f* using a logarithmic scale for the horizontal axis and decibel scale for the vertical axis. Include a legend that indicates which line style corresponds to which series (calculations, measurements).

Table 5-1 Closed Loop Power Supply Rejection Ratio.

|  |  |  |  |
| --- | --- | --- | --- |
| f [Hz] | 10 | 100 | 1000 |
| *PSRRdb* = 20 log10(*VinAC*/*VoutAC*) |  |  |  |

*PSRRdB*



f [Hz]

Figure 5-1 PSRR Values Obtained with Different Setup of the Closed Loop Linear Regulator.

5-2 Based on your learning, discuss the trend of *PSRRdb* you observe and indicate what parameter of the linear regulator would you change to improve PSRR at high frequency:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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### **6 Conclusion**

### 6-1 Summary

Write a summary of what you observed and learned about the closed loop operation of a linear regulator, regarding its DC accuracy and noise rejection capability with respect to source voltage AC perturbations. Discuss the conditions and the parameters influencing the closed loop response of the linear regulator, and how you can improve the Power Supply Rejection Ratio.

### 6-2 Expansion Activities

1. The parameters *Vth*, *β* and *λ* of the MOSFET model are characterized by a tolerance determined by manufacturing processes, and they depend on the MOSFET junction temperature. Assuming that:

* the value of *Vth* can range between 0.85V and 1.35
* the value of *β* can range between 0.19V and 0.33
* the value of *λ* can range between 0.01V and 0.05

1. Determine the combination of values of MOSFET parameters that would improve the linear regulator PSRR.
2. Use Multisim Live simulation circuit schematic of Figure 3-1 to verify your prediction.
3. Determine the frequency response of the linear regulator with respect to the reference voltage *Vref* with the simulation circuit schematic of Figure 3-1, by using the *AC Sweep* option.
   1. Set the switches J4 and J6 to be closed.
   2. Replace the *Vref* DC generator with an AC generator and set VO=1.024V, Freq=1Hz, VA=0.1V.
   3. Set AC\_mag = 0.1V in the *AC analysis value* menu option of the voltage generator *Vref*.
   4. Set AC\_mag = 0 V in the *AC analysis value* menu option of the voltage generator *Vin*.
   5. Set Start freq. = 1Hz and Stop freq. = 1MHz in the *Configuration Panel*.
   6. Set *Show plots* box unchecked on probe *Vin*.
   7. Run the simulation and watch the resulting AC Sweep plots (Bode plots). The continuous line is the magnitude of the ratios *Tref* = *VoutAC/VrefAC*, while the dashed line is the phase shift between *VoutAC* with respect to *VrefAC*.

The response should be flat up to a certain frequency. That frequency is the closed loop bandwidth of the linear regulator, which is the frequency range wherein the regulator is able to track accurately the reference voltage, while exhibiting a good PSRR. A wide bandwidth is a highly valuable feature of a linear regulator.

1. Analyze the effect of output capacitance on the PSRR of the linear regulator, by means of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.
2. Short the jumper J59 to set the output capacitance at 11µF.
3. Repeat Experiment 2, following the relevant instructions.
4. Calculate the value in decibel *PSRRdB* = 20log10(*VinAC*/*VoutAC*) at each frequency.
5. Compare the results with the values collected in Table 5-1 and discuss the differences based on your learning.
6. Analyze the effect of error amplifier setup on the PSRR of the linear regulator, by means of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.
7. Open the jumpers J60 and J62 to set the frequency pole *f0* at 104kHz.
8. Repeat Experiment 2, following the relevant instructions.
9. Calculate the value of the *PSRRdB* = 20log10(*VinAC*/*VoutAC*) at each frequency.
10. Compare the results with the values collected in Table 5-1 and discuss the differences based on your learning.
11. Analyze the effect of output voltage setup on the PSRR of the linear regulator, by means of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.
12. Short the jumper J61 to set the nominal output voltage at 3.3V.
13. Repeat Experiment 2, following the relevant instructions. [**Note:** set the offset of *Oscilloscope* CH-2 at -3.45V and CH-3 at -5.25V]
14. Calculate the value of the *PSRRdB* = 20log10(*VinAC*/*VoutAC*) at each frequency.
15. Compare the results with the values collected in Table 5-1 and discuss the differences based on your learning.

### 6-3 Resources for learning more

* This book provides the fundamentals of linear regulators control:

C.Basso, *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide*, Artech House

## Answer Key – Check Your Understanding Questions Only



Check Your Understanding

1-1 C

1-2 C

1-3 A

1-4 C

1-5 high *f0*, high *Adc*