Homework Assignment 6

Professor Karem A. Sakallah
EECS 598-006: Formal Verification of Hardware & Software Systems

Due date : March 28, 2017

Guidelines

- The College of Engineering Honor Code applies to all work in this course.
- The due date is firm. Follow submission instructions (at the end).

Objectives

This assignment involves the use of two model checking tools that employ the incremental induction approach for safety checking. The first tool, **PDR**, is part of the UC Berkeley ABC package; it performs bit-level verification. The second tool, **Averroes**, was developed at the University of Michigan; it performs incremental induction on an EUF abstraction of the system under verification. Instructions on how to install and use these tools can be found on the Pages tab in Canvas.

The goal of the assignment is to compare the performance of PDR and Averroes for checking the the safety property $Y \leq X$ on the hardware design in the file diagonal.v for increasing bit widths of the state variables X and Y. Specifically, assuming a timeout of 1000 seconds, you need to run PDR and Averroes and plot their run times as a function of bit widths $W \in \{2, 4, 6, 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 64\}$.

1 [PDR: Bit-level Incremental Induction] (50 Points)

Plot the rune time of PDR as a function of W for the following two initial starting states and note if the system times out or runs out of memory.

(a) $(X, Y) = (1, 0)$

(b) $(X, Y) = (0, 0)$

2 [Averroes: Incremental Induction with EUF Abstraction] (50 Points)

Plot the run time of Averroes as a function of W for the following two initial starting states and note if the system times out or runs out of memory.

(a) $(X, Y) = (1, 0)$

(b) $(X, Y) = (0, 0)$

Submission

To submit your homework, please compile a .pdf report that includes requested information for each question solution, and name your file **{uniquename}_hw6.pdf**.