**EE331**

**Devices and Circuits**

**Spring 2013**

Final Project

*Delay Circuit*

Joel S. Atienza

Bohan Wang

Alan Trinh

*Section AA*

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## Abstract

This circuit acquires an input pulse and delays it for a given range of time and width. The delay unit consists of NAND gates, resistor and capacitors which operate in parts to manipulate the pulse. The design requires the basic understanding of digital logic gates, RC circuits and lab equipments, so this project tests the application of most topics covered in EE 331.

## Introduction

For this project, we are asked to delay a pulse for a given range of time and width, independent of input. Time delay is common and useful in everyday life. Whenever a circuit is intended to respond later than input, a delay unit is required. For instance, decoration light circuits usually contain delay units to control the gradual change of light when switch is either turned on or off. Although most delay units will implement in much more complex components, this simple design is sufficient to deal with a pulse using only CMOS NAND gates, capacitors and resistors.

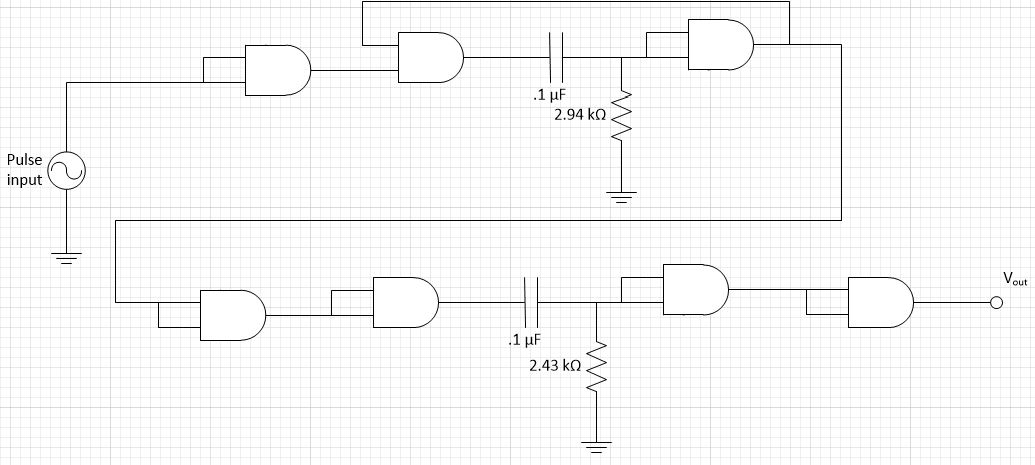
## Circuit Design

Required Materials

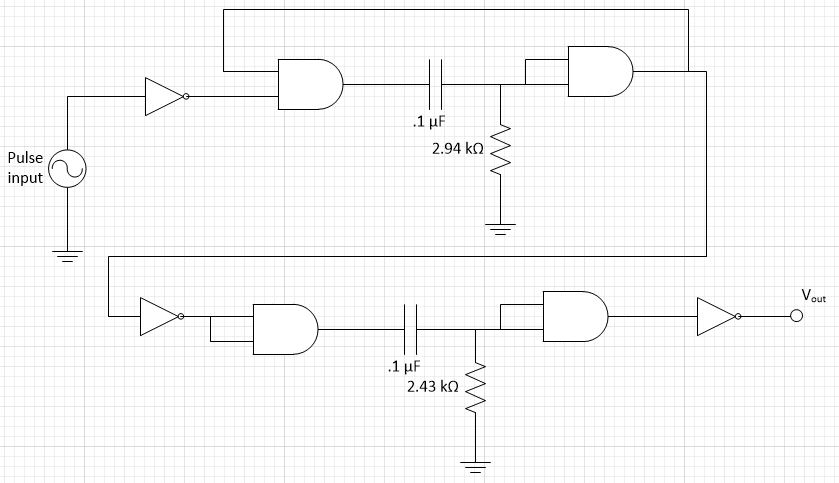
|  |  |  |
| --- | --- | --- |
| Component | Cost | EE Store Part # |
| .1 Capacitor (x3) | $0.60 | CC-.1U |
| 5 Potentiometer (x2) | $2.00 | T20-5k |
| Quad 2 input NAND (x2) | $0.80 | CD4011 |

If it were the 10 cent resistors, it would be cheaper - $1.60

The following diagram illustrates the design of the circuit. The two NAND gates that surround a resistor and capacitor pair create the delayed pulses. The first pair of “delaying NAND gates” operate as a latching monostable circuit while the second pair functions as a non-latching monostable circuit. The reason why a latching design was used for the first delaying pair of NAND gates was because the range of input width ranges from values that are smaller as well as larger than the delay time. This means that the intermediate pulse that will eventually be used to represent the delay between input pulse and output pulse could potentially be shorter or longer than the input pulse. Since a non-latching circuit is only useful if the output pulse is shorter in duration than the trigger pulse, it would be necessary to utilize the latching circuit. Similarly, since the overall output pulse will always be shorter than the delay time, there is no need to use a latching circuit so it’s left in its non-latching configuration.



Although we only used NAND gates from the CD4011 CMOS chip, some of the logic gates were used simply as an inverter. The location of the inverters from our original design are illustrated below. It was necessary to insert an inverter at the start of our circuit because the pulses created by each pair of NAND gates surrounding a pair of capacitors and resistors will output a pulse that is triggered off the “falling edge” of the trigger pulse. Since it was required to delay the pulse starting from the moment the input pulse is detected, we had to turn the rising edge of the trigger pulse into a falling edge. The easiest way to accomplish this was to invert the input pulse. However, the second and third inverters were required because the output pulses generated by both the latching and non-latching monostable sections are upside down from the way we need it to be. Therefore, we added an inverter to fix the problem.



## 

## A DC supply voltage source is added to power the chip.

## 

Equation used to determine resistor value:

By using the given time delay from the specifications and keeping the capacitance the same, the k value was calculated and thus, an appropriate resistance for the potentiometer is calculated.

## Implementation and Result

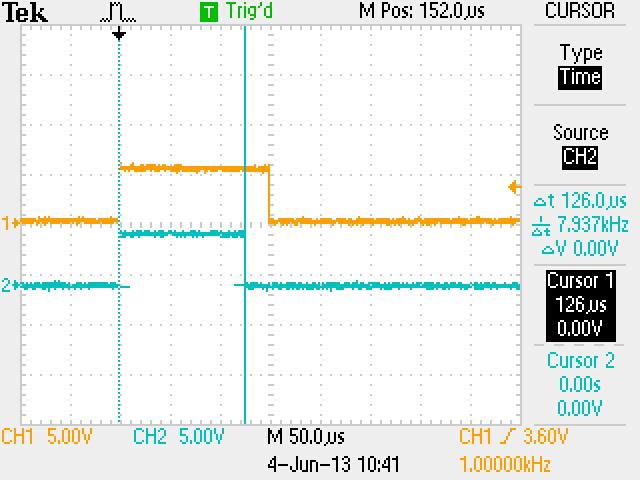
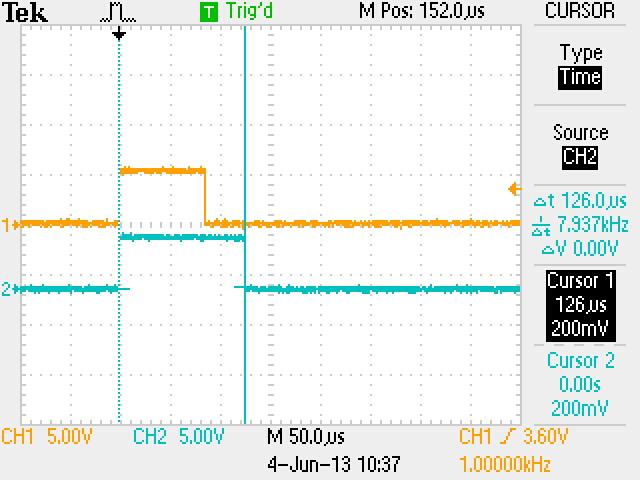
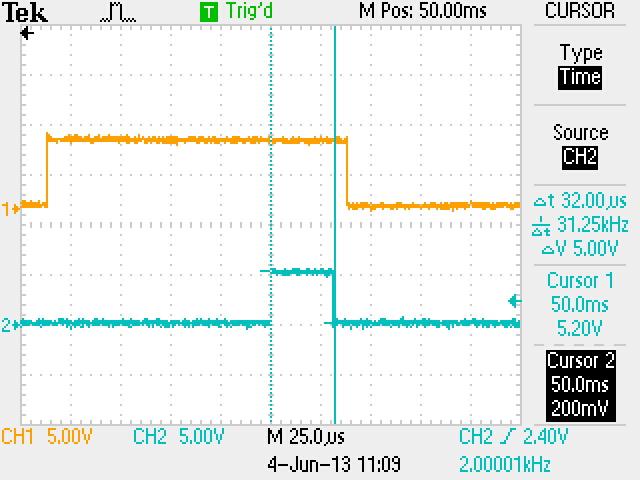
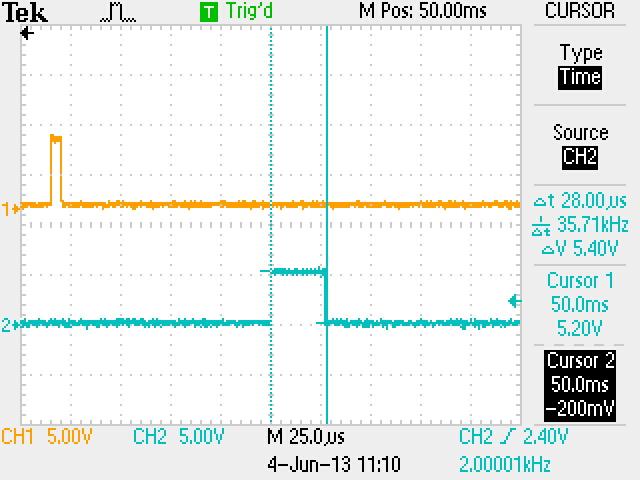
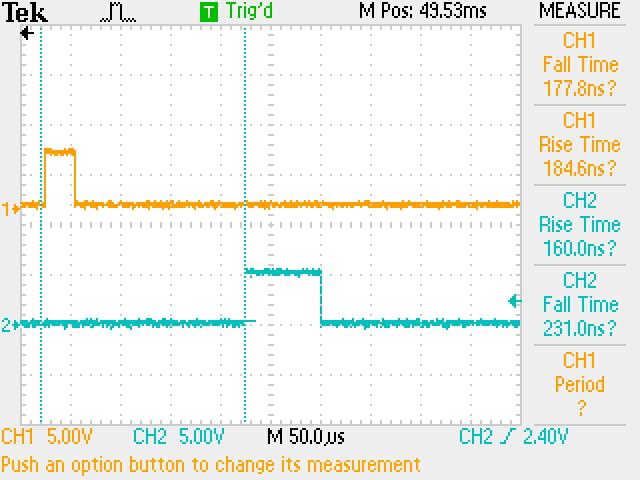


Fig 1 output of nonlatching monostable circuit Fig 2 output of nonlatching monostable

with input pulse 30 μs circuit with input 150μs



output pulse when input 5μs output pulse when input is 150μs



delay time period

We use two potentiometer instead of fixed resistors. Since the pulse width is determined by time constant τ = RC, changing the resistance is the easiest way to change the width. The first potentiometer determines the intermediate pulse as shown in Fig 1 and 2, i.e., the delay time. The second potentiometer determines the output pulse width.

The t in first two graphs are the actual delay time since the latching circuit is triggered by the falling edge of the pulse. It can be shown that delay is hardly affected by input pulse width.

When input pulse width is 5 μs

|  |  |
| --- | --- |
| Delay time | 126 μs |
| Output pulse width | 30 μs |
| Rise/Fall output | 80ns |
| Output amplitude | 5.2V |

When input pulse width is 150 μs

|  |  |
| --- | --- |
| Delay time | 126 μs |
| Output pulse width | 30 μs |
| Rise/Fall output | 80ns |
| Output amplitude | 5.2V |



When trying to obtain more groups of data, a 10V DC power is accidentally applied on the CMOS chip, so it might be damaged from the following measurements which disagree with the spec. When input is 5μs, output width is about 28 μs, whereas the output width is 32 μs when input width is 150 μs. Also the rise and fall time have changed.

|  |  |
| --- | --- |
| Rise time input | 177.8 ns |
| Fall time input | 184.6 ns |
| Rise time output | 160 ns |
| Fall time output | 231 ns |

However, this circuit still produces the same waveform and delay as in the demonstration.

## Discussion

The circuit design performed as expected because it obtained the satisfactory results specified in the lab. As required, the circuit delays an input pulse to give an output pulse that is between 29.5 and 33 microseconds, regardless of the input time period. The input pulse’s time period was to be any width between 5 to 150 microseconds. The circuit performed better than expected. The output pulse was kept at a constant 30 microseconds even when the lower end of the input time pulse had a period range of .2 to 150 microseconds. Additionally, the circuit gave a satisfactory time delay within the range of the time period specified in the lab instructions (between 120 to 132 microseconds): the combined NAND gates created a delay with a time period of 126 microseconds. The circuit was also successful in that it fulfilled the requirement that the rise and fall times of the pulse would be within 220 nanoseconds and that the output voltage would be less than 0.3 V or greater than 4.7 V. The experimental rise and fall times ended up being 80 nanoseconds while the output max voltage ended up being 5.2 V.

When it came to the connection between the input and output pulse, there was a slight deviation from the required value specified in the lab instructions. Both the delayed and output pulses are supposed to be independent of the input pulse. The circuit’s pulse fulfilled that specification for the most part. However, once the period of the input was extended to the upper ends of its period range (about 150 microseconds and higher), the output period (and thus the delayed period) was shown to have a slight dependence on the input’s period. This was most likely caused by slight errors in circuit design due to resistance and capacitance values that didn’t exactly match the calculated values as well as using CMOSs with different “k” constants. The CMOS source of error occurred because while building the circuit, the gates of the CMOS kept getting burned out and four new transistors total had to be purchased. Nevertheless, the dependence of the output time period was negligible and the circuit was a success.

**Conclusion**

This project is generally a success. We generate the expected delay and satisfy all the specs except the output width independence. The result shows that delay units can be built out of simple logic gates and RC loads, and the delay parameters can be adjusted by simply modifying load resistance. Although it is a simple design, how effective this circuit can handle other forms of input is not certain. For instance the gradual change of decoration lights can be implemented by delay units with more complicated schematic. However, this project shows the basics of how delay units manipulate simple signal. The ability of the circuit to invert the pulse at its beginning, turning the rising edge of the input pulse into a falling edge, delaying the pulse afterwards with NAND gates, and then reinverting the output pulse to flip the signal right side up justifies its performance in meeting the lab specifications.

Despite the fact that multiple transistors were purchased for the circuit, the actual cost of the circuit is cheap (in an ideal situation where the CMOS’s aren’t accidentally burned out during experimentation). Using the items required to build the circuit (mentioned in the “Circuit Design” portion of this report), the total cost ended up being $3.40. The use of two NAND gate CMOSs, three .1Capacitors, and two potentiometers, the circuit ended up being very efficient. This is a favorable price wise when it comes to designing a low-cost circuit that can delay output signals of specific time periods that while being independent of the input signal.

## References

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