9.6.1 Register Descriptions

The read-only ID control register is programmed during device manufacture to indicate device characteristics.

9.6.1.1 ID: ID Control Register (address = 00h) (reset = xxh)

Figure 74. ID Control Register

7	6	5	4	3	2	1	0
DEV_ID[7:5]			1	0	DEV_ID[2:0]		
R-x			R-2h		R-x		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. ID Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEV_ID[7:5]	R	xh	**Device ID** These bits indicate the device family. 000 = Reserved 011 = Reserved 100 = ADS129x device family 101 = Reserved 110 = ADS129xR device family 111 = Reserved
4:3	RESERVED	R	2h	**Reserved** Always read back 2h
2:0	DEV_ID[2:0]	R	xh	**Channel ID** These bits indicates number of channels. 000 = 4-channel ADS1294 or ADS1294R 001 = 6-channel ADS1296 or ADS1296R 010 = 8-channel ADS1298 or ADS1298R 011 = Reserved 111 = Reserved

9.6.1.2 CONFIG1: Configuration Register 1 (address = 01h) (reset = 06h)

Figure 75. CONFIG1: Configuration Register 1

7	6	5	4	3	2	1	0
HR	$\overline{\text{DAISY\_EN}}$	CLK_EN	0	0	DR[2:0]		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-6h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	HR	R/W	0h	**High-resolution or low-power mode** This bit determines whether the device runs in low-power or high-resolution mode. 0 = LP mode 1 = HR mode
6	$\overline{\text{DAISY\_EN}}$	R/W	0h	**Daisy-chain or multiple readback mode** This bit determines which mode is enabled. 0 = Daisy-chain mode 1 = Multiple readback mode
5	CLK_EN	R/W	0h	**CLK connection** (1) This bit determines if the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1. 0 = Oscillator clock output disabled 1 = Oscillator clock output enabled
4:3	RESERVED	R/W	0h	**Reserved** Always write 0h
2:0	DR[2:0]	R/W	6h	**Output data rate** For High-Resolution mode, $f_{MOD} = f_{CLK} / 4$. For low power mode, $f_{MOD} = f_{CLK} / 8$. These bits determine the output data rate of the device. 000: $f_{MOD} / 16$ (HR Mode: 32 kSPS, LP Mode: 16 kSPS) 001: $f_{MOD} / 32$ (HR Mode: 16 kSPS, LP Mode: 8 kSPS) 010: $f_{MOD} / 64$ (HR Mode: 8 kSPS, LP Mode: 4 kSPS) 011: $f_{MOD} / 128$ (HR Mode: 4 kSPS, LP Mode: 2 kSPS) 100: $f_{MOD} / 256$ (HR Mode: 2 kSPS, LP Mode: 1 kSPS) 101: $f_{MOD} / 512$ (HR Mode: 1 kSPS, LP Mode: 500 SPS) 110: $f_{MOD} / 1024$ (HR Mode: 500 SPS, LP Mode: 250 SPS) 111: Reserved (do not use)

(1) Additional power is consumed when driving external devices.

9.6.1.3 CONFIG2: Configuration Register 2 (address = 02h) (reset = 40h)

Configuration register 2 configures the test signal generation. See the *Input Multiplexer* section for more details.

Figure 76. CONFIG2: Configuration Register 2

7	6	5	4	3	2	1	0
0	0	WCT_CHOP	INT_TEST	0	TEST_AMP	TEST_FREQ[1:0]	
R/W-1h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	1h	**Reserved** Always write 0h
5	WCT_CHOP	R/W	0h	**WCT chopping scheme** This bit determines whether the chopping frequency of WCT amplifiers is variable or fixed. 0 = Chopping frequency varies, see Table 7 1 = Chopping frequency constant at f_{MOD} / 16
4	INT_TEST	R/W	0h	**TEST source** This bit determines the source for the test signal. 0 = Test signals are driven externally 1 = Test signals are generated internally
3	RESERVED	R/W	0h	**Reserved** Always write 0h
2	TEST_AMP	R/W	0h	**Test signal amplitude** These bits determine the calibration signal amplitude. 0 = 1 × –(VREFP – VREFN) / 2400 V 1 = 2 × –(VREFP – VREFN) / 2400 V
1:0	TEST_FREQ[1:0]	R/W	0h	**Test signal frequency** These bits determine the calibration signal frequency. 00 = Pulsed at f_{CLK} / 2^{21} 01 = Pulsed at f_{CLK} / 2^{20} 10 = Not used 11 = At dc

9.6.1.4 CONFIG3: Configuration Register 3 (address = 03h) (reset = 40h)

Configuration register 3 configures multireference and RLD operation.

Figure 77. CONFIG3: Configuration Register 3

7	6	5	4	3	2	1	0
$\overline{\text{PD\_REFBUF}}$	1	VREF_4V	RLD_MEAS	RLDREF_INT	$\overline{\text{PD\_RLD}}$	RLD_LOFF_SENS	RLD_STAT
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Configuration Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	$\overline{\text{PD\_REFBUF}}$	R/W	0h	**Power-down reference buffer** This bit determines the power-down reference buffer state. 0 = Power-down internal reference buffer 1 = Enable internal reference buffer
6	RESERVED	R/W	1h	**Reserved** Always write 1h
5	VREF_4V	R/W	0h	**Reference voltage** This bit determines the reference voltage, VREFP. 0 = VREFP is set to 2.4 V 1 = VREFP is set to 4 V (use only with a 5-V analog supply)
4	RLD_MEAS	R/W	0h	**RLD measurement** This bit enables RLD measurement. The RLD signal may be measured with any channel. 0 = Open 1 = RLD_IN signal is routed to the channel that has the MUX_Setting *010* (V_{REF})
3	RLDREF_INT	R/W	0h	**RLDREF signal** This bit determines the RLDREF signal source. 0 = RLDREF signal fed externally 1 = RLDREF signal (AVDD – AVSS) / 2 generated internally
2	$\overline{\text{PD\_RLD}}$	R/W	0h	**RLD buffer power** This bit determines the RLD buffer power state. 0 = RLD buffer is powered down 1 = RLD buffer is enabled
1	RLD_LOFF_SENS	R/W	0h	**RLD sense function** This bit enables the RLD sense function. 0 = RLD sense is disabled 1 = RLD sense is enabled
0	RLD_STAT	R	0h	**RLD lead-off status** This bit determines the RLD status. 0 = RLD is connected 1 = RLD is not connected

9.6.1.5 LOFF: Lead-Off Control Register (address = 04h) (reset = 00h)

The lead-off control register configures the lead-off detection operation.

Figure 78. LOFF: Lead-Off Control Register

7	6	5	4	3	2	1	0
COMP_TH2[2:0]			VLEAD_OFF_EN	ILEAD_OFF[1:0]		FLEAD_OFF[1:0]	
R/W-0h			R/W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. Lead-Off Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	COMP_TH[2:0]	R/W	0h	**Lead-off comparator threshold** Comparator positive side 000 = 95% 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% Comparator negative side 000 = 5% 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
4	VLEAD_OFF_EN	R/W	0h	**Lead-off detection mode** This bit determines the lead-off detection mode. 0 = Current source mode lead-off 1 = pullup or pulldown resistor mode lead-off
3:2	ILEAD_OFF[1:0]	R/W	0h	**Lead-off current magnitude** These bits determine the magnitude of current for the current lead-off mode. 00 = 6 nA 01 = 12 nA 10 = 18 nA 11 = 24 nA
1:0	FLEAD_OFF[1:0]	R/W	0h	**Lead-off frequency** These bits determine the frequency of lead-off detect for each channel. 00 = When any bits of the LOFF_SENSP or LOFF_SENSN registers are turned on, make sure that FLEAD[1:0] are either set to 01 or 11 01 = AC lead-off detection at f_{DR} / 4 10 = Do not use 11 = DC lead-off detection turned on

9.6.1.6 CHnSET: Individual Channel Settings (n = 1 to 8) (address = 05h to 0Ch) (reset = 00h)

The CH[1:8]SET control register configures the power mode, PGA gain, and multiplexer settings channels. See the *Input Multiplexer* section for details. CH[2:8]SET are similar to CH1SET, corresponding to the respective channels.

Figure 79. CHnSET: Individual Channel Settings Register

7	6	5	4	3	2	1	0
PD*n*	GAIN*n*[2:0]			0	MUX*n*[2:0]		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Individual Channel Settings (*n* = 1 to 8) Field Descriptions

Bit	Field	Type	Reset	Description
7	PD*n*	R/W	0h	**Power-down** This bit determines the channel power mode for the corresponding channel. 0 = Normal operation 1 = Channel power-down. When powering down a channel, TI recommends that the channel be set to input short by setting the appropriate MUXn[2:0] = 001 of the CHnSET register.
6:4	GAIN*n*[2:0]	R/W	0h	**PGA gain** These bits determine the PGA gain setting. 000 = 6 001 = 1 010 = 2 011 = 3 100 = 4 101 = 8 110 = 12
3	RESERVED	R/W	0h	**Reserved** Always write 0h
2:0	MUX*n*[2:0]	R/W	0h	**Channel input** These bits determine the channel input selection. 000 = Normal electrode input 001 = Input shorted (for offset or noise measurements) 010 = Used in conjunction with RLD_MEAS bit for RLD measurements. See the *Right Leg Drive (RLD) DC Bias Circuit* subsection of the *ECG-Specific Functions* section for more details. 011 = MVDD for supply measurement 100 = Temperature sensor 101 = Test signal 110 = RLD_DRP (positive electrode is the driver) 111 = RLD_DRN (negative electrode is the driver)

9.6.1.7 RLD_SENSP: RLD Positive Signal Derivation Register (address = 0Dh) (reset = 00h)

This register controls the selection of the positive signals from each channel for right leg drive (RLD) derivation. See the *Right Leg Drive (RLD) DC Bias Circuit* section for details.

Registers bits[5:4] are not available for the ADS1294 or ADS1294R. Bits[7:6] are not available for the ADS1294, ADS1294R, ADS1296, or ADS1296R.

Figure 80. RLD_SENSP: RLD Positive Signal Derivation Register

7	6	5	4	3	2	1	0
RLD8P	RLD7P	RLD6P	RLD5P	RLD4P	RLD3P	RLD2P	RLD1P
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. RLD Positive Signal Derivation Field Descriptions

Bit	Field	Type	Reset	Description
7	RLD8P	R/W	0h	**IN8P to RLD** Route channel 8 positive signal into RLD derivation 0: Disabled 1: Enabled
6	RLD7P	R/W	0h	**IN7P to RLD** Route channel 7 positive signal into RLD derivation 0: Disabled 1: Enabled
5	RLD6P	R/W	0h	**IN6P to RLD** Route channel 6 positive signal into RLD derivation 0: Disabled 1: Enabled
4	RLD5P	R/W	0h	**IN5P to RLD** Route channel 5 positive signal into RLD derivation 0: Disabled 1: Enabled
3	RLD4P	R/W	0h	**IN4P to RLD** Route channel 4 positive signal into RLD derivation 0: Disabled 1: Enabled
2	RLD3P	R/W	0h	**IN3P to RLD** Route channel 3 positive signal into RLD derivation 0: Disabled 1: Enabled
1	RLD2P	R/W	0h	**IN2P to RLD** Route channel 2 positive signal into RLD channel 0: Disabled 1: Enabled
0	RLD1P	R/W	0h	**IN1P to RLD** Route channel 1 positive signal into RLD channel 0: Disabled 1: Enabled

9.6.1.8 RLD_SENSN: RLD Negative Signal Derivation Register (address = 0Eh) (reset = 00h)

This register controls the selection of the negative signals from each channel for right leg drive derivation. See the *Right Leg Drive (RLD) DC Bias Circuit* section for details.

Registers bits[5:4] are not available for the ADS1294 and ADS1294R. Bits[7:6] are not available for the ADS1294, ADS1294R, ADS1296, or ADS1296R.

Figure 81. RLD_SENSN: RLD Negative Signal Derivation Register

7	6	5	4	3	2	1	0
RLD8N	RLD7N	RLD6N	RLD5N	RLD4N	RLD3N	RLD2N	RLD1N
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. RLD Negative Signal Derivation Field Descriptions

Bit	Field	Type	Reset	Description
7	RLD8N	R/W	0h	**IN8N to RLD** Route channel 8 negative signal into RLD derivation 0: Disabled 1: Enabled
6	RLD7N	R/W	0h	**IN7N to RLD** Route channel 7 negative signal into RLD derivation 0: Disabled 1: Enabled
5	RLD6N	R/W	0h	**IN6N to RLD** Route channel 6 negative signal into RLD derivation 0: Disabled 1: Enabled
4	RLD5N	R/W	0h	**IN5N to RLD** Route channel 5 negative signal into RLD derivation 0: Disabled 1: Enabled
3	RLD4N	R/W	0h	**IN4N to RLD** Route channel 4 negative signal into RLD derivation 0: Disabled 1: Enabled
2	RLD3N	R/W	0h	**IN3N to RLD** Route channel 3 negative signal into RLD derivation 0: Disabled 1: Enabled
1	RLD2N	R/W	0h	**IN2N to RLD** Route channel 2 negative signal into RLD derivation 0: Disabled 1: Enabled
0	RLD1N	R/W	0h	**IN1N to RLD** Route channel 1 negative signal into RLD derivation 0: Disabled 1: Enabled

9.6.1.9 LOFF_SENSP: Positive Signal Lead-Off Detection Register (address = 0Fh) (reset = 00h)

This register selects the positive side from each channel for lead-off detection. See the *Lead-Off Detection* section for details. The LOFF_STATP register bits are only valid if the corresponding LOFF_SENSP bits are set to 1.

Registers bits[5:4] are not available for the ADS1294 or ADS1294R. Bits[7:6] are not available for the ADS1294, ADS1294R, ADS1296, or ADS1296R.

Figure 82. LOFF_SENSP: Positive Signal Lead-Off Detection Register

7	6	5	4	3	2	1	0
LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Positive Signal Lead-Off Detection Field Descriptions

Bit	Field	Type	Reset	Description
7	LOFF8P	R/W	0h	**IN8P lead off** Enable lead-off detection on IN8P 0: Disabled 1: Enabled
6	LOFF7P	R/W	0h	**IN7P lead off** Enable lead-off detection on IN7P 0: Disabled 1: Enabled
5	LOFF6P	R/W	0h	**IN6P lead off** Enable lead-off detection on IN6P 0: Disabled 1: Enabled
4	LOFF5P	R/W	0h	**IN5P lead off** Enable lead-off detection on IN5P 0: Disabled 1: Enabled
3	LOFF4P	R/W	0h	**IN4P lead off** Enable lead-off detection on IN4P 0: Disabled 1: Enabled
2	LOFF3P	R/W	0h	**IN3P lead off** Enable lead-off detection on IN3P 0: Disabled 1: Enabled
1	LOFF2P	R/W	0h	**IN2P lead off** Enable lead-off detection on IN2P 0: Disabled 1: Enabled
0	LOFF1P	R/W	0h	**IN1P lead off** Enable lead-off detection on IN1P 0: Disabled 1: Enabled

9.6.1.10 LOFF_SENSN: Negative Signal Lead-Off Detection Register (address = 10h) (reset = 00h)

This register selects the negative side from each channel for lead-off detection. See the *Lead-Off Detection* section for details. The LOFF_STATN register bits are only valid if the corresponding LOFF_SENSN bits are set to 1.

Registers bits[5:4] are not available for the ADS1294 or ADS1294R. Bits[7:6] are not available for the ADS1294, ADS1294R, ADS1296, or ADS1296R.

Figure 83. LOFF_SENSN: Negative Signal Lead-Off Detection Register

7	6	5	4	3	2	1	0
LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Negative Signal Lead-Off Detection Field Descriptions

Bit	Field	Type	Reset	Description
7	LOFF8N	R/W	0h	**IN8N lead off** Enable lead-off detection on IN8N 0: Disabled 1: Enabled
6	LOFF7N	R/W	0h	**IN7N lead off** Enable lead-off detection on IN7N 0: Disabled 1: Enabled
5	LOFF6N	R/W	0h	**IN6N lead off** Enable lead-off detection on IN6N 0: Disabled 1: Enabled
4	LOFF5N	R/W	0h	**IN5N lead off** Enable lead-off detection on IN5N 0: Disabled 1: Enabled
3	LOFF4N	R/W	0h	**IN4N lead off** Enable lead-off detectionn on IN4N 0: Disabled 1: Enabled
2	LOFF3N	R/W	0h	**IN3N lead off** Enable lead-off detectionion on IN3N 0: Disabled 1: Enabled
1	LOFF2N	R/W	0h	**IN2N lead off** Enable lead-off detectionction on IN2N 0: Disabled 1: Enabled
0	LOFF1N	R/W	0h	**IN1N lead off** Enable lead-off detectionction on IN1N 0: Disabled 1: Enabled

9.6.1.11 LOFF_FLIP: Lead-Off Flip Register (address = 11h) (reset = 00h)

This register controls the direction of the current used for lead-off derivation. See the *Lead-Off Detection* section for details.

Figure 84. LOFF_FLIP: Lead-Off Flip Register

7	6	5	4	3	2	1	0
LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Lead-Off Flip Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOFF_FLIP8	R/W	0h	**Channel 8 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 8 for lead-off derivation. 0: No Flip: IN8P is pulled to AVDD and IN8N pulled to AVSS 1: Flipped: IN8P is pulled to AVSS and IN8N pulled to AVDD
6	LOFF_FLIP7	R/W	0h	**Channel 7 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 7 for lead-off derivation. 0: No Flip: IN7P is pulled to AVDD and IN7N pulled to AVSS 1: Flipped: IN7P is pulled to AVSS and IN7N pulled to AVDD
5	LOFF_FLIP6	R/W	0h	**Channel 6 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 6 for lead-off derivation. 0: No Flip: IN6P is pulled to AVDD and IN6N pulled to AVSS 1: Flipped: IN6P is pulled to AVSS and IN6N pulled to AVDD
4	LOFF_FLIP5	R/W	0h	**Channel 5 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 5 for lead-off derivation. 0: No Flip: IN5P is pulled to AVDD and IN5N pulled to AVSS 1: Flipped: IN5P is pulled to AVSS and IN5N pulled to AVDD
3	LOFF_FLIP4	R/W	0h	**Channel 4 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 4 for lead-off derivation. 0: No Flip: IN4P is pulled to AVDD and IN4N pulled to AVSS 1: Flipped: IN4P is pulled to AVSS and IN4N pulled to AVDD
2	LOFF_FLIP3	R/W	0h	**Channel 3 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 3 for lead-off derivation. 0: No Flip: IN3P is pulled to AVDD and IN3N pulled to AVSS 1: Flipped: IN3P is pulled to AVSS and IN3N pulled to AVDD
1	LOFF_FLIP2	R/W	0h	**Channel 2 LOFF Polarity Flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 2 for lead-off derivation. 0: No Flip: IN2P is pulled to AVDD and IN2N pulled to AVSS 1: Flipped: IN2P is pulled to AVSS and IN2N pulled to AVDD
0	LOFF_FLIP1	R/W	0h	**Channel 1 LOFF Polarity Flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 1 for lead-off derivation. 0: No Flip: IN1P is pulled to AVDD and IN1N pulled to AVSS 1: Flipped: IN1P is pulled to AVSS and IN1N pulled to AVDD

9.6.1.12 LOFF_STATP: Lead-Off Positive Signal Status Register (address = 12h) (reset = 00h)

This register stores the status of whether the positive electrode on each channel is on or off. See the *Lead-Off Detection* section for details. Ignore the LOFF_STATP values if the corresponding LOFF_SENSP bits are not set to 1.

When the LOFF_SENSEP bits are 0, the LOFF_STATP bits should be ignored.

Figure 85. LOFF_STATP: Lead-Off Positive Signal Status Register (Read-Only)

7	6	5	4	3	2	1	0
IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Lead-Off Positive Signal Status Field Descriptions

Bit	Field	Type	Reset	Description
7	IN8P_OFF	R	0h	**Channel 8 positive channel lead-off status** Status of whether IN8P electrode is on or off 0: Electrode is on 1: Electrode is off
6	IN7P_OFF	R	0h	**Channel 7 positive channel lead-off status** Status of whether IN7P electrode is on or off 0: Electrode is on 1: Electrode is off
5	IN6P_OFF	R	0h	**Channel 6 positive channel lead-off status** Status of whether IN6P electrode is on or off 0: Electrode is on 1: Electrode is off
4	IN5P_OFF	R	0h	**Channel 5 positive channel lead-off status** Status of whether IN5P electrode is on or off 0: Electrode is on 1: Electrode is off
3	IN4P_OFF	R	0h	**Channel 4 positive channel lead-off status** Status of whether IN4P electrode is on or off 0: Electrode is on 1: Electrode is off
2	IN3P_OFF	R	0h	**Channel 3 positive channel lead-off status** Status of whether IN3P electrode is on or off 0: Electrode is on 1: Electrode is off
1	IN2P_OFF	R	0h	**Channel 2 positive channel lead-off status** Status of whether IN2P electrode is on or off 0: Electrode is on 1: Electrode is off
0	IN1P_OFF	R	0h	**Channel 1 positive channel lead-off status** Status of whether IN1P electrode is on or off 0: Electrode is on 1: Electrode is off

9.6.1.13 LOFF_STATN: Lead-Off Negative Signal Status Register (address = 13h) (reset = 00h)

This register stores the status of whether the negative electrode on each channel is on or off. See the *Lead-Off Detection* section for details. Ignore the LOFF_STATN values if the corresponding LOFF_SENSN bits are not set to 1.

When the LOFF_SENSEN bits are 0, the LOFF_STATP bits should be ignored.

Figure 86. LOFF_STATN: Lead-Off Negative Signal Status Register (Read-Only)

7	6	5	4	3	2	1	0
IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Lead-Off Negative Signal Status Field Descriptions

Bit	Field	Type	Reset	Description
7	IN8N_OFF	R	0h	**Channel 8 negative channel lead-off status** Status of whether IN8N electrode is on or off 0: Electrode is on 1: Electrode is off
6	IN7N_OFF	R	0h	**Channel 7 negative channel lead-off status** Status of whether IN7N electrode is on or off 0: Electrode is on 1: Electrode is off
5	IN6N_OFF	R	0h	**Channel 6 negative channel lead-off status** Status of whether IN6N electrode is on or off 0: Electrode is on 1: Electrode is off
4	IN5N_OFF	R	0h	**Channel 5 negative channel lead-off status** Status of whether IN5N electrode is on or off 0: Electrode is on 1: Electrode is off
3	IN4N_OFF	R	0h	**Channel 4 negative channel lead-off status** Status of whether IN4N electrode is on or off 0: Electrode is on 1: Electrode is off
2	IN3N_OFF	R	0h	**Channel 3 negative channel lead-off status** Status of whether IN3N electrode is on or off 0: Electrode is on 1: Electrode is off
1	IN2N_OFF	R	0h	**Channel 2 negative channel lead-off status** Status of whether IN2N electrode is on or off 0: Electrode is on 1: Electrode is off
0	IN1N_OFF	R	0h	**Channel 1 negative channel lead-off status** Status of whether IN1N electrode is on or off 0: Electrode is on 1: Electrode is off

9.6.1.14 GPIO: General-Purpose I/O Register (address = 14h) (reset = 0Fh)

The general-purpose I/O register controls the action of the three GPIO pins. When RESP_CTRL[1:0] is in mode 01 and 11, the GPIO2, GPIO3, and GPIO4 pins are not available for use.

Figure 87. GPIO: General-Purpose I/O Register

7	6	5	4	3	2	1	0
GPIOD[4:1]				GPIOC[4:1]			
R/W-0h				R/W-Fh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. General-Purpose I/O Field Descriptions

Bit	Field	Type	Reset	Description
7:4	GPIOD[4:1]	R/W	0h	**GPIO data** These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect. GPIO is not available in certain respiration modes.
3:0	GPIOC[4:1]	R/W	Fh	**GPIO control (corresponding GPIOD)** These bits determine if the corresponding GPIOD pin is an input or output. 0 = Output 1 = Input

9.6.1.15 PACE: Pace Detect Register (address = 15h) (reset = 00h)

This register provides the pace controls that configure the channel signal used to feed the external pace detect circuitry. See the *Pace Detect* section for details.

Figure 88. PACE: Pace Detect Register

7	6	5	4	3	2	1	0
0	0	0	PACEE[1:0]		PACEO[1:0]		$\overline{\text{PD\_PACE}}$
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. (For example, CONTROL_REVISION Register) Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0h	**Reserved** Always write 0h
4:3	PACEE[1:0]	R/W	0h	**Pace even channels** These bits control the selection of the even number channels available on TEST_PACE_OUT1. Only one channel may be selected at any time. 00 = Channel 2 01 = Channel 4 10 = Channel 6 (ADS1296, ADS1296R, ADS1298, ADS1298R) 11 = Channel 8 (ADS1298 and ADS1298R)
2:1	PACEO[1:0]	R/W	0h	**Pace odd channels** These bits control the selection of the odd number channels available on TEST_PACE_OUT2. Only one channel may be selected at any time. 00 = Channel 1 01 = Channel 3 10 = Channel 5 (ADS1296, ADS1296R, ADS1298, ADS1298R) 11 = Channel 7 (ADS1298, ADS1298R)
0	$\overline{\text{PD\_PACE}}$	R/W	0h	**Pace detect buffer** This bit is used to enable/disable the pace detect buffer. 0 = Pace detect buffer turned off 1 = Pace detect buffer turned on

9.6.1.16 RESP: Respiration Control Register (address = 16h) (reset = 00h)

This register provides the controls for the respiration circuitry; see the *Respiration* section for details.

Figure 89. RESP: Respiration Control Register

7	6	5	4	3	2	1	0
RESP_ DEMOD_EN1	RESP_MOD_ EN1	1	RESP_PH[2:0]			RESP_CTRL[1:0]	
R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Respiration Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESP_DEMOD_EN1	R/W	0h	**Enables respiration demodulation circuitry (ADS129xR only; for ADS129x always write 0)** This bit enables and disables the demodulation circuitry on channel 1. 0 = RESP demodulation circuitry turned off 1 = RESP demodulation circuitry turned on
6	RESP_MOD_EN1	R/W	0h	**RESP_MOD_EN1: Enables respiration modulation circuitry (ADS129xR only; for ADS129x always write 0)** This bit enables and disables the modulation circuitry on channel 1. 0 = RESP modulation circuitry turned off 1 = RESP modulation circuitry turned on
5	RESERVED	R/W	0h	**Reserved** Always write 1h
4:2	RESP_PH[2:0]	R/W	0h	**Respiration phase**(1) 000 = 22.5° 001 = 45° 010 = 67.5° 011 = 90° 100 = 112.5° 101 = 135° 110 = 157.5° 111 = N/A
1:0	RESP_CTRL[1:0]	R/W	0h	**Respiration control** These bits set the mode of the respiration circuitry. 00 = No respiration 01= External respiration 10 = Internal respiration with internal signals 11 = Internal respiration with user-generated signals

(1) RESP_PH[2:0] phase control bits only for internal respiration (RESP_CTRL = 10) and external respiration (RESP_CTRL = 01) modes when the CONFIG4.RESP_FREQ[2:0] register bits are 000b or 001b.

9.6.1.17 CONFIG4: Configuration Register 4 (address = 17h) (reset = 00h)

Figure 90. CONFIG4: Configuration Register 4

7	6	5	4	3	2	1	0
RESP_FREQ[2:0]			0	SINGLE_SHOT	WCT_TO_RLD	$\overline{\text{PD\_LOFF\_COMP}}$	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. Configuration Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESP_FREQ[2:0]	R/W	0h	**Respiration modulation frequency** These bits control the respiration control frequency when RESP_CTRL[1:0] = 10 or RESP_CTRL[1:0] = 10(1). 000 = 64 kHz modulation clock 001 = 32 kHz modulation clock 010 = 16kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 011 = 8kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 100 = 4kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 101 = 2kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 110 = 1kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 111 = 500Hz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. Modes 000 and 001 are modulation frequencies in internal and external respiration modes. In internal respiration mode, the control signals appear at the RESP_MODP and RESP_MODN terminals. All other bit settings generate square waves as described above on GPIO4 and GPIO3.
4	RESERVED	R/W	0h	**Reserved** Always write 0h
3	SINGLE_SHOT	R/W	0h	**Single-shot conversion** This bit sets the conversion mode. 0 = Continuous conversion mode 1 = Single-shot mode
2	WCT_TO_RLD	R/W	0h	**Connects the WCT to the RLD** This bit connects WCT to RLD. 0 = WCT to RLD connection off 1 = WCT to RLD connection on
1	$\overline{\text{PD\_LOFF\_COMP}}$	R/W	0h	**Lead-off comparator power-down** This bit powers down the lead-off comparators. 0 = Lead-off comparators disabled 1 = Lead-off comparators enabled
0	RESERVED	R/W	0h	**Reserved** Always write 0h

(1) These frequencies assume f_{CLK} = 2.048 MHz.

9.6.1.18 WCT1: Wilson Central Terminal and Augmented Lead Control Register (address = 18h) (reset = 00h)

The WCT1 control register configures the device WCT circuit channel selection and the augmented leads.

Figure 91. WCT1: Wilson Central Terminal and Augmented Lead Control Register

7	6	5	4	3	2	1	0
aVF_CH6	aVL_CH5	aVR_CH7	aVR_CH4	$\overline{\text{PD\_WCTA}}$	WCTA[2:0]		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Wilson Central Terminal and Augmented Lead Control Field Descriptions

Bit	Field	Type	Reset	Description
7	aVF_CH6	R/W	0h	**Enable (WCTA + WCTB)/2 to the negative input of channel 6 (ADS1296, ADS1296R, ADS1298, and ADS1298R)** 0 = Disabled 1 = Enabled
6	aVL_CH5	R/W	0h	**Enable (WCTA + WCTC)/2 to the negative input of channel 5 (ADS1296, ADS1296R, ADS1298, and ADS1298R)** 0 = Disabled 1 = Enabled
5	aVR_CH7	R/W	0h	**Enable (WCTB + WCTC)/2 to the negative input of channel 7 (ADS1298 and ADS1298R)** 0 = Disabled 1 = Enabled
4	aVR_CH4	R/W	0h	**Enable (WCTB + WCTC)/2 to the negative input of channel 4** 0 = Disabled 1 = Enabled
3	$\overline{\text{PD\_WCTA}}$	R/W	0h	**Power-down WCTA** 0 = Powered down 1 = Powered on
2:0	WCTA[2:0]	R/W	0h	**WCT Amplifier A channel selection, typically connected to RA electrode** These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTA amplifier 001 = Channel 1 negative input connected to WCTA amplifier 010 = Channel 2 positive input connected to WCTA amplifier 011 = Channel 2 negative input connected to WCTA amplifier 100 = Channel 3 positive input connected to WCTA amplifier 101 = Channel 3 negative input connected to WCTA amplifier 110 = Channel 4 positive input connected to WCTA amplifier 111 = Channel 4 negative input connected to WCTA amplifier

9.6.1.19 WCT2: Wilson Central Terminal Control Register (address = 18h) (reset = 00h)

The WCT2 configuration register configures the device WCT circuit channel selection.

Figure 92. WCT2: Wilson Central Terminal Control Register

7	6	5	4	3	2	1	0
$\overline{\text{PD\_WCTC}}$	$\overline{\text{PD\_WCTB}}$	WCTB[2:0]			WCTC[2:0]		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Wilson Central Terminal Control Field Descriptions

Bit	Field	Type	Reset	Description
7	$\overline{\text{PD\_WCTC}}$	R/W	0h	**Power-down WCTC** 0 = Powered down 1 = Powered on
6	$\overline{\text{PD\_WCTB}}$	R/W	0h	**Power-down WCTB** 0 = Powered down 1 = Powered on
5:3	WCTB[2:0]	R/W	0h	**WCT amplifier B channel selection, typically connected to LA electrode.** These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTB amplifier 001 = Channel 1 negative input connected to WCTB amplifier 010 = Channel 2 positive input connected to WCTB amplifier 011 = Channel 2 negative input connected to WCTB amplifier 100 = Channel 3 positive input connected to WCTB amplifier 101 = Channel 3 negative input connected to WCTB amplifier 110 = Channel 4 positive input connected to WCTB amplifier 111 = Channel 4 negative input connected to WCTB amplifier
2:0	WCTC[2:0]	R/W	0h	**WCT amplifier C channel selection, typically connected to LL electrode.** These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTC amplifier 001 = Channel 1 negative input connected to WCTC amplifier 010 = Channel 2 positive input connected to WCTC amplifier 011 = Channel 2 negative input connected to WCTC amplifier 100 = Channel 3 positive input connected to WCTC amplifier 101 = Channel 3 negative input connected to WCTC amplifier 110 = Channel 4 positive input connected to WCTC amplifier 111 = Channel 4 negative input connected to WCTC amplifier