CS3520 - Domain ISA Specification

Group: No Blueprint

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1. Overview & Motivation

The MedAI ISA (Medical Artificial Intelligence Instruction Set Architecture) is designed for AI-driven mobile healthcare systems deployed across Africa's remote regions. It supports three essential workloads: geospatial analysis, fingerprint recognition, and image-based triage. The goal is to enable real-time processing on both low-power edge devices and high-performance cloud systems.

Design Goals:
- Efficiency: Execute real-time biometric and geospatial tasks on low-power mobile and IoT platforms.
- Scalability: Operate across microcontrollers, smartphones, and cloud nodes.
- Accuracy: Support precise floating-point and vector arithmetic for AI workloads.
- Integration: Combine communication, AI inference, and biometric features in one architecture.

Suitability:
This ISA integrates SIMD extensions, vector math, and low-power operation modes, making it ideal for healthcare-related AI workloads that mix heavy and lightweight computations.

2. Architectural Design Choices

Design Aspect	Specification
Instruction Philosophy	Hybrid RISC-AI: Base RISC simplicity + specialized AI instructions (GEO, FREC, IMG).
Registers	32 general-purpose 32-bit registers (R0–R31); dedicated FP registers (F0–F15).
Data Types	8-, 16-, 32-bit integers; 32-bit floats; vector arrays (up to 128 bits).

Addressing Modes	Immediate, register-indirect, base+offset, PC-relative.
Memory Model	Little-endian; word-aligned (4 bytes).
Instruction Formats	Fixed 32-bit encoding with R-type, I-type, and S-type AI formats.

3. Instruction Set Summary

The instruction set combines standard RISC operations with domain-specific AI extensions for geospatial, biometric, and image processing tasks.

Category	Mnemonic	Operands	Description
Arithmetic	ADD, SUB, MUL, DIV	Rd, Rs1, Rs2	Standard integer arithmetic
Logic	AND, OR, XOR, NOT	Rd, Rs1, Rs2	Bitwise operations
Memory	LD, ST	Rd, [Rs1+imm]	Load/store word
Control Flow	BEQ, BNE, JMP	Rs1, Rs2, imm	Conditional/unconditional branch
Floating Point	FADD, FMUL, FDIV	Fd, Fs1, Fs2	FP arithmetic for AI inference
Vector Ops	VADD, VMUL	Vd, Vs1, Vs2	Parallel operations for image and geo computations
Geospatial	GEO_DIST	Rd, Rs1, Rs2	Compute haversine distance between coordinates
Geospatial	GEO_NEAR	Rd, Rs1, Rs2	Return nearest healthcare provider index
Fingerprint	FREC_MATCH	Rd, Rs1, Rs2	Compare biometric descriptors and return match score
Image Processing	IMG_SIFT	Rd, Rs1	Perform SIFT-like keypoint extraction

Image Processing	IMG_NORM	Rd, Rs1	Normalize descriptor vector
System/Power	SLP, WAKE	-	Enter/exit low-power mode for IoT edge devices

4. Instruction Encoding Summary

Format A (R-type):
Bits: 31–26 | 25–21 | 20–16 | 15–11 | 10–0
Fields: Opcode | Rs1 | Rs2 | Rd | Function code

Format B (I-type):
Bits: 31–26 | 25–21 | 20–16 | 15–0
Fields: Opcode | Rs1 | Rd | Immediate

Format C (S-type / AI special):
Bits: 31–26 | 25–21 | 20–16 | 15–0
Fields: Opcode | Rs1 | Rs2 | Sub-opcode / Mode

Opcode width: 6 bits | Register fields: 5 bits each | Immediate/Subcode: 16 bits | Total: 32 bits

5. Design Rationale & Trade-offs

Aspect	Discussion
Simplicity vs Capability	Core ISA remains RISC-based for simplicity, with specialized AI instructions for healthcare tasks.
Code Density vs Performance	Fixed 32-bit encoding simplifies decoding; vectorized instructions boost efficiency.
Hardware Impact	GEO and IMG instructions need vector units or FPUs but reduce software complexity and latency.
Extensibility	The ISA can easily be extended for ML accelerators or additional biometric algorithms.