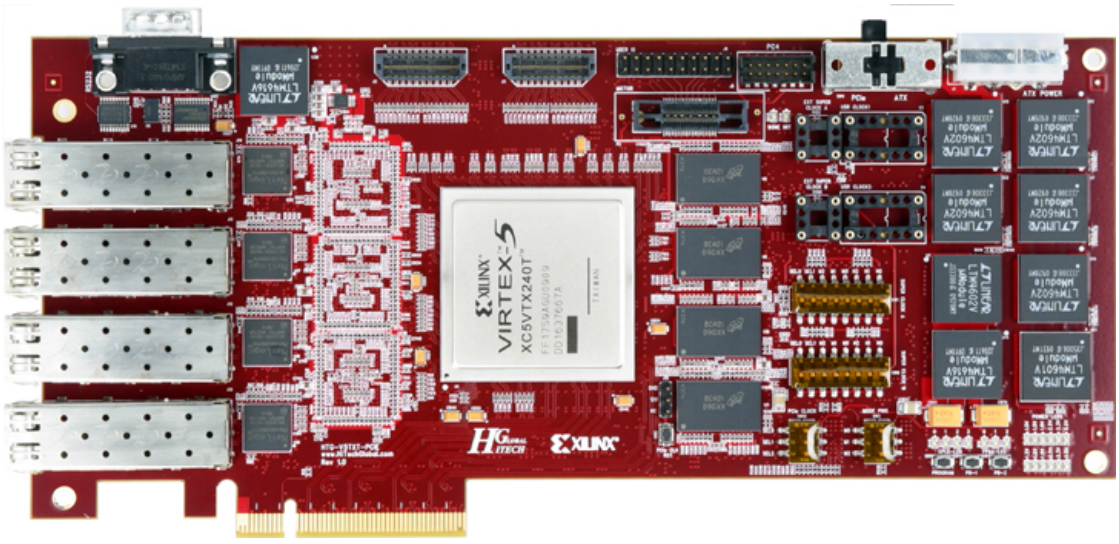
HiTech Global Virtex® 5 TX240T Development Platform

HTG-V5TXT-PCIE User Manual (preliminary)

Version 3.0 February 2010



HiTech Global does not assume any liability arising out of the application or use of any product described or shown herein; nor does it convey any license under its patents, copyrights, or mask work rights or any rights of others. HiTech Global reserves the right to make changes, at any time, in order to improve reliability and functionality of this product. HiTech Global will not assume responsibility for the use of any circuitry described herein other than circuitry entirely embodied in its products. HiTech Global provides any design, code, or information shown or described herein "as is." By providing the design, code, or information as one possible implementation of a feature, application, or standard, HiTech Global makes no representation that such implementation is free from any claims of infringement. End users are responsible for obtaining any rights they may require for their implementation. HiTech Global expressly disclaims any warranty whatsoever with respect to the adequacy of any such implementation, including but not limited to any warranties or representations that the implementation is free from claims of infringement, as well as any implied warranties of merchantability or fitness for a particular purpose.

HiTech Global will not assume any liability for the accuracy or correctness of any engineering or software support or assistance provided to a user. HiTech Global products are not intended for use in life support appliances, devices, or systems. Use of a HiTech Global product in such applications without the written consent of the appropriate HiTech Global officer is prohibited.

Revision History

Date	Version	Notes
11/1/2009	1.0	Preliminary
1/14/2010	2.0	
2/12/2010	3.0	

Table Of Contents

Chapter 1: Introduction to Virtex 5 TXT Platform

The Xilinx Virtex-5 TXT FPGA platform offers a low-risk path enabling manufacturers of telecommunications equipment to quickly prototype and bring to production new products that address the rapidly developing market for 100G networks. These FPGAs are ideal for building high-throughput line cards (40Gbps, 100Gbps+) for routers and switches, and high-density ports in data centers.

Their high-bandwidth capabilities also address the requirements of video broadcast and editing equipment, medical imaging systems, and other applications that must move large amounts of uncompressed video data.

Flexible Bridging

Incorporating up to 48 GTX multi-rate transceivers (twice the number found on any other available FPGA), these devices offer the bandwidth for single-FPGA bridging of key standards such as:

- 100G Ethernet to 120G Interlaken
- 40G Quad XAUI to 50G Interlaken
- OC-768 to OTU-3
- SFI-5 to 4x SFI4.2
- Customer-proprietary protocols

With up to 48 multi-rate transceivers, each supporting line rates from 150 Mbps to 6.5 Gbps, Virtex-5 TXT FPGAs provide the flexibility to build high-bandwidth interfaces for bridging between ASIC and ASSP devices on line cards and backplanes for networking routers and switches.

The Interlaken interface is emerging as a standard for high-bandwidth chip-to-chip interfaces in networking and telecommunications equipment for 40G and higher rates.

Virtex-5 TX240T FPGAs include more than 11Mbits of built-in Block RAM for buffering data streams. For implementations that require deeper buffers, Virtex-5 FPGAs make it easy to build reliable interfaces to the latest high-speed memories for over 10ms worth of buffering at 100Gbps. The user-configurable I/O pins on Virtex-5 FPGAs incorporate SelectIO™ technology that provides critical interface timing adjustment and signal integrity.

Use Virtex-5 TXT FPGAs to build a 40Gbps datapath for connecting an Ethernet switch to an NPU or ASIC. Multi-rate GTX transceivers and IP from Xilinx make it easy to build a quad XAUI interface. Multi-rate GTX transceivers implement SFI-5 protocol for bridging 40G SONET (OC-768) to long-haul DWDM (OTU-3) optical modules.

A single TXT device can support the ITU G.709 GFEC option. Alternatively, combining a Virtex-5 LXT FPGA with a TXT device enables implementation of more advanced FEC like ITU G.975I4 EFEC.

The flexibility of GTX transceivers makes it easy to interconnect four 10G NPU or packet processing devices (using SFI4.2) with a 40G framer (supporting SFI5) on a telecom line card

using a single TX150T FPGA. However, the TX240T provides additional logic capacity for integrating the 40G OC768 framer as well.

1.1) Summary of Virtex-5 TX240T FPGA Features

Table (1) provides high-level summary of Virtex-5 LX240T FPGA.

	XC5VTX240T
Slices	37,440
Logic Cells	239,616
CLB Flip-Flops	149,760
Maximum Distributed RAM (Kbits)	2,400
Block RAM/FIFO w/ECC (36Kbits each)	324
Total Block RAM (Kbits)	11,664
Digital Clock Managers (DCM)	12
Phase Locked Loop (PLL)/PMCD	6
Maximum Single-Ended Pins	680
Maximum Differential I/O Pairs	340
DSP48E Slices	96
PCI Express Endpoint Blocks	1
10/100/1000 Ethernet MAC Blocks	4
RocketIO™ GTX High-Speed Transceivers	48
Configuration Memory (Mbits)	65.8

Table (1): Main Virtex-5 TX240T FPGA Features

Additional product information is available at http://www.xilinx.com/products/virtex5/txt.htm

Chapter 2: Virtex 5 TXT FPGA Platform

2.1) Introduction

The HTG-V5TXT board is powered by Xilinx Virtex-5 XC5VTX240T FPGA which offers 48 GTX serial transceivers (6.5 Gbps), one x8 PCI Express Gen 1 End-point block and around 240,000 Logic cells. The board integrates the most fundamental electrical and optical interfaces for building 40G subsystems. It implements PCI Express Gen1/Gen2, SFP+, and high speed RLDRAM-II and QDR-II memory interfaces, and expansion connections for 20 GTX transceivers.

2.2) Main Features

► x1 Xilinx XC5VTX240T-2FFG1759 FPGA (RoHS Compliant)
► x8 PCI Express Gen 1/ Gen2 End-point Connector
► x4 SFP+ Connectors supported by Netlogic AEL2005 (10GbE LAN PHY/SerDes with EDC)
► Twenty Configurable GTX Serial Transceivers (available through two high-speed Samtec connectors)
► Three x36 QDR II (CY7C1515JV18)
► Four x36 RLDRAM II (MT49H16M36HT-25)
► x1 Mictor Connector for debugging
► x2 Platform XL Flash components (128mb each)
► x1 Xilinx XC2C256 CPLD
► x1 DB9 (RS232)
► User LEDs & Push Buttons
► PCIe and Stand Alone operation modes
► 4.25 " x 9.5 "

2.3) Kit Content

- The Virtex- 5 HTG-V5TXT-PCIE Board
- Jungo WinDriver™ Software Drivers for Linux and Windows (30-day Evaluation) – Also available at: http://www.jungo.com/st/partners/hitechglobal.html
- CD-ROM [Schematics (searchable .pdf), Gerber files (top & bottom), User Manual, User Constraint File (UCF), Reference Designs; PCIE Gen 1 Reference Designs (in binary format), QDRII, RLDRMII)

2.4) System Requirements

- Hardware:
  - PC or Server with PCI Express Gen 1 and/or 2 slot. The following PC Mother board with multiple PCIe slots is available through HiTech Global: (http://www.hitechglobal.com/Accessories/PCIExpress-Gen2_PC.htm
  - Xilinx USB Programming Cable (HW-USB-G)
- Software Tools
  - Xilinx ISE™ Foundation 11.1 (EF-ISE-FND)
  - PCI Express Driver (30-day evaluation version is provided)

2.5) Main Components & Placement

Figure (1) and (2) illustrate location and quantity of main components used on the HTG-V5TX-PCIE board.

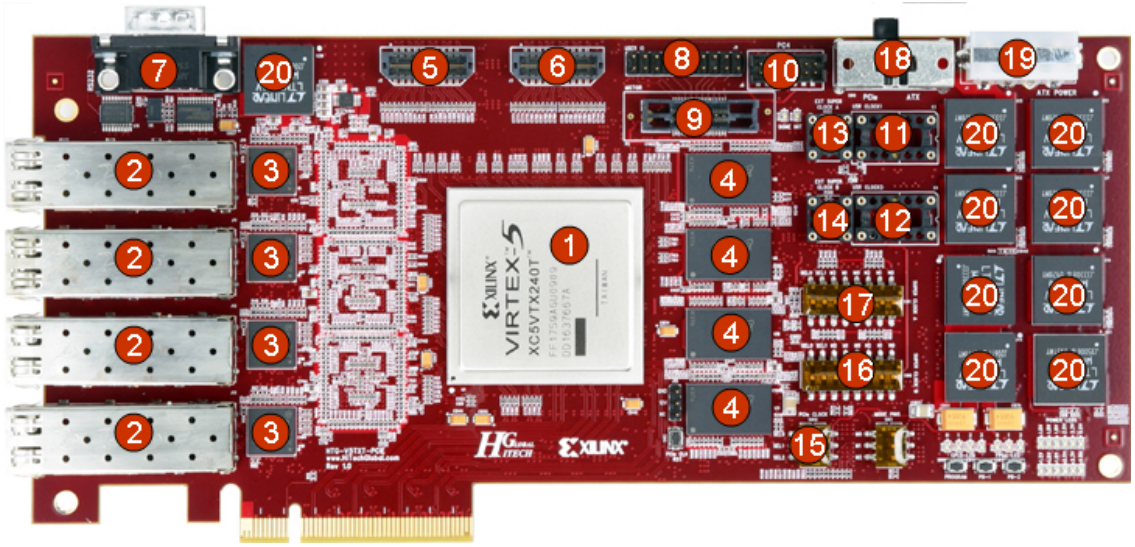


Figure (1): Front Side

(1) Virtex-5 TX240T FPGA, **(2)** SFP+ Cages, **(3)** 10GbE LAN PHY/SerDes with EDC **(4)** RLDRAM-II **(5)** Ten Configurable Serial Transceivers **(6)** Ten additional Configurable Serial Transceivers, **(7)** RS232 Port, **(8)** GPIO Headers, **(9)** Mictor Connector, **(10)** PC4 JTAG Connector, **(11)** Socket for User Clock #1, **(12)** Socket for User Clock # 2, **(13)** Socket for Super Clock #1, **(14)** Socket for Super Clock #2 **(15)** PCI Express Jitter Attenuator Switch, **(16)** Super Clock #2 Switch, **(17)** Super Clock #1 Switch **(18)** PCIe/ATX Switch, **(19)** ATX Power Connector, **(20)** Power Regulators

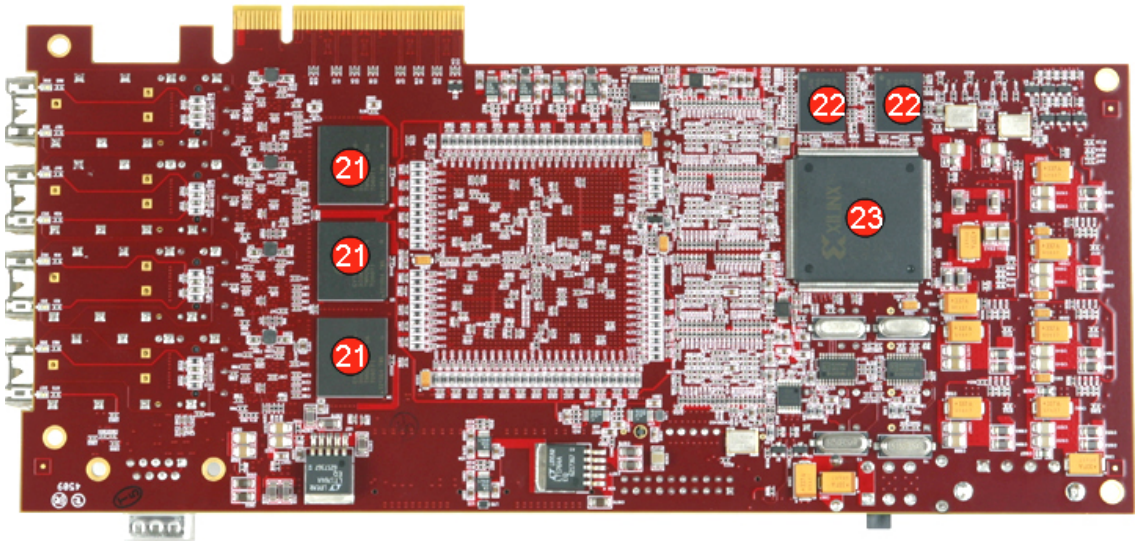


Figure (2): Back Side

(21) QDR-II, **(22)** Platform Flash XL, **(23)** CPLD

2.6) Power distribution

The HTG-V5TX-PCIE board is fully powered by External 12V ATX supply for stand-alone operation. The board is powered by both External 12V ATX supply and host PC in PCI Express mode. Figure (3) provides summary of power distribution for the board.

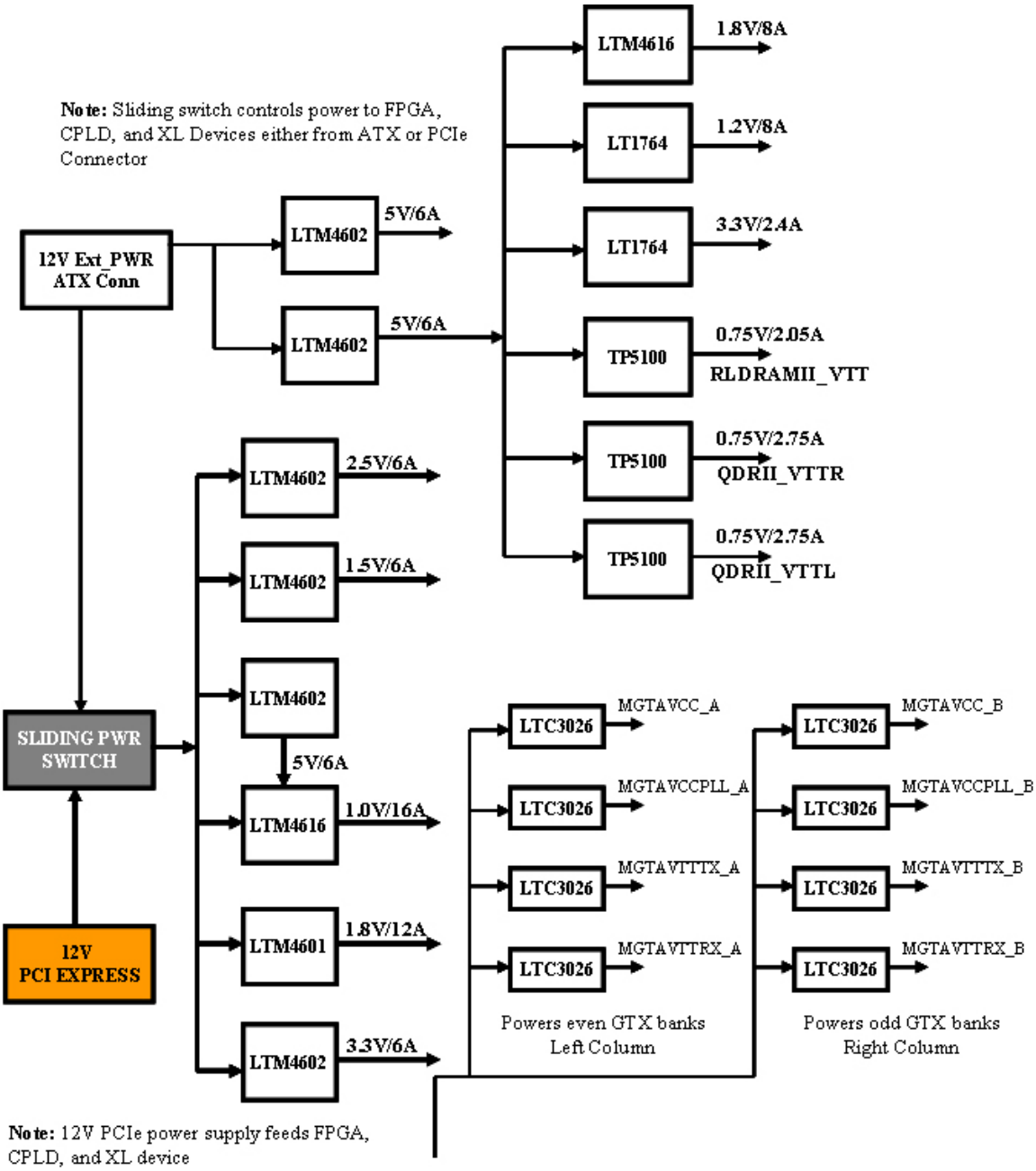


Figure (3): Power Distribution

2.7) Clock Distribution

The HTG-V5TXT platform provides flexible and effective clock distributions for the on-board FPGA via one differential and three single-ended clocks.

As illustrated by figure (4), the differential clock is generated by two fixed crystals, one socket for CAN oscillators and one low-jitter FEMTOClock Synthesizer. Table (2.a), (2.b), and (2.c) show different mode settings for the on-board clock synthesizer. Additional information for the frequency synthesizer is available at: http://www.idt.com/products/getDoc.cfm?docID=17250637

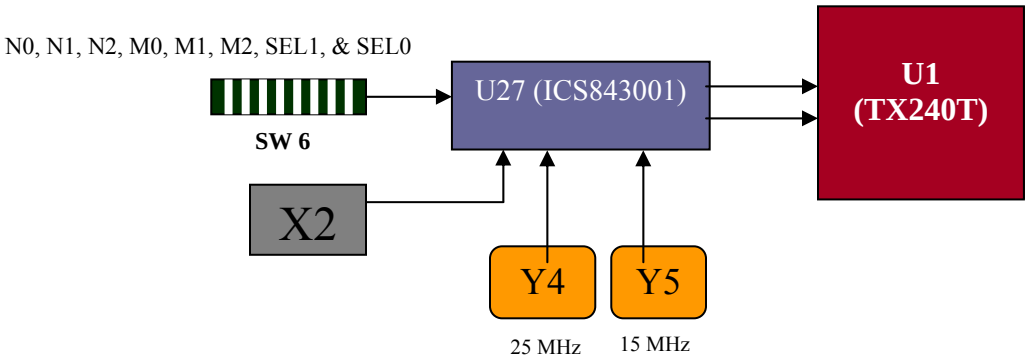


Figure (4): Differential Clock Circuit

Inputs			M Divider Value	Input Frequency (MHz)	
M2 (SW6: 6th key)	**M1** (SW6: 5th key)	**M0** (SW6: 4th key)		Minimum	Maximum
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

Table (2.a): ICS843001 (U27) Programmable "M" Output Divider Function Table

Inputs			M Divider Value
N2 (SW6: 3rd key)	**N1** (SW6: 2nd key)	**N0** (SW6: 1st key)	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

Table (2.b) ICS843001 (U27) Programmable "N" Output Divider Function Table

Inputs			Outputs	
F_SEL2	**F_SEL1**	**F_SEL0**	**QA0/nQA0, QA0/nQA0**	**QB0/nQB0**
0	0	0	2 ÷	2÷
1	0	0	5÷	2÷
0	1	0	4÷	2 ÷
1	1	0	2÷	4÷
0	0	1	2 ÷	5÷
1	0	1	5÷	4÷
0	1	1	4÷	5÷
1	1	1	4÷	4÷

Table (2.c): ICS874003 (U27) F_SEL[2:0] Function Table

The single-ended FPGA clocks are provided by two on-board fixed crystals with 100 MHz (X5) and 25 MHz (X6) values. Two additional sockets (X3 and X4) are also available for user defined CAN crystals.

Table (3) provides FPGA pin assignment for each clock.

Clock Name	Description	FPGA Pin #
FPGA_SPRCK_N	Differential clock generated by the FPGA Super clock (U27) - Negative	AM26
FPGA_SPRCK_P	Differential clock generated by the FPGA Super clock (U27) - Positive	AL26
USR_100MHz	Single ended clock generated by the X5 crystal	AN25
USR_25MHz	Single ended clock generated by the X6 crystal	AJ25
USR_OSC_CLK1	Single ended clock generated by the X3 socket	AN20
USR_OSC_CLK2	Single ended clock generated by the X4 socket	AL25

Table (3): FPGA Clock Pin Assignment

2.8) PCI Express

Figure (5) : 8-Lane PCI Express End-Point

The TX240T FPGA's GTX Serial Transceivers are used as PCI Express Physical Layer interface (PHY) The HTG-TX240T board can be used for PCI Express Gen 1 x1/x2/x4/x8 (using on-chip hard-coded PCIe block) or Gen 2 x1/x2/x4 (using soft IP core provided by HiTech Global)

As illustrated in table (3), eight GTX Serial Transceivers of the on-board Virtex-5 TX240T FPGA are connected to an 8-lane upstream connector for PCIE end point applications.

FPGA Pin Description	FPGA Pin Number	PCIe Signal Name	PCIe Connector Pin
MGTTXP0_114	AB22	PER0_C_P	A16
MGTTXN0_114	AF2	PER0_C_N	A17
MGTRXP0_114	AC1	PET0_P	B14
MGTRXN0_114	AD1	PET0_N	B15
MGTRXP1_114	AF1	PET1_P	B19
MGTRXN1_114	AE1	PET1_N	B20
MGTTXP1_114	AG2	PER1_C_P	A21
MGTTXN1_114	AF2	PER1_C_N	A22
MGTTXP0_118	AH2	PER2_C_P	A25
MGTTXN0_118	AJ2	PER2_C_N	A26
MGTRXP0_118	AJ1	PET2_P	B23
MGTRXN0_118	AK1	PET2_N	B24
MGTRXP1_118	AM1	PET3_P	B27
MGTRXN1_118	AL1	PET3_N	B28
MGTTXP1_118	AN2	PER3_C_P	A29
MGTTXN1_118	AM2	PER3_C_N	A30
MGTTXP0_122	AP2	PER4_C_P	A35
MGTTXN0_122	AR2	PER4_C_N	A36
MGTRXP0_122	AR1	PET4_P	B33
MGTRXN0_122	AT1	PET4_N	B34
MGTRXP1_122	AV1	PET5_P	B37
MGTRXN1_122	AU1	PET5_N	B38

MGTTXP1_122	AW2	PER5_C_P	A39
MGTTXN1_122	AV2	PER5_C_N	A40
MGTREFCLKP_122	**AT4**	**PCIECLK0_P**	**A13**
MGTREFCLKN_ 122	**AT3**	**PCIECLK0_N**	**A14**
MGTTXP0_126	BA1	PER6_C_P	A43
MGTTXN0_126	BA2	PER6_C_N	A44
MGTRXP0_126	BB2	PET6_P	B41
MGTRXN0_126	BB3	PET6_N	B42
MGTRXP1_126	BB5	PET7_P	B45
MGTRXN1_126	BB4	PET7_N	B46
MGTTXP1_126	BA6	PER7_C_P	A47
MGTTXN1_126	BA5	PER7_C_N	A48

Table (3) PCI Express Upstream Connections Summary

PCI Express Jitter Attenuator

The HTG-TX240T board is supported by an IDT ICS874003-05 PCI Express Jitter Attenuator Chip. This chip is a high performance Differential- to-LVDS Jitter Attenuator designed for use in PCI Express systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. This jitter attenuator chip can also convert the 100 MHz clock coming from host PC to different derivatives.

Figures (6) and Table (4) illustrate the implementation of the attenuator chip and output frequency selection modes.

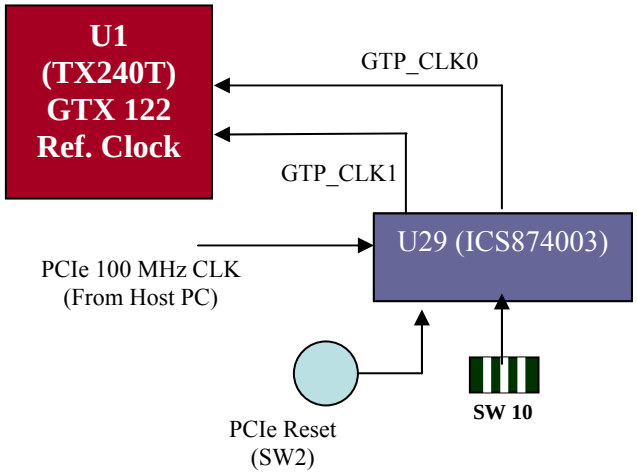


Figure (6) PCI Express Jitter Attenuator Diagram

Figure (7) PCIe Jitter Attenuator Control (SW10)

INPUT (SW10)			OUTPUT
F_SEL2	F_SEL1	F_SEL0	QB0/nQB0
0	0	0	DIV2 (250 MHz when input = 100 MHz)
1	0	0	DIV2 (250 MHz when input = 100 MHz)
0	1	0	DIV2 (250 MHz when input = 100 MHz)
1	1	0	DIV4 (125 MHz when input = 100 MHz)
0	0	1	DIV5 (100 MHz when input = 100 MHz)
1	0	1	DIV4 (125 MHz when input = 100 MHz)
0	1	1	DIV5 (100 MHz when input = 100 MHz)
1	1	1	DIV4 (125 MHz when input = 100 MHz)

Table (4) PCI Express Jitter Attenuator Mode Select

2.9) SFP+

The HTG-TX240T board is supported by four independent SFP+ (10Gbps) interfaces. As illustrated by figure (7) each interface is consisted of one SFP+ Cage , one Physical Layer transceiver chip (Netlogic AEL2005) with an integrated Electronic Dispersion Compensation (EDC) engine and four Serial Transceivers connecting to the TX240T FPGA.

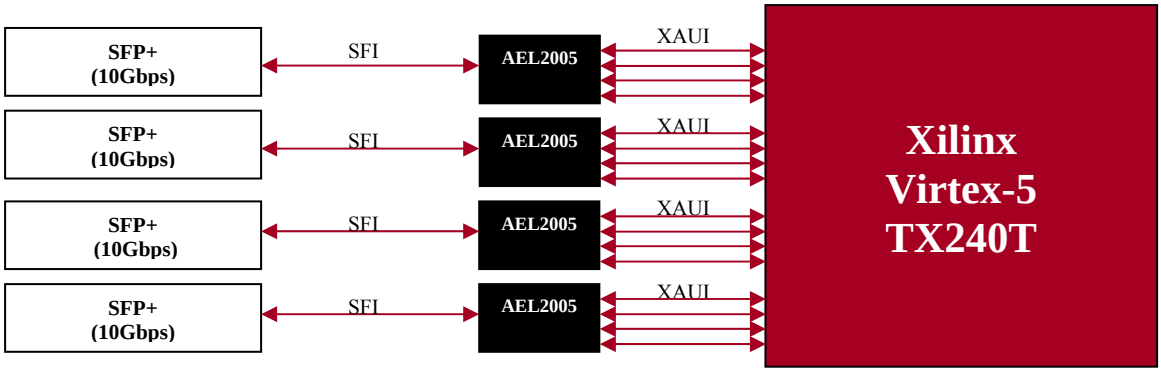


Figure (7) SFP+ Interface

AEL2005 device is a physical layer transceiver with an integrated Electronic Dispersion Compensation (EDC) engine - compliant with IEEE802.3aq specifications. The device integrates NetLogic Microsystems' SerDes/PHY technology low-power EDC engine with up to 5db of margin over the symmetric stress test pulse sensitivity specifications defined in the 10GASE-LRM standard.

The NetLogic Microsystems AEL2005 device provides full PCS, PMA, and XGXS sub-layer functionality through the consolidation of the receiver and transmitter PHY functions on a single chip along with the integration of encode/decode/alignment logic, FIFOs, on-chip clock drivers, multiple loop-back features and PRBS & Ethernet frame generation & verification for both the line side and the system side.

As illustrated by figure (9.a) the entire SFP+ interface is supported by an independent clock circuit providing identical clock distribution across all four connectors.

Note: XAUI lanes to J11, J12, J13 AEL2005s are reversed for smooth routing.

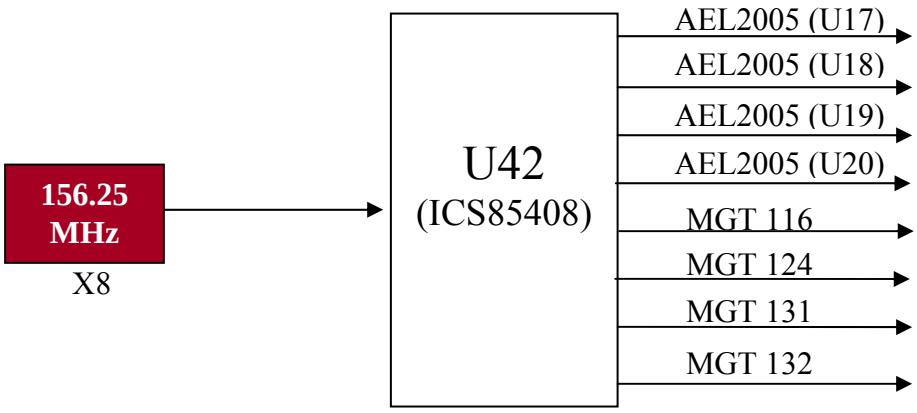


Figure (9.a) SFP+ Clock Distribution

As illustrated by figure (9.b) a 125MHz clock is available for 1Gbps Ethernet mode. This clock should disabled by "J16" jumper when the HTG-V5TXT board is used 10Gb mode.

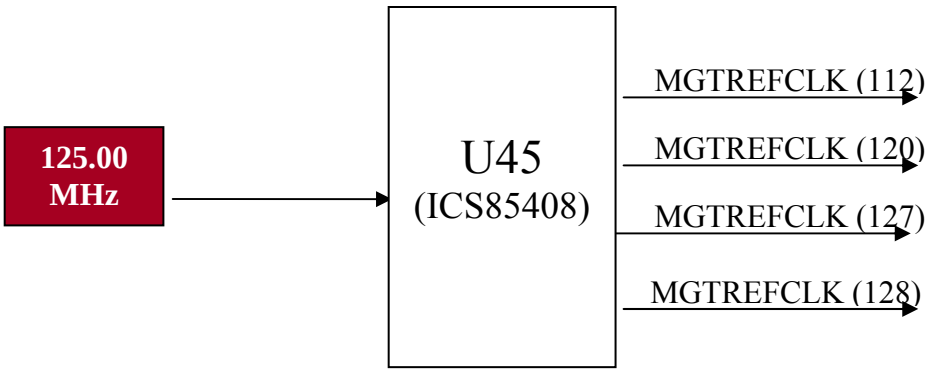


Figure (9.b) Clock Distribution for 1Gb Ethernet Mode

2.10) QDR-II Memory

The HTG-TX240T board is populated with three Cypress QDRII Components with part number CY7C1515JV18-300BZXC.

The CY7C1515JV18 is 1.8V Synchronous Pipelined SRAMs, equipped with QDR II architecture. QDR II architecture consists of two separate ports: the read port and the write port to access the memory array. The read port has dedicated data outputs to support read operations and the write port has dedicated data inputs to support write operations. QDR II architecture has separate data inputs and data outputs to completely eliminate the need to "turn-around" the data bus that exists with common I/O devices. Each port is accessed through a common address bus. Addresses for read and write addresses are latched on alternate rising edges of the input (K) clock. Accesses to the QDR II read and write ports are completely independent of one another. To maximize data throughput, both read and write ports are equipped with DDR interfaces. Each address location is associated with four 36-bit words that burst sequentially into or out of the device. Because data is transferred into and out of the device on every rising edge of both input clocks (K and K and C and C), memory bandwidth is maximized while simplifying system design by eliminating bus 'turnarounds'.

Depth expansion is accomplished with port selects, which enables each port to operate independently.

All synchronous inputs pass through input registers controlled by the K or K input clocks. All data outputs pass through output registers controlled by the C or C (or K or K in a single clock domain) input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Additional product information is available at http://www.cypress.com/?docID=18672

Table (5), (6), and (7) illustrate FPGA's pin assignment for each interface.

Signal Name (QDR II "A" – U4)	FPGA Pin Number	FPGA Bank #
QDR2_A_DQ0	K30	27
QDR2_A_DQ1	L30	27
QDR2_A_DQ2	H30	27
QDR2_A_DQ3	J30	27
QDR2_A_DQ4	L32	27
QDR2_A_DQ5	M33	27
QDR2_A_DQ6	F31	27
QDR2_A_DQ7	G31	27
QDR2_A_DQ8	M32	27
QDR2_A_DQ9	M31	27
QDR2_A_DQ10	F30	27
QDR2_A_DQ11	N30	27
QDR2_A_DQ12	N31	27
QDR2_A_DQ13	F29	27
QDR2_A_DQ14	E29	27
QDR2_A_DQ15	P32	27
QDR2_A_DQ16	P31	27

QDR2_A_DQ17	H29	27
QDR2_A_DQ18	G29	27
QDR2_A_DQ19	R30	27
QDR2_A_DQ20	P30	27
QDR2_A_DQ21	H33	27
QDR2_A_DQ22	J32	27
QDR2_A_DQ23	G36	27
QDR2_A_DQ24	F35	27
QDR2_A_DQ25	G34	27
QDR2_A_DQ26	F34	27
QDR2_A_DQ27	E36	27
QDR2_A_DQ28	F32	27
QDR2_A_DQ29	G32	27
QDR2_A_DQ30	F37	27
QDR2_A_DQ31	E37	27
QDR2_A_DQ32	J31	27
QDR2_A_DQ33	H31	27
QDR2_A_DQ34	K32	27
QDR2_A_DQ35	L29	27
QDR2_A_CQ_P	L31	27
QDR2_A_CQ_N	K29	27
QDR2_A_D0	Y29	11
QDR2_A_D1	Y30	11
QDR2_A_D2	W31	11
QDR2_A_D3	W30	11
QDR2_A_D4	AA31	11
QDR2_A_D5	AA30	11
QDR2_A_D6	Y35	11
QDR2_A_D7	AA35	11
QDR2_A_D8	U33	11
QDR2_A_D9	AB36	11
QDR2_A_D10	AC36	11
QDR2_A_D11	V33	11
QDR2_A_D12	U32	11
QDR2_A_D13	AA34	11
QDR2_A_D14	AB34	11
QDR2_A_D15	V31	11
QDR2_A_D16	U31	11
QDR2_A_D17	AB31	11
QDR2_A_D18	AB32	11
QDR2_A_D19	W36	11
QDR2_A_D20	W35	11
QDR2_A_D21	Y37	11
QDR2_A_D22	AA37	11
QDR2_A_D23	V36	11
QDR2_A_D24	W37	11
QDR2_A_D25	AA36	11
QDR2_A_D26	W32	11

QDR2_A_D27	W33	11
QDR2_A_D28	AA32	11
QDR2_A_D29	Y32	11
QDR2_A_D30	V34	11
QDR2_A_D31	V35	11
QDR2_A_D32	Y34	11
QDR2_A_D33	Y33	11
QDR2_A_D34	T37	11
QDR2_A_D35	U37	11
QDR2_A_A0	H34	23
QDR2_A_A1	J33	23
QDR2_A_A2	M36	23
QDR2_A_A3	N36	23
QDR2_A_A4	N33	23
QDR2_A_A5	P33	23
QDR2_A_A6	R32	23
QDR2_A_A7	R33	23
QDR2_A_A8	N34	23
QDR2_A_A9	J35	23
QDR2_A_A10	J36	23
QDR2_A_A11	L37	23
QDR2_A_A12	M37	23
QDR2_A_A13	K38	23
QDR2_A_A14	K37	23
QDR2_A_A15	T32	23
QDR2_A_A16	T31	23
QDR2_A_A17	K35	23
QDR2_A_A18	L34	23
QDR2_A_BW0B	P37	23
QDR2_A_BW1B	R38	23
QDR2_A_BW2B	P36	23
QDR2_A_BW3B	J38	23
QDR2_A_RW_B	P38	23
QDR2_A_LD	G37	23
QDR2_A_K_N	K33	23
QDR2_A_K_P	K34	23
QDR2_A_C_N	N35	23
QDR2_A_C_P	P35	23
QDR2_A_DOFF_B	J37	23

Table (5): FPGA Pin Assignment for QDR-II "A" Component (U4)

NOTE:
1.DATA (D0-D35) INPUT SIGNALS ARE SAMPLED ON RISING EDGE OF K AND K#
2.DATA (DQ0-DQ35) OUTPUT SIGNALS ARE DRIVEN OUT ON RISING EDGE OF C AND C#
3.BWS ARE SAMPLED ON THE RISING EDGE OF K AND #K CLOCKS WHEN WRITE OPERATIONS ARE ACTIVE
4.BWS DETERMINES WHICH BYTE IS WRITTEN INTO DEVICE

BWS0 - D[8:0], BWS1 - D[17:9], BWS2 - D[26:18], BWS3 - D[35:27]

Signal Name (QDR II "B" – U5)	FPGA Pin Number	FPGA Bank #
QDR2_B_DQ0	J21	7
QDR2_B_DQ1	J22	7
QDR2_B_DQ2	H21	7
QDR2_B_DQ3	J20	7
QDR2_B_DQ4	A22	7
QDR2_B_DQ5	B21	7
QDR2_B_DQ6	C20	7
QDR2_B_DQ7	D20	7
QDR2_B_DQ8	F24	7
QDR2_B_DQ9	G23	7
QDR2_B_DQ10	A20	7
QDR2_B_DQ11	N23	7
QDR2_B_DQ12	M23	7
QDR2_B_DQ13	K20	7
QDR2_B_DQ14	L20	7
QDR2_B_DQ15	E23	7
QDR2_B_DQ16	E24	7
QDR2_B_DQ17	P22	7
QDR2_B_DQ18	P21	7
QDR2_B_DQ19	E25	7
QDR2_B_DQ20	F25	7
QDR2_B_DQ21	M21	7
QDR2_B_DQ22	N21	7
QDR2_B_DQ23	L22	7
QDR2_B_DQ24	M22	7
QDR2_B_DQ25	E22	7
QDR2_B_DQ26	D23	7
QDR2_B_DQ27	D22	7
QDR2_B_DQ28	G22	7
QDR2_B_DQ29	F22	7
QDR2_B_DQ30	D21	7
QDR2_B_DQ31	C21	7
QDR2_B_DQ32	L21	7
QDR2_B_DQ33	K22	7
QDR2_B_DQ34	B23	7
QDR2_B_DQ35	G21	7
QDR2_B_CQ_P	B22	7
QDR2_B_CQ_N	F21	7
QDR2_B_D0	M19	3
QDR2_B_D1	L19	3
QDR2_B_D2	M24	3
QDR2_B_D3	N24	3
QDR2_B_D4	J16	3
QDR2_B_D5	J15	3
QDR2_B_D6	L25	3
QDR2_B_D7	M26	3

QDR2_B_D8	K15	3
QDR2_B_D9	L15	3
QDR2_B_D10	L27	3
QDR2_B_D11	L26	3
QDR2_B_D12	M18	3
QDR2_B_D13	M17	3
QDR2_B_D14	K28	3
QDR2_B_D15	K27	3
QDR2_B_D16	L17	3
QDR2_B_D17	L16	3
QDR2_B_D18	M27	3
QDR2_B_D19	M28	3
QDR2_B_D20	P25	1
QDR2_B_D21	P26	1
QDR2_B_D22	P18	1
QDR2_B_D23	N19	1
QDR2_B_D24	N25	1
QDR2_B_D25	N26	1
QDR2_B_D26	P17	1
QDR2_B_D27	N18	1
QDR2_B_D28	N28	1
QDR2_B_D29	M14	1
QDR2_B_D30	L14	1
QDR2_B_D31	N29	1
QDR2_B_D32	M29	1
QDR2_B_D33	N16	1
QDR2_B_D34	M16	1
QDR2_B_D35	R27	1
QDR2_B_A0	J23	5
QDR2_B_A1	K23	5
QDR2_B_A2	K19	5
QDR2_B_A3	K18	5
QDR2_B_A4	J25	5
QDR2_B_A5	K25	5
QDR2_B_A6	F27	5
QDR2_B_A7	G27	5
QDR2_B_A8	E19	5
QDR2_B_A9	H26	5
QDR2_B_A10	J26	5
QDR2_B_A11	F16	5
QDR2_B_A12	F17	5
QDR2_B_A13	G28	5
QDR2_B_A14	H28	5
QDR2_B_A15	G16	5
QDR2_B_A16	H16	5
QDR2_B_A17	J27	5
QDR2_B_A18	J28	5
QDR2_B_BW0B	F20	5

QDR2_B_BW1B	L24	5
QDR2_B_BW2B	H19	5
QDR2_B_BW3B	G24	5
QDR2_B_RW_B	E20	5
QDR2_B_LD	K24	5
QDR2_B_K_N	H23	5
QDR2_B_K_P	G19	5
QDR2_B_C_N	F19	5
QDR2_B_C_P	H25	5
QDR2_B_DOFF_B	G17	5

Table (6): FPGA Pin Assignment for QDR-II "B" Component (U5)

NOTE:
1.DATA (D0-D35) INPUT SIGNALS ARE SAMPLED ON RISING EDGE OF K AND K#
2.DATA (DQ0-DQ35) OUTPUT SIGNALS ARE DRIVEN OUT ON RISING EDGE OF C AND C#
3.BWS ARE SAMPLED ON THE RISING EDGE OF K AND #K CLOCKS WHEN WRITE OPERATIONS ARE ACTIVE
4.BWS DETERMINES WHICH BYTE IS WRITTEN INTO DEVICE
BWS0 - D[8:0], BWS1 - D[17:9], BWS2 - D[26:18], BWS3 - D[35:27]

Signal Name (QDR II "C" – U6)	FPGA Pin Number	FPGA Bank #
QDR2_C_DQ0	F9	28
QDR2_C_DQ1	F10	28
QDR2_C_DQ2	L11	28
QDR2_C_DQ3	L10	28
QDR2_C_DQ4	F12	28
QDR2_C_DQ5	G12	28
QDR2_C_DQ6	M13	28
QDR2_C_DQ7	N13	28
QDR2_C_DQ8	G13	28
QDR2_C_DQ9	H13	28
QDR2_C_DQ10	M11	28
QDR2_C_DQ11	F14	28
QDR2_C_DQ12	E14	28
QDR2_C_DQ13	N11	28
QDR2_C_DQ14	P11	28
QDR2_C_DQ15	G14	28
QDR2_C_DQ16	F15	28
QDR2_C_DQ17	R12	28
QDR2_C_DQ18	P12	28
QDR2_C_DQ19	H15	28
QDR2_C_DQ20	H14	28
QDR2_C_DQ21	H10	28
QDR2_C_DQ22	J11	28
QDR2_C_DQ23	F11	28
QDR2_C_DQ24	G11	28
QDR2_C_DQ25	H9	28
QDR2_C_DQ26	G9	28

QDR2_C_DQ27	E12	28
QDR2_C_DQ28	K10	28
QDR2_C_DQ29	J10	28
QDR2_C_DQ30	J13	28
QDR2_C_DQ31	K14	28
QDR2_C_DQ32	K12	28
QDR2_C_DQ33	K13	28
QDR2_C_DQ34	J12	28
QDR2_C_DQ35	M12	28
QDR2_C_CQ_P	H11	28
QDR2_C_CQ_N	L12	28
QDR2_C_D0	P5	12
QDR2_C_D1	R5	12
QDR2_C_D2	AA10	12
QDR2_C_D3	AA11	12
QDR2_C_D4	T7	12
QDR2_C_D5	U7	12
QDR2_C_D6	W10	12
QDR2_C_D7	W11	12
QDR2_C_D8	AC9	12
QDR2_C_D9	V9	12
QDR2_C_D10	V8	12
QDR2_C_D11	AC10	12
QDR2_C_D12	AD11	12
QDR2_C_D13	P7	12
QDR2_C_D14	R7	12
QDR2_C_D15	AB11	12
QDR2_C_D16	AC11	12
QDR2_C_D17	N6	12
QDR2_C_D18	P6	12
QDR2_C_D19	Y8	12
QDR2_C_D20	Y7	12
QDR2_C_D21	T5	12
QDR2_C_D22	T6	12
QDR2_C_D23	Y10	12
QDR2_C_D24	AA9	12
QDR2_C_D25	V6	12
QDR2_C_D26	AA6	12
QDR2_C_D27	AA7	12
QDR2_C_D28	Y9	12
QDR2_C_D29	W8	12
QDR2_C_D30	AC6	12
QDR2_C_D31	AB6	12
QDR2_C_D32	W6	12
QDR2_C_D33	W7	12
QDR2_C_D34	AB7	12
QDR2_C_D35	AB8	12
QDR2_C_A0	U12	24

QDR2_C_A1	V11	24
QDR2_C_A2	R10	24
QDR2_C_A3	P10	24
QDR2_C_A4	P8	24
QDR2_C_A5	R9	24
QDR2_C_A6	T10	24
QDR2_C_A7	T11	24
QDR2_C_A8	J6	24
QDR2_C_A9	N8	24
QDR2_C_A10	M8	24
QDR2_C_A11	M9	24
QDR2_C_A12	N9	24
QDR2_C_A13	M6	24
QDR2_C_A14	M7	24
QDR2_C_A15	K8	24
QDR2_C_A16	J7	24
QDR2_C_A17	L7	24
QDR2_C_A18	K7	24
QDR2_C_BW0B	G8	24
QDR2_C_BW1B	U11	24
QDR2_C_BW2B	E8	24
QDR2_C_BW3B	U9	24
QDR2_C_RW_B	G7	24
QDR2_C_LD	V10	24
QDR2_C_K_N	L6	24
QDR2_C_K_P	F6	24
QDR2_C_C_N	G6	24
QDR2_C_C_P	U8	24
QDR2_C_DOFF_B	H5	24

Table (7): FPGA Pin Assignment for QDR-II "C" Component (U6)

NOTE:
1.DATA (D0-D35) INPUT SIGNALS ARE SAMPLED ON RISING EDGE OF K AND K#
2.DATA (DQ0-DQ35) OUTPUT SIGNALS ARE DRIVEN OUT ON RISING EDGE OF C AND C#
3.BWS ARE SAMPLED ON THE RISING EDGE OF K AND #K CLOCKS WHEN WRITE OPERATIONS ARE ACTIVE
4.BWS DETERMINES WHICH BYTE IS WRITTEN INTO DEVICE
BWS0 - D[8:0], BWS1 - D[17:9], BWS2 - D[26:18], BWS3 - D[35:27]

2.11) RLDRAM-II Memory

The HTG-TX240T board is populated with two Micron RLDRAM II Components with part number MT49H16M36HT-25:A

The Micron® reduced latency DRAM (RLDRAM®) II is a high-speed memory device designed for high bandwidth data storage—telecommunications, networking, and cache applications, etc. The chip's 8-bank architecture is optimized for sustainable high speed operation.

The DDR I/O interface transfers two data words per clock cycle at the I/O balls. Output data is referenced to the free-running output data clock.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock(s).

Read and write accesses to the RLDRAM are burst-oriented. The burst length (BL) is programmable from 2, 4, or 8 by setting the mode register.

The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

Bank-scheduled refresh is supported with the row address generated internally.

Additional product information is available at
http://download.micron.com/pdf/datasheets/rldram/MT49H16M36A.pdf

Table (8), and (9) illustrate FPGA's pin assignment for each interface.

Signal Name (RLDRAM "A") (U8 & U9)	FPGA Pin Number	FPGA Bank #
RLD2_A_DQ0	AH29	29
RLD2_A_DQ1	AH30	29
RLD2_A_DQ2	AT32	29
RLD2_A_DQ3	AR32	29
RLD2_A_DQ4	AT29	29
RLD2_A_DQ5	AN30	29
RLD2_A_DQ6	AM29	29
RLD2_A_DQ7	AV30	29
RLD2_A_DQ8	AU29	29
RLD2_A_DQ9	AL30	29
RLD2_A_DQ10	AL29	29
RLD2_A_DQ11	AU31	29
RLD2_A_DQ12	AV31	29
RLD2_A_DQ13	AT31	29
RLD2_A_DQ14	AT30	29
RLD2_A_DQ15	AP28	29
RLD2_A_DQ16	AN28	29
RLD2_A_DQ17	AJ30	29

RLD2_A_DQ18	AH31	29
RLD2_A_DQ19	AT25	29
RLD2_A_DQ20	AT26	29
RLD2_A_DQ21	AK29	29
RLD2_A_DQ22	AV25	29
RLD2_A_DQ23	AV26	29
RLD2_A_DQ24	AT34	29
RLD2_A_DQ25	AU34	29
RLD2_A_DQ26	AT27	29
RLD2_A_DQ27	AU27	29
RLD2_A_DQ28	AR33	29
RLD2_A_DQ29	AR34	29
RLD2_A_DQ30	AN29	29
RLD2_A_DQ31	AM28	29
RLD2_A_DQ32	AK34	25
RLD2_A_DQ33	AJ33	25
RLD2_A_DQ34	AK33	25
RLD2_A_DQ35	AK32	25
RLD2_A_DQ36	AP37	25
RLD2_A_DQ37	AP31	25
RLD2_A_DQ38	AN31	25
RLD2_A_DQ39	AN35	25
RLD2_A_DQ40	AN36	25
RLD2_A_DQ41	AM32	25
RLD2_A_DQ42	AM31	25
RLD2_A_DQ43	AM36	25
RLD2_A_DQ44	AL35	25
RLD2_A_DQ45	AL32	25
RLD2_A_DQ46	AL31	25
RLD2_A_DQ47	AU37	25
RLD2_A_DQ48	AT36	25
RLD2_A_DQ49	AU36	25
RLD2_A_DQ50	AV36	25
RLD2_A_DQ51	AJ32	25
RLD2_A_DQ52	AJ31	25
RLD2_A_DQ53	AR35	25
RLD2_A_DQ54	AR37	25
RLD2_A_DQ55	AT37	25
RLD2_A_DQ56	AN34	25
RLD2_A_DQ57	AM34	25
RLD2_A_DQ58	AP35	25
RLD2_A_DQ59	AP36	25
RLD2_A_DQ60	AM33	25
RLD2_A_DQ61	AN33	25
RLD2_A_DQ62	AK35	25
RLD2_A_DQ63	AL34	25
RLD2_A_A0	AJ36	13
RLD2_A_A1	AG37	13

RLD2_A_A2	AG36	13
RLD2_A_A3	AG31	13
RLD2_A_A4	AG32	13
RLD2_A_A5	AC33	13
RLD2_A_A6	AB33	13
RLD2_A_A7	AG33	13
RLD2_A_A8	AG34	13
RLD2_A_A9	AD37	13
RLD2_A_A10	AF31	13
RLD2_A_A11	AF32	13
RLD2_A_A12	AE35	13
RLD2_A_A13	AD35	13
RLD2_A_A14	AL36	13
RLD2_A_A15	AL37	13
RLD2_A_A16	AC30	13
RLD2_A_A17	AC31	13
RLD2_A_A18	AN38	13
RLD2_A_A19	AM38	13
RLD2_A_WE-B	AC34	13
RLD2_A_REF_B	AC35	13
RLD2_A_CLK0_N	AE34	13
RLD2_A_CLK0_P	AF34	13
RLD2_A_ CLK1_N	AE37	13
RLD2_A_CLK1_P	AF37	13
RLD2_A_DK0_N	AD30	13
RLD2_A_DK0_P	AD31	13
RLD2_A_DK1_N	AD33	13
RLD2_A_DK1_P	AD32	13
RLD2_A_DK2_N	AG38	13
RLD2_A_DK2_P	AH38	13
RLD2_A_DK3_N	AE32	13
RLD2_A_DK3_P	AE33	13
RLD2_A_BA0	AF35	13
RLD2_A_BA1	AF36	13
RLD2_A_BA2	AH36	13
RLD2_A_CS0_B	AK37	13
RLD2_A_CS1_B	AR30	29
RLD2_A_QK0_N	AR29	29
RLD2_A_QK0_P	AR28	29
RLD2_A_QK1_N	AU33	29
RLD2_A_QK1_P	AU32	29
RLD2_A_QK2_N	AH33	25
RLD2_A_QK2_P	AH34	25
RLD2_A_QK3_N	AP33	25
RLD2_A_QK3_P	AP32	25
RLD2_A_QVLD0	AP30	29
RLD2_A_QVLD1	AJ35	25

Table (8): FPGA Pin Assignment for RLDRAM-II "A" Component s (U5) & (U9)

NOTE:
CLK0_P AND CLK0_N MASTER CLK U10
CLK1_P AND CLK1_N MASTER CLK U11
DQ0-DQ17 **INPUT** ARE REFERENCED TO DK0_P AND DK0_N
DQ18-DQ35 **INPUT** ARE REFERENCED TO DK1_P AND DK1_N
DQ0-DQ8 **OUTPUT** ARE REFERENCED TO QK0_P AND QK0_N
DQ9-DQ17 **OUTPUT** ARE REFERENCED TO QK1_P AND QK1_N
DQ18-DQ26 **OUTPUT** ARE REFERENCED TO QK2_P AND QK2_N
DQ27-DQ35 **OUTPUT** ARE REFERENCED TO QK3_P AND QK3_N

Signal Name (RLDRAM "B") (U10 & U11)	FPGA Pin Number	FPGA Bank #
RLD2_B_DQ0	AR18	30
RLD2_B_DQ1	AR19	30
RLD2_B_DQ2	AU16	30
RLD2_B_DQ3	AT16	30
RLD2_B_DQ4	AP15	30
RLD2_B_DQ5	AP16	30
RLD2_B_DQ6	AR15	30
RLD2_B_DQ7	AL14	30
RLD2_B_DQ8	AM14	30
RLD2_B_DQ9	AT15	30
RLD2_B_DQ10	AU14	30
RLD2_B_DQ11	AV13	30
RLD2_B_DQ12	AU12	30
RLD2_B_DQ13	AL15	30
RLD2_B_DQ14	AK15	30
RLD2_B_DQ15	AH15	30
RLD2_B_DQ16	AJ15	30
RLD2_B_DQ17	AP18	30
RLD2_B_DQ18	AN18	30
RLD2_B_DQ19	AG13	30
RLD2_B_DQ20	AH14	30
RLD2_B_DQ21	AL16	30
RLD2_B_DQ22	AJ13	30
RLD2_B_DQ23	AH13	30
RLD2_B_DQ24	AU17	30
RLD2_B_DQ25	AU18	30
RLD2_B_DQ26	AK14	30
RLD2_B_DQ27	AK13	30
RLD2_B_DQ28	AR17	30
RLD2_B_DQ29	AT17	30
RLD2_B_DQ30	AR13	30
RLD2_B_DQ31	AT12	30
RLD2_B_DQ32	AR9	26
RLD2_B_DQ33	AR8	26
RLD2_B_DQ34	AT6	26

RLD2_B_DQ35	AU6	26
RLD2_B_DQ36	AU11	26
RLD2_B_DQ37	AN8	26
RLD2_B_DQ38	AP8	26
RLD2_B_DQ39	AR12	26
RLD2_B_DQ40	AP13	26
RLD2_B_DQ41	AM8	26
RLD2_B_DQ42	AM9	26
RLD2_B_DQ43	AN13	26
RLD2_B_DQ44	AM13	26
RLD2_B_DQ45	AP7	26
RLD2_B_DQ46	AR6	26
RLD2_B_DQ47	AT9	26
RLD2_B_DQ48	AR10	26
RLD2_B_DQ49	AK10	26
RLD2_B_DQ50	AL10	26
RLD2_B_DQ51	AN11	26
RLD2_B_DQ52	AP10	26
RLD2_B_DQ53	AJ10	26
RLD2_B_DQ54	AP12	26
RLD2_B_DQ55	AP11	26
RLD2_B_DQ56	AN10	26
RLD2_B_DQ57	AN9	26
RLD2_B_DQ58	AL11	26
RLD2_B_DQ59	AM11	26
RLD2_B_DQ60	AT7	26
RLD2_B_DQ61	AR7	26
RLD2_B_DQ62	AK12	26
RLD2_B_DQ63	AJ12	26
RLD2_B_A0	AM5	14
RLD2_B_A1	AM7	14
RLD2_B_A2	AM6	14
RLD2_B_A3	AD6	14
RLD2_B_A4	AD7	14
RLD2_B_A5	AG11	14
RLD2_B_A6	AF11	14
RLD2_B_A7	AF7	14
RLD2_B_A8	AE8	14
RLD2_B_A9	AH11	14
RLD2_B_A10	AF6	14
RLD2_B_A11	AF5	14
RLD2_B_A12	AL9	14
RLD2_B_A13	AK9	14
RLD2_B_A14	AH5	14
RLD2_B_A15	AG6	14
RLD2_B_A16	AG9	14
RLD2_B_A17	AF10	14
RLD2_B_A18	AH6	14

RLD2_B_A19	AG7	14
RLD2_B_WE-B	AF12	14
RLD2_B_REF_B	AG12	14
RLD2_B_CLK0_N	AH8	14
RLD2_B_CLK0_P	AG8	14
RLD2_B_ CLK1_N	AL7	14
RLD2_B_CLK1_P	AK8	14
RLD2_B_DK0_N	AE9	14
RLD2_B_DK0_P	AF9	14
RLD2_B_DK1_N	AP6	14
RLD2_B_DK1_P	AP5	14
RLD2_B_DK2_N	AJ8	14
RLD2_B_DK2_P	AH9	14
RLD2_B_DK3_N	AJ7	14
RLD2_B_DK3_P	AJ6	14
RLD2_B_BA0	AE10	14
RLD2_B_BA1	AD10	14
RLD2_B_BA2	AN5	14
RLD2_B_CS0_B	AK7	14
RLD2_B_CS1_B	AU13	30
RLD2_B_QK0_N	AN15	30
RLD2_B_QK0_P	AN14	30
RLD2_B_QK1_N	AP17	30
RLD2_B_QK1_P	AN16	30
RLD2_B_QK2_N	AL12	26
RLD2_B_QK2_P	AM12	26
RLD2_B_QK3_N	AV7	26
RLD2_B_QK3_P	AU8	26
RLD2_B_QVLD0	AT14	30
RLD2_B_QVLD1	AT10	26

Table (9): FPGA Pin Assignment for RLDRAM-II "A" Component s (U10) & (U11)

NOTE:
CLK0_P AND CLK0_N MASTER CLK U10
CLK1_P AND CLK1_N MASTER CLK U11
DQ0-DQ17 **INPUT** ARE REFERENCED TO DK0_P AND DK0_N
DQ18-DQ35 **INPUT** ARE REFERENCED TO DK1_P AND DK1_N
DQ0-DQ8 **OUTPUT** ARE REFERENCED TO QK0_P AND QK0_N
DQ9-DQ17 **OUTPUT** ARE REFERENCED TO QK1_P AND QK1_N
DQ18-DQ26 **OUTPUT** ARE REFERENCED TO QK2_P AND QK2_N
DQ27-DQ35 **OUTPUT** ARE REFERENCED TO QK3_P AND QK3_N

2.12) General Purpose Serial Transceiver Ports

The HTG-V5TXT provides access to 20 data-rate-adjustable GTX Serial Transceivers which can support serial standards with data rates from 150 mbps to 6.5 Gbps. These transceivers are accessible through two Samtec (QTH-020-01-F-D-DP-A) High-speed connectors J(2) and J(3). Each connector provides access to 10 GTX Serial Transceivers.

Table (10) and (11) illustrate pin assignment for each GTX Serial Transceiver on the Virtex-5 TX240T FPGA and QTH high-speed connectors:

Expansion Connector # J2 (Upper Left)					
Connector Pin #	Signal Name (RX Side)	FPGA Pin #	Connector Pin #	Signal Name (TX Side)	FPGA Pin #
1	GTRX0_N (MGTRXN0_123)	A39	2	GTTX0_N (MGTTXN0_123)	B38
3	GTRX0_P (MGTRXP0_123)	A38	4	GTTX0_P (MGTTXP0_123)	B37
5	GTRX1_N (MGTRXN1_123)	A40	6	GTTX1_N (MGTTXN1_123)	B41
7	GTRX1_P (MGTRXP1_123)	A41	8	GTTX1_P (MGTTXP1_123)	B42
9	GTRX2_N (MGTRXN0_119)	F42	10	GTTX2_N (MGTTXN0_119)	E41
11	GTRX2_P (MGTRXP0_119)	E42	12	GTTX2_P (MGTTXP0_119)	D41
13	GTRX3_N (MGTRXN1_119)	G42	14	GTTX3_N (MGTTXN1_119)	G41
15	GTRX3_P (MGTRXP1_119)	H42	16	GTTX3_P (MGTTXP1_119)	J41
17	GTRX4_N (MGTRXN0_115)	M42	18	GTTX4_N (MGTTXN0_115)	L41
19	GTRX4_P (MGTRXP0_115)	L42	20	GTTX4_P (MGTTXP0_115)	K41
21	GTRX5_N (MGTRXN1_115)	N42	22	GTTX5_N (MGTTXN1_115)	P41
23	GTRX5_P (MGTRXP1_115)	P42	24	GTTX5_P (MGTTXP1_115)	R41
25	GTRX6_N (MGTRXN0_111)	V42	26	GTTX6_N (MGTTXN0_111)	U41
27	GTRX6_P (MGTRXP0_111)	U42	28	GTTX6_P (MGTTXP0_111)	T41
29	GTRX7_N (MGTRXN1_111)	W42	30	GTTX7_N (MGTTXN1_111)	Y41
31	GTRX7_P (MGTRXP1_111)	Y42	32	GTTX7_P (MGTTXP1_111)	AA41
33	GTRX8_N (MGTRXN0_113)	AD42	34	GTTX8_N (MGTTXN0_113)	AC41
34	GTRX8_P (MGTRXP0_113)	AC42	36	GTTX8_P (MGTTXP0_113)	AB41

37	GTRX9_N (MGTRXN1_113)	AE42		38	GTTX9_N (MGTTXN1_113)	AF41
39	GTRX9_P (MGTRXP1_113)	AF42		40	GTTX9_P (MGTTXP1_113)	AG41

Table (10) : Distribution of General Purpose RocketIO Ports – "J2" Connector

Expansion Connector # J3 (Upper Right)					
Connector Pin #	Signal Name	FPGA Pin #	Connector Pin #	Signal Name	FPGA Pin #
1	GTRX10_N (MGTRXN0_117)	AK42	2	GTTX10_N (MGTTXN10_117)	AJ41
3	GTRX10_P (MGTRXP0_117)	AJ42	4	GTTX0_P (MGTTXP0_117)	AH41
5	GTRX11_N (MGTRXN1_117)	AL42	6	GTTX11_N (MGTTXN11_117)	AM41
7	GTRX11_P (MGTRXP1_117)	AM42	8	GTTX11_P (MGTTXP1_117)	AN41
9	GTRX12_N (MGTRXN0_121)	AT42	10	GTTX12_N (MGTTXN0_121)	AR41
11	GTRX12_P (MGTRXP0_121)	AR42	12	GTTX12_P (MGTTXP0_121)	AP41
13	GTRX13_N (MGTRXN1_121)	AU42	14	GTTX13_N (MGTTXN1_121)	AV41
15	GTRX13_P (MGTRXP1_121)	AV42	16	GTTX13_P (MGTTXP1_121)	AW41
17	GTRX14_N (MGTRXN0_125)	BB40	18	GTTX14_N (MGTTXN0_125)	BA41
19	GTRX14_P (MGTRXP0_125)	BB41	20	GTTX14_P (MGTTXP0_125)	BA42
21	GTRX15_N (MGTRXN1_125)	BB39	22	GTTX15_N (MGTTXN1_125)	BA38
23	GTRX15_P (MGTRXP1_125)	BB38	24	GTTX15_P (MGTTXP1_125)	BA37
25	GTRX16_N (MGTRXN0_129)	BB34	26	GTTX16_N (MGTTXN0_129)	BA35
27	GTRX16_P (MGTRXP0_129)	BB35	28	GTTX16_P (MGTTXP0_129)	BA36
29	GTRX17_N (MGTRXN1_129)	BB33	30	GTTX17_N (MGTTXN1_129)	BA32
31	GTRX17_P (MGTRXP1_129)	BB32	32	GTTX17_P (MGTTXP1_129)	BA31
33	GTRX18_N (MGTRXN0_133)	BB28	34	GTTX18_N (MGTTXN0_133)	BA29
34	GTRX18_P (MGTRXP0_133)	BB29	36	GTTX18_P (MGTTXP0_133)	BA30
37	GTRX19_N (MGTRXN1_133)	BB27	38	GTTX19_N (MGTTXN1_133)	BA26
39	GTRX19_P (MGTRXP1_133)	BB26	40	GTTX19_P (MGTTXP1_133)	BA25

Table (11) : Distribution of General Purpose RocketIO Ports. – "J3" Connector

Serial Transceivers Super Clock

The on-board super clock provides different reference clocks for generating different data throughputs. As illustrated by figure (10) three GTX reference clocks (SM_CLK0, SM_CLK1, and SM_CLK2) are generated by the on-board oscillators (15MHz, 25MHz, or other values through pluggable CAN), frequency synthesizer, and buffer. Table (12) provides FPGA pin assignment for these reference clocks. Table (13.a) and (13.b) show different mode settings for the on-board clock synthesizer. Additional information for the frequency synthesizer is available at: http://www.idt.com/products/getDoc.cfm?docID=17250637

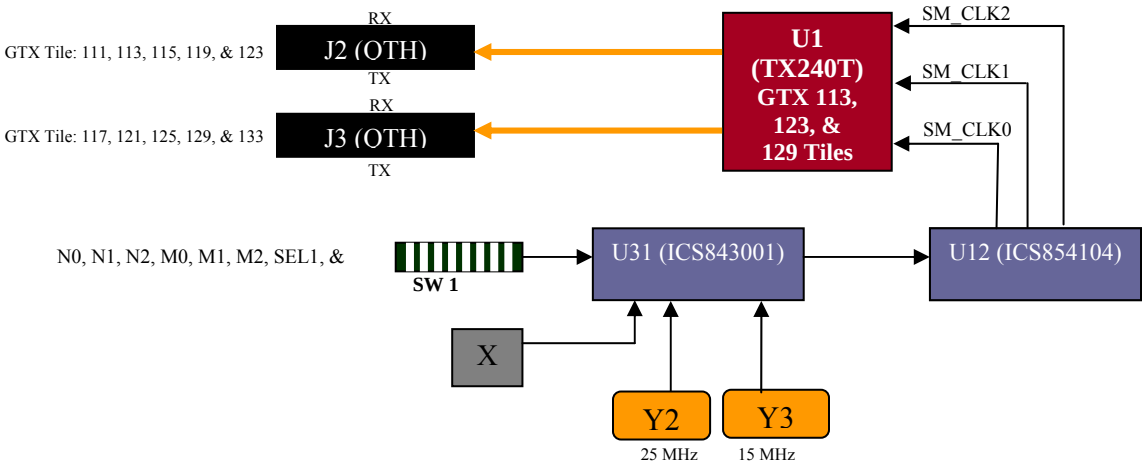


Figure (10) Adjustable Reference Clock for General Purpose RocketIO Ports

Reference Clock	Description	FPGA Pin #
SM_CLK0_N	Reference Clock for GTX # 123	C40
SM_CLK0_P	Reference Clock for GTX # 123	C39
SM_CLK1_N	Reference Clock for GTX # 113	AD40
SM_CLK1_P	Reference Clock for GTX # 113	AD39
SM_CLK2_N	Reference Clock for GTX # 129	AY34
SM_CLK2_P	Reference Clock for GTX # 129	AW34

Table(12) GTX Reference Clock Pin Assignment

Inputs			M Divider Value	Input Frequency (MHz)	
M2 (SW1: 6th key)	**M1** (SW1: 5th key)	**M0** (SW1: 4th key)		Minimum	Maximum
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

Table (13.a) ICS843001 (U31) Programmable "M" Output Divider Function Table

Inputs			M Divider Value
N2 (SW1: 3rd key)	**N1** (SW1: 2nd key)	**N0** (SW1: 1st key)	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

Table (13.b) ICS843001 (U31) Programmable "N" Output Divider Function Table

2.13) UART Interface:

The HTG-V5TXT board is supported by one UART Controller chip (Maxim MAX3380E) which has two receivers and two transmitters. The MAX3380E is capable of transmitting data at rates of 460kbps while maintaining RS-232 output levels. The MAX3381E offers a slower slew rate for applications where noise and EMI are issues.

Table (14) illustrates FPGA pin assignment for the UART interface.

Pin Description/Name	FPGA Pin #
RS232_T1N	BB21
RS232_T2N	BA22
RS232_R1OUT	BB23
RS232_R2OUT	BB22

Table (14): FPGA Pin Assignment for UART

2.14) Debug & GPIO Port

The HTG-V5TXT board is supported by one Mictor connector (part # 2-5767004-2) which simultaneously shares the same signals with a 20-pin General Purpose IO (GPIO) header. These connectors can be used for debugging purpose.

Table (15) illustrates FPGA pin assignment for the Debug and GPIO interfaces.

Pin Description/Name	FPGA Pin #
MICTOR01	AV20
MICTOR02	AW20
MICTOR03	AM23
MICTOR04	AN24
MICTOR05	AT19
MICTOR06	AU19
MICTOR07	AV23
MICTOR08	AU23
MICTOR09	BA21
MICTOR10	AY22

Table (15): FPGA Pin Assignment for UART

2.15) LEDs & Push Buttons

The HTG-V5TXT provides user LEDs and Push Buttons.

Table (16) illustrates FPGA pins assignment for the LED and Push Buttons.

Signal Name	Reference Designator	FPGA Pin #
LED01	DS9	AK25
LED02	DS10	AM24
LED03	DS11	AP20
PB01	SW4	AL24
PB02	SW5	AN19

Table (16): User Applications

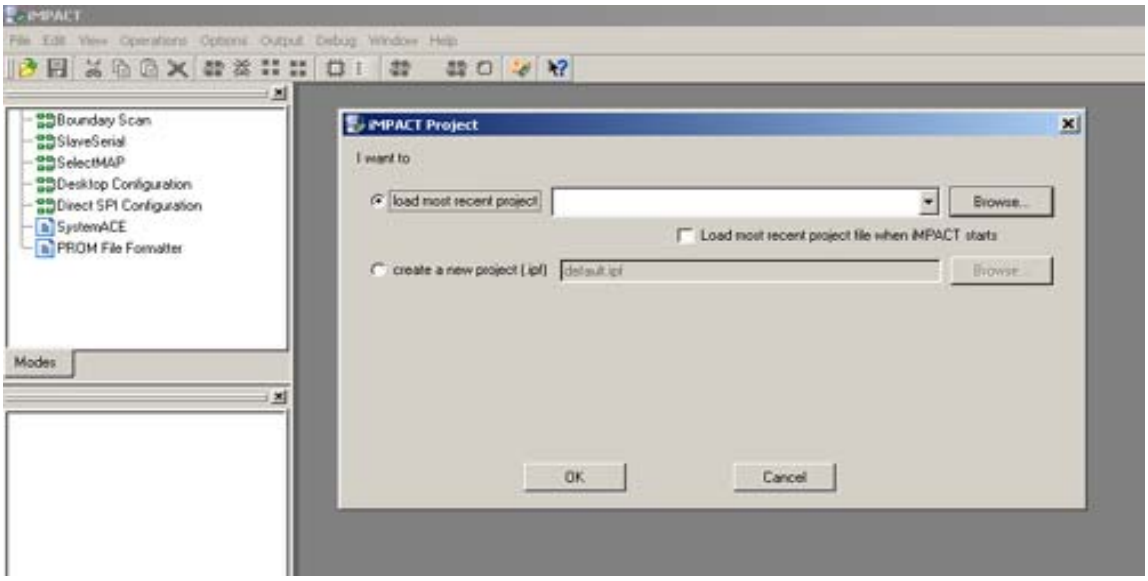
2.16) Configuration Options

The HTG-V5TXT board can be configured directly via JTAG (J6), Platform Flash XL (U40 and U41), and CPLD (U39).

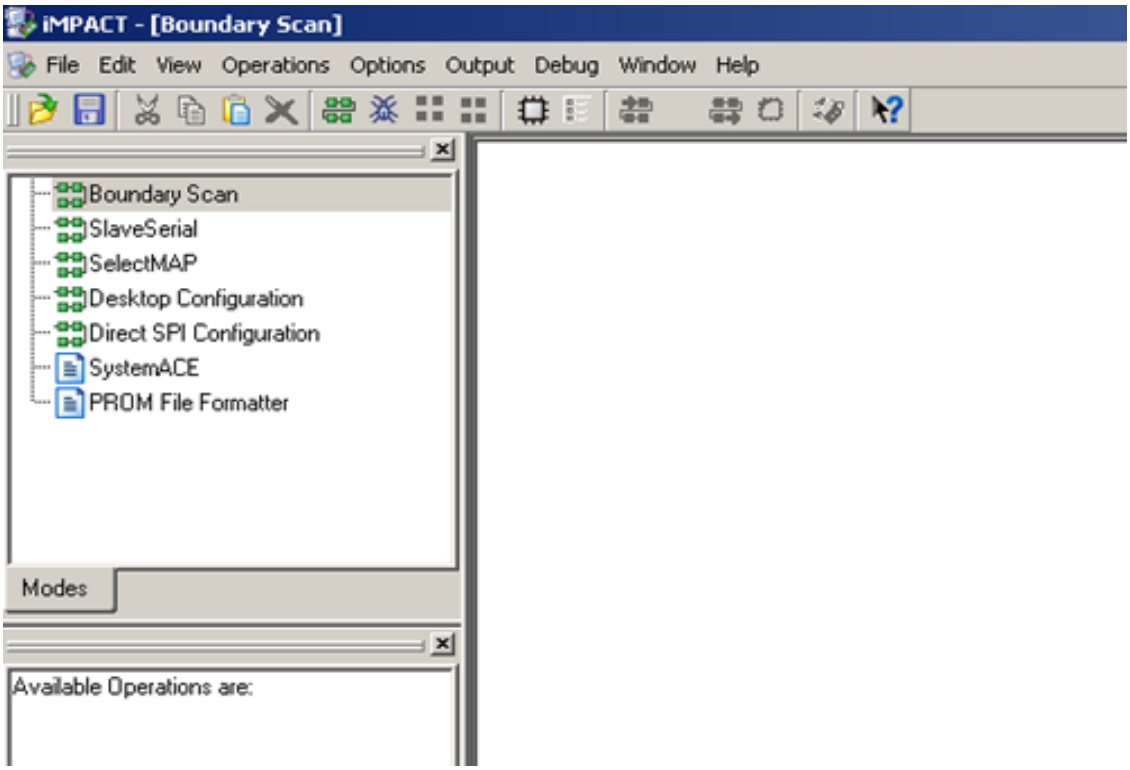
2.16.1) Direct FPGA Configuration

1) Connect the 14-pin header of the Xilinx USB programming cable to the **"J6"** connector. The USB header should be connected to USB port of a **PC** on the other side. The Xilinx ISE 10.1i (or higher version) should already been installed on the PC.
2) Power up the HTG-V5TXT boardvia ATX power connectors
3) Launch the ISE **"iMPACT"** tool:
   Start → All Programs → Xilinx ISE → Accessories → iMPACT.

4) Cancel the following window (iMPACT Project). This leads to verification of on-board Xilinx components.



5) Double Click on the "**Boundary Scan"** (the first item on the list) and Single Click on the **"Initialize Chain"** icon (the 7th icon from the left on the tool bar). This verifies correct connection between the board and PC by identifying the on-board Xilinx components in the chain (Platform Flash and FPGA).



Additional reading for Boundary Scan:

Virtex-5 devices support IEEE standards 1149.1 and 1532. IEEE 1532 is a standard for In-System Configuration (ISC), based on the IEEE 1149.1 standard. JTAG is an acronym for the Joint Test Action Group, the technical subcommittee initially responsible for developing the standard. This standard provides a means to ensure the board-level integrity of individual components and the interconnections between them. The IEEE 1149.1 Test Access Port and Boundary-Scan Architecture is commonly referred to as JTAG. With multi-layer PC boards becoming increasingly dense and more sophisticated surface
mounting techniques in use, Boundary-Scan testing is becoming widely used as an important debugging tool.

Devices containing Boundary-Scan logic can send data out on I/O pins in order to test connections between devices at the board level. The circuitry can also be used to send signals internally to test the device-specific behavior. These tests are commonly used to detect opens and shorts at both the board and device level.

In addition to testing, Boundary-Scan offers the flexibility for a device to have its own set of user-defined instructions. The added common vendor-specific instructions, such as configure and verify, have increased the popularity of Boundary-Scan testing and functionality.

Additional information is available at: http://direct.xilinx.com/bvdocs/userguides/ug191.pdf

6) At this stage you should program the FPGA with a .bit file.

Technical Support:

Technical support can be provided by contacting support@HiTechGlobal.com Support requests are responded in less than 24 hours.

Sales Support:

Sales support can be provided by contacting info@HiTechGlobal.com or +1 408 781-8043 (8:00 AM – 6:00 PM Pacific Standard Time)