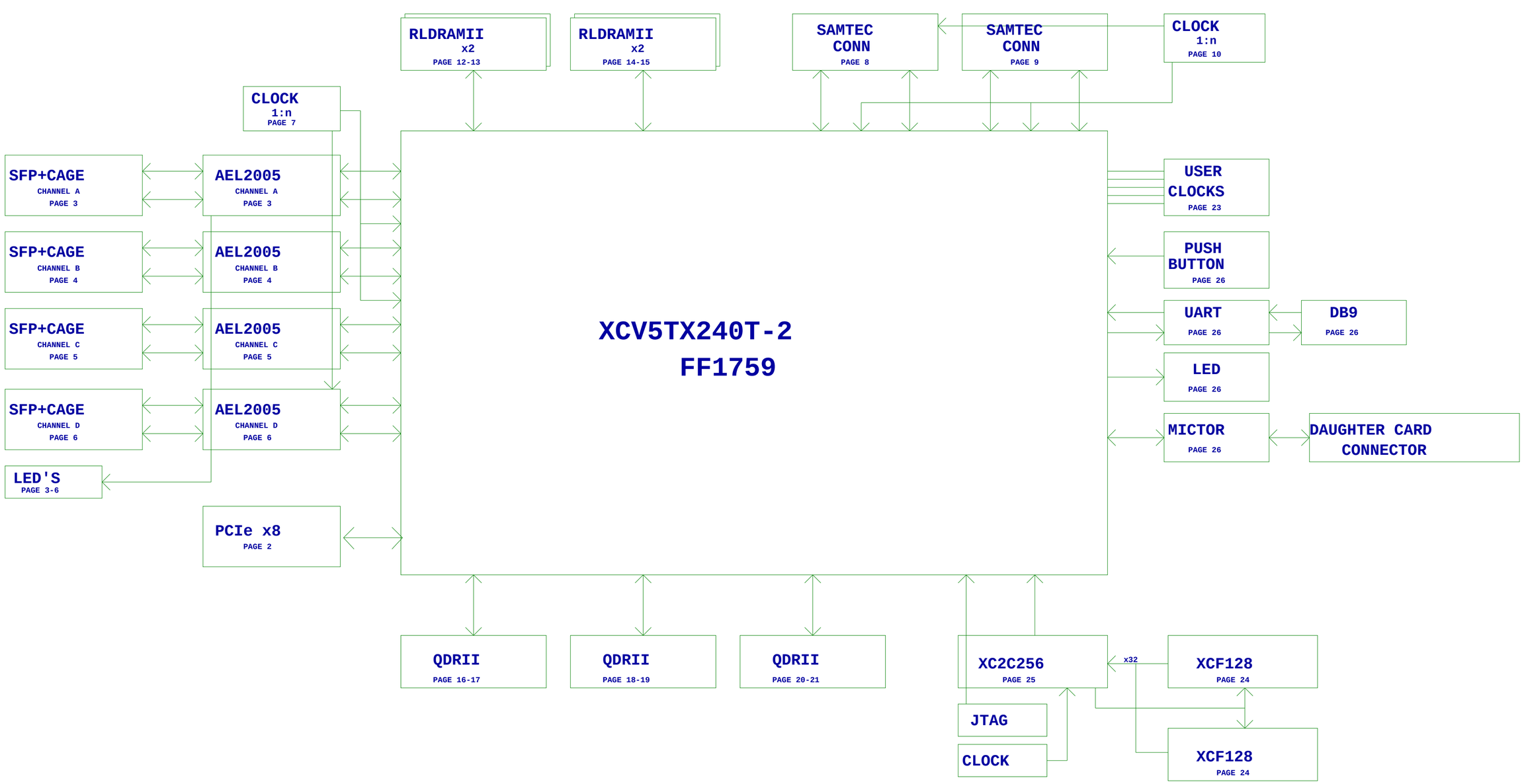
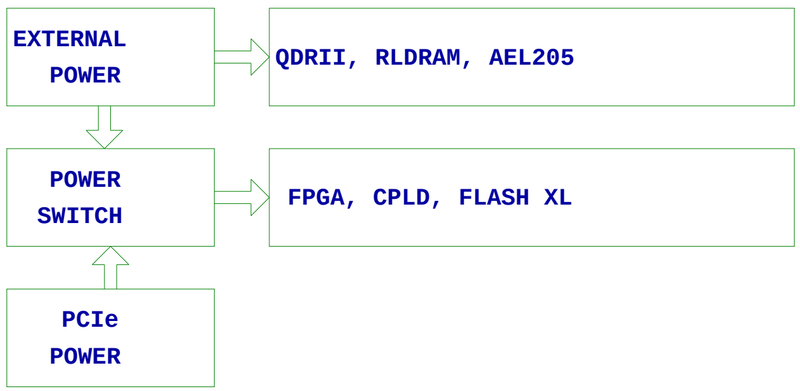


POWER SCHEME (PAGE 28-31)



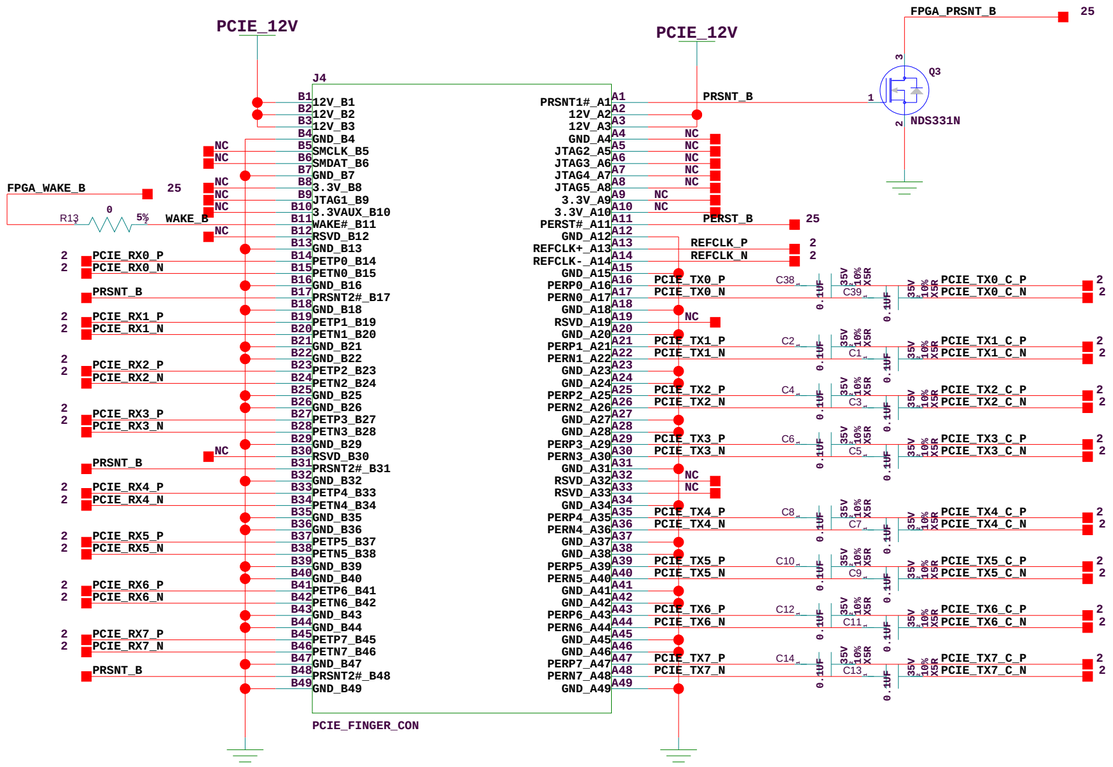
CONFIDENTIAL

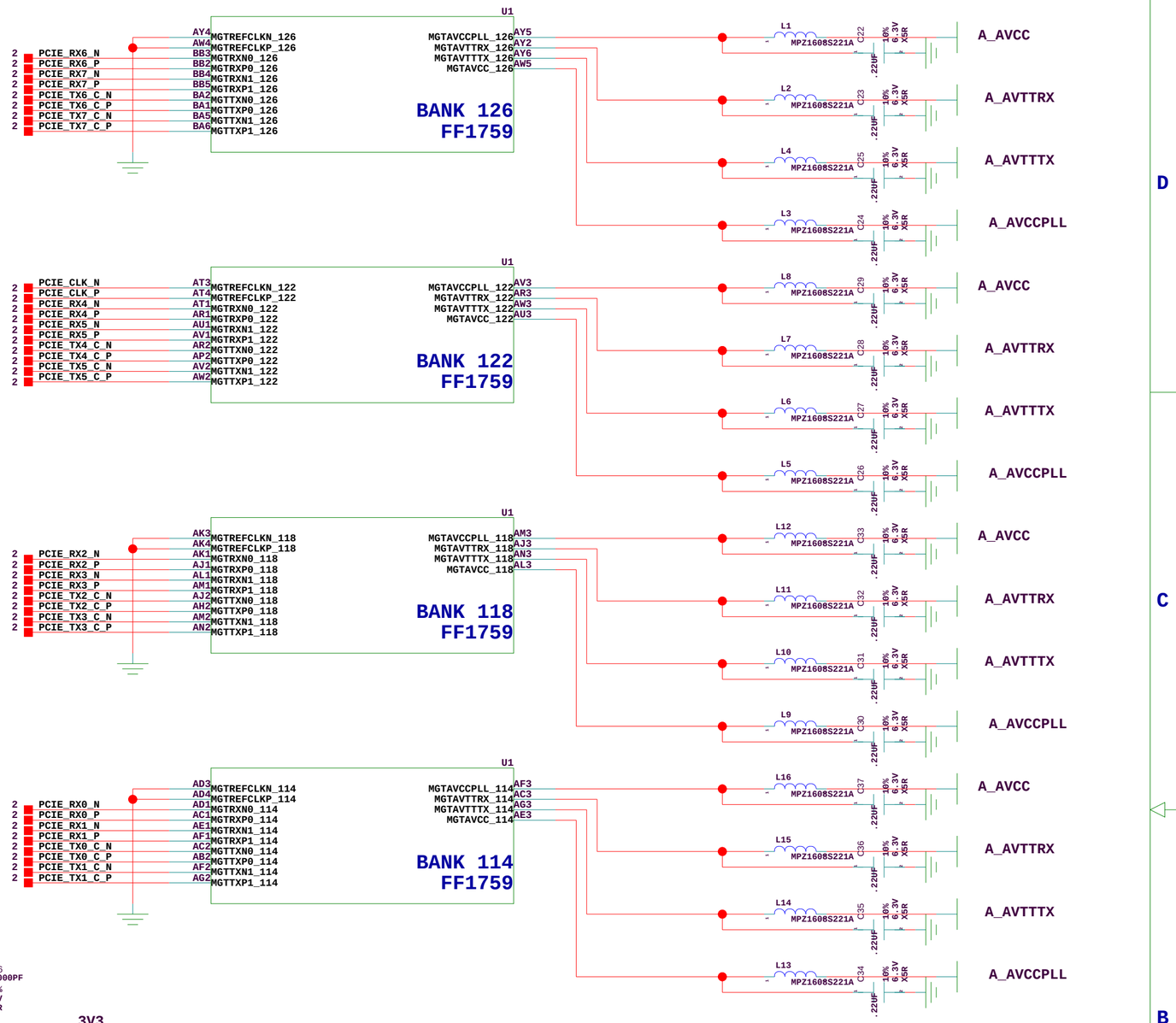
HITECH GLOBAL

TITLE: V5TXT-PCIE
BLOCK DIAGRAM

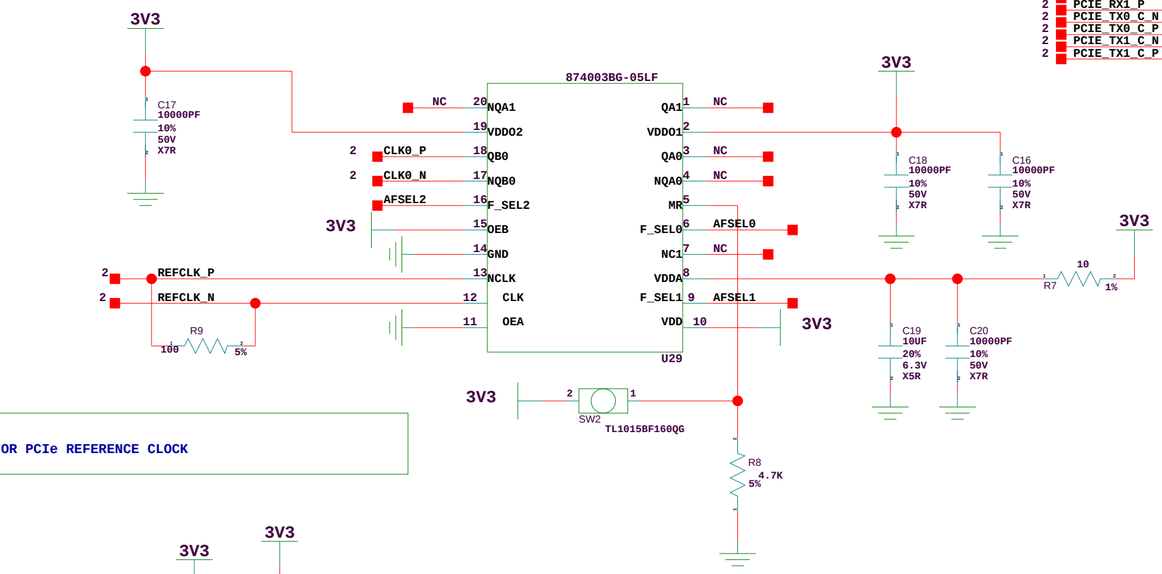
SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	of	
S.S		1	32	6-24-2010_20:53

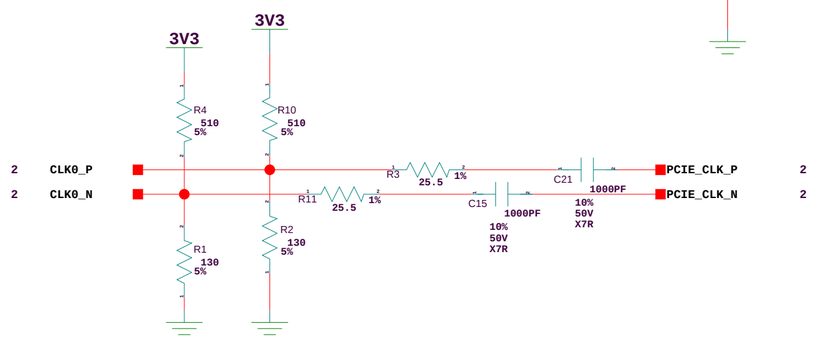


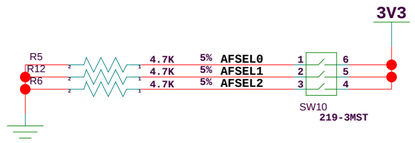


GTP JITTER ATTENUATOR



NOTE:
QA0 USED FOR PCIe REFERENCE CLOCK





INPUT			OUTPUT	
FSEL2	FSEL1	FSEL0	QA0/nQA0	QB0/nQB0
0	0	0	DIV2	DIV2
1	0	0	DIV5	DIV2
0	1	0	DIV4	DIV2
1	1	0	DIV2	DIV4
0	0	1	DIV2	DIV5
1	0	1	DIV5	DIV4
0	1	1	DIV4	DIV5
1	1	1	DIV4	DIV4

CONFIDENTIAL

HITECH GLOBAL

TITLE: V5TXT-PCIE
PCIE CONNECTOR AND TRANSCEIVERS

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		2 of 32	6-24-2010_20:53

TRANSCEIVERS SWAP FOR SMOOTH ROUTING

U17

AEL2005-1Q10C

ADDRESS: 0000

U1

BANK 128
FF1759

U1

BANK 132
FF1759

J7

1888247-2

J11

2007194-1

RESET CIRCUIT

CONFIDENTIAL

HITECH GLOBAL

TITLE

V5TXT-PCIE
10GBS PHY INTERFACE CHAIN A

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		3 of 32	6-24-2010_20:53

TRANSCEIVERS SWAP FOR SMOOTH ROUTING

U18

AEL2005-1Q10C

ADDRESS: 0001

J8 SFP_HOST_CONN 1888247-2

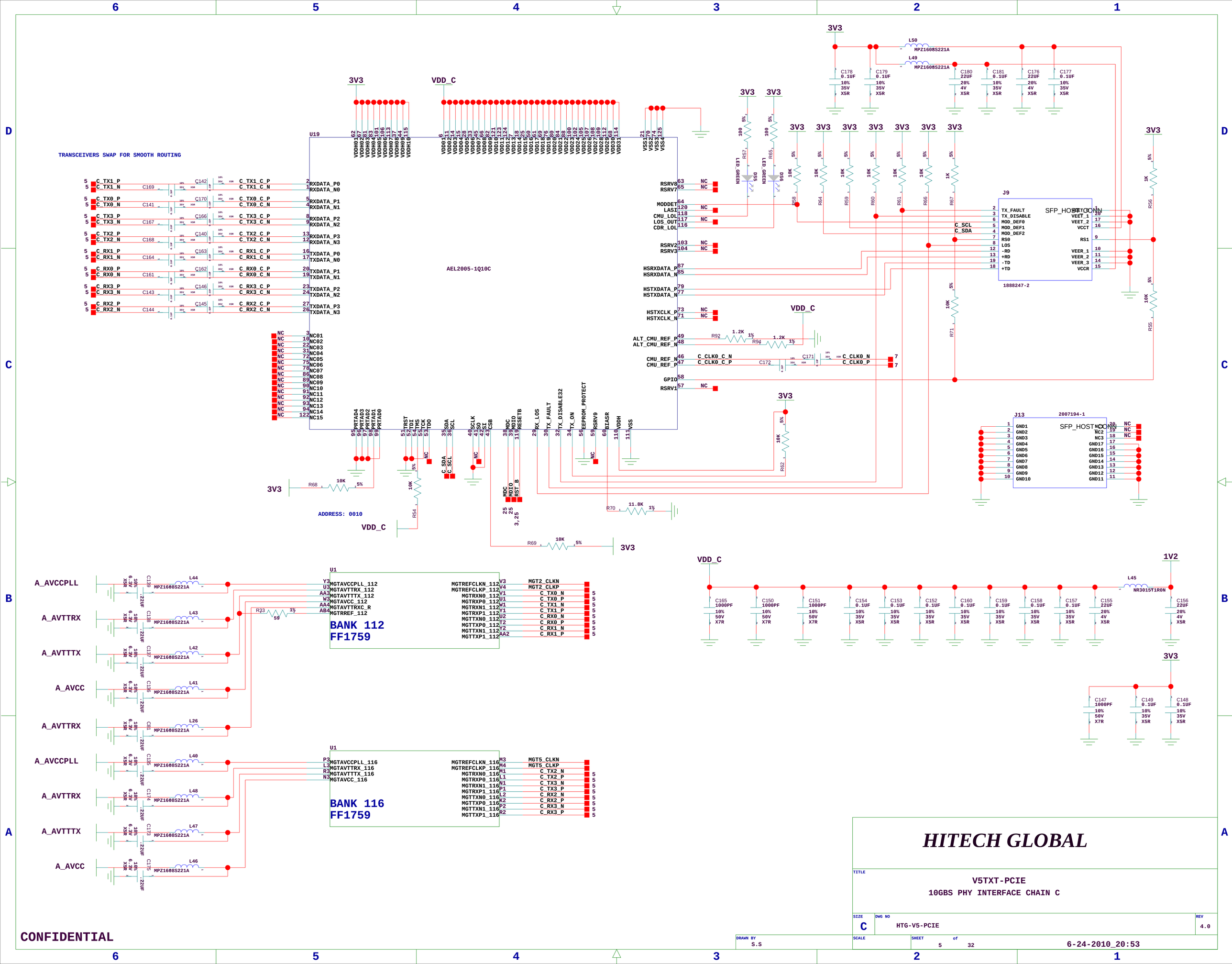
J12 2007194-1 SFP_HOST_CONN

U1 BANK 120 FF1759

U1 BANK 124 FF1759

CONFIDENTIAL

HITECH GLOBAL	
TITLE	V5TXT-PCIE 10GBS PHY INTERFACE CHAIN B
SIZE	C
DWG NO	HTG-V5-PCIE
REV	4.0
DRAWN BY	S.S
SCALE	
SHEET	4 of 32
	6-24-2010_20:53



HITECH GLOBAL

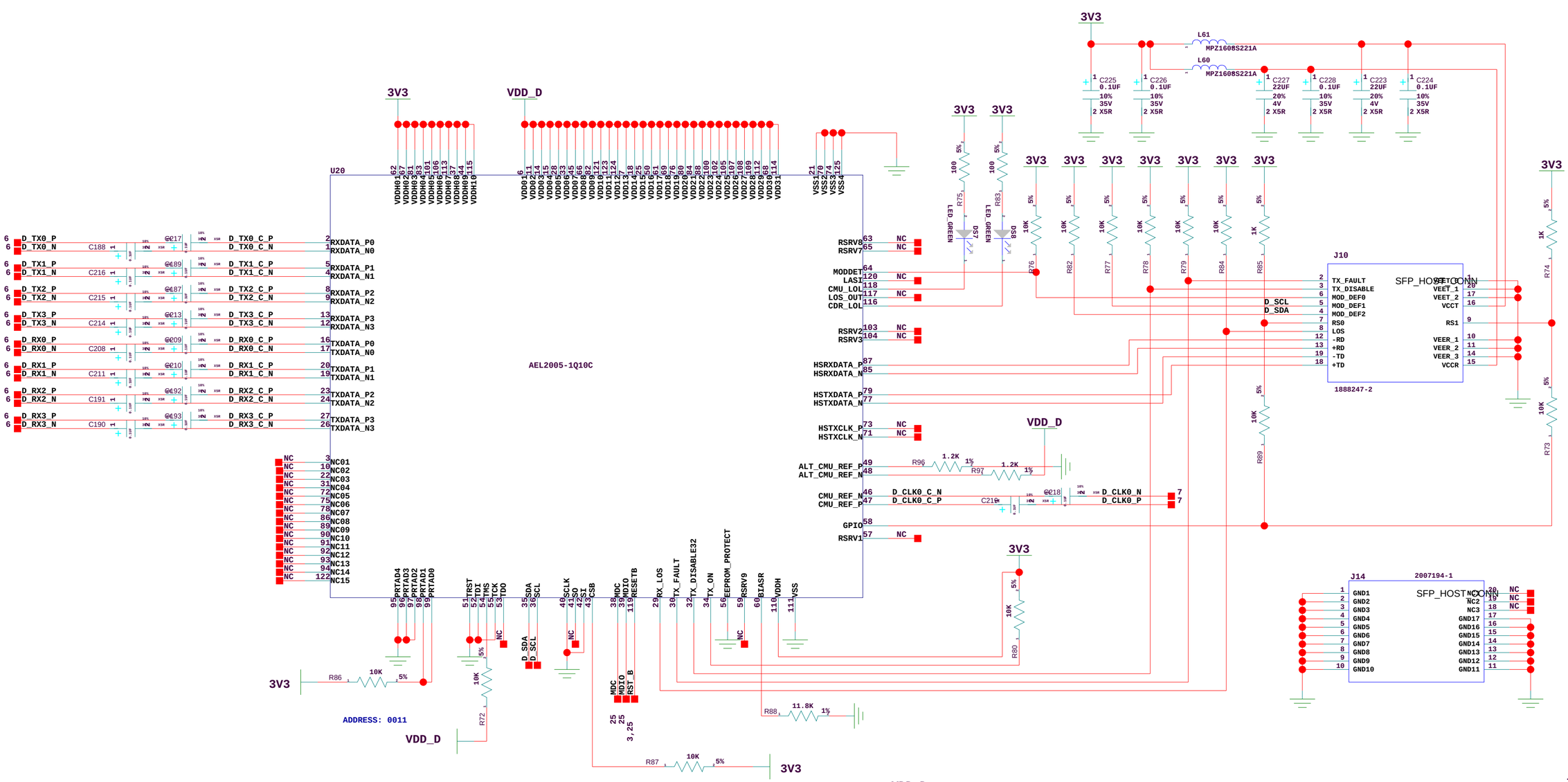
TITLE

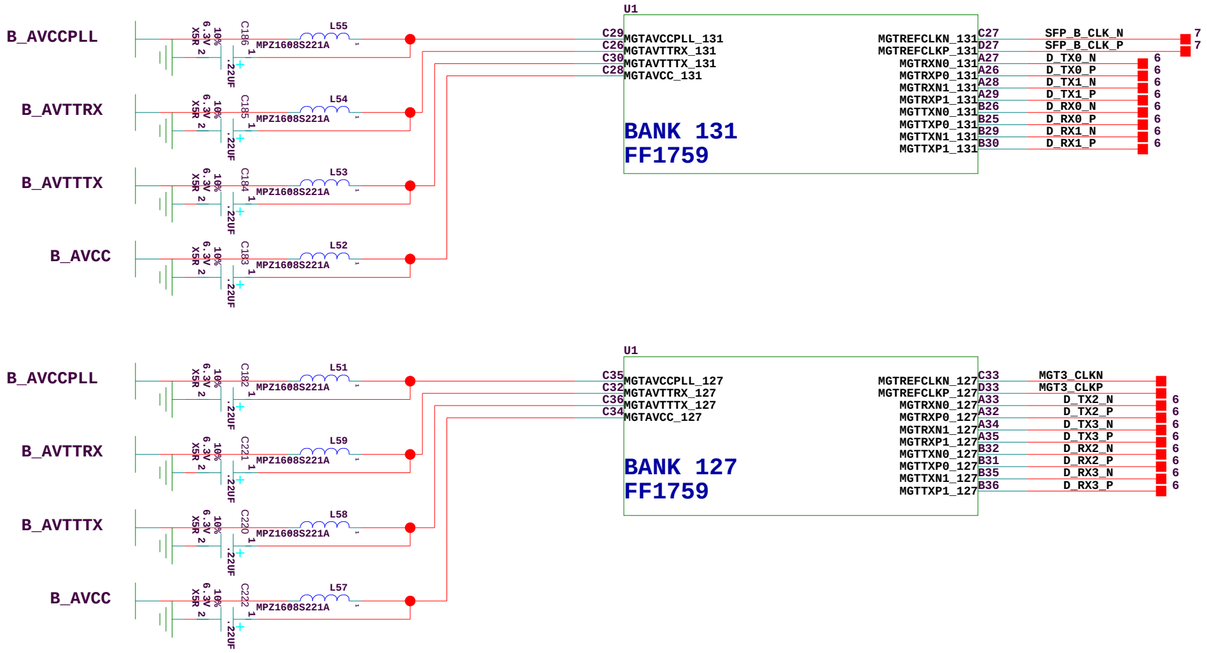
V5TXT-PCIE

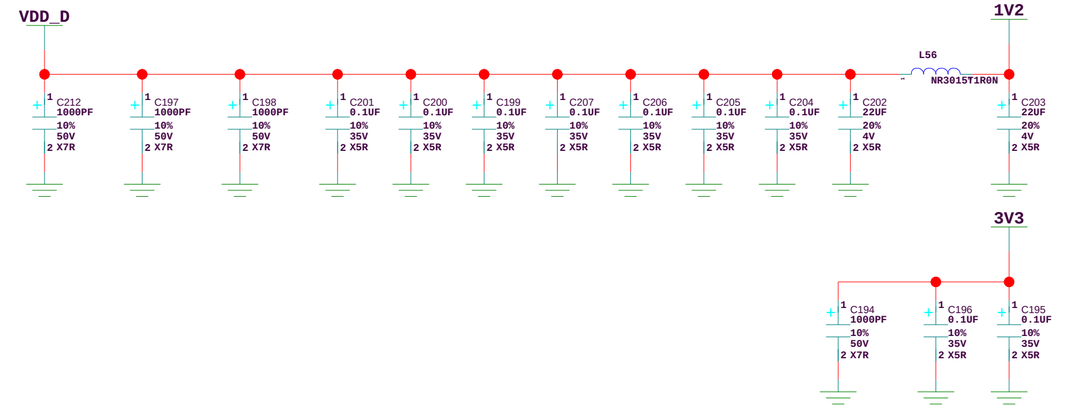
10GBS PHY INTERFACE CHAIN C

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	of	
S.S		5	32	6-24-2010_20:53







CONFIDENTIAL

HITECH GLOBAL

TITLE

V5TXT-PCIE

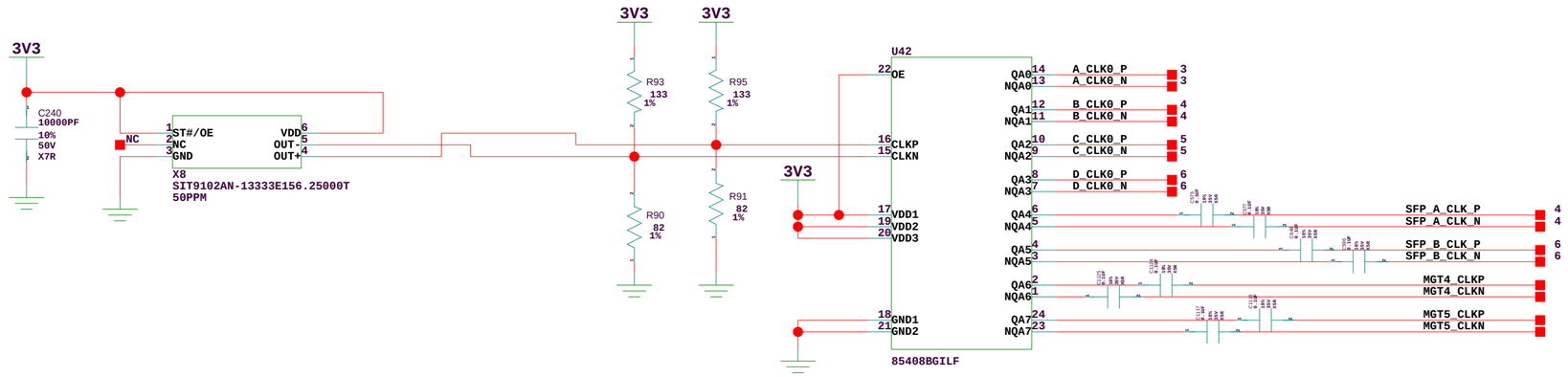
10GBS PHY INTERFACE CHAIN D

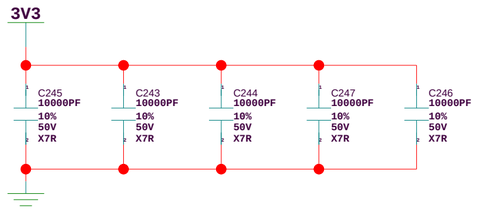
SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	of	
S.S		6	32	6-24-2010_20:53

156.25MHz LVPECL CLOCK OSCILLATOR

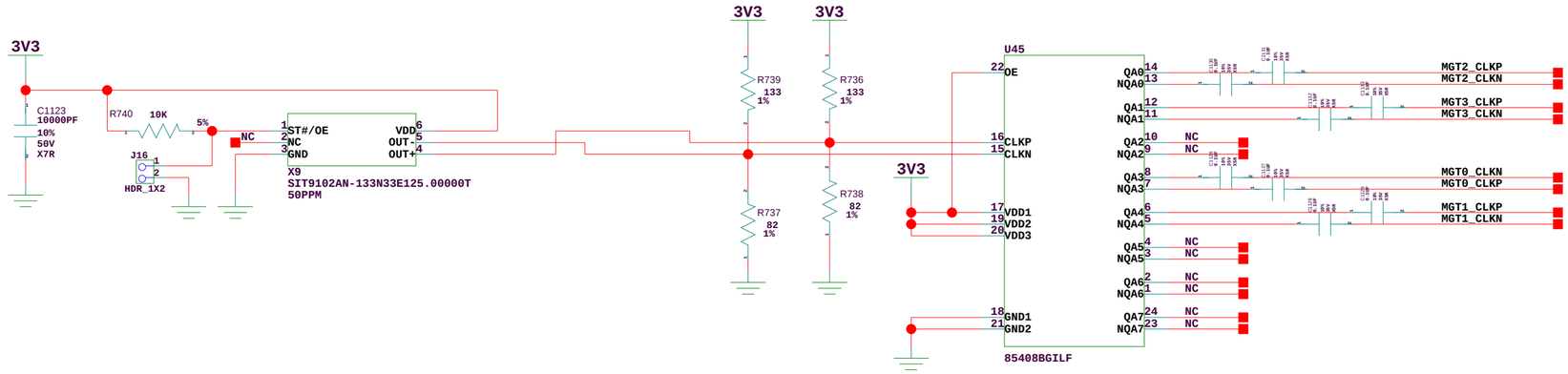
SFP CLOCK DISTRIBUTOR

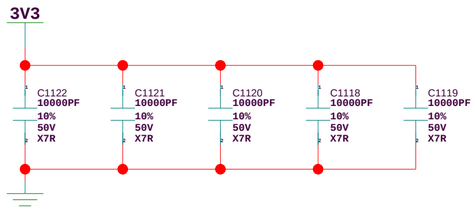




125MHz LVPECL CLOCK OSCILLATOR

SFP CLOCK DISTRIBUTOR





CONFIDENTIAL

HITECH GLOBAL

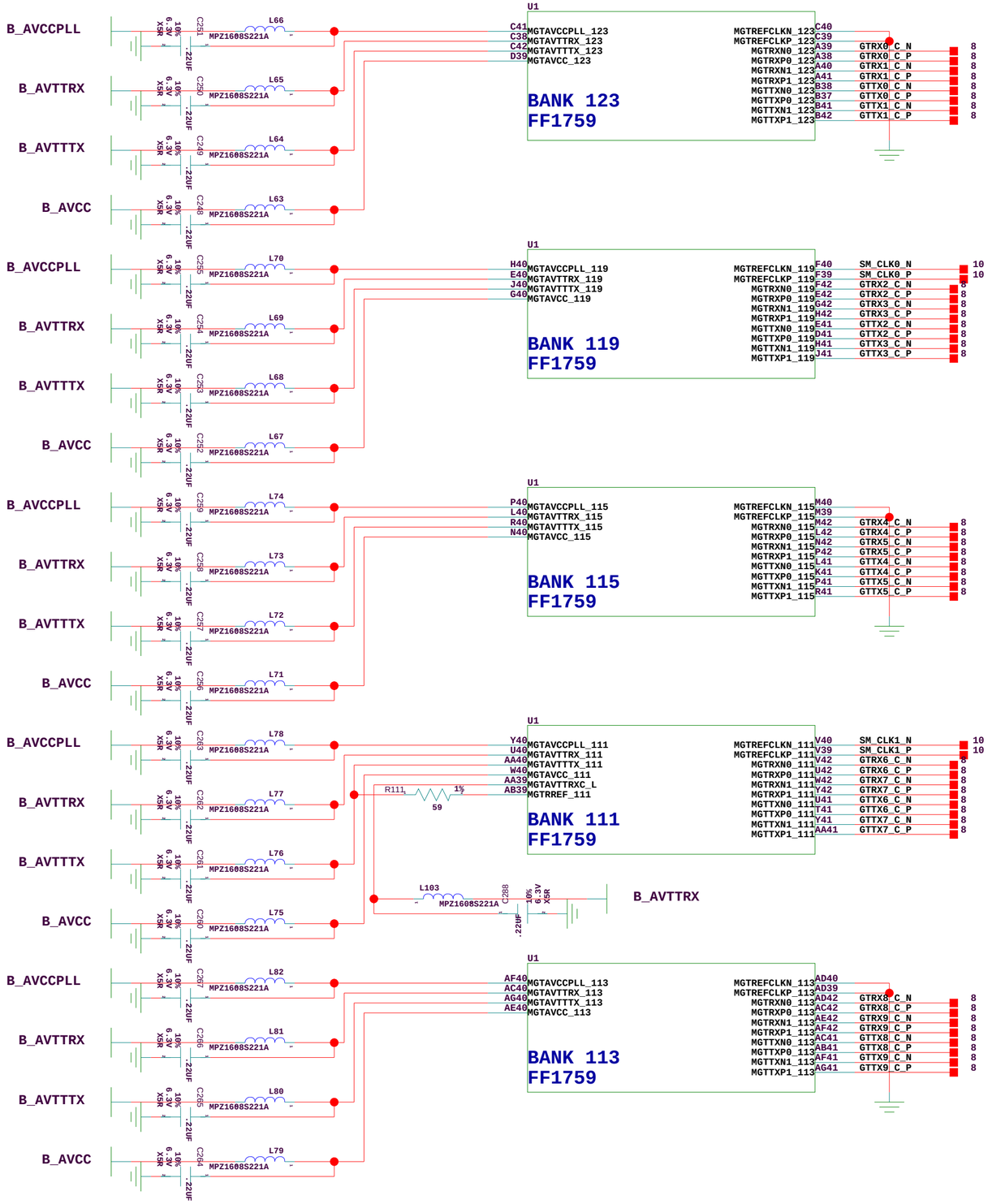
TITLE

V5TXT-PCIE

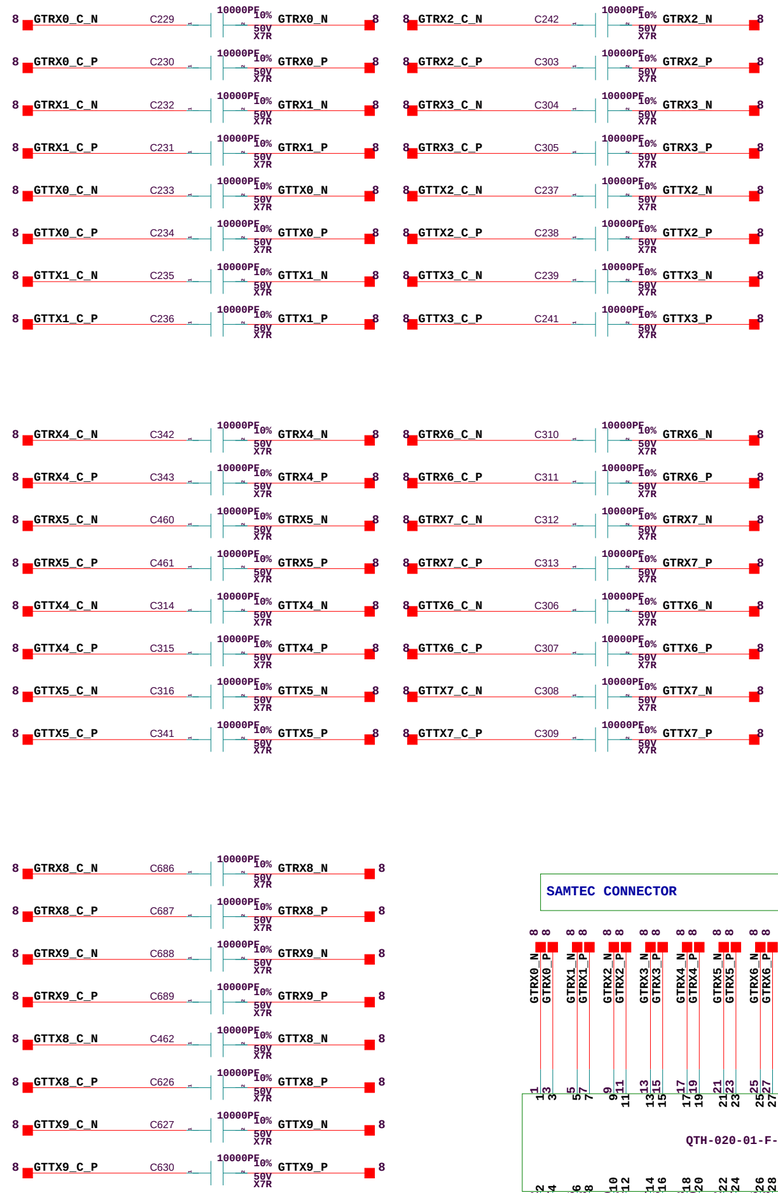
156.25MHZ&125MHZ CLOCK AND CLOCK DISTRIBUTOR

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

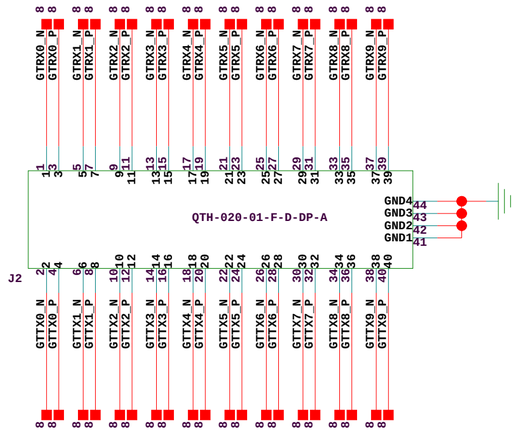
DRAWN BY	SCALE	SHEET	
S.S		7 of 32	6-24-2010_20:53



GTP's AC CAPS



SAMTEC CONNECTOR



HITECH GLOBAL

TITLE: V5TXT-PCIE
SAMTEC INTERFACE [0:9]

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		8 of 32	6-24-2010_20:53

CONFIDENTIAL

B_AVCCPLL
B_AVTTRX
B_AVTTTX
B_AVCC
B_AVCCPLL
B_AVTTRX
B_AVTTTX
B_AVCC
B_AVCCPLL
B_AVTTRX
B_AVTTTX
B_AVCC
B_AVCCPLL
B_AVTTRX
B_AVTTTX
B_AVCC

C271 C270 C269 C268 C275 C274 C273 C272 C279 C278 C277 C276 C283 C282 C281 C280 C287 C286 C285 C284
.22UF 10% 6.3V X5R
L86 L85 L84 L83 L90 L89 L88 L87 L94 L93 L92 L91 L98 L97 L96 L95 L102 L101 L100 L99
MPZ1608S221A

U1
BANK 117
FF1759
MGTAVCCPLL_117 AM40
MGTAVTTRX_117 AJ40
MGTAVTTTX_117 AN40
MGTAVCC_117 AL40
MGTREFCLKN_117 AK40
MGTREFCLKP_117 AK39
MGTRXN0_117 AK42 GTRX10_C_N 9
MGTRXP0_117 AJ42 GTRX10_C_P 9
MGTRXN1_117 AL42 GTRX11_C_N 9
MGTRXP1_117 AM42 GTRX11_C_P 9
MGTTXN0_117 AJ41 GTTX10_C_N 9
MGTTXP0_117 AH41 GTTX10_C_P 9
MGTTXN1_117 AM41 GTTX11_C_N 9
MGTTXP1_117 AN41 GTTX11_C_P 9

U1
BANK 121
FF1759
MGTAVCCPLL_121 AV40
MGTAVTTRX_121 AR40
MGTAVTTTX_121 AW40
MGTAVCC_121 AU40
MGTREFCLKN_121 AT40 SM_CLK2_N 10
MGTREFCLKP_121 AT39 SM_CLK2_P 10
MGTRXN0_121 AT42 GTRX12_C_N 9
MGTRXP0_121 AR42 GTRX12_C_P 9
MGTRXN1_121 AU42 GTRX13_C_N 9
MGTRXP1_121 AV42 GTRX13_C_P 9
MGTTXN0_121 AR41 GTTX12_C_N 9
MGTTXP0_121 AP41 GTTX12_C_P 9
MGTTXN1_121 AV41 GTTX13_C_N 9
MGTTXP1_121 AW41 GTTX13_C_P 9

U1
BANK 125
FF1759
MGTAVCCPLL_125 AY38
MGTAVTTRX_125 AY41
MGTAVTTTX_125 AY37
MGTAVCC_125 AW38
MGTREFCLKN_125 AY39
MGTREFCLKP_125 AW39
MGTRXN0_125 BB40 GTRX14_C_N 9
MGTRXP0_125 BB41 GTRX14_C_P 9
MGTRXN1_125 BB39 GTRX15_C_N 9
MGTRXP1_125 BB38 GTRX15_C_P 9
MGTTXN0_125 BA41 GTTX14_C_N 9
MGTTXP0_125 BA42 GTTX14_C_P 9
MGTTXN1_125 BA38 GTTX15_C_N 9
MGTTXP1_125 BA37 GTTX15_C_P 9

U1
BANK 129
FF1759
MGTAVCCPLL_129 AY32
MGTAVTTRX_129 AY35
MGTAVTTTX_129 AY31
MGTAVCC_129 AY33
MGTREFCLKN_129 AY34 SM_CLK3_N 10
MGTREFCLKP_129 AW34 SM_CLK3_P 10
MGTRXN0_129 BB34 GTRX16_C_N 9
MGTRXP0_129 BB35 GTRX16_C_P 9
MGTRXN1_129 BB33 GTRX17_C_N 9
MGTRXP1_129 BB32 GTRX17_C_P 9
MGTTXN0_129 BA35 GTTX16_C_N 9
MGTTXP0_129 BA36 GTTX16_C_P 9
MGTTXN1_129 BA32 GTTX17_C_N 9
MGTTXP1_129 BA31 GTTX17_C_P 9

U1
BANK 133
FF1759
MGTAVCCPLL_133 AY26
MGTAVTTRX_133 AY29
MGTAVTTTX_133 AY25
MGTAVCC_133 AY27
MGTREFCLKN_133 AY28
MGTREFCLKP_133 AW28
MGTRXN0_133 BB28 GTRX18_C_N 9
MGTRXP0_133 BB29 GTRX18_C_P 9
MGTRXN1_133 BB27 GTRX19_C_N 9
MGTRXP1_133 BB26 GTRX19_C_P 9
MGTTXN0_133 BA29 GTTX18_C_N 9
MGTTXP0_133 BA30 GTTX18_C_P 9
MGTTXN1_133 BA26 GTTX19_C_N 9
MGTTXP1_133 BA25 GTTX19_C_P 9

GTP's AC CAPS

9 GTRX10_C_N C777 10000PF 10% 50V X7R GTRX10_N 9
9 GTRX10_C_P C778 10000PF 10% 50V X7R GTRX10_P 9
9 GTRX11_C_N C779 10000PF 10% 50V X7R GTRX11_N 9
9 GTRX11_C_P C780 10000PF 10% 50V X7R GTRX11_P 9
9 GTTX10_C_N C773 10000PF 10% 50V X7R GTTX10_N 9
9 GTTX10_C_P C774 10000PF 10% 50V X7R GTTX10_P 9
9 GTTX11_C_N C775 10000PF 10% 50V X7R GTTX11_N 9
9 GTTX11_C_P C776 10000PF 10% 50V X7R GTTX11_P 9
9 GTRX14_C_N C793 10000PF 10% 50V X7R GTRX14_N 9
9 GTRX14_C_P C794 10000PF 10% 50V X7R GTRX14_P 9
9 GTRX15_C_N C795 10000PF 10% 50V X7R GTRX15_N 9
9 GTRX15_C_P C807 10000PF 10% 50V X7R GTRX15_P 9
9 GTTX14_C_N C789 10000PF 10% 50V X7R GTTX14_N 9
9 GTTX14_C_P C790 10000PF 10% 50V X7R GTTX14_P 9
9 GTTX15_C_N C791 10000PF 10% 50V X7R GTTX15_N 9
9 GTTX15_C_P C792 10000PF 10% 50V X7R GTTX15_P 9

9 GTRX12_C_N C769 10000PF 10% 50V X7R GTRX12_N 9
9 GTRX12_C_P C770 10000PF 10% 50V X7R GTRX12_P 9
9 GTRX13_C_N C771 10000PF 10% 50V X7R GTRX13_N 9
9 GTRX13_C_P C772 10000PF 10% 50V X7R GTRX13_P 9
9 GTTX12_C_N C765 10000PF 10% 50V X7R GTTX12_N 9
9 GTTX12_C_P C766 10000PF 10% 50V X7R GTTX12_P 9
9 GTTX13_C_N C767 10000PF 10% 50V X7R GTTX13_N 9
9 GTTX13_C_P C768 10000PF 10% 50V X7R GTTX13_P 9
9 GTRX16_C_N C785 10000PF 10% 50V X7R GTRX16_N 9
9 GTRX16_C_P C786 10000PF 10% 50V X7R GTRX16_P 9
9 GTRX17_C_N C787 10000PF 10% 50V X7R GTRX17_N 9
9 GTRX17_C_P C788 10000PF 10% 50V X7R GTRX17_P 9
9 GTTX16_C_N C781 10000PF 10% 50V X7R GTTX16_N 9
9 GTTX16_C_P C782 10000PF 10% 50V X7R GTTX16_P 9
9 GTTX17_C_N C783 10000PF 10% 50V X7R GTTX17_N 9
9 GTTX17_C_P C784 10000PF 10% 50V X7R GTTX17_P 9

9 GTRX18_C_N C761 10000PF 10% 50V X7R GTRX18_N 9
9 GTRX18_C_P C762 10000PF 10% 50V X7R GTRX18_P 9
9 GTRX19_C_N C763 10000PF 10% 50V X7R GTRX19_N 9
9 GTRX19_C_P C764 10000PF 10% 50V X7R GTRX19_P 9
9 GTTX18_C_N C690 10000PF 10% 50V X7R GTTX18_N 9
9 GTTX18_C_P C748 10000PF 10% 50V X7R GTTX18_P 9
9 GTTX19_C_N C749 10000PF 10% 50V X7R GTTX19_N 9
9 GTTX19_C_P C754 10000PF 10% 50V X7R GTTX19_P 9

SAMTEC CONNECTOR

J3 QTH-020-01-F-D-DP-A
GTRX10_N 1 GTRX10_P 3
GTRX11_N 5 GTRX11_P 7
GTRX12_N 9 GTRX12_P 11
GTRX13_N 13 GTRX13_P 15
GTRX14_N 17 GTRX14_P 19
GTRX15_N 21 GTRX15_P 23
GTRX16_N 25 GTRX16_P 27
GTRX17_N 29 GTRX17_P 31
GTRX18_N 33 GTRX18_P 35
GTRX19_N 37 GTRX19_P 39
GTTX10_N 2 GTTX10_P 4
GTTX11_N 6 GTTX11_P 8
GTTX12_N 10 GTTX12_P 12
GTTX13_N 14 GTTX13_P 16
GTTX14_N 18 GTTX14_P 20
GTTX15_N 22 GTTX15_P 24
GTTX16_N 26 GTTX16_P 28
GTTX17_N 30 GTTX17_P 32
GTTX18_N 34 GTTX18_P 36
GTTX19_N 38 GTTX19_P 40
GND4 44
GND3 43
GND2 42
GND1 41
9 on all pins

CONFIDENTIAL

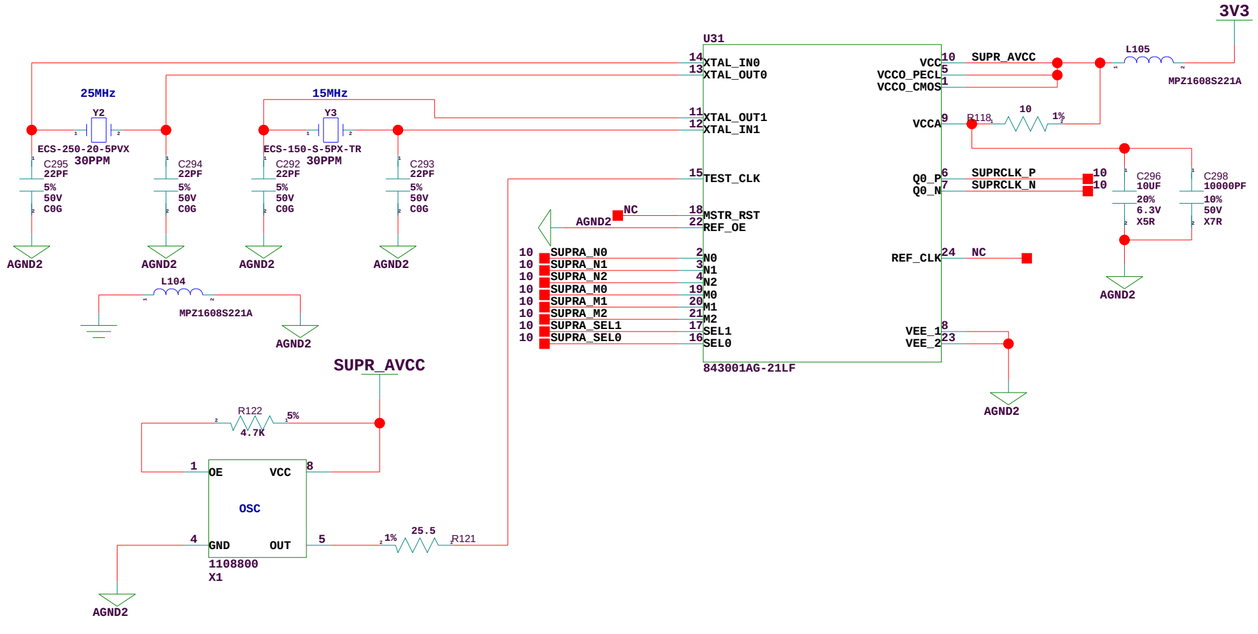
HITECH GLOBAL

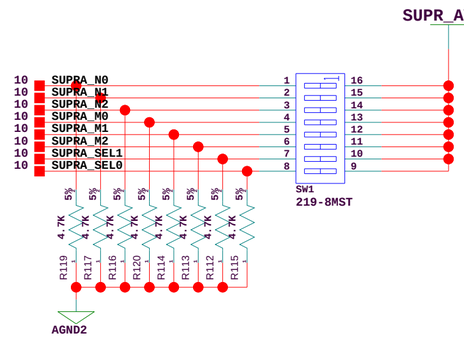
TITLE
V5TXT-PCIE
SAMTEC INTERFACE [10:19]

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		9 of 32	6-24-2010_20:53

SAMTEC GTP CLOCK GENERATOR





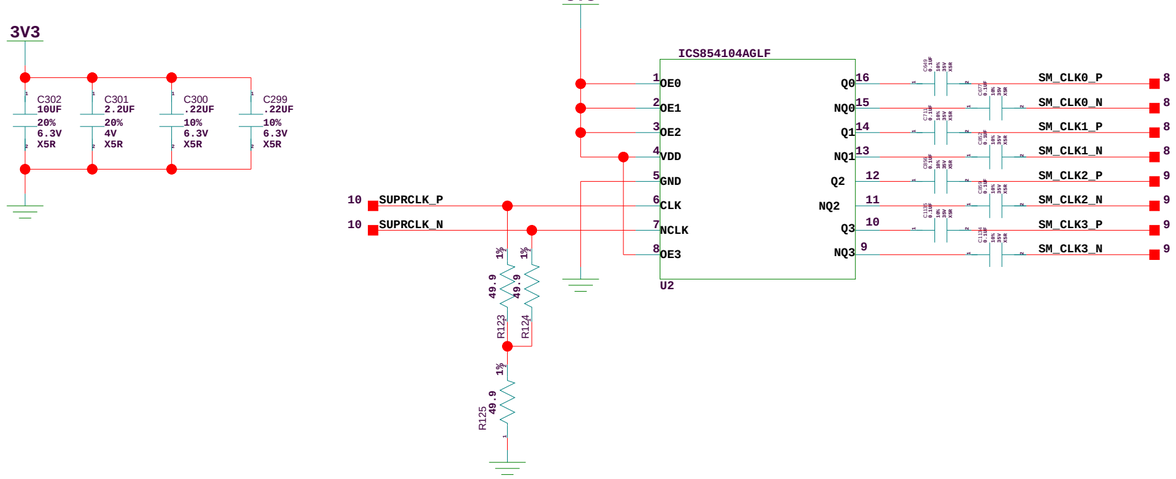
INPUTS			M-DIV	INPUTS FREQUENCY (MHz)	
M2	M1	M0		MIN FREQ	MAX FREQ
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

INPUTS			N-DIV
N2	N1	N0	
0	0	0	/1
0	0	1	/2
0	1	0	/3
0	1	1	/4
1	0	0	/5
1	0	1	/6
1	1	0	/8
1	1	1	/10

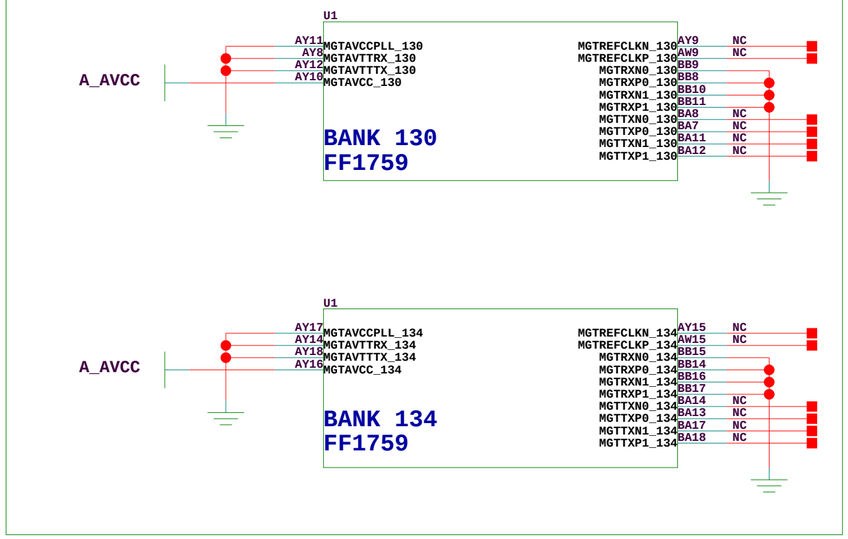
EXAMPLE:

IN [MHz]	M-DIV	N-DIV	OUT [MHz]
25	24	2	300

SAMTEC GTP CLOCK BUFFER



UNUSED GTP's

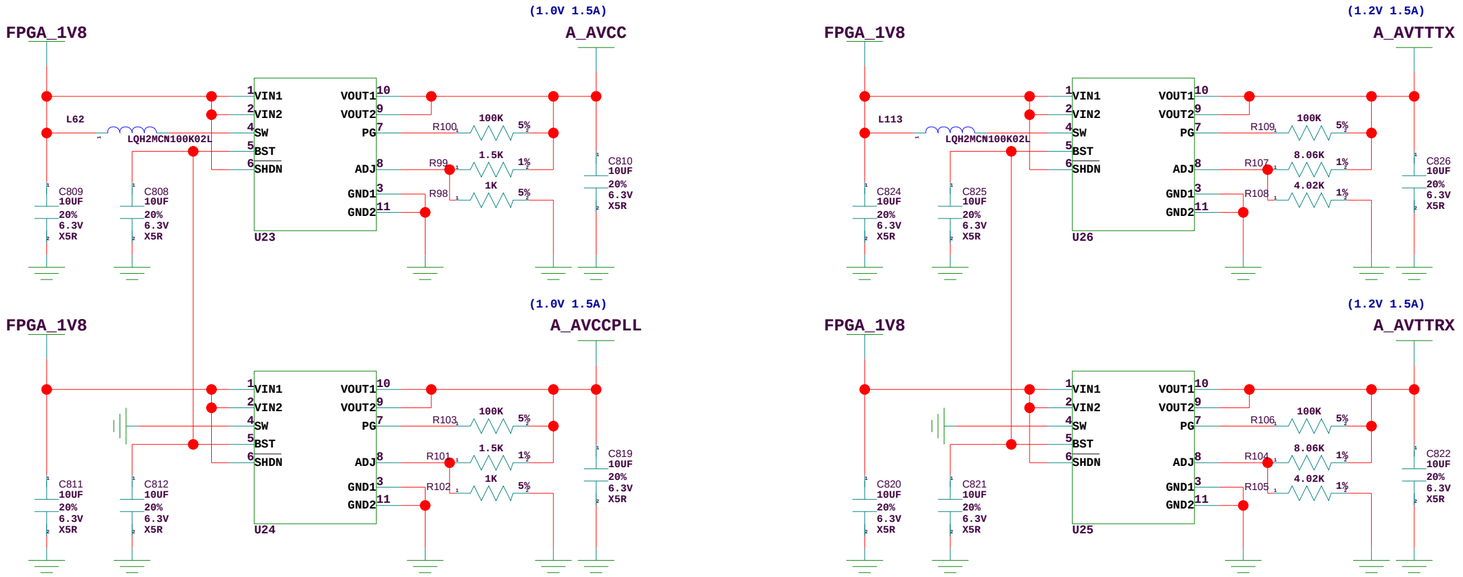


CONFIDENTIAL

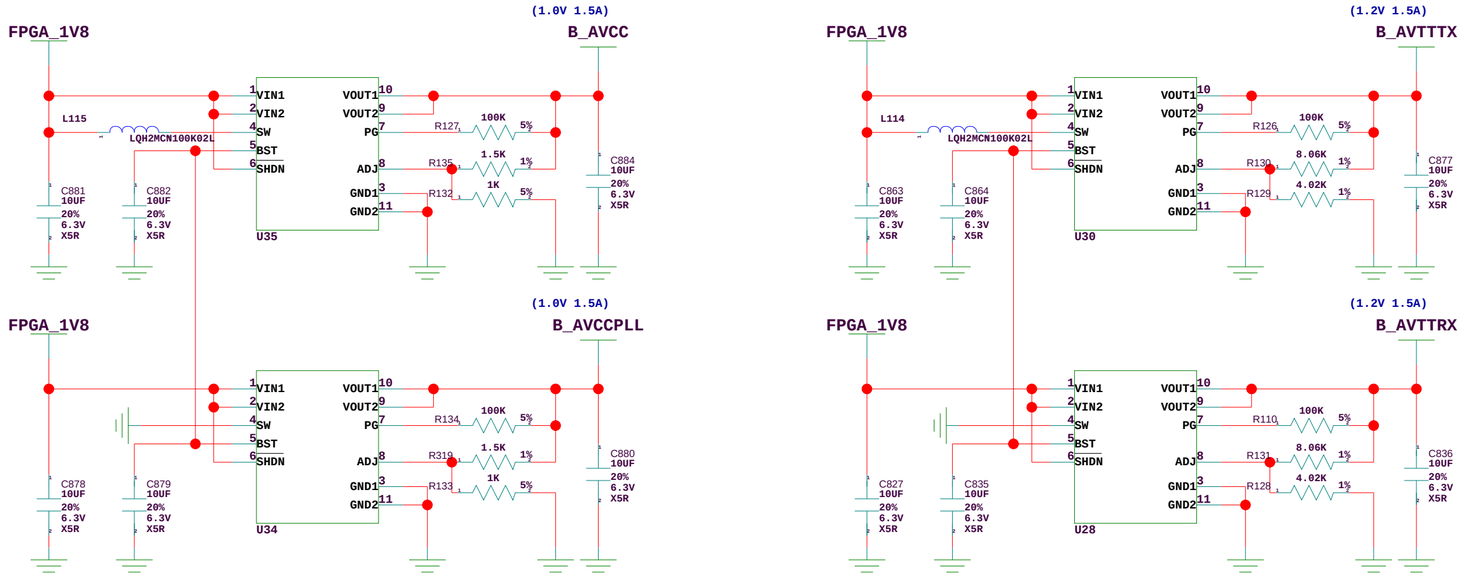
HITECH GLOBAL

TITLE	V5TXT-PCIE SAMTEC CLOCK INTERFACE		
SIZE	DWG NO		REV
C	HTG-V5-PCIE		4.0
DRAWN BY	SCALE	SHEET	
S.S		10 of 32	6-24-2010_20:53

MGT POWER SUPPLY ALL EVEN GTX BANKS



MGT POWER SUPPLY ALL ODD GTX BANKS



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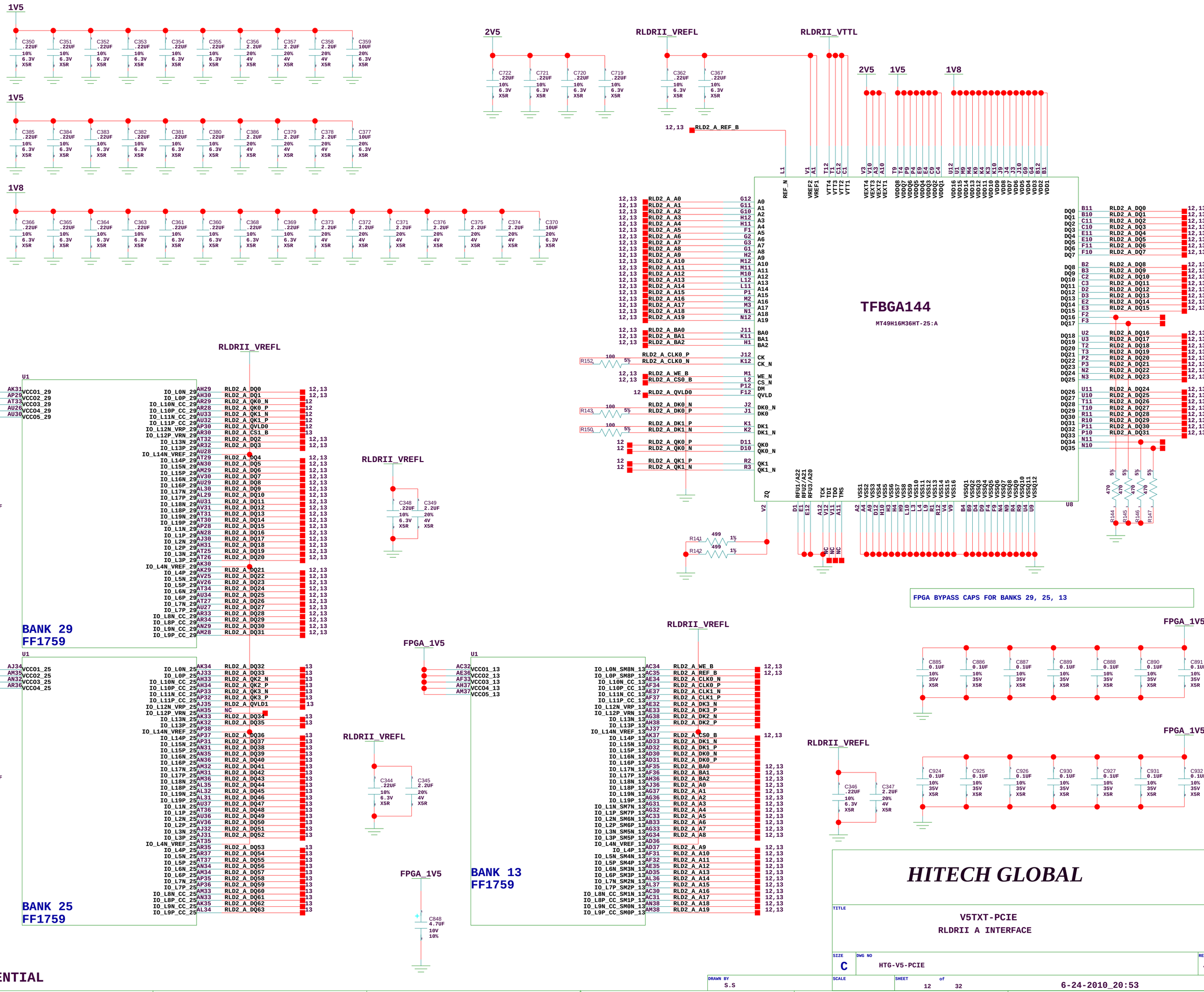
HITECH GLOBAL

TITLE: V5TXT-PCIE
MGT POWER, RLDRII AND QDRII TERM

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		11 of 32	6-24-2010_20:53


1V5
C350 .22UF 10% 6.3V X5R
C351 .22UF 10% 6.3V X5R
C352 .22UF 10% 6.3V X5R
C353 .22UF 10% 6.3V X5R
C354 .22UF 10% 6.3V X5R
C355 .22UF 10% 6.3V X5R
C356 2.2UF 20% 4V X5R
C357 2.2UF 20% 4V X5R
C358 2.2UF 20% 4V X5R
C359 10UF 20% 6.3V X5R
1V5
C385 .22UF 10% 6.3V X5R
C384 .22UF 10% 6.3V X5R
C383 .22UF 10% 6.3V X5R
C382 .22UF 10% 6.3V X5R
C381 .22UF 10% 6.3V X5R
C380 .22UF 10% 6.3V X5R
C386 2.2UF 20% 4V X5R
C379 2.2UF 20% 4V X5R
C378 2.2UF 20% 4V X5R
C377 10UF 20% 6.3V X5R
1V8
C366 .22UF 10% 6.3V X5R
C365 .22UF 10% 6.3V X5R
C364 .22UF 10% 6.3V X5R
C363 .22UF 10% 6.3V X5R
C361 .22UF 10% 6.3V X5R
C360 .22UF 10% 6.3V X5R
C368 .22UF 10% 6.3V X5R
C369 .22UF 10% 6.3V X5R
C373 2.2UF 20% 4V X5R
C372 2.2UF 20% 4V X5R
C371 2.2UF 20% 4V X5R
C376 2.2UF 20% 4V X5R
C375 2.2UF 20% 4V X5R
C374 2.2UF 20% 4V X5R
C370 10UF 20% 6.3V X5R
2V5
C722 .22UF 10% 6.3V X5R
C721 .22UF 10% 6.3V X5R
C720 .22UF 10% 6.3V X5R
C719 .22UF 10% 6.3V X5R
RLDRII_VREFL
C362 .22UF 10% 6.3V X5R
C367 .22UF 10% 6.3V X5R
RLDRII_VTTL
2V5
1V5
1V8
12,13 RLD2_A_REF_B
TFBGA144
MT49H16M36HT-25:A
U8
REF_N
VREF2
VREF1
VTT4
VTT3
VTT2
VTT1
VEXT4
VEXT3
VEXT2
VEXT1
VDD8
VDD7
VDD6
VDD5
VDD4
VDD3
VDD2
VDD1
VDD16
VDD15
VDD14
VDD13
VDD12
VDD11
VDD10
VDD9
VDD8
VDD7
VDD6
VDD5
VDD4
VDD3
VDD2
VDD1
ZQ
RFU1/A22
RFU2/A21
RFU3/A20
TCK
TDI
TDO
TMS
R141 499 1%
R142 499 1%
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19
BA0 BA1 BA2
CK CK_N
WE_N CS_N DM QVLD
DK0_N DK0
DK1 DK1_N
QK0 QK0_N
QK1 QK1_N
R152 100 5%
R143 100 5%
R150 100 5%
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35
R144 470 5%
R145 470 5%
R146 470 5%
R147 470 5%
FPGA_1V5
U1
BANK 29
FF1759
BANK 25
FF1759
BANK 13
FF1759
RLDRII_VREFL
C846 4.7UF 10V 10%
C847 4.7UF 10V 10%
C848 4.7UF 10V 10%
C348 .22UF 10% 6.3V X5R
C349 2.2UF 20% 4V X5R
C344 .22UF 10% 6.3V X5R
C345 2.2UF 20% 4V X5R
C346 .22UF 10% 6.3V X5R
C347 2.2UF 20% 4V X5R
FPGA BYPASS CAPS FOR BANKS 29, 25, 13
C885 0.1UF 10% 35V X5R
C886 0.1UF 10% 35V X5R
C887 0.1UF 10% 35V X5R
C889 0.1UF 10% 35V X5R
C888 0.1UF 10% 35V X5R
C890 0.1UF 10% 35V X5R
C891 0.1UF 10% 35V X5R
C924 0.1UF 10% 35V X5R
C925 0.1UF 10% 35V X5R
C926 0.1UF 10% 35V X5R
C930 0.1UF 10% 35V X5R
C927 0.1UF 10% 35V X5R
C931 0.1UF 10% 35V X5R
C932 0.1UF 10% 35V X5R
CONFIDENTIAL
HITECH GLOBAL
TITLE
V5TXT-PCIE
RLDRII A INTERFACE
SIZE C
DWG NO HTG-V5-PCIE
REV 4.0
DRAWN BY S.S
SCALE
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TERMINATION RESISTORS

RLDRII_VTTL

RLDRII_VTTL

RLDRII_VTTL

1V8

1V5

RLDRII_VTTL

RLDRII_VTTL

2V5

RLDRII_VREFL

RLDRII_VTTL

2V5 1V5 1V8

TFBGA144

MT49H16M36HT-25:A

NOTE:
CLK0_P AND CLK0_N MASTER CLK U10
CLK1_P AND CLK1_N MASTER CLK U11
DQ0-DQ17 INPUT ARE REFERENCED TO DK0_P AND DK0_N
DQ18-DQ35 INPUT ARE REFERENCED TO DK1_P AND DK1_N
DQ0-DQ8 OUTPUT ARE REFERENCED TO QK0_P AND QK0_N
DQ9-DQ17 OUTPUT ARE REFERENCED TO QK1_P AND QK1_N
DQ18-DQ26 OUTPUT ARE REFERENCED TO QK2_P AND QK2_N
DQ27-DQ35 OUTPUT ARE REFERENCED TO QK3_P AND QK3_N

HITECH GLOBAL

TITLE
V5TXT-PCIE
RLDRII B INTERFACE

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
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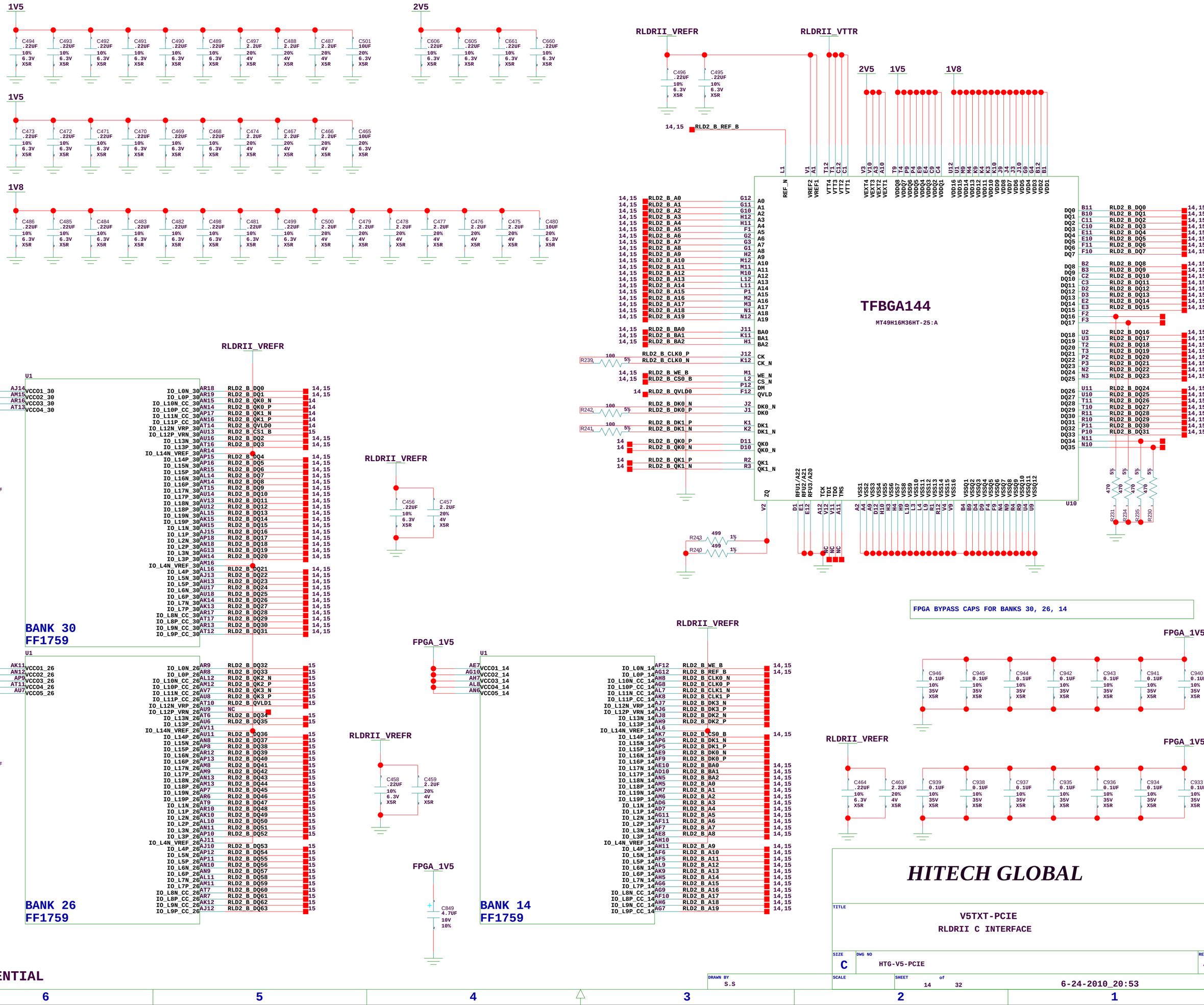
CONFIDENTIAL


1V5
C494 .22UF 10% 6.3V X5R
C493 .22UF 10% 6.3V X5R
C492 .22UF 10% 6.3V X5R
C491 .22UF 10% 6.3V X5R
C490 .22UF 10% 6.3V X5R
C489 .22UF 10% 6.3V X5R
C497 2.2UF 20% 4V X5R
C488 2.2UF 20% 4V X5R
C487 2.2UF 20% 4V X5R
C501 10UF 20% 6.3V X5R
2V5
C606 .22UF 10% 6.3V X5R
C605 .22UF 10% 6.3V X5R
C661 .22UF 10% 6.3V X5R
C660 .22UF 10% 6.3V X5R
1V5
C473 .22UF 10% 6.3V X5R
C472 .22UF 10% 6.3V X5R
C471 .22UF 10% 6.3V X5R
C470 .22UF 10% 6.3V X5R
C469 .22UF 10% 6.3V X5R
C468 .22UF 10% 6.3V X5R
C474 2.2UF 20% 4V X5R
C467 2.2UF 20% 4V X5R
C466 2.2UF 20% 4V X5R
C465 10UF 20% 6.3V X5R
1V8
C486 .22UF 10% 6.3V X5R
C485 .22UF 10% 6.3V X5R
C484 .22UF 10% 6.3V X5R
C483 .22UF 10% 6.3V X5R
C482 .22UF 10% 6.3V X5R
C498 .22UF 10% 6.3V X5R
C481 .22UF 10% 6.3V X5R
C499 .22UF 10% 6.3V X5R
C500 2.2UF 20% 4V X5R
C479 2.2UF 20% 4V X5R
C478 2.2UF 20% 4V X5R
C477 2.2UF 20% 4V X5R
C476 2.2UF 20% 4V X5R
C475 2.2UF 20% 4V X5R
C480 10UF 20% 6.3V X5R
RLDRII_VREFR
C496 .22UF 10% 6.3V X5R
C495 .22UF 10% 6.3V X5R
14,15 RLD2_B_REF_B
RLDRII_VTTR
2V5
1V5
1V8
L1 REF_N
V1 A1 VREF2 VREF1
T12 T1 C12 C1 VTT4 VTT3 VTT2 VTT1
V3 V10 A3 A10 VEXT4 VEXT3 VEXT2 VEXT1
T9 T4 P9 P4 E9 E4 C9 C4 VDDQ8 VDDQ7 VDDQ6 VDDQ5 VDDQ4 VDDQ3 VDDQ2 VDDQ1
U12 U1 M9 M4 K9 K4 K3 K10 J9 J4 J3 J10 G9 G4 B12 B1 VDD16 VDD15 VDD14 VDD13 VDD12 VDD11 VDD10 VDD9 VDD8 VDD7 VDD6 VDD5 VDD4 VDD3 VDD2 VDD1
14,15 RLD2_B_A0 G12 A0
14,15 RLD2_B_A1 G11 A1
14,15 RLD2_B_A2 G10 A2
14,15 RLD2_B_A3 H12 A3
14,15 RLD2_B_A4 H11 A4
14,15 RLD2_B_A5 F1 A5
14,15 RLD2_B_A6 G2 A6
14,15 RLD2_B_A7 G3 A7
14,15 RLD2_B_A8 G1 A8
14,15 RLD2_B_A9 H2 A9
14,15 RLD2_B_A10 M12 A10
14,15 RLD2_B_A11 M11 A11
14,15 RLD2_B_A12 M10 A12
14,15 RLD2_B_A13 L12 A13
14,15 RLD2_B_A14 L11 A14
14,15 RLD2_B_A15 P1 A15
14,15 RLD2_B_A16 M2 A16
14,15 RLD2_B_A17 M3 A17
14,15 RLD2_B_A18 N1 A18
14,15 RLD2_B_A19 N12 A19
14,15 RLD2_B_BA0 J11 BA0
14,15 RLD2_B_BA1 K11 BA1
14,15 RLD2_B_BA2 H1 BA2
RLD2_B_CLK0_P J12 CK
R239 100 5% RLD2_B_CLK0_N K12 CK_N
14,15 RLD2_B_WE_B M1 WE_N
14,15 RLD2_B_CS0_B L2 CS_N
P12 DM
14 RLD2_B_QVLD0 F12 QVLD
RLD2_B_DK0_N J2 DK0_N
R242 100 5% RLD2_B_DK0_P J1 DK0
RLD2_B_DK1_P K1 DK1
R241 100 5% RLD2_B_DK1_N K2 DK1_N
14 RLD2_B_QK0_P D11 QK0
14 RLD2_B_QK0_N D10 QK0_N
14 RLD2_B_QK1_P R2 QK1
14 RLD2_B_QK1_N R3 QK1_N
ZQ V2
R243 499 1%
R240 499 1%
RFU1/A22 RFU2/A21 RFU3/A20 TCK TDI TDO TMS
D1 E1 E12 A12 V12 V11 A11 NC NC NC
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16
A2 A4 A9 D12 H10 H3 H4 H9 L10 L3 L4 L9 R1 R12 V4 V9
VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 VSSQ10 VSSQ11 VSSQ12
B4 B9 D4 D9 F4 F9 N4 N9 R4 R9 U4 U9
U10
TFBGA144
MT49H16M36HT-25:A
DQ0 B11 RLD2_B_DQ0 14,15
DQ1 B10 RLD2_B_DQ1 14,15
DQ2 C11 RLD2_B_DQ2 14,15
DQ3 C10 RLD2_B_DQ3 14,15
DQ4 E11 RLD2_B_DQ4 14,15
DQ5 E10 RLD2_B_DQ5 14,15
DQ6 F11 RLD2_B_DQ6 14,15
DQ7 F10 RLD2_B_DQ7 14,15
DQ8 B2 RLD2_B_DQ8 14,15
DQ9 B3 RLD2_B_DQ9 14,15
DQ10 C2 RLD2_B_DQ10 14,15
DQ11 C3 RLD2_B_DQ11 14,15
DQ12 D2 RLD2_B_DQ12 14,15
DQ13 D3 RLD2_B_DQ13 14,15
DQ14 E2 RLD2_B_DQ14 14,15
DQ15 E3 RLD2_B_DQ15 14,15
DQ16 F2
DQ17 F3
DQ18 U2 RLD2_B_DQ16 14,15
DQ19 U3 RLD2_B_DQ17 14,15
DQ20 T2 RLD2_B_DQ18 14,15
DQ21 T3 RLD2_B_DQ19 14,15
DQ22 P2 RLD2_B_DQ20 14,15
DQ23 P3 RLD2_B_DQ21 14,15
DQ24 N2 RLD2_B_DQ22 14,15
DQ25 N3 RLD2_B_DQ23 14,15
DQ26 U11 RLD2_B_DQ24 14,15
DQ27 U10 RLD2_B_DQ25 14,15
DQ28 T11 RLD2_B_DQ26 14,15
DQ29 T10 RLD2_B_DQ27 14,15
DQ30 R11 RLD2_B_DQ28 14,15
DQ31 R10 RLD2_B_DQ29 14,15
DQ32 P11 RLD2_B_DQ30 14,15
DQ33 P10 RLD2_B_DQ31 14,15
DQ34 N11
DQ35 N10
5% 470 R231
5% 470 R234
5% 470 R235
5% 470 R230
FPGA_1V5
C851 4.7UF 10V 10%
RLDRII_VREFR
C456 .22UF 10% 6.3V X5R
C457 2.2UF 20% 4V X5R
U1
AJ14 VCCO1_30
AM15 VCCO2_30
AR16 VCCO3_30
AT13 VCCO4_30
IO_L0N_30 AR18 RLD2_B_DQ0 14,15
IO_L0P_30 AR19 RLD2_B_DQ1 14,15
IO_L10N_CC_30 AN15 RLD2_B_QK0_N 14
IO_L10P_CC_30 AN14 RLD2_B_QK0_P 14
IO_L11N_CC_30 AP17 RLD2_B_QK1_N 14
IO_L11P_CC_30 AN16 RLD2_B_QK1_P 14
IO_L12N_VRP_30 AT14 RLD2_B_QVLD0 14
IO_L12P_VRN_30 AU13 RLD2_B_CS1_B 15
IO_L13N_30 AU16 RLD2_B_DQ2 14,15
IO_L13P_30 AT16 RLD2_B_DQ3 14,15
IO_L14N_VREF_30 AR14
IO_L14P_30 AP15 RLD2_B_DQ4 14,15
IO_L15N_30 AP16 RLD2_B_DQ5 14,15
IO_L15P_30 AR15 RLD2_B_DQ6 14,15
IO_L16N_30 AL14 RLD2_B_DQ7 14,15
IO_L16P_30 AM14 RLD2_B_DQ8 14,15
IO_L17N_30 AT15 RLD2_B_DQ9 14,15
IO_L17P_30 AU14 RLD2_B_DQ10 14,15
IO_L18N_30 AV13 RLD2_B_DQ11 14,15
IO_L18P_30 AU12 RLD2_B_DQ12 14,15
IO_L19N_30 AL15 RLD2_B_DQ13 14,15
IO_L19P_30 AK15 RLD2_B_DQ14 14,15
IO_L1N_30 AH15 RLD2_B_DQ15 14,15
IO_L1P_30 AJ15 RLD2_B_DQ16 14,15
IO_L2N_30 AP18 RLD2_B_DQ17 14,15
IO_L2P_30 AN18 RLD2_B_DQ18 14,15
IO_L3N_30 AG13 RLD2_B_DQ19 14,15
IO_L3P_30 AH14 RLD2_B_DQ20 14,15
IO_L4N_VREF_30 AM16
IO_L4P_30 AL16 RLD2_B_DQ21 14,15
IO_L5N_30 AJ13 RLD2_B_DQ22 14,15
IO_L5P_30 AH13 RLD2_B_DQ23 14,15
IO_L6N_30 AU17 RLD2_B_DQ24 14,15
IO_L6P_30 AU18 RLD2_B_DQ25 14,15
IO_L7N_30 AK14 RLD2_B_DQ26 14,15
IO_L7P_30 AK13 RLD2_B_DQ27 14,15
IO_L8N_CC_30 AR17 RLD2_B_DQ28 14,15
IO_L8P_CC_30 AT17 RLD2_B_DQ29 14,15
IO_L9N_CC_30 AR13 RLD2_B_DQ30 14,15
IO_L9P_CC_30 AT12 RLD2_B_DQ31 14,15
BANK 30
FF1759
FPGA_1V5
C850 4.7UF 10V 10%
RLDRII_VREFR
C458 .22UF 10% 6.3V X5R
C459 2.2UF 20% 4V X5R
U1
AK11 VCCO1_26
AN12 VCCO2_26
AP9 VCCO3_26
AT11 VCCO4_26
AU7 VCCO5_26
IO_L0N_26 AR9 RLD2_B_DQ32 15
IO_L0P_26 AR8 RLD2_B_DQ33 15
IO_L10N_CC_26 AL12 RLD2_B_QK2_N 15
IO_L10P_CC_26 AM12 RLD2_B_QK2_P 15
IO_L11N_CC_26 AV7 RLD2_B_QK3_N 15
IO_L11P_CC_26 AU8 RLD2_B_QK3_P 15
IO_L12N_VRP_26 AT10 RLD2_B_QVLD1 15
IO_L12P_VRN_26 AU9 NC
IO_L13N_26 AT6 RLD2_B_DQ34 15
IO_L13P_26 AU6 RLD2_B_DQ35 15
IO_L14N_VREF_26 AV11
IO_L14P_26 AU11 RLD2_B_DQ36 15
IO_L15N_26 AN8 RLD2_B_DQ37 15
IO_L15P_26 AP8 RLD2_B_DQ38 15
IO_L16N_26 AR12 RLD2_B_DQ39 15
IO_L16P_26 AP13 RLD2_B_DQ40 15
IO_L17N_26 AM8 RLD2_B_DQ41 15
IO_L17P_26 AM9 RLD2_B_DQ42 15
IO_L18N_26 AN13 RLD2_B_DQ43 15
IO_L18P_26 AM13 RLD2_B_DQ44 15
IO_L19N_26 AP7 RLD2_B_DQ45 15
IO_L19P_26 AR6 RLD2_B_DQ46 15
IO_L1N_26 AT9 RLD2_B_DQ47 15
IO_L1P_26 AR10 RLD2_B_DQ48 15
IO_L2N_26 AK10 RLD2_B_DQ49 15
IO_L2P_26 AL10 RLD2_B_DQ50 15
IO_L3N_26 AN11 RLD2_B_DQ51 15
IO_L3P_26 AP10 RLD2_B_DQ52 15
IO_L4N_VREF_26 AJ11
IO_L4P_26 AJ10 RLD2_B_DQ53 15
IO_L5N_26 AP12 RLD2_B_DQ54 15
IO_L5P_26 AP11 RLD2_B_DQ55 15
IO_L6N_26 AN10 RLD2_B_DQ56 15
IO_L6P_26 AN9 RLD2_B_DQ57 15
IO_L7N_26 AL11 RLD2_B_DQ58 15
IO_L7P_26 AM11 RLD2_B_DQ59 15
IO_L8N_CC_26 AT7 RLD2_B_DQ60 15
IO_L8P_CC_26 AR7 RLD2_B_DQ61 15
IO_L9N_CC_26 AK12 RLD2_B_DQ62 15
IO_L9P_CC_26 AJ12 RLD2_B_DQ63 15
BANK 26
FF1759
FPGA_1V5
C849 4.7UF 10V 10%
RLDRII_VREFR
U1
AE7 VCCO1_14
AG10 VCCO2_14
AH7 VCCO3_14
AL8 VCCO4_14
AN6 VCCO5_14
IO_L0N_14 AF12 RLD2_B_WE_B 14,15
IO_L0P_14 AG12 RLD2_B_REF_B 14,15
IO_L10N_CC_14 AH8 RLD2_B_CLK0_N
IO_L10P_CC_14 AG8 RLD2_B_CLK0_P
IO_L11N_CC_14 AL7 RLD2_B_CLK1_N
IO_L11P_CC_14 AK8 RLD2_B_CLK1_P
IO_L12N_VRP_14 AJ7 RLD2_B_DK3_N
IO_L12P_VRN_14 AJ6 RLD2_B_DK3_P
IO_L13N_14 AJ8 RLD2_B_DK2_N
IO_L13P_14 AH9 RLD2_B_DK2_P
IO_L14N_VREF_14 AL6
IO_L14P_14 AK7 RLD2_B_CS0_B 14,15
IO_L15N_14 AP6 RLD2_B_DK1_N
IO_L15P_14 AP5 RLD2_B_DK1_P
IO_L16N_14 AE9 RLD2_B_DK0_N
IO_L16P_14 AF9 RLD2_B_DK0_P
IO_L17N_14 AE10 RLD2_B_BA0 14,15
IO_L17P_14 AD10 RLD2_B_BA1 14,15
IO_L18N_14 AN5 RLD2_B_BA2 14,15
IO_L18P_14 AM5 RLD2_B_A0 14,15
IO_L19N_14 AM7 RLD2_B_A1 14,15
IO_L19P_14 AM6 RLD2_B_A2 14,15
IO_L1N_14 AD6 RLD2_B_A3 14,15
IO_L1P_14 AD7 RLD2_B_A4 14,15
IO_L2N_14 AG11 RLD2_B_A5 14,15
IO_L2P_14 AF11 RLD2_B_A6 14,15
IO_L3N_14 AF7 RLD2_B_A7 14,15
IO_L3P_14 AE8 RLD2_B_A8 14,15
IO_L4N_VREF_14 AH10
IO_L4P_14 AH11 RLD2_B_A9 14,15
IO_L5N_14 AF6 RLD2_B_A10 14,15
IO_L5P_14 AF5 RLD2_B_A11 14,15
IO_L6N_14 AL9 RLD2_B_A12 14,15
IO_L6P_14 AK9 RLD2_B_A13 14,15
IO_L7N_14 AH5 RLD2_B_A14 14,15
IO_L7P_14 AG6 RLD2_B_A15 14,15
IO_L8N_CC_14 AG9 RLD2_B_A16 14,15
IO_L8P_CC_14 AF10 RLD2_B_A17 14,15
IO_L9N_CC_14 AH6 RLD2_B_A18 14,15
IO_L9P_CC_14 AG7 RLD2_B_A19 14,15
BANK 14
FF1759
FPGA BYPASS CAPS FOR BANKS 30, 26, 14
FPGA_1V5
C946 0.1UF 10% 35V X5R
C945 0.1UF 10% 35V X5R
C944 0.1UF 10% 35V X5R
C942 0.1UF 10% 35V X5R
C943 0.1UF 10% 35V X5R
C941 0.1UF 10% 35V X5R
C940 0.1UF 10% 35V X5R
RLDRII_VREFR
C464 .22UF 10% 6.3V X5R
C463 2.2UF 20% 4V X5R
FPGA_1V5
C939 0.1UF 10% 35V X5R
C938 0.1UF 10% 35V X5R
C937 0.1UF 10% 35V X5R
C935 0.1UF 10% 35V X5R
C936 0.1UF 10% 35V X5R
C934 0.1UF 10% 35V X5R
C933 0.1UF 10% 35V X5R
HITECH GLOBAL
TITLE
V5TXT-PCIE
RLDRII C INTERFACE
SIZE C
DWG NO HTG-V5-PCIE
REV 4.0
DRAWN BY S.S
SCALE
SHEET 14 of 32
6-24-2010_20:53
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TERMINATION RESISTORS

RLDRII_VTTR

RLDRII_VTTR

RLDRII_VTTR

RLDRII_VTTR

2V5

RLDRII_VREFR

RLDRII_VTTR

2V5 1V5 1V8

14,15 RLD2_B_REF_B

TFBGA144

MT49H16M36HT-25:A

U11

1V8

1V5

RLDRII_VTTR

RLDRII_VTTR

1V5

NOTE:
CLK0_P AND CLK0_N MASTER CLK U10
CLK1_P AND CLK1_N MASTER CLK U11
DQ0-DQ17 INPUT ARE REFERENCED TO DK0_P AND DK0_N
DQ18-DQ35 INPUT ARE REFERENCED TO DK1_P AND DK1_N
DQ0-DQ8 OUTPUT ARE REFERENCED TO QK0_P AND QK0_N
DQ9-DQ17 OUTPUT ARE REFERENCED TO QK1_P AND QK1_N
DQ18-DQ26 OUTPUT ARE REFERENCED TO QK2_P AND QK2_N
DQ27-DQ35 OUTPUT ARE REFERENCED TO QK3_P AND QK3_N

HITECH GLOBAL

TITLE

V5TXT-PCIE
RLDRII D INTERFACE

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		15 of 32	6-24-2010_20:53

CONFIDENTIAL

QDR2_2MX36
FBGA165

CY7C1515JV18-300BZXC

U4

1V5 1V8 QDRII_VREF QDRII_VTT

R321 499 1%
R322 499 1%
R323 10K 5%
R320 100 5%

QDR2_A_DOFF_B

DLLB ZQ

VSS13 VSS12 VSS11 VSS10 VSS9 VSS8 VSS7 VSS6 VSS5 VSS4 VSS3 VSS2 VSS1

VDDQ16 VDDQ15 VDDQ14 VDDQ13 VDDQ12 VDDQ11 VDDQ10 VDDQ9 VDDQ8 VDDQ7 VDDQ6 VDDQ5 VDDQ4 VDDQ3 VDDQ2 VDDQ1 VDD10 VDD9 VDD8 VDD7 VDD6 VDD5 VDD4 VDD3 VDD2 VDD1

VREF2 VREF1

C572 .22UF 10% 6.3V X5R
C571 .22UF 10% 6.3V X5R

C619 .22UF 10% 6.3V X5R
C618 .22UF 10% 6.3V X5R
C617 2.2UF 20% 4V X5R
C616 .22UF 10% 6.3V X5R
C615 .22UF 10% 6.3V X5R
C623 2.2UF 20% 4V X5R

R378 R377 R136 R376 R375 R374 R373 R372 R371 R370 R369 R368 R367 R366 R365 R364 R363 R362 R361 R325 R324 R424 R423 — 49.9 1%

QDR2_A_A0 QDR2_A_A1 QDR2_A_A2 QDR2_A_A3 QDR2_A_A4 QDR2_A_A5 QDR2_A_A6 QDR2_A_A7 QDR2_A_A8 QDR2_A_A9 QDR2_A_A10 QDR2_A_A11 QDR2_A_A12 QDR2_A_A13 QDR2_A_A14 QDR2_A_A15 QDR2_A_A16 QDR2_A_A17 QDR2_A_A18 QDR2_RW_B QDR2_A_LD QDR2_A_K_P QDR2_A_K_N

16,17

QDR2_A_C_P P6 C
QDR2_A_C_N R6 CB

16,17 QDR2_A_K_P B6 K
16,17 QDR2_A_K_N A6 KB

16,17	QDR2_A_D0	P10	D0
16,17	QDR2_A_D1	N11	D1
16,17	QDR2_A_D2	M11	D2
16,17	QDR2_A_D3	K10	D3
16,17	QDR2_A_D4	J11	D4
16,17	QDR2_A_D5	G11	D5
16,17	QDR2_A_D6	E10	D6
16,17	QDR2_A_D7	D11	D7
16,17	QDR2_A_D8	C11	D8
16,17	QDR2_A_D9	N10	D9
16,17	QDR2_A_D10	M9	D10
16,17	QDR2_A_D11	L9	D11
16,17	QDR2_A_D12	J9	D12
16,17	QDR2_A_D13	G10	D13
16,17	QDR2_A_D14	F9	D14
16,17	QDR2_A_D15	D10	D15
16,17	QDR2_A_D16	C9	D16
16,17	QDR2_A_D17	B9	D17
16,17	QDR2_A_D18	B3	D18
16,17	QDR2_A_D19	C3	D19
16,17	QDR2_A_D20	D2	D20
16,17	QDR2_A_D21	F3	D21
16,17	QDR2_A_D22	G2	D22
16,17	QDR2_A_D23	J3	D23
16,17	QDR2_A_D24	L3	D24
16,17	QDR2_A_D25	M3	D25
16,17	QDR2_A_D26	N2	D26
16,17	QDR2_A_D27	C1	D27
16,17	QDR2_A_D28	D1	D28
16,17	QDR2_A_D29	E2	D29
16,17	QDR2_A_D30	G1	D30
16,17	QDR2_A_D31	J1	D31
16,17	QDR2_A_D32	K2	D32
16,17	QDR2_A_D33	M1	D33
16,17	QDR2_A_D34	N1	D34
16,17	QDR2_A_D35	P2	D35

CQ	A11	QDR2_A_CQ_P	17
CQB	A1	QDR2_A_CQ_N	17
Q0	P11	QDR2_A_DQ0	17
Q1	M10	QDR2_A_DQ1	17
Q2	L11	QDR2_A_DQ2	17
Q3	K11	QDR2_A_DQ3	17
Q4	J10	QDR2_A_DQ4	17
Q5	F11	QDR2_A_DQ5	17
Q6	E11	QDR2_A_DQ6	17
Q7	C10	QDR2_A_DQ7	17
Q8	B11	QDR2_A_DQ8	17
Q9	P9	QDR2_A_DQ9	17
Q10	N9	QDR2_A_DQ10	17
Q11	L10	QDR2_A_DQ11	17
Q12	K9	QDR2_A_DQ12	17
Q13	G9	QDR2_A_DQ13	17
Q14	F10	QDR2_A_DQ14	17
Q15	E9	QDR2_A_DQ15	17
Q16	D9	QDR2_A_DQ16	17
Q17	B10	QDR2_A_DQ17	17
Q18	B2	QDR2_A_DQ18	17
Q19	D3	QDR2_A_DQ19	17
Q20	E3	QDR2_A_DQ20	17
Q21	F2	QDR2_A_DQ21	17
Q22	G3	QDR2_A_DQ22	17
Q23	K3	QDR2_A_DQ23	17
Q24	L2	QDR2_A_DQ24	17
Q25	N3	QDR2_A_DQ25	17
Q26	P3	QDR2_A_DQ26	17
Q27	B1	QDR2_A_DQ27	17
Q28	C2	QDR2_A_DQ28	17
Q29	E1	QDR2_A_DQ29	17
Q30	F1	QDR2_A_DQ30	17
Q31	J2	QDR2_A_DQ31	17
Q32	K1	QDR2_A_DQ32	17
Q33	L1	QDR2_A_DQ33	17
Q34	M2	QDR2_A_DQ34	17
Q35	P1	QDR2_A_DQ35	17

RB WB BW0B BW1B BW2B BW3B A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 NC2 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 TDO TDI TMS TCK

A8 A4 B7 A7 A6 B5 A3 A9 B4 B8 C5 C7 N5 N6 N7 P4 P5 P7 P8 R3 R4 R5 R7 R8 R9 C6 G6 H6 J6 K6 L5 L6 L7 M4 M5 M6 M7 M8 N4 N8 R1 R11 R10 R2

QDR2_A_LD QDR2_A_RW_B QDR2_A_BW0B QDR2_A_BW1B QDR2_A_BW2B QDR2_A_BW3B QDR2_A_A0 QDR2_A_A1 QDR2_A_A2 QDR2_A_A3 QDR2_A_A4 QDR2_A_A5 QDR2_A_A6 QDR2_A_A7 QDR2_A_A8 QDR2_A_A9 QDR2_A_A10 QDR2_A_A11 QDR2_A_A12 QDR2_A_A13 QDR2_A_A14 QDR2_A_A15 QDR2_A_A16 QDR2_A_A17 QDR2_A_A18

NC NC NC NC

C592 10UF 20% 6.3V X5R
C591 2.2UF 20% 4V X5R
C593 2.2UF 20% 4V X5R
C594 2.2UF 20% 4V X5R
C590 2.2UF 20% 4V X5R
C595 .22UF 10% 6.3V X5R
C589 .22UF 10% 6.3V X5R
C588 .22UF 10% 6.3V X5R
C587 .22UF 10% 6.3V X5R
C586 .22UF 10% 6.3V X5R
C585 .22UF 10% 6.3V X5R

C576 10UF 20% 6.3V X5R
C578 2.2UF 20% 4V X5R
C574 2.2UF 20% 4V X5R
C573 2.2UF 20% 4V X5R

C584 .22UF 10% 6.3V X5R
C583 .22UF 10% 6.3V X5R
C582 .22UF 10% 6.3V X5R
C581 .22UF 10% 6.3V X5R
C580 .22UF 10% 6.3V X5R
C579 .22UF 10% 6.3V X5R

C620 .22UF 10% 6.3V X5R
C614 .22UF 10% 6.3V X5R
C613 .22UF 10% 6.3V X5R
C612 .22UF 10% 6.3V X5R
C611 .22UF 10% 6.3V X5R
C610 .22UF 10% 6.3V X5R
C621 2.2UF 20% 4V X5R
C622 2.2UF 20% 4V X5R
C609 2.2UF 20% 4V X5R
C608 2.2UF 20% 4V X5R
C607 10UF 20% 6.3V X5R

C599 10UF 20% 6.3V X5R
C597 2.2UF 20% 4V X5R
C598 2.2UF 20% 4V X5R
C600 2.2UF 20% 4V X5R

R358 R357 R356 R355 R354 R353 R352 R351 R350 R349 R348 R347 R346 R345 R344 R343 R342 R341 R340 R339 R338 R337 R336 R335 R334 R333 R332 R331 R330 R329 R328 R327 R326 R381 R380 R379 — 49.9 1%

QDR2_A_D0 QDR2_A_D1 QDR2_A_D2 QDR2_A_D3 QDR2_A_D4 QDR2_A_D5 QDR2_A_D6 QDR2_A_D7 QDR2_A_D8 QDR2_A_D9 QDR2_A_D10 QDR2_A_D11 QDR2_A_D12 QDR2_A_D13 QDR2_A_D14 QDR2_A_D15 QDR2_A_D16 QDR2_A_D17 QDR2_A_D18 QDR2_A_D19 QDR2_A_D20 QDR2_A_D21 QDR2_A_D22 QDR2_A_D23 QDR2_A_D24 QDR2_A_D25 QDR2_A_D26 QDR2_A_D27 QDR2_A_D28 QDR2_A_D29 QDR2_A_D30 QDR2_A_D31 QDR2_A_D32 QDR2_A_D33 QDR2_A_D34 QDR2_A_D35

16,17

1. DATA (D0-D35) INPUT SIGNALS ARE
   SAMPLED ON RISING EDGE OF K AND K#
2. DATA (DQ0-DQ35) OUTPUT SIGNALS ARE
   DRIVEN OUT ON RISING EDGE OF C AND C#
3. BWS ARE SAMPLED ON THE RISING EDGE OF K AND #K
   CLOCKS WHEN WRITE OPERATIONS ARE ACTIVE
4. BWS DETERMINES WHICH BYTE IS WRITTEN INTO DEVICE
   BWS0 - D[8:0], BWS1 - D[17:9],
   BWS2 - D[26:18], BWS3 - D[35:27]

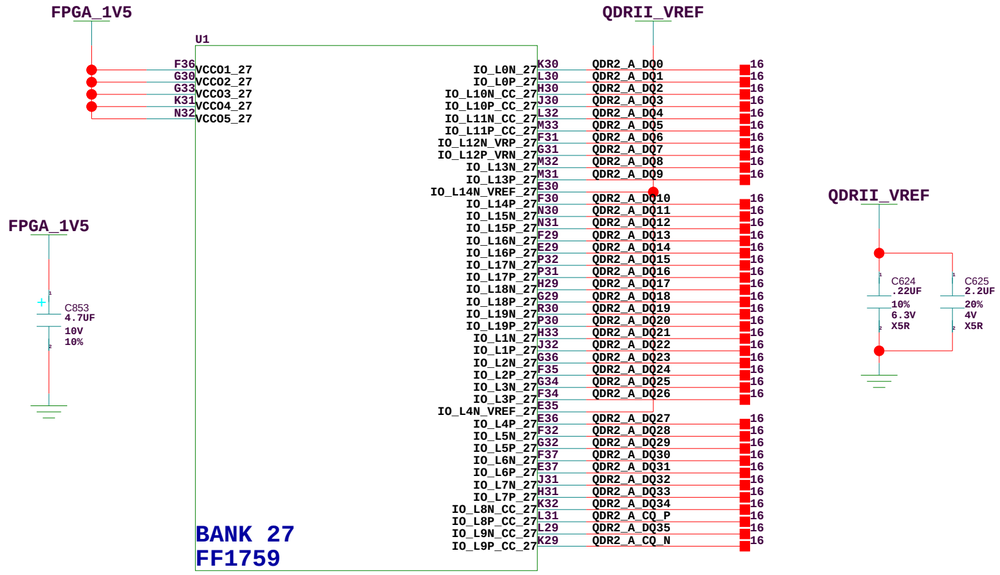
CONFIDENTIAL

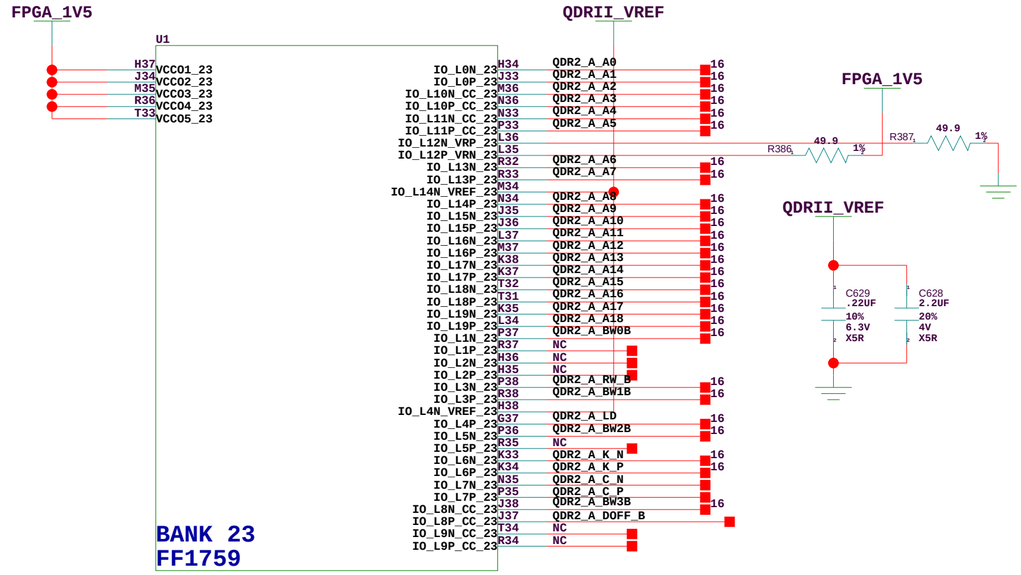
HITECH GLOBAL

TITLE
V5TXT-PCIE
QDRII A INTERFACE

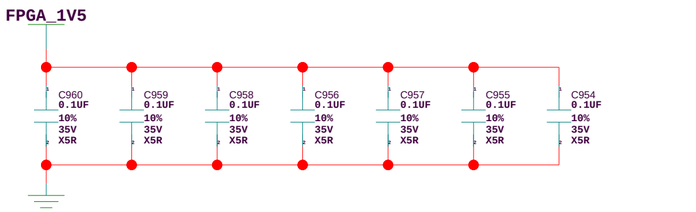
SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

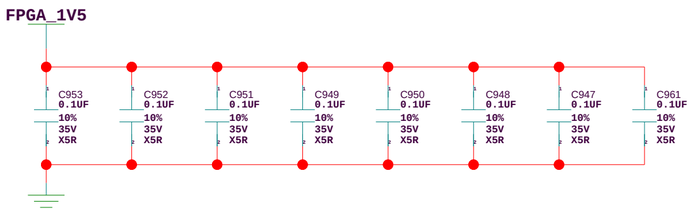
DRAWN BY	SCALE	SHEET	
S.S		16 of 32	6-24-2010_20:53

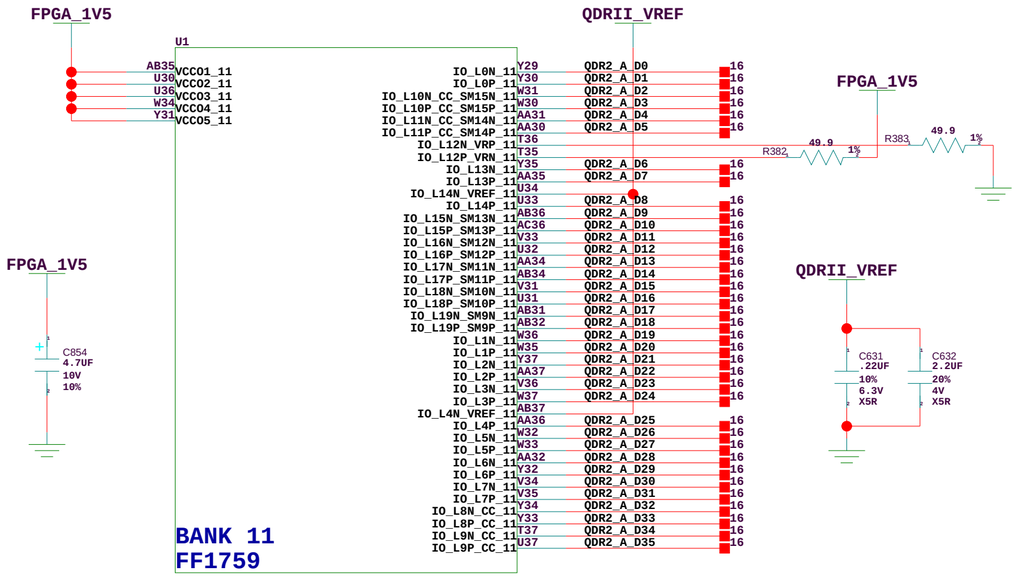




FPGA BYPASS CAPS FOR BANKS 27, 23, 11







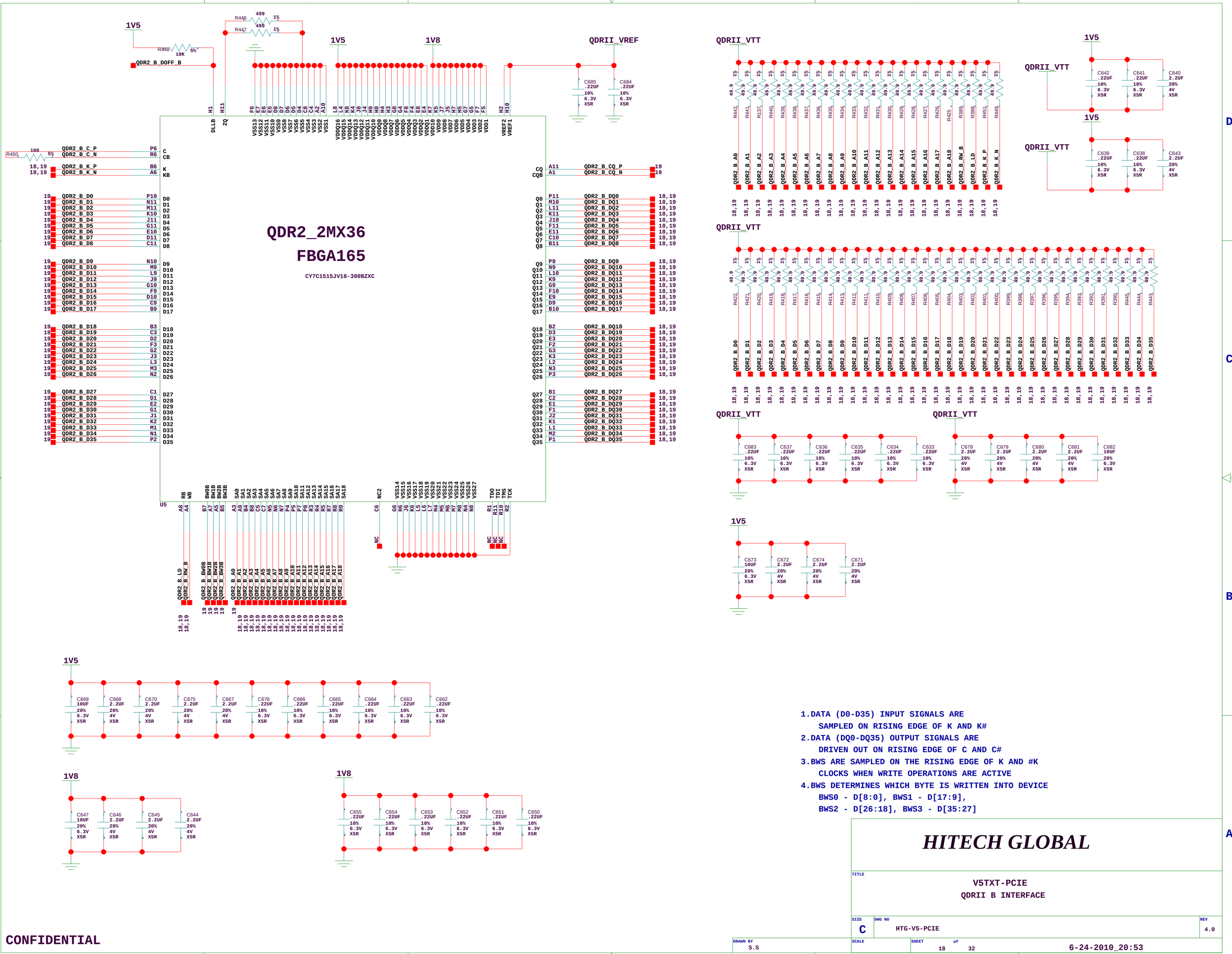
CONFIDENTIAL

HITECH GLOBAL

TITLE
V5TXT-PCIE
QDRII A FPGA INTERFACE

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		17 of 32	6-24-2010_20:53



1. DATA (D0-D35) INPUT SIGNALS ARE
   SAMPLED ON RISING EDGE OF K AND K#
2. DATA (DQ0-DQ35) OUTPUT SIGNALS ARE
   DRIVEN OUT ON RISING EDGE OF C AND C#
3. BWS ARE SAMPLED ON THE RISING EDGE OF K AND #K
   CLOCKS WHEN WRITE OPERATIONS ARE ACTIVE
4. BWS DETERMINES WHICH BYTE IS WRITTEN INTO DEVICE
   BWS0 - D[8:0], BWS1 - D[17:9],
   BWS2 - D[26:18], BWS3 - D[35:27]

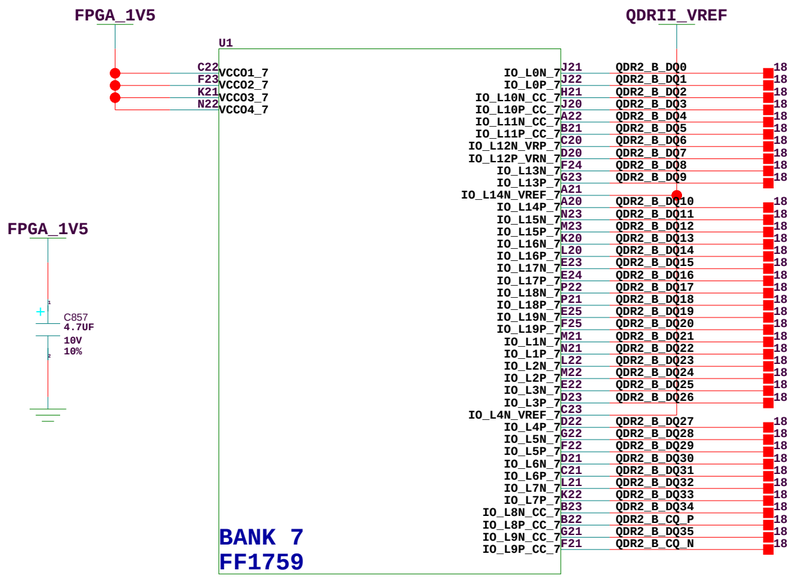
CONFIDENTIAL

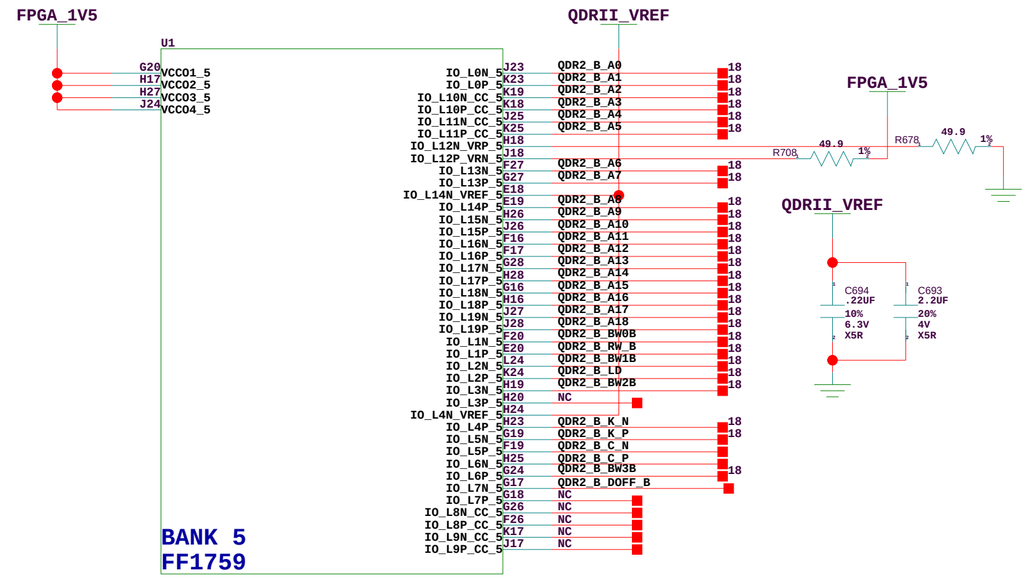
HITECH GLOBAL

TITLE: V5TXT-PCIE
QDRII B INTERFACE

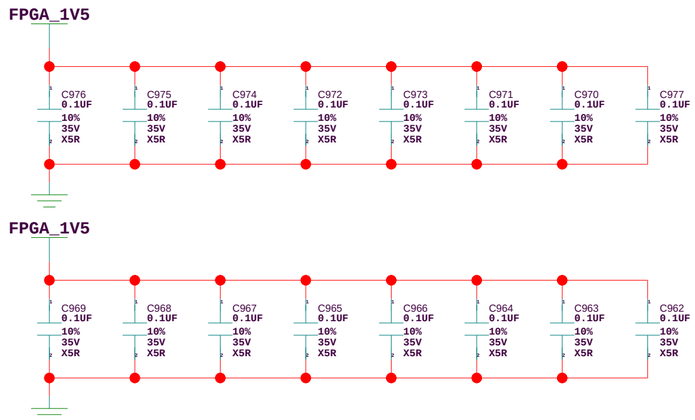
SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

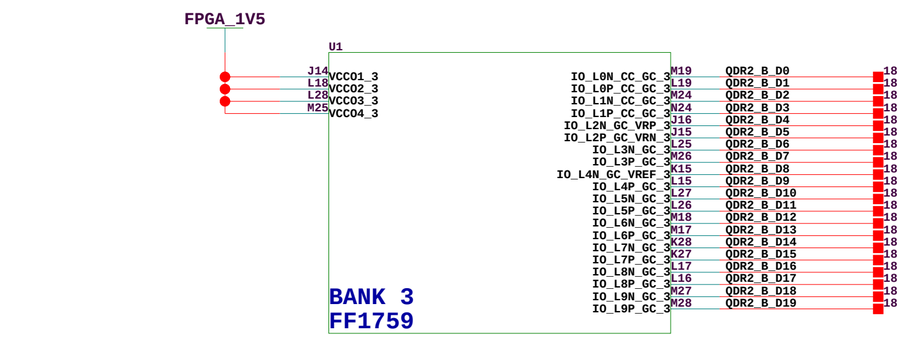
DRAWN BY	SCALE	SHEET	of	
S.S		18	32	6-24-2010_20:53

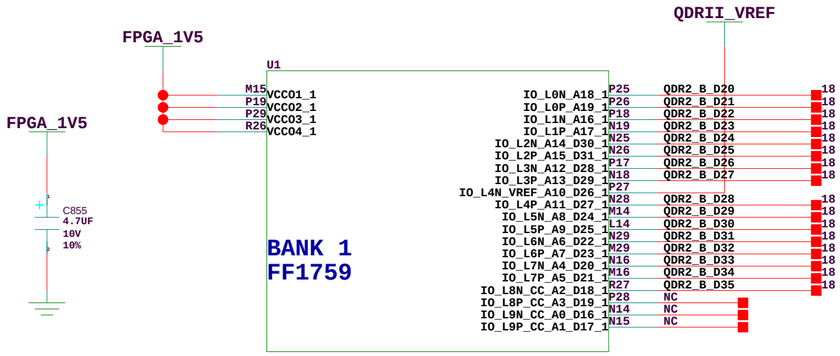




FPGA BYPASS CAPS FOR BANKS 7, 5, 3, 1







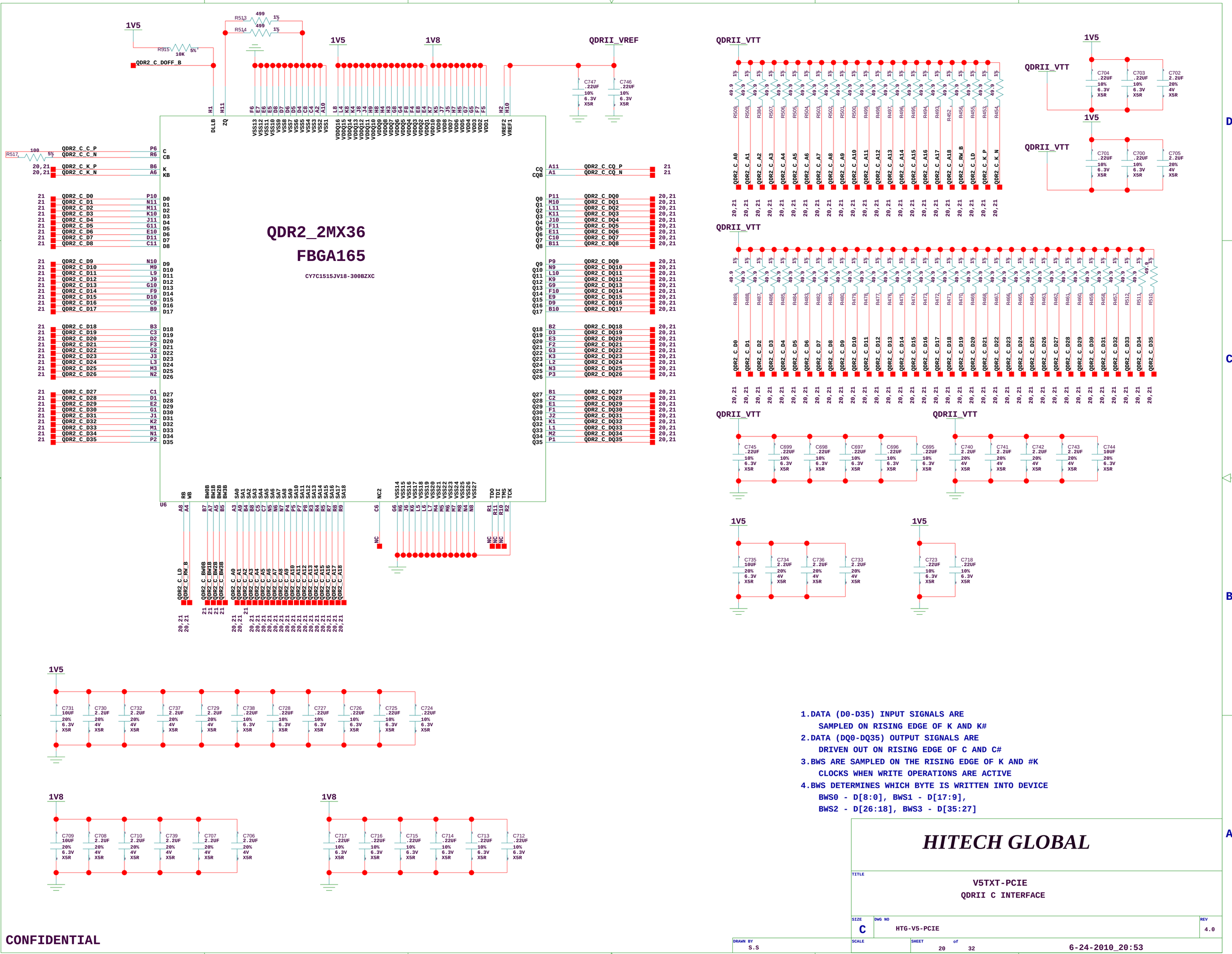
CONFIDENTIAL

HITECH GLOBAL

TITLE
V5TXT-PCIE
QDRII B FPGA INTERFACE

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		19 of 32	6-24-2010_20:53



1. DATA (D0-D35) INPUT SIGNALS ARE
   SAMPLED ON RISING EDGE OF K AND K#
2. DATA (DQ0-DQ35) OUTPUT SIGNALS ARE
   DRIVEN OUT ON RISING EDGE OF C AND C#
3. BWS ARE SAMPLED ON THE RISING EDGE OF K AND #K
   CLOCKS WHEN WRITE OPERATIONS ARE ACTIVE
4. BWS DETERMINES WHICH BYTE IS WRITTEN INTO DEVICE
   BWS0 - D[8:0], BWS1 - D[17:9],
   BWS2 - D[26:18], BWS3 - D[35:27]

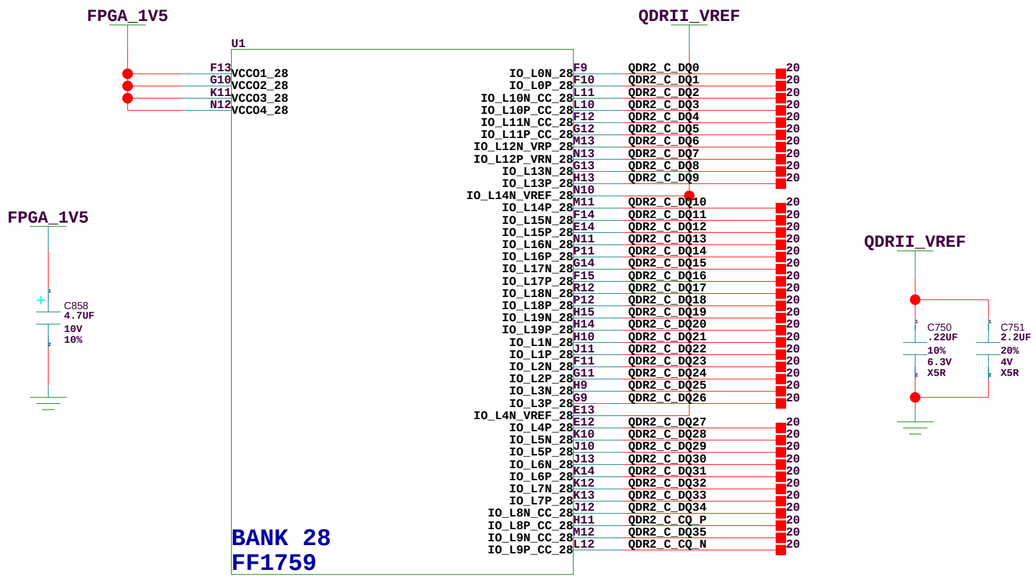
CONFIDENTIAL

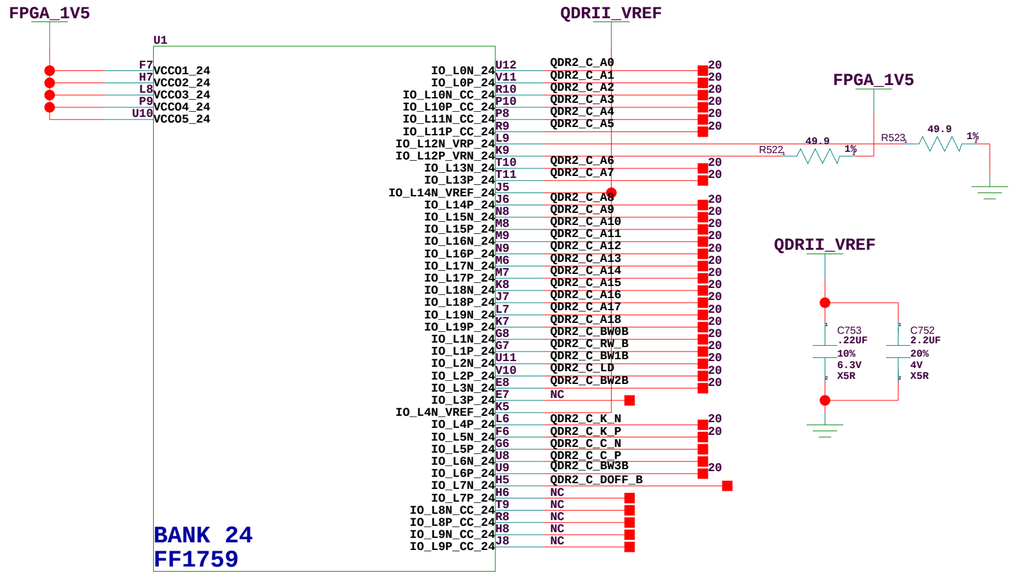
HITECH GLOBAL

TITLE: V5TXT-PCIE
QDRII C INTERFACE

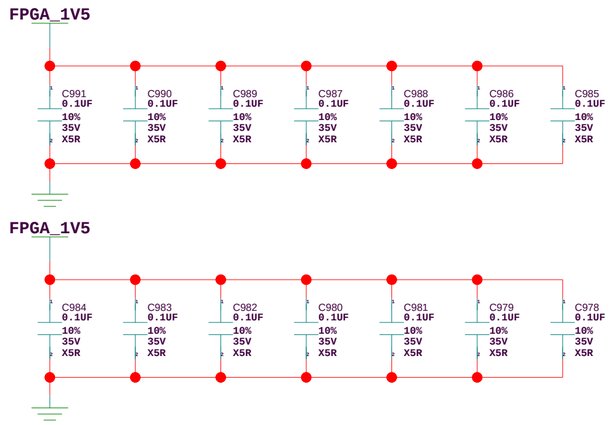
SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

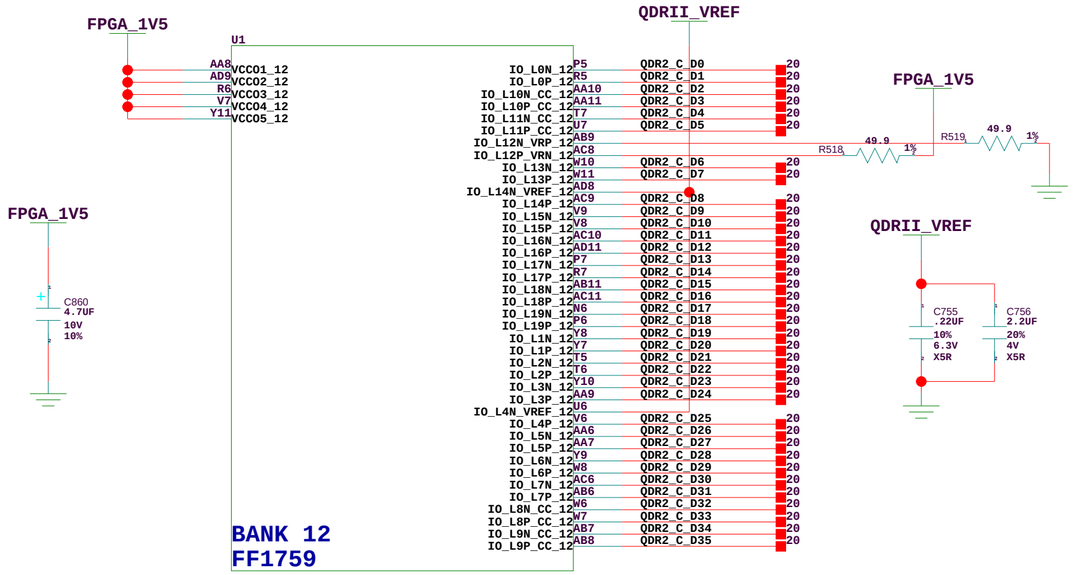
DRAWN BY	SCALE	SHEET	
S.S		20 of 32	6-24-2010_20:53





FPGA BYPASS CAPS FOR BANKS 28, 24, 12





CONFIDENTIAL

HITECH GLOBAL

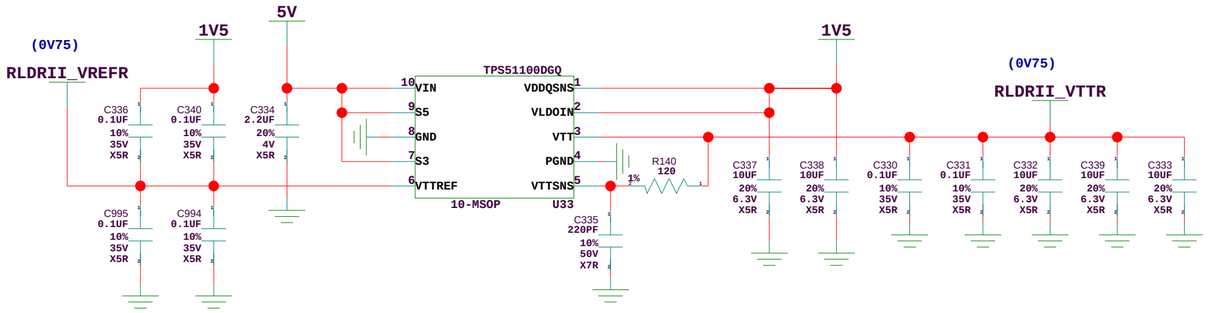
TITLE
V5TXT-PCIE
QDRII C FPGA INTERFACE

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		21 of 32	6-24-2010_20:53

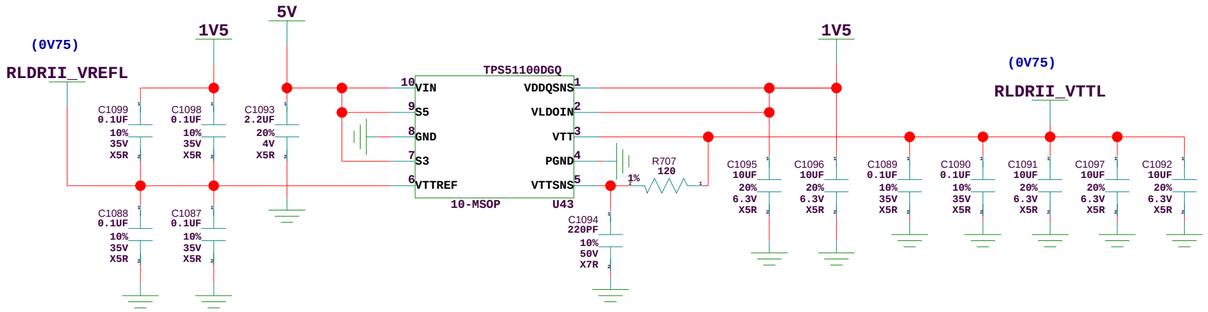
RLDRAMII RIGHT-TERMINATION POWER SUPPLY

POWER SUPPLY CAN SOURCE AND SINK 3A



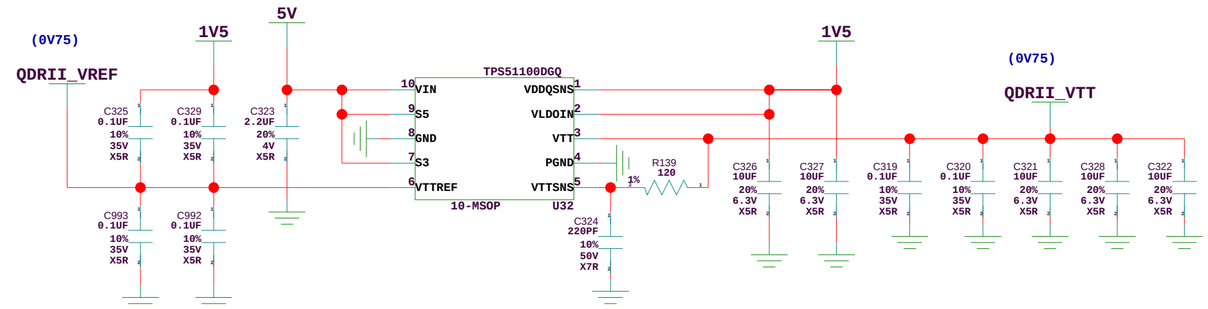
RLDRAMII LEFT-TERMINATION POWER SUPPLY

POWER SUPPLY CAN SOURCE AND SINK 3A



QDRII-TERMINATION POWER SUPPLY

POWER SUPPLY CAN SOURCE AND SINK 3A



CONFIDENTIAL

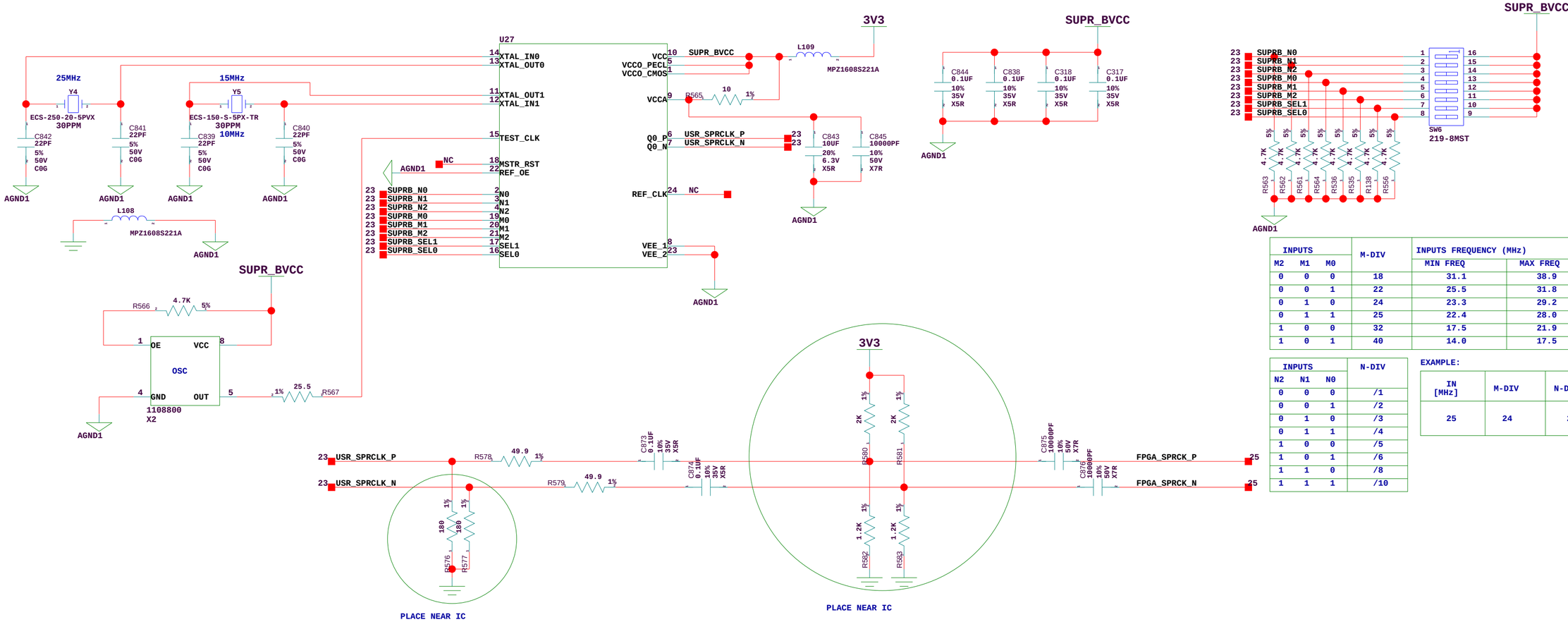
HITECH GLOBAL

TITLE: V5TXT-PCIE
RLDRAMII, QDRII TERMINATION POWER SUPPLY

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		22 of 32	6-24-2010_20:53

USER CLOCK GENERATOR



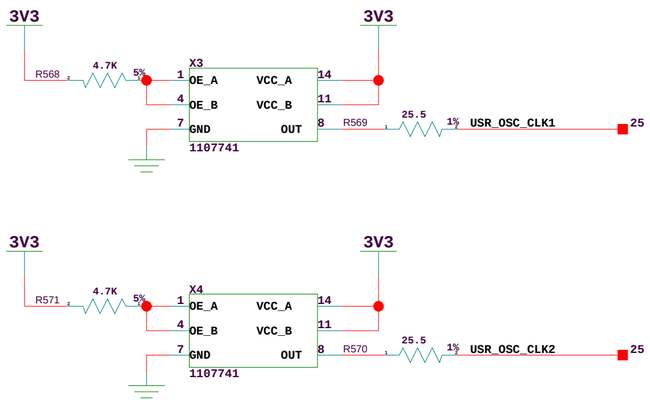
INPUTS			M-DIV	INPUTS FREQUENCY (MHz)	
M2	M1	M0		MIN FREQ	MAX FREQ
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

INPUTS			N-DIV
N2	N1	N0	
0	0	0	/1
0	0	1	/2
0	1	0	/3
0	1	1	/4
1	0	0	/5
1	0	1	/6
1	1	0	/8
1	1	1	/10

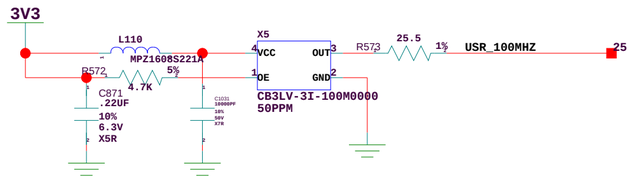
EXAMPLE:

IN [MHz]	M-DIV	N-DIV	OUT [MHz]
25	24	2	300

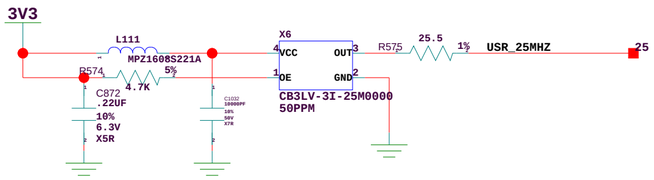
USER OSCILLATOR SOCKET CLOCKS



100MHz USER CLOCK



25MHz USER CLOCK



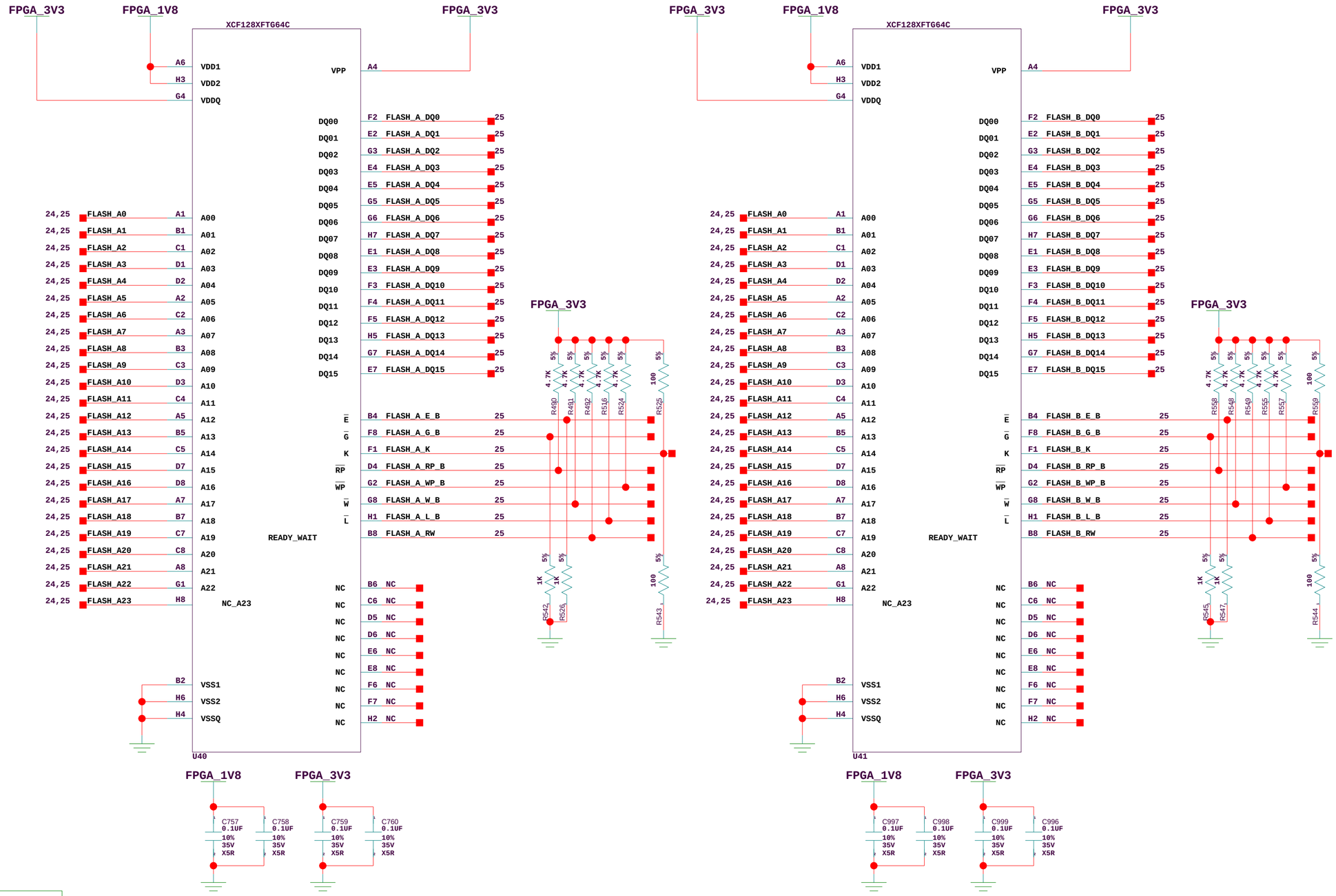
CONFIDENTIAL

HITECH GLOBAL

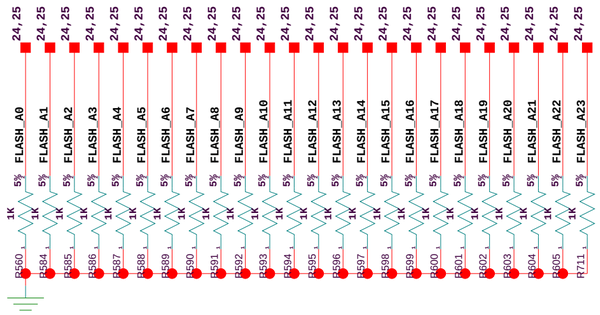
TITLE: V5TXT-PCIE
USER CLOCKS

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		23 of 32	6-24-2010_20:53



TERMINATION RESISTORS



CONFIDENTIAL

HITECH GLOBAL

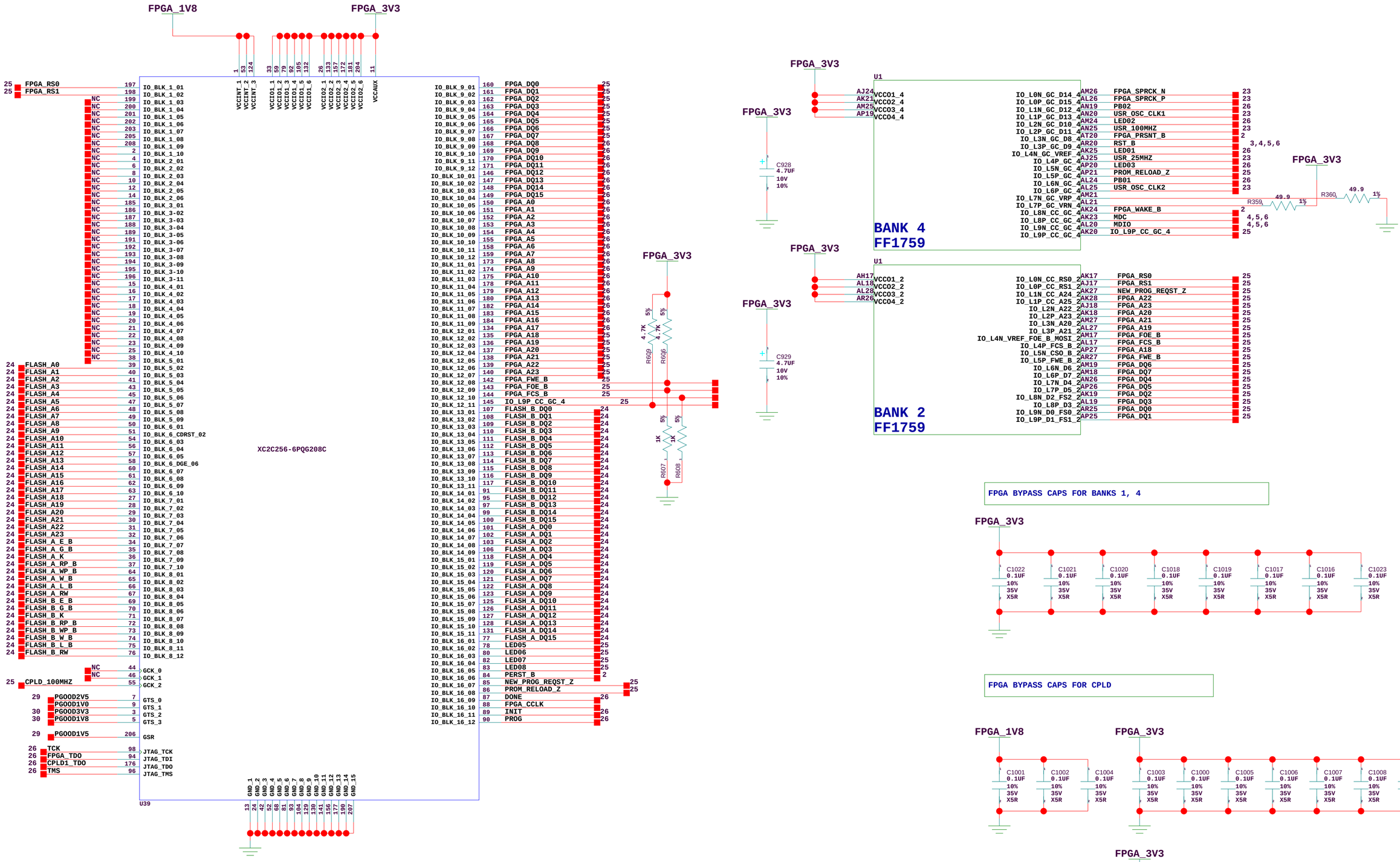
TITLE

V5TXT-PCIE

FLASH A AND B INTERFACE

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		24 of 32	6-24-2010_20:53



HITECH GLOBAL

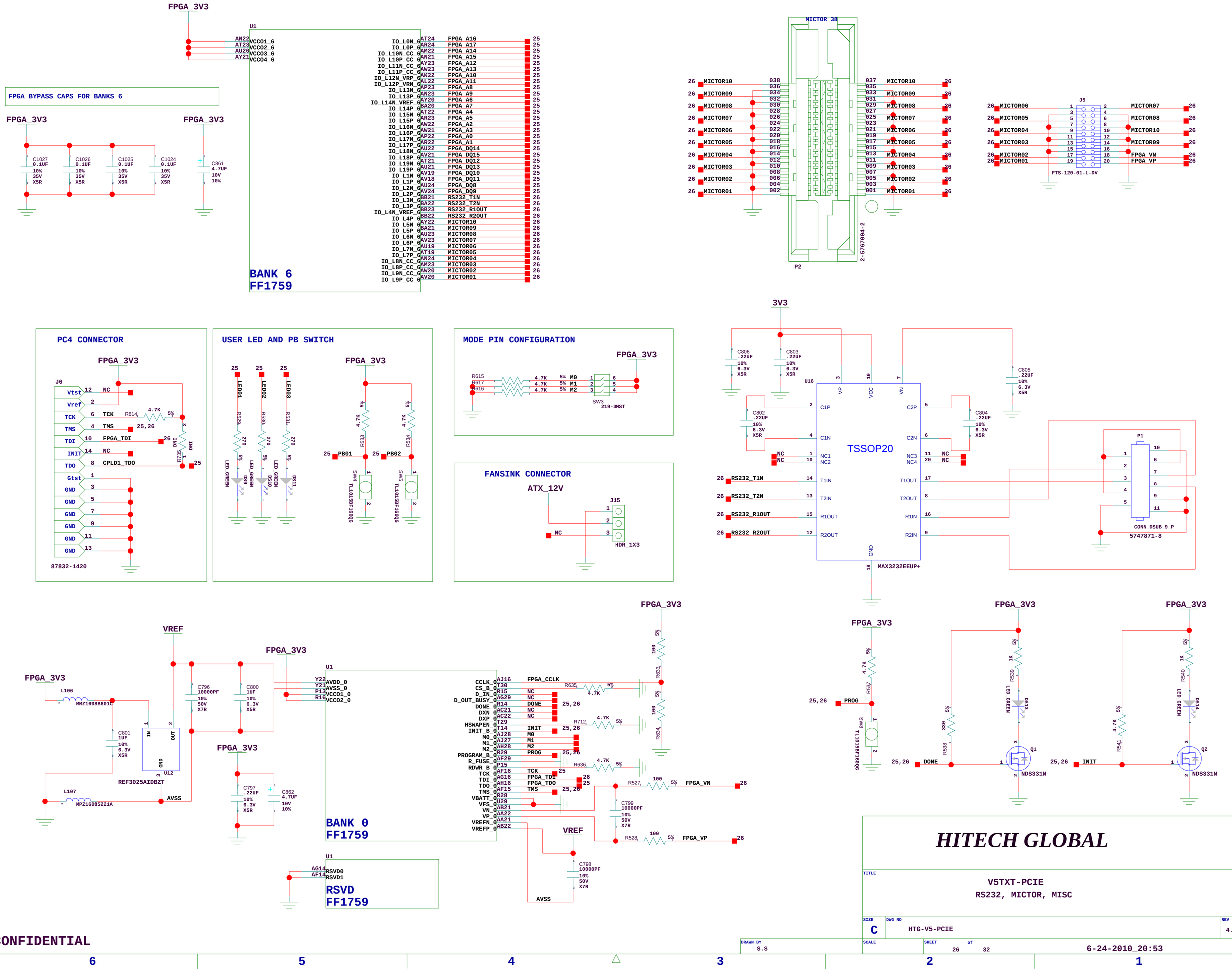
TITLE

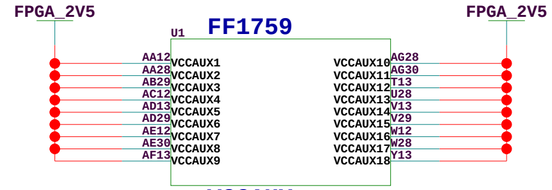
V5TXT-PCIE

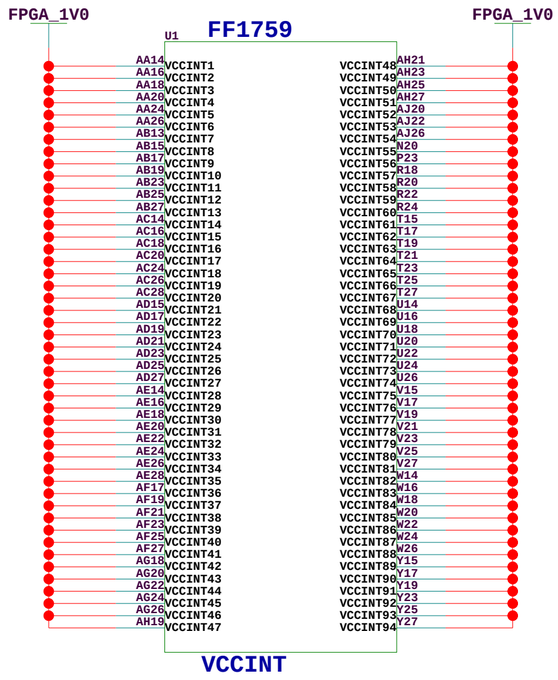
CPLD TO FGPA INTERFACE

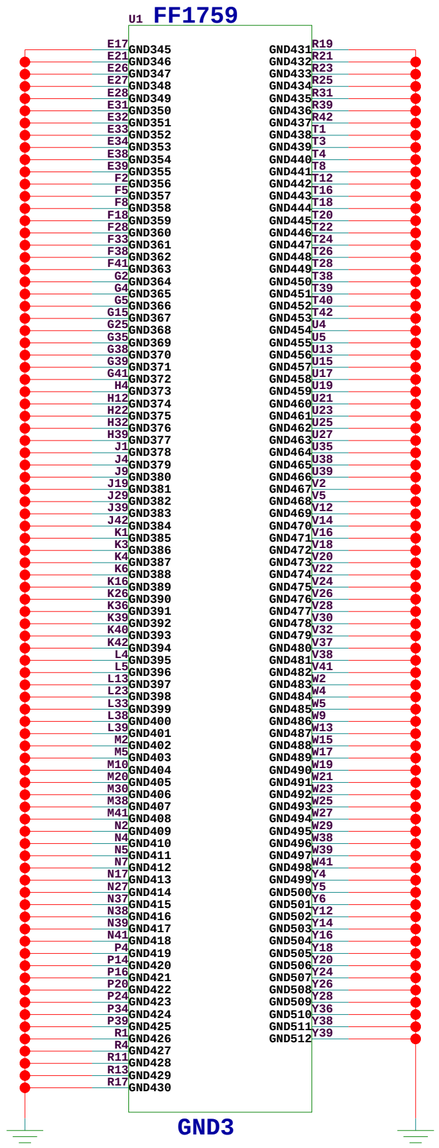
SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

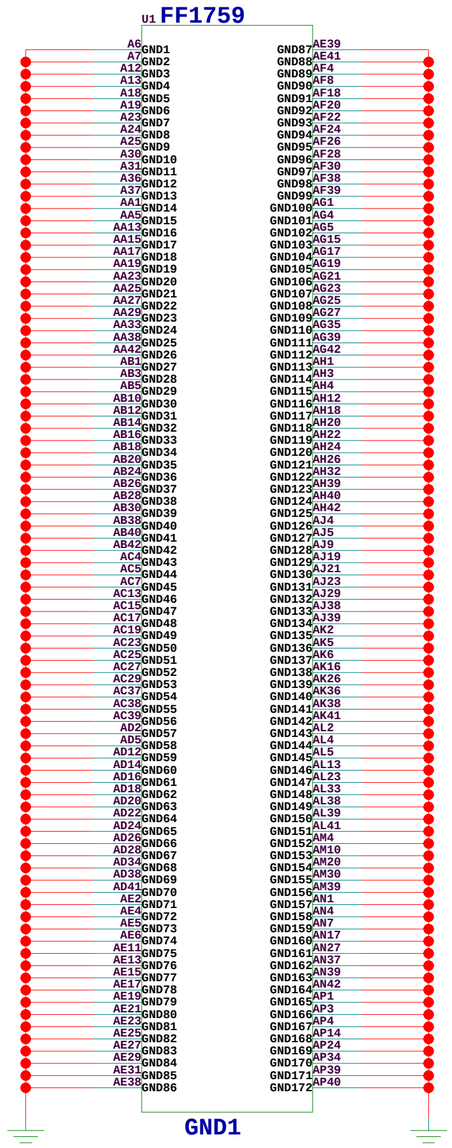
DRAWN BY	SCALE	SHEET	
S.S		25 of 32	6-24-2010_20:53

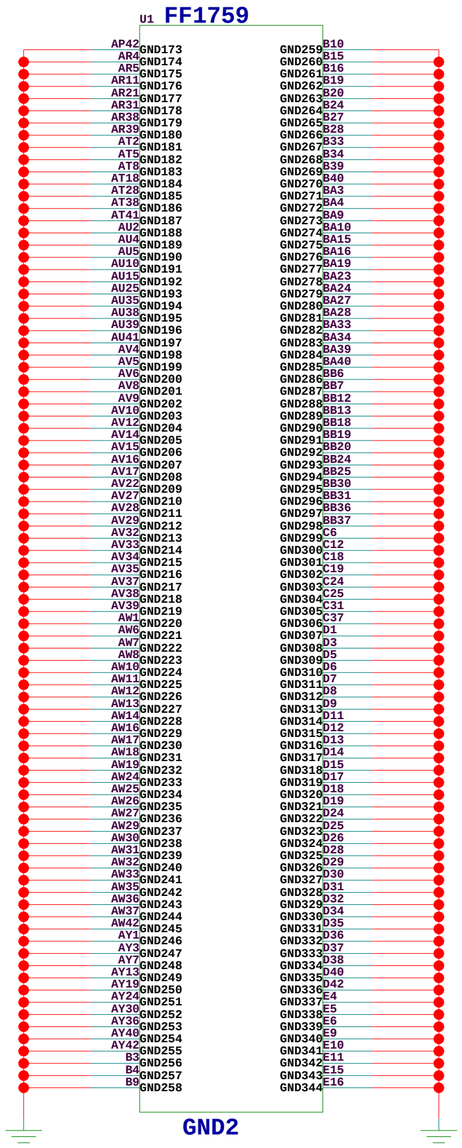

FPGA_3V3
U1
AN22 VCCO1_6
AT23 VCCO2_6
AU26 VCCO3_6
AY21 VCCO4_6
IO_L0N_6 AT24 FPGA_A16 25
IO_L0P_6 AR24 FPGA_A17 25
IO_L10N_CC_6 AM22 FPGA_A14 25
IO_L10P_CC_6 AN21 FPGA_A15 25
IO_L11N_CC_6 AY23 FPGA_A12 25
IO_L11P_CC_6 AW23 FPGA_A13 25
IO_L12N_VRP_6 AK22 FPGA_A10 25
IO_L12P_VRN_6 AL22 FPGA_A11 25
IO_L13N_6 AP23 FPGA_A8 25
IO_L13P_6 AN23 FPGA_A9 25
IO_L14N_VREF_6 AY20 FPGA_A6 25
IO_L14P_6 BA20 FPGA_A7 25
IO_L15N_6 AT22 FPGA_A4 25
IO_L15P_6 AR23 FPGA_A5 25
IO_L16N_6 AW22 FPGA_A2 25
IO_L16P_6 AW21 FPGA_A3 25
IO_L17N_6 AP22 FPGA_A0 25
IO_L17P_6 AR22 FPGA_A1 25
IO_L18N_6 AU22 FPGA_DQ14 25
IO_L18P_6 AV21 FPGA_DQ15 25
IO_L19N_6 AT21 FPGA_DQ12 25
IO_L19P_6 AU21 FPGA_DQ13 25
IO_L1N_6 AV19 FPGA_DQ10 25
IO_L1P_6 AV18 FPGA_DQ11 25
IO_L2N_6 AU24 FPGA_DQ8 25
IO_L2P_6 AV24 FPGA_DQ9 25
IO_L3N_6 BB21 RS232_T1N 26
IO_L3P_6 BA22 RS232_T2N 26
IO_L4N_VREF_6 BB23 RS232_R1OUT 26
IO_L4P_6 BB22 RS232_R2OUT 26
IO_L5N_6 AY22 MICTOR10 26
IO_L5P_6 BA21 MICTOR09 26
IO_L6N_6 AU23 MICTOR08 26
IO_L6P_6 AV23 MICTOR07 26
IO_L7N_6 AU19 MICTOR06 26
IO_L7P_6 AT19 MICTOR05 26
IO_L8N_CC_6 AN24 MICTOR04 26
IO_L8P_CC_6 AM23 MICTOR03 26
IO_L9N_CC_6 AW20 MICTOR02 26
IO_L9P_CC_6 AV20 MICTOR01 26
BANK 6
FF1759
FPGA BYPASS CAPS FOR BANKS 6
FPGA_3V3
C1027 0.1UF 10% 35V X5R
C1026 0.1UF 10% 35V X5R
C1025 0.1UF 10% 35V X5R
C1024 0.1UF 10% 35V X5R
FPGA_3V3
C861 4.7UF 10V 10%
MICTOR 38
P2
2-5767004-2
26 MICTOR10 038 037 MICTOR10 26
MICTOR09 036 035 MICTOR09
MICTOR08 034 033 MICTOR08
MICTOR07 032 031 MICTOR07
MICTOR06 030 029 MICTOR06
MICTOR05 028 027 MICTOR05
MICTOR04 026 025 MICTOR04
MICTOR03 024 023 MICTOR03
MICTOR02 022 021 MICTOR02
MICTOR01 020 019 MICTOR01
018 017
016 015
014 013
012 011
010 009
008 007
006 005
004 003
002 001
J5
FTS-120-01-L-DV
MICTOR06 MICTOR07
MICTOR05 MICTOR08
MICTOR04 MICTOR10
MICTOR03 MICTOR09
MICTOR02 FPGA_VN
MICTOR01 FPGA_VP
PC4 CONNECTOR
FPGA_3V3
J6
Vtst 12 NC
Vref 2
TCK 6 TCK R614 4.7K 5%
TMS 4 TMS 25,26
TDI 10 FPGA_TDI 26 DNI R735 0 DNI
INIT 14 NC
TDO 8 CPLD1_TDO 25
Gtst 1
GND 3
GND 5
GND 7
GND 9
GND 11
GND 13
87832-1420
USER LED AND PB SWITCH
FPGA_3V3
25 LED01 R529 270 5% LED_GREEN DS9
25 LED02 R530 270 5% LED_GREEN DS10
25 LED03 R531 270 5% LED_GREEN DS11
R533 4.7K 5%
R534 4.7K 5%
25 PB01 SW4 TL1015BF160QG
25 PB02 SW5 TL1015BF160QG
MODE PIN CONFIGURATION
FPGA_3V3
R615 R617 R616 4.7K 5%
M0 M1 M2
SW3 219-3MST
FANSINK CONNECTOR
ATX_12V
J15
NC
HDR_1X3
3V3
C806 .22UF 10% 6.3V X5R
C803 .22UF 10% 6.3V X5R
C805 .22UF 10% 6.3V X5R
U16
VP VCC VN
C1P C2P
C1N C2N
TSSOP20
NC1 NC2
NC3 NC4
T1IN T2IN
R1OUT R2OUT
T1OUT T2OUT
R1IN R2IN
GND
MAX3232EEUP+
C802 .22UF 10% 6.3V X5R
C804 .22UF 10% 6.3V X5R
26 RS232_T1N
26 RS232_T2N
26 RS232_R1OUT
26 RS232_R2OUT
P1
CONN_DSUB_9_P
5747871-8
VREF
FPGA_3V3
L106 MMZ1608B601C
C796 10000PF 10% 50V X7R
C800 1UF 10% 6.3V X5R
C801 1UF 10% 6.3V X5R
U12
IN OUT GND
REF3025AIDBZT
L107 MPZ1608S221A
AVSS
FPGA_3V3
C797 .22UF 10% 6.3V X5R
C862 4.7UF 10V 10%
U1
AVDD_0 AVSS_0 VCCO1_0 VCCO2_0
BANK 0
FF1759
CCLK_0 FPGA_CCLK
CS_B_0 NC
D_IN_0 NC
D_OUT_BUSY_0 DONE 25,26
DONE_0 NC
DXN_0 NC
DXP_0
HSWAPEN_0
INIT_B_0 INIT 25,26
M0_0 M0
M1_0 M1
M2_0 M2
PROGRAM_B_0 PROG 25,26
R_FUSE_0
RDWR_B_0
TCK_0 TCK 25
TDI_0 FPGA_TDI 26
TDO_0 FPGA_TDO 25
TMS_0 TMS 25,26
VBATT_0
VFS_0
VN_0
VP_0
VREFN_0
VREFP_0
R635 4.7K 5%
R712 4.7K 5%
R636 4.7K 5%
R633 100 5%
R634 100 5%
R527 100 5% FPGA_VN 26
R528 100 5% FPGA_VP 26
C799 10000PF 10% 50V X7R
C798 10000PF 10% 50V X7R
VREF
AVSS
U1
RSVD0 RSVD1
RSVD
FF1759
FPGA_3V3
R532 4.7K 5%
25,26 PROG
SW8 TL1015BF160QG
FPGA_3V3
R538 330 5%
R539 1K 5%
LED_GREEN DS13
25,26 DONE
Q1 NDS331N
FPGA_3V3
R541 4.7K 5%
R540 1K 5%
LED_GREEN DS14
25,26 INIT
Q2 NDS331N
HITECH GLOBAL
TITLE
V5TXT-PCIE
RS232, MICTOR, MISC
SIZE C
DWG NO HTG-V5-PCIE
REV 4.0
DRAWN BY S.S
SCALE
SHEET 26 of 32
6-24-2010_20:53
CONFIDENTIAL

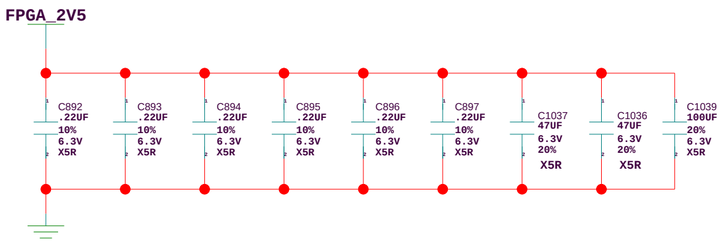


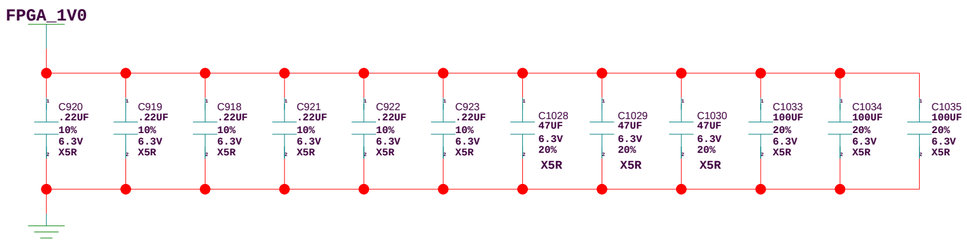


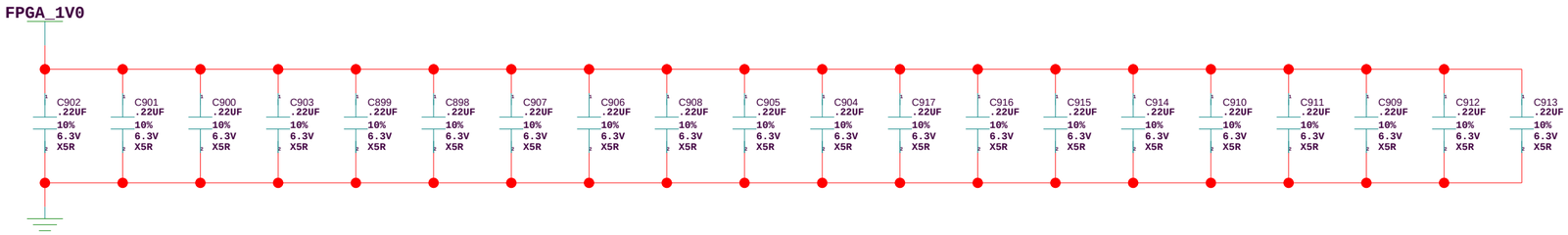












CONFIDENTIAL

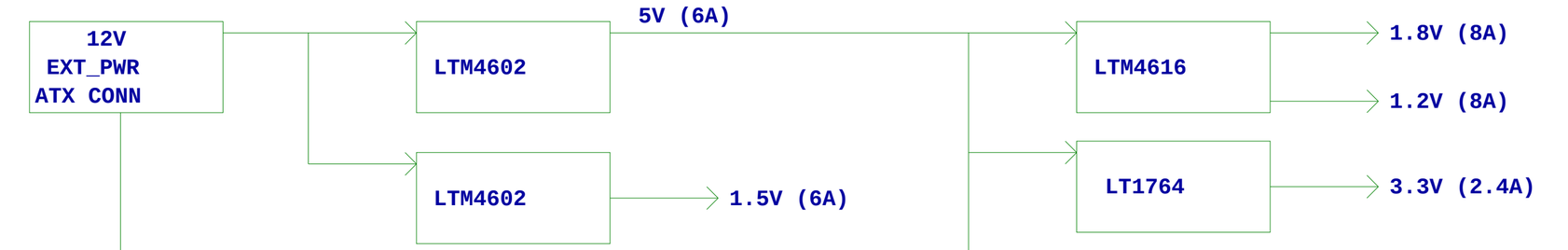
HITECH GLOBAL

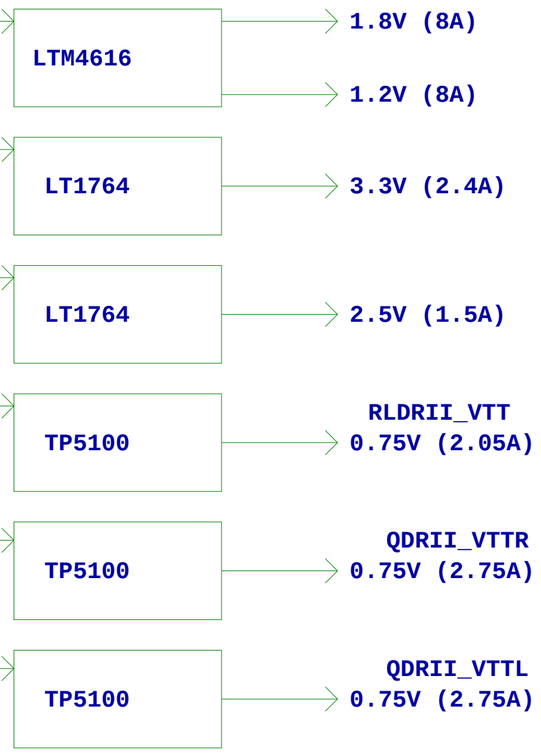
TITLE
V5TXT-PCIE
FPGA POWER AND BYPASS

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	of	
S.S		27	32	6-24-2010_20:53

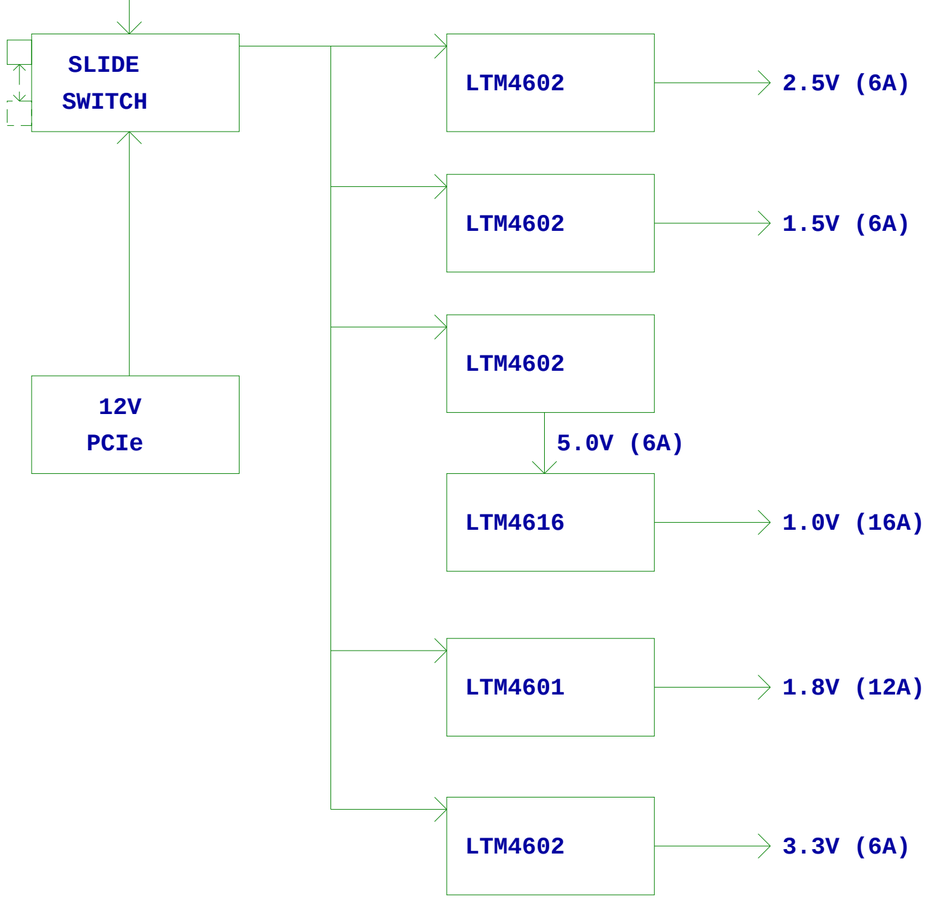
12V EXTERNAL POWER SUPPLY
FEEDS: QDRII, RLDRAM, AEL2005, OTHER DEVICES



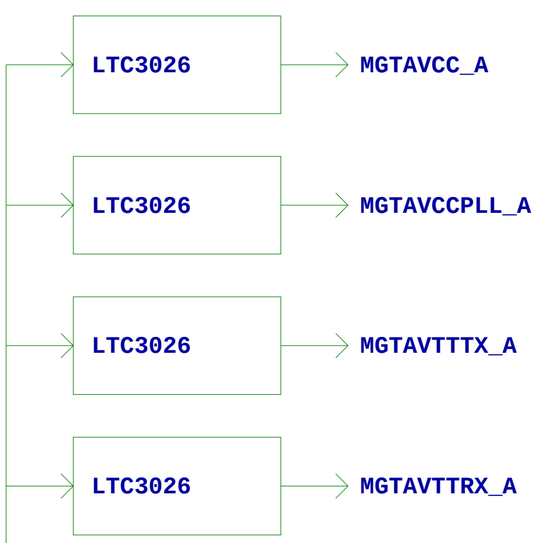


NOTE:
SLIDE SWITCH CONTROLS POWER TO
FPGA, CPLD, AND XL DEVICE EITHER
FROM ATX OR PCIe CONNECTOR

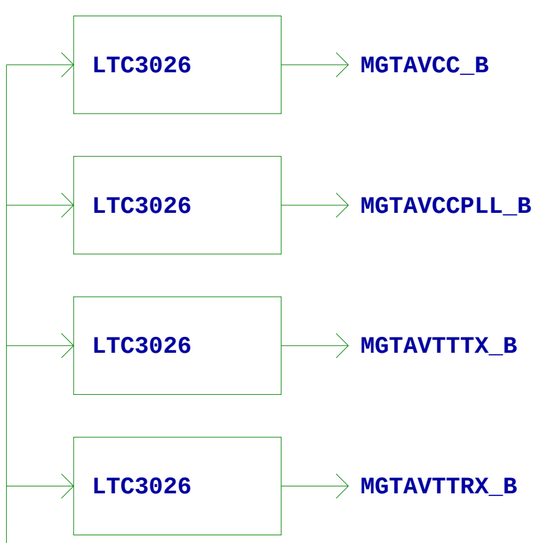
12V PCIe POWER SUPPLY (50W)
FEEDS: FPGA, CPLD, XL



POWER ALL EVEN GTX BANKS
LEFT COLUMN



POWER ALL ODD GTX BANKS
RIGHT COLUMN



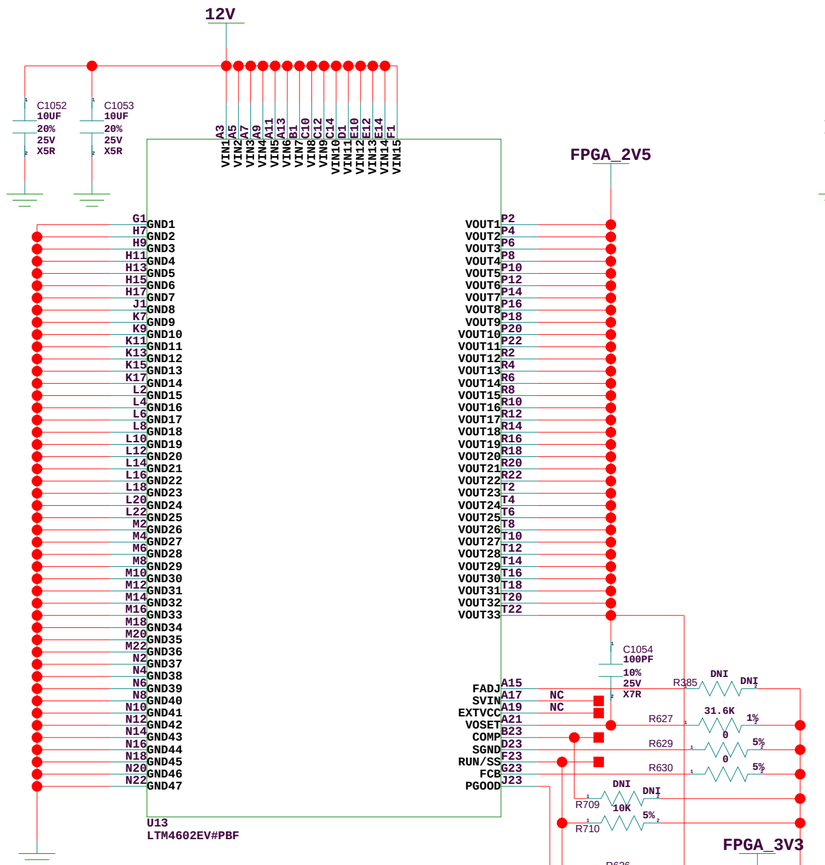
CONFIDENTIAL

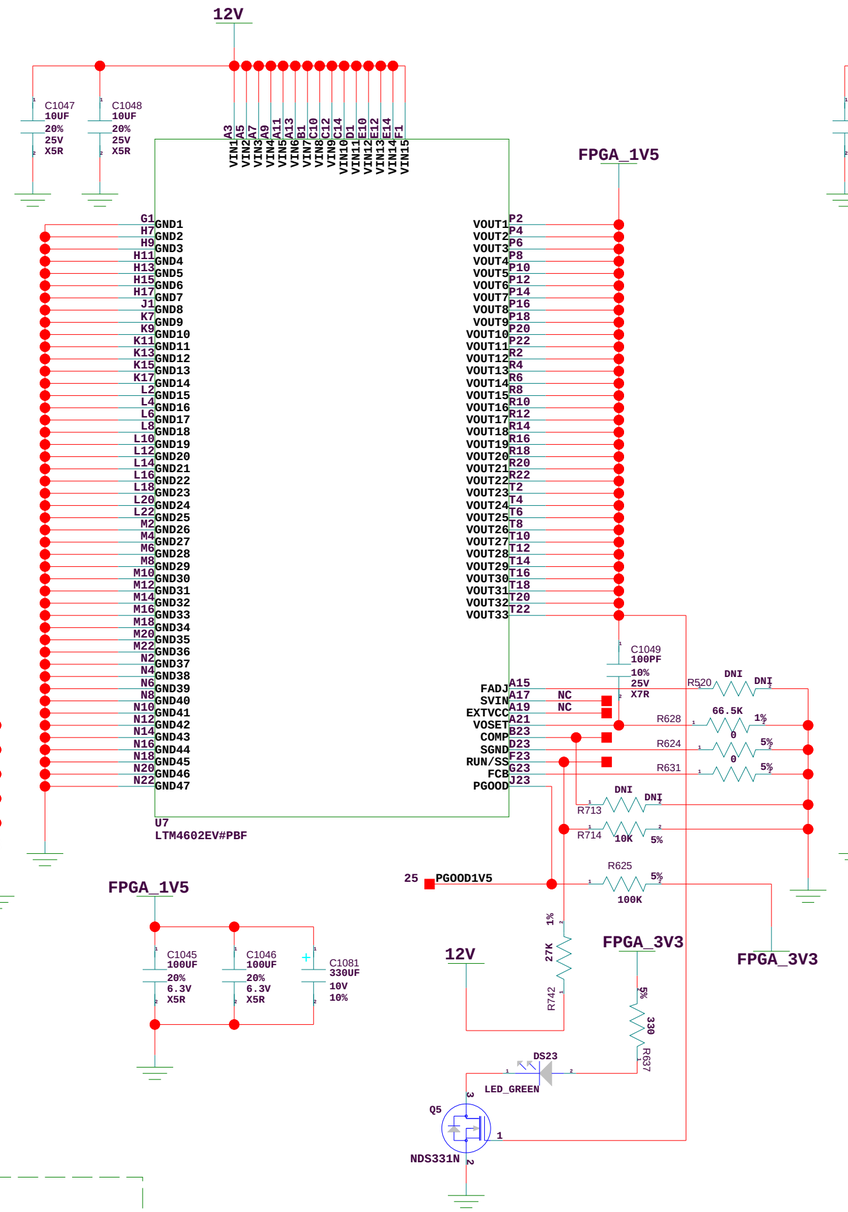
HITECH GLOBAL

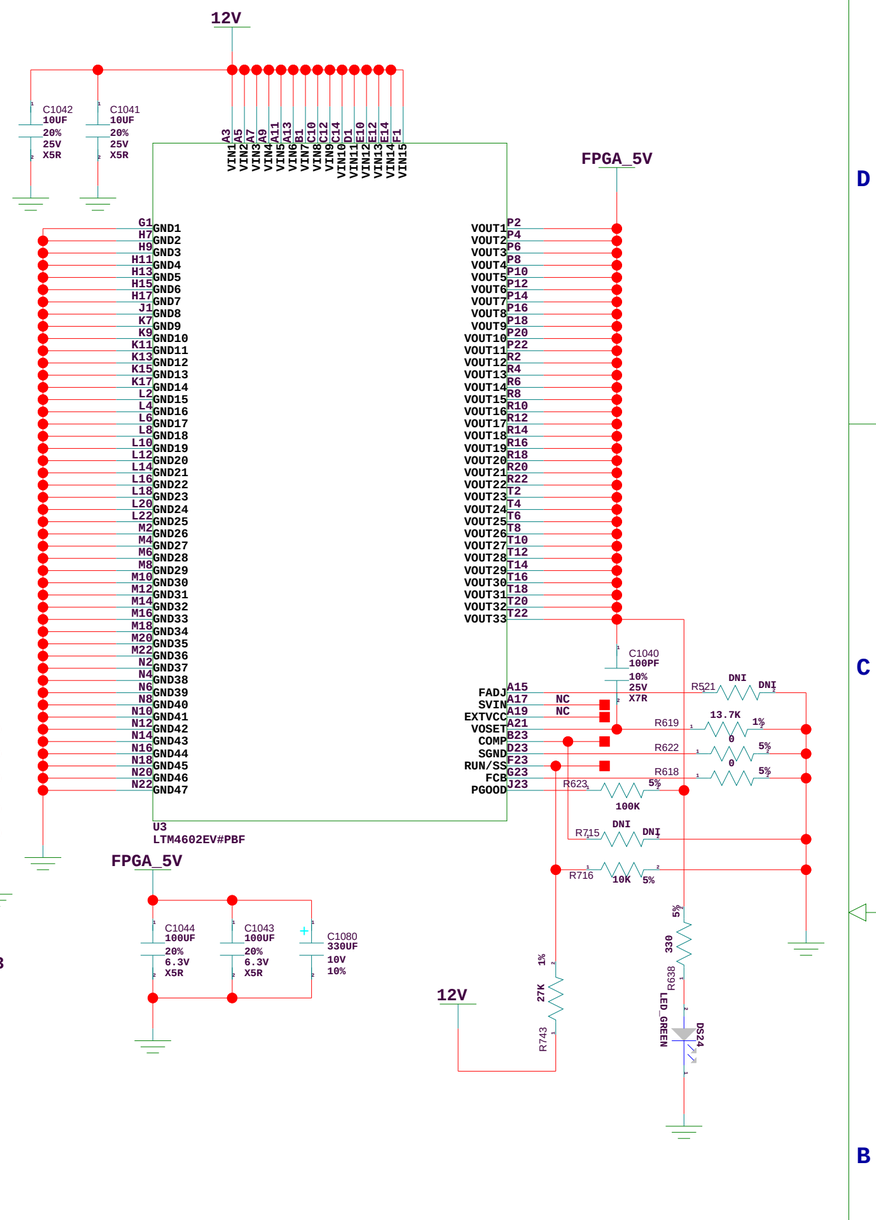
TITLE
V5TXT-PCIE
POWER BLOCK DIAGRAM

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		28 of 32	6-24-2010_20:53

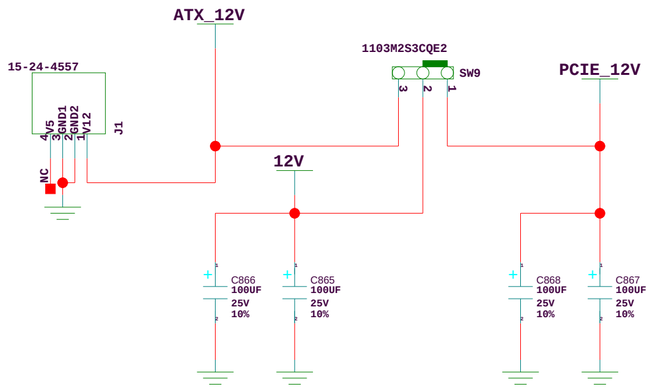






NOTE:

SWITCH CONTROLS POWER EITHER FROM PCIe OR FROM ATX CONNECTOR



CONFIDENTIAL

HITECH GLOBAL

TITLE

V5TXT-PCIE

5V, FPGA 2V5 AND FPGA 1V POWER SUPPLIES

SIZE	DWG NO	REV
C	HTG-V5-PCIE	4.0

DRAWN BY	SCALE	SHEET	
S.S		29 of 32	6-24-2010_20:53

RSET serves as a place holder

U44 LTM4616EV#PBF

U14 LTM4602EV#PBF

U21 LTM4601EV#PBF

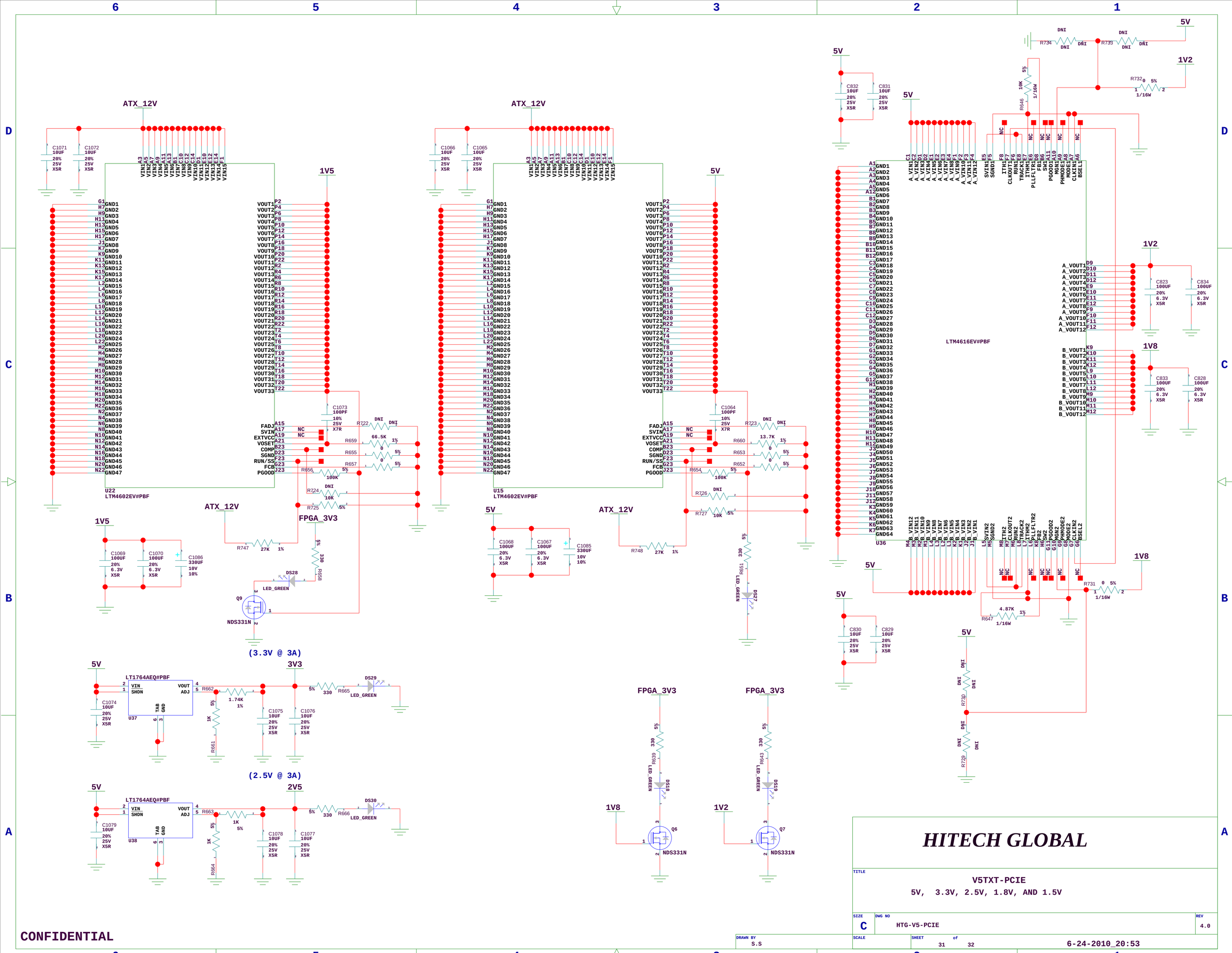
Q4 NDS331N

Q8 NDS331N

CONFIDENTIAL

TITLE	V5TXT-PCIE FPGA 3V3, 1V8, 1V0 POWER SUPPLIES
SIZE	C
DWG NO	HTG-V5-PCIE
REV	4.0
DRAWN BY	S.S
SCALE	
SHEET	30 of 32
	6-24-2010_20:53

HITECH GLOBAL


ATX_12V
U22
LTM4602EV#PBF
1V5
C1071 10UF 20% 25V X5R
C1072 10UF 20% 25V X5R
C1073 100PF 10% 25V X7R
R722 DNI DNI
R659 66.5K 1%
R655 0 5%
R657 5%
R656 100K 5%
R724 DNI
R725 10K 5%
FPGA_3V3
R747 27K 1%
R658 330 5%
DS28 LED_GREEN
Q9 NDS331N
C1069 100UF 20% 6.3V X5R
C1070 100UF 20% 6.3V X5R
C1086 330UF 10V 10%
(3.3V @ 3A)
LT1764AEQ#PBF
U37
5V
3V3
C1074 10UF 20% 25V X5R
R662 1.74K 1%
R661 1K 5%
C1075 10UF 20% 25V X5R
C1076 10UF 20% 25V X5R
R665 330 5%
DS29 LED_GREEN
(2.5V @ 3A)
U38
2V5
C1079 10UF 20% 25V X5R
R663 1K 5%
R664 1K 5%
C1078 10UF 20% 25V X5R
C1077 10UF 20% 25V X5R
R666 330 5%
DS30 LED_GREEN
ATX_12V
U15
LTM4602EV#PBF
1V5
C1066 10UF 20% 25V X5R
C1065 10UF 20% 25V X5R
C1064 100PF 10% 25V X7R
R723 DNI DNI
R660 13.7K 1%
R653 0 5%
R652 5%
R654 100K 5%
R726 DNI
R727 10K 5%
FPGA_3V3
R748 27K 1%
R651 330 5%
DS27 LED_GREEN
C1068 100UF 20% 6.3V X5R
C1067 100UF 20% 6.3V X5R
C1085 330UF 10V 10%
FPGA_3V3
R639 330 5%
DS18 LED_GREEN
Q6 NDS331N
R643 330 5%
DS19 LED_GREEN
Q7 NDS331N
5V
C832 10UF 20% 25V X5R
C831 10UF 20% 25V X5R
R734 DNI DNI
R733 DNI DNI
1V2
R732 0 5% 1/16W
R646 10K 5% 1/16W
LTM4616EV#PBF
A_VOUT1 A_VOUT2 A_VOUT3 A_VOUT4 A_VOUT5 A_VOUT6 A_VOUT7 A_VOUT8 A_VOUT9 A_VOUT10 A_VOUT11 A_VOUT12
C823 100UF 20% 6.3V X5R
C834 100UF 20% 6.3V X5R
1V8
B_VOUT1 B_VOUT2 B_VOUT3 B_VOUT4 B_VOUT5 B_VOUT6 B_VOUT7 B_VOUT8 B_VOUT9 B_VOUT10 B_VOUT11 B_VOUT12
C833 100UF 20% 6.3V X5R
C828 100UF 20% 6.3V X5R
U36
C830 10UF 20% 25V X5R
C829 10UF 20% 25V X5R
R647 4.87K 1% 1/16W
R731 0 5% 1/16W
R730 DNI DNI
R729 DNI DNI
CONFIDENTIAL
HITECH GLOBAL
TITLE
V5TXT-PCIE
5V, 3.3V, 2.5V, 1.8V, AND 1.5V
SIZE C
DWG NO HTG-V5-PCIE
REV 4.0
DRAWN BY S.S
SCALE
SHEET 31 of 32
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