

# SIGCOMM'16 Travel Grant Application Letter

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2nd year Ph.D. student • Joint Ph.D. program with USTC and MSRA

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### Personal Info

**Country:** P.R. China.

**Academic status:** Ph.D. Student.

**GeoDiversity:** I think I'm qualified for GeoDiversity travel grant, because I'm the 4th first author in mainland China that have published a paper in SIGCOMM.

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### Paper

**Author:** I'm the first author of paper *ClickNP: Highly Flexible and High-performance Network Processing with Reconfigurable Hardware* accepted to SIGCOMM'16.

**SRC:** I will participate in the ACM Student Research Competition (SRC).

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### Ph.D. Program

I'm in a joint Ph.D. program with University of Science and Technology of China (USTC) and Microsoft Research Asia (MSRA), advised by [Dr. Kun Tan](#).

My position at MSRA is a research intern and MSRA cannot cover travel expense for interns. My home institution, USTC, can cover travel expense up to 10,000 RMB (1,500 USD) per each Ph.D. student. However, as we will show later, this is insufficient to cover all costs.

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### Research Interest

**Data center networking:** Network function virtualization, Network programming.

**Reconfigurable hardware:** High level synthesis, Heterogeneous computing.

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### Research Summary and Plan

Highly flexible network functions are critical components to enable multi-tenancy in cloud environments. ASICs and network processors provide the best performance, but not flexible enough to implement novel network functions. CPUs and GPUs are highly programmable, but inefficient in terms of power, throughput and latency. Reconfigurable hardwares, namely FPGA, are architectures between the two extremes above. Modern FPGAs have millions of reconfigurable logic gates, hundreds Kbit registers, thousands of memory blocks, and in theory, each of them can work in parallel. The massive parallelism enables FPGA to outperform CPU and GPU at a clock frequency that is an order of magnitude lower.

However, FPGAs are historically expensive due to its small user base, and programmed with hardware description languages (HDLs) with low abstraction level and high programming complexity. Fortunately, both problems are being resolved in the last few years. First, FPGAs are being deployed at scale in datacenters and becoming inexpensive. Second, high-level synthesis (HLS) tools have been developed to convert a program in high-level language into HDLs.

ClickNP is the first FPGA-accelerated packet processing platform for general network functions, written completely in high-level language and achieving 40Gbps line rate. However, ClickNP is far from perfect and should be merely a starting point.

1. Programming in ClickNP is far more restrictive than on CPU. We need to carefully write code in a subset of OpenCL and give optimization hints to the compiler in order to exploit parallelism and generate efficient hardware. Higher-level programming abstractions and automated optimizations can be future works.
  2. FPGA is inefficient for tasks with low parallelism or high memory footprint, and it has limited area to hold logic. It is natural to ask whether there is a principled way to split a task on CPU and FPGA, given target throughput, resource constraints and communication cost. We will also rethink the role of FPGA as merely co-processor and build heterogeneous computing platforms making the most of CPUs and FPGAs.
  3. The massive parallelism makes FPGA a compelling platform for general computing acceleration. The accurate clocking makes FPGA irreplaceable for low latency general computing. We plan to extend the boundary of reconfigurable hardware by applying FPGAs to more areas, including but not limited to networking, crypto, distributed computing and machine learning.
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## Why Attend SIGCOMM

At the SIGCOMM conference, I plan to:

1. Present the paper in main conference.
2. Show a demo of ClickNP applications. (1) An Open vSwitch that supports L2 network virtualization with NVGRE. Additionally, the switch supports packet classification for firewall and strict priority queue for scheduling. (2) A stateful L4 load balancer that supports up to 32M concurrent flows and can accept 10M new flows per second. (3) As a final demo, we show that ClickNP is rather a general computing platform. We show a face detector in live video stream with convolutional neural network (CNN).
3. Search for opportunity to collaborate with the community and release ClickNP as a software that can integrate with an open network processing platform. ClickNP is a platform that may be useful to the network research community.

To me, it is the first time to submit a paper and attend an international conference. I'm really honored that my first paper gets accepted to the prestigious SIGCOMM conference. I treasure this opportunity very much as it will broaden my view, as well as giving me a chance to get in touch with worldwide researchers and collaborate on my future research.

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## Cost Estimate

**Conference Registration:** 300 USD.

**Air Ticket:**  $\approx$  1,500 USD. [Reference Link](#)

**Train Ticket within China:**  $\approx$  150 USD.

**Accommodation:**  $\approx$  300 USD for 6 days. [Reference Link](#)

**Brazil Visa Application:** 120 USD. [Reference Link](#)

**France Transit Visa Application:** 60 EUR. [Reference Link](#)

**Total Cost:**  $\approx$  2,440 USD.

**Travel Grant from Home Institution:** 10,000 RMB (1,500 USD). China is a developing country and my home institution, USTC, is in a relatively poor city (Hefei). USTC has limited travel grant for Ph.D. students to attend international conferences. Microsoft Research does not provide travel grant for interns.

**Cost Shortage:** 2,440 USD – 1,500 USD = 940 USD.

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## Thanks

I understand that preference will be given to applicants that do not present a paper in the conference. But China is really far from Brazil and the air ticket is expensive. Furthermore, my home institution does not have enough budget to cover full travel expense. I really appreciate if you could give me funding to attend the SIGCOMM conference. Thanks!