

Shreeyash Pandey

Systems Software Developer

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<https://fp32.org>

EXPERIENCE

• Vicharak

Systems Software Developer, Full-time

Surat, India

August 2023 – August 2025

Gati Project - Edge ML Accelerator

- Architected an FPGA based edge-ML accelerator for, and designed hardware building blocks (e.g., im2col, systolic arrays).
- Developed cycle-accurate simulators for architectural verification, performance profiling, and design tradeoff analysis.
- Designed and implemented a dataflow compiler, integrating graph-level (layer fusion, tiling) and ISA-specific hardware optimizations to achieve real-time (20-30fps) inference of image recognition and object detection workloads on low-power edge device.
- Engineered a dynamic hardware generator to create model-specific, optimized FPGA configurations for increased inference efficiency.
- Developed a high-throughput runtime engine for edge deployment, including optimized NEON kernel development for ARM processors.

FPGA EDA Compiler Reverse Engineering

- Reverse Engineered the Intermediate Representation used by FPGA Compiler of a proprietary toolchain
- Added support for it in the Open Source synthesis software: Yosys

Binary Neural Networks on FPGA

- Investigated hyper-quantized (Binary, Ternary) neural networks for their efficacy to be deployed on FPGAs
- Ported existing binary networks to validate performance and understand bottlenecks
- Modelled novel architectures of binarized neural nets in PyTorch

• Vicharak

Linux Kernel Developer, Intern

Surat, India

January 2023 – August 2023

- Port Tianocore EDK2 to ARM Cortex-A series proprietary chip
- Configure and Compile the Linux Kernel for various target architectures like x86 and ARM.
- Understand and Implement UEFI/PI specification to bring-up incompatible boards and allow a greater range of kernels to boot.
- Inspect relevant firmwares with tools like Ghidra to find and debug problems.

TALKS

• No-ISA is the Best ISA - Shreeyash Pandey, Rishik Ram

<http://tiny.cc/e6dp001>

IICT 2024, Bangalore

EDUCATION

• G.H. Raisoni Institute Of Engineering And Technology

Bachelor of Engineering in Computer Science Engineering; CGPA: 8.5

Nagpur, India

August 2019 – May 2023

PROJECTS

• TinyTapeout

June 2025 – Present

- Part of the team working on getting a RISC-V chip with CORDIC extensions to tapeout on the TinyTapeout project
- Responsibilities include extending TableGen and adding support for new instructions in the LLVM RISC-V backend
- Verifying correctness by running the flow on the chip prototype running on the FPGA.

• Clogwave - debug complex C code like verilog

LLVM, C++

<https://github.com/bojle/clogwave>

December. 2023 – Present

- Implemented an LLVM pass that instruments C code with VCD dumping callbacks that when the program is run, generates a VCD dump and can be viewed in tools like gtkwave.
- Waveform view of sequential code allows interdependent variables to be analysed wrt to other variables.

- **Evofox-phantom**

Python, libUSB, libHID, Wireshark

<https://github.com/bojle/evofox-phantom>

February. 2022 – May 2022

- Reverse engineered the communication protocol of a gaming mouse with Wireshark
- Devised a python program to emulate the behavior of a proprietary hardware device.
- A video demo of the project can be found here: <https://youtu.be/1RXHDZS5G4I>

TECHNICAL SKILLS

- **Programming Languages:** C, C++, Bash (Shell Scripting), Python, UV, x86 Assembly, ARM Assembly, RISC-V, Verilog
- **Frameworks and Libraries:** PyTorch, Onnxruntime, Tensorflow, Tinygrad, CUDA, TensorRT, LLVM, ONNX, Protobufs
- **Documentation:** Writing technical documentation and tools for it such as: Markdown, RST, Sphinx
- **Tools:** Git, Make, CMake, GDB, Valgrind, Compiler Explorer
- **Operating Systems and ISAs:** Linux, Windows, ARM, x86, 6502