CS 2110 — Quiz 3 (35 minutes)
October 3rd, 2018

Full name: _____

GT username: _____

This quiz is worth a total of **100 points**.

In accordance with the Georgia Institute of Technology Honor Code, I have neither given nor received aid on this quiz.

Signature: _____

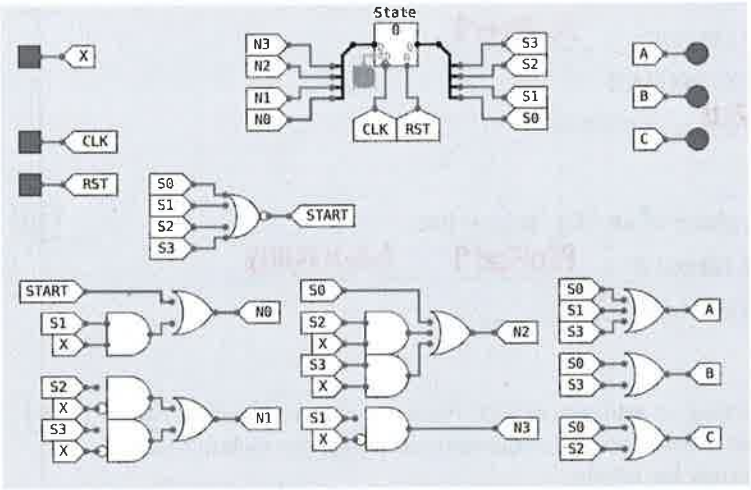
Please make sure all of your answers are contained within the answer boxes or the fill-in lines.

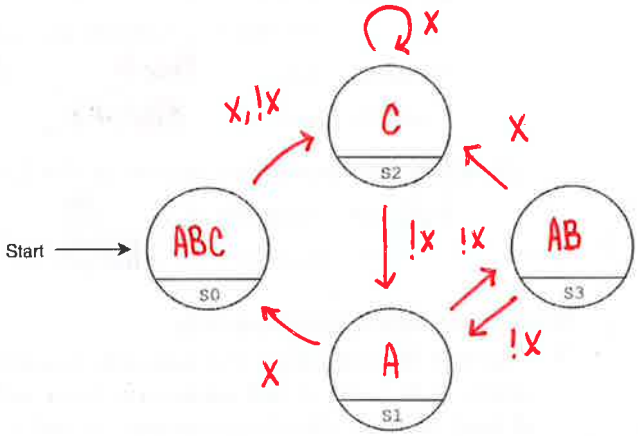
You have been provided with scratch paper for your work. You will **NOT** be given credit for showing work. Having anything except the answer inside the boxes or above the fill-in lines might cause incorrect results.

Write your name and answers legibly. You will not receive credit for illegible answers.

State Machines

1. Consider the following one-hot state machine circuit. The current state of the machine is represented by four bits, $S_3S_2S_1S_0$. The next state of the machine is represented by four bits, $N_3N_2N_1N_0$. There is one input $\{X\}$ and three outputs $\{A, B, C\}$. Annotate the diagram (on the right) with appropriate arrows for transitions and letters for outputs. **You must explicitly draw every possible transition.** [20]





Karnaugh Maps

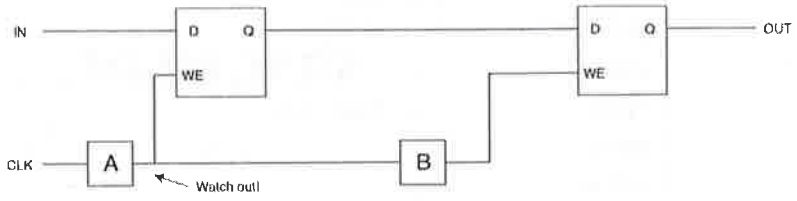
2. Consider the following simplified boolean expression and fill-in cells of the corresponding Karnaugh map with either 0s or 1s. [16]

Expression: $BD + \overline{A}D + \overline{A}BC$

AB \ CD	11	10	00	01
11	1	0	0	1
10	0	0	0	0
00	1	0	0	1
01	1	1	0	1

Sequential Logic: Edge-Triggered Components

3. Consider the following edge-triggered component composed of two *positive level-triggered* D latches. `OUT` should only change when `CLK` is moving from low to high, i.e. *positive edge-triggered*. [10]



Which component for box A?:

○ Wire ● NOT

Which component for box B?:

○ Wire ● NOT

Short Answer

4. For the following questions please answer in the space provided.

   (a) What is the largest positive number (in **decimal**) we can represent literally (i.e. as an immediate value) within an LC-3 `AND` instruction? [5]

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   (b) Consider a machine with memory addresses `0x0000` to `0x07FF` where the largest decimal integer that can be read or written is `127` and the smallest is `-128`. Integers are stored with **two's complement**. [5]

   What is the address space? 2^{11}

   What is the addressability? 8

LC-3 Datapath

5. The Fetch and Decode instruction phases have been completed. Consider the Execute phase for the following instructions. *Note:* Please use the signal name terminology indicated on your reference sheet.

   (a) Fill-in the appropriate signals for the Execute phase of an `ST` instruction: [10]

   Cycle 1: ADDR1MUX = PC; ADDR2MUX = PCoffset9;
   MARMUX = ADDER; gateMARMUX; LD.MAR

   Cycle 2: ALUK = PassA; GateALU; LD.MDR

   Cycle 3: MEM.EN; MEM.WE

   (b) Fill-in the appropriate signals for the Execute phase of an `LEA` instruction: [10]

   Cycle 1: ADDR1MUX = PC; ADDR2MUX = PCoffset9; GateMARMUX;
   MARMUX = ADDER; LD.REG; LD. CC

LC-3 Instruction Dissassembly

6. Consider the following LC-3 assembly program, starting at address `x3000`. Notice we have specified the addresses in memory and contents at those addresses. There are also comments detailing the instructions at each address, where appropriate, as well as a column for labels. [24]

   Please appropriately fill in each empty entry (notice there are **six** lines) in the "Contents" and "Instruction" columns. **Indicate the appropriate label, not the offset.**

Label	Address	Contents	Instruction
	x3000	x5020	;; AND R0, R0, #0
	x3001	x220D	;; LD R1, ADDR_STR
	x3002	xA40B	;; LDI R2, ADDR_CHR
	x3003	x94BF	;; NOT R2, R2
	x3004	x14A1	;; ADD R2, R2, #1
LOOP	x3005	x6640	;; LDR R3, R1, #0
	x3006	x0405	;; BRZ DONE
	x3007	x16C2	;; ADD R3, R3, R2
	x3008	x0A01	;; BRNP SKIP
	x3009	x1021	;; ADD R0, R0, #1
SKIP	x300A	x1261	;; ADD R1, R1, #1
	x300B	x0FF9	;; BR LOOP
DONE	x300C	xB003	;; STI R0, ADDR_CNT
	x300D	xF025	;; TRAP x25
ADDR_CHR	x300E	x4050	;;
ADDR_STR	x300F	x4800	;;
ADDR_CNT	x3010	x5000	;;