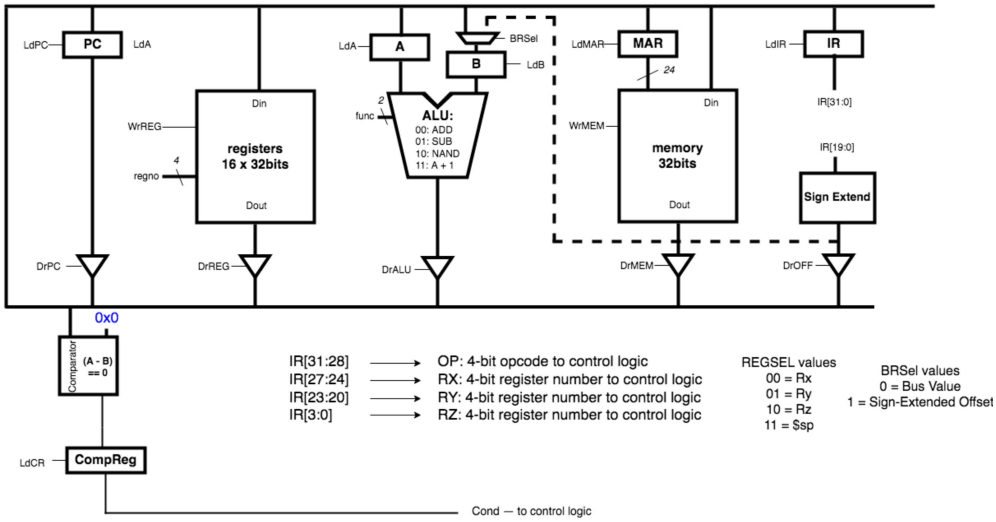
CS 2200 Homework 3
Spring 2019

Rules:

- Please print a copy of the assignment and hand write your answers. No electronic submissions are allowed. **Please print as one double-sided page. Do NOT staple multiple sheets together.** There will be a **30** point penalty if you do not.
- This is an individual assignment. You may discuss concepts but not the answers.
- Due Date: **6th February 2019 – 6:15 PM**. Bring your BuzzCard. Show up on time.

Name:_____ **GT Username:**_____ **Section:**_____

LC-5000 Datapath



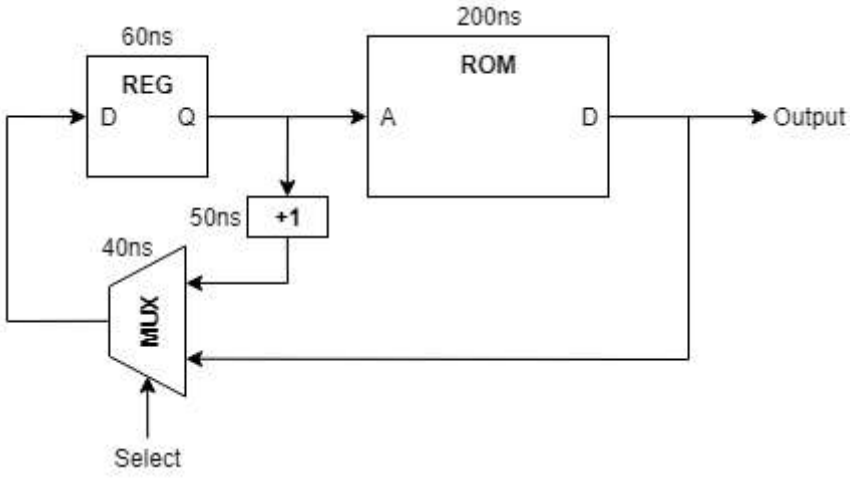
The above is the datapath of the **LC-5000**, a modified version of LC-2200. **Notice the extra MUX in front of the ALU "B" register.**

1. Write out the microstates for a more efficient **JALR** and **SW** using the modifications on the LC-5000 datapath. For each microstate, give the control signals used (see the example). Signals irrelevant to the state can be omitted and will be assumed to be zero. **You will lose points for an inefficient answer!**

ADD (example)	**JALR**	**SW**
ADD0: DrREG, LdA, RegSel=01 **ADD1:** DrREG, LdB, RegSel=10 **ADD2:** DrALU, WrReg, func=00, RegSel=00		

2. Normally, every microstate has a static “next state” field which indicates which state it will enter next. However, in the **LC-2200**, there are some situations where this is not the case, and the “next state” associated with the state is not enough information to determine the next state. Name **two** of these cases and what extra information they need to determine the next microstate (refer to chapter 2/3):

3. The following circuit implements a finite state machine using an asynchronous ROM and a synchronous state register. Based on the input to the circuit, the next state can be either the incremented value of the state register, or come from the ROM.



Calculate the maximum clock frequency allowed for this circuit assuming the following parameters:

- The propagation time of wires is negligible
- The Select input changes only on a clock edge
- The input of the register must be stable for **60ns** to be latched
- The address input of the ROM must be stable for **200ns** to produce the new output
- The input of the incrementer must be stable for **50ns** to produce the new output
- The inputs to the multiplexer must be stable for **40ns** to produce the new output

Show your work.

Maximum Frequency (MHz): _____