CS 2200 Homework 5

Spring 2019

- Please print a copy of the assignment and hand write your answers. No electronic submissions are allowed. **Please print as one double-sided page. Do NOT staple multiple sheets together. There will be a 50 point penalty if you do this improperly.**
- This is an individual assignment. You may discuss concepts but not the answers.
- Due Date: **20th February 2019 – 6:15 PM** in recitation. Bring your BuzzCard. Show up on time.

Name:_____ **GT Username:**_____ **Section:**_____

1. Branching instructions like BLT and BEQ occur quite often in assembly code. Let's say that an engineer proposes to improve the BLT and BEQ instructions such that it takes one-fourth time to execute, and BLT and BEQ instructions makes up 25% of the total instructions. If a program takes 120 ns to execute before the improvement, find:
    a. Time taken to execute the program after the improvement.

    b. Speedup achieved by the improvement.

2. Consider the table below. You find some way to reduce the CPI of Type B instructions to 5, but have to increase the cycle time. What is the maximum increase(in %age) in the cycle time that makes this change beneficial?

Instruction type	Cycles	Frequency in program
A	4	30%
B	7	30%
C	10	40%

3. Consider the pipelined LC-2200 architecture as described in the textbook. Suppose we want to implement the following RAMA-2200 instruction: **`LEA  DR, PCoffset20.`**
What are the **minimum** contents that must be placed in each pipeline buffer in order to support this instruction? **Write each value and its corresponding number of bits in parenthesis.**

FBUF	DBUF	EBUF	MBUF
- Fetched Instruction (32 bits)			

4. Consider Instructions I_1 through I_3 below. Trace the passage of these instructions through the 5 stage pipeline described in the book in the table below. The first two clock cycles have been done for you. **Assume that data forwarding is not supported.**

```
I1 : nand   $t1, $t1 , $t1
I2 : addi   $t1, t1, 1
I3 : add    $v0, $a0, $t1
```

Clock Cycle	IF	ID/RR	EX	MEM	WB
1	I_1	-	-	-	-
2	I_2	I_1	-	-	-
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					