CS 2200 Fall 2018 Exam #2 (version A)

GT/Prism ID:_____

Name: KEY

Section	Points	Lost	Gained	Total	TA
Processor Scheduling	**13**				
Memory Management	**23**				
Demand Paging	**12**				
Caches	**25**				
Total	**73**				

- Note: By writing your name at the top of this test you are certifying that this test is entirely your own work.
- You may ask proctors for clarification but you are ultimately responsible for the answer you write on the paper.
- Illegible answers are wrong answers.
- Please look through the entire test before starting.

PLEASE WORK ON MATCHING PROBLEMS **LAST**!
Especially question 9.

Good luck!

Initials: _____

POWERS OF TWO

2^0	1
2^1	2
2^2	4
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^10	1024
2^11	2048
2^12	4096
2^13	8192
2^14	16384
2^15	32768
2^16	65536
2^17	131072
2^18	262144
2^19	524288
2^20	1048576
2^21	2097152
2^22	4194304
2^23	8388608
2^24	16777216
2^25	33554432
2^26	67108864
2^27	134217728
2^28	268435456
2^29	536870912
2^30	1073741824
2^31	2147483648
2^32	4294967296
2^33	8589934592
2^34	17179869184
2^35	34359738368
2^36	68719476736

Initials:_____

Processor Scheduling

1. (3 Points) Matching (Match the single best answer, Some terms may not be used)

C Convoy Effect	A. A term or abbreviation that has no actual meaning for Process Scheduling
E Starvation	B. A scheduling alogithm that determines the next process to run by the arrival time.
B Non-Preemptive FCFS	C. A phenomena where a single long running process can cause adverse performance by blocking shorter running processes.
F Non-Preemptive Priority	D. A scheduling algorithm that uses the shortest running time to determine which process gets to run.
D Non-Preemptive SJF	E. A phenomena where a process may never get to run because the scheduling algorithm always selects someone else to run.
A IO Block Delay	F. A scheduling algorithm that uses some measure of criticality to determine which process runs next.

2. (2 Points) A process control block (ignore threading concerns) contains (circle all that apply, minus for incorrect selections)

(a.) The program counter
(b.) The program-visible registers
c. The internal registers (A, B, MAR)
(d.) The process id
(e.) The current state of the process (running, waiting, etc.)
(f.) The address of the page table for the process (PTBR)

Initials: _____

3. (6 Points) Preemptive Round-Robin

Given the following 3 processes and their burst times (assume initially they are in the ready queue in this order (P1, P2, P3):

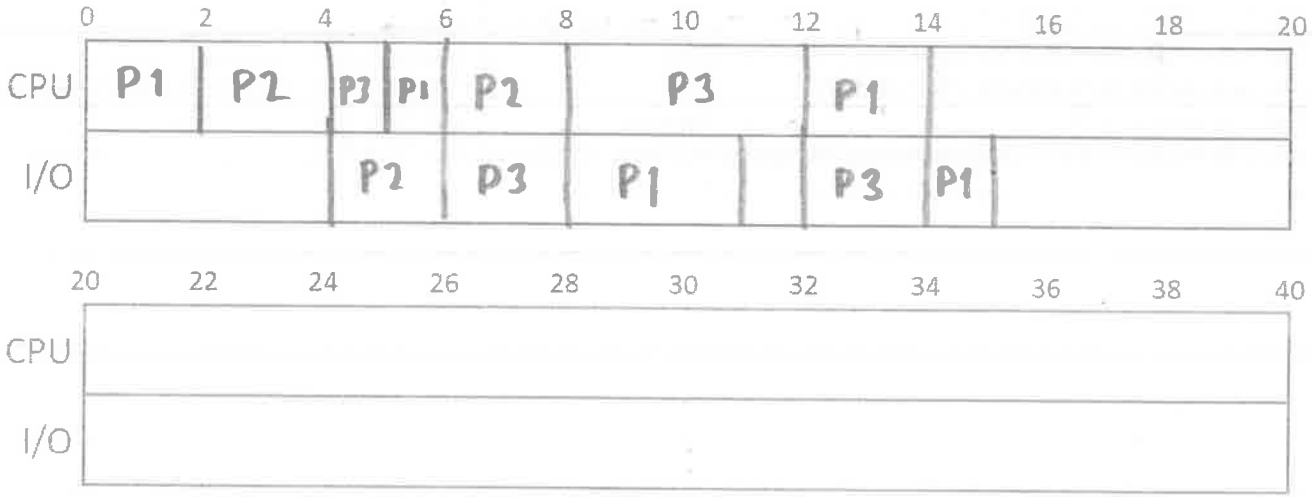
	CPU	IO	CPU	IO
P1	3	3	2	1
P2	2	2	2	done
P3	1	2	4	2

Time Quanta of OS for CPU: 2 IO is a FIFO queue not preempted.What is the response time and wait time for each of the processes (P1, P2, P3)?

Fill in answer in this table:

Process	Elapsed Time	Wait Time
P1	15	6
P2	8	2
P3	14	5

SHOW WORK BELOW IF YOU WANT ANY PARTIAL CREDIT!!!



Initials: _____

4. (2 Points) How is the timeslice (quanta) for the OS determined in preemptive scheduling?

a. Selected by the designer, but can really be anything reasonable
b. Dictated by the clock timing of the hardware pipeline
(c.) Tradeoff between apparent interactivity of processes and the context switch time
d. None of the above are true

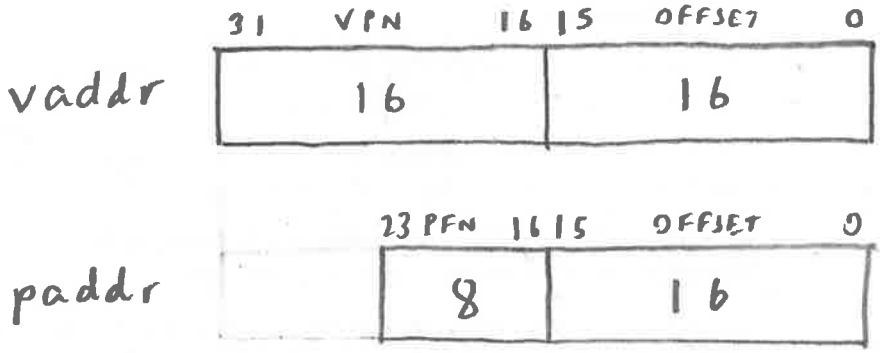
Memory Management

5. (2 Points) Paging is a modern memory management technique that eliminates both external and internal fragmentation.

a. True
(b.) False

6. Given a 32 bit address for Virtual Memory and a 24 bit address for Physical Memory and a 64K page size.

a. (6 Points) Show the translation for both a virtual and physical address. Be sure to indicate the size in bits of each part of the translation.



b. (2 Points) How many entries are in the page table?

64k

7. (2 Points) The translation look-aside buffer is:

a. A hardware cache used by the memory management unit to speed translation of VA to PA
b. A software structure used by the OS to speed translation between VA and PA
c. A mapping of VPN to PFN
(d.) Both a and c are true
e. None of the above are true

8. (2 Points) Which of the following must be true for demand paging to work?

EITHER (a.) The offsets of VA and PA must be identical
(b.) The page size must be identical for Virtual and Physical addresses
c. There must be the same number of VPN and PFN
d. The high-order six bits of the VA and PA must match.
e. The page table and the frame table must be the same size.

Initials: _____

9. (7 Points) Matching (select best answer, some answers may not be used)
DO THIS LAST IF THERE IS TIME!!

C Fence Register	A. The memory that the programmer visualizes is true, but that may not actually exist at runtime.
E External Fragmentation	B. Translating between the program addresses and actual addresses which occurs when the program is first loaded into memory.
G Coalescing	C. A historical memory management technique that supported a single process and allowed the kernel space to be protected.
H Bounds Registers	D. Dividing memory up into fixed sized chunks that can be assigned to a process. The sizes of the chunks are designed by the OS and do not change.
I Compile-Time Binding	E. Memory that is unusable because the chunk available is too small, but overall free memory is adequate.
B Load-Time Binding	F. The actual amount of memory you have installed on your motherboard.
M Run-Time Binding	G. Merging adjacent chunks of memory that are free so that you can get a bigger chunk for allocation.
A Virtual Memory	H. A historical memory management technique that provides each process with an upper and lower limit of fixed memory.
F Physical Memory	I. This situation occurs when the addresses used by the compiler are the actual physical addresses.
K Base + Limit Registers	J. The memory starts as one giant chunk and gets divided so that each process gets the exact amount it needs.
L Internal Fragmentation	K. A historical memory management technique that allows processes to be relocated in memory during execution.
N Compaction	L. The amount of memory that is unusable because the allocated amount to a process is slightly larger that what is required.
D Fixed Partitioning	M. Translating between the program and physical addresses occurs while the program is running, and may change during execution.
J Variable Partitioning	N. Moving processes around in memory to free up a larger amount of free memory.

Initials: _____

10. (2 Points) A page fault occurs when:

a. There is a TLB miss
b. The page table is not in the L1 cache
c. The valid bit in the page table is false for the requested page
d. There is a cache miss in the L3 cache which makes us go off-chip to main memory

DEMAND PAGING

11. Consider the following situation:

Page Table – Process: 123 (Partial)

	PFN	
~~V~~ I	54	0
V	32	1
V	89	2

Page Table – Process 345 (Partial)

	PFN	Index
V	66	12
V	82	13
~~V~~ V	~~32~~ 102	14
~~V~~ V	~~76~~ 54	15

Frame Table

PID	VPN	PFN
123	1	32
~~123~~ 345	~~X~~ 15	54
345	12	66
456	18	76
345	13	82
123	2	89
345	14	102

Free Frame List (1 entry) = 102 LRU indicates frame 54 is next selection.

a. (6 Points) Process 345 requests virtual page 14. Update the tables above to show the correct entries after this request is satisfied.

b. (6 Points) Process 345 requests virtual page 15. Update the tables above to show the correct entries after this request is satisfied.

Initials: _____

CACHING

12. (5 Points) Consider the following information:
Access time of L1 cache is 1 ns, Hit rate 95%.
Access time of TLB is 1 ns, Hit rate 98%.
Access time of the L2 cache is 6 ns, Hit rate 80%.
Access time of the L3 cache is 10 ns, Hit rate 70%.
Access time of main memory is 90 ns.
What is the average memory access time for this memory hierachy?
Put answers into this table:

Average Memory Access Time	1.8034
EMAT (TLB)	1.0334
EMAT (L1)	1.67
EMAT (L2)	13.4
EMAT (L3)	37

$EMAT(L3) = 10 + (1-.7)90 = 10 + 27 = 37$

$EMAT(L2) = 6 + (1-.8)37 = 6 + \frac{2}{10}37 = 6 + 7.4 = 13.4$

$EMAT(L1) = 1 + (1-.95)13.4 = 1 + \frac{1}{20}13.4 = 1 + .67 = 1.67$

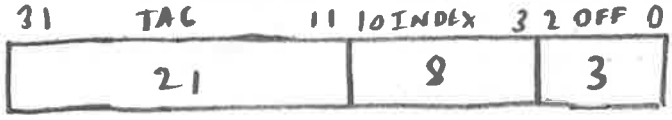
$EMAT(TLB) = 1 + (1-.98)1.67 = 1 + \frac{2}{100}1.67 = 1 + .0334 = 1.0334$

$AVG = TLB + L1 = 1.67 + 1.0334 = 1.8034$

Initials: _____

13. Consider the following design:
32 bit addresses, 32K 4-way set associative cache with 32 byte word addressable blocks. This is a write-through, write allocate cache.

a. (3 Points) Sketch the division of the address into its required component parts to access this cache.



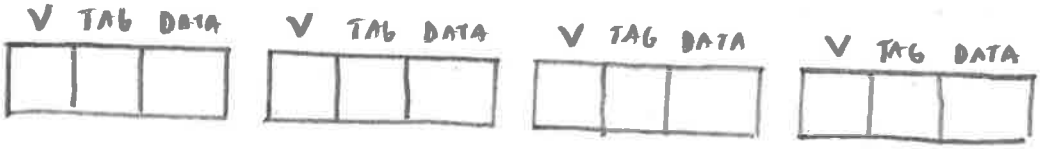
b. (2 Points) How many cache lines are there?

256

c. (2 Points) How many hardware comparators would be needed for this cache?

4

d. (4 Points) Draw a picture of one cache line showing the entries on each line and any required metadata associated with the entry.



Initials: _____

14. (9 Points) Consider a 2-way set associative cache with only 2 lines that uses a 1 bit LRU.

The cache is currently empty. You get the following sequence of addresses (shown as Tag, Index pairs):

(0,0), (0,1) , (1,0), (2,0), (1,1) , (0,1), (0,0) , (0,1), (0,0) TYPO

ACCEPTED BOTH ANSWERS

Fill in the table with the following information:
(Miss Types are: Compulsory, Conflict, Capacity, NA (Was a Hit))

Address	Miss Type
(0,0)	COMPULSORY
(0,1)	COMPULSORY
(1,0)	COMPULSORY
(2,0)	COMPULSORY
(1,1)	COMPULSORY
(0,1)	HIT
(0,0)	CAPACITY
(1,0)	HIT / CAPACITY
(0,0)	HIT

Initials: _____