## CS 2200 Homework 6

## Spring 2019

- Please print a copy of the assignment and hand write your answers. No electronic submissions
  are allowed. Please print as one double-sided page. Do NOT staple multiple sheets
  together. There will be a 60 point penalty if you do this improperly.
- This is an individual assignment. You may discuss concepts but not the answers.
- Due Date: 6th March 2019 6:15 PM in recitation. Bring your BuzzCard. Show up on time.

| Name: | GT Username: | Section: |
|-------|--------------|----------|
|       |              |          |

1. The RAMA-2200 processor uses a 5-stage pipeline of stages:

IF ID/RR EX MEM WE

You can assume the following about the processor:

- All registers are initialized to 0
- There is data forwarding from EX, MEM, and WB to ID/RR
- Branches are resolved in **EX**
- Branches are handled conservatively (Branch Not Taken)
- CPI = 1 in the event of no hazards

The assembly code in the diagram below is run to completion. Show the first 12 cycles of code execution with the following waterfall diagram. We have filled in the first instruction (A)'s path for you.

- **I1.** ADDI \$t0, \$t0, 1
- **I2.** ADDI \$t1, \$t1, 1
- **I3.** BEQ \$t1, \$t0, I2
- **I4**. LW \$t2, 0(\$s0)
- **I5.** NAND \$s1, \$t2, \$t2
- **I6.** HALT

| Cycle | IF         | ID/RR      | EX         | MEM | WB |
|-------|------------|------------|------------|-----|----|
| 0     | I1         |            |            |     |    |
| 1     | l2         | I1         |            |     |    |
| 2     | l3         | <b>I</b> 2 | <b>I</b> 1 |     |    |
| 3     | <b>I</b> 4 | <b>I</b> 3 | <b>I</b> 2 | I1  |    |
| 4     | <b>I</b> 4 | NOP        | I3         | I2  | I1 |
| 5     |            |            |            |     |    |
| 6     |            |            |            |     |    |
| 7     |            |            |            |     |    |
| 8     |            |            |            |     |    |
| 9     |            |            |            |     |    |
| 10    |            |            |            |     |    |
| 11    |            |            |            |     |    |

a. Fill in the table below with the number of NOPs (bubbles) each situation will produce. In the case of the RAW hazard, assume that there are no other instructions in between the write instruction and read instruction.

|                                     | No data forwarding             | Data forwarding            |
|-------------------------------------|--------------------------------|----------------------------|
| RAW Hazard                          |                                |                            |
| Load-to-Use RAW Hazard              |                                |                            |
|                                     | When the branch does not occur | When the branch does occur |
| Conservative Branching              |                                |                            |
| Branching with Branch<br>Prediction |                                |                            |

b. Explain how you calculated the number of NOPs produced by a load instruction with data forwarding in the previous question.

3. For each instruction below, state what type of hazard(Structural, Data, or Control) the instruction can cause, if any. If the instruction causes a data hazard, then state what type of data hazard it is.

|                                  | Class of Hazard (If any) | Type of Data Hazard (If applicable) |
|----------------------------------|--------------------------|-------------------------------------|
| <b>I1</b> . ADDI \$t0, \$t0, 1   |                          |                                     |
| <b>I2.</b> ADDI \$t1, \$t0, 1    |                          |                                     |
| <b>I3.</b> NAND \$t1, \$t1, \$t1 |                          |                                     |
| <b>I4.</b> BLT \$t0, \$t1, END   |                          |                                     |

3. When we consider branch prediction, why is flushing necessary? What may happen if we do not implement flushing?

4. What is the branch target buffer? How does it help us, and what does it store?