CS 2200 Homework 9

Spring 2019

Instructions:

- Please print a copy of the assignment and hand write your answers. No electronic submissions are allowed. **Please print as one double-sided page. Do NOT staple multiple sheets together. There will be a 90 point penalty if you do not.**
- This is an individual assignment. You may discuss concepts but not the answers.
- Due Date: **04/03/19 – 6:00 PM** in recitation. Bring your BuzzCard. Show up on time.

Name:_____ **GT Username:**_____ **Section:**_____

1. Average Access Time

Say we have two setups for hierarchical memory with the following miss rates and hit times:

Memory 1

Hardware	Miss Rate	Hit Time
L1 Cache	0.05	10ns
L2 Cache	0.2	15ns
Main Memory	0	80ns

Memory 2

Hardware	Miss Rate	Hit Time
L1 Cache	0.15	2ns
L2 Cache	0.5	8ns
Main Memory	0	65ns

a. Compute the AAT (average access time) for each setup. Show your work below.

Memory 1 AAT = _____

Memory 2 AAT = _____

b. Which setup would you choose? Explain why. **Memory 1** **Memory 2**

2. Cache Addressing

Draw the layout of how this cache will interpret an address using the figure below as a guide. Label all parts of the address and their respective sizes. Use the following cache parameters to answer the question:

- 32 bit address
- cache size of 256K words (1024 KB)
- 8 way set associative
- block size of 256 words
- 4-byte words
- byte addressable
- LRU Replacement Policy

what part of the addr?			
size (in bits)			

3. Cache Trace

Given the following 2-way set associative cache (8 total blocks), fill in the following table with LRU replacement policy. Show the corresponding cache way (C1 or C2) and the cache index hosting the memory location. In the case of a miss, show the type of miss (cold/compulsory, capacity, conflict) as well.

The processor makes the following 16 accesses to memory location in the order shown:

0, 3, 18, 9, 7, 10, 11, 3, 10, 7, 8, 0, 10, 2, 18, 6

Assume the following initial configuration of the cache:

Index	C1	C2
0	0	--
1	1	--
2	2	--
3	3	--

The first access has been completed for you.

ref	Memory Location	C1	C2	Hit/Miss	Type of miss
	0	**Index = 0**	**--**	**Hit**	**--**
1	**3**				
2	**18**				
3	**9**				
4	**7**				
5	**10**				
6	**11**				
7	**3**				
8	**10**				
9	**7**				
10	**8**				
11	**0**				
12	**10**				
13	**2**				
14	**18**				
15	**6**				