**Logo

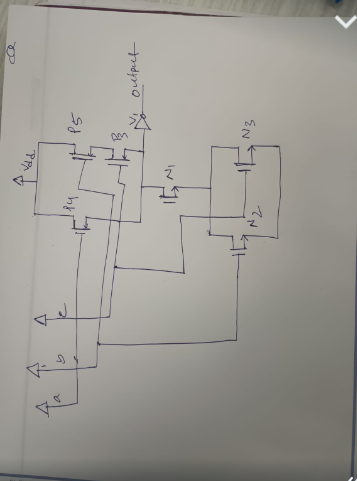
Description automatically generated San Francisco Bay University**

**EE461L - Digital Design and HDL Lab**

**Quiz #1**

**Student Name: Student ID:**

1. **Design the module for a combinational gate by using *MOS* primitives based on the following logic expression, and then write the testbench to verify it.** 
   1. **Draw the circuit schematic in *cmos* and *pmos* first.**
   2. **Write the Verilog module according to the above circuit.**
   3. **Create the testbench to verify it and show the waveforms.**



**Design:**

module comb\_gate (a, b, c, out);

input a, b, c;

output reg out;

wire not\_a, b\_and\_c;

not n0 (a, not\_a);

nmos n1 (b, c, b\_and\_c);

pmos p1 (b, c, b\_and\_c);

nmos n2 (b\_and\_c, a, out);

pmos p2 (not\_a, out, vdd);

endmodule

**module tb();**

reg a, b, c;

wire out;

comb\_gate cmospmos(.a(a), .b(b), .c(c), .out(out));

initial begin

$dumpfile("dump.vcd");

$dumpvars(2);

a = 0; b = 0; c = 0;

#10 $display("a=%b, b=%b, c=%b, out=%b", a, b, c, out);

a = 0; b = 0; c = 1;

#10 $display("a=%b, b=%b, c=%b, out=%b", a, b, c, out);

a = 0; b = 1; c = 0;

#10 $display("a=%b, b=%b, c=%b, out=%b", a, b, c, out);

a = 0; b = 1; c = 1;

#10 $display("a=%b, b=%b, c=%b, out=%b", a, b, c, out);

a = 1; b = 0; c = 0;

#10 $display("a=%b, b=%b, c=%b, out=%b", a, b, c, out);

a = 1; b = 0; c = 1;

#10 $display("a=%b, b=%b, c=%b, out=%b", a, b, c, out);

a = 1; b = 1; c = 0;

#10 $display("a=%b, b=%b, c=%b, out=%b", a, b, c, out);

a = 1; b = 1; c = 1;

#10 $display("a=%b, b=%b, c=%b, out=%b", a, b, c, out);

#100 $finish;

end

endmodule